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Chapter 4, Ex 16, 18, 20

#4 Input

#16 with bit addressing, you can change bits without effecting other bits

#18 SBI DDRB, 2
SBI DDRB, 5
L1: SBI PORTB, 2
SBI PORTC, 5
CBI PORTB, 2
CBI PORTB, 5
RJMP L1

#26 CBI DDRB, 5
CBI DDRB, 6
LDI R16, 0xFF
OUT DDRC, R16
LP1: SBIC PINB, 5
RJMP L2
LOW:
LDI R16, 0x55
OUT PORTC, R16
RJMP L1
L2: SBIS PINP, 6
RJMP IS_LOW
LDI R16, 0xAA
OUT PORTC, R16
RJMP L1

Chapter 19 of, e, 226, 240

19 a) 0110 0101 AND 0111 0110 = 0110 0100 = 0x64

c) 1001 0101 AND 0111 0101 = 0101 0101 = 0x55

e) 1100 0101 OR 0001 0010 = 1101 0111 = 0xD7

22 Both

24a) 0 01010110 00110101 C=0 10011010 01001100 = 99h

additional Problems.

#1 DDRx: you use this register the pins for portx.

PORTx: used to enable or disable the pullup registers

Pinx: used to recive data from port pins

#12
```
SBI DDRC,5
CBI DDRC 4
SBI PORTC, 4
LOOP: SBIS PINC, 4
      RJMP TURNLEDOFF
      CBI PORTC, 5
      RJMP LOOP
OFF: SBI PORT, 5
     RJMP LOOP
```

#3 8M Separate Things

#4 c, e, f

#5 a Direct
b Direct
c Register with GPR
d Register with GPR
e Register Indirect

#6 0x10 → 0x200
0x41 → 0x201
48 → 0x202
0b11110000 → 0x203
0xAB → 0x204
0b1000011110 → 0x205

#7 a| valid → PB5
b| Vialid → bit 3 R16
c| valid → bit 0 R21
d| INVALID -

#8 .ORG 0
LDI R16, 0xFF
OUT DDRC, R16
LDI R16, 0xF0
OUT PORTB R16
IN R19, PORT B
LDI R17, 0x00
LDI R14, 9
LOOP:
INC R17
ROR R19

```
DEC R4
BENE LOOP
OUTPORTC R17
```