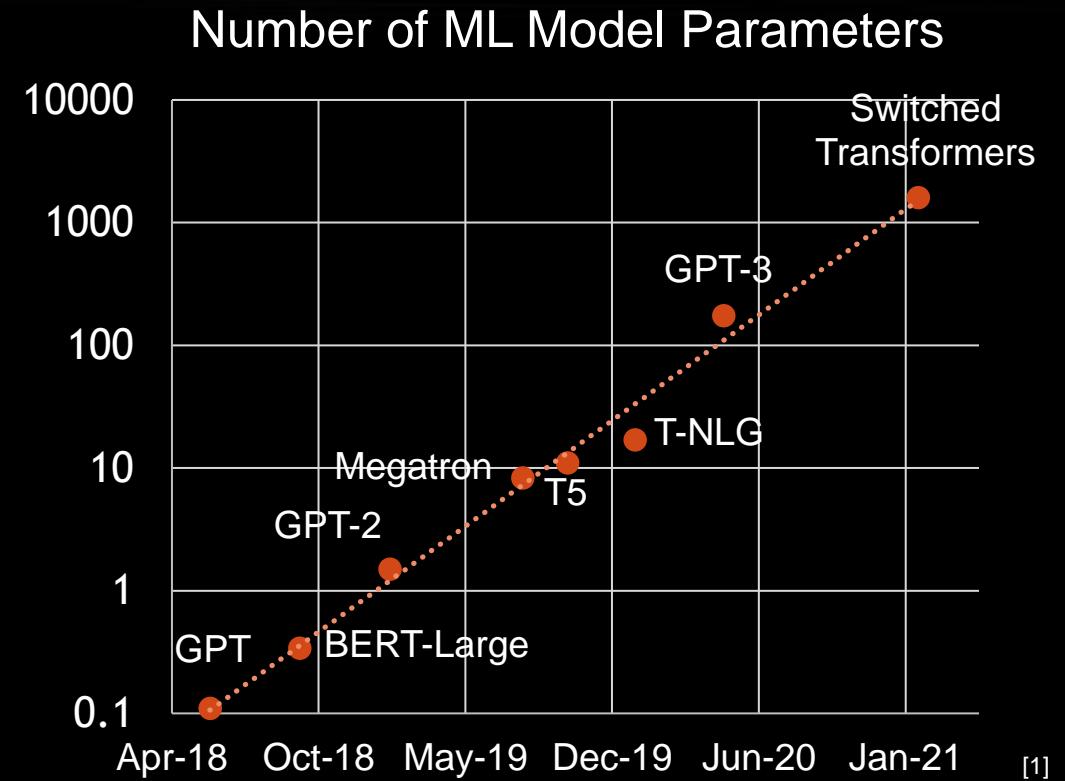
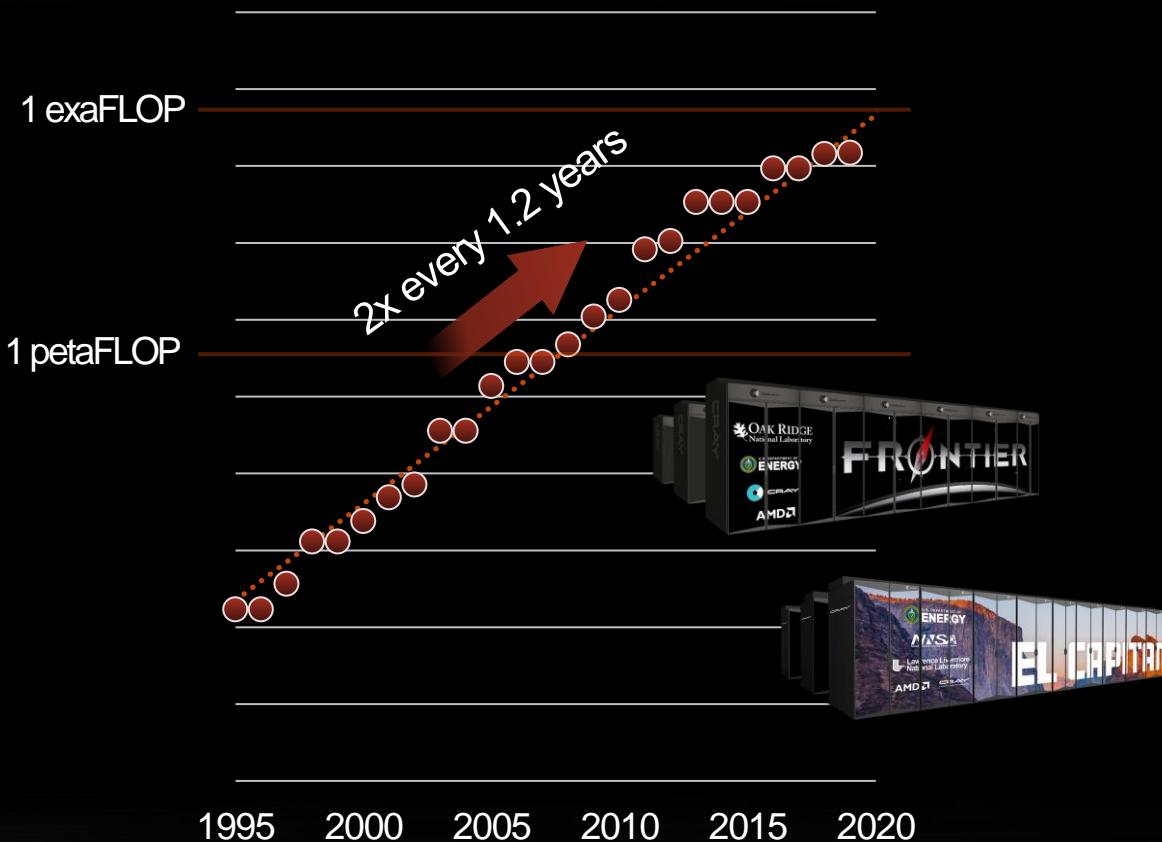




# An Overview of Chiplet Technology for the AMD EPYC™ and Ryzen™ Processor Families

Gabriel Loh  
August 24<sup>th</sup>, 2021  
IEEE SCV – Industry Spotlight

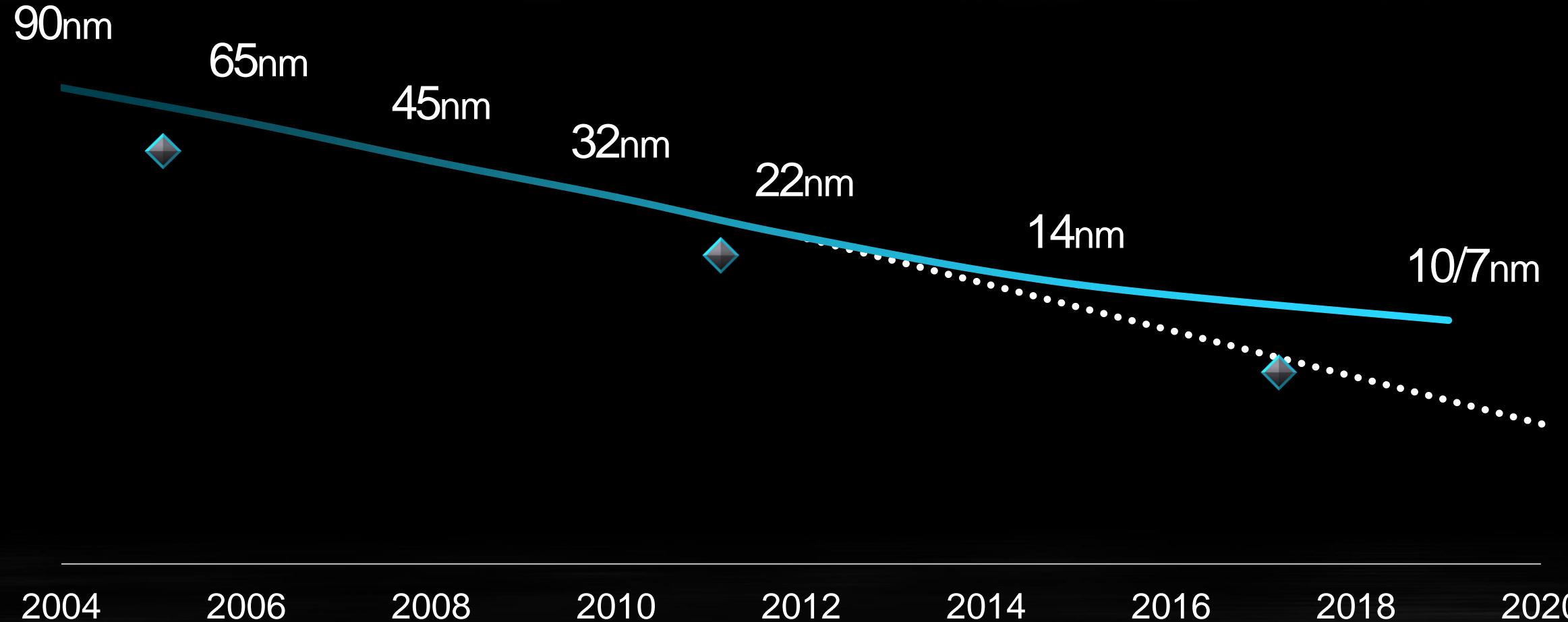
# Insatiable Performance Demands



Required compute doubling every ~3.4 months [2]

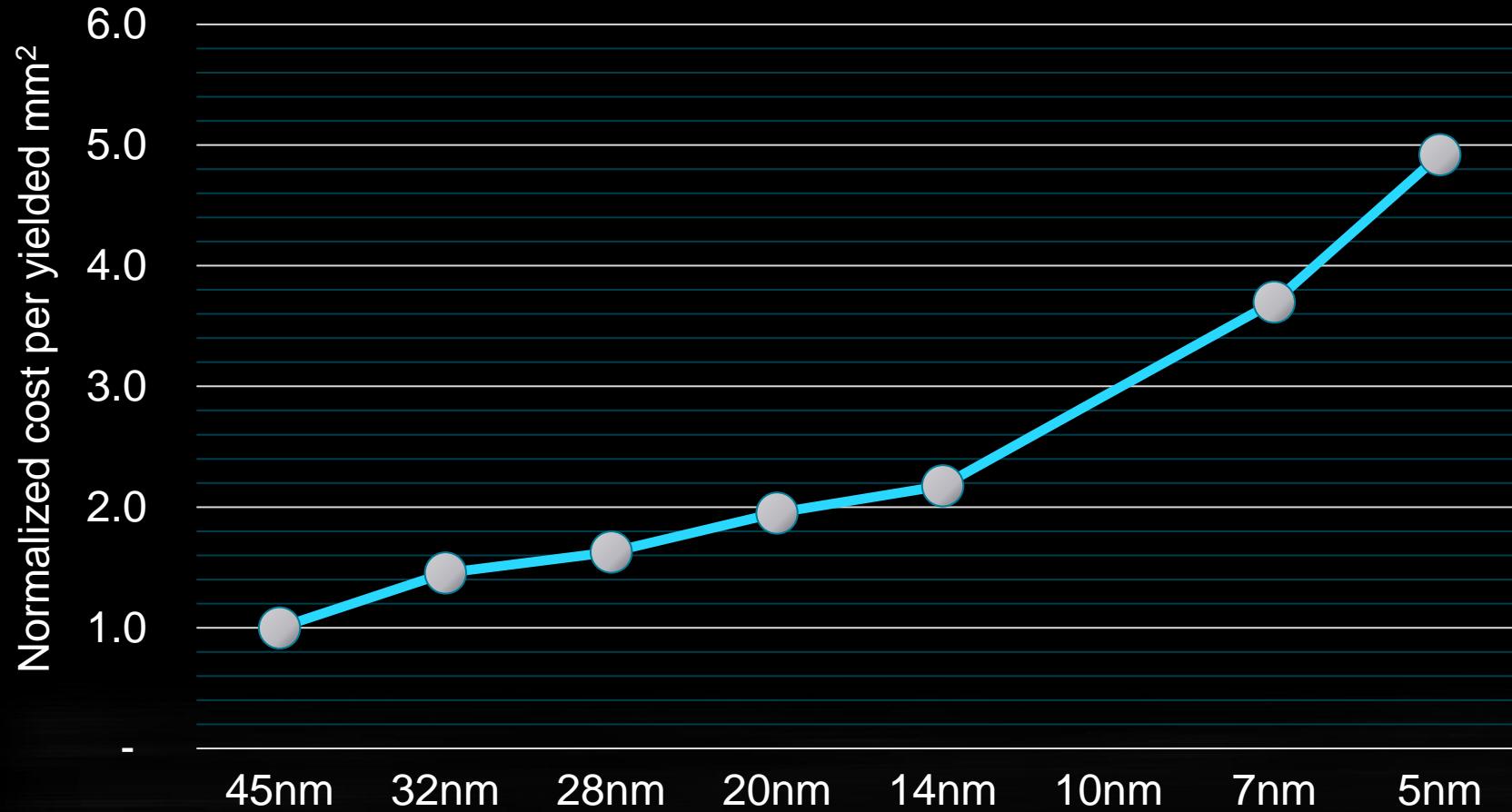
[1] Based on published parameter counts of leading training models. [2] <https://openai.com/blog/ai-and-compute>

# Technology Challenges



# Technology Challenges

Cost Per Yielded mm<sup>2</sup> for a 250mm<sup>2</sup> Die



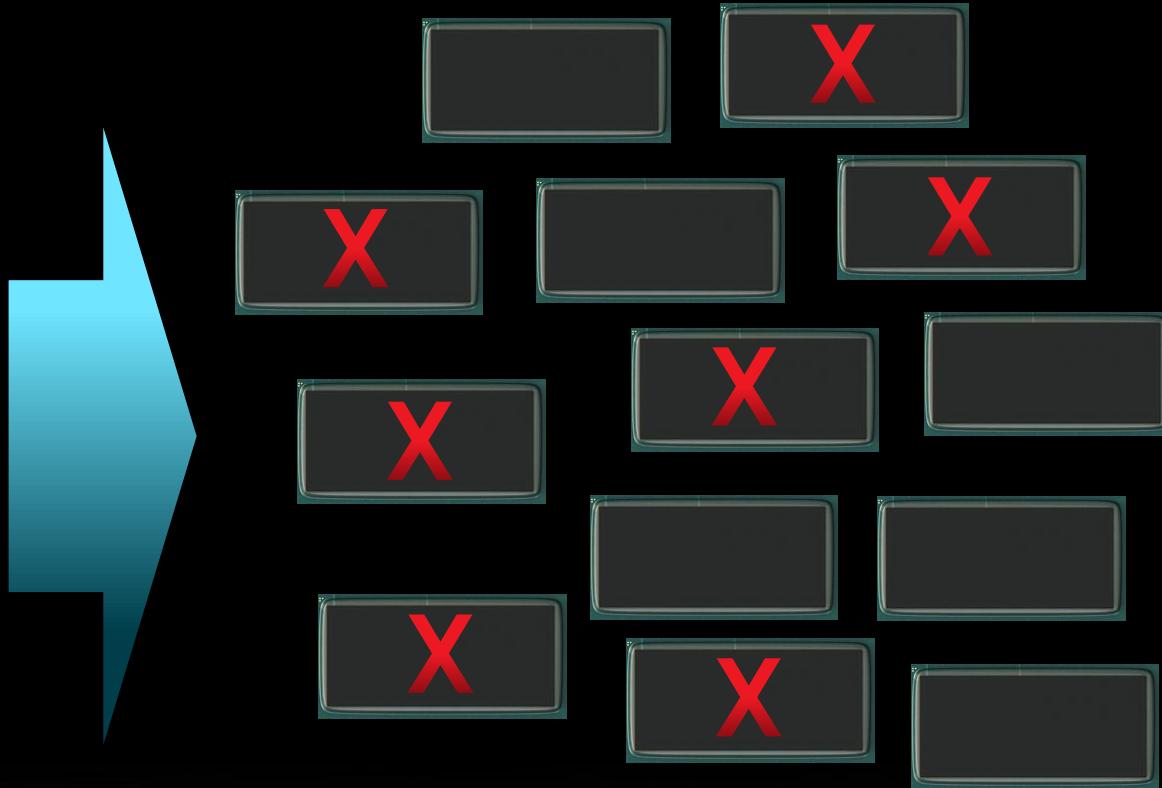
Also...

- ▲ Non-recurring costs per SoC
- ▲ Engineering design
- ▲ Verification
- ▲ Mask sets

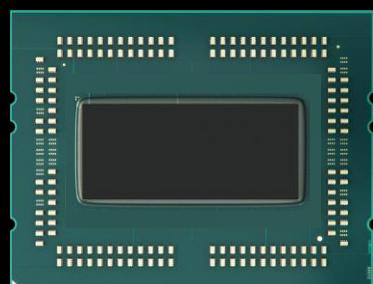
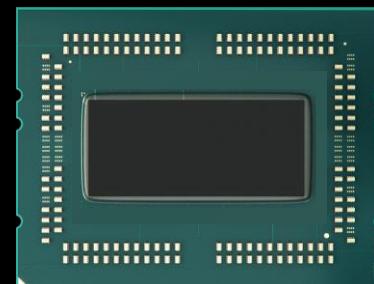
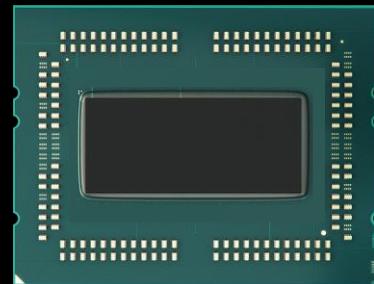
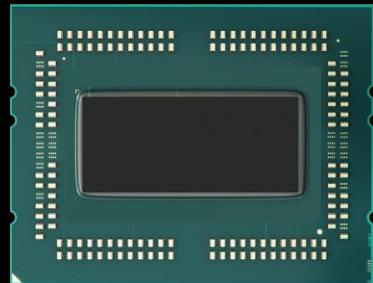
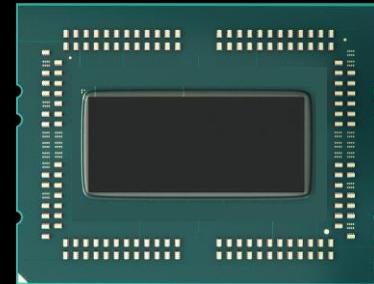
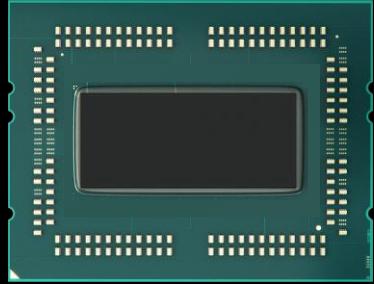
# Monolithic Die Manufacturing



# Monolithic Die Manufacturing



# Monolithic Die Manufacturing

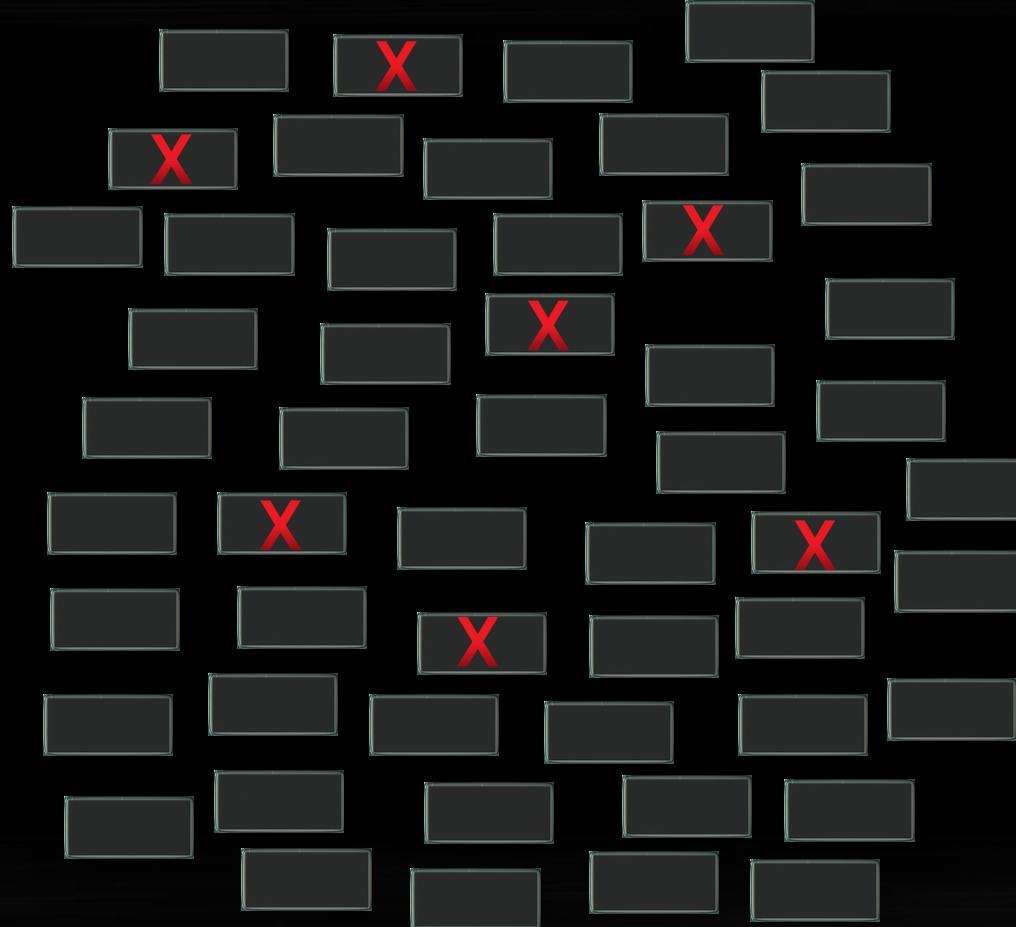


Yielded Processors

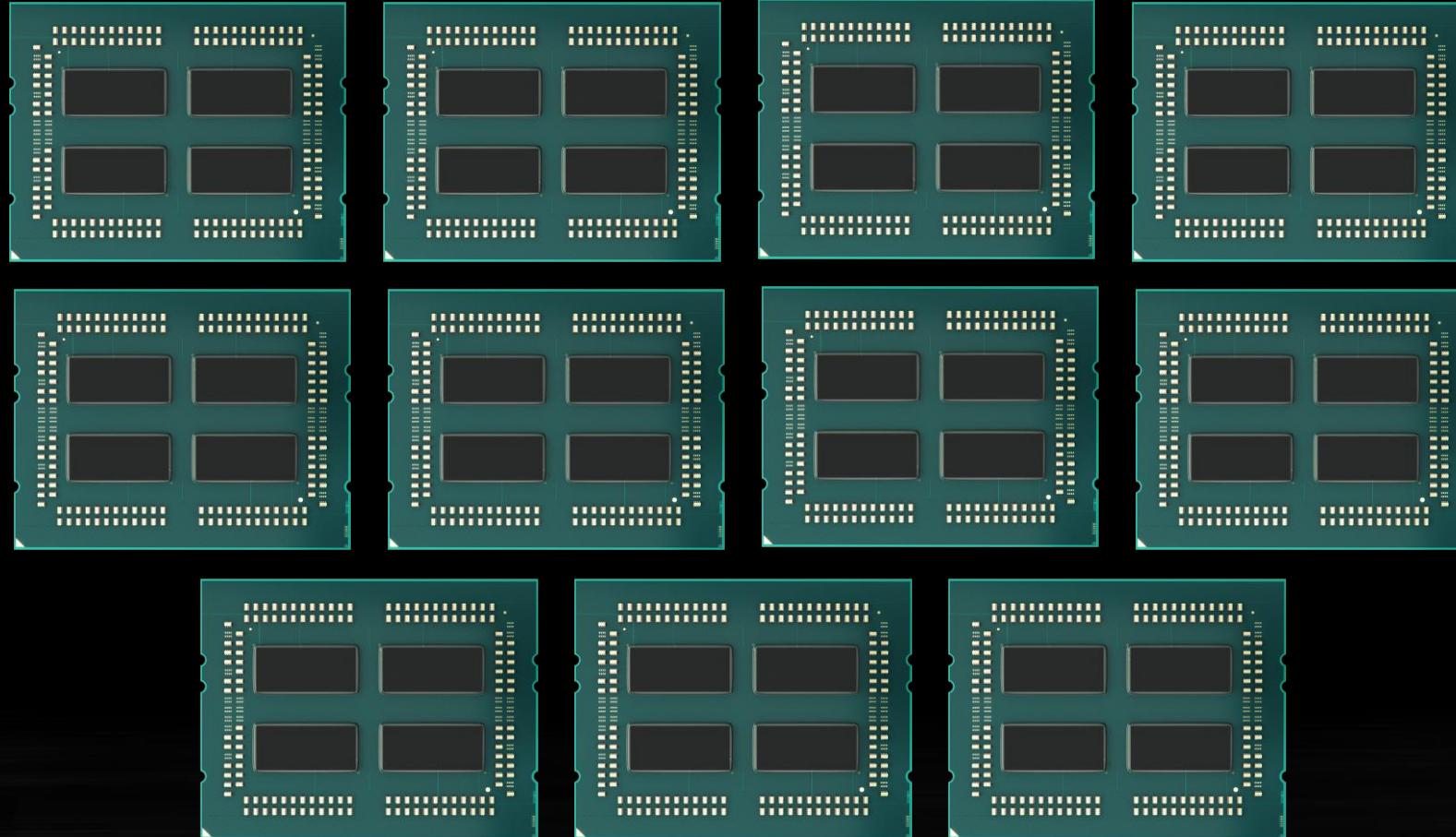
# High-level Chiplets Concept



# High-level Chiplets Concept

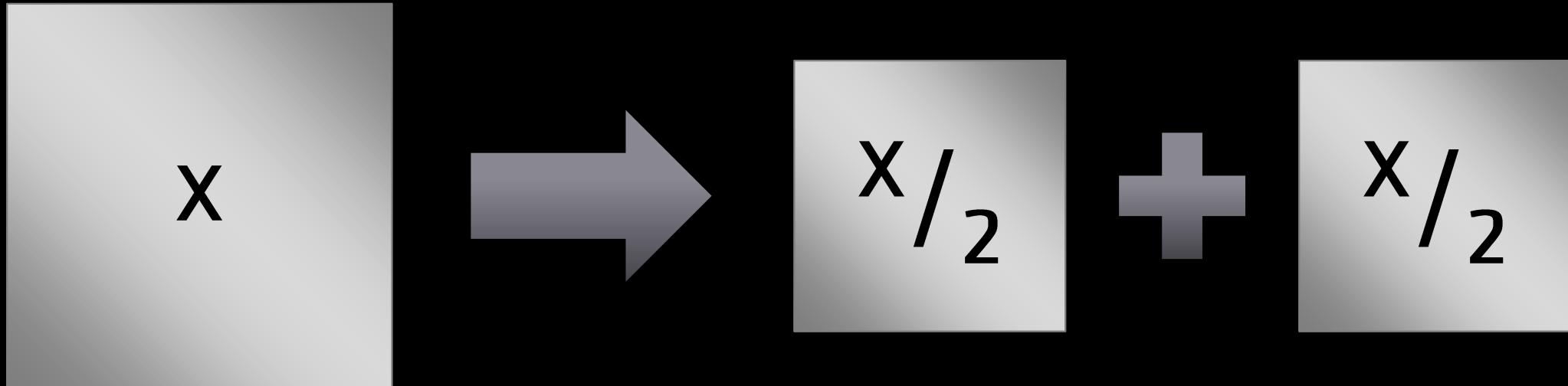


# High-level Chiplets Concept



**More Yielded Processors**

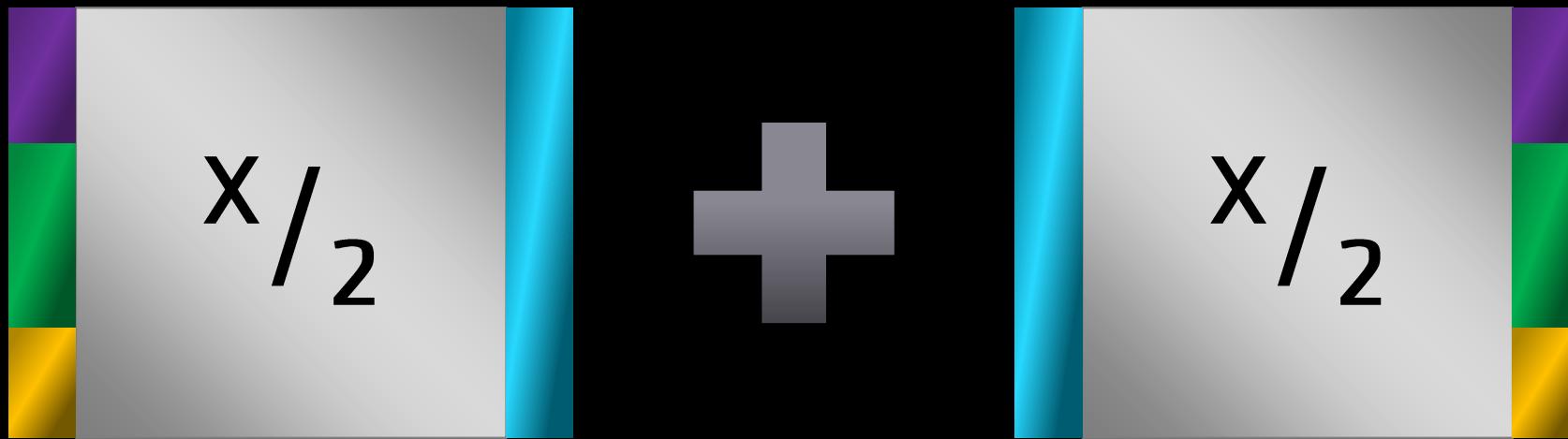
# Chiplet Cost



**Silicon cost is non-linear  
with die area**

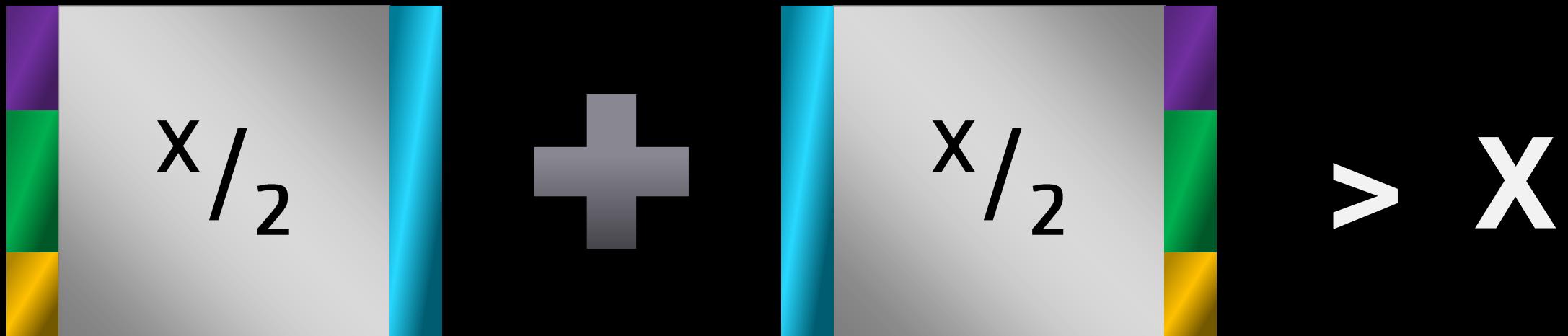
# Chiplet Overheads

- ▲ Inter-chiplet communication interfaces
- ▲ Per-die functionality



# Chiplet Overheads

- ▲ Inter-chiplet communication interfaces
- ▲ Per-die functionality
- ▲ Architectural design effort, partitioning





# Case Study: AMD EPYC™ Processors

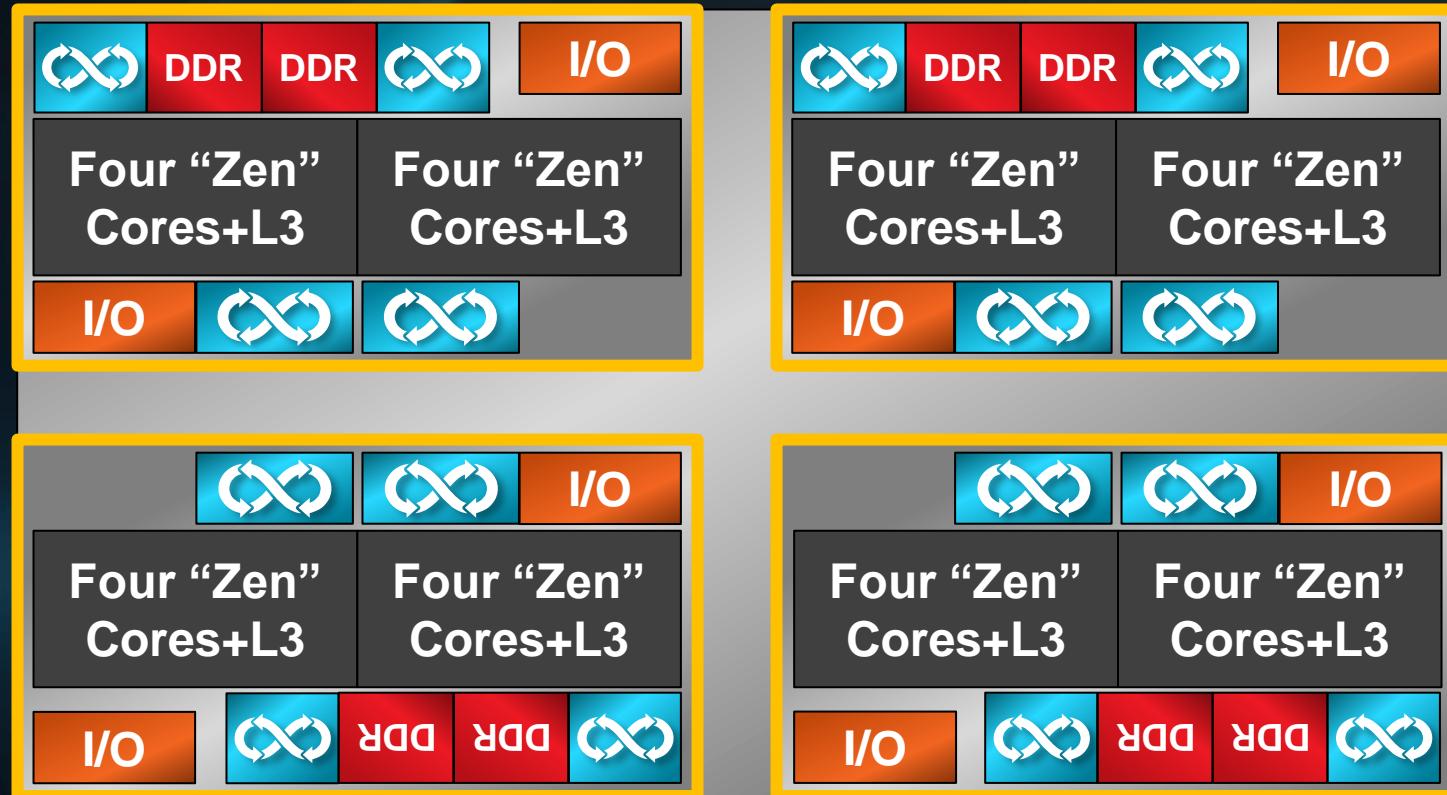
# 1<sup>st</sup>-gen AMD EPYC™ Product Targets



- ▲ Up to 32 "Zen" CPU cores
- ▲ Eight DDR4 memory channels
- ▲ 128 lanes PCIe® gen4 I/O

**Monolithic 32-core Chip  
777mm<sup>2</sup> total area in 14nm**

# 1<sup>st</sup>-gen AMD EPYC™ MCM Organization



▲ 213mm<sup>2</sup> per chiplet (14nm)

▲ 4x → 852mm<sup>2</sup> total

+10% silicon area

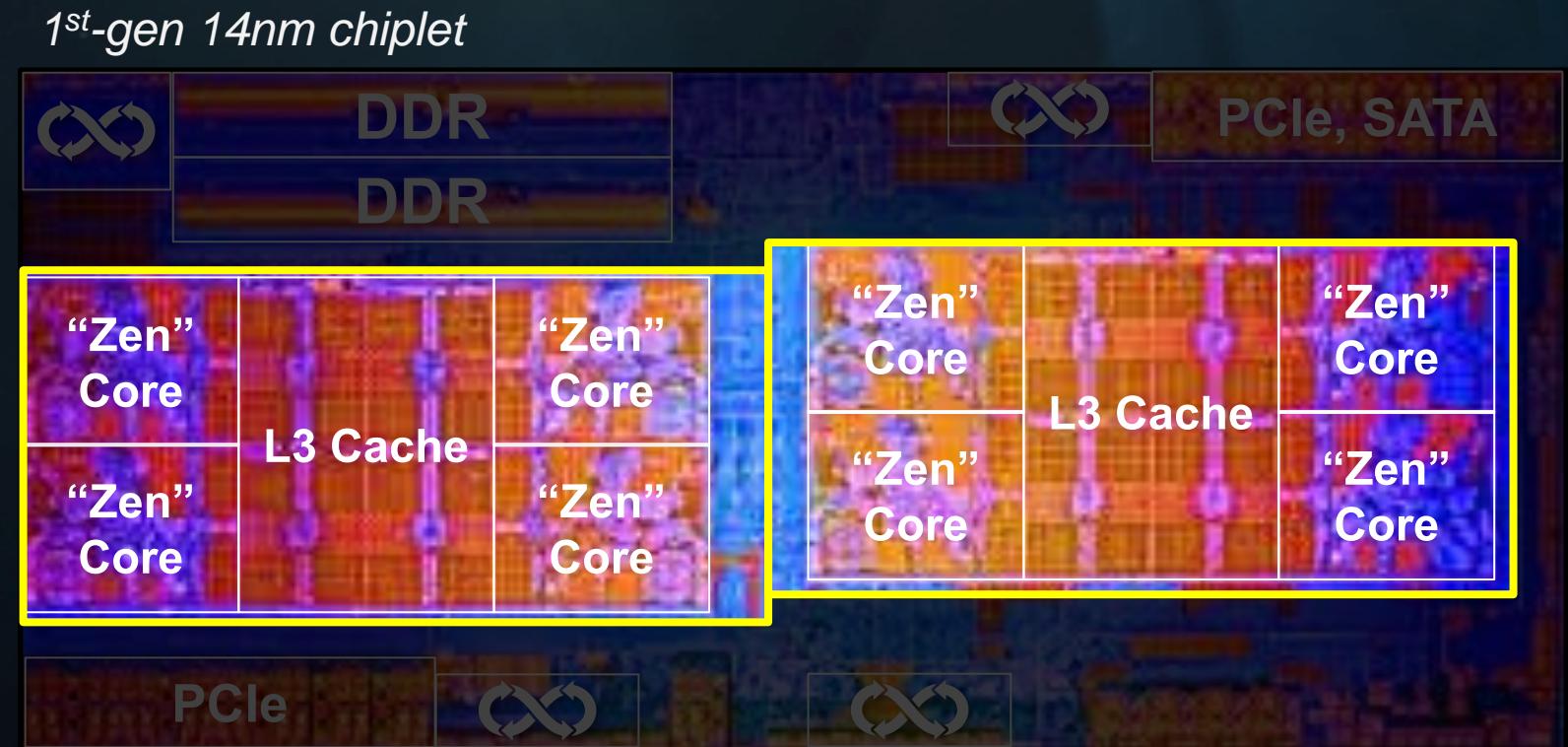
0.59x cost

# Moving to 7nm Technology

2x device density

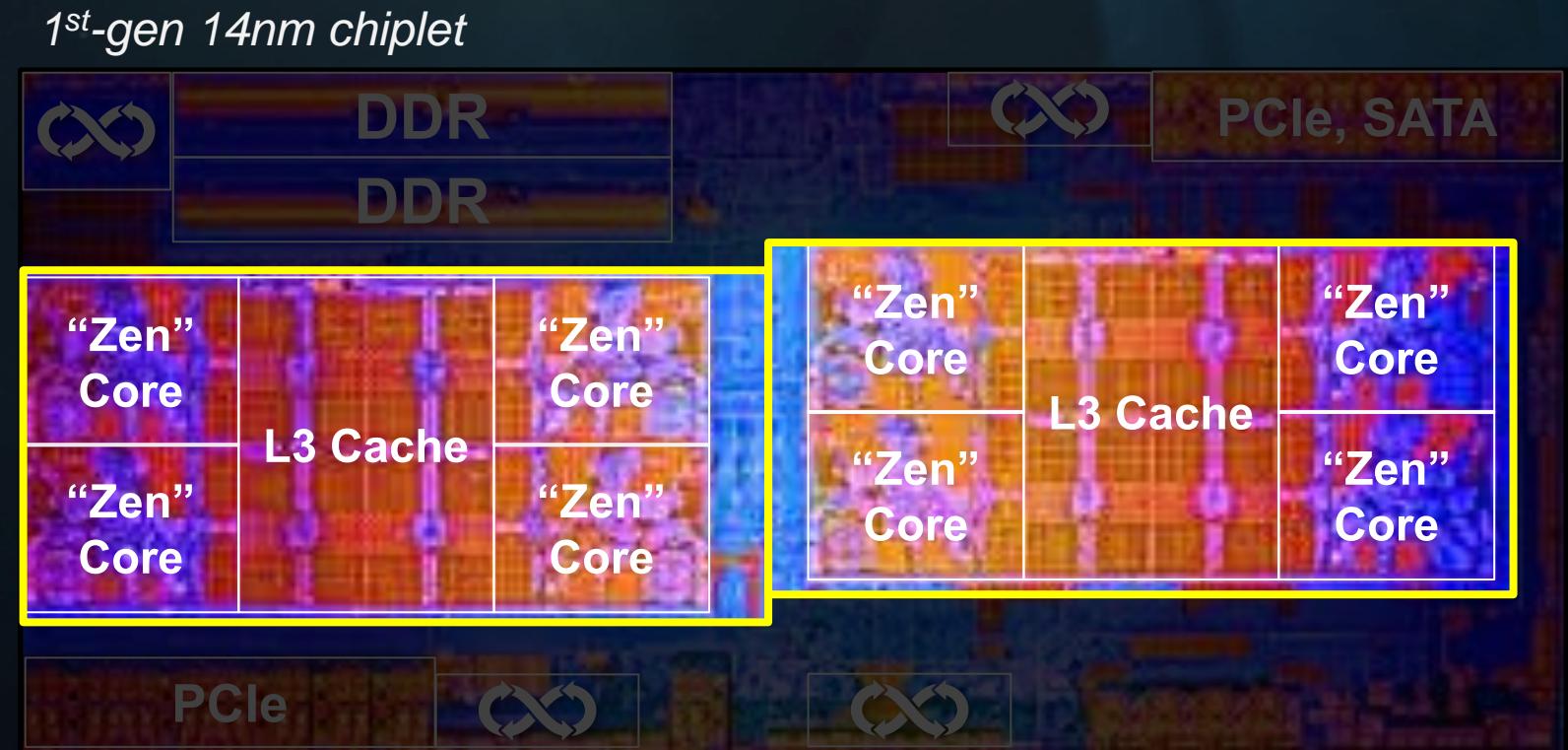
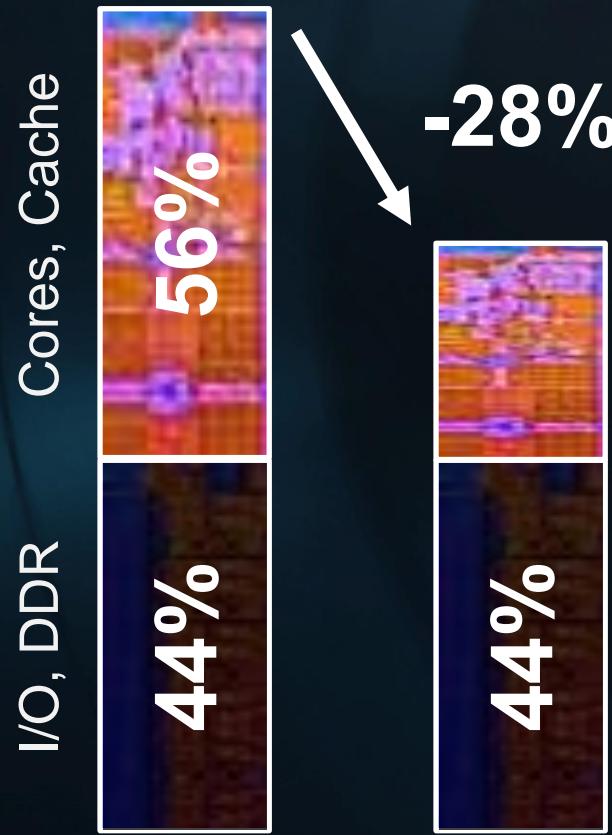
+25% performance  
or  
50% power at 1x perf.

64-core possibility!



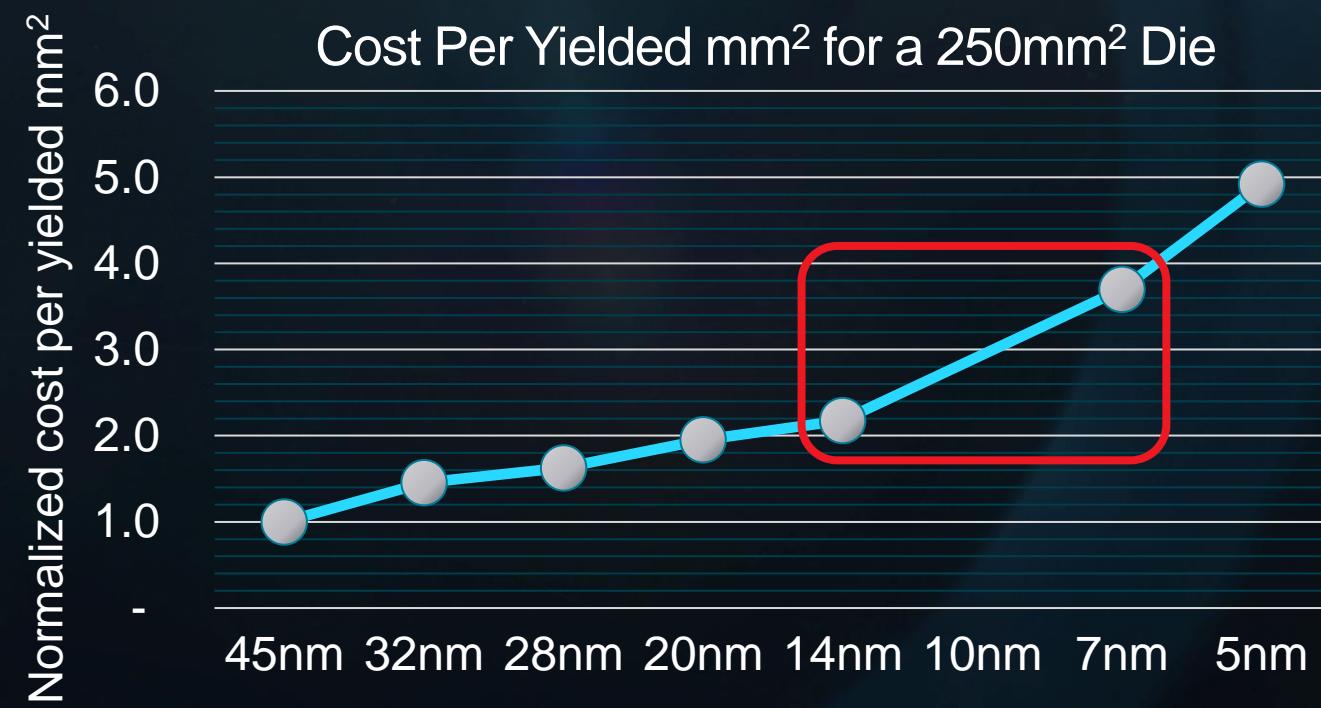
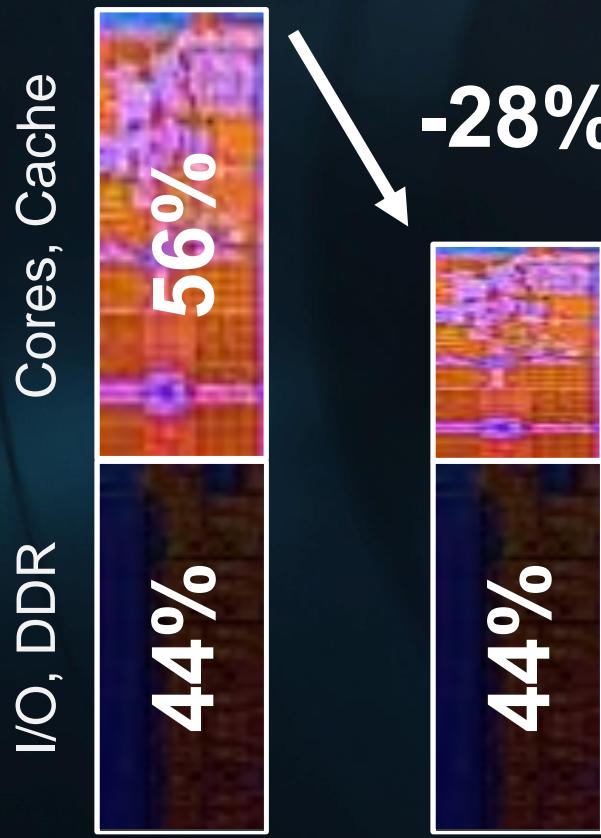
# Moving to 7nm Technology

2x device density

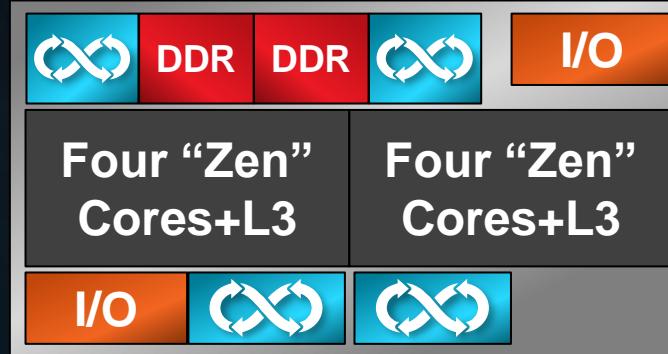


# Moving to 7nm Technology

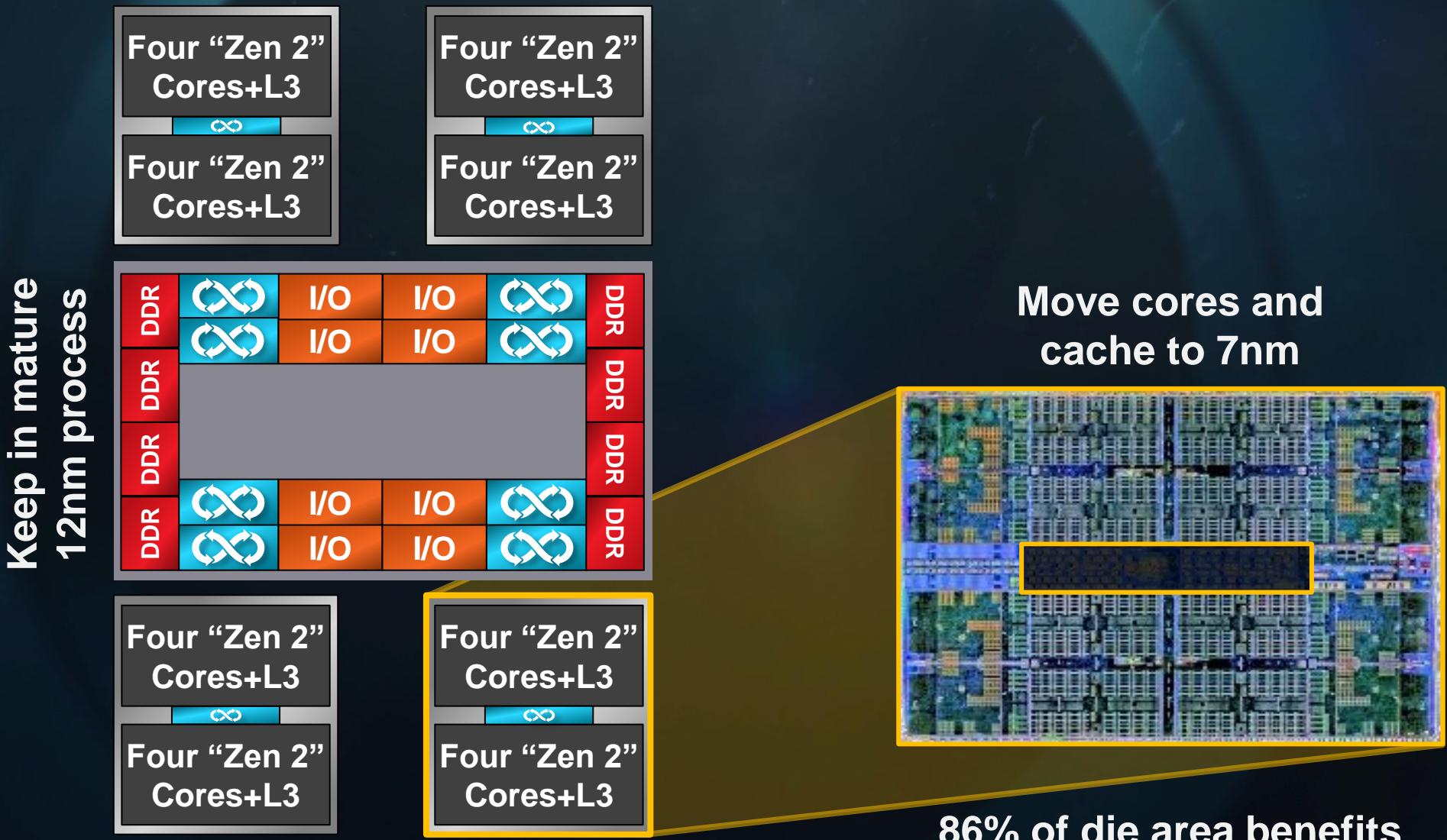
2x device density



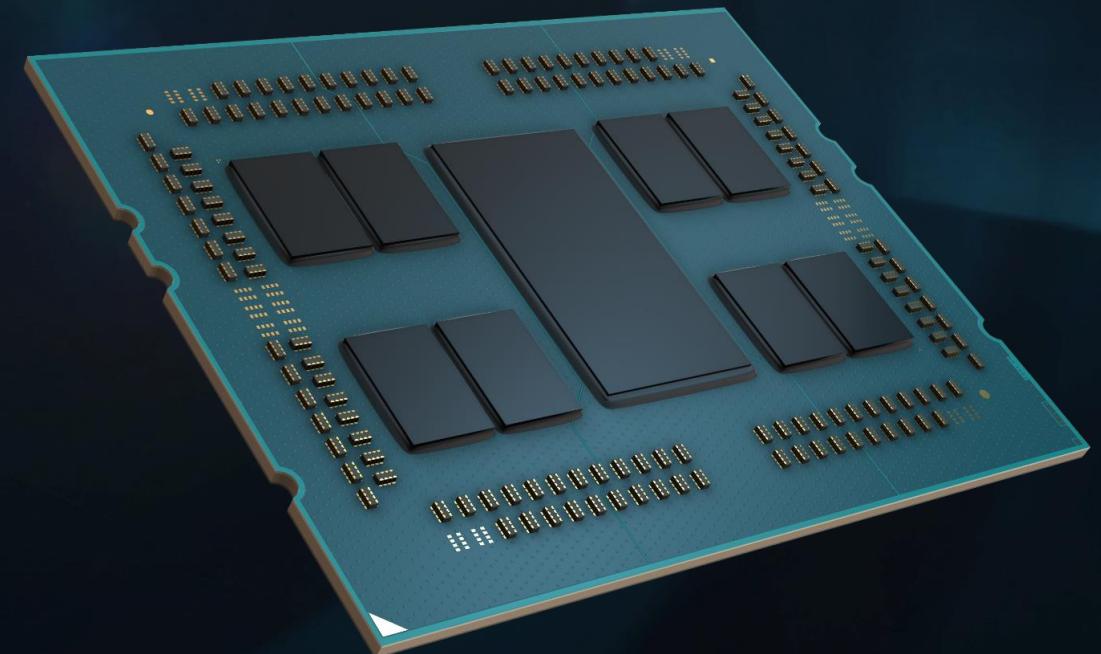
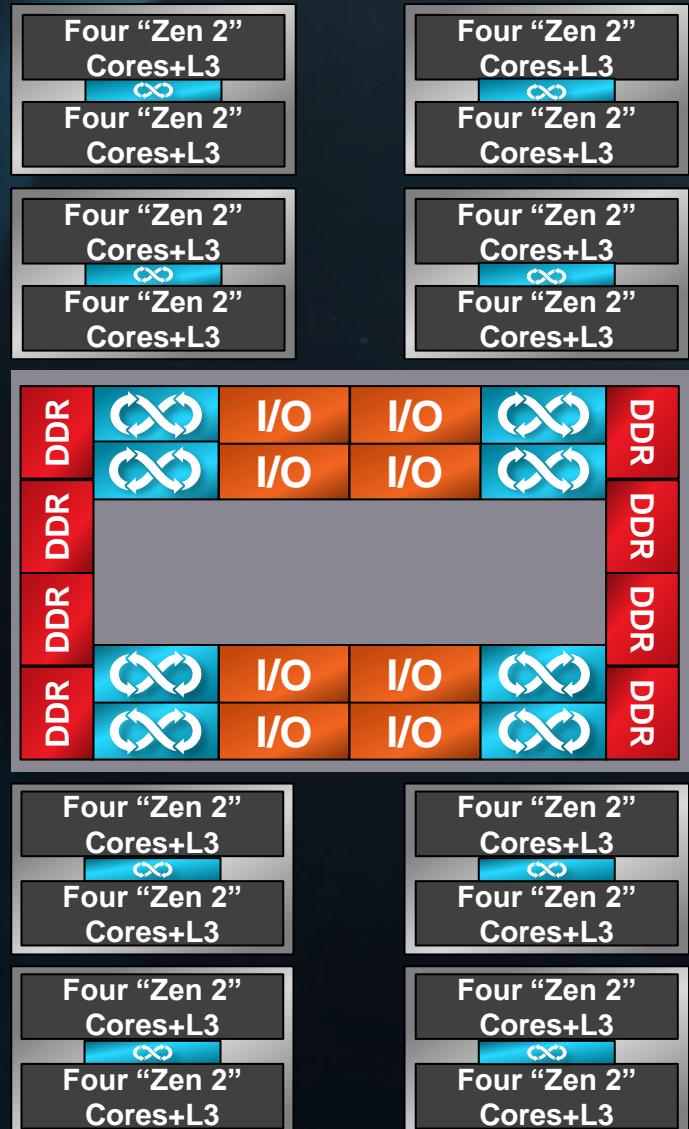
# Technology-optimized Chiplet Organization



# Technology-optimized Chiplet Organization

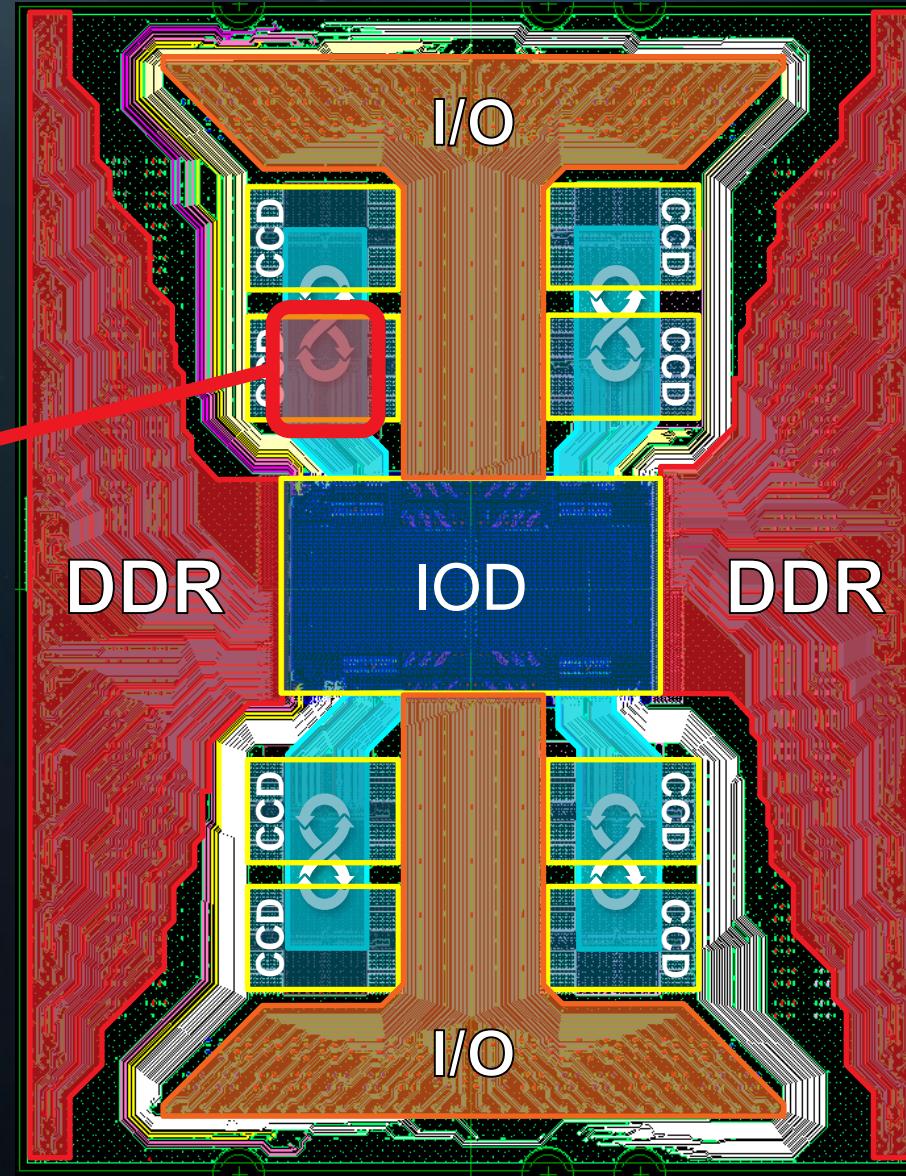


# Technology-optimized Chiplet Organization



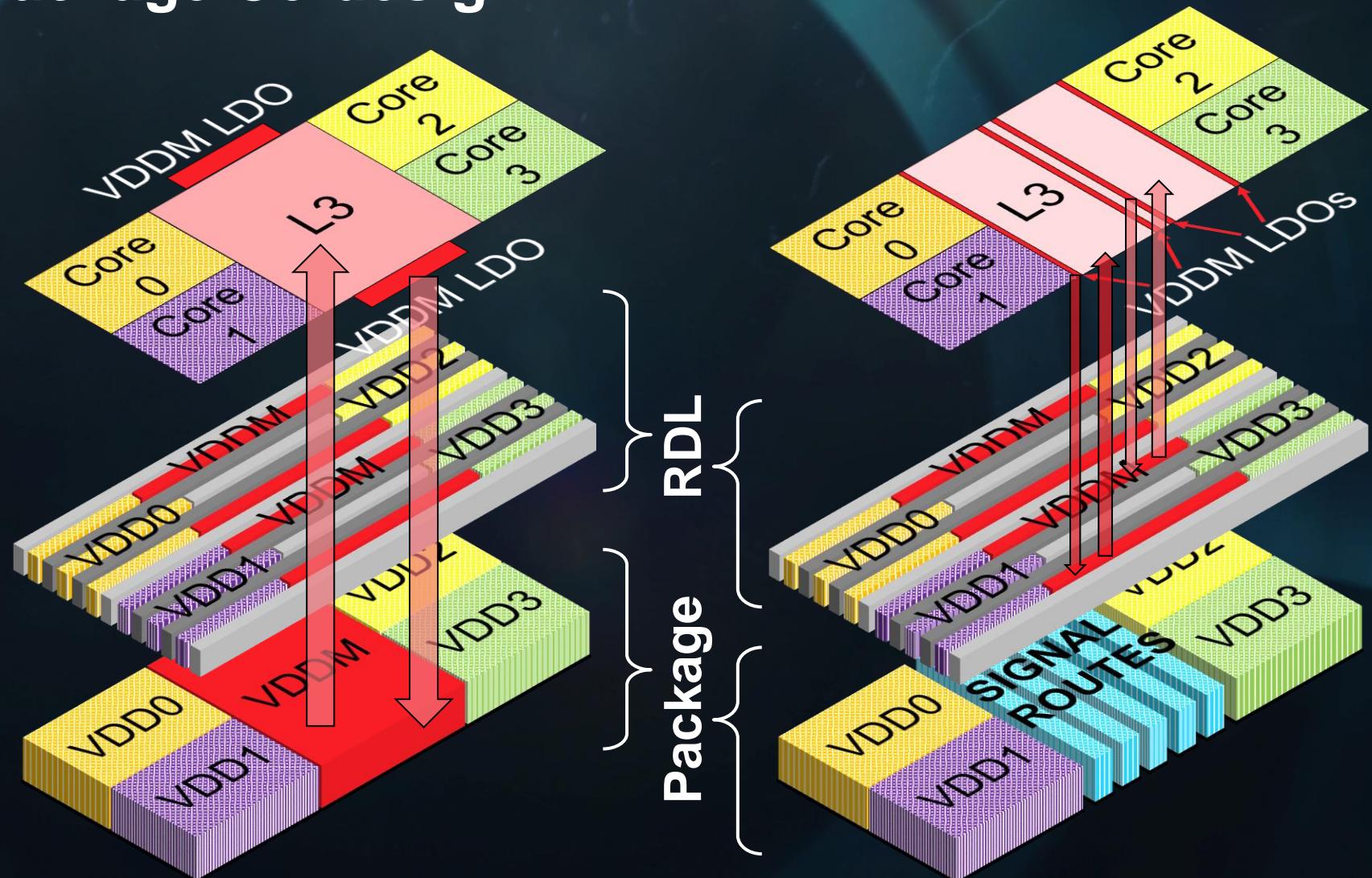
# Packaging Challenges

- ▲ Chiplets can help address silicon challenges, but can also introduce other new challenges to overcome
- ▲ Example: package routing already fully utilized
  - ▲ Package layers in 1<sup>st</sup>-gen processor used for power delivery to CCD

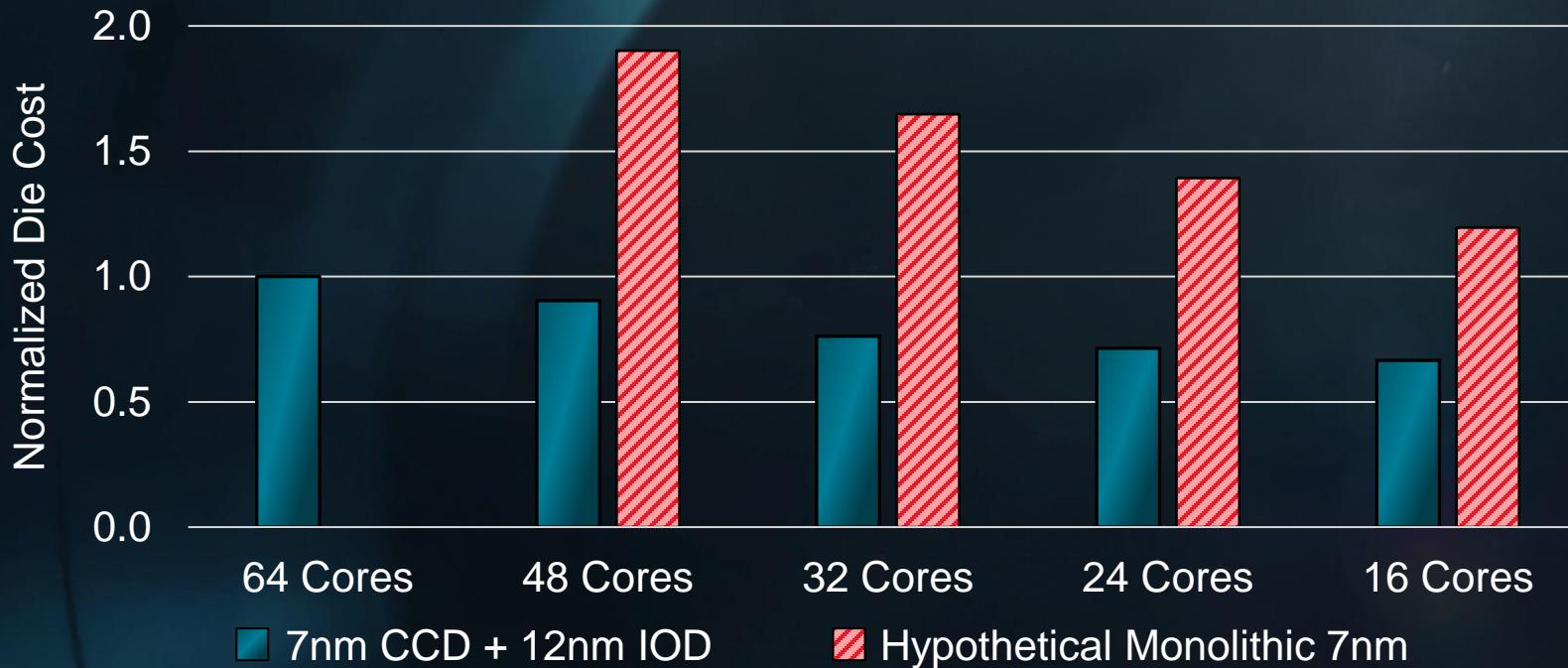


# Solution: Silicon-Package Co-design

- ▲ Metal resources below chiplet previously consumed by power distribution
- ▲ Coordinated re-design of both L3 VDDM LDOs and package metal/routing resources enabled solution
- ▲ Solution achieved VDDM IR drop within 10mV
- ▲ Take-away: advanced chiplet design requires an increasingly vertical and multi-domain co-design approach



# 2<sup>nd</sup>-gen AMD EPYC™ Benefits



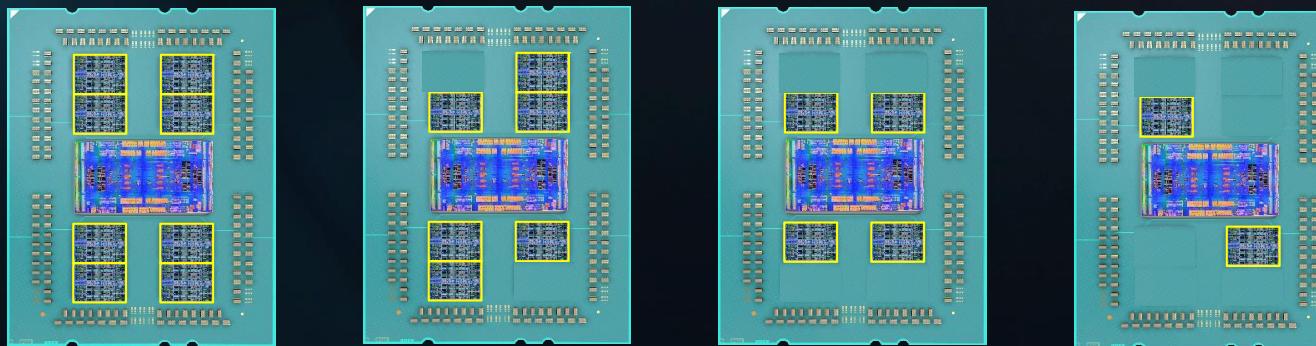
**Great cost benefit vs. monolithic**

**Linear cost with core count**

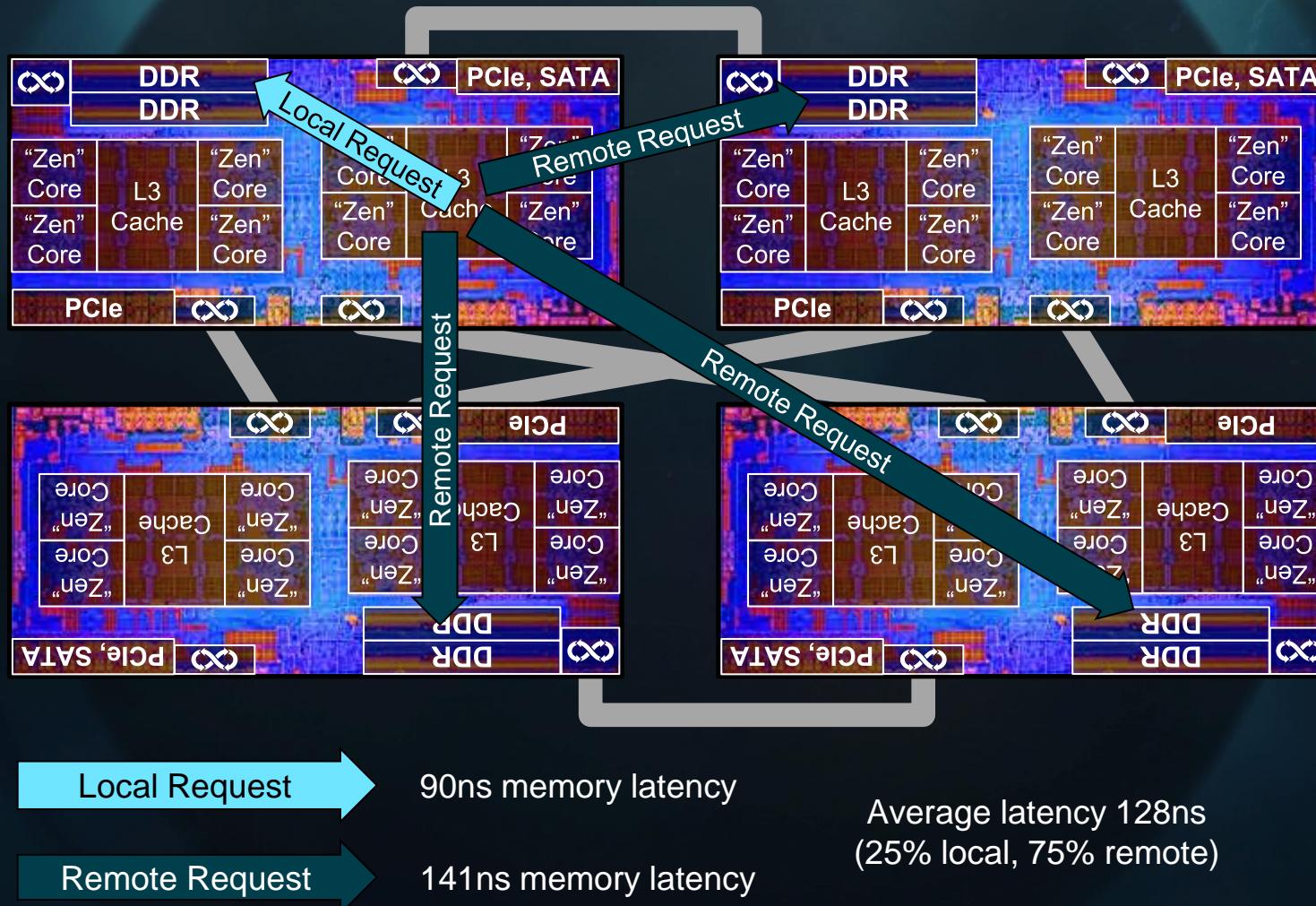
**Makes 64 cores possible**

**Two tape-outs for full stack**

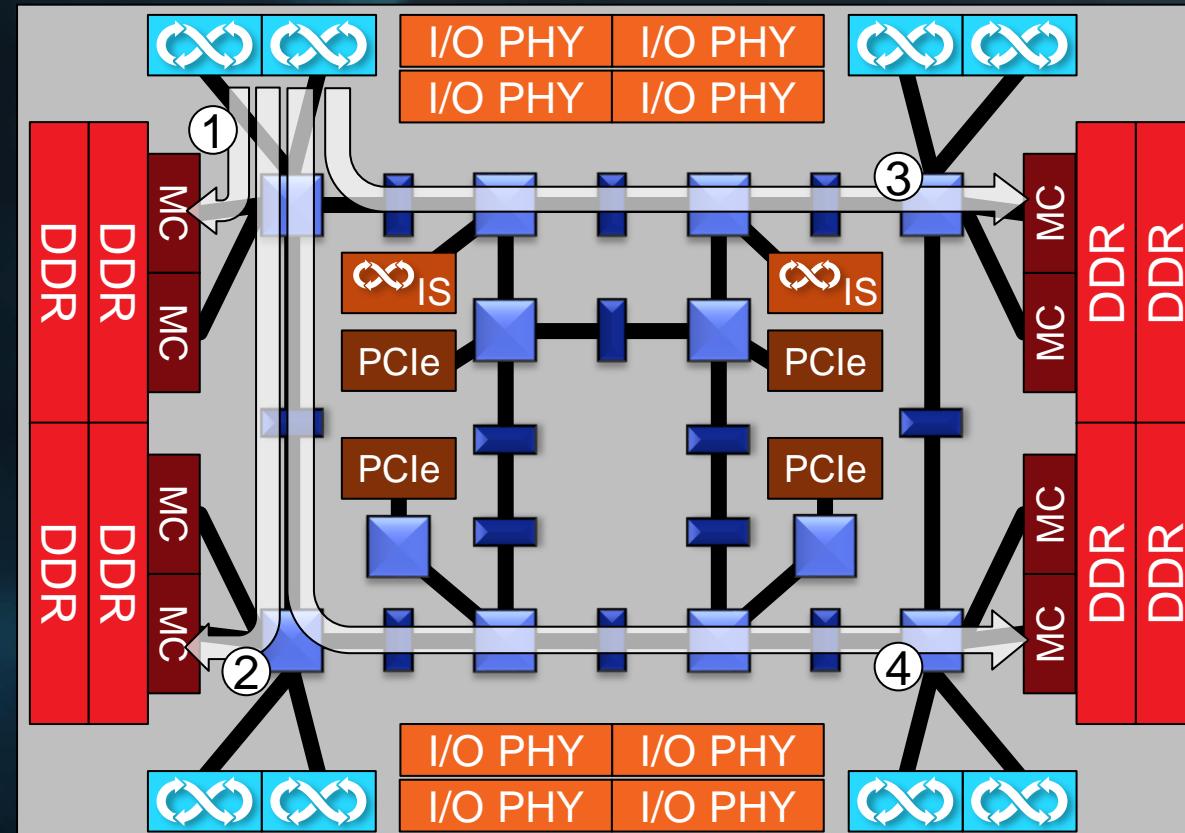
**Full memory and IO**



# Additional Advantages of Technology-optimized Chiplet Organization



# Additional Advantages of Technology-optimized Chiplet Organization



■ Data Fabric switch: 2 FCLK  
(best-case, low load)

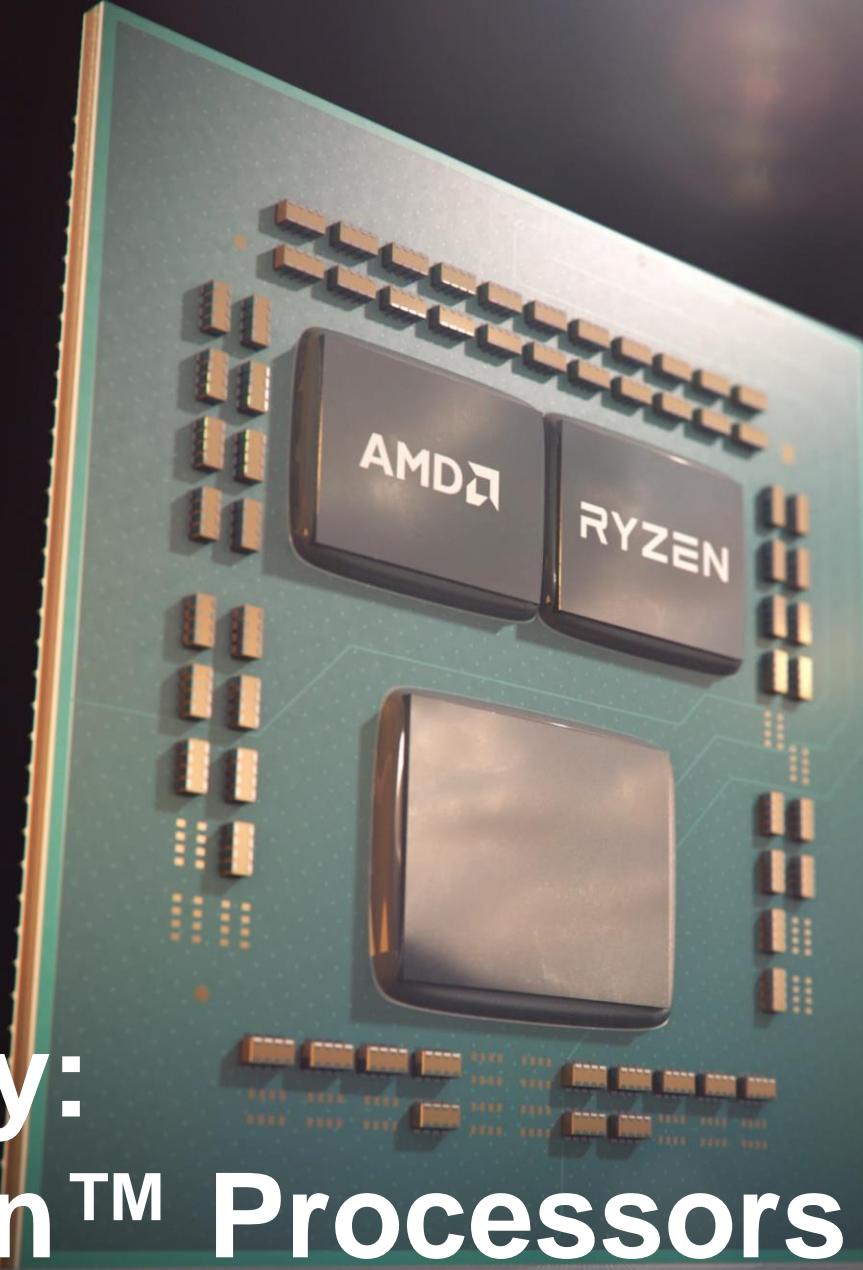
■ Repeater: 1 FCLK

① ~94ns  
② ~97ns  
③ ~104ns  
④ ~114ns } @ FCLK = 1.46 GHz

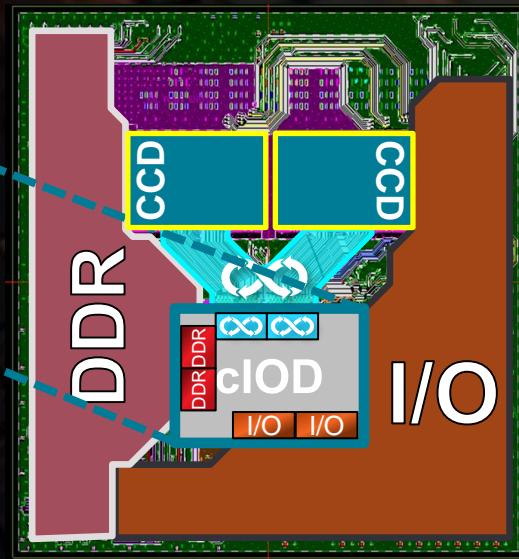
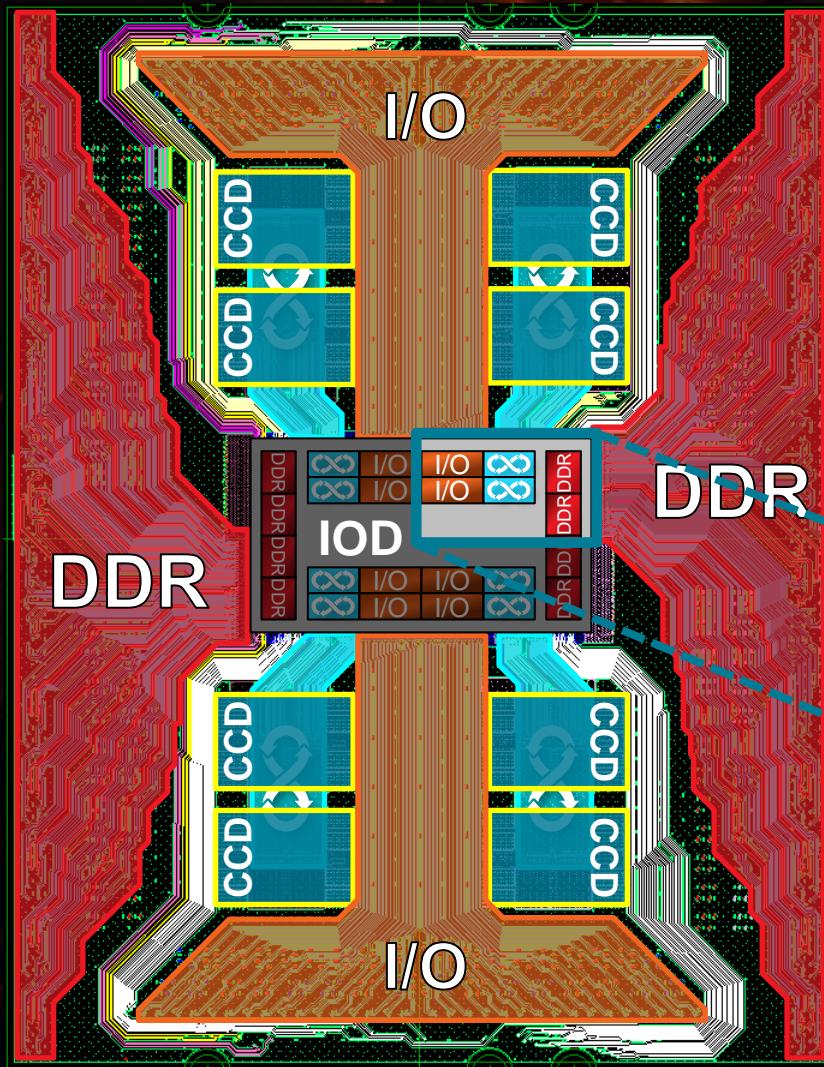
Improvement in Worst-Best case latency  
from 51ns to 20ns

Despite mandatory hop, local  
latency only increases 4ns (90ns → 94ns)

# Case Study: AMD Ryzen™ Processors



# Leveraging Technology Across Markets

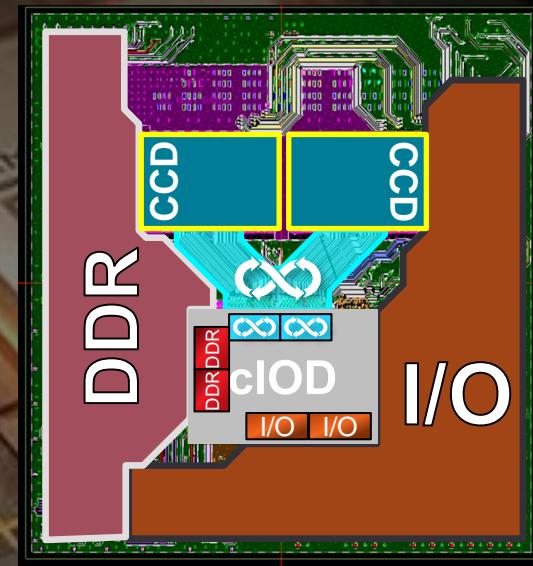
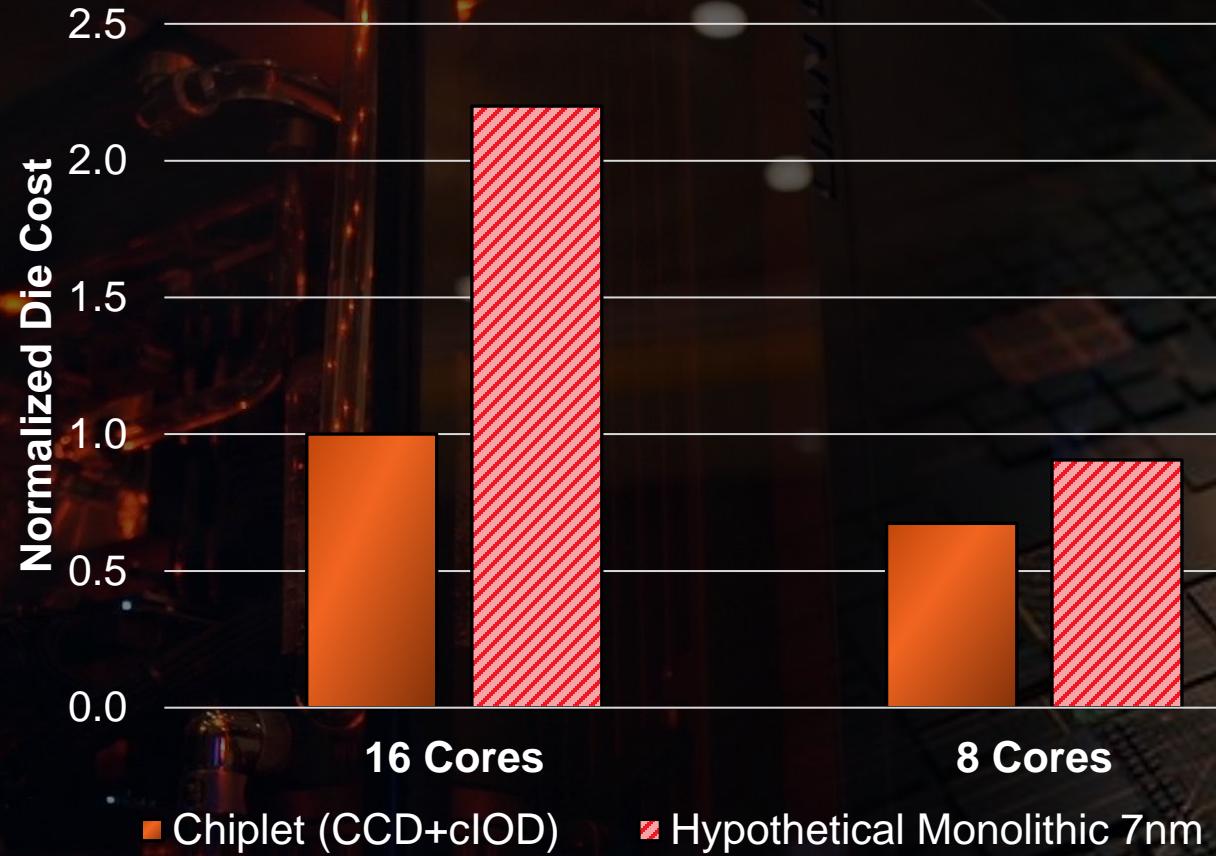


CCD Reuse

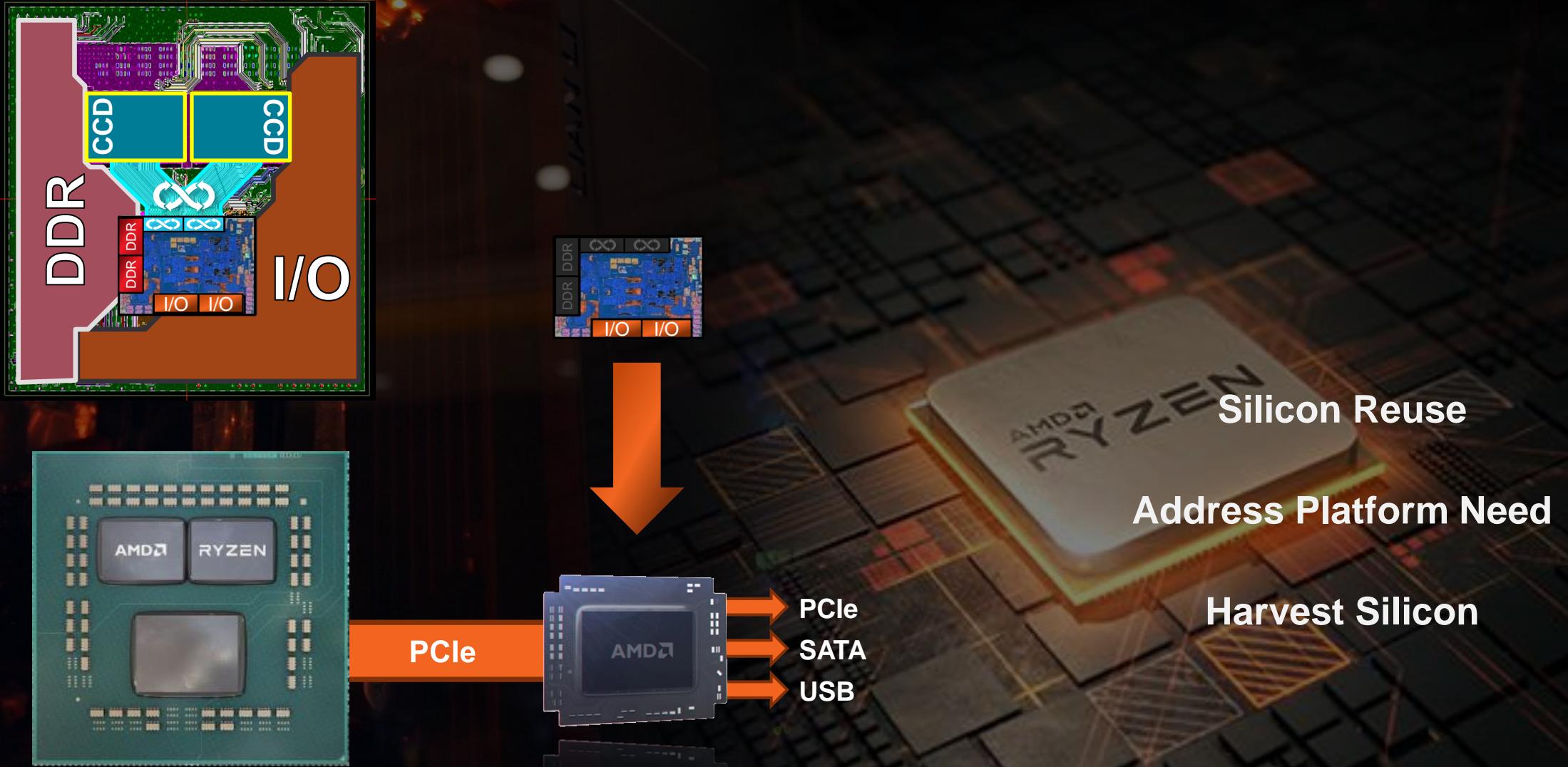
Direct IOD IP leverage

Up to 16-core desktop

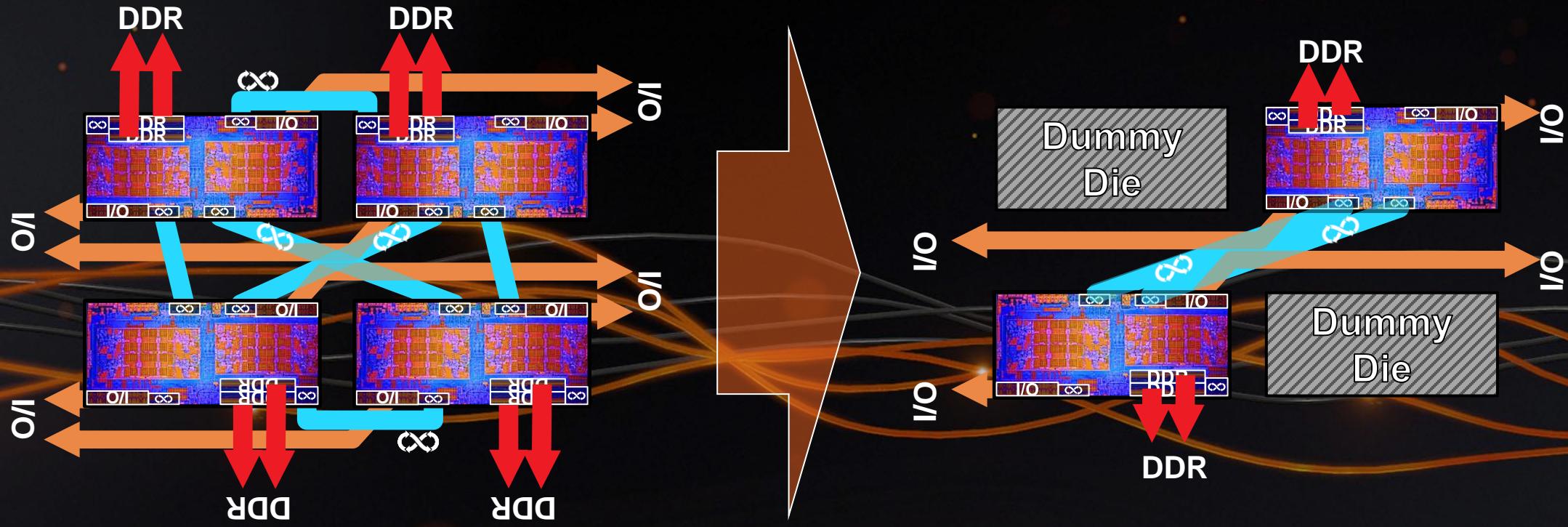
# Chiplet Benefits for AMD Ryzen™ Processors



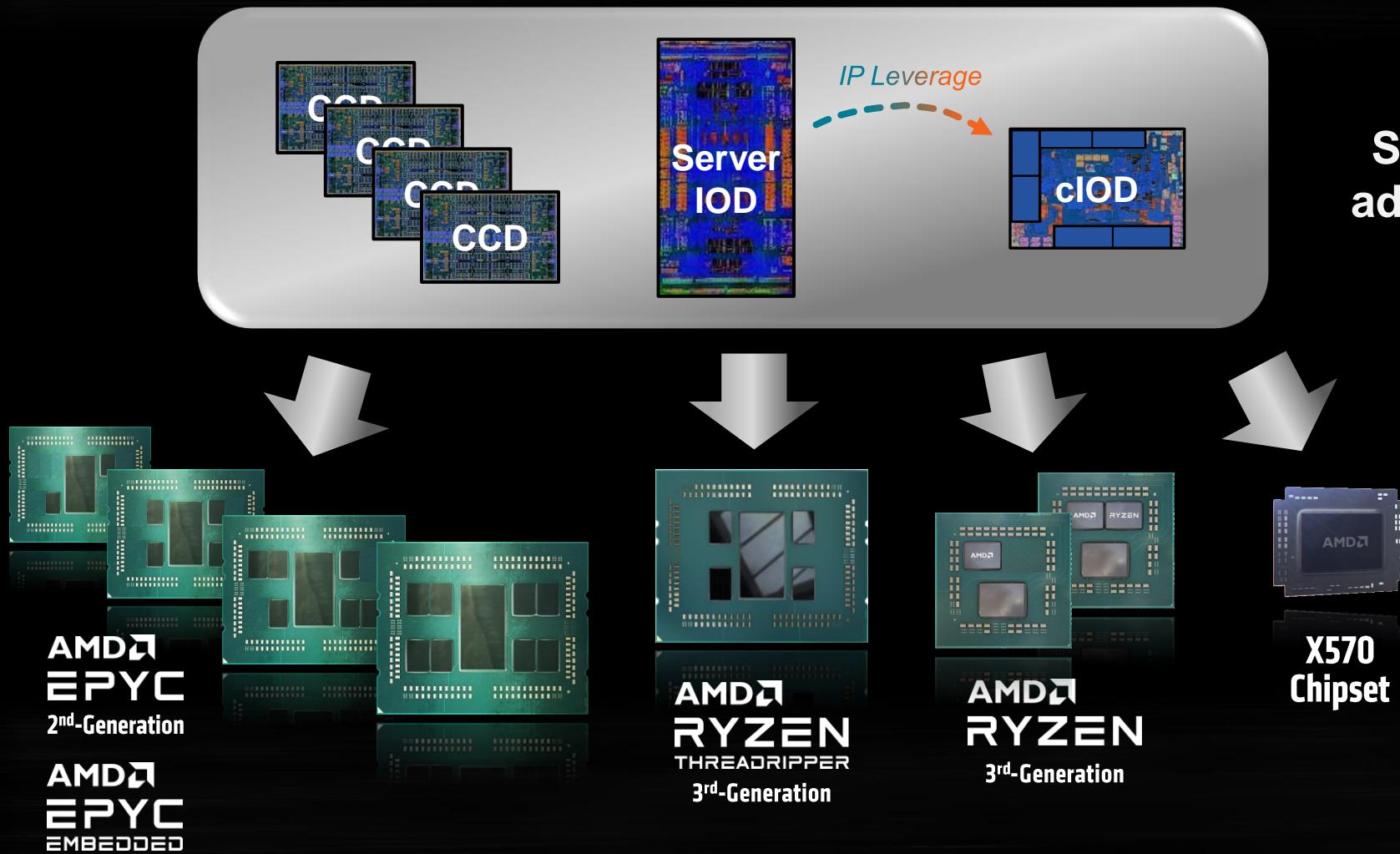
# Further Silicon Leverage



# Silicon Reuse + Package Customization



# Summary



See our ISCA 2021 paper for additional details and insights

**Thanks to the multiple AMD teams  
across the globe**

**Their dedication and hard work are  
what truly breathes life into all of  
our products**

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