

NCKU-ES
Introduction to Digital IC Design
Fall 2017

Lab 3

Design of Arithmetic Logic Unit

Professor:Wen-Long Chin

TA: Cheng-Chieh Chang

、 Chieh-Sheng Cheng

VLSI signal processing LAB

- Objectives

- To learn the basics of behavioral code

- LAB content

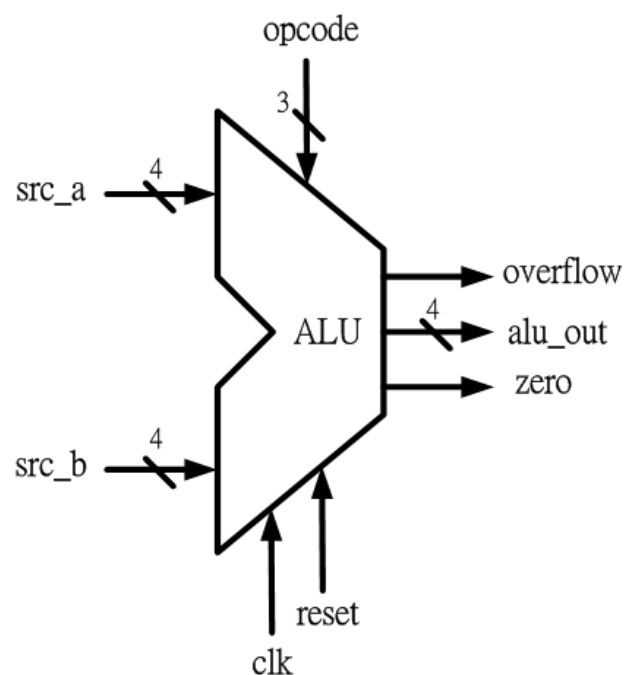
- LAB3: Arithmetic Logic Unit

LAB 3: Arithmetic Logic Unit

● Design Description

- An arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and logical operations.
- Please design an ALU which performs **8** operations.

● Block Diagram



● Specifications

- Top module name : **alu** (File name: alu.v).
- Input pins: src_a[3:0], src_b[3:0], opcode[2:0], clk, reset .
- Output pins: overflow, alu_out[3:0], zero.
- All inputs and outputs are **synchronized** at **clock positive edge**.
- It is a **synchronous-reset** architecture, alu_out becomes 0 when the reset equal to 1.
- Note that src_a, src_b are **signed number**. Overflow detection can refer to the handout.
- The zero bit becomes 1 when the alu_out equal to 0, and 0 otherwise.

- The **overflow bit becomes 1** when the calculation result (alu_out) is greater than what it can represent.

● Functionality

opcode	ALU operation
000	No operation
001	src_a AND src_b
010	src_a OR src_b
011	Pass src_a
100	src_a + src_b
101	src_a - src_b
110	src_a >> src_b (Logic shift right)
111	src_a << src_b (Logic shift left)

➤ Example

opcode	ALU operation example
000 (No operation)	alu_out=4'd0, zero=1'b1, overflow=1'b0
001 (AND)	src_a=4'b0001, src_b=4'b1110 → alu_out=4'b0000, zero=1'b1, overflow=1'b0
010 (OR)	src_a=4'b0001, src_b=4'b1110, → alu_out=4'b1111, zero=1'b0, overflow=1'b0
011 (Pass src_a)	src_a=4'b0001, src_b=4'b1110, → alu_out=4'b0001, zero=1'b0, overflow=1'b0 src_a=4'b0000, src_b=4'b0010, → alu_out=4'b0000, zero=1'b1, overflow=1'b0
100 (+)	src_a=4'b0001, src_b=4'b1001, → alu_out=4'b1010, zero=1'b0, overflow=1'b0 src_a=4'b0111, src_b=4'b0111, → alu_out=4'b1110, zero=1'b0, overflow=1'b1
101 (-)	src_a=4'b0001, src_b=4'b1001, → alu_out=4'b1000, zero=1'b0, overflow=1'b1 src_a=4'b0111, src_b=4'b0011, → alu_out=4'b0100, zero=1'b0, overflow=1'b0
110 (>>)	src_a=4'b0111, src_b=4'b0011, → alu_out=4'b0000, zero=1'b1, overflow=1'b0
111 (<<)	src_a=4'b0111, src_b=4'b0011, → alu_out=4'b1000, zero=1'b0, overflow=1'b0

- Note

- 本次作業提供測試程式(Testbench)，各位同學的作業須能通過測試程式的驗證

- 書面報告需包含

1. 設計原理(Design principle)及架構 (Architecture)
2. 波型(Waveform)分析
3. 通過測試程式的圖

(請詳細描述原理及分析波型)

```
----- ALU check successfully -----
```

```
    $$  
   $ $  
  $ $  
 $ $  
$ $  
$$$$$$$$  $$$$$$$$  
$$$$$$$  $  
$$$$$$$  $  
$$$$$$$  $  
$$$$$$$  $  
$$$$$$$  $  
$$$$$$$$$$$  $  
$$$$$  $$$$$$$$$$  
Simulation complete via $finish(1) at time 1 US + 0  
./testfixture_stu.v:143 $finish ;  
ncsim> exit  
[art@localhost lab3]$
```

- 書面報告請勿手寫

- 評分標準依是否達到題目要求各事項，未達到要求依項扣分。

1. 功能驗證：75%
2. 書面報告：25%

- 繳交的作業資料夾組織與命名請與下頁圖示相同

- 作業繳交至 Moodle

- 上傳截止日期: **2017/11/8(三) 23:55**

請務必於上傳截止日期前繳交作業

- Directory Organization

