VLSI Questions

Compilation of previous year questions and internal papers

([S] -> Supply exam, [I] -> Internal)

Module 1

	Question	asked in
1	Describe the process steps of n-well CMOS fabrication with neat sketches	2022
2	Describe the process steps of p-well CMOS fabrication with neat sketches	2025[I]
3	Explain the process steps involved in the nMOS fabrication with neat sketches.	2022 2025[I]
4	Explain CMOS IC fabrication technology in detail.	2022[S]
5	Explain the four approaches involved in the fabrication of CMOS IC technology with neat figures. → Refers to n-well, p-well, twin tub, SOI	2023
6	Discuss the Twin tub process in detail.	2022[S]
7	Explain Ion implantation process in IC fabrication.	2022[S]
8	Describe the various second order MOS device effects in detail.	2022 2025[I]
9	Discuss any five non-ideal I-V effects that come into play, when the channel length is scaled down to the order of the depletion layer.	2022[S]
10	Compare bipolar and MOS/CMOS technologies.	2023 2025[I]
11	What are major considerations in using bipolar drivers	2023
12	What is threshold voltage? What are the factors affecting the threshold voltage of NMOS device?	2023
13	Explain the various regions of operation in n-channel MOS transistor	2023
14	Describe the working of an enhancement mode transistor action with neat sketches	2025[I]

15 Derive the expression for drain-to-source current (I_{ds}) for an n-channel MOS in three regions of operation. Also draw its V-I characteristics. 2025[I]

16 Describe the following terms: 2023

a) Body effect
b) Subthreshold condition
c) Junction leakage.

Module 2

1 Implement the function $Y = \overline{A(C + BD)}$ using CMOS logic 2022

2 Justify the statement "An NMOS passes good logic '0' and PMOS passes good logic '1' " 2022

3 Determine $Zp.u/Zp.d$ ratio for an NMOS inverter when it is driven directly from another NMOS inverter. 2022 2022[S]

4 Determine pull up to pull down (Z_{pu}/Z_{pd}) ratio for an NMOS inverter when it is driven through a series of pass transistors. 2025[I]

5 Design an Ex-OR Gate using pass transistor. 2022[S]

6 Explain the alternative forms of pull up in detail. 2022[S] 2023 2025[I]

7 Explain the five regions of operation (or DC characteristics) of a CMOS inverter transfer characteristics in detail. 2022 2022[S] 2023 2025[I]

8 Implement the function $Y = \overline{AB + C(D + F)}$ using CMOS logic 2023 2025[I]

Module 3

1 Draw the circuit and stick diagram of two input CMOS NAND gate. 2022 2023

2 Draw the circuit and stick diagram of a 4:1 nMOS inverter. 2025[I]

3	Discuss the λ-based design rules in detail	2022[S]
4	Describe in detail about Layout design rule.	2023
5	Draw the Layout diagram for CMOS NOR circuit	2022[S]
6	Realize using CMOS and also draw the stick diagram for $Y = \overline{(A+B)C}$	2022[S]

Module 4

1	A particular layer of MOS circuit has a resistivity $\rho = 1\Omega$ cm. A section of this layer is 55μm long and 5μm wide and has a thickness of 1μm. Calculate the resistance from one end of this section to the other. What is the value of sheet resistance R_s?	2022
2	The resistance of the semiconductor material is 600Ω. The sheet resistance, if the dimensions of the material are 0.125μm wide and 1 mm long is?	2022[S]
3	Calculate the resistance of the given poly-silicon wire with 8μm width, 250μm length and sheet resistance = 5Ω per square.	2023
4	What is scaling and objectives of scaling in MOS circuits? What are the three scaling models and two scaling factors?	2022 2025[I]
5	Determine the scaling factors for: a) Gate capacitance C_g b) Channel resistance R_s c) Gate delay T_d d) Saturation current I_{dss} e) Switching energy per gate E_g	2025[I]
6	Explain the process of scaling; Give the scaling factors for various device parameters and explain its limitations.	2022[S] 2023
7	Discuss the influence of β_n/β_p ratio on the CMOS. transfer characteristics.	2022
8	Define the delay unit 'τ'	2022 2023 2025[I]
9	Explain the concept of sheet resistance and standard unit capacitance	2023 2025[I]
10	Determine the delays associated with a pair of NMOS inverters having ratio 4:1 in terms of 'τ'.	2022 2025[I]

11 Determine the delay involved in the operation of a pair of CMOS inverters in terms of delay unit (τ). 2023

12 Estimate the rise time and fall time in a CMOS inverter. 2022 2025[I]

13 What are super buffers? Explain its significance. 2022 2022[S]

14 What are the problems associated with driving large capacitive loads? How is it solved using cascaded inverters? 2022 2025[I]

15 Explain about BICMOS drivers in detail 2022[S]

16 Identify the delay estimation model shown in the figure and derive the parameters such as $I_{\text{dsp}}, V_{\text{out}}, t$ 2022[S]