EMBEDDED SYSTEM DESIGN ASSIGNMENT 0

MCQ

1.

The microprocessor of a computer can operate on any information if it is present in _____ only.

a) Program Counter
b) Flag
c) Main Memory
d) Secondary Memory

Answer: c

Explanation: If the information isn't in the computer's main store, the microprocessor can't do anything with it. The primary storage area in a computer, also known as main storage or memory, is where data is stored for easy access by the computer's processor. Random-access memory (RAM) and memory are frequently used interchangeably to refer to primary or main storage.

2.

Which of the following is the correct sequence of operations in a microprocessor?

a) Opcode fetch, memory read, memory write, I/O read, I/O write
b) Opcode fetch, memory write, memory read, I/O read, I/O write
c) I/O read, opcode fetch, memory read, memory write, I/O write
d) I/O read, opcode fetch, memory write, memory read, I/O write

Answer: a
Explanation: Initially, the opcode is fetched from memory, then memory read and write operations are performed followed by I/O read and I/O write operations.

3.

Which of the following is not a condition flag?

a) Trap flag
b) Auxiliary carry flag
c) Parity flag
d) Zero flag

Answer: a
Explanation: Trap, direction, and interrupt are the control flags. Carry, parity, auxiliary carry, zero, sign and overflow flags are the condition flags.

4.

Which type of hardware organization does one address instructions use.

a). Linked list
b). Stack
c). Queue
d). None of these

Ans: (b)

Explanation: Zero address instruction requires stack.

5.

Which of the following is a software interrupt?
a) TRAP
b) INTR
c) RST-6.5
d) RST-5

Answer: d
Explanation: TRAP, INTR, and RST-6.5 are the hardware interrupts but RST-5 is a software interrupt present. All software interrupts are vectored interrupts.

6.

Which of the following is true about stack pointer?
a) Stack pointer contains the address of the top of the stack memory
b) Stack pointer is an 8-bit register
c) Stack pointer stores data permanently
d) Stack pointer is initialized after stack operation

Answer: a
Explanation: Stack pointer is initialized before stack operation, it is a 16-bit register that stores data temporarily. It follows a LIFO operation. So, it contains the address of the top of the stack memory.

7.

Which of the following is a register-indirect addressing mode instruction set?

a) LDA 2700H
b) ADI 36H
c) DAA
d) LDAX B

Answer: d
Explanation: LDA 2700H is a direct addressing mode instruction. ADI 36H is an immediate addressing mode instruction. DAA is an implicit addressing mode and LDAX B is a register-indirect addressing mode instruction.

8.

Which of the following interfacing IC is a DMA controller?
a) 8257/37
b) 8155
c) 8253/54
d) 8279

Answer: a
Explanation: 8155 is a multipurpose programmable I/O device. 8253/54 is a programmable counter. 8279 is a keyboard/display controller and 8257/37 is a DMA controller.

9.

Which of the following options comes under the non – saturated logic family in Digital Electronics?
a) Emitter – coupled Logic
b) High-Threshold Logic
c) Integrated – injection Logic
d) Diode – Transistor Logic

Answer: a
Explanation: Bipolar IC's can be classified as saturated and non – saturated logic families. ECL (Emitter – coupled Logic) and Schottky TTL are said to come under the non – saturated logic family.

10.

Which of the following options represent the synchronous control inputs in an S – R flip flop?

a) S
b) R
c) Clock
d) Both S and R

Answer: d
Explanation: The input for which the flip flop changes its state when synchronized with the clock is called the synchronous control inputs. For the S – R flip flop, both S and R are synchronous control inputs.

11.

What are the basic gates in MOS logic family?
a) NAND and NOR
b) AND and OR
c) NAND and OR
d) AND and NOR

Answer: a
Explanation: The MOS logic family uses the MOSFET devices to perform its operation. NAND and NOR are the basic gates that are the building blocks of most digital circuits.

12.

Which of the following give the correct number of multiplexers required to build a 32 x 1 multiplexer?
a) Four 16 x 1 multiplexers
b) Three 16 x 1 multiplexer
c) Four 8 x 1 multiplexer
d) Three 8 x 1 multiplexer

Answer: c

Explanation: Higher – order multiplexers can be implemented using lower – order multiplexers. A 32 x 1 multiplexer can be built using Four 16 x 1 multiplexers, Two 8 x 1 multiplexers, or Eight 4 x 1 multiplexers.

13.

The device which is allowed to initiate data transfers on the BUS at any time is called _____
a) Processor
b) BUS master
c) Controller
d) BUS arbitrator

Answer: b
Explanation: The device which is currently accessing the BUS is called as the BUS master.

14.

What is the interface circuit?
a) Helps in the decoding of the address on the address BUs
b) Helps in installing of the software driver for the device
c) Houses the buffer that helps in data transfer
d) None of the mentioned

Answer: a
Explanation: Once the address is put on the BUS the interface circuit decodes the address and uses the buffer space to transfer data.

15.

Which option is true regarding the carry in the ripple adders?
a) Must travel through the configuration
b) Is generated at the end of each operation
c) Are generated at the beginning only
d) None of the mentioned

Answer: a
Explanation: The carry must pass through the configuration of the circuit till it reaches the particular step.

TRUE/FALSE

I/O-mapped systems identify their input and output devices by giving them an 8-bit port number.

A. True

B. False

Answer: Option **A**

A microcontroller integrates multichip systems with RAM, ROM, and I/O.

A. True

B. False

Answer: Option **A**

The stack is a data storage area in RAM used by certain microprocessor operations.

A. True

B. False

Answer: Option **A**

Short Answer (Numeric)

1. How many outputs will a 3 bit decoder produce?

   Ans. 8

   Details: 3 bits generates combination equal to 2^3 =8

2. Find No of misses excluding compulsory miss for the following block fetch sequence using LRU principle for fully associative cache having 4 blocks 0,1,2,3,0,1,4,0,1,2,3

   Ans 3

Details: content of cache

0	0	0	0	0	0	0	0	0	0	3(mis)
	1	1	1	1	1	1	1	1	1	1
		2	2	2	2	4(miss)	4	4	4	4
			3	3	3	3	3	3	2(miss)	2

3. Find out the frequency of the pipeline where time required to carry out each stage of the pipeline are 5ms, 8ms, 1ms, 3ms respectively.

   Ans. 125 Hz

Details: frequency of pipe line = frequency of slowest stage, therefore 1/8ms=125

4. For a signal with maximum frequency 22khz, what will be the minimum frequency of the sampling circuit needed to sample the signal so that it could be reproduced closest to original (without aliasing).

   Ans. 44 KHz

Details: Nyquist–Shannon sampling theorem