Assignment 2

MCQ:

1. We can optimise the datapath of an FSMD by
   A. Sharing a single functional unit, in case the same operation occurs in different states.
   B. Implementing a shared ALU system among operations occurring in different states.
   C. Both A and B
   D. None of the above.

Solution: Option C. Both A and B

Explanation: On sharing the same functional unit, the one to one mapping from operation to unit will not be required. Also, sharing an ALU will reduce the complexity of the datapath implemented.

2. FPGAs can be used for implementing
   A. Hardware Security Modules (HSM)
   B. High Frequency Trading (HFT) systems
   C. Both A and B
   D. None of the above

Solution: Option C. Both A and B

Explanation: FPGAs can be used for implementing an HSM since they can be used for encryption and decryption of digital signatures at a very low latency. The high operation speed of FPGAs also allow the acceleration of different components of an HFT system like network stack, financial protocol parsing.

3. The interconnectivity among the circuital elements of an FPGA in established using
   A. Fuse
   B. Antifuse
   C. SRAM
   D. Both B and C

Solution: Option D. Both B and C

Explanation: Antifuse is used in FPGA in segmented channel routing architecture since they have a small area and low parasitic resistance and capacitance. SRAM cells are present in SRAM-based FPGAs in the form arrays and they program the interconnects in the FPGA.

4. Suppose I want to use a single FPGA board to perform two sets of mathematical operations one after the other. What kind of interconnectivity will be suitable?
   A. Antifuse FPGA
   B. SRAM-based FPGA
   C. Both A and B
   D. None of the above

Solution: Option B. SRAM-based FPGA

Explanation: Antifuse FPGAs use antifuses(low resistance devices having a small area and a limited field of operation). Hence, they are programmable only once and therefore can perform only one mathematical operation which does not satisfy the requirements. SRAM-based FPGA

boards have arrays of SRAM cells which program the interconnectivity and hence can be programmed to perform two mathematical operations one after the other.

5. The inputs of any Programmable Logic Device is fed through
    A. OR gates
    B. NOR gates
    C. AND gates
    D. NAND gates

Solution: Option C. AND gates
Explanation: The input is fed through the AND gate followed by inverting and/or non inverting buffers.

6. The Configurable Logic Blocks on an FPGA comprise
    A. XOR gate, transistor, Decoder
    B. Johnson counter, transistor, Half Adder
    C. Flip flop, LUT, Multiplexer
    D. None of the above

Solution: Option C. Flip flop, LUT, Multiplexer
Explanation: Flip flop to store one bit of data, LUT to contain the predefined output of certain logical operations, and multiplexer to select between inputs, are the components of a CLB.

7. Which of the following is a library in VHDL?
    A. IEEE
    B. std_logic_1164
    C. numeric_std
    D. None of the above

Solution: Option A. IEEE
Explanation: IEEE is a standard library in VHDL. std_logic_1164(used to define interconnection data types) and numeric_std(used to define numeric types and standard arithmetic functions) are packages in the IEEE library.

8. What type of FPGA is preferred for designing aerospace devices?
    A. Antifuse FPGAs
    B. SRAM-based FPGAs
    C. Both A and B
    D. None of the above

Solution: Option A. Antifuse FPGAs
Explanation: Antifuse FPGAs have a faster boot than SRAM-based FPGAs. Also, antifuse FPGAs are not affected by radiation.

9. Reducing the size of CLBs will lead to
   A. Increase in area of FPGA
   B. Decrease in the propagation delay of FPGA
   C. Both A and B
   D. None of the above

Solution: Option C. Both A and B
Explanation: Reducing the size of an CLB leads to an increase in their number in the FPGA. Also the propagation delay increases due to the increase in the number of CLBs.

10. In VHDL, port description is given by
   A. Identifier
   B. Mode
   C. Datatype
   D. All of the above

Solution: Option D. All of the above
Explanation: Port description has an identifier(not a reserved word), mode(in, out, buffer), and datatype(predefined).

Short-Answer type(Alphanumeric answers only):

11. What is the default size(in bits) of integers in VHDL?
Solution : 32
Explanation: VHDL was made in the time when the dominant processors in the market were of 32 bits. Even now for FPGAs the default size is kept to 32 bits.

12. Analyse the following piece of code to design a blinking LED.

```
signal pulse:std.logic := '0';
signal count:integer range 0 to 4999:=0;
begin
        counter:process(CLK)
        begin
        if 'CLK' event and CLK = '1' then
                if count = 4999 then
                        count=0
                        pulse=not pulse
                else
                        count+=1
                endif
        endif
        end process
        LED=pulse
end
```

How many times does the LED blink if the above code is programmed in an antifuse FPGA with the interconnections coded to run once?

Solution: 5000
Explanation: Since the FPGA is antifuse, the code runs only for once. On analyzing the code, we see that the loop runs for 5000 times and each time the counter to check the blink of the LED is incremented till it reaches 4999. Hence the LED blinks 5000 times.