Assignment 3

MCQ:

1. Three main Hardware Description Languages(HDL) that are currently used widely in the industry are

A. VHDL
B. Verilog
C. System Verilog
D. All of the above

Solution: Option D. All of the above
Explanation: Fact

2. Synthesis of ASIC systems is done best using

A. System Verilog
B. Verilog
C. Both A and B
D. None of the above

Solution: Option D. All of these
Explanation: ASIC systems are built using VHDL which was developed by the US Department of Defense.

3. What are the basic levels of modeling in Verilog?

A. Structural
B. Behavioral
C. Dataflow
D. All of the above

Solution: Option D. All of the above
Explanation: Verilog can be used to make basic low level module instantiations like a schematic(Structural), dataflow graphs showcasing the input and output functions and their relations(Dataflow), and also express the system in an algorithmic manner(Behavioral).

4. Which of the following, in Verilog, represents a high impedance value for a component?

A. 1
B. 0
C. x
D. z

Solution: Option D. z
Explanation: z is given to components whose value has a high impedance. It makes sure of the fact that the component is not in use.

5. Major data types in Verilog are:

A. Net
B. Variable
C. Both A and B
D. None of the above

Solution: Option C. Both A and B
Explanation: Net represents wires in a hardware system and variables represent registers.

6. Which of the following operators are unary in Verilog?
   A. =
   B. ==
   C. {}
   D. ~^

Solution: Option D. ~^
Explanation: = does not exist in Verilog. == is the assignment operator(requires at least 2 operands). {} is a concatenation operator which requires more than one operand. ~^ is the XNOR operator which when used with a single variable returns the XNOR value of the variable.

7. What does the port declaration " input [3:0] r1" mean?
   A. r1 port is an input bus with a size of 4 bits.
   B. r1 port is an inout bus with a size of 3 bits.
   C. r1 port is an input port with a size of 3 bits.
   D. None of the above.

Solution: Option A. r1 port is an input bus with a size of 4 bits.
Explanation: The port r1 is an input port with a size of 4 bits according to the given Verilog syntax.

8. a <= #10 b+c is an example of
   A. Inter Statement delay
   B. Intra Statement delay
   C. Both A and B
   D. None of the above

Solution: Option B. Intra Assignment delay
Explanation: The syntax for intra assignment delay is <LHS> = #<delay> <RHS>

9. " `timescale 1ns/10ps " means
   A. The unit of time in the simulation is 1nanosecond.
   B. The value of time_precision is 10picoseconds.
   C. Both A and B.
   D. None of the above

Solution: Option C. Both A and B
Explanation: The syntax for timescale is : `timescale <time_unit>/<time_precision>

10. For two components, a and b, which of the following represents the equality of both, including x and z?(As per the IEEE standard)
   A. =
   B. ==
   C. ===
   D. None of the above

Solution: Option C. ===
Explanation: As per the IEEE std 1800-2012, = is not a valid operator, == is used to represent equality, result can be unknown, === represents equality, including x and z.

Short-Answer type(Alphanumeric answers only):

11. Find the output for the following piece of code:

```
module bench();
integer i;
reg clk;
initial begin
  clk = 0;
  #5 $finish;
end
always #1 clk = !clk;
always @ (posedge clk)
begin : FOR_OUT
  for (i=0; i < 10; i = i + 3) begin
    if (i == 9) begin
      disable FOR_OUT;
    end
    $write (i);
  end
end
endmodule
```

Solution: 0 3 6 0 3 6 0
Explanation: From the for loop it is clear that the output for one clock cycle will be 0 3 6. Since the $finish has a delay of 5s, at t=1 the output will be 0 followed by 3 and 6 at t=2. Therefore, the final output at t=5 will be 0 3 6 0 3 6 0.

12. How many of the following tasks are terminated by newlines:
$display, $write, $monitor, $strobe.

Solution: 3
Explanation: Newline is not added in $write.