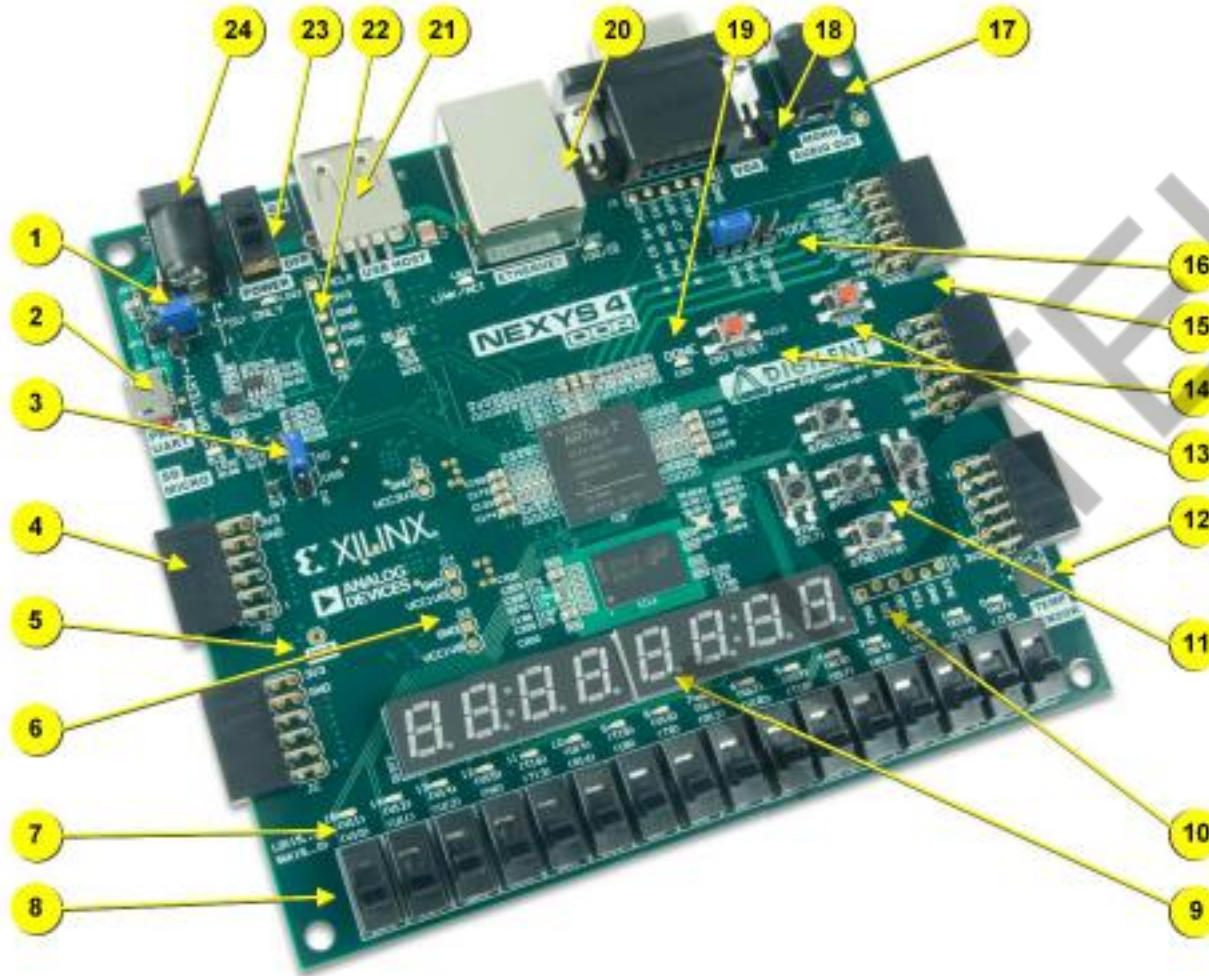


INTRODUCTION TO VIVADO & FPGA BOARD PROTOTYPING

Design of basic digital circuits on FPGA Board(Nexys-4 DDR)
using FPGA Design tools(Vivado)

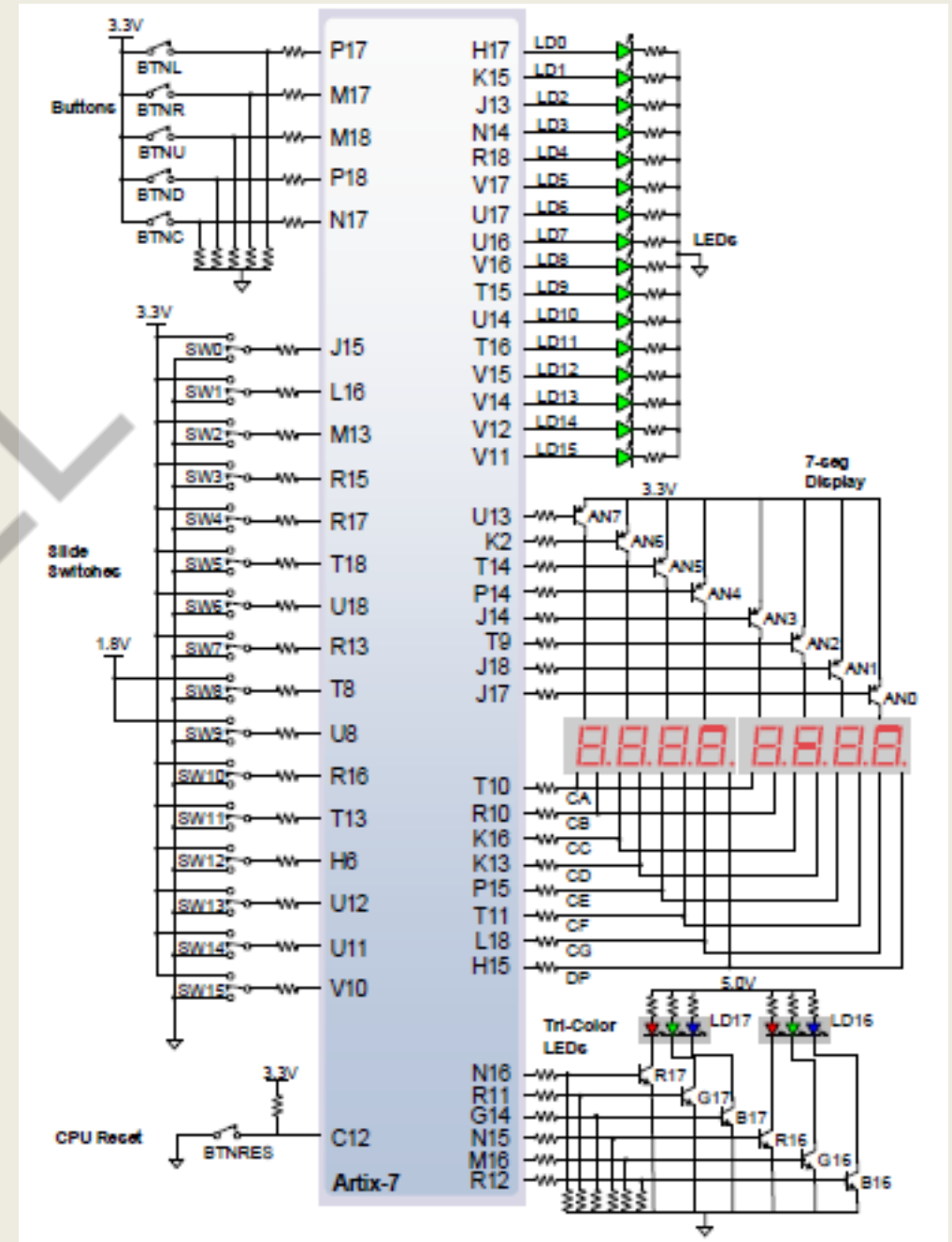
Nexys-4 DDR Board



Callout	Component Description	Callout	Component Description
1	Power select jumper and battery header	13	FPGA configuration reset button
2	Shared UART/JTAG USB port	14	CPU reset button (for soft cores)
3	External configuration jumper (SD / USB)	15	Analog signal Pmod port (XADC)
4	Pmod port(s)	16	Programming mode jumper
5	Microphone	17	Audio connector
6	Power supply test point(s)	18	VGA connector
7	LEDs (16)	19	FPGA programming done LED
8	Slide switches	20	Ethernet connector
9	Eight digit 7-seg display	21	USB host connector
10	JTAG port for (optional) external cable	22	PIC24 programming port (factory use)
11	Five pushbuttons	23	Power switch
12	Temperature sensor	24	Power jack

Nexys-4 Basic I/O

- Manufactured by Digilent
- Contains an FPGA of Artix-7 Family
- Configured directly from Vivado through USB JTAG/UART
- The **five pushbuttons** generate a low output when they are at rest, and a high output only when they are pressed.
- **Slide switches** generate constant high or low inputs depending on their position.
- The **sixteen individual LEDs** are anode-connected to the FPGA via resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin.
- The anodes of the seven LEDs forming each **7-segment display** digit are tied together into one “common anode” circuit node, but the LED cathodes remain separate. The common anode signals are available as eight “digit enable” input signals to the 8-digit display. The cathodes of similar segments on all the displays are connected into seven circuit nodes. This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted. To illuminate a segment, both the anode and the cathode should be driven low.



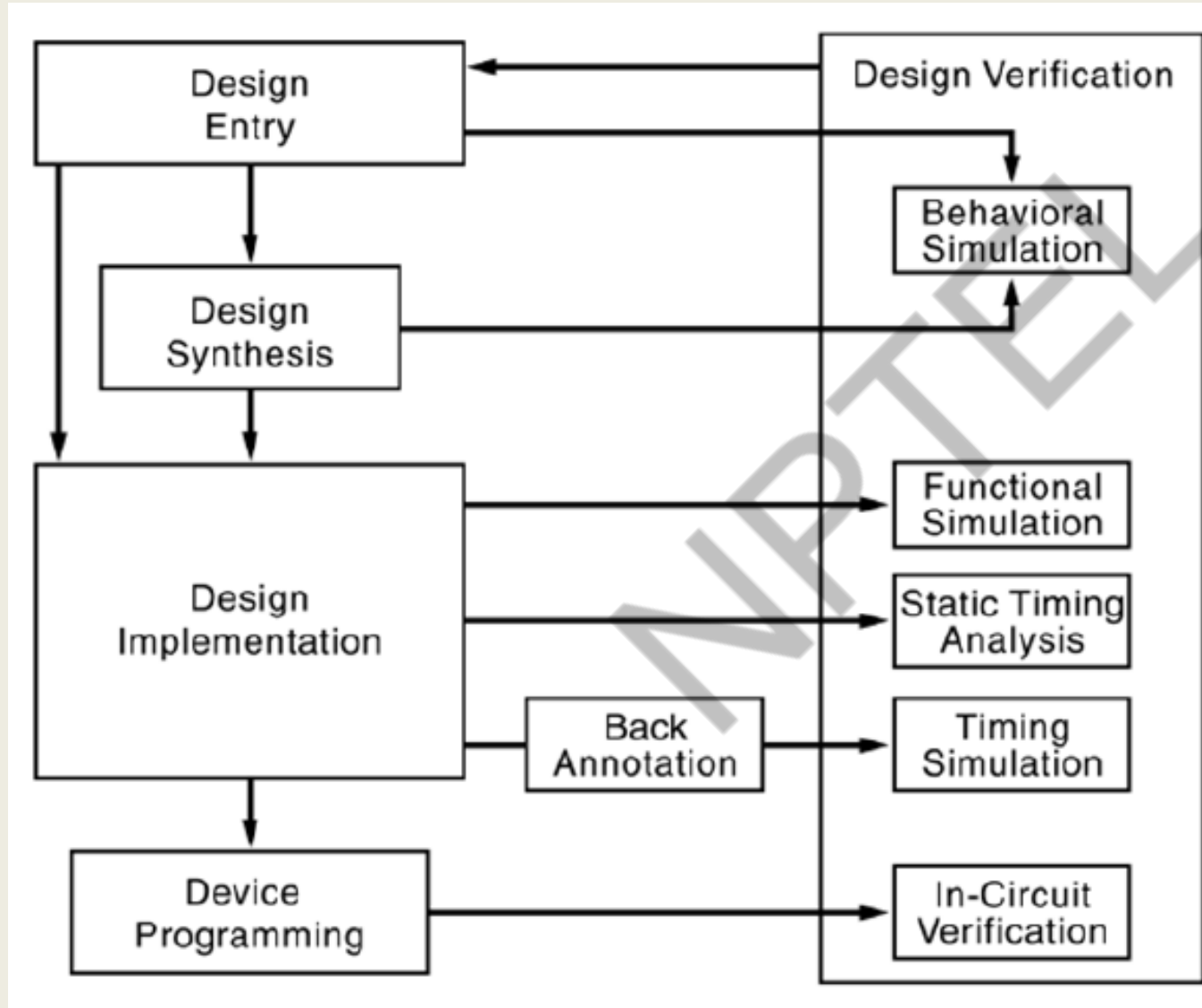
Xilinx Artix-7™ FPGA xc7a100t-1csg324

- Xilinx® 7 series FPGAs include three families:
 - The Artix®-7 family is optimized for lowest cost and power for the highest volume applications.
 - The Virtex®-7 family is optimized for highest system performance and capacity.
 - The Kintex®-7 family is an innovative class of FPGAs optimized for the best price-performance.
- Artix-7 xc7a100t feature summary:
 - 101,440 logic cells and 15,850 logic slices, each with four 6-input LUTs and 8 flip-flops
 - 4,860 Kbits of fast block RAM (135 × 36 Kb blocks)
 - 6 clock management tiles, each with phase-locked loop (PLL)
 - 240 DSP slices (with 25 × 18 multiplier, 48-bit accumulator, and pre-adder)
 - On-chip analog-to-digital converter (XADC)
 - Configuration bitstream length of 30,606,304 bits (~3.6 MB)

Vivado IDE Solution

- 7-Series (or newer) devices
- Interactive design and analysis
 - Timing analysis, connectivity, resource utilization, timing constraint analysis and I/O assignment.
- RTL development and analysis
 - Elaboration of HDL
 - Hierarchical exploration
 - Schematic generation
- XSIM simulator integration
- Full Tcl scripting support
- Interactive IP plug & play environment
- Synthesis and implementation in one package.

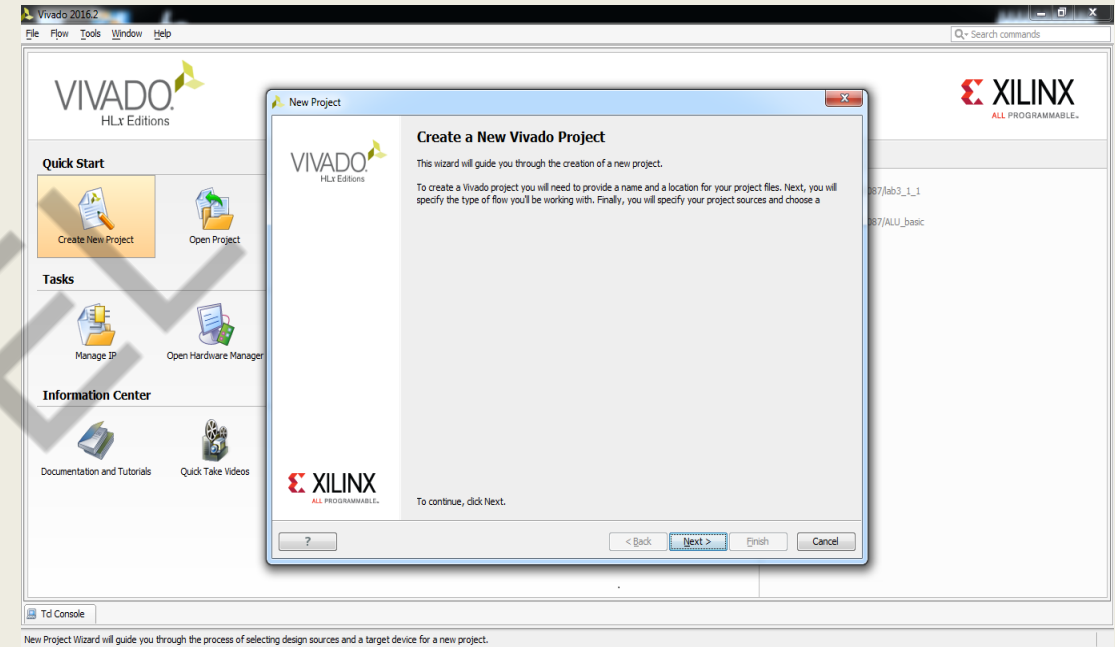
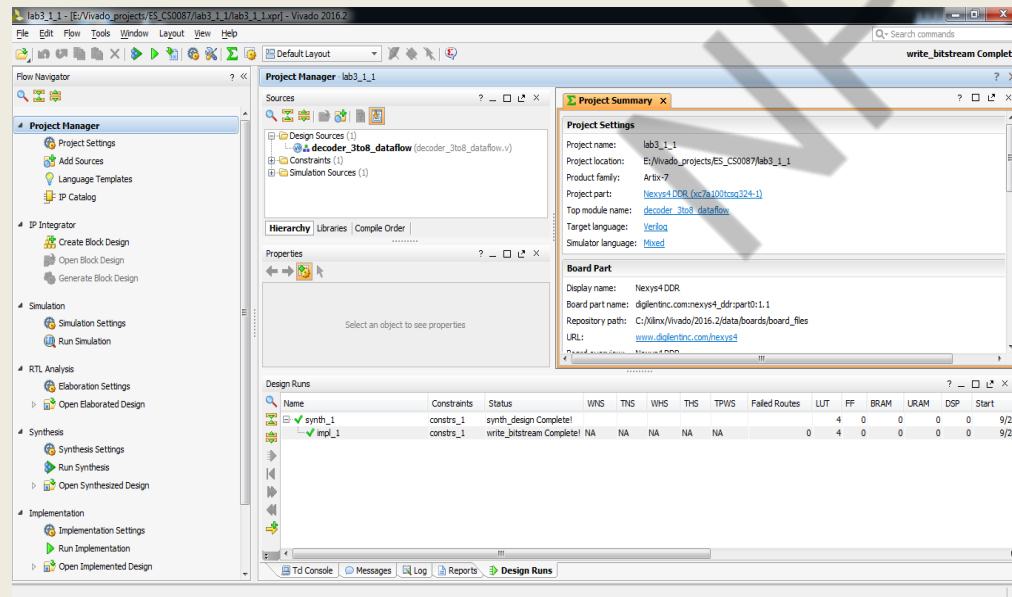
FPGA Design Flow



- Design entry based on:
 - Verilog
 - IP Catalog

Vivado Design Suite Walkthrough

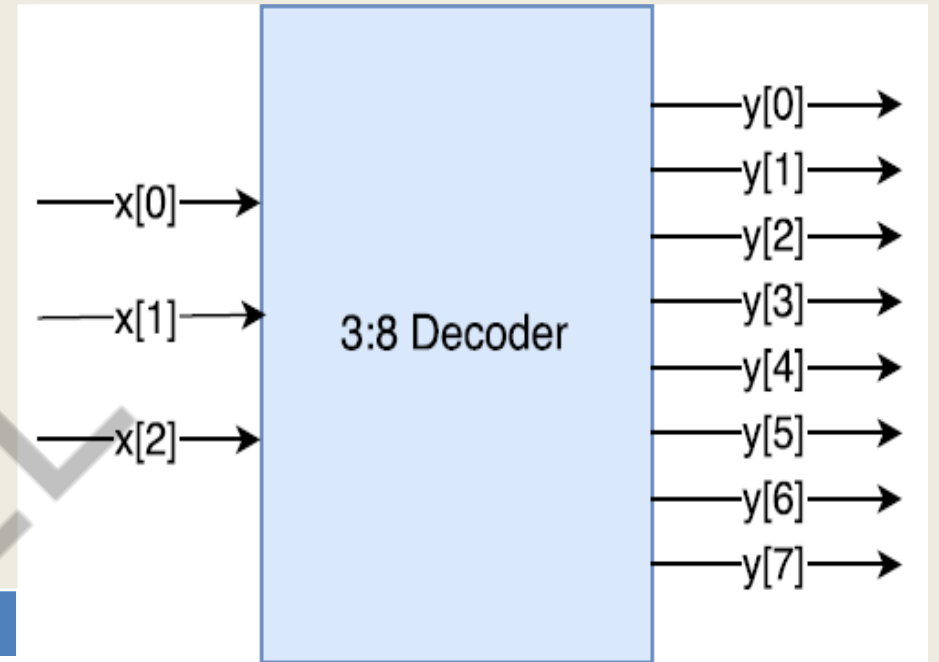
- Download and install Vivado Design Suite
- Getting started page
- Creating a new project
- Flow navigator
- Synthesis and Implementation
- Adding .xdc file
- Generating board programming file



Example-1

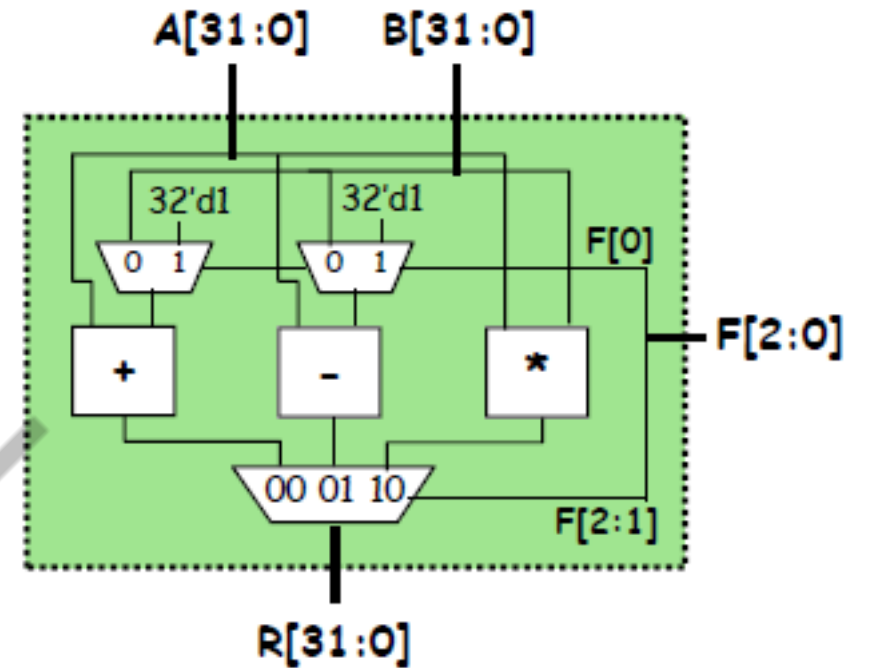
- Design of a 3:8 Decoder.
- One 3-bit input vector x .
- The output is 8-bit vector y .

X[0]	X[1]	X[2]	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



Example -2

- Design of a 32-bit ALU.
- Two 32-bit input vectors A and B .
- One 3-bit input arithmetic function selection F.
- The result is the 32-bit output vector R.
- Following components(or submodules) are used:
 - 2:1 MUX
 - 3:1 MUX
 - 32-bit Adder
 - 32-bit Subtractor
 - 16-bit Multiplier



Function Table

F2	F1	F0	Function
0	0	0	$A + B$
0	0	1	$A + 1$
0	1	0	$A - B$
0	1	1	$A - 1$
1	0	X	$A * B$

References

- [Slide Source](#)
- [Board File Installation](#)
- [Digilent Nexys-4 DDR Documentation](#)
- [Lab1,2 & 3](#)
- [Xilinx 7 Series FPGA Overview](#)
- [Xilinx 7 Series Product Selection Guide](#)