Assignment 6

MCQ:

1. To reduce the energy consumption of an embedded system, there needs to be at most ____ discrete voltage levels.

A. Three
B. Four
C. Two
D. Five

Solution: Option C. Two

Explanation: This is the statement of the Ishihara Yasuura Lemma.

2. Suppose I have to build a device that has to perform multiplication of 2-bit numbers. Which chip design will let me perform multiple multiplications at highest energy efficiency?

A. DSP
B. ASIC
C. FPGA
D. None of the above

Solution: Option B. ASIC

Explanation: ASIC has the highest throughput in terms of operations per joule followed by FPGA and DSP.

3. What is dark silicon with reference to the electronic industry?

A. Amount of circuitry on a chip which cannot be powered at the given operating voltage due to thermal constraints of the chip.
B. The dark coloured silicon used in the transistors.
C. Both A and B.
D. None of the above.

Solution: Option A. Amount of circuitry on a chip which cannot be powered at the given operating voltage due to thermal constraints of the chip.

Explanation: Option A is the definition of dark silicon.

4. Which are the assumptions in the SD algorithm?

A. Arrival and deadline time of all tasks are known.
B. Worst-case execution time is not known.
C. Both A and B.
D. None of the above.

Solution: Option A. Arrival and deadline time of all tasks are known.

Explanation: Worst-case execution time is known in case of the SD algorithm, hence option B is incorrect. Option A is a fact.

5. In a system performing parallel processing of n tasks, the power of the system is

A. Directly proportional to n
B. Inversely proportional to n
C. Directly proportional to n^2
D. Inversely proportional to n^2

Solution: Option D. Inversely proportional to n^2.

Explanation: Ppar = Pseq/n^2. Therefore the power of a parallel processing system is inversely proportional to n^2.

6. Which of the following properties about VLIW(Very Large Instruction Word) are false?

A. Reduces complexity of hardware
B. Reduces power consumption
C. Increases clock rate
D. Reduces program code size

Solution: Option D. Reduces program code size

Explanation: The program code size increases due to the multiple instructions and hence the compilers and hardware is difficult to design.

7. Zero overhead loops

A. Automatically repeats the body of the loops.
B. Can be implemented both in hardware and software.
C. Speeds up the processing of the device.
D. All of the above.

Solution: Option D. All of the above

Explanation: Features of the Zero overhead loop instruction which is common in DSPs and CISC instruction sets.

8. In a system performing parallel processing of n tasks, the time to run the program is ____ the time taken by the system executing sequentially.

A. Same as
B. Greater than
C. Less than
D. Slightly less than

Solution: Option A. Same as

Explanation: The time is not affected by parallel scheduling of tasks. Only the power consumed varies.

9. “VLIW is used in RISC architecture so that it can exploit instruction-level parallelism and provide a cheaper and faster execution device.”

A. True
B. False
C. Cannot be determined

Solution: Option A. True

Explanation: VLIW stands for Very Long Instruction Words with parallel dispatch and is used to schedule multiple instructions at once thus reducing the complicated nature of the used hardware.

10. What is the bit size of the original ARM Thumb instruction set?
    A. 64
    B. 16
    C. 32
    D. None of the above

Solution: Option B. 16
Explanation: Fact. The new Thumb2 set has both 16 and 32 bit instructions.

Short-Answer type(Alphanumeric answers only):

11. Suppose a system with a clock of 50Hz is made to run 4 tasks parallely. Calculate the new clock frequency(upto two decimal places in Hz).
Solution: 12.50

Explanation: fpar = fseq/n for n tasks run parallely. Putting fseq = 50 and n=4, fpar = 12.50 Hz

12. Suppose a system with a clock of 50Hz runs 4 tasks. The power consumed for running all the tasks sequentially is 64W. Calculate the power to run all tasks per clock(in W).
Solution: 16

Explanation:
Ppar = Pseq/ n^2 and Ppar per clock = Ppar * n = Pseq/ n .
Putting n = 4 and Pseq = 64, Ppar per clock = 16W.