Template synthesis and morphology of CdS nanowire diode arrays using anodic alumina membranes

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It is well known that template synthesis is a simple and versatile method for preparing nanostructures. Due to their uniform and nearly parallel porous structures, anodic alumina membranes (AAM) have become ideal templates for the electrochemical deposition of nanowire arrays. Nanocrystalline semiconductor materials have attracted considerable attention and CdS, in particular, has been extensively studied due to its potential applications in field effect transistors (FETS), light emitting diodes (LEDs), photocatalysis and biological sensors. For electrochemical deposition of CdS nanowires, the electrolyte solution consisted of 0.055M $CdCl_2$ and 0.19M elemental sulphur in dimethyal sulfoxide (DMSO). The growth of CdS nanowires was carried out in an electrochemical cell fabricated in our laboratory. Surface morphology of the deposited CdS nanowires was studied using SEM and HRTEM. I-V characteristics were studied by Keithley Dual Source Meter using platinum probes for contacts. Experimental results show that nanowire arrays grown in AAM behave as resonating tunneling diodes (RTDs).

1. Introduction

Nanostructural materials have become attractive because of their unique characteristics. Due to the quantum confinement effect and the large surface to volume ratio, nanoparticles and nanowires show some unique physical and chemical properties. Nanocrystalline semiconductor materials such as PbS, CdS and ZnS have attracted considerable attention due to their unique properties which are missing in bulk materials [1-3]. Semiconductor nanowires have been assembled into FETs, p-n diodes, LEDs, bipolar junction transistors, nanoscale lasers, gas sensors, nanoresonators and nanogenerators [4]. CdS nanowires, in particular, have been extensively studied due to their potential applications in field effect transistors (FETS), light emitting diodes (LEDs), photocatalysis and crossed Si-CdS nanowires recently used in nanoscale injection laser and in integrated photonics [4-7]. Many novel technologies [8] have been used to prepare CdS nanowires such as the vapour-liquid-solid (VLS) process, laser assisted chemical vapour deposition (CVD), thermal CVD, metal-catalysed molecular beam epitaxy (MBE) and chemical beam epitaxy (CBE). In our investigation, we have used template-based synthesis [9-11] of CdS nanowires using anodic alumina membrane (AAM) as a template.

It is well known that template synthesis is a simple and versatile method for preparing nanostructures within the pores of a microporous template membrane. Due to their uniform and nearly parallel porous structures, anodic alumina membranes (AAM) have become ideal templates for the electrochemical deposition of the highly anisotropic, aligned nanowire arrays. Routkevitch et al. [12] reported that ac electrodeposition in an AAM template is a simple and efficient method to fabricate aligned CdS nanowires. We preferred to use dc electrodeposition approach to obtain aligned and well distributed nanowire arrays, as well as uniform single crystal structure.

2. Experimental Technique

Commercially available AAM (Anodisc 25, Whatman, UK) having an average pore diameter of 200 nm, a nominal thickness of 60 um and pore density of 10^9 pores/cm^2, was used as a template. A copper film was deposited by vacuum evaporation onto the back of the template membrane. Electrochemical cell used for fabrication of CdS nanowires has been designed in our laboratory [9]. A silver rod was used as an anode and the cathode consists of copper foil attached to copper coated AAM by an adhesive tape of good conductivity.

For electrochemical deposition of CdS, we adopted the process used by Mondal *et al* [11]. The electrolyte solution consisted of 0.055M $CdCl_2$ and 0.19M elemental sulphur in dimethyal sulfoxide (DMSO). This solution prevents the corrosion of AAM during the deposition. The growth of CdS nanowires was carried out for 10 min at a solution temperature of 80 ^{0}C with a dc potential of 2V applied

between Ag anode and Cu cathode. The deposited samples were washed with hot DMSO to remove excess sulphur from the surface followed by rinsing in de-ionised water.

Surface morphology of the deposited CdS nanowires was studied using SEM and HRTEM. For this purpose, AAM was kept immersed in 1 M NaOH for 2 hours in a beaker to dissolve alumina template. The CdS nanowires were liberated from the host matrix, washed in distilled water and dried in an oven at 50^0C for 30 minutes. The cleaned and dried nanowires were mounted on aluminium stubs with the help of double adhesive tape, sputtered with a layer of gold using JEOL sputter JFC 1100. Scanning Electron Microscope (JEOL JSM 6100) was used to record cross-sectional (figure 1a) and lateral views (figure 1b) of grown nanowires at an accelerating voltage of 15kV using different magnifications.

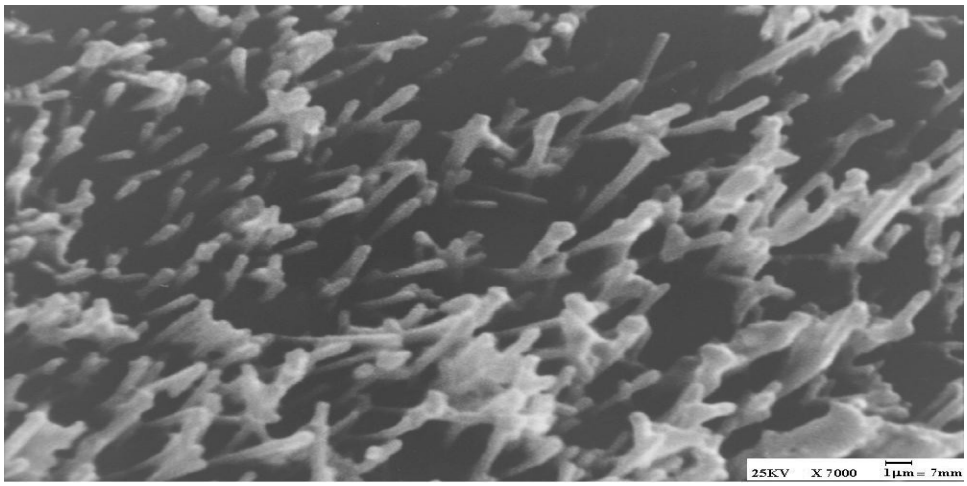

Figure 1 SEM micrograph showing top view of CdS nanowires

Figure 1(b) SEM micrograph showing lateral view of CdS nanowires

High Resolution Transmission Electron Microscope (HRTEM, Hitachi H 7500) at Punjab University, Chandigarh was used for measurements of CdS nanowire diameters. For this purpose, nanowire arrays were removed from the template in ethanol and a few drops of this solution were loaded on carbon coated gold grids and inserted in HRTEM. Measurements were carried out in imaging mode at 80 kV under ultra high vacuum conditions. CdS nanowires show diameter variation from 222 nm to 300 nm and branching in one of the nanowires (Fig. 2).

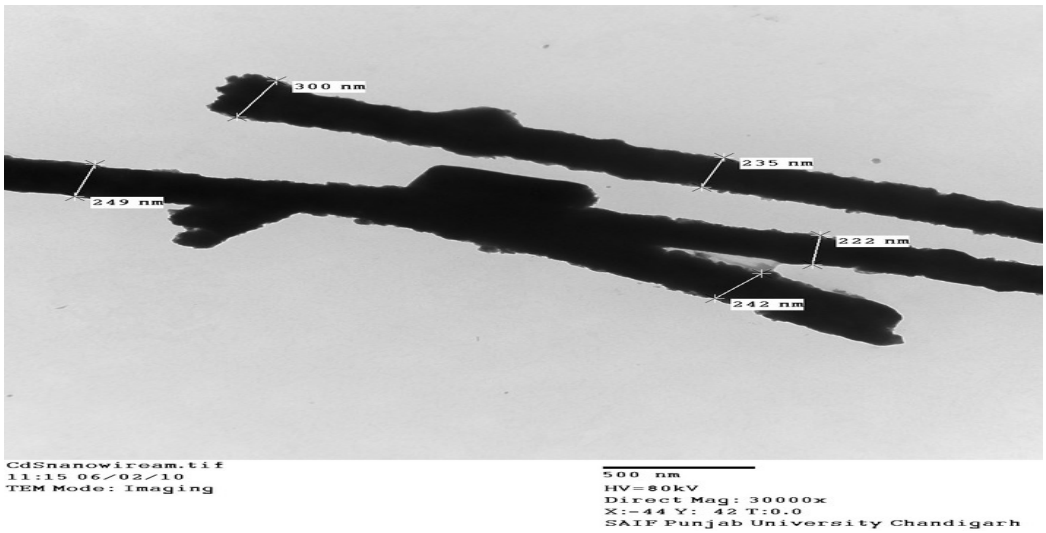

Figure 2. HRTEM image showing diameter variation and branching of CdS nanowires

I-V characteristics of CdS nanowires were studied using Keithley Model 4200 SCS programmable dual source meter facility of Central Scientific Instruments Organisation (CSIO), Chandigarh. I-V plot of CdS nanowires (Fig. 3) was obtained using platinum probes of 0.5μm diameter tip for making contacts with copper strip and nanowire arrays.

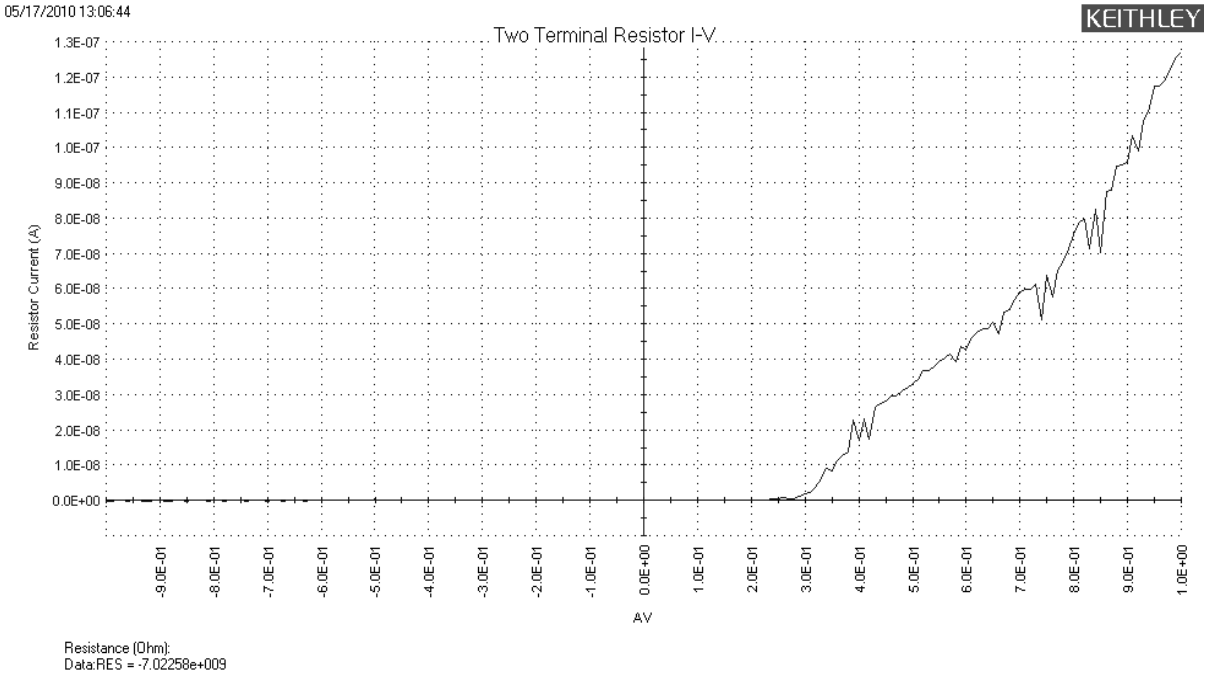

Figure 3. I-V plot of CdS nanowire diode arrays showing RTD characteristics

3. Results and discussions

The process for the electrodeposition [13] of CdS in the DMSO solution containing $CdCl_2$ and elemental sulphur involves three steps: First, the elemental sulphur in the solution diffuses to the electrode surface and absorbs on it. Second, the absorbed sulphur atoms undergo an electrochemical deoxidization reaction and produces S^{2-} ion. Third, the generated S^{2-} ions react with Cd^{2+} ions in the solution to form CdS crystalline core, which is fastest one among the three steps. Electrodeposition is limited to one direction in AAM pores to grow nanowires of uniform dimensions.

It is well known that nanowires offer several unique merits [4]: First, nanowire devices can be assembled in a rational and predictable manner because the size, interfacial properties, and electronic properties can be precisely

controlled during synthesis. Second, it is possible to have unique possibilities of building blocks not possible in conventional electronics. Third, the structure of nanowires can be rationally designed both axially and radially for creating nanodevices that exhibit both multifunctionality and integration. Our preliminary investigations establish that CdS nanowires ensembles behave as diode arrays.

Schonenberger *et al* [14] reported that pore diameters of commercially available templates vary over a large range. The diameter variation found in nanowires fabricated by them was in the ratio of 1:3. In our investigations, HRTEM micrographs show diameter variation of CdS nanowires in the range 222-300 nm. It clearly shows that nanowires are not perfect cylinders of 200 nm diameter but show a rugged structure from one end to the other. The aspect ratio, that is, the ratio of length to diameter, is on the order of 300.

I-V characteristics of CdS nanowires exhibit some interesting features. A prominent feature of I-V plot is a number of peaks and valleys showing decrease in current with increase of voltage, resulting in negative differential resistance (NDR). This behaviour is typical of a resonant tunneling diode (RTD) in which electrons can tunnel through some resonant states at certain energy levels. The presence of several NDR zones on the I-V plot is a definite proof of a RTD structure in CdS nanowires. In the literature, RTDs fabricated by InAs/InP III-V nanowire heterostructures have been reported [15].

4. Conclusions

Template synthesis using AAM is an efficient tool for fabrication of CdS nanowire diode arrays. SEM and HRTEM micrographs reveal morphology of CdS heterostructures with non-uniform cylindrical shape. CdS nanowire arrays exhibit RTD structure with negative differential resistance. This preliminary study opens a new route for fabrication of high performance electronic devices based on RTD behaviour of CdS nanowires.

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