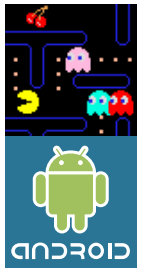
Fundamentals of Computer Systems

Introductory Topics

Columbia University

Computer Systems Work Because of Abstraction

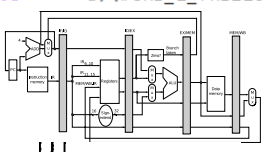


Application Software

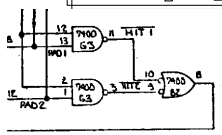
Operating Systems

```
  ;; voice 1 wave select
ld      a,(#CH1_W_NUM)
and     a
ld      a,(#CH1_W_SEL)
jr      nz,#00b4
ld      a,(#CH1_E_TABLE0)
```

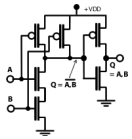
Architecture



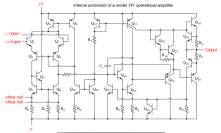
Micro-Architecture



Logic

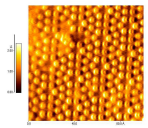


Digital Circuits



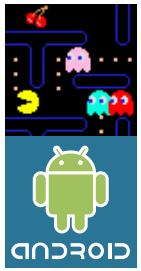
Analog Circuits

Devices



Physics

Computer Systems Work Because of Abstraction

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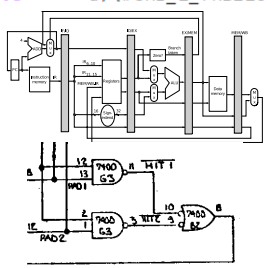
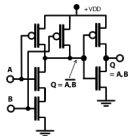
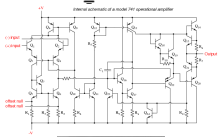
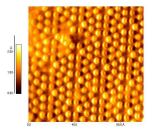








Application Software	COMS 3157, 4156, et al.
Operating Systems	COMS W4118
Architecture	Second Half of 3827
Micro-Architecture	Second Half of 3827
Logic	First Half of 3827
Digital Circuits	First Half of 3827
Analog Circuits	ELEN 3331
Devices	ELEN 3106
Physics	ELEN 3106 et al.

The digital abstraction

Abstraction hides unimportant details

The digital abstraction of 0 and 1, hides physical representation (0-5V? 0.1.8V? Physical switch? Gears?, etc.)

On top of these 0s and 1s we represent:

- numbers,
- letters, and
- programs!

More abstraction: gates

Logic gates are abstractions of circuits that manipulate the physical representations of 0 and 1.

Design principles

- Hierarchy
- Modularity
- Regularity

All used to manage complexity.

Resource Efficiency

Abstraction provides function, but performance or efficiency may be a different story.

Course Administration

Lectures 10:10–11:25 AM Tue, Thur
501 Schermerhorn Hall
Sep 5 – Dec 7
Holidays: Nov 7, 23

Resources

We will use courseworks for all course materials:

- syllabus,
- slides,
- assignments,
- grades,
- etc.

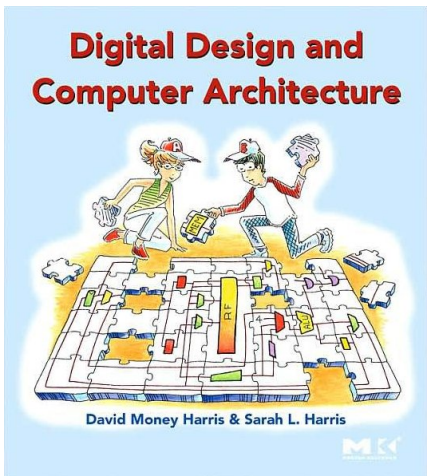
There is a link to Piazza which we will use for Q&A and announcements.

Textbook

No required text, but there is a recommendation:

David Harris and Sarah Harris. *Digital Design and Computer Architecture.*

Almost precisely right for the scope of this class: digital logic and computer architecture.



Office Hours

The seven (and counting) TAs and I will all offer office hours.

Always consult the course calendar (linked from the syllabus in courseworks) for the upcoming hours.

Design Projects

Over the course of the semester, you will complete six design projects:

- *five* hardware designs,
- *one* software design in MIPS.

I will demo logic simulator (Logisim) and MIPS simulator (Spim) in lecture.

There is no one right answer.

Grading Rubric

Combinational Design	15%
Sequential Design	15%
Datapath Design	15%
MIPS Programming	20%
Pipeline Design	20%
Cache Design	15%

Test harness and scoring rubric will be provided with each assignment.

Project Logistics

Projects are due by 11:59:00PM on their due date.

Repeat submissions are fine. We will grade the last one.

Parts of project are autograded. Follow all “rules and regulations” specified in the prompt.

Each student gets three free late days (atomic 24h extensions).

May use at most two on any one project.

Safeguard Your Work

It is your responsibility to keep your work safe.

1. Backups in the event of technical disasters (lost laptops, hard drive failures, etc.)

2. Do not share solutions with classmates or the public.

Collaboration Policy

All projects are individual projects.

You may discuss general strategies, but each student is expected to produce his/her own design.

- OK: Discussing general strategies, helping eachother debug.
- Not OK: Producing a single solution on a whiteboard and individually coding it up.
- Not OK: “Borrowing” a friends implementation of a particular module.

Use your judgement about outside resources. (E.g., Reading wikipedia is fine, but asking stackoverflow.com to help debug your assembly code is not.)

In unclear situations, **ask**.

Read the CS Department’s Academic Honesty Policy

Regrade Policy

For objective errors only.

Must request in writing (via private Piazza post) within one week of scores being released.

Beauty Prizes

Vast majority of the scoring is objective.

As with code, style matters. Logic schematics not only capture your design, they express it.

For each project TAs will identify the 10 (or more) most elegant solutions and award a 10% extra credit “beauty prize”.

Projects must be functional in order to be eligible.

Registration and Wait List

This class is currently full.

If we can secure a larger lecture hall, we will increase cap.

The waitlist is being managed via EE advising office.

It is offered every semester.