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NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2018-2019

CE3001/CZ3001 – ADVANCED COMPUTER ARCHITECTURE

Apr/May 2019 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. An appendix on selected MIPS instructions is provided on Page 5.

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1. (a) Owing to an enhancement in the architecture of a processor, 60% of a program runs 12 times faster and the remaining 40% of the program runs 4 times faster. Find the overall speedup of the program due to this enhancement.

(5 marks)

(b) Consider machine M1 running at its maximum operating clock frequency of 200 MHz at operating voltage of 3 V. If the operating voltage of the processor is reduced to 1.5 V, find the percentage change in the dynamic power consumption and static power consumption, provided that the processor runs at its maximum possible clock frequency at 1.5 V.

(5 marks)

(c) Consider the following code segment in Listing Q1, which is intended to be executed in a 5-stage pipelined MIPS processor. Assume that write-back and register-read operations of different instructions can be performed in the same clock cycle.

Note: Question No. 1 continues on Page 2

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Listing Q1

```
I1                ADDI      $s1, $zero, #0xZYXV
I2                ADDI      $s2, $zero, #0x00C0
I3    Loop:       LW        $s0, 0 ($s2)
I4                INSTR     $s0, $s0, $s1
I5                SW        $s0, 0 ($s2)
I6                ADDI      $s2, $s2,    #0xFFFC
I7                BNE       $s2, $zero, Loop
```

(i) The 12th, 8th, 4th and 0th bits of the content of register $s0 need to be toggled. Determine the value of #0xZYXV and the INSTR.

(3 marks)

(ii) Identify the data dependencies in Listing Q1. Remove the data dependencies by inserting NOPs.

(5 marks)

(iii) Calculate the number of stall cycles needed for the execution of the code in Listing Q1, if full data forwarding is allowed. Show the forwarding paths across the instructions during pipelined execution. Find the steady state CPI with data forwarding. Assume that the program counter is updated with the branch target address at the execute stage. Also determine the number of iterations of the loop.

(7 marks)

2. (a) The hexadecimal value of the current content of the program counter (PC) in a MIPS processor is 0x500000AC as shown in Table Q2. The code needs to move to a PC value 0x500FFFAC. Identify and justify the control instruction (branch/jump) that needs to be used here and the required offset in hexadecimal for the control instruction.

Table Q2

Program counter value in hexadecimal	Instruction
0x500000A4	ADD $t1, $zero, $zero
0x500000A8	ADD $t0, $zero, $zero
0x500000AC	Branch / Jump to loop
----	-----
0x500FFFAC (loop)	ADD $t0, $t1, $t2

Note: Question No. 2 continues on Page 3

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Find the maximum and minimum addresses of the instruction memory to which the control of execution of a MIPS code could be moved forward and backward by the earlier identified control instruction.

(8 marks)

(b) Write a non-leaf MIPS procedure, 'Max', to find the largest number from an array of integers. Assume that the address of the first element of the array is stored in register $s1. Assume that you are given a function 'max-2'. The function 'max-2' takes two values from the registers $a0 and $a1, and returns the greater value through register $v0. Store the final result in memory location 0x00100304.

(12 marks)

(c) Name the three different kinds of hazards that introduce penalty stall cycles in a pipelined architecture. Give one example for each.

(5 marks)

3. (a) Consider a Byte-addressable memory with the address space of 32 bits. A 128 KB (1 KB = 1024 Bytes) eight-way set-associative cache is used for this memory system with the cache block size of 128 Bytes. Determine the number of bits for the tag, set index and block offset fields of the address, respectively.

(8 marks)

(b) Tables Q3a and Q3b show the actual miss rates and average memory access times for different cache block sizes of a given cache.

Table Q3a: Actual Miss Rate v.s. Block Size

Block Size (Bytes)	Cache Size			
	4KB	16KB	64KB	256KB
64	7.00%	2.64%	X%	0.51%
256	9.51%	3.29%	1.15%	0.49%

Table Q3b: Average Memory Access Time v.s. Block Size

Block Size (Bytes)	Cache Size			
	4KB	16KB	64KB	256KB
64	7.16	Y	1.93	Z
256	11.65	4.69	2.29	1.55

Note: Question No. 3 continues on Page 4

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(i) Assume that the hit time takes 1 clock cycle and the memory system takes 80 clock cycles of overhead and then delivers 16 bytes every 2 clock cycles. For example, it can supply 16 bytes in 82 clock cycles, 32 bytes in 84 clock cycles, and so on. Compute the missing entries X, Y and Z in Tables Q3a and Q3b.

(8 marks)

(ii) Which block size has smaller average memory access time for the cache size of 256K Bytes? Which block size has the minimum miss rate for the same cache size?

(6 marks)

(iii) Between miss rate and average access time, which one is more important to the cache performance?

(3 marks)

4. (a) Name the two different write policies to write on a cache and update the memory. Which one is more widely used considering the huge difference in speed between cache and memory?

(5 marks)

(b) A virtual memory has the page size of 1024 bytes, 8 virtual pages, and 4 physical page frames. The page table is given in Table Q4.

Table Q4

Virtual Page	Physical Page Frame
0	Not in the main memory
1	0
2	2
3	Not in the main memory
4	1
5	Not in the main memory
6	3
7	Not in the main memory

(i) List all the virtual addresses (in decimal) that would cause page faults.

(8 marks)

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(ii) Find the physical addresses (in decimal) for the virtual addresses of 1024 and 3071 in decimal, respectively.

(6 marks)

(c) We have learned different processor architectures. Examples include Application Specific Integrated Circuits (ASIC), Field Programmable Gate Array (FPGA) and Graphic Processing Unit (GPU).

(i) Among the three architectures listed above, which type of architecture could provide the best performance per unit power consumption, and which type of architecture has the best programmability?

(4 marks)

(ii) Is the big.LITTLE Architecture a homogeneous or heterogeneous computing system?

(2 marks)

Appendix: Syntax of Selected MIPS Instructions

Instruction Name	**Instructions Syntax**	**Meaning**
Add Word	ADD $rd, $rs, $rt	$rd ← $rs + $rt
Add Immediate Word	ADDI $rd, $rs, imm	$rd ← $rs + imm
And	AND $rd, $rs, $rt	$rd ← $rs & $rt
Load Word	LW $rd, offset ($rs)	$rd ← MEM[$rs + offset]
Store Word	SW $rd, offset ($rs)	MEM[$rs + offset] ← $rd
Branch on Not Equal	BNE $rs, $rt, offset	if $rs != $rt, PC ← PC + 4 + offset<<2
Branch on Equal	BEQ $rs, $rt, offset	if $rs == $rt, PC ← PC + 4 + offset<<2
Jump	J target	PC ← nPC[31-28]::target::00
Jump Register	JR $rs	PC ← $rs
Jump and Link	JAL target	$ra ← nPC; PC ← nPC[31-28]:: target::00

END OF PAPER

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1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.