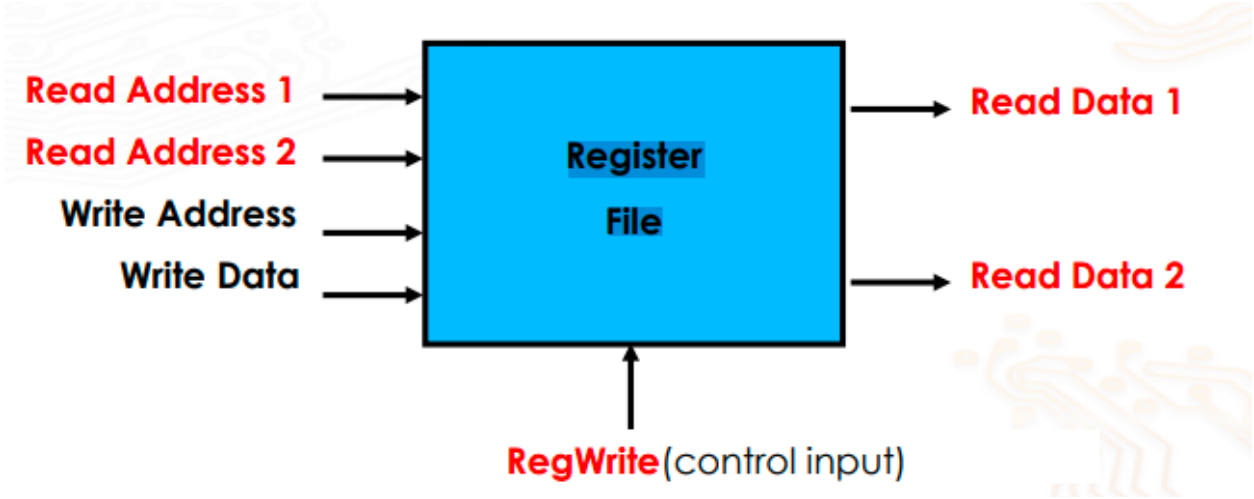
Module 3: Data path and Control Design

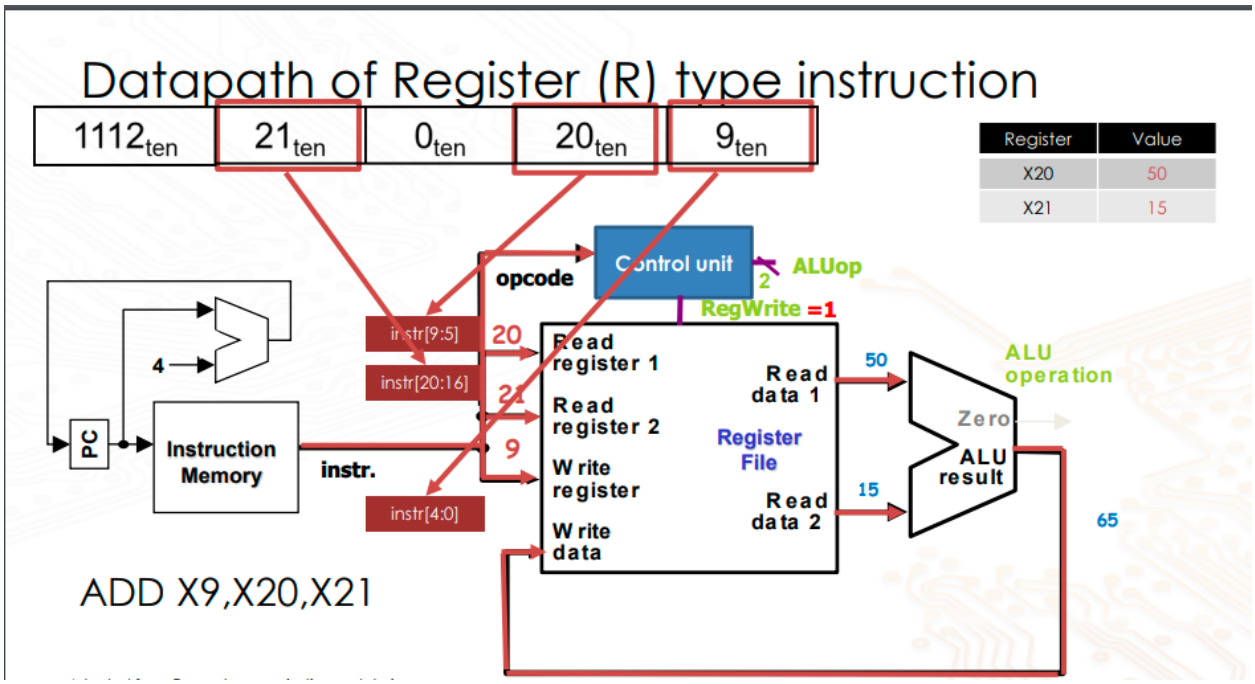
Review of basic logic devices and register file

- **ALU:** arithmetic ALU
- **Register file:** Consists of a set of registers that can be read and written by supplying a register to be accessed,



Single-cycle datapath design

- Datapath for R-type instructions

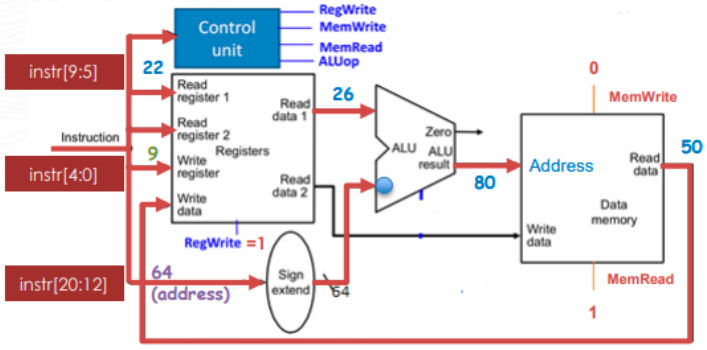


- Datapath for D-type instructions

Data transfer (D)type – Base addressing Part 3/4)

- Operation **LDUR Rt, [Rn, #address]**
- LDUR X9, [X22, #64] //[X9] ←mem[[X22] +64]

1986	64	0	22	9
Opcode 11 bits	Address 9 bits	Op2 2 bits	Rn 5 bits	Rt 5 bits



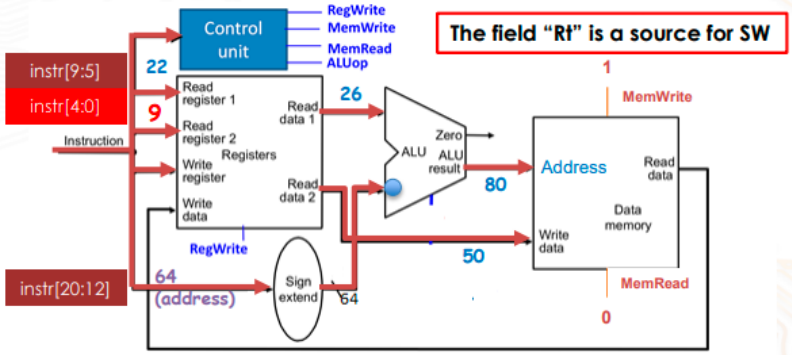
Register	Value
X22	26

Memory[80]
50

Data transfer (D)type – Base addressing Part 4/4)

- Operation **STUR Rt, [Rn, #address]**
- STUR X9, [X22, #64]] //[X9] →mem[[X22] +64]

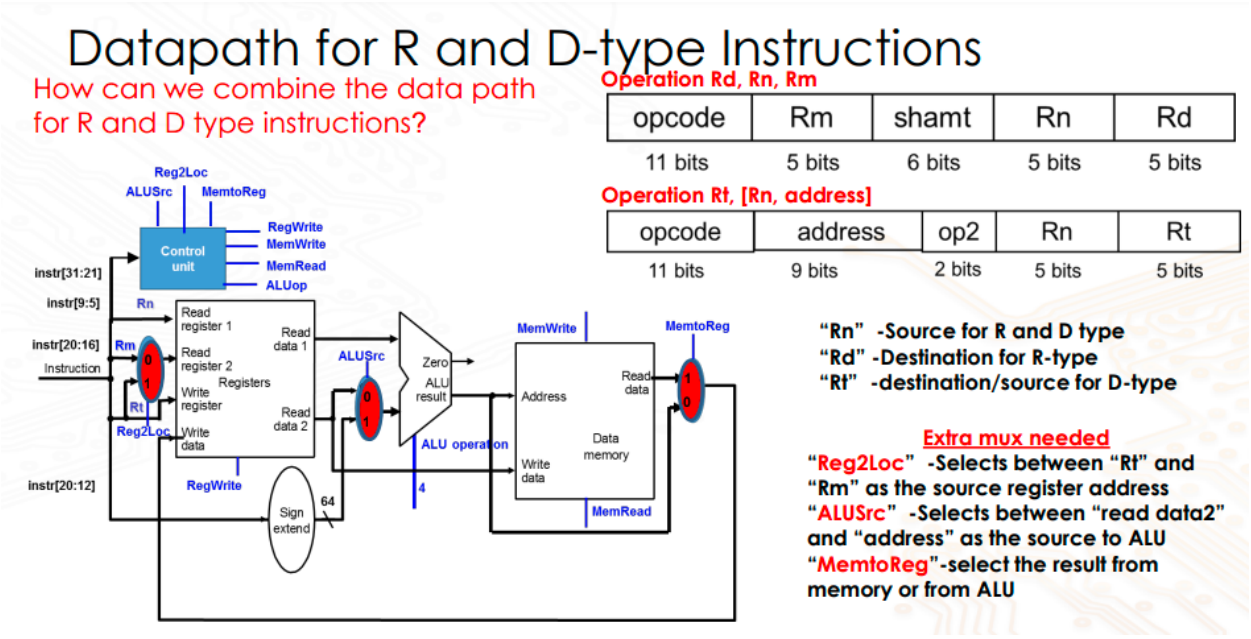
1984	64	0	22	9
Opcode 11 bits	Address 9 bits	Op2 2 bits	Rn 5 bits	Rt 5 bits



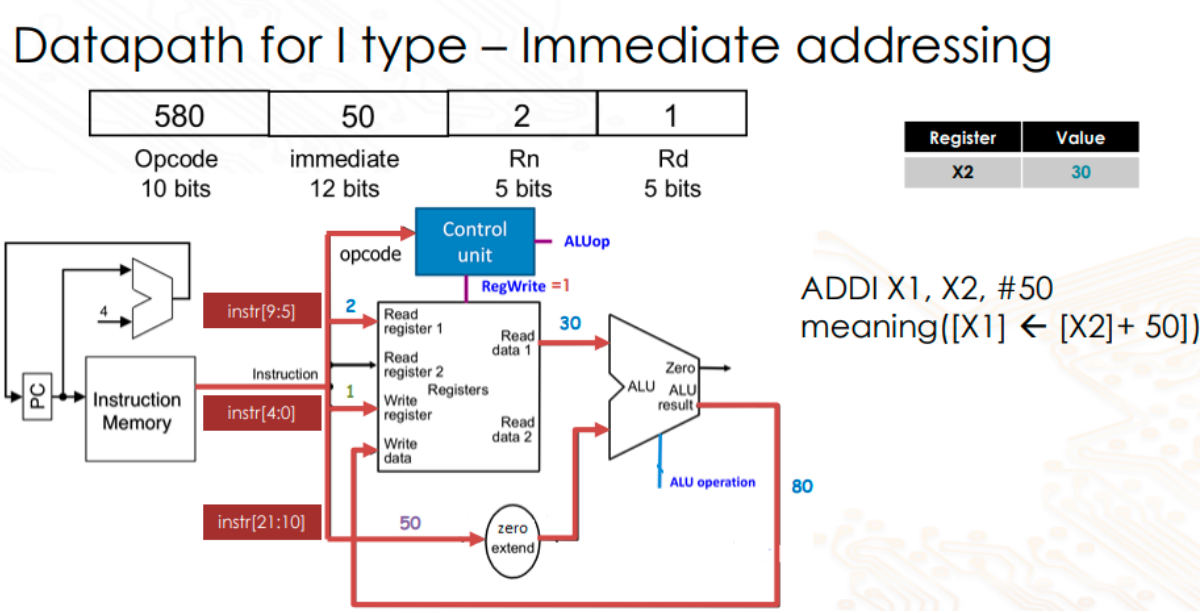
Register	Value
X22	26
X9	50

Memory[80]
50

- Combined datapath for R and D-type instruction

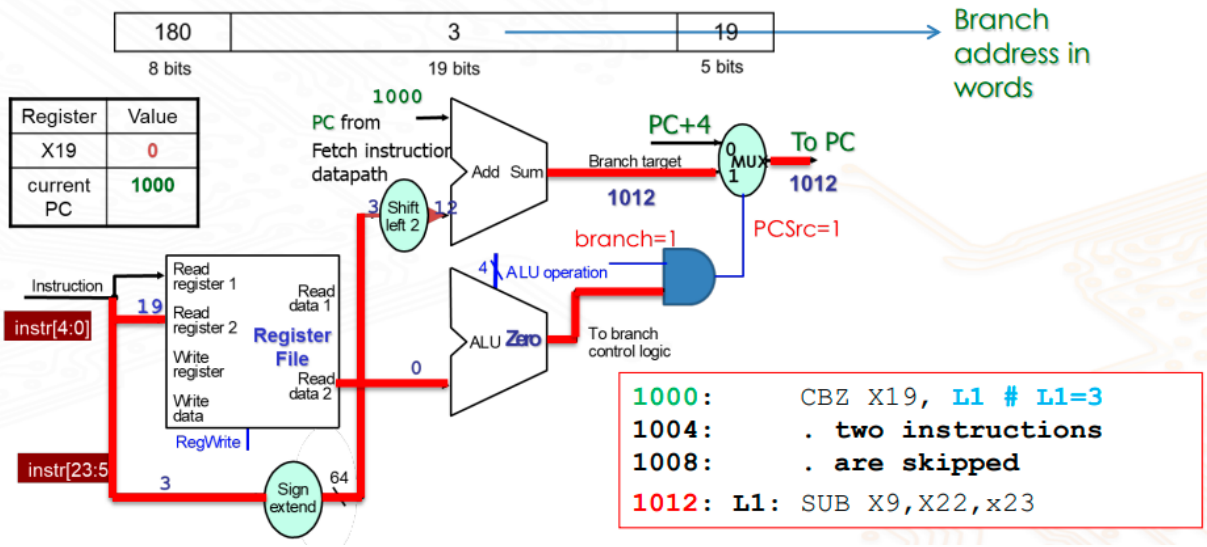


- Datapath for I-type instructions



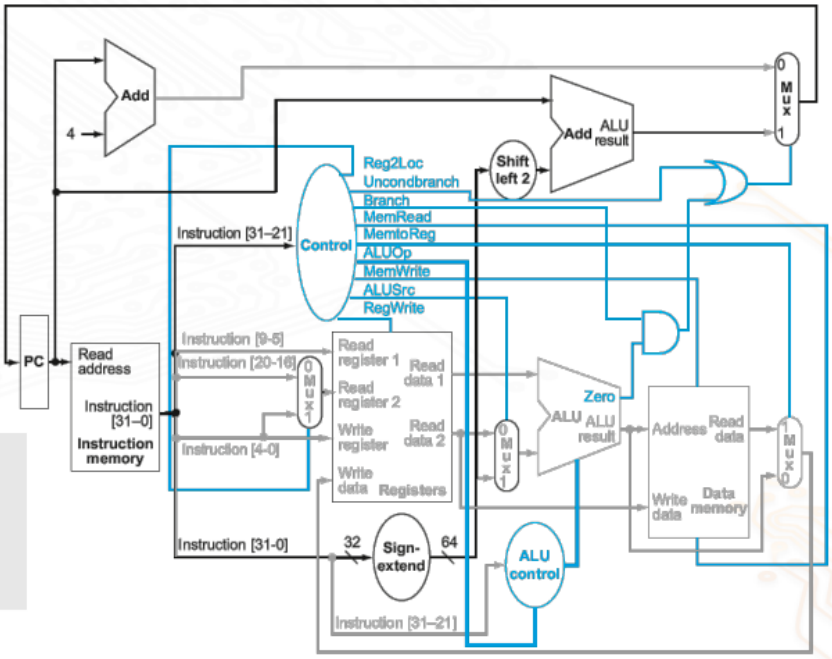
- Datapath for CB-type instructions

Datapath for CB type – Branch instruction



- Combined datapath for R,D, I, CB, and B-type instructions

Complete Datapath including B Instructions



B (B-type) datapath