CX20921 Far Field Voice Input Processor SoC Data Sheet

General Description

The CX20921 is a high-performance, far field voice input processor System-on-Chip (SoC). The CX20921 is the first product in this category with an integrated voice trigger function that supports a low system power Wake-on-Voice (WoV) function. The device includes 24-bit microphone Analog-to-Digital Converters (ADCs), a powerful dual core 32-bit hardware Digital Signal Processor (DSP), and integrated power management. Combined with Conexant's AudioSmart™ far field voice input processing software suite, including Smart Source Pickup (SSP) noise suppression and full-duplex Acoustic Echo Cancellation (AEC), the CX20921 is the ideal turnkey solution for adding voice control, voice search, and Voice over Internet Protocol (VoIP)/speakerphone functionalities to SmartTV, Set-Top Box (STB), Smart appliances, and automotive hands-free control and communication systems.

The CX20921 device supports a microphone array with up to two synchronized ADCs and programmable pre-amplifiers. Each pre-amplifier is paired with a dedicated bias supply to eliminate crosstalk. The entire input path guarantees 106dB dynamic range, which maximizes speech-to-noise ratio with low boost and prevents microphone saturation.

Conexant's proprietary far field AudioSmart software takes advantage of the built-in hardware to deliver a superior voice interactive experience in the most challenging room environments. The voice processing chain also supports multi-thread processing streams, which are independently optimized for voice communication and automatic speech recognition.

When ADC and DSP are active in the Wake-on-Voice (WoV) mode, the device consumes less than 70mW, which is well below the 0.5W European Commission (EC) 1275/2008 requirement for standby power.

Applications

- Voice-controlled Smart TV/STB
- Smart Bluetooth/WiFi speaker
- Voice interactive smart appliance
- Internet of Things (IOT) devices
- Automotive hands-free control/communication

Features

- Low-power WoV mode with an embedded third-party speech recognition engine
- Enables high-performance Automatic Speech Recognition (ASR) and excellent voice clarity with only two microphones through Conexant's AudioSmart voice input processing software, which includes:
  - SSP noise suppression
  - Full-duplex AEC
- Compatible with multiple leading embedded and server-based speech recognition vendors
- Dual far field, 24-bit, 106dB dynamic range ADCs with microphone pre-amplification and independent Microphone Bias (micbias) supply—enables low microphone gain for far field signals without saturating for loud near field signals
- Powerful, dual-core 32-bit DSP
- Multiple Integrated Interchip Sound (I^2S) serial data interfaces
- Inter-Integrated Circuit (I^2C) serial control interface
- Serial Peripheral Interface (SPI) for low-cost flash support

Revision History

Document No.	Release Date	Change Description
001DSR02	09/18/15	**Updated:** • "Pin Signal Definitions" table. • "Universal Asynchronous Receiver/Transmitter (UART)."
001DSR01	03/11/15	**Updated:** • "Pin Signal Definitions" table. • "Data Transfer on the I^2C Bus."
001DSR00	02/13/15	**Updated:** • Template. • Complete document update.
C	10/13//14	**Updated:** • "Package Thermal Data" table. **Added:** • "External SPI Flash Requirements and Approved Devices List." • "CX20921 Device PCB Footprint."
B	02/14/14	**Updated:** • "Ordering Part Number" table. • "Test Board and Conditions for Thermal Data" table. **Added:** • "Power Consumption."
A	06/07/13	Initial release.

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Introduction

Overview

The CX20921 is a high-performance, far field voice input processor SoC. The CX20921 is the first product in this category with an integrated voice trigger function that supports a low system power WoV function. The device includes 24-bit microphone ADCs, a powerful dual core 32-bit hardware DSP, and integrated power management. Combined with Conexant's advanced far field AudioSmart software, the CX20921 is the ideal turnkey solution for adding voice control, voice search, and VoIP functionalities to SmartTV, STB, automotive hands-free systems, and Smart appliances.

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Features

Cores

- C-programmable dual core 32-bit DSP (CAPE) with X and Y data, P memory spaces running at worst-case 200MHz, and yields 800MIPS
- Each core has dual Multiply-Accumulate (MAC) and dual memory
- Fixed point DSP with floating point assist
- Each MAC supports 32 x 24-bit and 64-bit accumulators
- Supports zero-overhead loop, circular buffers, and bit-reverse indexing
- 32-bit Arithmetic Logic Unit (ALU) that supports efficient bit manipulation
- Data memory access is 16-bit, 32-bit, and 64-bit
- Virtually all programming is done in C, using a very efficient C-compiler from Target
- Natively supported data types include: int, short, long, long long, Q15, Q23, Q8.23, and Q31

On-Chip Memory

Integrated memory 747KB SRAM and 66KB ROM:

- ROM = 46KB (Data) and 20KB (Program)
- RAM = 522KB (Data) and 225KB (Program)

Voice CODEC

- Two high performance ADCs with programmable pre-amplifiers
- Differential or single-ended microphone inputs
- Microphone or line input support
- ADC audio performance:
  - Dynamic range = 106dB at 0dB
  - THD+N = –84dB at –1dBFS
- Supported audio sample rates:
  - 8kHz
  - 16kHz
  - 24kHz
  - 32kHz
  - 44.1kHz
  - 48kHz
  - 96kHz
- Two microphone bias—one for each of the two ADCs. Supported voltage = 1.5V to 4.0V.
- Programmable pre-amplifier with integrated analog and digital gains:
  - Analog gain = 6dB to 24dB with 1dB steps
  - Digital gain = –74dB to 12dB with 0.125dB steps
- Smart gain controller adjusts the gain in both analog and digital to allow high dynamic range at different gains

Interfaces

- Universal Serial Bus (USB) 2.0 full-speed USB Audio Class (UAC):
  - Supports up to five endpoints
  - Fully configurable endpoints
- Stereo digital microphone Pulse Density Modulated (PDM) interface (muxed pin):
  - Clock frequency = 1.536MHz and 3.072MHz
  - Supported sample rates = 8kHz to 96kHz
  - Available gain boost range from 0dB to 48dB in 12dB steps
- I^2S:
  - Output supports:
    - Four-channel I^2S output available through pin muxing
    - Three-wire or six-wire digital audio interface
    - Master and slave configuration
    - 8kHz up to 192kHz sample rates
    - 8-bit, 16-bit, and 24-bit sample width
    - Left-justified and Right-justified mode (I^2S only)
  - Input supports:
    - Six-channel I^2S available through pin muxing
    - Four-wire or five-wire digital audio interface
    - Master and slave configuration
    - 8kHz up to 192kHz sample rates
    - 8-bit, 16-bit, and 24-bit sample width
    - Left-justified and Right-justified mode (I^2S only)
- SPI master:
  - Five-wire interface with two slave chip select outputs
  - Second slave chip select is optional through pin muxing
  - Maximum clock frequency up to 50MHz
- I^2C slave:
  - Maximum clock frequency of 1MHz
  - Control and boot
- One Universal Asynchronous Receiver/Transmitter (UART) interface—Maximum baud rate up to 1.5625Mbps
- Sony/Philips Digital Interface Format (S/PDIF) Receiver (RX) (muxed pin) that supports sample rates from 44.1kHz up to 192kHz
- One dedicated General Purpose Input/Output (GPIO)—One multiplexed with I2S_TX_CLK_2

Clocks

- 24MHz crystal clock
- On-chip programmable Phase Locked Loops (PLLs)—Five internal PLLs for the audio processor

Power Management

- Integrated Direct Current-to-Direct Current (DC-DC) converter

External Memory Interface Support

- Serial flash

Boot Device

- Serial Electrically Erasable Programmable Read-Only Memory (EEPROM)

Footprint

- 7mm x 7mm, 60-pin QFN, single row 0.4mm pitch

DSP Algorithms

***Conexant** DSP Algorithms*

- Multi-thread processing
- Multi-vendors speech recognition hit rate optimization
- Skype TV-certified Super Wide Band (SWB) far field voice processing with Watch Live and Talk
- Multi-channel AEC

Third-Party Digital Signal Processing (DSP) Algorithms with Royalties

- Speech recognition for voice wake function

Note: Contact Conexant's Sales Office for a more recent list of third-party algorithms.

Firmware and Software

- Small footprint Real-Time Operating System (RTOS)
- Drivers for all peripherals
- File system for SPI memory
- USB Human Interface Device (HID)
- Sculptor configuration toolbox

Hardware Interface

Block Diagram

The following figure shows the CX20921 block diagram.

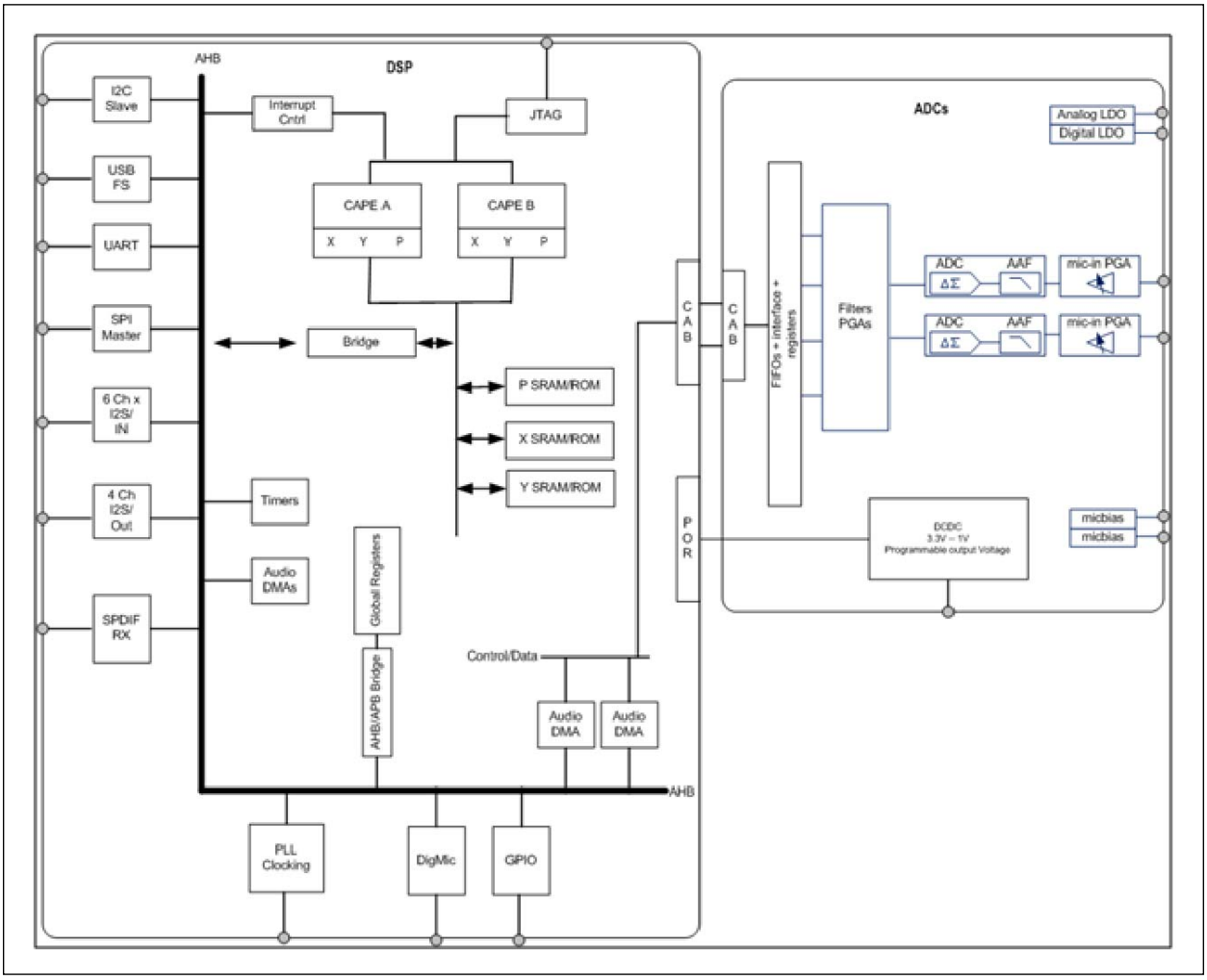


Figure 1: CX20921 Block Diagram

Pin Information

Pin Configuration

The following figure shows the CX20921 pin configuration.

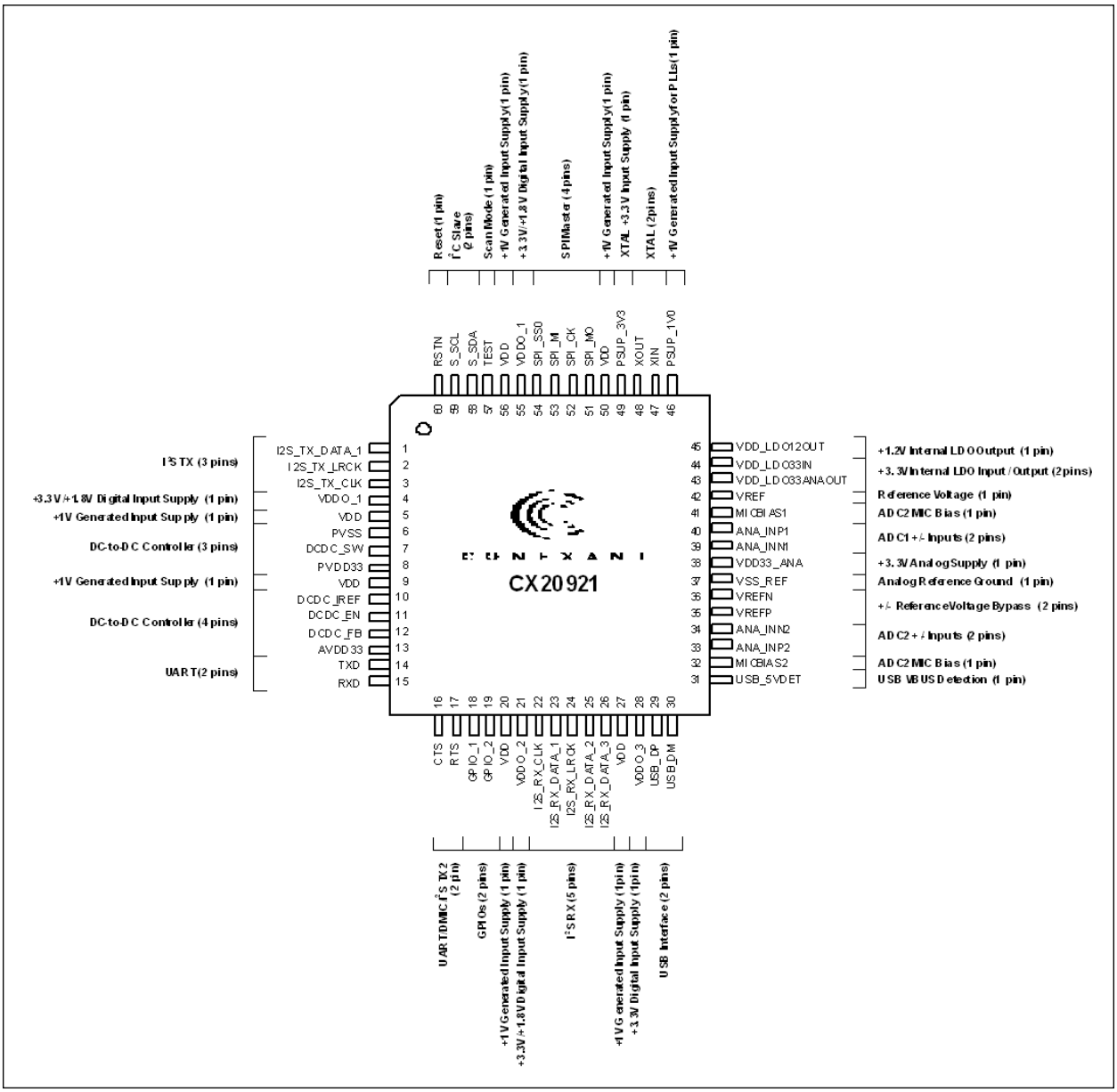


Figure 2: CX20921 Pin Configuration

Pin Signal Definitions

Table 1 provides the CX20921 pin description. The following lists the acronyms used in this table:

- AI = Analog In
- AO = Analog Out
- DI = Digital In
- DIO = Digital Input/Output
- DO = Digital Out
- PD = Pull-Down
- PU = Pull-Up
- PWR = Power

Table 1: Pin Signal Definitions

Label	Pin Number	I/O Type	Signal Name/Description
I^2S			
I2S_TX_DATA_1	1	DO	**I^2S Transmit Data.** Master/slave configurable using the control interface.
I2S_TX_LRCK	2	DIO	**I^2S Transmit Frame.** Master/slave configurable using the control interface.
I2S_TX_CLK	3	DIO	**I^2S Transmit Clock.** Master/slave configurable using the control interface.
DC-DC Controller			
DCDC_PVSS	6	Ground	**DC-DC Power Ground.**
DCDC_SW	7	PWR	**DC-DC Switch Pin.** Connect to the external filtering as indicated on the reference schematic.
PVDD33	8	PWR	**DC-DC 3.3V Power Stage Input Power Supply Input.** 3.3V—Connect to the external decoupling capacitor and system 3.3V.
DCDC_IREF	10	AO	**DC-DC Current Reference.** 3.3V—Connect to the PD 301K resistor.
DCDC_EN	11	AI	**DC-DC Enable Pin.** Output voltage from Low Drop-Out (LDO). Enables 3.3V to 1V buck conversion.
DCDC_FB	12	AI	**DC-DC Buck Output Feedback Scaled-Down Pin.**
AVDD33	13	PWR	**DC-DC Analog Power Pin.** 3.3V—Connect to the external decoupling capacitor and system 3.3V.
UART Interface			
TXD	14	DO	**UART Serial Transmission Data.** Muxed with the MCLK output.
RXD	15	DI	**UART Serial Receiving Data.**
CTS	16	DI	**UART Clear-to-Send (CTS).** Muxed with the DMIC_DATA and I2S_TX_LRCK2 signals.
RTS	17	DO	**UART Request-to-Send (RTS).** Muxed with the DMIC_CLK and I2S_TX_DATA_2 signals.
General GPIO			
GPIO_1	18	DIO	**General Purpose IO.** Programmable PU and drive control.
GPIO_2	19	DIO	**General Purpose IO.** Programmable PU and drive control. This pin is muxed with the I2S_TX_CLK2 signal.

Table 1: Pin Signal Definitions (Continued)

Label	Pin Number	I/O Type	Signal Name/Description
I²S Receive Interface			
I2S_RX_CLK	22	DIO	**I²S Receive Clock.** Master/slave configurable using the control interface.
I2S_RX_DATA_1	23	DI	**I²S Receive Data.** Master/slave configurable using the control interface.
I2S_RX_LRCK	24	DIO	**I²S Receive Frame.** Master/slave configurable using the control interface.
I2S_RX_DATA_2	25	DI	**Second I²S Receive Data.** Master/slave configurable using the control interface.
I2S_RX_DATA_3	26	DI	**Third I²S Receive Data.** Master/slave configurable using the control interface. This pin muxed with the SPDIF_IN signal.
USB Interface			
USB_DP	29	DIO	**USB Data Positive.** Positive channel of the USB bus data line.
USB_DM	30	DIO	**USB Data Negative.** Negative channel of the USB bus data line.
USB_5VDET	31	DI	**USB 5V Detect.** The USB 5V VBUS signal should be connected to a resistor divider to reduce the level to 3.3V at this pin.
Analog Voice CODEC			
MICBIAS2	32	AO	**ADC2 Micbias.** Output.
ANA_INP2	33	AI	**ADC2 Positive Input.** Differential or single-ended.
ANA_INN2	34	AI	**ADC2 Negative Input.** Differential or single-ended.
ANA_INN1	39	AI	**ADC1 Negative Input.** Differential or single-ended.
ANA_INP1	40	AI	**ADC1 Positive Input.** Differential or single-ended.
MICBIAS1	41	AO	**ADC1 Micbias.** Output.
References			
VREFP	35	Analog I/O	**Positive Reference Voltage Bypass.** DSM high-side sampling reference voltage.
VRERN	36	Analog I/O	**Negative Reference Voltage Bypass.** DSM high-side sampling reference voltage.
VSS_REF	37	Ground	**Analog Reference Voltage.** Analog LDO and micbias reference voltage.
VREF	42	Analog I/O	**Analog Reference Voltage.** Analog LDO and micbias reference voltage.
Crystal Signals			
XIN	47	DI	**Crystal In.** Connect to a 24MHz crystal circuit.
XOUT	48	DO	**Crystal Out.** Connect to a 24MHz crystal circuit return.
SPI Master Interface			
SPI_MO	51	DO	**SPI Master Data Out.**
SPI_CK	52	DO	**SPI Master Clock.**
SPI_MI	53	DI	**SPI Master Data In.**
SPI_SS0	54	DO	**SPI Master Slave Select.**

Table 1: Pin Signal Definitions (Continued)

Label	Pin Number	I/O Type	Signal Name/Description
Scan Mode			
TEST	57	DI	**Test.** Only to be used by a Conexant Test Engineer. Connect to a PD 10kΩ resistor.
I²C Slave Interface			
S_SDA	58	DIO	**I²C Slave Data Pin.** Connect pin to a PU resistor (typically 1.8K) going to VDDO_1. The I²C address is 0x41, with an available bond option for another address.
S_SCL	59	DI	**I²C Slave Clock Pin.** Connect pin to a PU resistor (typically 1.8K) going to VDDO_1.
Control Signals			
RSTN	60	DI	**Reset.** Active low input pin—Internal PU. During the initial power-up, the external reset should be asserted for a minimum of 100ms to allow all power supplies to be stable, and for the internal crystal start-up time from the power-up to become stable.
Generated Supplies			
VDD_LDO33ANAOUT	43	PWR	**3.3V Internal LDO Output Supply Pin.** 3.3V—Output of the analog LDO.
VDD_LDO12OUT	45	PWR	**1.2V Internal LDO Output Supply Pin.** 1.2V.
Input Supplies			
VDDO_1	4, 55	PWR	**3.3V/1.8V Digital I/O Power Pin.** Supply to the DIO blocks (e.g., I²S TX, I²C slave, and SPI master interfaces). Connect to 3.3V or 1.8V power depending on the interface signal voltage level requirements.
VDD	5, 9, 20, 27, 50, 56	PWR	**1V Digital Input Power Pin.** Core supply generated from the internal DC-DC. Connect to the output of the internal DC-DC after the filter circuit indicated on the reference schematic.
VDDO_2	21	PWR	**3.3V/1.8V Digital I/O Power Pin.** Supply to the DIO blocks (e.g., I²S RX, GPIOs, and UART interfaces). Connect to system 3.3V or 1.8V power depending on interface signal voltage level requirements.
VDDO_3	28	PWR	**USB Interface Power Supply Pin.** 3.3V—Connect to system 3.3V.
VDD33_ANA	38	PWR	**Analog Supply for ADCs PGA.** 3.3V—Should be sourced by the internal analog 3.3V LDO (VDD_LDO33ANAOUT).
VDD_LDO33IN	44	PWR	**Supply to Analog 3.3V LDO.** Connect to system 3.3V
PSUP_1V0	46	PWR	**Internal PLLs Power Supply Pin.** 1V—Connect to the internal DC-DC output. Refer to the reference schematic for the filtering requirement.
PSUP_3V3	49	PWR	**Xtal Circuit Power Supply Pin.** 3.3V—Connect to system 3.3V.
Ground Signal			
EP	61	Ground	**Ground.** Connect the device paddle to ground on the PCB.

Electrical Characteristics

Recommended Operating Conditions

Unless otherwise noted:

- T_A = 25°C
- Input supply = 3.3V, 1kHz signal
- Fs = 48kHz
- PGA gain = 0dB

Table 2: Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit	Comments
General					
Analog Voltage Supply (input to 3.3V LDO)	3	3.3	3.6	V	VDD_LDO33ANAOUT
Digital Core Power Supply	0.95	1	1.05	V	Voltage generated internally from the DC-DC (VDD, PSUP_1V0).
Digital I/O Supply	3	3.3	3.6	V	VDDO_1, VDDO_2, VDDO_3, and PSUP_3V3.
Ground (MGND, PGND, and DGND)	-	0	-	-	-
Microphone Input					
Input Signal Level	-	1xAVDD/3.3	-	Vrms	-
Signal-to-Noise Ratio (SNR) (A-Weighted)	-	106	-	dB	Microphone gain = 6dB (measured at the –60dBFS input).
Total Harmonic Distortion	-	–85	-	dB	Microphone gain = 0dB (measured at the –1dBFS input).
Power Supply Rejection Ratio	-	80	-	dB	At 217Hz.
Mute Attenuation	80	-	-	dB	-
Input Resistance	-	500	-	kΩ	Programmable to be 500K (default), 250K, 125K, and 25K.
Micbias					
Bias Voltage	1.5	-	4	V	-
Bias Current	-	-	10	mA	-
Noise in the Signal Bandwidth	-	–116	-	dBV	20kHz bandwidth.

Digital Inputs and Outputs

Table 3: Digital Inputs and Outputs

Signal Name	Supply Level
3.3V/1.8V Input Pads Cells	
SPI_MI	VDDO_1 = 3.3V/1.8V
S_SCL	VDDO_1 = 3.3V/1.8V
I2S_RX_DATA_1	VDDO_2 = 3.3V/1.8V
I2S_RX_DATA_2	VDDO_2 = 3.3V/1.8V
I2S_RX_DATA_3	VDDO_2 = 3.3V/1.8V
RXD	VDDO_2 = 3.3V/1.8V
CTS	VDDO_2 = 3.3V/1.8V
USB_5VDET	VDDO_3 = 3.3V
3.3V/1.8V Output Pads Cells	
SPI_MO	VDDO_1 = 3.3V/1.8V
SPI_CK	VDDO_1 = 3.3V/1.8V
SPI_SS0	VDDO_1 = 3.3V/1.8V
TXD	VDDO_2 = 3.3V/1.8V
RTS	VDDO_2 = 3.3V/1.8V
I2S_TX_DATA_1	VDDO_1 = 3.3V/1.8V
3.3V/1.8V I/O Pads Cells	
S_SDA	VDDO_1 = 3.3V/1.8V
I2S_RX_CLK	VDDO_2 = 3.3V/1.8V
I2S_RX_LRCK	VDDO_2 = 3.3V/1.8V
GPIO_1	VDDO_2 = 3.3V/1.8V
GPIO_2	VDDO_2 = 3.3V/1.8V
USB_DP	VDDO_3 = 3.3V
USB_DM	VDDO_3 = 3.3V
I2S_TX_LRCK	VDDO_1 = 3.3V/1.8V
I2S_TX_CLK	VDDO_1 = 3.3V/1.8V

Power Consumption

The following table provides the power consumption for typical firmware modes.

Table 4: Power Consumption

Mode	Enabled Functionalities	Power
SNN2	Two multi-channel AEC (2-CH), EQ, SSP, De-reverb, DRC, 16kHz output, no trigger. The SSP beam is set to extract a source placed in the center in the angular region between 10° and –10°, which is typically referred as a narrow-beam SSP. The DSP is tuned for natural language speech recognition.	49mA (161.7mW @ 3.3V)
SNW2	Two multi-channel AEC (2-CH), EQ, SSP, De-reverb, DRC, 16kHz output, no trigger. The SSP beam is set to extract the most dominant source from the background, and the main speaker can be anywhere as the angular region is set to 90° and –90°, which is typically referred as a wide-beam SSP. The DSP is tuned for natural language speech recognition.	49mA (161.7mW @ 3.3V)
MP16	Enables testing of the MIC input signal or the echo reference signals without any processing at the 16kHz output.	46mA (151.8mW @ 3.3V)
R6CH	Enables use of the USB port to record six channels simultaneously—Two-channel microphone and four-channel echo reference.	46mA (151.8mW @ 3.3V)

Interfaces

Universal Serial Bus (USB) 2.0

The CX20921 has a single USB two-device port, with an embedded USB 2.0 Transceiver Macrocell (UTM) Physical layer (PHY). The USB controller supports:

- Full-speed with a data rate of 12Mbps.
- Control, interrupt, bulk, and isochronous data transfer types.

General Purpose Input/Output (GPIO)

The CX20921 has two GPIOs:

- GPIO1 = A dedicated GPIO used for a WoV function that toggles to wake an external device when the CX20921 recognizes an audio wake trigger event.
- GPIO2 = A GPIO.

  Note: The GPIO2 is multiplexed with I2S_TX_CLK_2.

Direct Current-to-Direct Current (DC-DC) Converter—Internal 1V

The internal DC-DC 1V buck converter generates 1Vdc supply for the VDD digital core. The:

- Switching frequency = 1.536MHz.
- Wide range programmable output voltage range = 0V ~ 1.2V (1V typical use).
- Internal loop compensation minimizes the number of external components required.

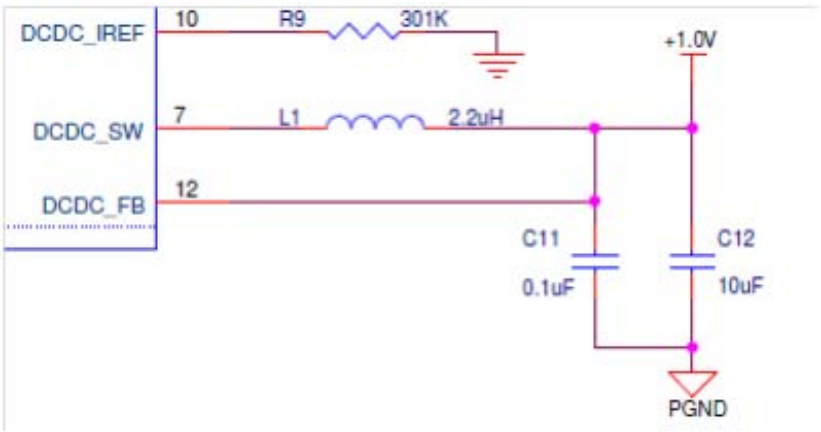


Figure 3: DC-DC Converter—Internal 1V

The following lists Conexant's DC-DC component recommendations:

- Inductor L1 = 2.2µH, low DCR <= 50mΩ, tolerance = ±20%.
- Capacitor C12 = 10µF, low ESR <= 50mΩ, tolerance = ±25%.

Table 5: DC-DC Converter Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Input Voltage Range	I_{LOAD} = 0A to 1A	3	3.3	3.6	V
Output Voltage	I_{LOAD} = 1A, 3.0V ≤ V_{IN} ≤ 3.6V, T_A = 25°C	0.95	1	1.05	V
Adjustment Step Size	-	-	4.7	-	mV
Number of Adjustment Steps	-	-	256	-	-
Adjustment Range	-	0	-	1.21	V
Output Voltage Ripple	-	-	3	-	%
Line Regulation	3.0V ≤ V_{IN} ≤ 3.6V, I_{LOAD} = 0A	-	3	-	%
Load Regulation	V_{IN} = 3.3V, 0A ≤ I_{LOAD} ≤ 1A	-	3	-	%
Full Load Efficiency	V_{IN} = 3.3V, I_{LOAD} = 1A	-	80	-	%
Load Current	V_{IN} = 3.3V	0	-	1	A
Overshoot/Undershoot	Instant Δ I_{LOAD} = ±1A	-	200	-	mV
Start-up Time	-	-	10	-	ms
Quiescent Current	V_{IN} = 3.3V, I_{LOAD} = 0A	-	300	-	uA
Switching Frequency	V_{IN} = 3.3V	-	1.536	-	MHz

Reset (Active Low)

During initial power-up, the external reset should be held low for a minimum of 100ms to allow all power supplies to become stable and for the internal crystal to stabilize. Refer to the customer reference schematic for Resistor-Capacitor (RC) circuit values and connections.

Serial Peripheral Interface (SPI) Master

The CX20921 offers an SPI master interface that is intended to interface with SPI slave devices, such as serial flash. The SPI block consists of a TX and an RX First In, First Out (FIFO) that is 8x32 bits with several registers for control and status. The SPI interface accommodates various controls for clock polarity, a phase shift of the clock, and slave select polarity.

The SPI clock is derived from the PLL_SPI_CLK and can be programmed by a field in the control register. Two slave selection signals are available to allow use of two different SPI peripherals (SS0, SS1).

Note: The SPI_SS1 is multiplexed with UART_CTS, DMIC_DATA, and I2S_TX_DATA_2.

Table 6: SPI Interface Signals

Signal Name	I/O	Def	Function
SPI_CLK	O	NA	Maximum of 50MHz.
SPI_MI	I	NA	Master serial data IN.
SPI_MO	O	NA	Master serial data OUT.
SPI_SS0	O	NA	Chip select 0.
SPI_SS1	O	NA	Chip select 1.

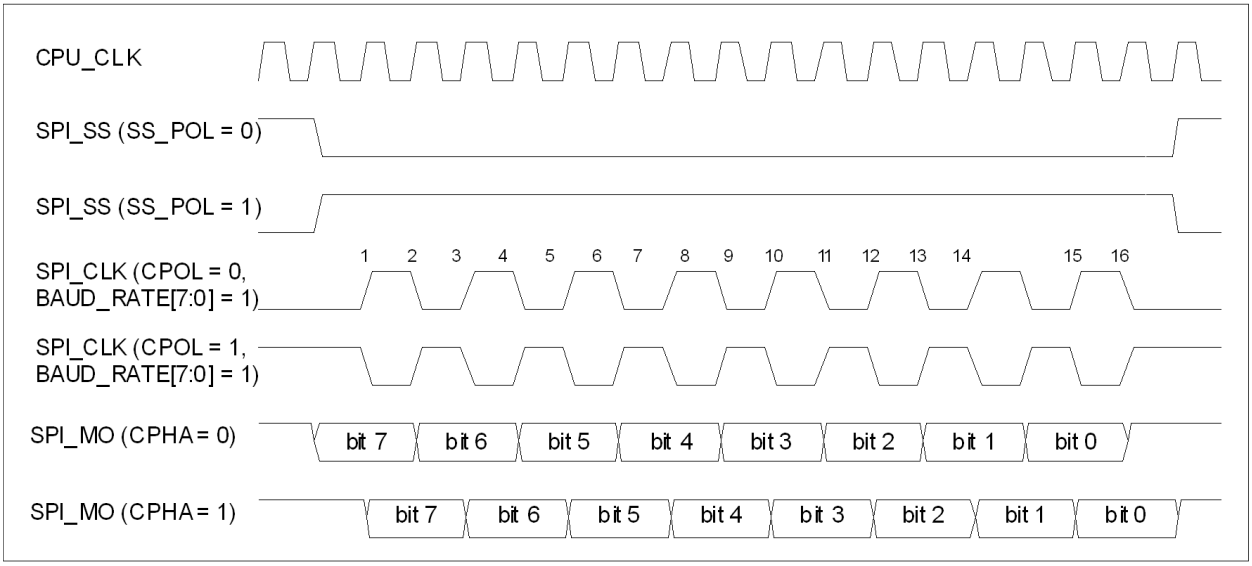


Figure 4: SPI Transmit Timing

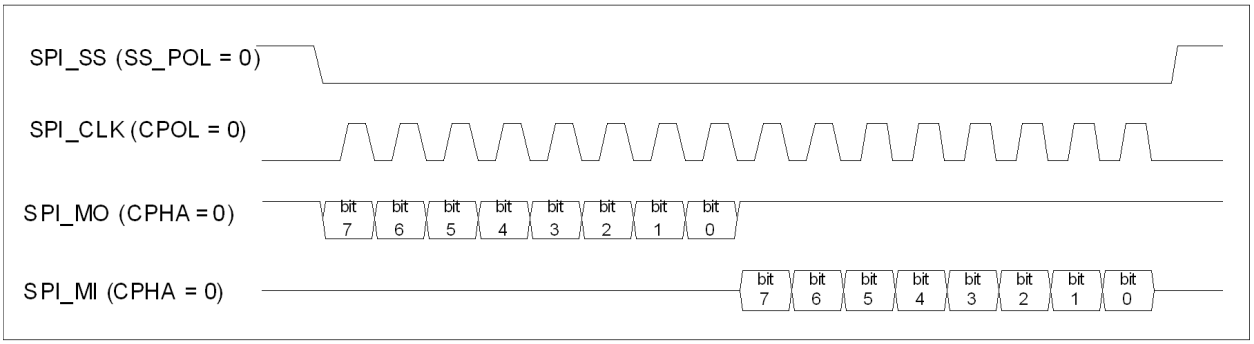


Figure 5: SPI Transmit and Receive Timing

External SPI Flash Requirements and Approved Devices List

When using an external SPI flash device, the following requirements must be met:

- Flash device must support 4KB block/sector erase opcode (0x20).
- Flash device must support read opcode (0x03) at a clock rate of at least 12MHz.
- Up to 128Mb flash device can be supported—the address field in the opcode should be 24-bit.
- Flash device must support Read ID opcode (0x9F).

The following lists the Conexant-approved SPI flash devices:

- AT25DF041A
- AT25DQ161
- AT25DQ321A
- AT25DF641
- AT25DF321A
- GD25Q80B
- GD25Q32B
- GD25Q64B
- MX25L4006E
- MX25L3206E
- MX25L6406E
- SST25VF016B
- W25Q16DV
- W25Q32FV
- W25Q64FV
- W25Q128FV

Inter-Integrated Circuit (I^2C) Slave

The CX20921 supports a single I^2C slave interface. The I^2C slave is a standard I^2C slave, with address hexadecimal 0x41.

I^2C Data Flow Communication

The following steps describe how to write to the CX20921 device.

1. Send a START sequence.
2. Send the I^2C address of the slave.
3. Send the register address for a write (24-bit).
4. Send the data bytes (4-byte data).
5. Optionally, send any further data bytes (e.g., burst operation).
6. Send the STOP sequence.

The following steps describe how to read from the CX20921 device.

1. Send a START sequence.
2. Send the I^2C address of the slave.
3. Send the register address (24-bit).
4. Send a START sequence (repeated START).
5. Read the data bytes (4-byte data).
6. Optionally, read any further data bytes in case of a burst read mode.
7. Send the STOP sequence.

Data Transfer on the I²C Bus

Every byte put on the Serial Data (SDA) line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. The data is transferred with the Most Significant Bit (MSB) first, as shown in the following figure.

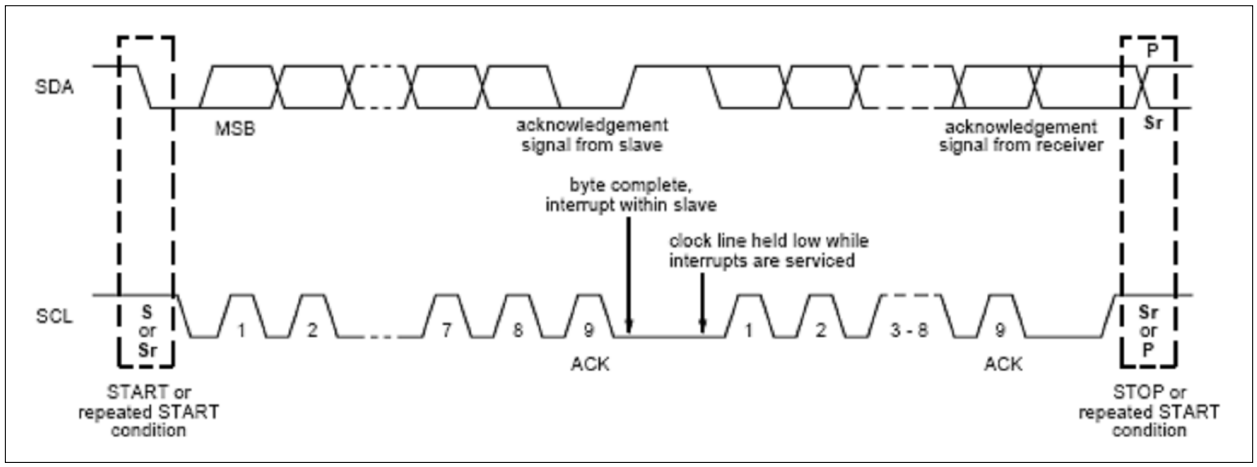


Figure 6: I²C Bus Transactions

A HIGH to LOW transition on the SDA line while the Serial Clock Line (SCL) is HIGH is a special case that indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

Both START and STOP conditions are always generated by the I²C master. The I²C bus is considered to be busy after the START condition, and then free again a certain time after the STOP condition.

The following figure shows the data transfer format on the I²C bus.

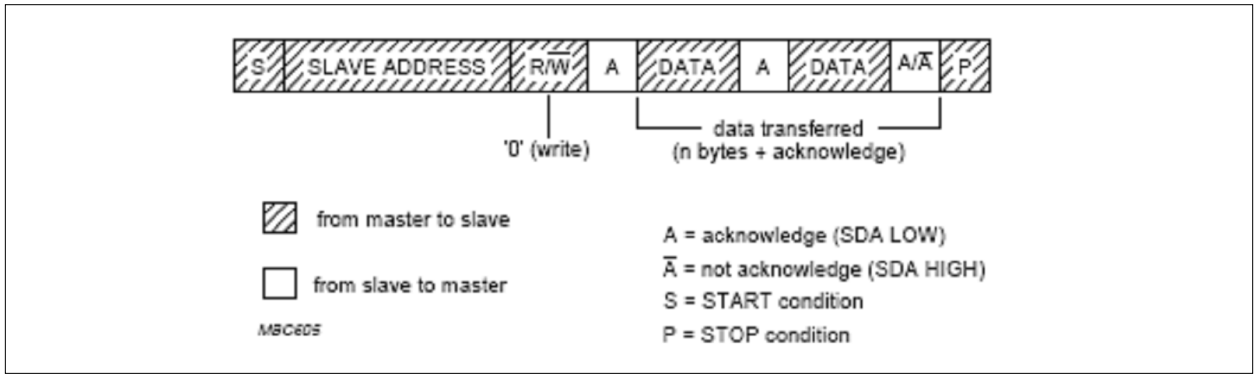


Figure 7: I²C Data Transfer Format

I²C Slave Address Format

The following table lists the slave addressing format for I²C.

Table 7: I²C Slave Address Format

Slave Address	R/W Bit	Description
0000 000	0	General call address.
0000 000	1	START byte.
0000 001	X	CBUS address.
0000 010	X	Reserved for a different bus format.
0000 011	X	Reserved for future purposes.
0000 1XX	X	Hs mode master code.
1111 1XX	X	Reserved for future purposes.
1111 0XX	X	10-bit slave addressing.

I²C Interface Timing for 400kHz Mode

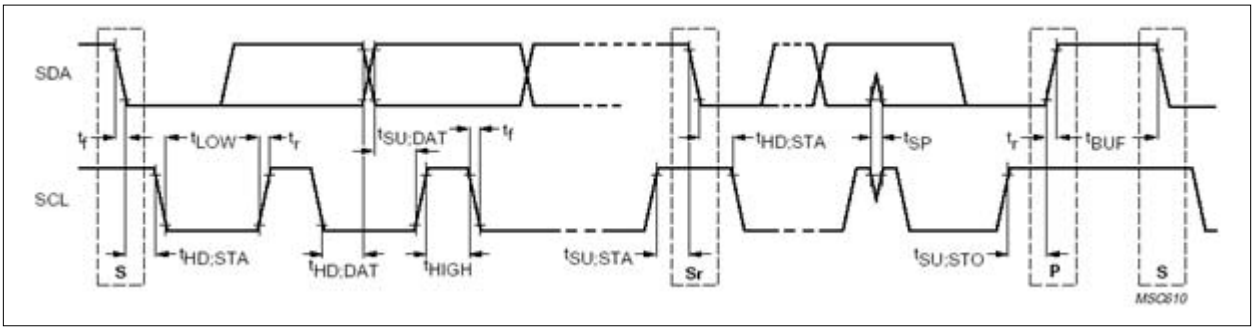


Figure 8: Interface Timing Requirements for 400kHz Transfer

Table 8: Interface Timing Requirements for 400kHz Transfer

I²C (400kHz)	Symbol	Minimum	Maximum
Set-up Time START Condition	$t_{SU.STA}$	0.6µs	-
Hold Time START Condition	$t_{HD..STA}$	0.6µs	-
SCL Clock Low Period	t_{LOW}	1.3µs	-
SCL Clock High Period	t_{HIGH}	0.6µs	-
Data Set-up Time	$t_{SU.DAT}$	100ns	-
Data Hold Time	$t_{HD.DAT}$	0	0.9µs
Set-up Time for STOP Condition	$t_{SU.STO}$	0.6µs	-

Universal Asynchronous Receiver/Transmitter (UART)

The internal UART with Flow Control (FC UART) is compatible with a standard 16550 UART. The added features of the FC UART over the 16550 are higher clock frequency and a flow control mechanism.

The UART functions include RX, TX, CTS, and RTS.

Note:

- RTS is multiplexed with DMIC_CLK and I2S_TX_LRCLK_2.
- CTS is multiplexed with DMIC_DATA, SPI select 1 (SPI_SS1), and I2S_TX_DATA_2.
- TXD is multiplexed with MCLK output.

The UART operates at 115,200bps, no parity bit, 8 data bits, and 1 STOP bit. Only the UART TX/RX signals are needed to download new firmware images to the SPI flash device through the CX20921. The RTS/CTS are not needed for firmware downloads.

Digital Microphone Interface (DMIC)

The CX20921 supports one digital microphone external interface using a two-wire interface. The Digital Microphone Interface (DMIC) supports stereo operation and supports independent sample rates from 8kHz to 96kHz.

The supported clock frequencies are 1.536MHz and 3.072MHz. The left-channel microphone data is latched on the falling edge of the clock, and sent by the microphone on the rising edge of the clock. Conversely, the right-channel microphone data is latched on the rising edge of the clock, and sent by the microphone on the falling edge of the clock.

Note:

- DMIC_CLK is multiplexed with UART_RTS and I2S_TX_LRCLK_2.
- DMIC_DATA is multiplexed with UART_CTS, SPI select 1 (SSI_SS1), and I2S_TX_DATA_2.

The available gain boost ranges are from 0dB to 48dB, in 12dB steps.

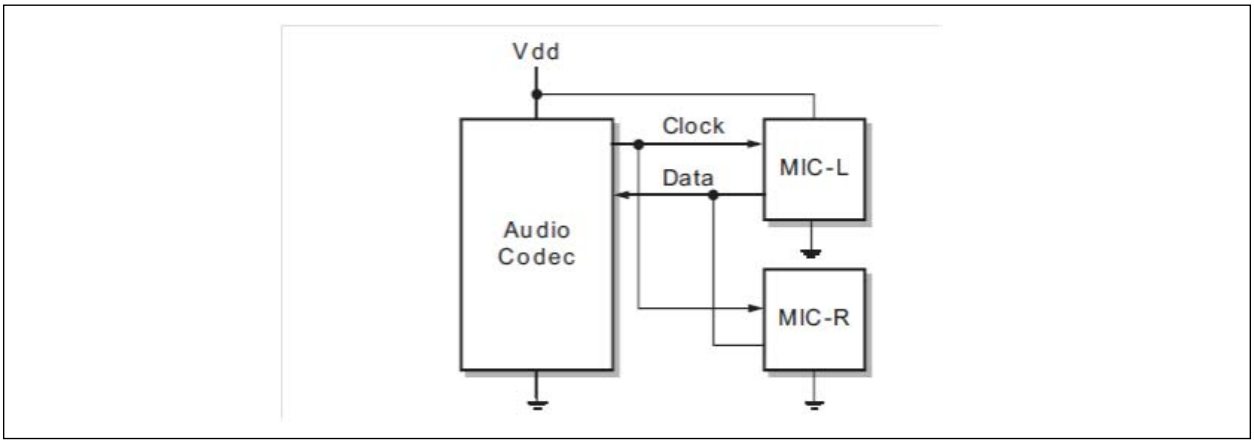


Figure 9: DMIC

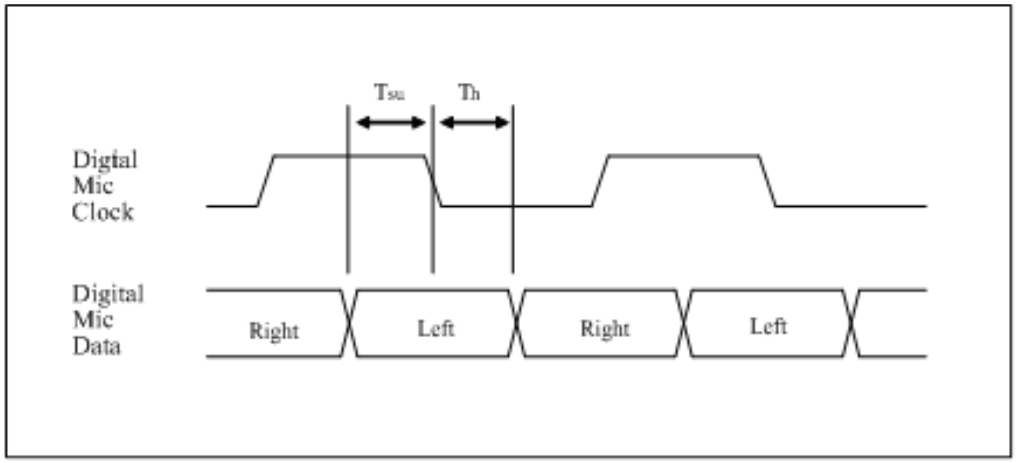


Figure 10: DMIC Timing

Table 9: DMIC Parameters

Parameter	Symbol	Value	Units	Comments
Clock Frequency	F	1.536 3.072	MHz	-
Output Low (Maximum)	V_{ol}	0.4	V	-
Output High (Minimum)	V_{oh}	2.6	V	-
Input Low (Maximum)	V_{il}	0.94	V	-
Input High (Minimum)	V_{ih}	1.20	V	-
Setup (Minimum)	T_{su}	36	ns	The Setup and Hold parameters apply to both left channel (falling edge of clock) and right channel (rising edge of clock).
Hold (Minimum)	T_h	0	ns	The Setup and Hold parameters apply to both left channel (falling edge of clock) and right channel (rising edge of clock).

Sony/Philips Digital Interface Format (S/PDIF) Receiver

The CX20921 supports the industry-standard IEC 60958 digital audio interface, also known as S/PDIF.

The S/PDIF receiver is a serial, uni-directional, self-clocking interface for the interconnection of digital audio equipment. The S/PDIF provides a digital audio interface for receiving and playback of audio. The audio data is coded in PCM format with a resolution of 16-bits or 24-bits per sample.

The S/PDIF receiver supports sample rates from 44.1kHz up to 192kHz.

Note: The SPDIF_IN signal is multiplexed with I2S_RX_DATA_3.

Integrated Interchip Sound (I^2S)

The CX20921 supports independent three-wire TX and five-wire RX interfaces. Each interface can be set for master or slave mode. The:

- TX and RX interfaces can be powered independently.
- TX three-wire mode consists of signals BCLK, LRCLK, and TX_DATA.
- RX five-wire mode consists of signals BCLK, LRCLK, and RX_DATA_1, RX_DATA_2, RX_DATA_3

Note: The I2S_RX_DATA_3 is multiplexed with SPDIF_IN.

Both interfaces support audio sample rates from 8kHz up to 192kHz for both record and playback. The supported sample widths are 8-bit, 16-bit, and 24-bit.

The CX20921 supports standard I^2S mode, left-justified mode, and right-justified mode.

Note:

- I2S_TX_LRCLK_2 is multiplexed with DMIC_CLK and RTS.
- I2S_TX_DATA_2 is multiplexed with DMIC_DATA, SPI select 1 (SSI_SS1), and CTS.
- I2S_TX_CLK_2 is multiplexed with GPIO2.

I²S Mode Timing

The I²S timing uses the WS (LRCK) to define whether the data is being transmitted for the left channel or for right channel. The WS is low for the left channel, and high for the right channel. A WS polarity control bit is provided to allow either high or low to represent the left channel. The default setting of the polarity control is 0, which means a low WS = left channel. The WS does not need to be symmetrical. A system clock (BCLK) running at a minimum of 2 x (sample width +1) sample frequency is used to clock in the data. There is a delay of one clock bit from the time the WS signal changes state to the first data bit on the data line. The data is written MSB first, and is valid on the rising edge of the bit clock. When the programmed sample width is taken, any remaining bits are ignored.

In the following figure, the width of the LRCK frame is wider than 2N bits (N=8, 16, or 24).

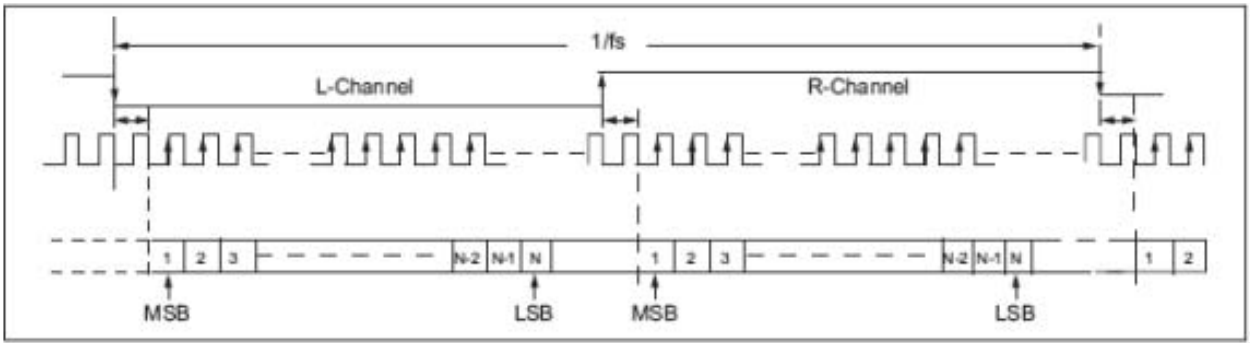


Figure 11: I²S Timing Diagram

Important! When dealing with I²S, take care when the number of bits in the sample word matches the number of clocks per frame. Because true I²S requires a one clock shift of the data, the Least Significant Bit (LSB) of each word arrives after the WS signal changes state (shown in Figure 12). To handle this correctly, the internal channel indicator should only change state after the bit count is reached and the state of WS does not match the expected value for the current channel.

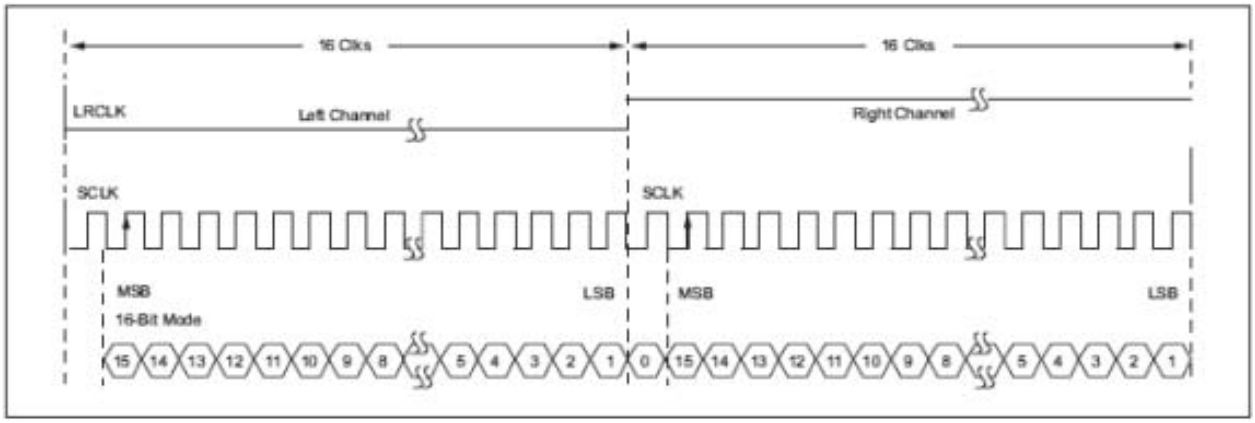


Figure 12: I²S Timing Diagram—16 Bits per Channel I²S

Left-Justified Mode

Left-justified timing uses the WS clock to define when the data being transmitted is for the left channel or the right channel. The WS is high for the left channel, and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. The first data bit appears on the data lines at the same time WS toggles. The data is written MSB first, and is valid on the rising edge of bit clock. When the programmed sample width is taken, any remaining bits are ignored. If the WS toggles before the full word length is read, the remaining bits are zeroed.

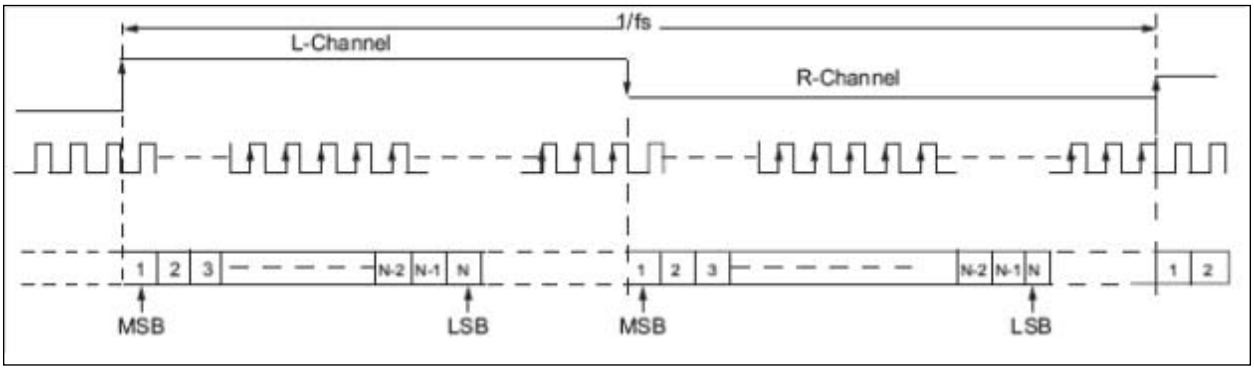


Figure 13: Left-Justified Timing Diagram

Right-Justified Mode

Right-justified timing uses the WS clock to define whether the data is being transmitted for the left channel or right channel. The WS is high for the left channel, and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. Data is captured in a 24-bit shift register until the WS toggles. When the WS toggles the last 24 bits, 16 bits or 8 bits are transferred to the channel indicated by the previous state of WS. In right-justified mode, the LSB of data is always clocked by the last bit clock before the WS transitions. The data is written MSB first and is valid on the rising edge of bit clock. All leading bits are ignored.

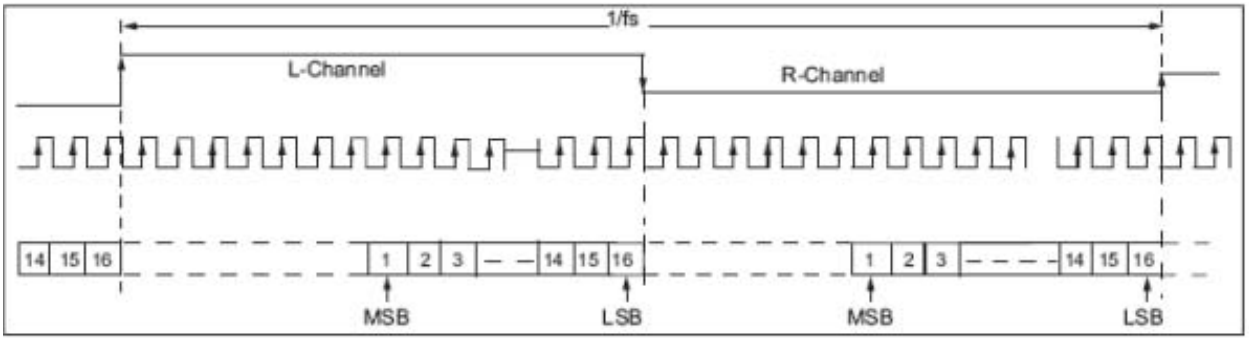


Figure 14: Right-Justified Timing Diagram

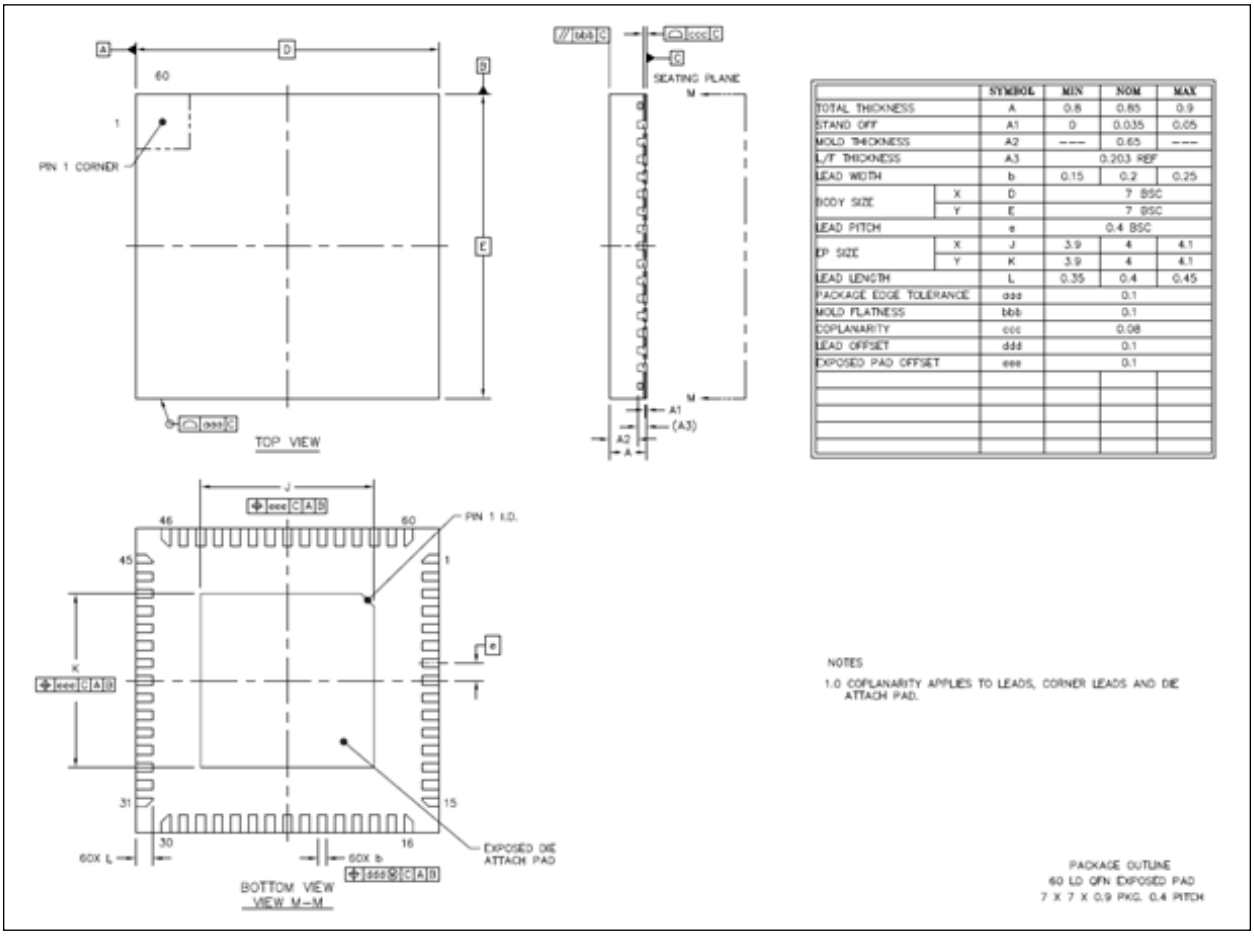
Multiplexed Signals

The following table summarized the several pins that are multiplexed in the CX20921 device.

Table 10: Multiplexed Signals

Signal	Muxed Function	Comment
GPIO2	GPIO	GPIO.
	I2S_TX_CLK_2	I^2S out 2 stereo CLK.
RTS	RTS	FC UART.
	DMIC_CLK	Digital microphone CLK.
	I2S_TX_LRCLK_2	I^2S out 2 stereo LRCK.
CTS	CTS	FC UART.
	DMIC_DATA	Digital microphone data.
	SPI_SS1	SPI master 2 slave select.
	I2S_TX_DATA_2	I^2S out 2 stereo data.
I2S_RX_DATA_3	I2S_RX_DATA_3	I^2S in 3 stereo data.
	SPDIF_IN	S/PDIF in shared.

Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 15: Package Dimensions: 60-Pin QFN

Package Thermal Data

Table 11: Package Thermal Data

Item	Description
Die Power (W)	0.817
Ambient Temperature Maximum/Minimum (°C)	70/0 (CX20921-21Z) 85/–40 (CX20921-99Z)
Junction Temperature Maximum/Minimum (°C)	125/0
Storage Temperature Maximum/Minimum (°C)	125/–40
Θ_{TA} Maximum (°C/W)	32.7
ψ_{JT} Maximum (°C/W)	0.248
ψ_{JB} Maximum (°C/W)	6.411

Table 12: Test Board and Conditions for Thermal Data

Item	Description
Size (in mm)	76.2 x 114.3
Motherboard Thickness (in mm)	1.6 ± 10%
Motherboard Material	FR-4
Number of Layers in Motherboard	4

Note: The data is based on the JEDEC JESD51-5 test board.

CX20921 Device PCB Footprint

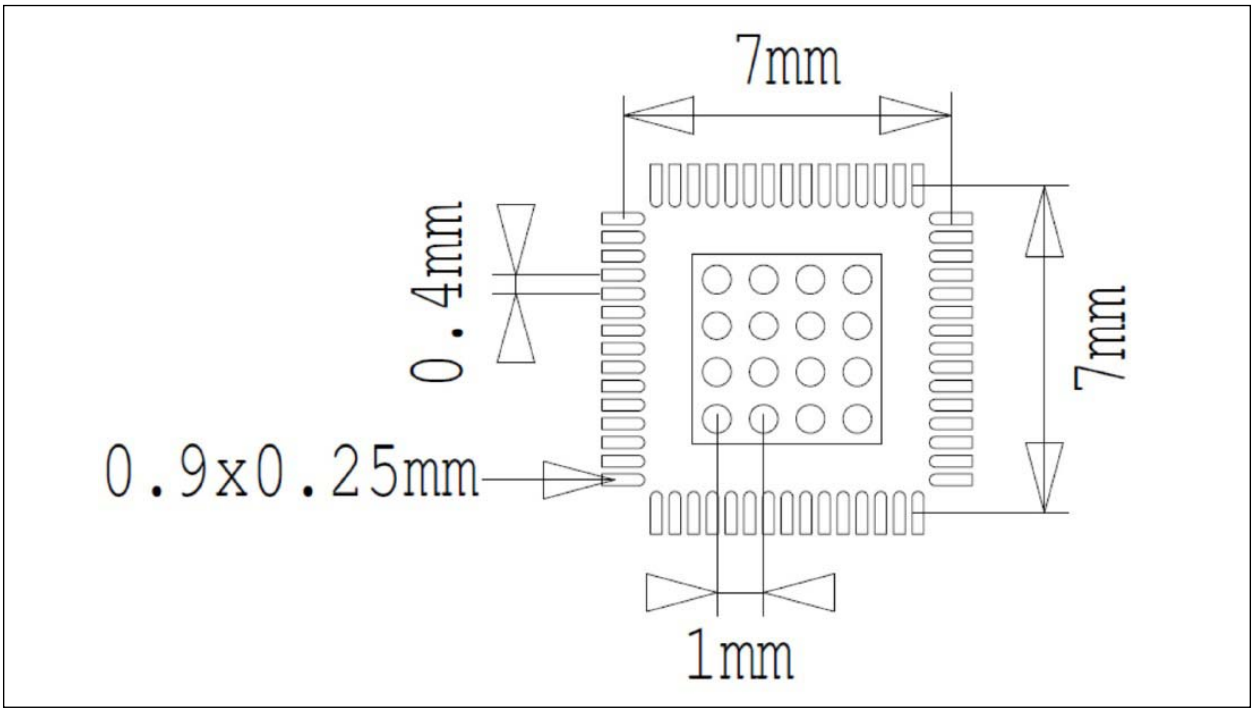


Figure 16: CX20921 Device PCB Footprint

Ordering Information

Table 13: Ordering Information

Device Part Number	Part Number	Description	Package
CX20921-21Z	CX20921	Far field voice input IC.	60-QFN 7mm x 7mm
CX20921-99Z	CX20921	Adds extended temperature range support.	60-QFN 7mm x 7mm

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