BP1048B2 Datasheet

High Performance 32-bit Bluetooth Audio Processor

Versions:

Date	Version	Description
2019/6	V0.2	Preliminary English version

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1. Overview

Core and Memory

- High performance 32-bit RISC core, @ max. 288MHz, supports DSP instruction, with floating-point unit(FPU) integrated
- FFT/IFFT accelerator supports operations of up to 1024 complex numbers or 2048 real numbers
- 320KB on-chip SRAM, 32KB I-Cache and 32KB D-Cache
- Internal 16M bits FLASH code and data storage
- EFUSE configuration register
- 2-wire SDP(Serial Debug Port), break-point and code tracking debug
- 40 interrupt vectors
- 4-level interrupt priority

Audio

- Four audio ADC, SNR≥94dB, 9 sampling rate: 8KHz / 11.025KHz / 12KHz / 16KHz / 22.05KHz / 24KHz / 32KHz / 44.1KHz / 48KHz
- Support up to 4 digital microphones or 2 analog microphone with AGC
- ADC line-in supports single-end or differential input
- Three audio DAC, SNR≥105dB, 9 sampling rate: 8KHz / 11.025KHz / 12KHz / 16KHz / 22.05KHz / 24KHz / 32KHz / 44.1KHz / 48KHz
- Directly drive earphone of 16Ω or 32Ω with power of 40mW
- Two duplex I2S(or IIS), sampling rate 8K~192Kbps, max. 32bits
- One half-duplex S/PDIF supporting HDMI audio and ARC

Bluetooth

- Dual mode Bluetooth V5.0, compatible with Bluetooth V4.2 and V2.1+EDR
- Support Piconet and Scatternet networking protocols
- Maximum transmit power is 10dBm, support class1, class2 and class3
- Receiving sensitivity (T.B.D)
- Support A2DP/AVRCP/HFP/HSP/OPP/HID/SPP/PBAP/GATT/SM profiles
- Support PLC(Package Loss Concealment)

Power, Clock and Reset

- DC 3.3~5V power supply @ LDOIN
- Internal LDOs: 5V to 3.3V and 3.3V to 1.2V
- RC 12MHz and two PLL clocks
- Support 24MHz crystal
- Internal POR(Power on Reset), LVD(Low-Voltage-Detection) and Watchdog
- Multiple low-power options: CPU clock frequency reduction, system clock frequency reduction, sleep, deep sleep

Timer, PWM and PWC

- 2 basic timers (TIM1, TIM2)
- 4 general timers (TIM3, TIM4, TIM5, TIM6), with PWM and PWC function

Peripherals

- Max. 28 GPIOs
- All GPIOs support external interrupt and wakeup
- GPIOs configurable: pull-up, pull-down, Hi-impedance , pull-down current source, etc
- USB 2.0 Full-speed OTG controller and PHY, 6 endpoints

- One SPI master(SPIM) @ max.60M
- One SPI slave(SPIS) @ max.60M
- One SDIO @ max.30M
- Two duplex UART @ max.3Mbps, the UART0 with flow control
- One I2C master/slave controller @ max.400K
- 12-bit SAR-ADC @ max. 450K sampling rate, sampling from 12 external IOs or 2 internal voltages
- One IR interface, supports NEC or SONY mode
- True random number generator

DMA

- 8-channel DMA, all memory direct addressing, addresses can be assigned to any peripherals except OTG, IR and I2C
- Unique automatic transmit-and-capture mechanism for memory and IO matching, or DMA-GPIO, can simulate various communication and controlling timing

SDK Firmware Stack and IDE

- Audio algorithm list:

  Decode: MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV(IMA-ADPCM & PCM), AIF, AIFC

  Encode: MP2/MP3, IMA-ADPCM
- Sound effects:

  Echo, Reverb, 3D, Virtual bass, Auto-tune/pitch shifter/Voice changer, EQ, DRC, AEC, Noise suppression, Frequency-shifting, Screaming detection and suppression
- SDK includes abound of examples and middleware
- Free Eclipse-based IDE and GCC compiler
- Support FreeRTOS
- All C programming, easy for porting

Firmware Programming and Protection

- Multiple flash programming supported: debugger, specific burner/programmer, or Flash Burner Lite
- Firmware upgradable with Dual-bank
- 32-bit customized key for firmware encryption
- On-chip 64-bit unique ID

ESD

- HBM 2KV ESD capability

Package and Operational Temperature

- LQFP48-7x7mm
- Working temperature: -40℃ ~ 85℃

Application Fields

- Bluetooth audio speaker
- Bluetooth Karaoke equipment
- Bluetooth Headphone
- Bluetooth Car audio
- Multiple microphone system for intelligent voice application with Bluetooth

2. Functional Block Diagram

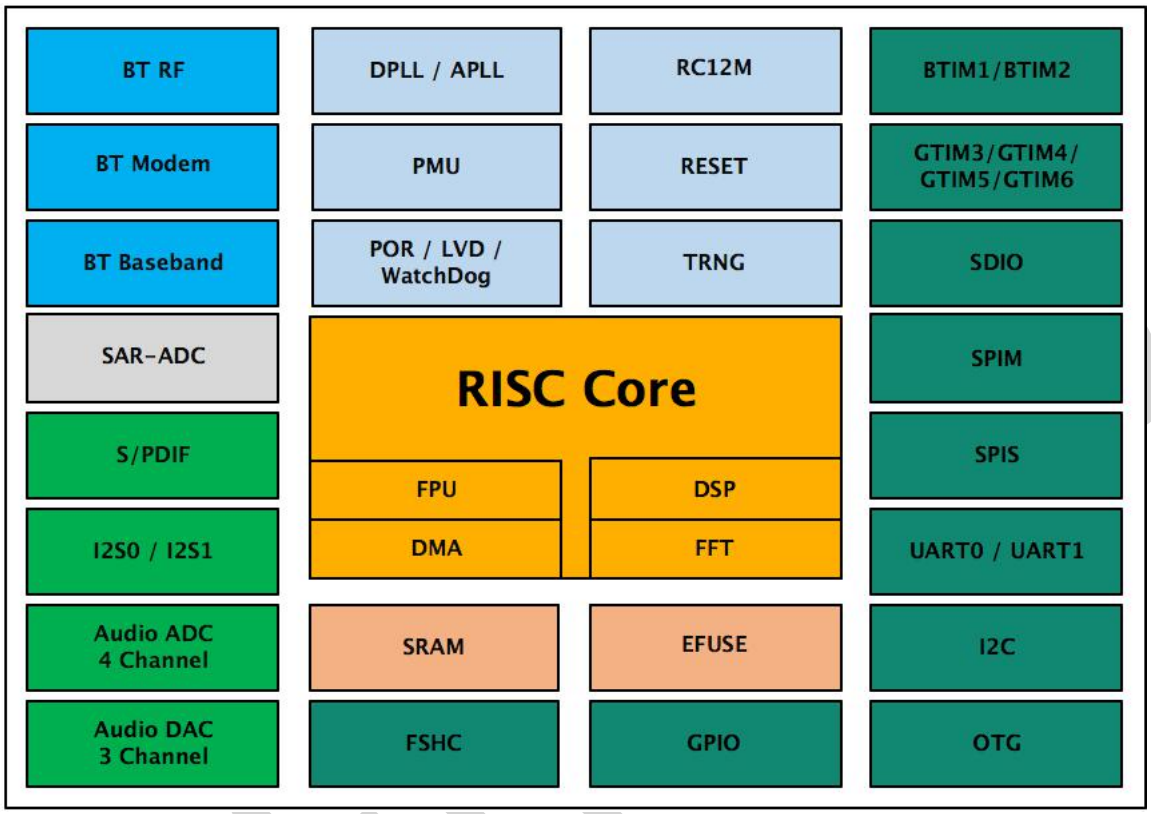

Figure 1. Functional Block Diagram of BP1048B2

3. Pin Definition

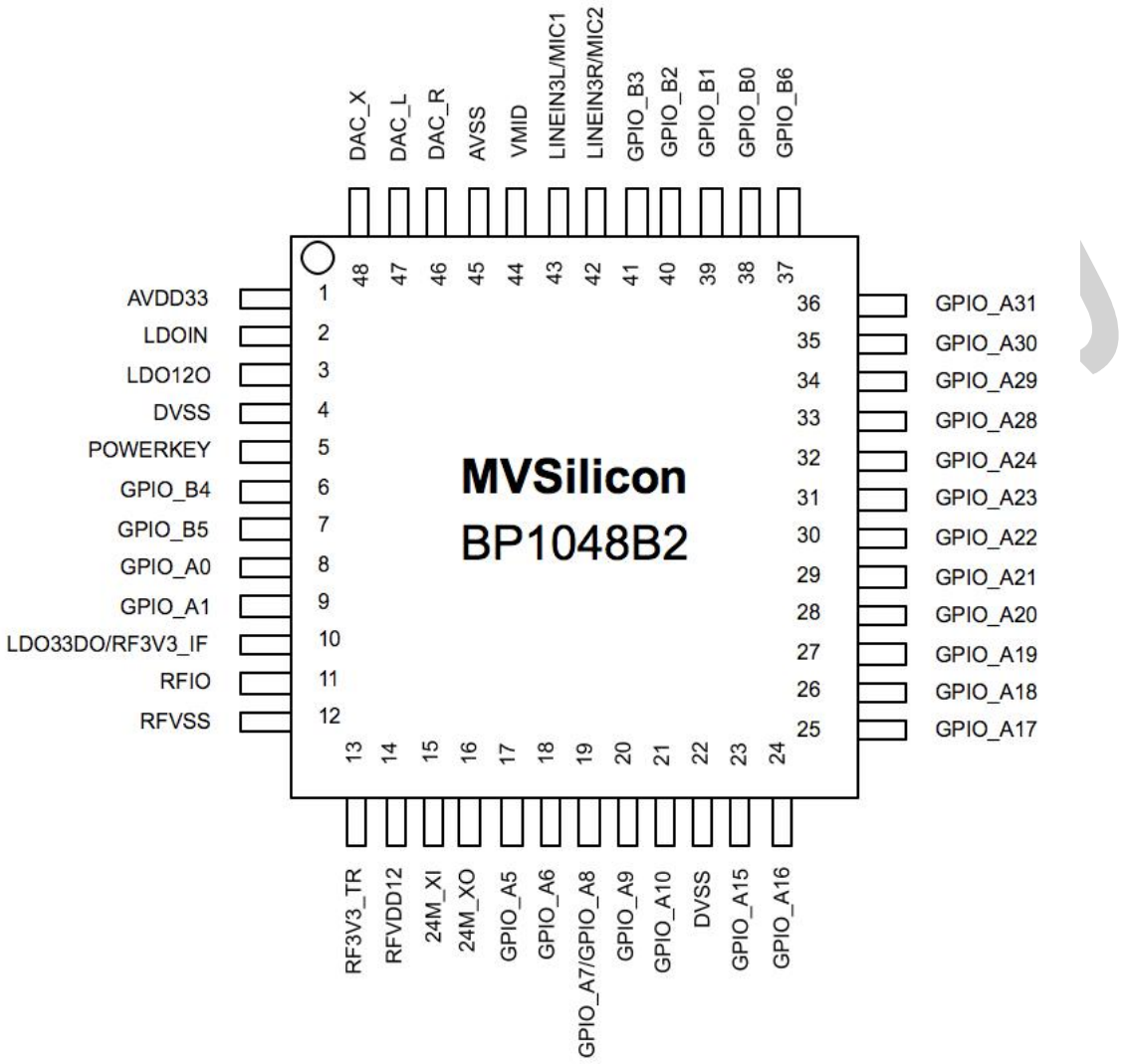

Figure 2. Pin Definition

4. GPIO Pin Description

Table 1. Pin definition

Pin#	Pin Name	Type	Other multiplexing function(s)
1	AVDD33	PWR	Analog power output, external filter capacitor is required
2	LDOIN	PWR	Power input for whole chip
3	LDO12O	PWR	1.2V core power, external filter capacitor is required

4	DVSS	GND	Digital ground
5	POWERKEY	I	Configurable power key, also be used as an ADC channel (AD11)
6	GPIO_B4	I/O	I2C_SDA
7	GPIO_B5	I/O	I2C_SCL
8	GPIO_A0	I/O	UART0_RXD / UART0_TXD / I2S0_MCLK_OUT / I2S0_MCLK_IN / TIM3_PWM
9	GPIO_A1	I/O	UART0_TXD / UART0_RXD / TIM4_PWM
10	LDO33DO / RF3V3_IF	PWR	Digital 3.3V power output, external filter capacitor is required / RF power 3.3V input
11	RFIO	AI/AO	RF antenna port
12	RFVSS	GND	RF ground
13	RF3V3_TR	PWR	RF power 3.3V input
14	RFVDD12	PWR	RF power 1.2V output, external filter capacitor is required
15	24M_XI	I	24M crystal XI
16	24M_XO	O	24M crystal XO
17	GPIO_A5	I/O	SPIM_MOSI / UART0_RXD / I2C_SDA
18	GPIO_A6	I/O	SPIM_CLK / UART0_TXD / I2C_SCL
19	GPIO_A7 / GPIO_A8	I/O	SPIM_MISO / UART0_CTS / I2S1_MCLK_OUT / I2S1_MCLK_IN / UART0_RTS / I2S1_LRCLK / TIM3_PWM
20	GPIO_A9	I/O	UART1_RXD / I2S1_BCLK / TIM4_PWM
21	GPIO_A10	I/O	UART1_TXD / I2S1_DO / I2S1_DI / TIM5_PWM
22	DVSS	GND	Digital ground
23	GPIO_A15	I/O	SD_DAT
24	GPIO_A16	I/O	SD_CLK
25	GPIO_A17	I/O	SD_CMD
26	GPIO_A18	I/O	USB_DM / UART1_RXD
27	GPIO_A19	I/O	USB_DP / UART1_TXD
28	GPIO_A20	I/O	AD0 / SD_DAT / SPIM_MOSI / SPIS_MOSI / I2S0_LRCLK / I2S1_LRCLK
29	GPIO_A21	I/O	AD1 / SD_CLK / SPIM_CLK / SPIS_CLK / I2S0_BCLK / I2S1_BCLK
30	GPIO_A22		AD2 / SD_CMD / SPIM_MISO / SPIS_MISO / I2S0_DO / I2S0_DI / TIM3_PWM
31	GPIO_A23	I/O	AD0 / SPIS_CS / I2S0_DI / I2S0_DO / TIM4_PWM
32	GPIO_A24	I/O	AD1 / I2S0_MCLK_OUT / I2S0_MCLK_IN / TIM5_PWM
33	GPIO_A28	I/O	AD5 / SPDIF_AI_0 / I2S1_LRCK / SPDIF_DI / SPDIF_DO / TIM4_PWM
34	GPIO_A29	I/O	AD6 / SPDIF_AI_1 / I2S1_BCLK / SPDIF_DI / SPDIF_DO / CLK_OUT / IR
35	GPIO_A30	I/O	AD7 / SPDIF_AI_2 / I2C_SDA / I2S1_DO / I2S1_DI / SPDIF_DI / SPDIF_DO / DMIC1_DAT
36	GPIO_A31	I/O	AD8 / SPDIF_AI_3 / I2C_SCL / I2S1_DI / I2S1_DO / SPDIF_DI / SPDIF_DO / DMIC1_CLK
37	GPIO_B6	I/O	EFUSE VDD / CLK_OUT / IR
38	GPIO_B0	I/O	LINEIN4_R / AD9 / TIM5_PWM / SW_CLK
39	GPIO_B1	I/O	LINEIN4_L / AD10 / TIM6_PWM / SW_D
40	GPIO_B2	I/O	LINEIN5_R / DMIC0_DAT
41	GPIO_B3	I/O	LINEIN5_L / DMIC0_CLK
42	LINEIN3_R / MIC2	AI	Analog audio input or MIC2 input
43	LINEIN3_L / MIC1	AI	Analog audio input or MIC1 input

44	VMID	AO	Bias voltage for audio module internal use
45	AVSS	GND	Analog ground
46	DAC_R	AO	Audio right-channel output
47	DAC_L	AO	Audio left-channel output
48	DAC_X	AO	Audio x-channel output

Note:

1) Pad types:
   I: digital input; O: digital output; AI: analog input; AO: analog output; I/O: bi-directional input/output; PWR: Power; GND: Ground
2) All GPIOs are grouped into A, B. Group A has 22 signals and Group B has 7.
3) BP1048B2 is a CMOS device and all unconnected GPIO pins are supposed to be set to pull-up or pull-down in order to avoid the unnecessary power consumption cause by the electric charge accumulation.
4) GPIOs response differently with the different type of resets:
   a) If Power-on-Reset (POR) is active, GPIOs will be reset as input and be set to high-impedance as indicated in table 2.
   b) If Watchdog reset or software SYSTEM RESET is active, GPIOs, based on the register configuration, can either keep the previous status(multiplexing, input/output or pull-up/down setting) before the reset or be set as the same as described in a) or table 2.

Table 2. GPIO State and Electric level (POR)

Pin(s)	Type	Electric level
GPIO_A[1:0]	Floating	High Impedance
GPIO_A[10:5]	Floating	High Impedance
GPIO_A[24:15]	Floating	High Impedance
GPIO_A[31:28]	Floating	High Impedance
GPIO_B[6:0]	Floating	High Impedance

5) When the POWERKEY is not used, please keep the POWERKEY pin unconnected. Do not short to the ground or LDOIN.

5. Electrical Characteristics

5.1 Working condition for BP1048B2

Table 3. Working Condition of BP1048B2

Parameter	Pin	Min	Typ	Max	Unit
Ambient temperature		-40		85	℃
Power supply for chip	LDOIN	3.3		5	V
Power supply for analog modules	AVDD		3.3		V
Internal LDO for digital power supply	LDO33DO		3.3		V
Core working voltage	LDO12O		1.2		V

5.2 Digital IO Electrical Characteristics

Table 4. Digital IO DC Characteristics

Symbol	Meaning	Min.	Typ.	Max.	Unit	Testing Condition
VIH	Input High	2.2		3.6	V	VDD33=3.3V
VIL	Input Low	-0.3		1.0	V	VDD33=3.3V
IL	Input leakage current	-10		10	uA	
VOH	Output High	3.0			V	@IOH=8mA
VOL	Output Low			0.3	V	@IOL=8mA

Table 5. Digital IO Driving and Pull-Up/Down Capability

Name	IOs	Normal	Enhanced	Unit	Testing Condition
Driving Capability	GPIO_A[10:5] / GPIO_A[17:15] / GPIO_A24 / GPIO_A[31:30]	8	24	mA	VDD33=3.3V, typical
	GPIO_A[1:0] / GPIO_A[23:18] / GPIO_A[29:28] / GPIO_B[3:0] / GPIO_B[6]	4	8	mA	VDD33=3.3V, typical
	GPIO_B[5:4]	19	34	mA	VDD33=3.3V, typical
Pull-up	All GPIOs	20	70	uA	VDD33=3.3V, typical
Pull-down	All GPIOs	20	70	uA	VDD33=3.3V, typical
Pull-down current source	GPIO_A[10:5] / GPIO_A[17:15] / GPIO_A24 / GPIO_A[31:30] / GPIO_B[5:4]	1.3	2.6 / 1.3+2.6	mA	VDD33=3.3V, typical
	GPIO_A[1:0] / GPIO_A[23:18] /		2.6	mA	VDD33=3.3V, typical

	GPIO_A[29:28] / GPIO_B[3:0] / GPIO_B[6]				

5.3 Audio Performance

Table 6. Audio DAC performance@44.1KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				24	Bits
Full Scale Output Signal Level	AVDD=3.3V		1.067		Vrms
Sampling frequency		8		48	KHz
Dynamic Range	A-Weighted, 1KHz -60dBFS input signal		105		dB
Signal to Noise Ratio	A-Weighted, 1KHz 0dBFS, input signal		105		dB
Total Harmonic Distortion + Noise	A-Weighted ,1KHz -6dBFS, input signal		-86		dB
Gain Error			0.008		dB
Group Delay	20 samples		2.65		ms
Phase deviation			0.18		degree
Channel Separation			-106		dB

Table 7. Audio ADC performance @Line-in channel，44.1KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				16	bits
Full Scale input Signal Level	AVDD=3.3V		0.85		Vrms
Sampling frequency		8		48	KHz
PGA Gain Range		-18		12	dB
Input Resistance	PGA gain=0dB		36		KΩ
Dynamic Range	No Filter 1KHz input signal		94		dB
	A-Weighted 1KHz input signal		96		dB
Signal to Noise Ratio	No Filter, 850mVrms 1KHz input signal		94		dB
	A-Weighted, 850mVrms 1KHz input signal		96		dB
Total Harmonic Distortion + Noise	700mVrms 1KHz input signal		-86		dB
Gain Error			0.033		dB
Group Delay	20 samples		850		us

Channel Separation			-100		dB

Table 8. Audio ADC performance @microphone channel, 44.1KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				16	bits
Full Scale input Signal Level	AVDD=3.3V		0.85		Vrms
Sampling frequency		8		48	KHz
PGA Gain Range	Without GainBoost	-20		20	dB
	With GainBoost	-20		47	dB
Input Resistance	PGA gain=20dB with Gainboost		1.5		KΩ
Dynamic Range	No Filter		94		dB
	A-Weighted		96		dB
Signal to Noise Ratio	No Filter		94		dB
	A-Weighted		96		dB
Total Harmonic Distortion + Noise	PGA Gain=0, -2dBFS Without GainBoost		-80		dB
	PGA Gain=0, -2dBFS With GainBoost		-86		dB
Gain Error			0.03		dB
Group Delay			850		us
Channel Separation			-97		dB

6. Operational Frequency and Power Consumption

6.1 Clock source and Operational frequency

T.B.D

6.2 Power Consumption under Typical Mode

Table 9. Power consumption

Typical Mode	Typical Current	Condition
Bluetooth A2DP	T.B.D.	
Bluetooth HFP	T.B.D.	
Bluetooth sniff	T.B.D.	
Powerdown	T.B.D.	

7. Package

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50BSC	
L	0.35	0.50	0.65
L1		1.00BSC	
θ	0	—	8°

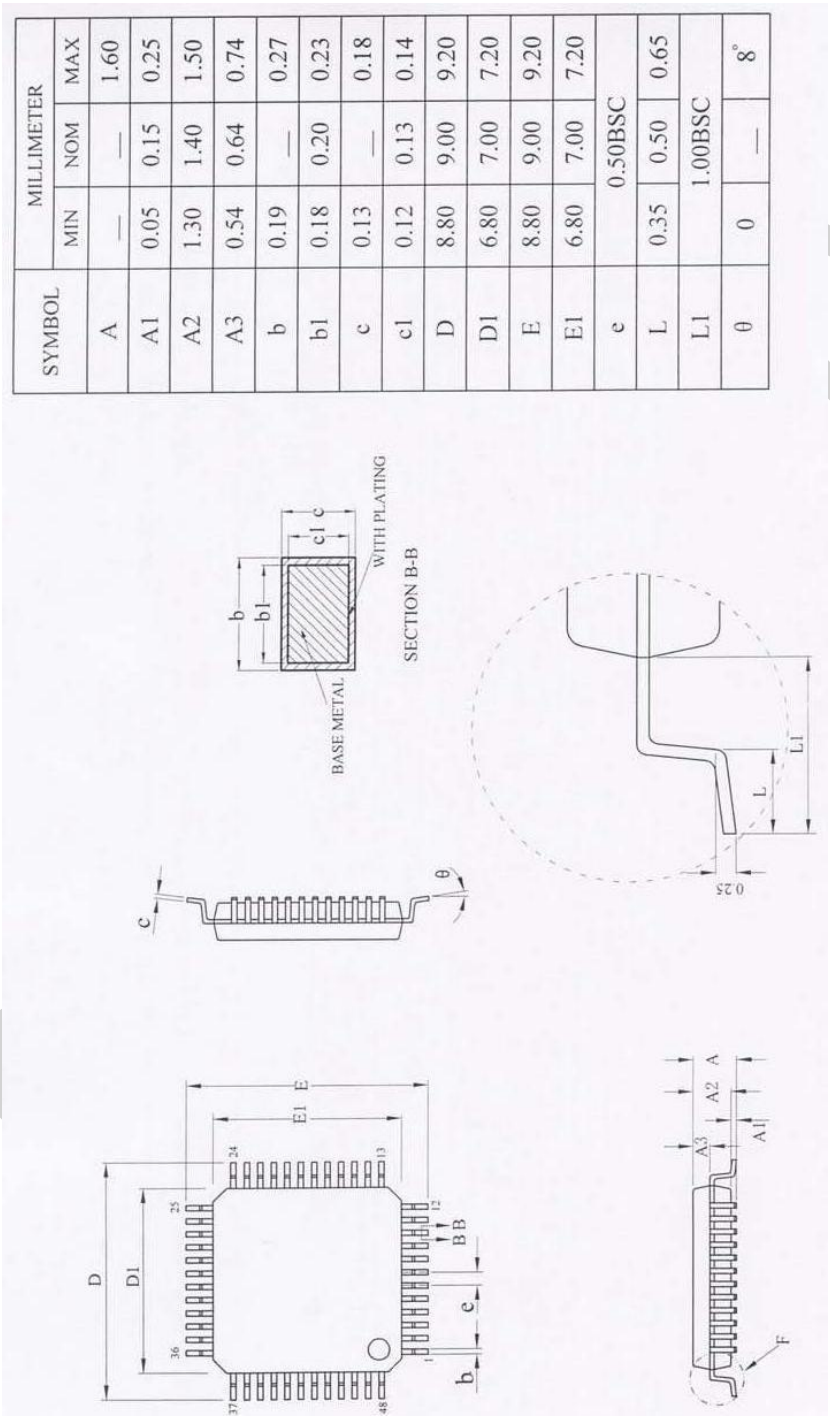

Figure 3. Package and Size

8. Storage and Soldering

Storage temperature: -65℃ ~ 150℃.

BP1048B2 is a moisture sensitive component. The moisture sensitivity classification is **Class 3**.

It' s important that the parts are handled under precaution and a proper manner.

The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <40℃ and <90% relative humidity(RH)
2. Peak Package Body Temperature: 250℃
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
   a. Mounted within 168 hours of factory condition ≤30℃ / 60% RH
   b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
   a. Humidity indicator card is >10% when read at 23±5℃ immediately after moisture barrier bag is opened
   b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40℃) baking requirement in Tape/Reel form.

9. Declaration

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