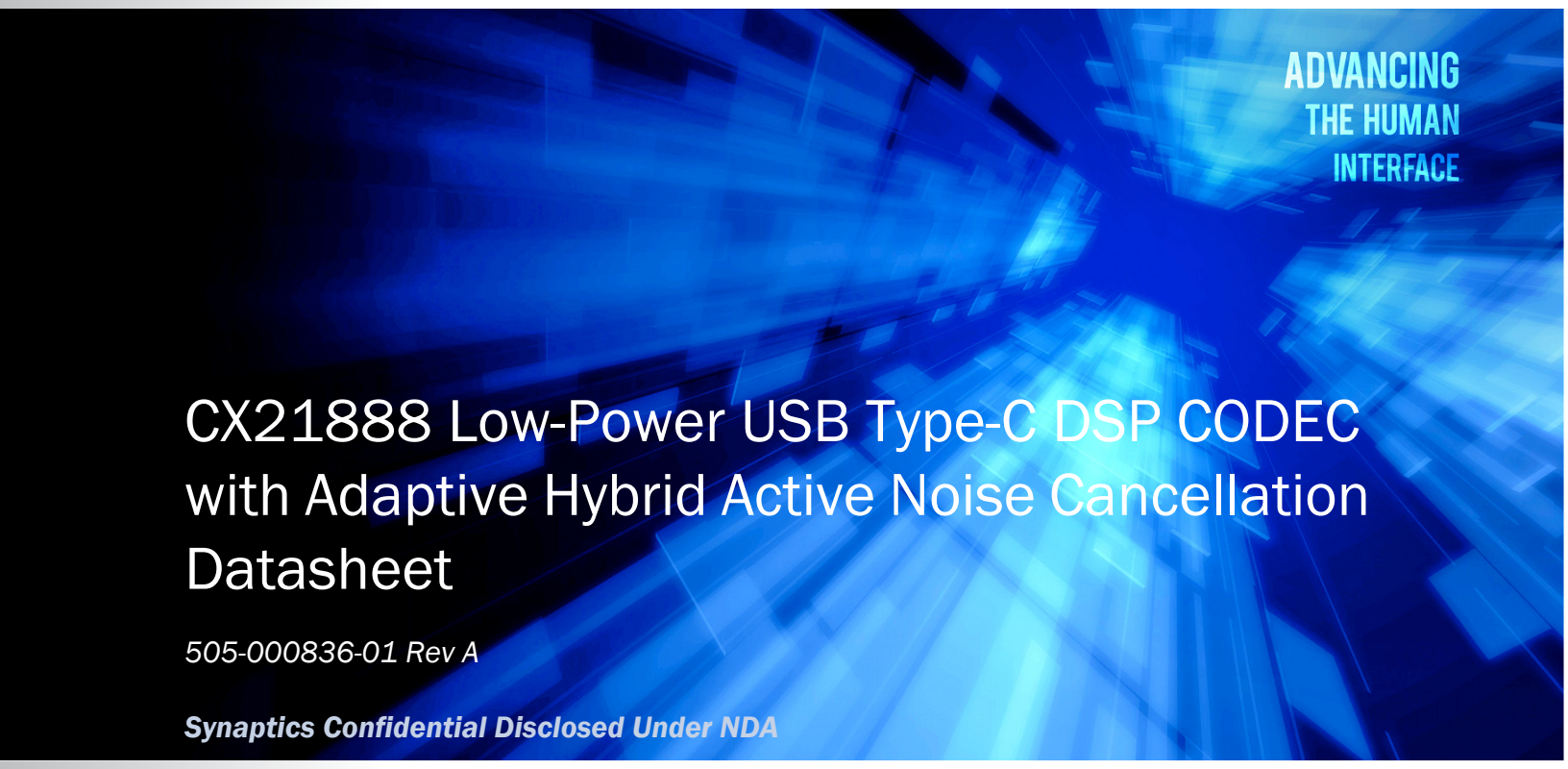
Synaptics®



CX21888 Low-Power USB Type-C DSP CODEC with Adaptive Hybrid Active Noise Cancellation Datasheet

505-000836-01 Rev A

Synaptics Confidential Disclosed Under NDA

Revision History

Document No.	Release Date	Change Description
505-000836-01	01/31/18	**Updated:** • Figure 1, ”CX21888 System Block Diagram,” on page 12 • Figure 22, ”CX21888 Pin Diagram,” on page 45 • Table 6, “Pin Assignments and Signal Definitions,” on page 46 • “Power Consumption” on page 52 • Table 11, “Internal Power Supplies,” on page 57
049-21888DSR00	05/15/17	Initial release

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General Description

The Synaptics® AudioSmart™CX21888 is a single-chip solution for headset applications. Its Active Noise Cancellation (ANC) eliminates up to 45 dB of external sound, for a clearer, more enjoyable listening experience.

The CX21888 combines the benefits of a USB-C codec with the power of DSP. With an onboard 24-bit/96 kHz digital and analog I/O, microphone preamplifiers and a capless headphone amplifier, the CX21888 is a true single-chip solution for applications that demand high audio quality and lower power consumption.

The key features of the CX21888 include:

- Low latency feedforward and feedback paths
- Adaptive hybrid solution (adaptive feedforward with fixed feedback)
- Ambient Inclusion (talk-through) path
- Playback cancellation
- 3D audio processing

The CX21888 integrates a high-performance stereo ADC (98 dBA dynamic range) and DAC (110 dBA dynamic range). Microphone performance is enhanced through programmable preamplifiers paired with a dedicated bias supply to eliminate crosstalk. A ground-referenced output removes the need for capacitors on the headphone output, ensuring consistent performance with a wide variety of transducers. An integrated DC-DC converter supports internal power switches, dynamic voltage scaling, and frequency scaling mechanisms to reduce power consumption. It can also provide power for all peripheral devices connected to the board.

The device has the configuration capability to switch between ANC ON and OFF and Ambient Inclusion ON and OFF modes.

Benefits

- Brings USB Type-C technology to mobile/portable devices that require low power consumption
- Adds extensive DSP capabilities to support Super-Wide-band Noise Reduction (SWB NR), Smart Voice Pickup (SVP) via in-ear microphones, Super-Wideband Acoustic Echo Canceler (SWB AEC) and Wind Noise Canceler for easy and powerful tuning of audio products.
- Improves sound quality by reducing background ambient noise

Features

- ARM Cortex-M0+ controller, up to 50 MHz operation
- Synaptics' dual-core, 32-bit hardware fixed point DSP, up to 100 MHz operation
- Floating point assist
- Up to 504 KB in SRAM
- Wake on Voice (WoV)
- Skype and USB 2.0 compliant full-speed device
- One six-wire I^2S/Pulse Code Modulation (PCM) device
- Two stereo PDM Digital Microphone Interfaces (DMICs)
- Two I^2C masters, or one I^2C master and one I^2C slave
- One SPI connected to an external SPI flash memory with two Chip Selects (CSs).
- One UART

- One watchdog timer
- One tri-color, RGB (PWM) LED drivers
- One stereo ADC (98 dB dynamic range, A-weighted) and one stereo DAC (110 dB dynamic range, A-weighted)
- Standard sampling rates support 8 kHz to 96 kHz
- Three-monitor 10-bit ADCs that support volume control, temperature sensor, and battery monitor.
- Low-latency Active Noise Cancellation (ANC)
- ANC up to 45 dB noise cancellation
- ANC effective at frequencies of up to 8 kHz
- Single wide range input power supply (2.70V–5.25V)
- Temperature range of –40°C to 85°C
- 90L BGA (6.0 mm x 5.5 mm) package

Introduction

The CX21888 device combines the exceptional low-power, energy-efficient and easy-to-use ARM Cortex-M0+ 32-bit MCU with Synaptics' award-winning high-performance dual-core, 32-bit hardware DSP. The CX21888 sets a new standard for flexibility, ease-of-use, performance, and energy efficiency.

The CX21888 is designed with high-quality audio. It incorporates integrated stereo 24-bit/96 kHz ADC and DAC, with 98 dBA and 110 dBA dynamic range, respectively. The true-ground headphone driver requires no output capacitors, so it delivers reliable performance with a wide variety of headphone drivers.

The device is an ideal SoC solution for many different applications, such as advanced USB Type-C headsets, wireless headsets, ultra-low power embedded audio processing units, and voice trigger applications. It supports up to six microphones for beam forming, voice pick up and other voice applications.

Conexant Audio Framework (CAF) Tuning Tool

Various configurations of the CX21888 device can be supported using Conexant Audio Framework (CAF) tuning tool. The CAF V2.2.0.0 supports the following features:

- Microphone boost
- Acoustic Echo Canceler (AEC)
- Capture Dynamic Range Compression (DRC)
- Playback DRC
- Capture Equalizer (EQ)
- Playback EQ
- Capture Noise Reduction (NR)

Additional information can be found in the Conexant Audio Framework Tuning Tool User Guide (see document # 002UGR00).

System Block Diagram

Figure 1 shows the CX21888 system block diagram.

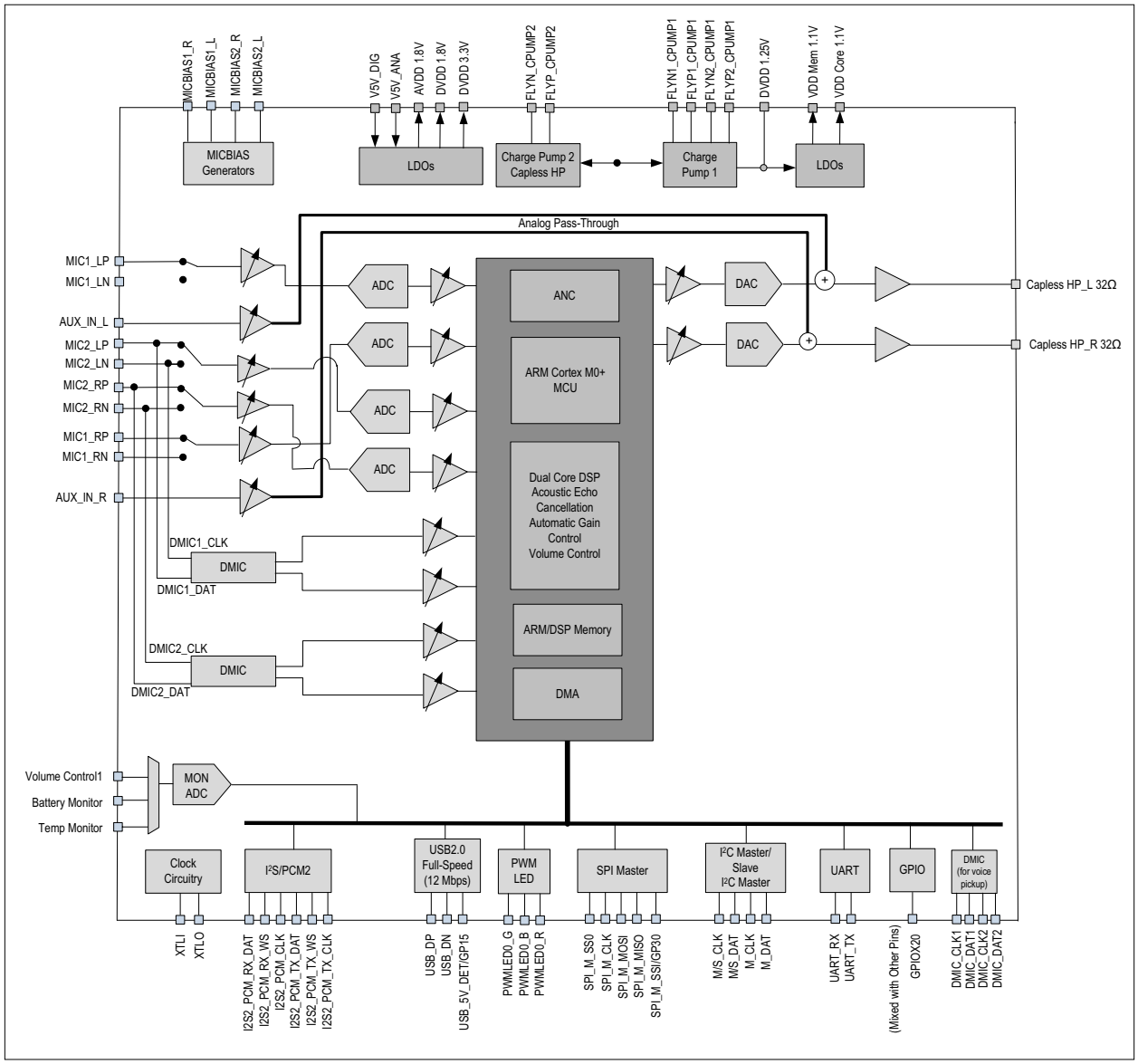


Figure 1: CX21888 System Block Diagram

DSP algorithms enhance the performance of any audio device that incorporates the CX21888. These functions include acoustic echo canceling, noise suppression, equalization, microphone automatic gain control, and volume control. In addition, Synaptics' SVP algorithm optimizes microphone performance by suppressing as much as 45 dB of ambient noise and improving signal-to-noise ratio (SNR) by as much as 19 dB.

The CX21888 has integrated an ARM Cortex M0+ based MCU with Synaptics' dual-core fixed point DSP with floating point assist to achieve an optimized architecture and peripheral set. The ARM Cortex M0+ based, low-power 32-bit MCU operates at CPU frequencies of up to 50 MHz. Each DSP core can run up at to 100 MHz, for a total of 2x100 MHz.

The CX21888 supports up to 504 KB of SRAM that can be shared between the ARM Cortex M0+ MCU and the DSP. The peripheral complement of the CX21888 includes one I^2C-bus master and one slave interface (or two I^2C masters), up to two I^2S interfaces, one SPI, two multi-rate timers, a self wake-up timer, four monitor ADCs, two PDM DMICs, an S/PDIF input and output, and up to 20 GPIO pins.

Each programmable microphone preamplifier is paired with a dedicated bias supply to eliminate crosstalk, which maximizes the speech-to-noise ratio with low boost and prevents microphone saturation. An integrated DC-DC converter, supporting internal power switches, Dynamic Voltage Scaling (DVS), and frequency scaling mechanisms to reduce power consumption for low-power applications. This converter can also provide power supplies for all peripheral devices connected on the board.

CX21888 Audio CODEC Features

- ARM Cortex-M0+ controller, up to 50 MHz operation
- Synaptics' dual-core, 32-bit hardware fixed point DSP, with each running up to 100 MHz operation
- Floating point assist
- Up to 504 KB in SRAM
- Skype and USB 2.0 compliant full-speed device
- One six-wire I^2S/PCM device
- S/PDIF input
- Two stereo PDM DMICs
- Two I^2C masters, or one I^2C master and one I^2C slave
- One SPI connected to an external SPI flash memory with two CSs
- One UART
- One watchdog timer
- One tri-color (RGB) PWM LED drivers
- One stereo ADC (98 dB dynamic range, A-weighted) and one stereo DAC (110 dB dynamic range, A-weighted)
- Standard sampling rates support 8 kHz to 96 kHz

Functional Applications

- USB Type-C headset with ANC
- Wireless headset with ANC
- Voice trigger
- Smart voice processing

Device Description

The Synaptics AudioSmart™ CX21888 is a single-chip solution for applications such as headsets, with extended capabilities for docking stations and voice command products.

The CX21888 combines the benefits of a USB-C codec with the power of DSP. With an onboard 24-bit/96 kHz digital and analog I/O, microphone preamplifiers and a capless headphone amplifier, the CX21888 is a true single-chip solution for applications that demand high audio quality and lower power consumption.

Whether connected via USB, analog or wireless, the CX21888's DSP provides the power needed to maximize the features and performance of headsets and other audio products, including acoustic echo canceling, noise reduction, equalization, microphone automatic gain control (AGC), and volume control. In addition, Synaptics' Smart Voice Pickup (SVP) algorithm greatly improves ambient noise rejection for microphones.

ARM Cortex M0+ Microcontroller

The device core uses an energy-efficient ARM® Cortex® M0+ 32-bit microcontroller unit (MCU) that controls the Synaptics dual-core, fixed-point 32-bit DSP with floating-point assist. The DSP engine operates at up to 100 MHZ, for a total of 400 MIPS. The device supports up to 504 KB of SRAM, which can be shared between the ARM Cortex MCU and the DSP.

ARM's Most Energy-Efficient Cortex-M Class Processor

The ARM Cortex M0+ processor is a high-performance and energy-efficient ARM processor.

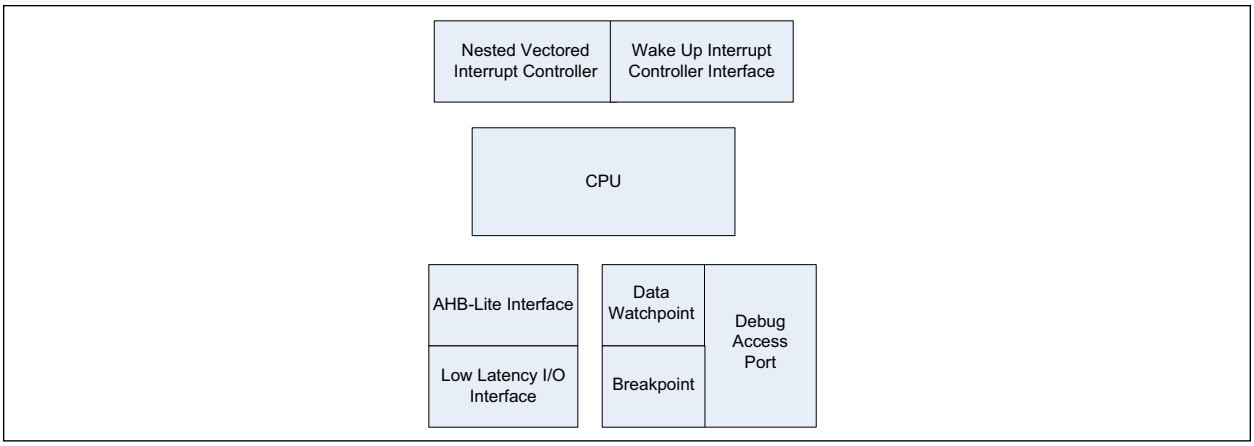


Figure 2: ARM Cortex Core Architecture

Simplicity

The Cortex M0+ processor keeps the same 56 instructions of the Cortex-M0 processor, enabling simple and quick development. The Thumb® instruction set offers an unrivaled code-density while providing access to 32-bit computation performance.

- Processor power consumption as low as 9 μA/MHz
- Outstanding result of 1.77 CoreMark/MHz

Specifications

- The ARMv6-M Thumb instruction set
- Thumb-2 technology
  - An ARMv6-M compliant 23-bit SysTick timer
- Fast single-cycle 32-bit hardware multiplier.
- Support for either little-endian or byte invariant big-endian data accesses.
- The ability to have deterministic, fixed-latency, interrupt handling.
- Load/store multiple and multicycle multiply instructions that can be abandoned and restarted to facilitate rapid interrupt handling.
  - Unpriviledged/Priviledged support for improved system integrity
- C-Application Binary Interface compliant exception model
- Uses the ARMv6-M, C-Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-model entry using Wait For Interrupt (WFI). Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature.

NVIC Features

- 27 interrupt inputs, each with four levels or priority.
- Dedicated Non-Maskable Interrupt (NMI) input
- Support for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.

Analog Outputs

The DAC data path contains interpolation, filtering and delta sigma modulation functions including gain/attenuation stages, PC beep mixing function, a De-POP circuit, and signal ramping and a mixer function.

It also implements an envelope detection function that is used to adjust the headphone amplifier power supply charge pump, such that it produces a high operating voltage (+/- 1.7V) when required by a high output signal level, and a lower operating voltage (+/- 0.9V) when the output signal level is below approximately -8 dBFS.

Digital-to-Analog Converter (DAC)

- Stereo
- 16-bit/24-bit data path
- Sampling rates = 8 kHz, 16 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Digital PGA on ADC output = –69 dB to 0dB in 0.5 dB steps
- Five bi-quad filters EQ on DAC outputs = Each DAC supports a five-band EQ. The implementation consists of five, second-order Infinite Impulse Responses (IIRs) in series within each channel. The filter coefficients are programmable. For the DRC, Synaptics sends the absolute maximum value of the EQ's output. The firmware runs the algorithm, and then sets the GAIN stage of the DRC.

Headphone Output

- Headphone/line driver = capless, stereo
- Line-out (10 kΩ) 1VRMS or headphone (32Ω) 31 mW
- Frequency range = 20 Hz to 20 kHz
- THD+N at –3 dBFS = –85 dB at 32Ω load
- Dynamic range = 110 dBFS A-wt
- Magnitude response = ±0.25 dB ripple, 0.5 dB p-p
- Crosstalk = –92 dB maximum
- The headphone outputs have the following configuration options:
  - Power on/off
  - Mute on/off
  - Maximum output limiting to comply with GS Mark

Line Output

- Line-out (10 kΩ) 1VRMS
- Frequency range = 20 Hz to 20 kHz
- Dynamic range = 110 dB at 10 kΩ load
- THD+N = –83 dB at 10 kΩ load

Analog Inputs

The ADC path contains filtering and decimation functions including gain/attenuation stages and DC filtering functions. It also includes a dedicated mixer path to process data from the DAC path.

Analog-to-Digital Converter

- Stereo
- 16-bit/24-bit data path
- Sampling rates = 8 kHz, 16 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Digital PGA on ADC output = –69 dB to 24 dB in 0.5 dB steps

Line Input

Auxiliary = Stereo, multiplexer with stereo microphone

- Auto-disable of micbias
- Boost = –6 dB to 0 dB in 6 dB steps
- Noiseless power-up/down
- THD+N at –3 dBFS = –85 dB
- Dynamic range = 95 dBFS A-wt
- Magnitude response = ±0.25 dB ripple, 0.5 dB p-p
- FS = $1V_{RMS}$

Microphone Input

- Microphone = Stereo, multiplexer with stereo auxiliary
- Boost = 0 dB to 30 dB in 6 dB steps
- Noiseless power-up/down
- Dynamic range = 95 dBFS A-wt
- THD+N at –3 dBFS = –85 dB
- Magnitude response = ±0.25 dB ripple, 0.5 dB p-p
- 12-band EQ filter on the input path

Microphone Bias (Micbias) Generator

The micbias generator provides current bias to a microphone that is AC-coupled to a multi-function input port. The current bias is achieved by driving a fixed-voltage input series resistor. The pad for the micbias uses a special Electro-Static Discharge (ESD) structure that allows a negative swing under normal operation, yet still clamps negative ESD spikes.

The micbias is only needed for singled-ended microphones, and is not necessary for differential microphone applications. The micbias operational amplifier can sense a high-current condition, which is useful to sense headset button pushes. When the headset button is pushed, the microphone line is grounded using a very small resistance (several ohms). This information can be used to signal the OS/driver that a button press occurred, and the OS/driver can take action. The micbias logic is capable of supplying an output current of more than 2 mA. The micbias voltage can be configured from 1.6V to 3.1V.

Monitor ADC

The 10-bit monitor ADC monitors the volume controls and various other inputs such as temperature and battery voltages. The monitor ADC is designed for conversion speeds up to 15 ksps and can support up to four single inputs. Input channel 2 is specially designed to support battery voltages of up to 5.5V. The monitor ADC is accurate to 15 mV.

Table 1: Monitor ADC

Parameter		Minimum	Typical	Maximum	Unit
ADC Input Range	Input 1, and 3	–	–	3.6	V
	Input 2	–	–	5.5	V

Figure 3 shows the monitor ADC functional block diagram.

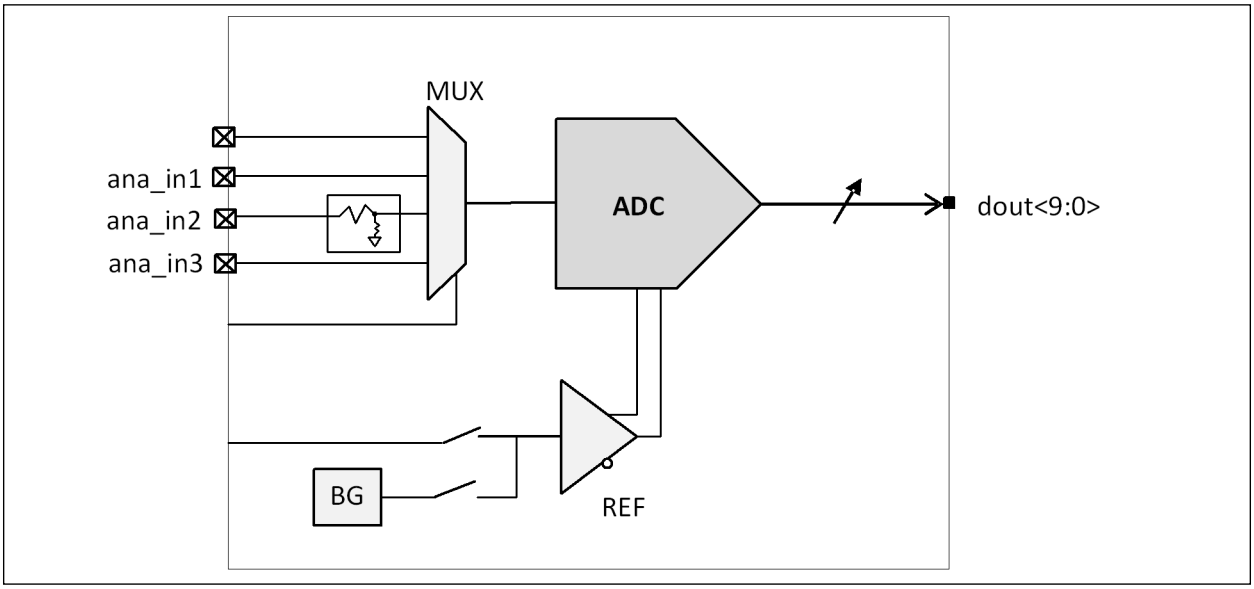


Figure 3: Monitor ADC Functional Block Diagram

The monitor ADC uses a successive approximation method, with an analog DAC and comparator, controlled by state machines. The digital logic is, in turn, controlled by firmware, through a register interface.

With four inputs, the monitor ADC provides the ability to monitor up to three external voltages. The ADC output is a 10-bit value for each channel, with 0x000 representing the minimum input voltage, and 0x3FF representing the maximum input voltage.

Active Noise Cancellation

Noise and electronic interference is disruptive and distracting. It can impede an important phone call, enjoyment of music or media on headphones, or the healthy objective of experiencing peaceful solitude.

Active Noise Cancellation (ANC) is a noise reduction technique in which an anti-noise (equal in magnitude but opposite in phase) is generated through loudspeakers and directed towards the location where noise cancellation is required. Noise and anti-noise signals cancel each other acoustically, such as over the air.

The ANC process enables superior noise reduction as compared to passive methods, both in terms of comfort and performance.

The CX21888 supports hybrid ANC as shown in Figure 4.

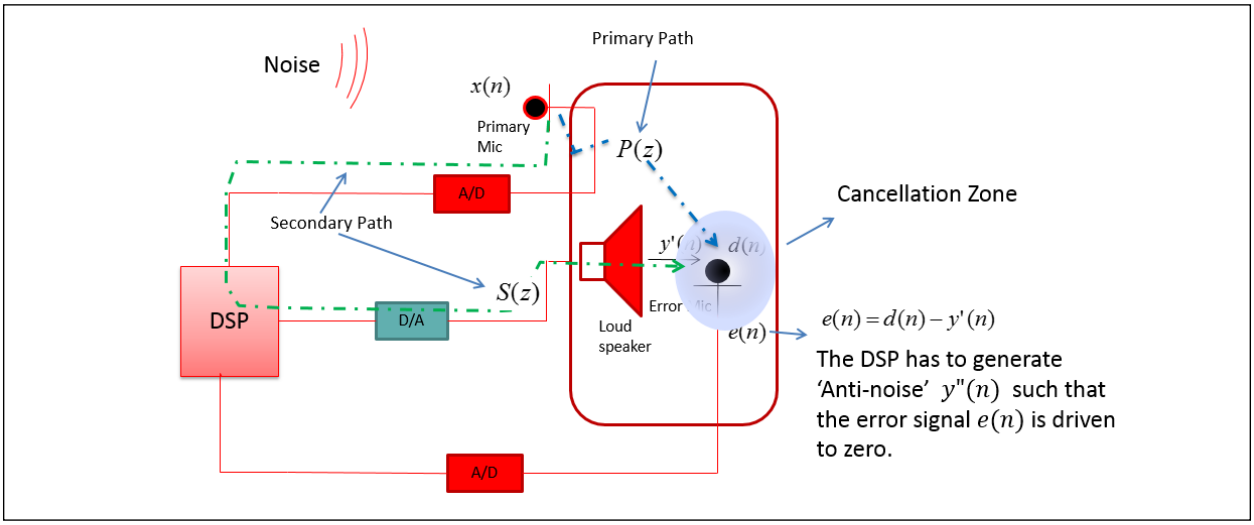


Figure 4: Hybrid Active Noise Cancellation

In a feedforward setup, one microphone is placed outside the ear cup. The microphone hears the noise before the person does. ANC then processes the noise and creates the anti-noise before sending the resulting signal to the headset speaker.

In a feedback ANC, one microphone is placed inside the ear cup and it hears the resulting signal in the same way as the listener.

In a hybrid setup, a microphone is positioned externally and inside the ear cup.

Digital Audio

The Universal Serial Bus (USB) function controller in the CX21888 is a USB 2.0-compliant full-speed device with integrated transceiver and on-chip matching and pull-up resistors. It enumerates to the host as a standard USB Audio Device and HID Consumer Control supporting:

- USB Digital Audio Out (Audio Playback Device)
- USB Digital Audio In (Microphone/Recording Device)
- HID Consumer Control handling standard volume and mute functionality

Pulse Code Modulation (PCM)/I^{2}S Interface

The CX21888 supports the following modes and configurations on the I^{2}S/PCM bus:

- Bit width = 8, 16, and 24 for I^{2}S/PCM
- Most Significant Bit (MSB) first for the I^{2}S/PCM
- Left (L) or Right (R) justified data format for the I^{2}S
- Maximum external clock rate = 12.288 MHz
- I^{2}S Data driven on falling edge of clock, sampled on rising edge
- Master/slave mode for the I^{2}S/PCM
- PCM interface supports up to 32 slots, with up to three slots of input and up to three slots of output.

The CX21888 supports independent six-wire Tx and Rx interfaces. Each interface can be set for master or slave mode.

Both interfaces support audio sample rates from 8 kHz up to 192 kHz for both record and playback. The supported sample widths are 8-bit, 16-bit, and 24-bit. In addition, the PCM supports a four-channel Tx/Rx for the PCM mode, while the I^{2}S only supports two channels.

The CX21888 supports standard I^{2}S mode, left-justified mode, and right-justified mode. The CX21888 also supports three PCM modes of operation:

- Short frame mode
- Long frame mode
- Multi-slot mode

The default interface mode is I^{2}S, which is configurable to PCM mode through the control register.

Sony/Philips Digital Interface Format (S/PDIF)

The CX21888 supports the industry standard IEC 60958 digital audio interface, also known as *S/PDIF*. The S/PDIF is a serial, uni-directional, self-clocking interface for the interconnection of digital audio equipment.

The S/PDIF provides a digital audio interface for the receiving and playback of audio. Audio data is coded in PCM format with a resolution of 16-bits or 24-bits per sample. The S/PDIF supports sample rates from 44.1kHz up to 192kHz.

Digital Microphone Interface (DMIC) for Voice Pickup

The DMIC module provides the necessary clock and data I/O to interface with up to two digital microphone devices, as well as the required decimation filter chain to convert the microphone PDM outputs to a PCM representation. The module additionally provides a DC blocking filter and gain control. The DMIC provides a microphone clock output. Various microphone clock frequencies are supported, from 300kHz to 4MHz.

> ***Note:*** The capabilities of each microphone should be ascertained before establishing the interface clock frequency.

The DMIC supports stereo microphones, with the left and right channels being sampled on opposite clock edges. By default, the left channel is sampled on the falling clock edge, while the right channel is sampled on the rising clock edge.

Universal Serial Bus (USB) Interface

The CX21888 supports USB 2.0 Full Speed (FS) at 12 Mbps. The device is compliant with both the *USB Audio Device Class Definition Specification* and the *Microsoft United Communication Peripheral Device Specification*, Revision 1.0, Section 8.1. The CX21888 also addresses the following USB End Points (EPs):

- 0 = IN-Status, OUT-Control
- 1 = IN-ADC, OUT-DAC
- 2 = OUT-DAC
- 4 = IN-HID

The CX21888 employs Phase-Locked Loop (PLL)/Sample Rate Conversion (SRC) solutions for clock synchronization using the USB suspend mode current of 1.8 mA. This is lower than the requirement defined in the USB specification of 2.5 mA. The device USB port is clocked using a 24 MHz crystal clock source and can be resumed/suspended using the keypad buttons.

I²S Mode Timing

The I²S timing uses WS (LRCK) to define whether the data is being transmitted for the left channel or for right channel. The WS is low for the left channel and high for the right channel. A WS polarity control bit is provided to allow either high or low to represent the left channel. The default setting of the polarity control is 0, which means low WS = left channel. The WS need not be symmetrical. A system clock (BCLK) running at a minimum of 2 x (sample width +1) x sample frequency is used to clock in the data. There is a delay of 1 clock bit from the time the WS signal changes state to the first data bit on the data line. The data is written MSB first and is valid on the rising edge of the bit clock. When the programmed sample width is taken, any remaining bits are ignored.

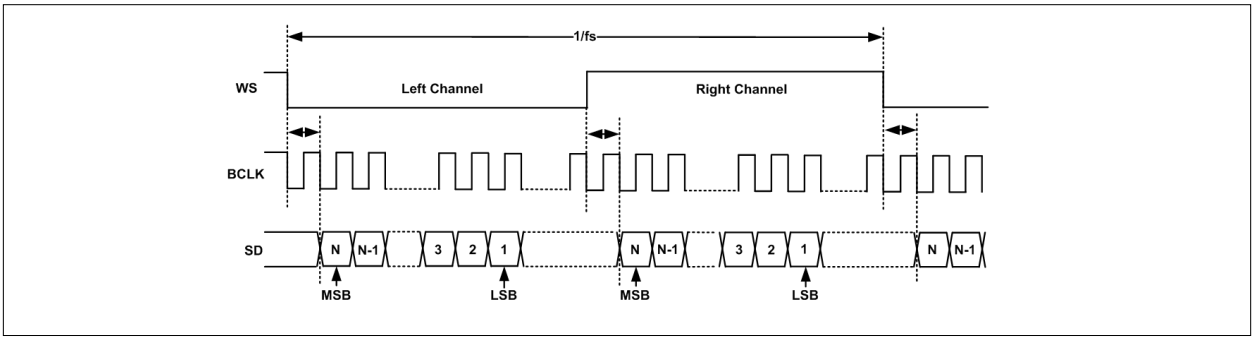


Figure 5: I²S Timing Diagram—Width of LRCK Frame is Wider than 2N Bits (N=8, 16, or 24)

One case to be careful with is I²S, when the number of bits in the sample word matches the number of clocks per frame. Because a true I²S requires a one clock shift of the data, the LSB of each word arrives after the WS signal changes state, as illustrated in Figure 6. To handle this correctly, the internal channel indicator should only change state after the bit count is reached and the state of WS does not match the expected value for the current channel.

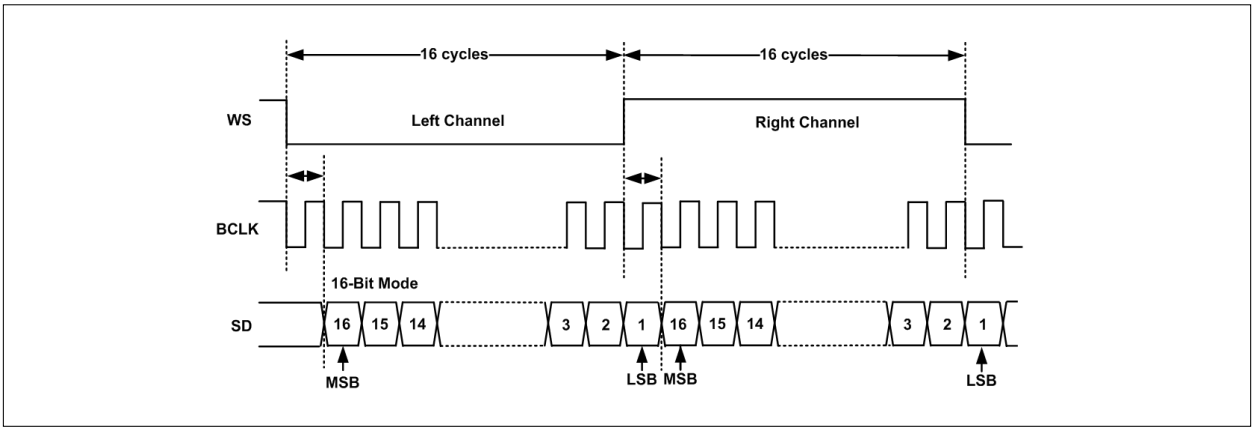


Figure 6: I²S Timing Diagram—16-Bit per Channel I²S

Left-Justified Mode

Left-justified timing uses the WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. The WS is high for the left channel and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. The first data bit appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of bit clock. When the programmed sample width is taken, any remaining bits are ignored. If the WS toggles before the full word length is read, the remaining bits are zeroed.

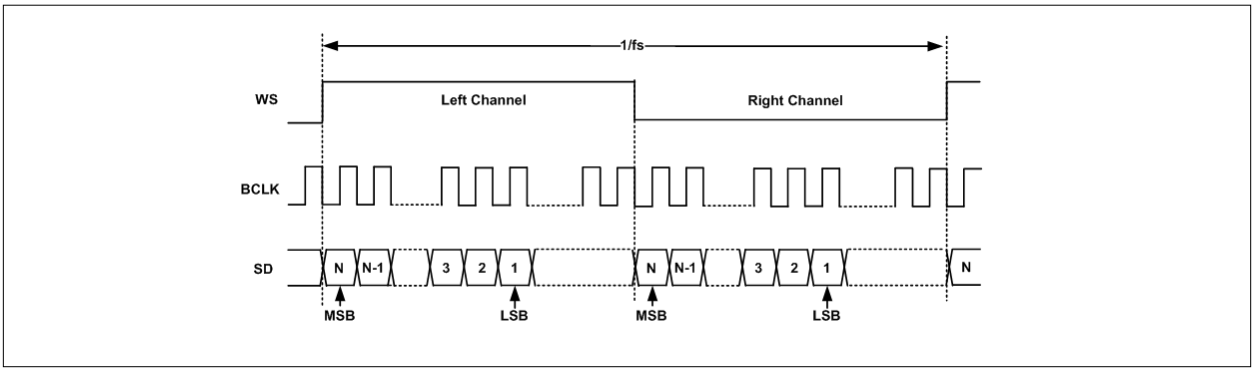


Figure 7: Left-Justified Timing Diagram

Right-Justified Mode

Right-justified timing uses the WS clock to define whether the data is being transmitted for the left channel or for right channel. The WS is high for the left channel and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. Data is captured in a 24-bit shift register until the WS toggles. When the WS toggles, the last 24, 16, or 8 bits are transferred to the channel indicated by the previous state of WS. In right-justified mode, the LSB of data is always clocked by the last bit clock before the WS transitions. The data is written MSB first and is valid on the rising edge of bit clock. All leading bits are ignored.

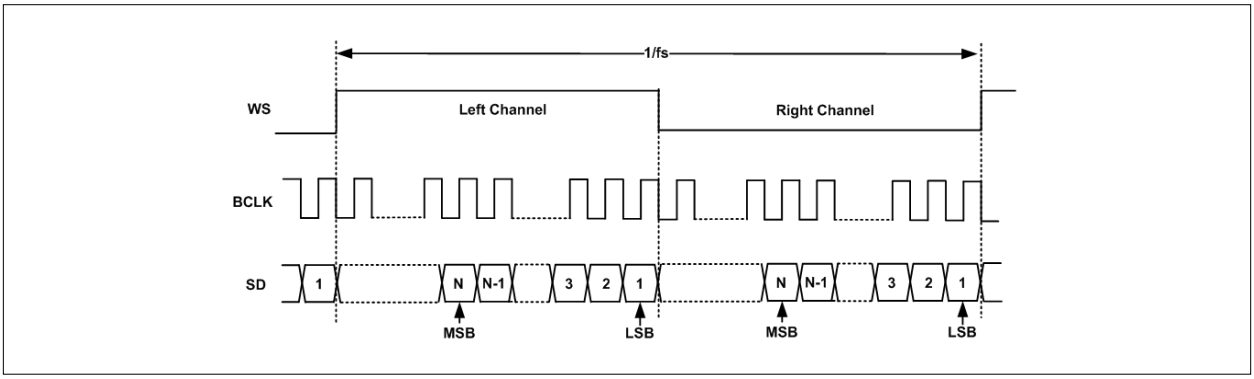


Figure 8: Right-Justified Timing Diagram

PCM Short Frame Mode

In short frame mode, the falling edge of PCM_SYNC indicates the start of the PCM word. The PCM_SYNC is one clock long. Data is driven out on the rising edge of PCM_CLK after the PCM_SYNC pulse.

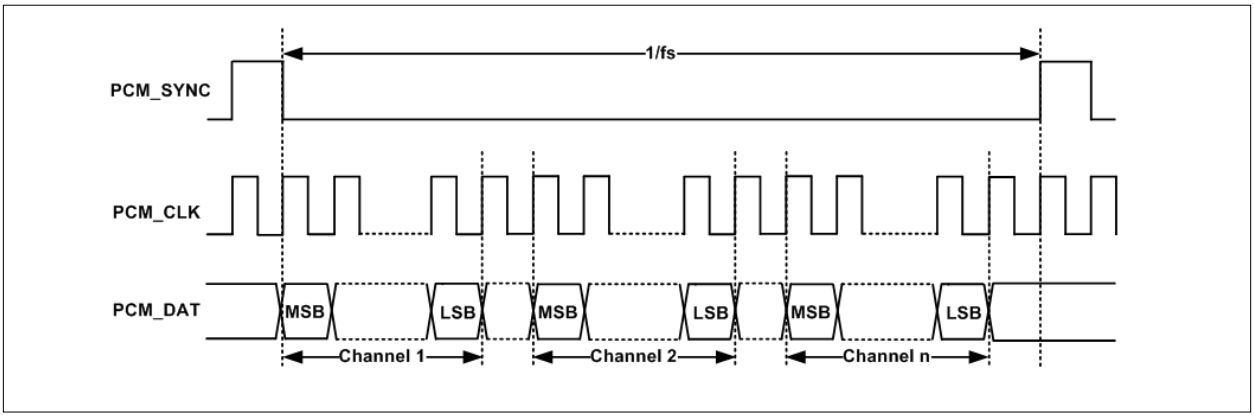


Figure 9: PCM Short Frame Timing Diagram

PCM Long Frame Mode

In long frame mode, the rising edge of PCM_SYNC indicates the start of the PCM word. The PCM_SYNC is at least two clocks long. Data is driven out on the rising edge of PCM_CLK coincident with the rising edge of PCM_SYNC.

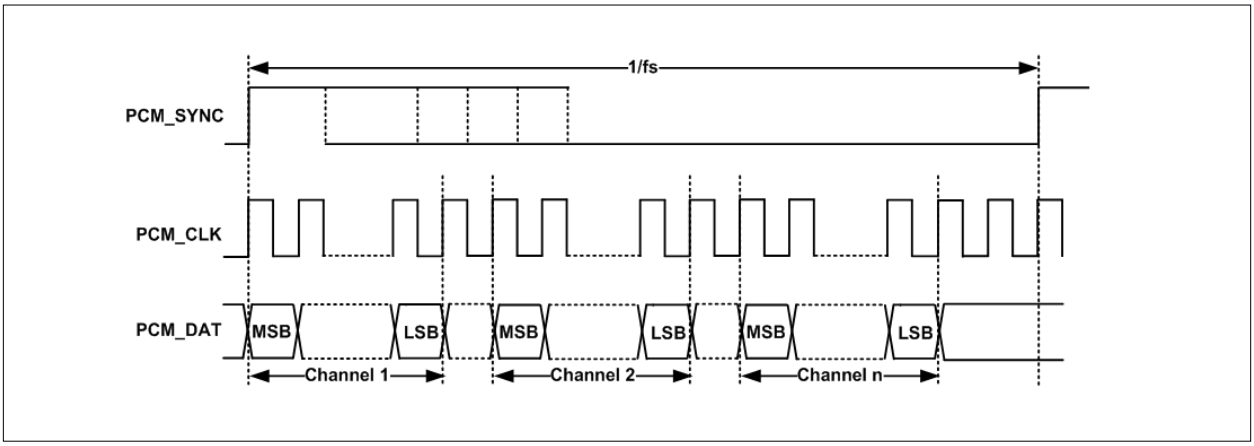


Figure 10: PCM Long Frame Mode Timing Diagram

PCM Multi-Slot Mode

In multi-slot mode, PCM_SYNC can be either long or short. Four words of data can be sent or received. The position of the start of the PCM word is determined by the length of the sync pulse. Slots are determined by counting data width clocks (8, 16, or 24) from the first PCM word.

The CX21888 PCM supports up to four channels, but while transmitting, the channel selection should always be from Channel_1.

Control

I²C Slave

The CX21888 supports a single I²C slave interface. The I²C slave is a standard I²C slave with address hexadecimal 0x41. The I²C slave:

- Used for USB/I²C tunneling and external co-processor control
- Supports 100 kHz and 400 kHz

Data Flow Diagram

Complete the following process to write to the CX21888 device.

1. Send a start sequence.
2. Send the I²C address of the slave.
3. Send the register address for the write (24-bit).
4. Send the data bytes (4-byte data).
5. Optional: Send any further data bytes (burst operation).
6. Send the stop sequence.

Complete the following process to read from the CX21888 device.

1. Send a start sequence.
2. Send the I²C address of the slave.
3. Send the register address (24-bit).
4. Send a start sequence again (repeated start).
5. Read the data bytes (4-byte data).
6. Optional: Read any further data bytes in case of a burst read mode.
7. Send the stop sequence.

Transferring Data on the I2C Bus

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, as shown in the following figure.

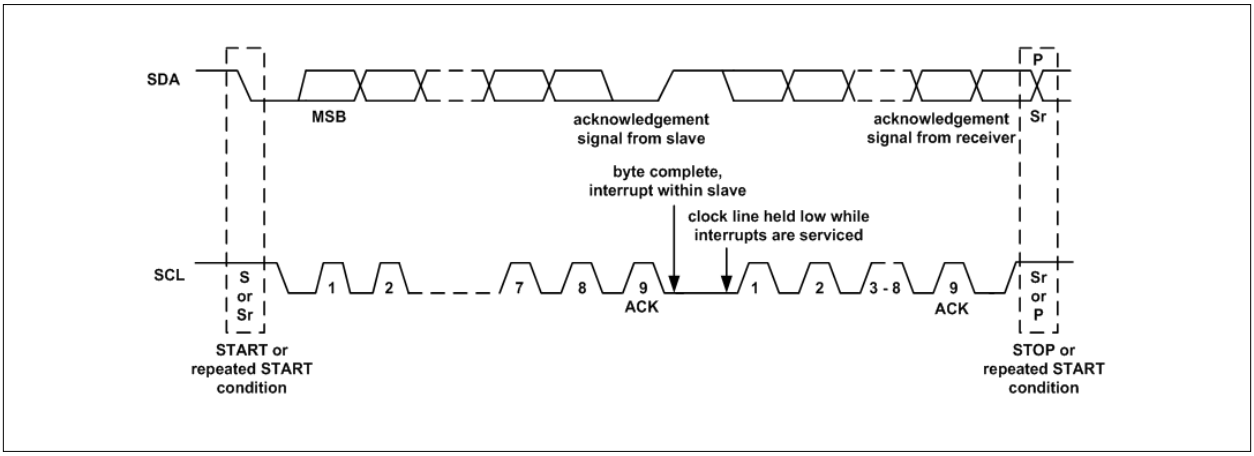


Figure 11: I2C Bus Transactions

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The data transfer format on the I2C bus is shown in the following figure.

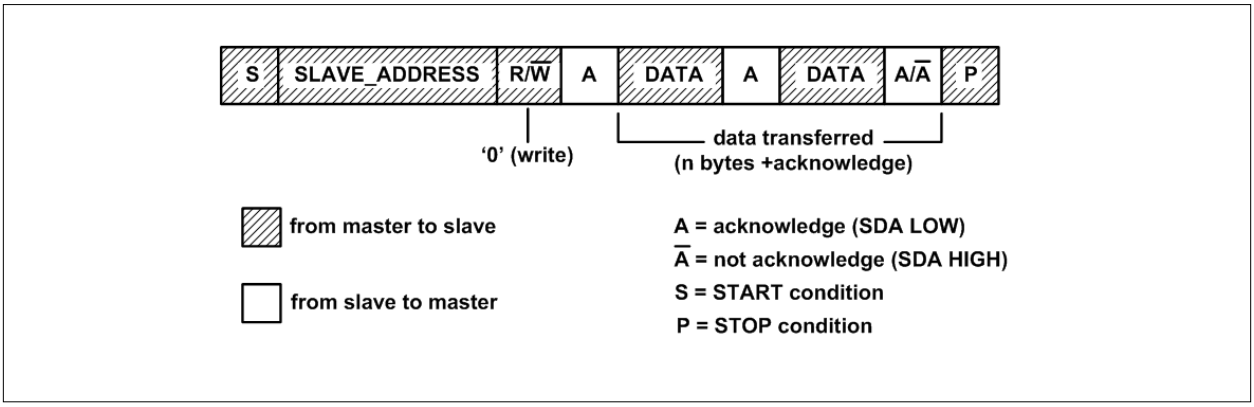


Figure 12: I2C Data Transfer Format

I²C Slave Address Format

The slave addressing format for I²C is shown in the following figure.

Slave Address	R/W Bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

Figure 13: I²C Slave Address Format

I²C Interface Timing for 400 kHz Mode

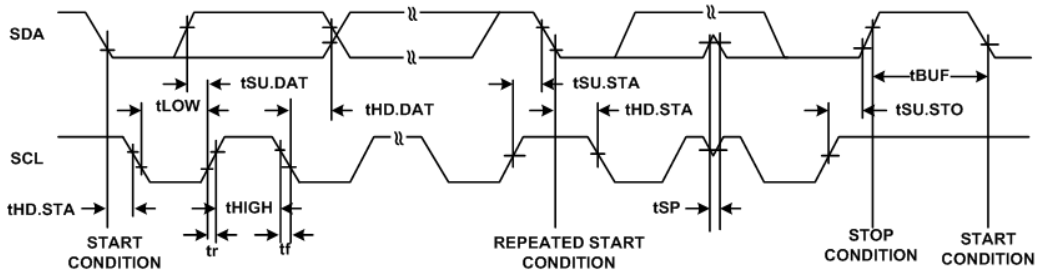


Figure 14: Interface Timing Requirements for 400 kHz Transfer

Table 2: Interface Timing Requirements for 400 kHz Transfer

I2C (400kHz)	Symbol	Minimum	Maximum
Set-up Time Start Condition	$t_{SU.STA}$	0.6µs	-
Hold Time Start Condition	$t_{HD..STA}$	0.6µs	-
SCL Clock LOW Period	t_{LOW}	1.3µs	-
SCL Clock HIGH Period	t_{HIGH}	0.6µs	-
Data Set-up Time	$t_{SU.DAT}$	100ns	-
Data Hold Time	$t_{HD.DAT}$	0	0.9µs
Set-up Time for STOP Condition	$t_{SU.STO}$	0.6µs	-

Serial Peripheral Interface (SPI) Master

The SPI is a SPI master interface that is intended to interface with SPI slave devices, such as a serial flash. The SPI block consists of a Tx and Rx First In, First Out (FIFO) that is 8x32 bits with several registers for control and status. The SPI accommodates various controls for clock polarity, a phase shift of the clock, and slave select polarity.

The SPI clock is derived from the PLL_SPI_CLK and can be programmed by a field in the control register. Two slave selection signals are available to allow use of two different SPI peripherals (SS0, SS1).

Table 3: ***SPI Interface Signals***

Signal Name	I/O	Default	Function
SPI_CLK	O	NA	Maximum of 50MHz.
SPI_MI	I	NA	Serial master in.
SPI_MO	O	NA	Master serial data out.
SPI_SS0	O	NA	CS 0.
SPI_SS1	O	NA	CS 1.

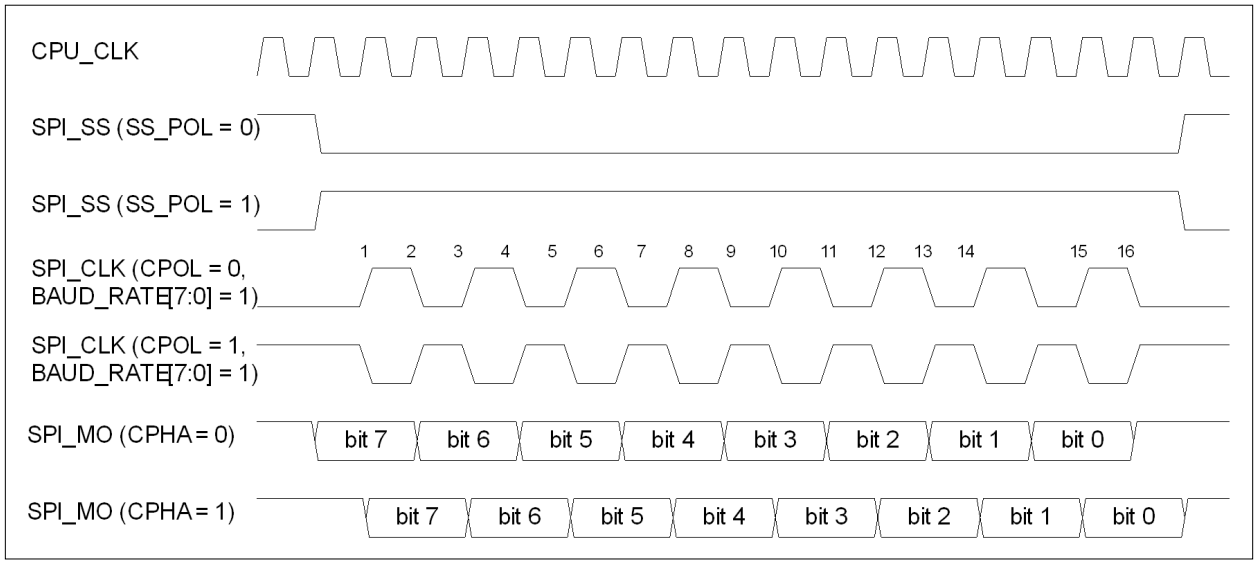


Figure 15: SPI Tx Timing

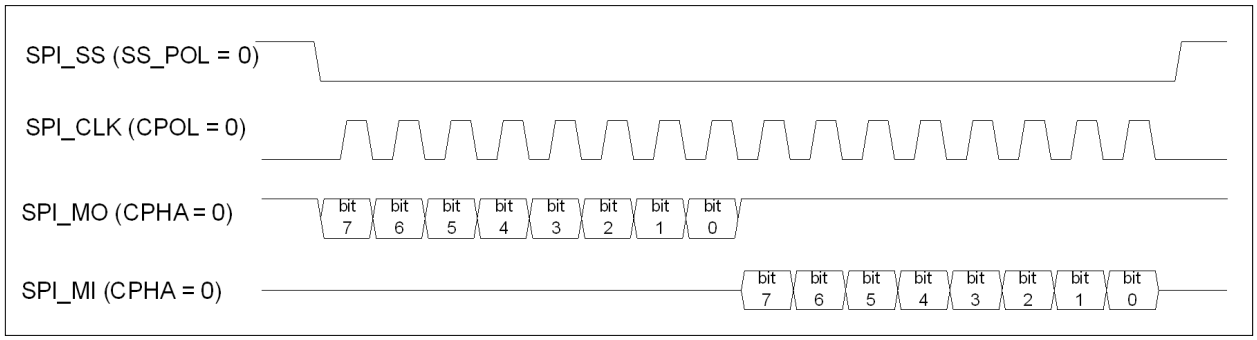


Figure 16: SPI Tx and Rx Timing

UART

The internal UART with Flow Control (FC UART) is compatible with a standard 16550 UART. The added features of the FC UART over the 16,550 UART is the higher clock frequency and a FC mechanism. A data rate of up to 3 Mbps can be supported on the UART interface. The UART operates at 115,200 bps, no parity bit, 8 data bits, and 1 stop bit. Only the UART Tx/Rx signals are needed to download new firmware images to the SPI flash device through the CX21888. The RTS/CTS functions are not needed for firmware downloads.

- Standard baud rate = 115,200
- Used for a debug interface or Micro-Controller Unit (MCU) interface
- Shared with GPIO pins:
  - Pin 8 = GP9/UART_RX
  - Pin 59 = GP10/UART_TX

Tri-Color LED Pulse-Width Modulation (PWM) Driver

The following figure provides a block diagram of the tri-color LED PWM driver.

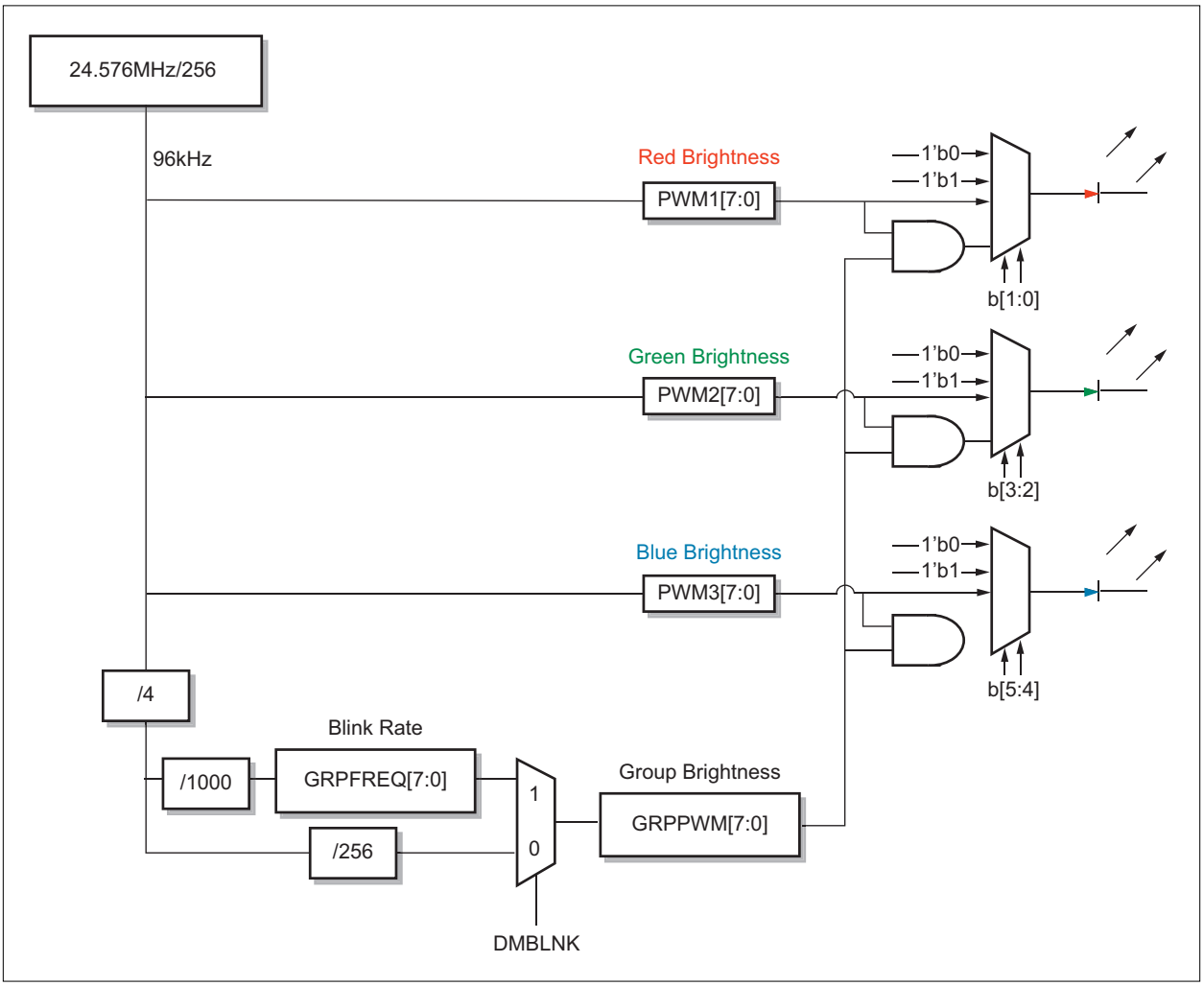


Figure 17: Tri-Color LED PWM Driver

The CX21888 supports two 3-bit LED drivers that are optimized for RGB color mixing applications:

- Each LED output has its own 8-bit resolution (256 steps) with a fixed frequency. An individual PWM controller operates at 96kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value.
- A fourth 8-bit resolution (256 steps) group PWM controller uses187Hz with a duty cycle that is adjustable from 0% to 99.6% to allows the LED group to be set to set from fully off to maximum brightness (default).
- An 8-bit resolution (256 steps) adjustable frequency between 24Hz to once every 10.66 seconds has a duty cycle that is adjustable from 0% to 99.6% to blink all LEDs.
- The PWM LED drivers can sink to GND or source to 3.3V, 13mA for each pin.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value, or at both individual and group PWM controller values.

General Purpose I/O's (GPIOs)

The CX21888 supports the following:

- 20 shared and dedicated Input/Outputs (I/Os)
- Keypad matrix support
- Configured as inputs during reset
- USB remote wake-up
- Each GPIO can sink to GND or source to 3.3V, 6.1mA

Single-and Multi-Function I/Os

While some device I/Os have a single associated function, others have more than one associated function. Selection between the available I/O functions is accomplished through registers located in the AHB Registers Module. Specifically, the IO Function Selection (IO_MUX_A) and IO Function Selection (IO_MUX_B) registers. Table 4 summarizes the various device digital I/O, and lists any alternate functionality provided by each.

*Table 4: **Digital I/O Functions***

HW Function A (Default I/O Function)	HW Function B	HW Function C	HW Function D
GP0	DMIC_CLK2	–	–
GP4	–	–	–
GP5	–	–	–
GP7	–	–	–
GP8	DMIC_DAT1	–	–
GP9	UART_RX	–	–
GP10	UART_TX	–	–
GP11	–	–	–
GP12	–	–	–
GP13	DMIC_DAT2	–	–
GP14	MADC3	–	–

*Table 4: **Digital I/O Functions***

HW Function A (Default I/O Function)	HW Function B	HW Function C	HW Function D
GP15	USB 5V Detect	–	–
GP16	MADC1	–	–
GP18	I2C_S_CLK	I2C1_M_CLK	–
GP19	I2C_S_DAT	I2C1_M_DAT	I2C_S_DAT and I2C1_M_DAT
GP20	I2C2_M_CLK	–	–
GP21	I2C2_M_DAT	–	–
GP22	PWM_LED0_R	–	–
GP23	PWM_LED0_G	–	–
GP24	PWM_LED0_B	–	–
GP30	SPI_M_SS1	I2S2_PCM_TX_CLK	–
GP31	MCLK		
SPI_M_SS0	–	–	–
SPI_M_CLK	–	–	–
SPI_M_MOSI	–	–	–
SPI_M_MISO	–	–	–
DMIC_CLK1	–	GP29	–
DMIC_CLK2	GP0	UART_RX	–
DMIC_DAT1	–	GP8	–
DMIC_DAT2	–	GP13	UART_TX
I2S2_PCM_RX_CLK	–	–	–
I2S2_PCM_RX_WS	–	–	–
I2S2_PCM_TX_WS	–	–	–
I2S2_PCM_RX_DAT	–	–	–
I2S2_PCM_TX_DAT	–	–	–

GPIO Functional Applications

GPIOs can be used to implement various software-driven functions. Many of these I/Os also have alternate, hardware-based functionality. Basic GPIO functionality is managed through a set of registers in the AHB Registers Module, or alternatively through a set of ARM M0+ I/O Bus Registers. The AHB registers are available to any AHB bus master, while the ARM M0+ I/O Bus registers are available only to the ARM M0+ processor. Both sets of registers control the same GPIO functionality, and provide the following control capabilities for all GPIO capable device I/Os:

- Establish GPIO output drive state
- Establish GPIO output driver enable
- Establish GPIO input receiver enable
- Read current GPIO pin state
- Enable interrupt propagation to ARM and DSP CPUs
- Enable rising edge interrupt capture
- Enable falling edge interrupt capture
- Read current interrupt status

In addition to basic GPIO functionality, certain electrical operating characteristics may be managed through registers in the AHB Registers Module. These include:

- Output drive strength
- Enabling an integrated pull-up or pull-down

GPIOs with MADC Functionality

The following two GPIO pins have optional hardware-based monitor ADC functionality:

- GP14 – MADC3
- GP16 – MADC1

If MADC functionality is selected for any of these GPIOs, the output drivers, the integrated pull-ups and the integrated pull-downs are automatically disabled. Aside from these specific modifications, the GPIO management functions for these I/Os (such as input receiver enable, etc) continue to be derived from the GPIO control registers when MADC functionality is selected.

GPIOs with I^2C Functionality

The following four GPIO pins have optional hardware-based I^2C functionality:

- GP18 – I2C_S_CLK or I2C1_M_CLK
- GP19 – I2C_S_DAT or I2C1_M_DAT
- GP20 – I2C2_M_CLK
- GP21 – I2C2_M_DAT

Note that the I^2C-capable I/Os use unique I^2C circuitry which impacts behavior, even when GPIO functionality is selected in the following ways:

- These I/O have open-drain output drivers only. They are capable of driving low, but not high.
- The output drive strength is not controllable
- No built-in pull-up or pull-down is available
- The input electrical performance differs from the standard CMOS input receivers.

If I^2C functionality is selected for any of these GPIOs, the output-enable and input-enable functions will be automatically configured appropriately for the selected function (output only, input only, or bi-directional). An *I^2C High Speed* mode selection is available if I^2C functionality is selected for any of these pins.

Design Note: These I/O pad cells include an I^2C mode control, which is automatically enabled if I^2C functionality is selected.

GPIOs with LED PWM Functionality

The following four GPIO pins have optional hardware-based LED PWM functionality:

- GP22 – PWM_LED0_R
- GP23 – PWM_LED0_G
- GP24 – PWM_LED0_B

Note that the LED PWM-capable I/Os utilize special high current capable circuitry. This impacts behavior, even when GPIO functionality is selected in the following ways:

- A different set of output current drive strength selections are available. If LED PWM functionality is selected for any of these GPIOs, the output enable will be automatically asserted, and the integrated pull-up and pull-down features will be automatically disabled.

Design Note: These I/O pads cells include a GPIO_MODE control input, which is to be permanently tied to the GPIO mode.

GPIOs with Other Digital Functionality

A number of I/Os have additional, optional hardware-based functionality. These utilize the same pad I/O circuitry as the Simple GPIO (above).

- GP8 – DMIC_DAT1
- GP9 - UART_RX
- GP10 - UART_TX
- GP13 – DMIC_DAT2
- GP14 – SPDIF Input
- GP15 - USB 5V detect
- GP29 – DMIC_CLK1
- GP30 – I2S2_PCM_TX_CLK, SPI_M_SS1
- GP31 – MCLK

Most of these alternate functions (with the exception of USB 5V detection) are selected through register settings in the IO Function Selection (IO_MUX_A) or IO Function Selection (IO_MUX_B) register. If any of these alternate functionalities are selected for any of these I/Os, the output drivers and input receivers are automatically controlled as appropriate for the selected function (input, output or bi-directional).

The integrated pull-up and pull-down functions, as well as the output drive strength, are not controlled automatically, however, and should be set using the associated GPIO control registers. The USB 5V detect functionality of GP15 requires that the input receive function for GP15 be enabled, and that the output driver and integrated pull-up/pull-down be disabled. It does not require selection via the IO multiplexer registers.

GPIO Functionality on Multiple I/Os

Several device digital I/Os use GPIO functionality as an alternative function that is redundant with the corresponding GPIO I/O. These pins, and their alternate GPIO functions, are:

- DMIC_CLK2 - GPIO 0
- DMIC_DAT1 - GPIO 8
- DMIC_DAT2 - GPIO 13
- DMIC_CLK1 - GPIO 29

When GPIO functionality is selected as an alternate function for one of these pins, it appears simultaneously on its primary pin and the alternate pin. All of the control of the GPIO is managed as usual for the GPIO, with the one exception that the input value is determined by the logical OR'ing of the inputs from the primary and alternate pin. The usual control of the DMIC_CLK1, DMIC_CLK2, DMIC_DAT1 or DMIC_DAT2 pins is non operational if GPIO functionality is selected.

Multi-Button Headset Controls

Communications headsets provide control buttons that are integrated into the headset. The most common implementation is a single button that shorts the microphone input to ground. This button is typically used for call answer, call end, mute, and unmute depending on the duration of the button press.

Many headsets provide two additional buttons for volume (up/down) and other functions. These buttons connect a resistance across the microphone to change the voltage measured on the microphone pin. These resistances may be linear devices such as resistors or nonlinear devices such as diodes.

Multiple button support is targeted for four buttons as described by the Google standard. One of the Monitor ADCs can be used to support this multi-button function.

Feature-Algorithms

Wake on Voice

Wake on Voice (WoV) is activated by voice and listens for personalized commands without consuming valuable battery life. The implementation of a voice trigger is conducted with a CPU processor by performing voice activity and keyword detection. Once a trigger phrase is detected, the CPU can wake up the host via USB or via GPIO pins toggle or via an I^2C command. WoV implementation is system-dependent.

Smart Voice Pickup

The Synaptics SVP function provides optimum transmit microphone voice quality for headset users by reducing ambient noise to optimize the real-time voice communication experience. With SVP technology, on-line gamers can hear each other loud and clear – even in noisy environments such as a busy household, school dormitory or gaming café.

SVP technology is based on a proprietary SSP noise suppression algorithm. SSP is a blind source separation technology that uses spatial representation of target speech and noise sources to reduce interference and achieve up to 45 dB noise suppression and up to 19 dB signal-to-noise ratio (SNR) improvement.

Clocking

Primary Clock Sources

The CX21888 device utilizes two primary clocking sources, a 24 MHz crystal oscillator and an on-die RC oscillator. The 24 MHz crystal oscillator is used in most power states. It is also the first clock to be active following a power-on reset. It may be shut off under firmware control when entering low power operating states. However, care must be exercised to not leave the device without any clock source and with no active wakeup mechanisms.

The XTLI input of the 24 MHz crystal oscillator may also be driven directly by an external clock source. The internal oscillator circuity will detect this condition, and automatically shut off, saving power. The external clock source should provide a 24 MHz reference.

Derived Clocks

Numerous on-chip clocks are derived from the crystal, RC oscillator and PLL clocks described above. In some cases, clocks can also be derived from interface clock signals. For example, timer clocks may be optionally derived from I^2S frame clocks.

DSP Peripheral

Typically, the clocks for both DSP cores and most DSP peripherals (including memories) are derived from the PLL1 output, with a division of between 1 and 192. Note that this division consists of a pre-divide of from 1 to 3, followed by a power-of-2 divide of between 1 and 64.

In low power states, the clocks may be derived from the RC oscillator output. Both DSP cores, and most DSP specific peripherals, always operate at the same frequency. The three clocks (DSP 0, DSP 1 and DSP peripheral) are identical, except that each is independently gated. The maximum DSP clock frequency is 100 MHz.

Note that while the DSP and AHB clocks are synchronous to each other. They are not necessarily at the same frequency.

DSP Timers

The six DSP timers can be clocked from any of the following clock sources:

- Crystal oscillator
- DSP clock (divided by 2)
- ARM/AHB clock
- SPDIF Input module clock (divided by 2)
- I2S0 RX frame clock
- I2S0 TX frame clock
- I2S1 RX frame clock
- I2S1 TX frame clock
- I2S2 RX frame clock
- I2S2 TX frame clock

Note that this list of timer clock sources has been updated from Hudson/Reno, and that the associated control registers have also been modified to accommodate the new list of clock sources. Many of these clock sources are asynchronous to each other, and to the DSP clock. The individual timer modules are designed to accommodate the required asynchronous clock domain crossings.

ARM M0+ CPU and AHB

DSP and AHB clocks are synchronous to each other. They are not necessarily at the same frequency.

The maximum ARM/AHB clock rate is 50 MHz.

The ARM M0+ CPU receives four versions of the ARM/AHB clock. All four are identical, with the exception of when each may be gated off for power savings.

Synchronous Clocks

FCLK

The first of the four synchronous clocks, FCLK is a *free running* clock. It clocks a small amount of logic in the WIC portion of the CPU. FCLK must be running for the CPU to recognize and wake from interrupt events.

However, when a deep-sleep state is entered, the PMU provides a mechanism to automatically stop the FCLK to conserve power. When a wakeup event is detected, the PMU then re-starts the FCLK. This supports a truly static deep-sleep state, whereas the ARM CPU would otherwise require FCLK to continue running during deep-sleep.

SCLK

The second of the four synchronous clocks, SCLK clocks a small amount of logic in the processor, primarily in the NVIC. It may be gated off if the processor is in a WIC deep sleep mode, unless a debugger is connected.

HCLK

The third of the four synchronous clocks, HCLK provides clocking for the majority of the processor. It may be gated off if the processor is in a sleep mode (WIC or non-WIC), unless a debugger is connected. The GATEHCLK output from the CM0PINTEGRATION module is available to indicate when HCLK may be gated off.

DCLK

The fourth of the four synchronous clocks, DCLK provides clocking to debug interface logic that is not clocked by the debugger clock (below). It may be gated off at any time that a debugger is not connected. The CDBGPWRUPACK input to the CM0PINTEGRATION module will indicate when a debugger is connected, and can be used to control clock gating.

ARM M0+ CPU Debug Clock Input

In addition to the four synchronous clocks listed above, a portion of the ARM M0+ CPU logic is clocked by an attached debugger. This clock input is SWCLKTCK.

ARM M0+ CPU SysTick Timer Clock

The SysTick timer within the ARM M0+ CPU is clocked by the CPU's SCLK input. However, the CPU provides a mechanism for coordinating the SysTick with a synchronized version of an external time base.

ARM Timers

The three ARM timers are clocked by the AHB bus clock. The clock generation module can, however, provide a divided version of several clock sources to the AHB Timers module. These divided clocks are treated as data within the AHB Timers module, and synchronized into the AHB bus domain, where they can be used to trigger counting of by the AHB timers. The available divided clock outputs are:

- Crystal oscillator
- RC oscillator
- PLL2 output
- PLL3 output

The division factor is specified by registers in this Clock Generation module (not within the AHB Timers module). Note that the maximum reference frequency for the AHB timers is 12.5 MHz.

USB

The USB controller requires a 60 MHz clock. Typically, this will be provided by PLL4, operating at 60 MHz. The USB controller is also attached to the AHB bus as a slave for register access, and to the AHB bus as a master for data transfers.

SPI Master

The SPI master interface module requires a clock of up to 100 MHz, to provide a maximum serial throughput of 50 Mbps. This would typically be provided as a divided version of the PLL1 output, but may be provided as a divided version of any of the PLLs, or the crystal oscillator.

The SPI master interface module also attaches to the APB bus for register access, and the AHB bus as a slave for data FIFO access.

Digital Microphone

The digital microphone integrated circuit (IC) module supports up to four attached digital microphones. The microphones share a common clock output from the CX21888. Internally, the module is implemented as four separate datapaths, each with a separately gated clock. The internal gated clocks operate at the same frequency as the external microphone clock. The microphone clock may be configured for operating frequencies from about 384 KHz to about 4 MHz. These limits represent the anticipated operating limits of any attached microphones.

Because the digital microphone interface transports data on both edges of the interface clock, a 2x speed clock is also used within the module, but is limited to a small portion of the module logic. This clock is

enabled automatically when any of the datapath clocks are enabled.

The clock divider control register is used to establish the 2x clock speed. The bit rate is automatically configured as ½ the selected clock frequency. The DMIC module also uses the AHB (APB) clock for a bus interface and audio DMA interface.

I2S/PCM

The I2S/PCM supports a maximum clock rate of 50 MHz and typically uses a divided version of the PLL2 output or PLL3 output, depending on whether the sample rate is related to 48 Ksps or 44.1 Ksps.

Note that when operating in slave mode, the incoming I2S bit clock is used as a clock within the module.

The I2S/PCM interface module also uses the AHB clock for a bus interface and an audio DMA interface. The S/PDIF output module uses a 24.576 MHz clock (typically divided from PLL2) for 48 Ksps-related sample rates, or a 22.579 MHz clock (typically divided from PLL3) for 44.1 Ksps related sample rates. It also utilizes AHB clock for an APB bus interface and an audio DMA interface.

The S/PDIF input module uses a high speed clock to over-sample the incoming waveform. This is typically provided as either a direct or divided version of the PLL2 output, for sample rates related to 48 Ksps, or PLL3 for sample rates related to 44.1Ksps. The SPDIF input module also utilizes the AHB clock, as it interfaces with the APB bus for register access, and the audio DMA for data transfers.

UART

The UART utilizes the AHB bus clock for both the internal serializer/deserializer functionality, and the AHB bus interface.

I2C Master

Utilizes the AHB clock only.

I2C Slave

Utilizes the incoming I2C clock from an external master for serializer/deserializer function. Utilizes AHB clock for bus interface.

Audio DMA

AHB clock only.

Flexi DMA

Uses AHB clock only.

LED PWM

The LED PWM clock is derived from the RC oscillator (at 6 MHz) or the Crystal Oscillator (at 24 MHz). A divider is used to create 93.75 KHz for the LED PWM module.

Monitor ADC

The monitor ADC clock is derived from the RC oscillator (at 6 MHz) or the Crystal Oscillator (at 24 MHz). A divider is used to create 750 kHz for the monitor ADC module.

Other Clock-Derived Outputs

In addition to derived clock outputs, the clock generation module creates a number of timing references that are not directly used as clocks. Instead, these references are typically sampled by flip-flops, as data inputs.

PLL2 / PLL3 - Tracking and ARM Timer Reference Outputs

As noted above, PLL2 and PLL3 are each supported by PLL Tracking mechanisms, which allow these PLLs to be frequency locked to alternate frequency references (see PLL Tracking Loop above).

Included among the alternate frequency references are the outputs of the PLLs themselves. PLL2 can track PLL3, and PLL3 can track PLL2. To facilitate this, a divided version of each PLL output is made available. The division to be applied to each PLL output is established in the PLL2_Control1 and PLL3_Control1 registers.

In addition to being available as PLL tracking references, these divided outputs are available as timing references for the ARM Timers. See “ARM Timers” on page 38.

Note that the maximum reference frequency for the ARM Timers is 12.5 MHz.

RC Oscillator - Timer Reference Output

The RC Oscillator is available as a reference to the ARM Timers, as noted in the ARM Timers chapter of this document. See “ARM Timers” on page 38. To facilitate this, a divided version of the RC Oscillator is made available. The division to be applied is established in the ARM_Timer_Clock_and_WD_Reset_Control register.

In addition to serving as a reference to the ARM timers, this divided RC oscillator output is available to create a wakeup event when the PMU places the device into a deep sleep state.

ARM SysTick Reference Output

The ARM M0+ CPU implements an internal timer, referred to as the SysTick timer. The logic for this timer exists within the ARM M0+ CPU, and operates from the CPU’s SCLK clock input. However, since the ARM CPU clock rate is variable, the SysTick timer requires an additional timing reference in order to maintain consistent timing accuracy.

The additional timing reference is a pulse stream, derived from either the crystal oscillator or the RC oscillator, and synchronized into the CPU SCLK clock domain. Each pulse is 1 SCLK period in duration, and is derived such that it can be timing closed with the ARM CPU, synchronously with SCLK.

The selection between the crystal oscillator and RC oscillator is accomplished in the Processor_Clk_Source register.

The frequency of the pulse stream is configurable through register settings. The ARM M0+ CPU does, however, require information regarding the pulse stream frequency. This takes the form of an input and is programmable through a register setting to indicate how the pulse stream frequency relates to 100 Hz. The pulse stream should generally be configured as a multiple of 100 Hz. If not, an additional indication to the ARM M0+ CPU is available, through a register setting, to indicate that no such relationship exists.

DSP Core Features

The CX21888 device integrates two Conexant Audio Processing Engine (CAPE) DSP cores. Other DSP-related chapters within this document describe additional modules that are closely related to the DSP cores. This section describes a number of features of the DSP core, and how two instances of the core are used within the CX21888 device. The section is not intended to provide an exhaustive description of the DSP, but rather a summary of specified aspects that are essential for understanding the overall CX21888 device architecture.

Clock

The DSP is synchronous to the rising edge of a single clock input (clock). Within the CX21888 device, the maximum clock frequency for the DSP is 100 MHz.

Reset

The DSP uses a single synchronous, active low reset input (reset_n_ext).

DSP Memory System and Interfaces

The DSP uses a Harvard architecture, with separate program and data interfaces. Additionally, it implements two data related interfaces, rather than just one, to expedite signal processing functions.

Each DSP is grouped into three memory interfaces (Program, X-Data and Y-Data). However, rather than provide three independent memory groupings for each of the two DSPs (for a total of six groupings), a single grouping of each type is shared between the two DSPs. Additionally, the DSP memories are accessible by either AHB layer.

The DSP Memory System is responsible for arbitrating between all of these accesses to the various DSP memories. To help minimize contention for memory access, each of the three memory groupings is further divided into sub-sections. Contention will only occur if two or more bus masters are attempting to access the same memory subsection.

In addition to the three memory groupings, the DSP Memory System arbitrates access to a limited set of registers that are mapped to the DSP Y address spaces. The following describes the three memory interfaces.

Program Memory Interface (P)

The DSP implements mostly 20-bit wide instructions, but also implements a number of 40-bit wide instructions. The P memory interface is therefore 40 bits wide. In most circumstances, this results in the fetching of two instructions per clock cycle, allowing both of the internal MACs to be fully utilized. The P interface consists of a 40-bit wide data input bus, a 40-bit wide data output bus and an 18-bit address bus.

Data Memory Interface (X)

The X data memory interface is 64 bits wide, and supports 16, 32 and 64 bit wide accesses. Note that 8-bit accesses are not supported. The X data memory interface implements separate data buses for each of the possible access widths. So, in total, the X data memory interface implements a 16-, 32- and 64-bit wide input data bus, a 16-, 32- and 64-bit wide output data bus, and a 21-bit address bus.

Note that the address data unit is a 16-bit word.

Data Memory Interface (Y)

The Y data memory interface is 32 bits wide, and supports 16 and 32 bit wide accesses. Note that 8-bit accesses are not supported. The Y data memory interface implements separate data buses for each of the possible access widths. So, in total, the X data memory interface implements a 16- and 32-bit wide input data bus, a 16- and 32- bit wide output data bus, and a 21-bit address bus.

Note that the address data unit is a 16-bit word. Within the CX21888 device, DSP access to peripherals (registers) are mapped to the Y data bus. It should be specifically noted that because the Y interface implements separate 16- and 32-bit data buses, a given register may be implemented such that it responds to only a 16- or 32-bit wide access.

DSP Memory Subgroups

The CX21888 DSP has a total of 21 memory (and register) subgroups as shown in Table 5.

*Table 5: **DSP Memory Subgroups***

Program Memory Subsections	X-Data Memory Subsections	Y-Data Memory Subsections
Program ROM Sec 0	X-Data RAM Sec 0	Y-Data RAM Sec 0
Program ROM Sec 1	X-Data RAM Sec 1	Y-Data RAM Sec 1
Program ROM Sec 2	X-Data RAM Sec 2	Y-Data RAM Sec 2
Program ROM Sec 3	X-Data RAM Sec 3	Y-Data RAM Sec 3
Program RAM Sec 0	X-Data RAM Sec 4	Y-Data ROM Sec 0
Program RAM Sec 1	X-Data RAM Sec 5	Y-Data ROM Sec 1
Program RAM Sec 2	X-Data ROM Sec 0	DSP registers

External Interrupt Controller

There are many sources of interrupt exceptions within the CX21888 device. An interrupt controller module external to the DSP cores is used to organize these interrupt sources, and route them to the two DSP cores. One Interrupt Controller module is used to manage interrupts to both DSP cores. The interrupt controller module provides an indication of the highest priority interrupt source that is asserting an interrupt at any given time.

It should be noted that the Interrupt Controller in the CX21888 device routes interrupts to just the ireq_n[2:0] inputs of the DSP cores. The ireq_n[7:3] inputs are unused.

As previously noted, ireq_n[0] is the non-maskable interrupt (NMI) input to the DSP processors, while ireq_n[2:1] are maskable through the Interrupt Mask Register (internal to DSP) and must be enable with the IE bit of the Status register.

Boot

The power-on-default state of the CX21888 device holds both DSP cores in an unpowered state. The ARM M0+ CPU will boot first. When appropriate, the ARM M0+ will enable power to the DSP cores. It will also enable clocking to DSP 0 and release DSP 0 from reset.

The ARM M0+ CPU has its own reset status registers, separate from the DSP core registers. Software running on the ARM M0+ CPU can leave the DSP reset status registers unchanged, in which case, from the perspective of DSP 0, it will appear that a power-on reset (POR) has occurred.

Analog Volume Non-Linearity (DNL and INL)

Differential nonlinearity (DNL) describes the deviation between two analog values corresponding to adjacent input digital values.

Integral nonlinearity (INL) defines the maximum deviation between the ideal output of a DAC and the actual output level (after offset and gain errors have been removed).

Both processes are essential specification for measuring error in a DAC.

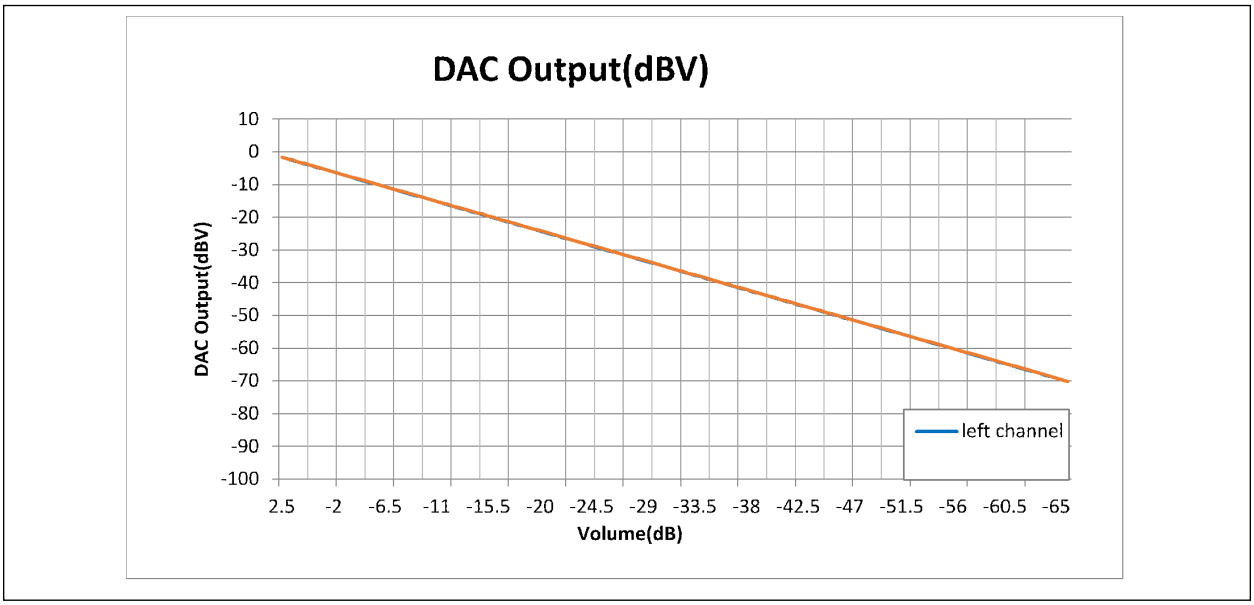


Figure 18: DAC Output versus Volume Setting

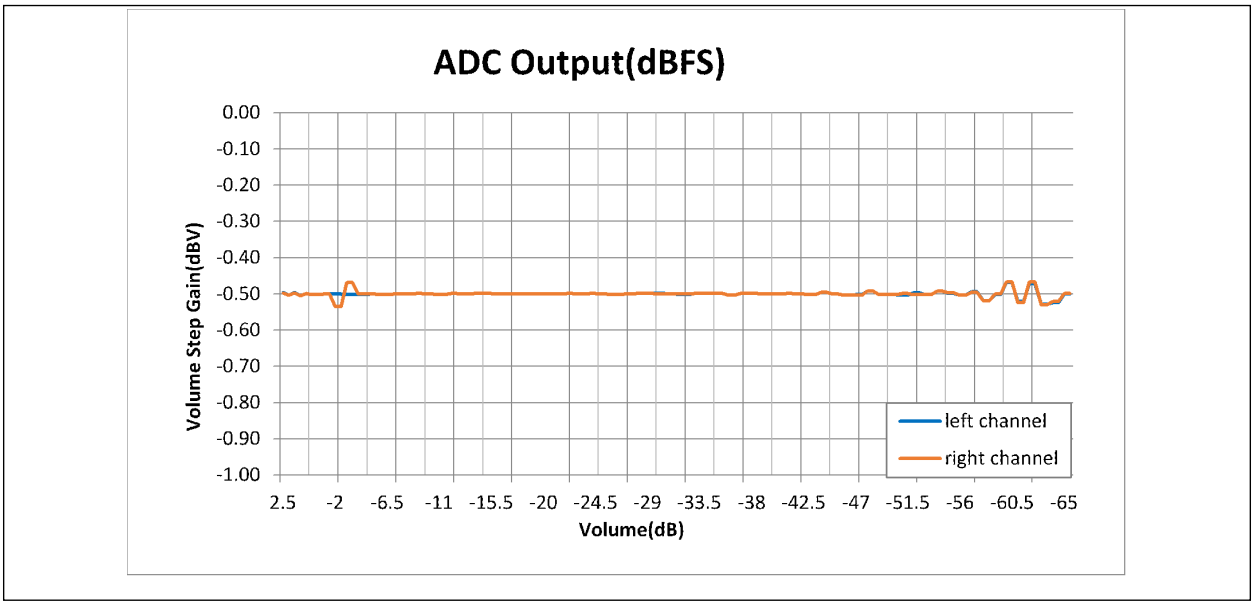


Figure 19: ADC Output versus Volume Setting

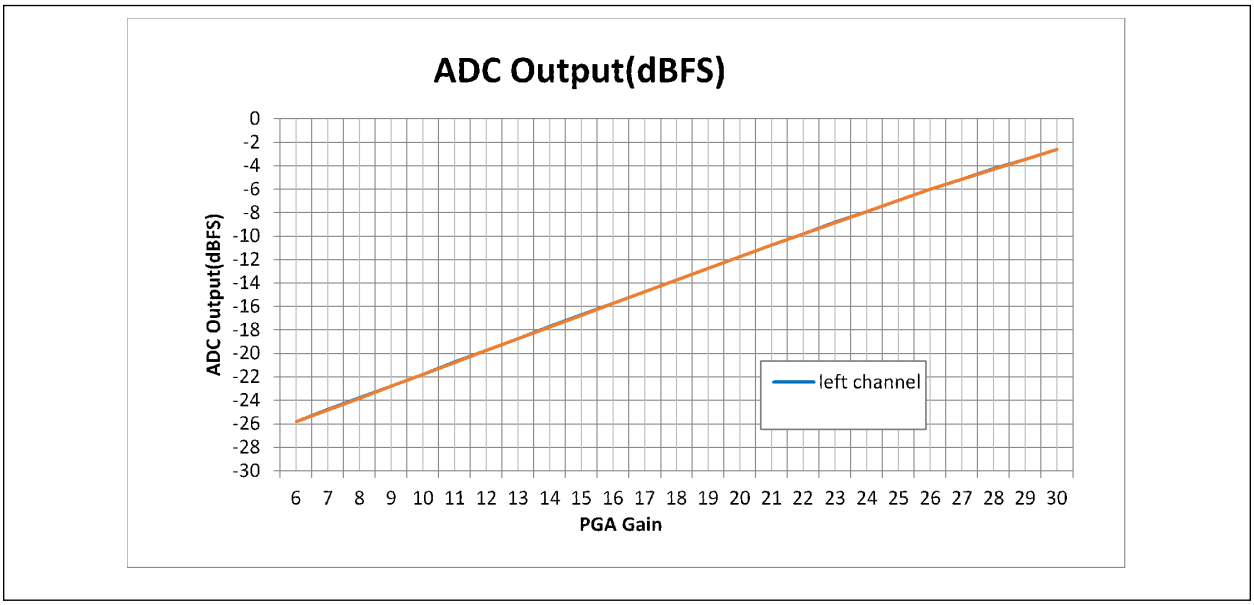


Figure 20: ADC Output versus PGA Gain

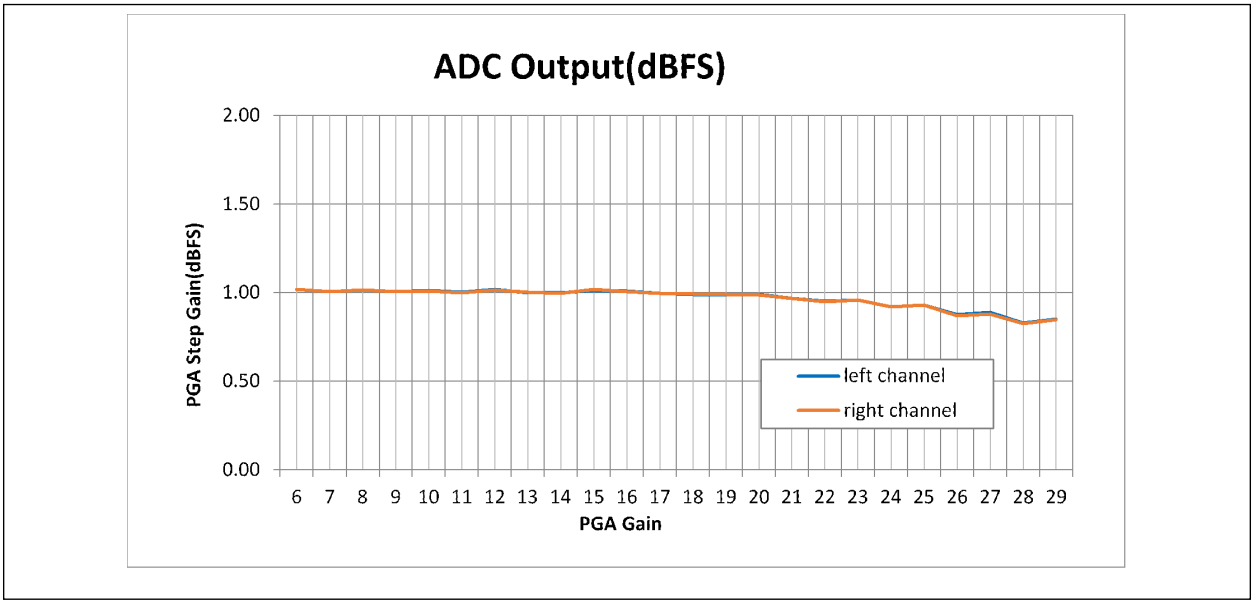


Figure 21: PGA Step Gain versus PGA Gain

Pin Descriptions

Pin Diagram

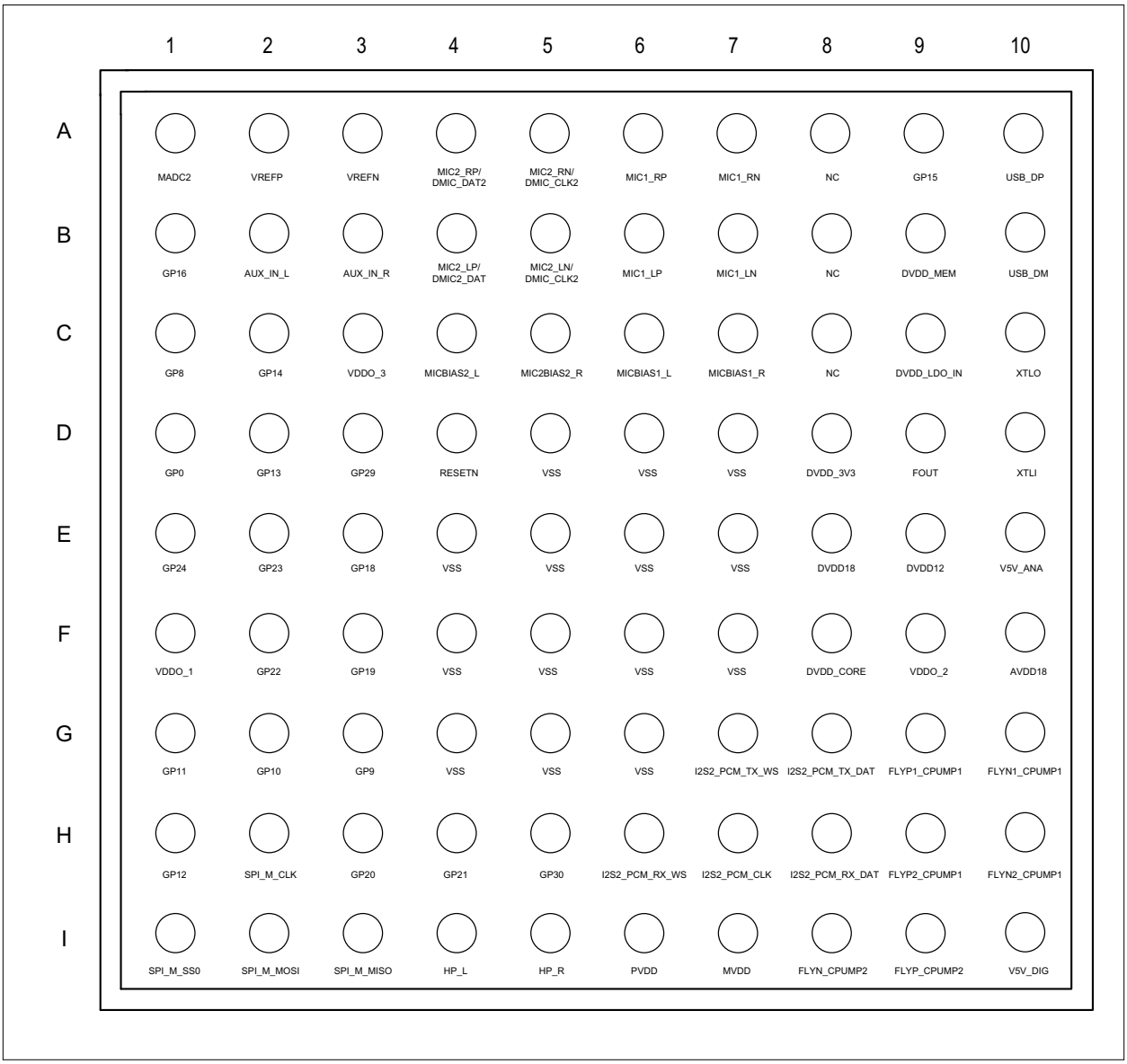


Figure 22: CX21888 Pin Diagram

Pin Assignments and Signal Definitions

Table 6: Pin Assignments and Signal Definitions

Label	Pin Number	I/O Type	Default pull up/pull down	Configurable pull up/pull down	Signal Name/Description
Crystal Signals					
XTLI	D10	Digital In	–	–	Crystal In. Connect XTALI to a 24MHz crystal circuit.
XTLO	C10	Digital Out	–	–	Crystal Out. Connect XTALO to the crystal circuit return.
I2S/PCM and S/PDIF Interfaces					
I2S2_PCM_TX_DAT	G8	Digital Out	–	Yes	I2S/PCM Port 1 Transmit (Tx) Word Data.
I2S2_PCM_RX_DAT	H8	Digital In	–	Yes	I2S/PCM Port 1 Receive (Rx) Word Data
I2S2_PCM_TX_WS	G7	Digital I/O	–	Yes	I2S /PCM Word Port 1 Tx Select
I2S2_PCM_RX_WS	H6	Digital I/O	–	Yes	I2S /PCM Word Port 1 Rx Select
I2S2_PCM_TX_CLK/ SPI_M_SS1/GP30	H5	Digital I/O	–	Yes	I2S /PCM Port 1 Tx Bit Clock. Alternate functions: • SPI Slave Select 1 • GPIO
I2S2_PCM_ CLK	H7	Digital I/O	–	Yes	I2S /PCM Port 1 Rx Bit Clock.
SPI Control Interface					
SPI_M_SS0	J1	Digital Out	–	Yes	SPI Slave Select 0
SPI_M_CLK	H2	Digital Out	pull down (40k-60k)	Yes	SPI Clock
SPI_M_MOSI	J2	Digital Out	–	Yes	SPI Master Output
SPI_M_MISO	J3	Digital In	–	Yes	SPI Master Input
* I^2C: Note that this I/O has an open-drain output driver only, either in GPIO or I2C mode.					
I2C_MS_DAT/GP19 *	F3	Digital I/O	–	–	I2C Master/Slave Data. Master/ slave mode selectable through the firmware setting. Alternate function: • GPIO
I2C_MS_CLK/GP18 *	E3	Digital I/O	–	–	I2C Master/Slave Clock. Master/ slave mode selectable through the firmware setting. Alternate function: • GPIO
I2C2_M_DAT/GP21 *	H4	Digital I/O	–	–	I2C Master/Slave Data. Alternate function: • GPIO
I2C2_M_CLK/GP20 *	H3	Digital Out	–	–	I2C Master/Slave Clock. Alternate function: • GPIO

Table 6: Pin Assignments and Signal Definitions (Continued)

Label	Pin Number	I/O Type	Default pull up/pull down	Configurable pull up/pull down	Signal Name/Description
Monitor ADC (MADC)					
MADC3/SPDIF_IN/GP14	C2	Analog In	–	Yes	Monitor ADC 3. This low resolution analog input can be connected to a volume knob, battery sensor, or temperature sensor. Alternate function: • S/PDIF • GPIO
MADC2	A1	Analog In 5V tolerant	–	–	Monitor ADC 2. This low resolution analog input can be connected to a volume knob, battery sensor, or temperature sensor.
MADC1/GP16	B1	Analog In Digital I/O	–	Yes	Monitor ADC 1. This low resolution analog input can be connected to a volume knob, battery sensor, or temperature sensor. Alternate function: • GPIO
USB					
USB_DP	A10	Digital I/O	–	–	USB Data Positive.
USB_DM	B10	Digital I/O	–	–	USB Data Negative.
Reset					
RESETN	D4	Digital In	pull up (40k-60k)		Reset. Active low input asserted to initialize registers, sequencers, and signals to a consistent reset state. The RESETN signal should remain low for 5ms after all power rails have become stable, and then should go to VDDO.
Button/Keyboard Interface					
KSOUT0/GP11	G1	Digital In	–	Yes	Volume Down Keypad Scan Input. For use with a standard four-button keypad interface.
KSOUT1/GP12	H1	Digital In	–	Yes	Volume Up Keypad Scan Input. For use with a standard four-button keypad interface.
Tri-Color PWM LED					
PWMLED0_R/GP22	F2	Digital Out	–	Yes	Tri-color PWM LED (Red). Alternate function: • GPIO
PWMLED0_G/GP23	E2	Digital Out	–	Yes	Tri-color PWM LED (Green). Alternate function: • GPIO
PWMLED0_B/GP24	E1	Digital Out	–	Yes	Tri-color PWM LED (Blue). Alternate function: • GPIO

Table 6: Pin Assignments and Signal Definitions (Continued)

Label	Pin Number	I/O Type	Default pull up/pull down	Configurable pull up/pull down	Signal Name/Description
GPIO					
USB_5V_DET/GP15	A9	Digital In	–	Yes	USB 5V Detect. At this pin, the USB 5V VBUS signal should be connected to a resistor divider to reduce the level to 3.3V. Alternate function: • GPIO
UART					
UART_RX/GP9	G3	Digital In	–	Yes	UART Rx. Alternate function: • GPIO
UART_TX/GP10	G2	Digital Out	–	Yes	UART Tx. Alternate function: • GPIO
Digital Microphone					
DMIC_DAT1/GP8	C1	Digital In	–	Yes	Digital Microphone (for voice pickup) Port 1 Data. Alternate function: • GPIO
DMIC_CLK1/GP29	D3	Digital Out	–	Yes	Digital Microphone (for voice pickup) Port 1 Clock. Alternate function: • GPIO
DMIC_DAT2/GP13	D2	Digital In	–	Yes	Digital Microphone (for voice pickup) Port 2 Data. Alternate function: • GPIO
DMIC_CLK2/GP0	D1	Digital Out	–	Yes	Digital Microphone (for pickup) Port 2 Clock. Alternate function: • GPIO
DMIC1_CLK	B5	Digital Out	–	–	Digital Microphone (for ref mic) Port 1 Clock. Alternate function: • MIC2_LN
DMIC1_DAT	B4	Digital In	–	–	Digital Microphone (for ref mic) Port 1 Data. Alternate function: • MIC2_LP
DMIC2_CLK	A5	Digital Out	–	–	Digital Microphone (for err mic) Port 1 Clock. Alternate function: • MIC2_RN
DMIC2_DAT	A4	Digital In	–	–	Digital Microphone (for err mic) Port 1 Data. Alternate function: • MIC2_RP

Table 6: Pin Assignments and Signal Definitions (Continued)

Label	Pin Number	I/O Type	Default pull up/pull down	Configurable pull up/pull down	Signal Name/Description
Analog Audio Inputs					
MIC1_RP	A6	Analog In	–	–	Reference Microphone Input Right (Positive). Use with single-ended microphone implementations.
MIC1_RN	A7	Analog In	–	–	Reference Microphone Input Right (Negative). Use with differential microphone implementations.
MIC1_LP	B6	Analog In	–	–	Reference Microphone Input Left (Positive). Use with single-ended microphone implementations.
MIC1_LN	B7	Analog In	–	–	Reference Microphone Input Left (Negative). Use with differential microphone implementations.
MIC2_RP	A4	Analog In	–	–	Error Microphone Input Right (Positive). Use with single-ended microphone implementations.
MIC2_RN	A5	Analog In	–	–	Error Microphone Input Right (Negative). Use with differential microphone implementations.
MIC2_LP	B4	Analog In	–	–	Error Microphone Input Left (Positive). Use with single-ended microphone implementations.
MIC2_LN	B5	Analog In	–	–	Error Microphone Input Left (Negative). Use with differential microphone implementations.
AUX_IN_R	B3	Analog In	–	–	Line Input Right
AUX_IN_L	B2	Analog In	–	–	Line Input Left
Analog Audio Outputs					
HP_L	J4	Analog Out	–	–	Headphone Left Output.
HP_R	J5	Analog Out	–	–	Headphone Right Output.
Input Power					
V5V_DIG	J10	Power input	–	–	2.7V - 5V Supply Input.
V5V_ANA	E10	Power input	–	–	2.7V - 5V Supply Input.
Digital Power					
DVDD_CORE	F8	Power	–	–	VDD_CORE 1.1V Output.
VDDO	C3, F1, F9	Power input	–	–	Input Power. Connect to DVDD18 or DVDD33. All three VDDO pins must be connected to the same voltage rail.
DVDD_3V3	D8	Power output	–	–	Digital 3.3V Supply Output.

Table 6: Pin Assignments and Signal Definitions (Continued)

Label	Pin Number	I/O Type	Default pull up/pull down	Configurable pull up/pull down	Signal Name/Description
DVDD18	E8	Power output	–	–	Digital 1.8V Supply Output.
DVDD_MEM	B9	Power Output	–	–	Digital 1.1V Supply Output for Internal Memory.
DVDD_LDO_IN	C9	Power Input	–	–	Digital 1.25V Supply Input. Connect to DVDD12 pin.
DVDD12	E9	Power Output	–	–	Digital 1.25V Supply Output.
Analog Power					
AVDD18	F10	Power Output	–	–	1.8V Analog Power Output.
VREFP	A2	Power Output	–	–	Analog Reference Power (Positive).
VREFN	A3	Power Output	–	–	Analog Reference Power (Negative).
MICBIAS1_L	C6	Power Output	–	–	Reference Microphone Bias (Micbias) Output (Left).
MICBIAS1_R	C7	Power Output	–	–	Reference Micbias Output (Right).
MICBIAS2_L	C4	Power Output	–	–	Error Microphone Bias (Micbias) Output (Left).
MICBIAS2_R	C5	Power Output	–	–	Error Micbias Output (Right).
CP Reference Voltage					
FLYP1_CPUMP1	G9	Power	–	–	CP Fly Capacitor, Core Voltage.
FLYN1_CPUMP1	G10	Power	–	–	CP Fly Capacitor, Core Voltage.
FLYP2_CPUMP1	H9	Power	–	–	CP Fly Capacitor, Core Voltage.
FLYN2_CPUMP1	H10	Power	–	–	CP Fly Capacitor, Core Voltage.
PVDD	J6	Power Output	–	–	Internally Generated Positive Supply, Headphone CP.
MVDD	J7	Power Output	–	–	Internally Generated Negative Supply, Headphone CP.
FLYP_CPUMP2	J9	Power	–	–	CP Fly Capacitor, Headphone.
FLYN_CPUMP2	J8	Power	–	–	CP Fly Capacitor, Headphone.
Ground Signal					
GROUND	E4, F4, G4, D5, E5, F5, G5, D6, E6, F6, G6, D7, E7, F7	Ground	–	–	Ground pins

Power Management

The power management of audio codec operates off of a single power supply with a range of 2.7V to 5.5V. Internal to the codec is a complex power management architecture that generates the different required power supplies. This ensures an efficient and comprehensive system power consumption scheme.

DVDD33, 3.3V, Output

Generated from internal LDO, sourced by 5V input power and provides up to 100 mA to external devices.

DVDD18, 1.8V, Output

Generated from the internal LDO sourced by the 5V input power. Use this pin to provide up to 100 mA to external devices.

AVDD18, 1.8V, Output

Generated from the internal LDO sourced by the 5V input power. This supply is used for Line-in, Mic-in, and Programmable Gain Amplifier (PGA) functions.

VDDO, Input

All three VDDO pins are used to power the digital I/O interfaces. These pins should be connected to either the DVDD33 or DVDD18 power output, depending on the required I/O level. All three pins must be connected to the same voltage, which means that all I/Os must run at the same voltage level.

VDD_CORE, Internal

Digital 1.1V power, internal. This supply powers up the core logic.

DVDD_MEM, 1.1V, Internal

Digital 1.1V power for internal memory. All internal memories are connected to this power supply.

DVDD12, 1.25V, Output

Generated from the internal CP sourced by the 5V input power. This supply is used by the internal LDOs to generate core and memory power supplies.

DVDD_LDO_IN, 1.25V, Input

Connects to the DVDD12 output.

Charge Pumps

The charge pump (CP) functions as a DC to DC converter that uses capacitors as power-storage components to create either a higher- or lower-voltage power source. CP circuits can provide high efficiencies (often as high as 90–95%) while maintaining electrical simplicity.

Power Consumption

Case 1: USB Type C CODEC with Internal LDOs

The input voltage V5V_ANA = V5V_DIG = 5V is used for these measurements. The CX21888 provides the power supply for external SPI flash and four microphones in this scenario. Basic DSP functions (ASRC, EQ, DRC) are supported.

*Table 7: **CX21888 Power Consumption: Case 1***

Parameter	Min.	Typ.	Max.	Unit	Comments
USB Suspend Current	–	1.5	–	mA	The device is ready to wake-up from USB resume
Idle Current- ANC OFF	–	10	–	mA	ADC and DAC are powered down and processing is disabled.
Headphone Active, Output Level = -25dBFS (0.1mW) with ANC OFF	–	18	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Headphone Active, Output Level = -15dBFS (1mW) with ANC OFF	–	21	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with fixed feedforward ANC ON	–	21	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with fixed feedforward ANC ON	–	23	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with hybrid adaptive ANC ON	–	30	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with hybrid adaptive ANC ON	–	33	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active-stereo with ANC OFF	–	14	–	mA	Microphone input = -100dBV
Record Path Active, Headphone Active, Output Level=-15dBFS (1mW) with ANC OFF	–	24	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm playing 16-bit/48kHz sample rate, 997Hz tone
Wake-On-Voice (stage0 - VAD)	–	1.6	–	mA	Waiting for energy detection
Wake-On-Voice (stage1- key word detection)	–	3.7	–	mA	Listening for key word

Case 2: USB Type C CODEC with External Supplies for AVDD18 and DVDD33

The input voltage V5V_ANA = V5V_DIG = 5V is used for these measurements. External DC-DC converters are used for AVDD18 and DVDD33 over-riding internal LDOs. Basic DSP functions (ASRC, EQ, DRC) are supported.

*Table 8: **CX21888 Power Consumption: Case 2***

Parameter	Min.	Typ.	Max.	Unit	Comments
USB Suspend Current	–	1.4	–	mA	The device is ready to wake-up from USB resume
Idle Current- ANC OFF	–	8.45	–	mA	ADC and DAC are powered down and processing is disabled.
Headphone Active, Output Level = -25dBFS (0.1mW) with ANC OFF	–	15.7	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Headphone Active, Output Level = -15dBFS (1mW) with ANC OFF	–	18.7	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with fixed feedforward ANC ON	–	19	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with fixed feedforward ANC ON	–	21.6	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with hybrid adaptive ANC ON	–	25.7	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with hybrid adaptive ANC ON	–	29	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active- stereo with ANC OFF	–	11	–	mA	Microphone input = -100dBV
Record Path Active, Headphone Active, Output Level=-15dBFS (1mW) with ANC OFF	–	20	–		Microphone input = -36dBV, Headphone load = 32 ohm playing 16-bit/48kHz sample rate, 997Hz tone
Wake-On-Voice (stage0 - VAD)	–	1.5	–		Waiting for energy detection
Wake-On-Voice (stage1- key word detection)	–	3.5	–		Listening for key word

Case 3: I²S CODEC with Internal LDOs

The input voltage V5V_ANA = V5V_DIG = 3.3V is used for these measurements. The CX21888 provides the supply for external SPI flash and four microphones in this scenario. Basic DSP functions (ASRC, EQ, DRC) are supported.

*Table 9: **CX21888 Power Consumption: Case 3***

Parameter	Min.	Typ.	Max.	Unit	Comments
Idle Current- ANC OFF	–	3.5	–	mA	ADC and DAC are powered down and processing is disabled.
Headphone Active, Output Level = -25dBFS (0.1mW) with ANC OFF	–	20	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Headphone Active, Output Level = -15dBFS (1mW) with ANC OFF	–	23	–	mA	Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with fixed feedforward ANC ON	–	28	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with fixed feedforward ANC ON	–	31	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -25dBFS (0.1mW) with hybrid adaptive ANC ON	–	37	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active, Headphone Active, Output Level = -15dBFS (1mW) with hybrid adaptive ANC ON	–	40	–	mA	Microphone input = -36dBV, Headphone load = 32 ohm, playing 16-bit/48kHz sample rate, 997Hz tone
Record Path Active-stereo with ANC OFF	–	11	–	mA	Microphone input = -100dBV
Record Path Active, Headphone Active, Output Level=-15dBFS (1mW) with ANC OFF	–	28	–		Microphone input = -36dBV, Headphone load = 32 ohm playing 16-bit/48kHz sample rate, 997Hz tone

Electrical Characteristics

Table 10 describes test conditions.

- V5V_DIG = V5V_ANA = 5V
- DVDD12 = 1.2V
- AVDD18 = DVDD18 = PVDD = 1.8V
- MVDD=-1.7V, AGND=DGND=0V
- T_A = 25°C
- fin = 997Hz
- fs = 48kHz
- Gain setting = 0dB
- 24-bit audio data

Table 10: Test Conditions

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
DAC Output Path (HP_L, HP_R) Line-Out Load R_L=10kΩ					
Dynamic Range	-	-	110	-	dB
THD+N	–1dBFS (0.891V_{rms})	-	–79	-	dB
THD+N	–3dBFS (0.707V_{rms})	-	–79	-	dB
Crosstalk	10kHz @ –20dBFS	-	–92	-	dB
PSRR	100mV_{p-p}, 1kHz, Any Supply 100mV_{p-p}, 10kHz, Any Supply	-	-	-	dB
DAC Output Path (HP_L, HP_R) Headphone Load R_L=33 Ω					
Dynamic Range	-	-	110	-	dB
THD+N	–1dBFS (0.891V_{rms}) Pout = 24mW	-	–72	-	dB
THD+N	–3dBFS (0.707V_{rms}) Pout = 15.6mW	-	–77	-	dB
Crosstalk	10kHz @ –20dBFS	-	–83	-	dB
PSRR	100mV_{p-p}, 1kHz, Any Supply 100mV_{p-p}, 10kHz, Any Supply	-	-	-	dB
Headphone Output Driver (HP_L, HP_R)					
Minimum Output Load Resistance	-	TBD	-	-	Ω
Maximum Output Load Capacitance	-	-	-	400	pF
ADC Input Paths					
Maximum Full Scale Input	Single-ended Input	-	-	0.5 –6	Vrms dBv
	Differential Input	-	-	1 0	Vrms dBv
Input Resistance	Line-In (Single-ended) –6dB Line-In (Single-ended) 0dB Mic-In (Single-ended) Mic-In (Differential)	-	8K 16K 500K 500K	-	Ω

Table 10: Test Conditions (Continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Programmable Gain	Line-In (Single-ended)	–6	-	0	dB
	Line-In Gain Step	-	6	-	
	Mic-In (Single-ended and Differential)	6	-	30	
	Mic-In Gain Steps	-	1	-	
Dynamic Range	Differential Mic-In (6dB PGA Gain)	-	98.1	-	dB
	Differential Min-In (30dB PGA Gain)		92.8		
	Single-ended Mic-In (6dB PGA Gain)		97		
	Single-ended Mic-In (30dB PGA Gain)		91.7		
	Single-ended Line-In (0dB PGA Gain)		96.3		
THD+N	Differential Mic-In (6dB PGA Gain) –1dB FS	-	–70	-	dB
	Differential Mic-In (6dB PGA Gain) –3dB FS		–86		
	Differential Min-In (30dB PGA Gain) –1dB FS		–72		
	Differential Mic-In (30dB PGA Gain) –3dB FS		–82		
	Single-ended Mic-In (12dB PGA Gain) –1dB FS		–70		
	Single-ended Mic-In (30dB PGA Gain) –3dB FS		–80		
	Single-ended Mic-In (30dB PGA Gain) –1dB FS		–69		
	Single-ended Mic-In (30dB PGA Gain) –3dB FS		–74		
	Single-ended Line-In (0dB PGA Gain)		–80		
Channel Separation	Differential Mic-In	-	–87	-	dB
	Single-ended Mic-In		–84		
	Single-ended Line-In		–78		
Common Mode Rejection	–20dBv Input of 217Hz PGA in Differential Mode; 6dB Gain	-	–85	-	dB
Maximum Full Scale Input	Single-ended Input	-	-	0.5	Vrms
				–6	dBv
	Differential Input	-	-	1	Vrms
				0	dBv

Table 11: Internal Power Supplies

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input Supply Voltage	2.7	5.0	5.5	V	V5V_ANA and V5V_DIG.
Analog Output Supply Voltage	1.7	1.8	1.9	V	AVDD18.
CP 1 Output	1.14	1.35	1.5	V	DVDD12.
Digital Output 1.8V Supply Voltage	1.7	1.8	1.9	V	DVDD18.
Digital Output 3.3V Supply Voltage	2.5*	3.3	3.6	V	DVDD33.

Note: The minimum voltage below 3V tracks with the input 5V supply. If the input voltage is:

- > 3.5, then DVDD33 = 3.3V
- > 2.7 and < 3.5V, then DVDD33 = Input voltage –200mV
- < 2.7 and > 2.5V, then DVDD33 = 2.5V

Application Block Diagrams

Active Noise Canceling USB Headset

The CX21888 is designed to improve the quality and authenticity of audio experiences for music listening and phone conversations by reducing background ambient noise. The device provides multi-level control of ambient inclusion selection. The CX21888 provides a Super-Wide-band Acoustic Echo Canceller (SWB AEC), noise reduction (NR), and Smart Voice Pickup (SVP) to allow clear target speech pickup while rejecting unwanted noise on the road or in a noisy public venue or in a busy office environment.

The CX21888 supports up to four analog microphones (single-ended or differential). Benefits include:

- Low suspend mode current of 1.8 mA
- High power stereo headphone output of 31 mW at 32Ω load.
- Support for GPIOs to drive LEDs with built-in PWM capabilities
- USB bus power: Internal LDO regulators in the CX21888 allow single 3.3V or 5V to support all internal power supplies with minimal external passive components.

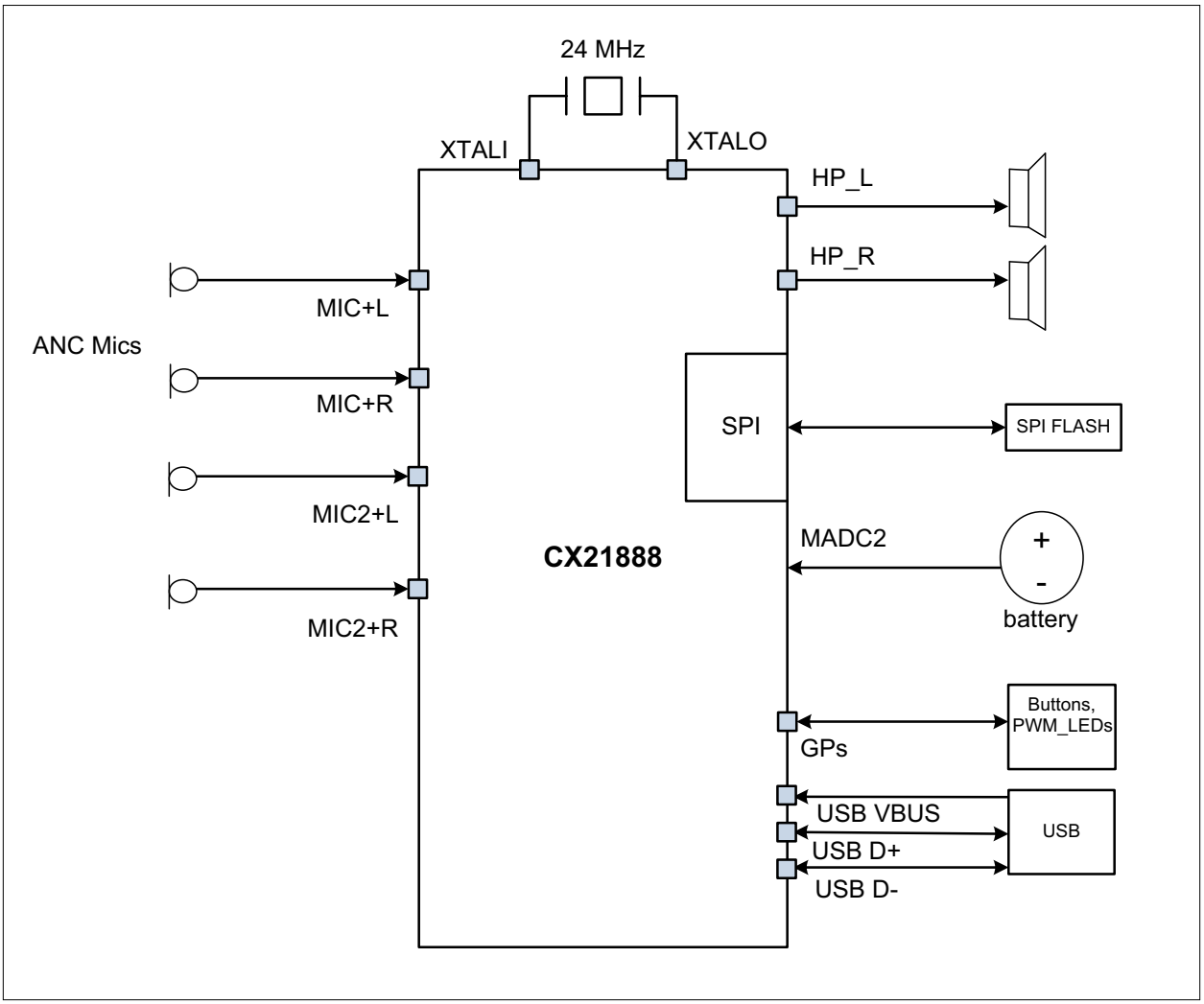


Figure 23: Active Noise Cancellation USB Headset

ANC Bluetooth Headset

The CX21888 is an extremely low-power device designed to extend battery life of Bluetooth headsets for wireless communications. It can be configured as either a PCM or I^2S device via the I^2C bus to work with a Bluetooth radio to deliver a high performance Bluetooth headset with advanced DSP features. These features include noise-reduction, echo-cancellation, and AGC to allow crystal clear phone calls in busy traffic or noisy outdoor environments. Built-in CX21888 LDOs enable Bluetooth headset designers to minimize BOM cost and reduce device power consumption.

The CX21888 offers powerful ACE, NR, and SVP to allow clear target speech pickup while rejecting unwanted babble interference on the road, in a noisy public venue or in a busy office environment. The CX21888 accepts an external reference clock of 24 MHz on the XTALI pin instead of an external XTAL.

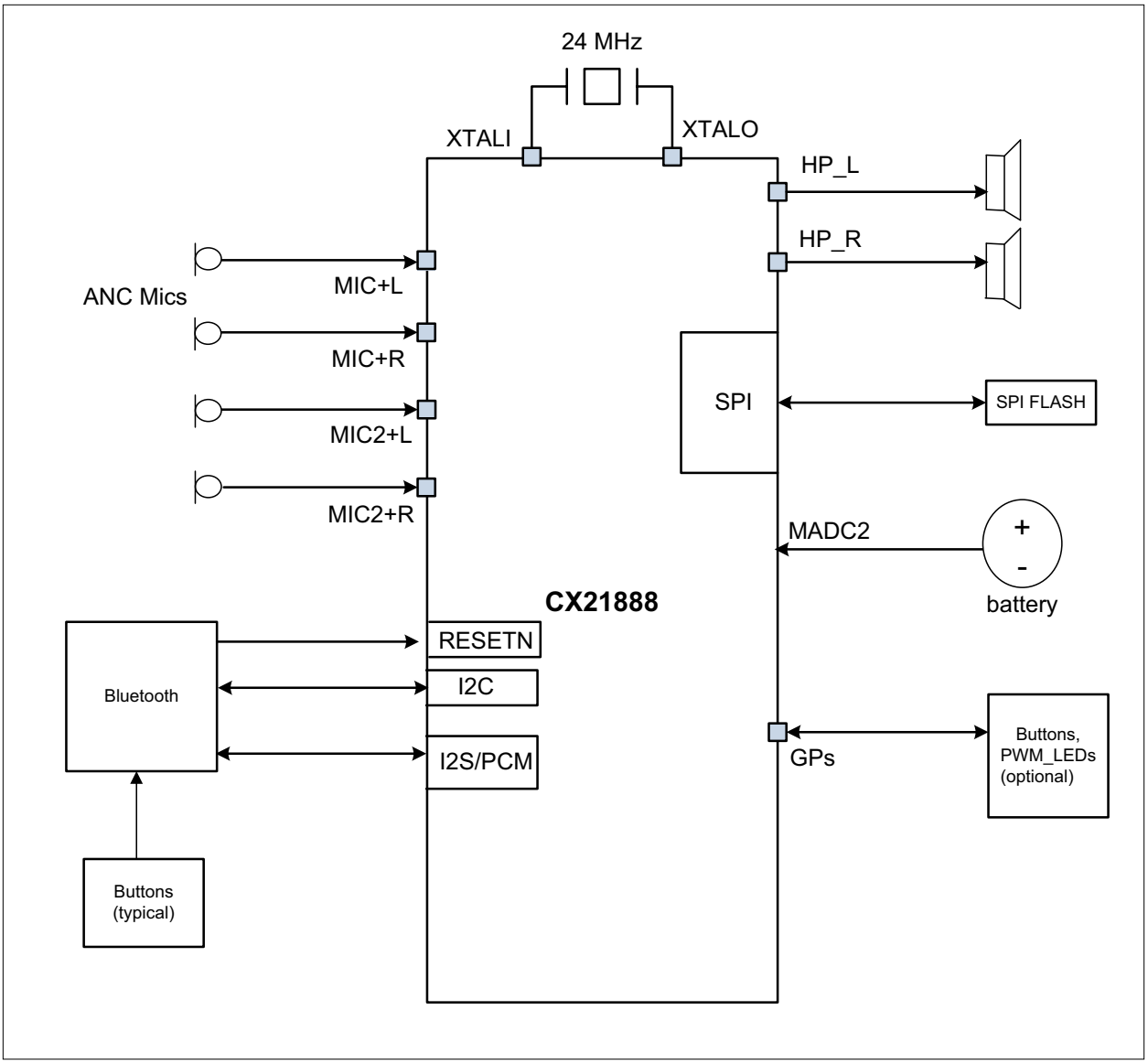


Figure 24: ANC Bluetooth Headset

ANC 3.5 mm Jack Headset

The CX21888 supports four analog microphones for ANC along with LINEIN signals for incoming voice calls for low latency applications. A battery voltage of up to 5.5V can be monitored with MADC2.

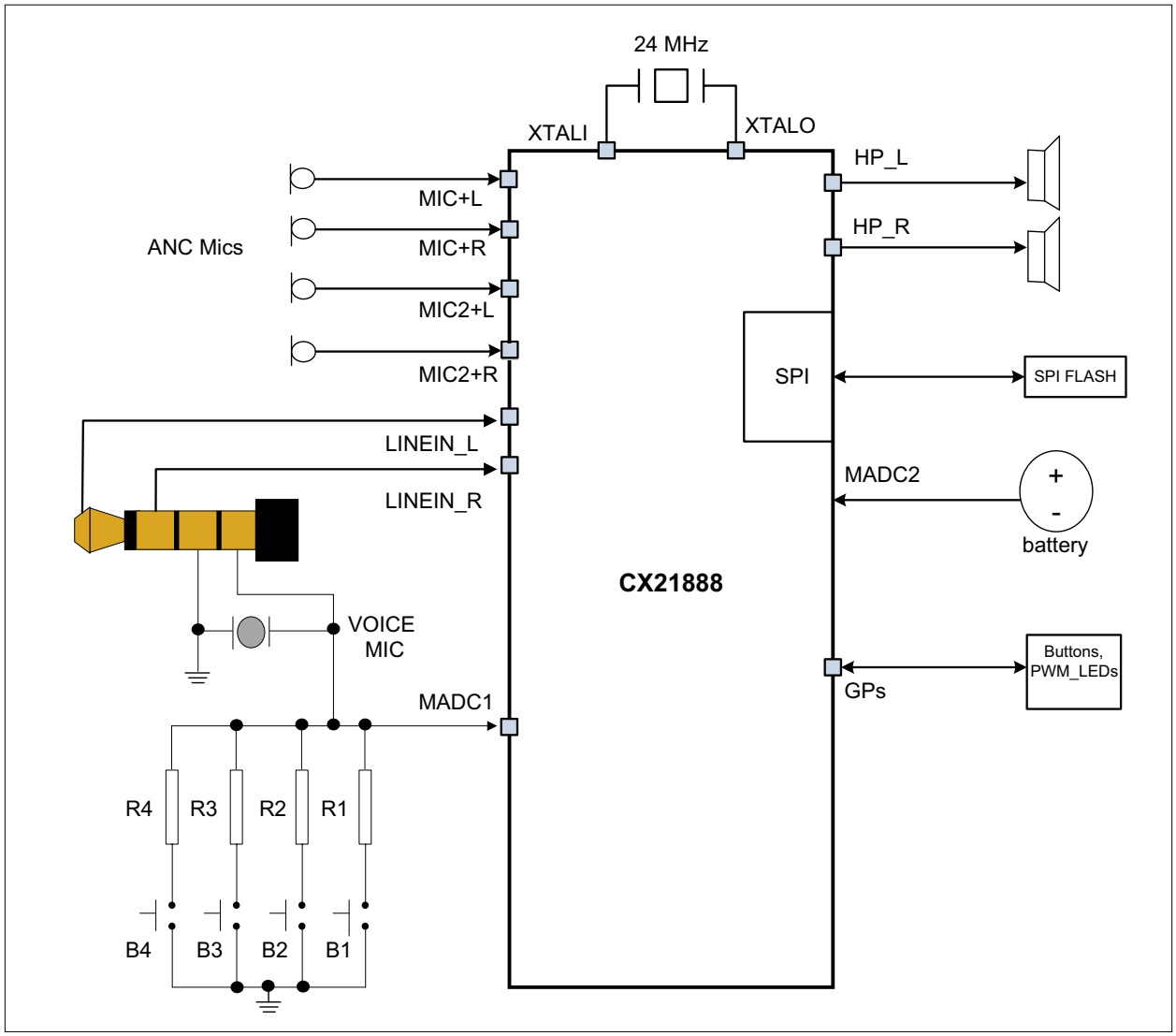
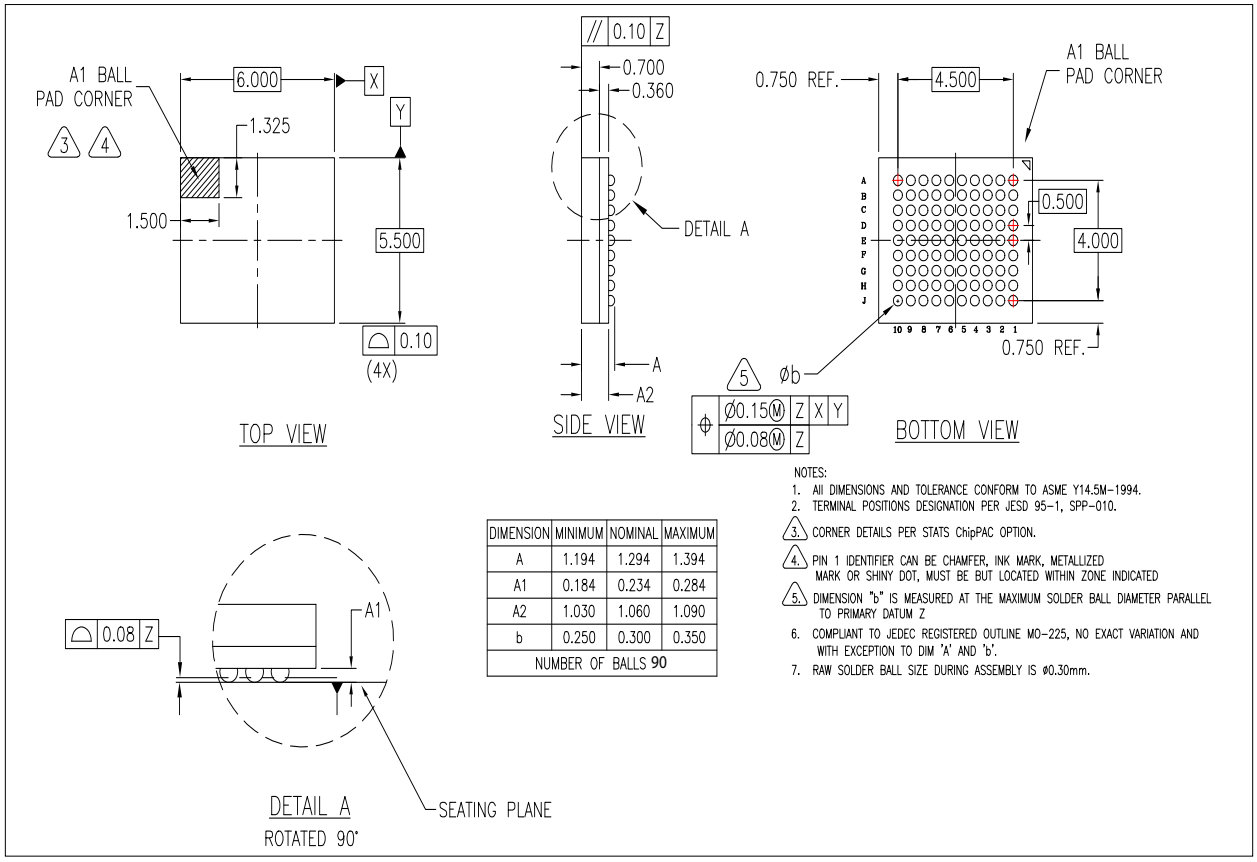


Figure 25: ANC 3.5 mm Jack Headset

Mechanical Information

Package Dimensions

Figure 26 shows the CX21888 package dimensions.



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.194	1.294	1.394
A1	0.184	0.234	0.284
A2	1.030	1.060	1.090
b	0.250	0.300	0.350
NUMBER OF BALLS 90			

Figure 26: CX21888 Package Dimensions

PCB Footprint

Figure 27 shows the recommended PCB layout footprint for the CX21888.

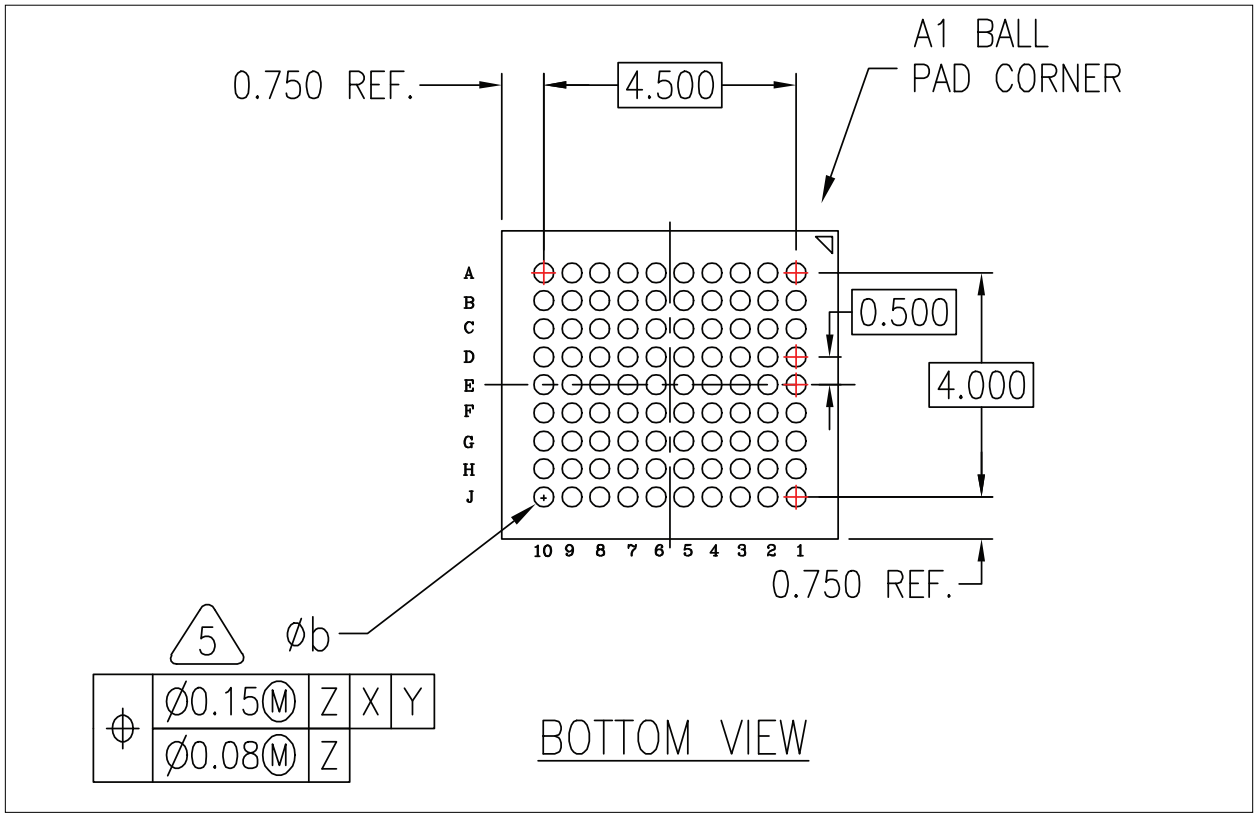


Figure 27: CX21888 Recommended PCB Footprint

Ordering Information

Ordering Part Number	Part Number	Description	Package
DSAC-L888-10CH	CX21888-10Z	Low-Power USB Type-C DSP CODEC with Adaptive Hybrid Active Noise Cancellation.	6.0 mm x 5.5 mm 90L BGA

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