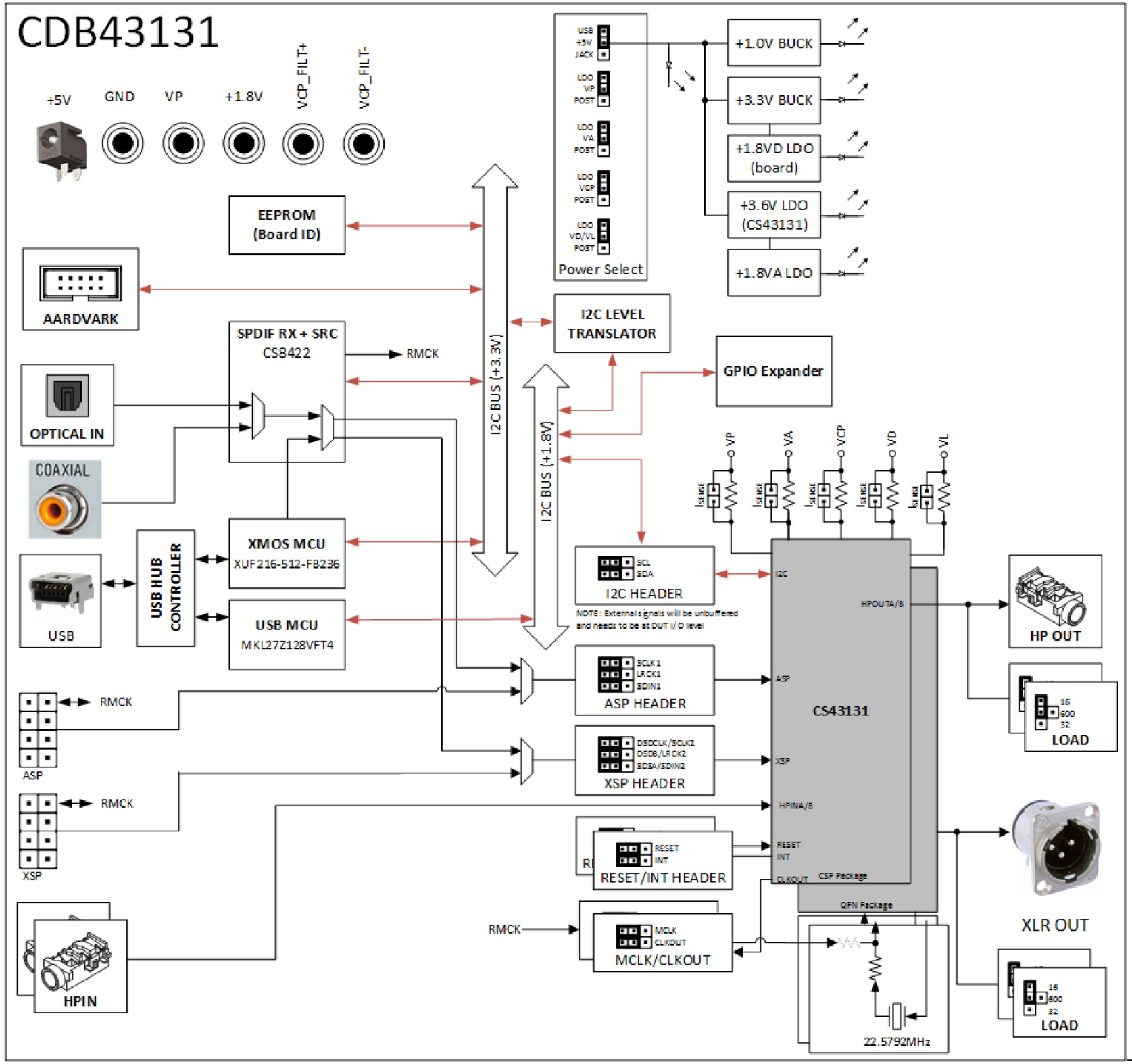
CDB43131



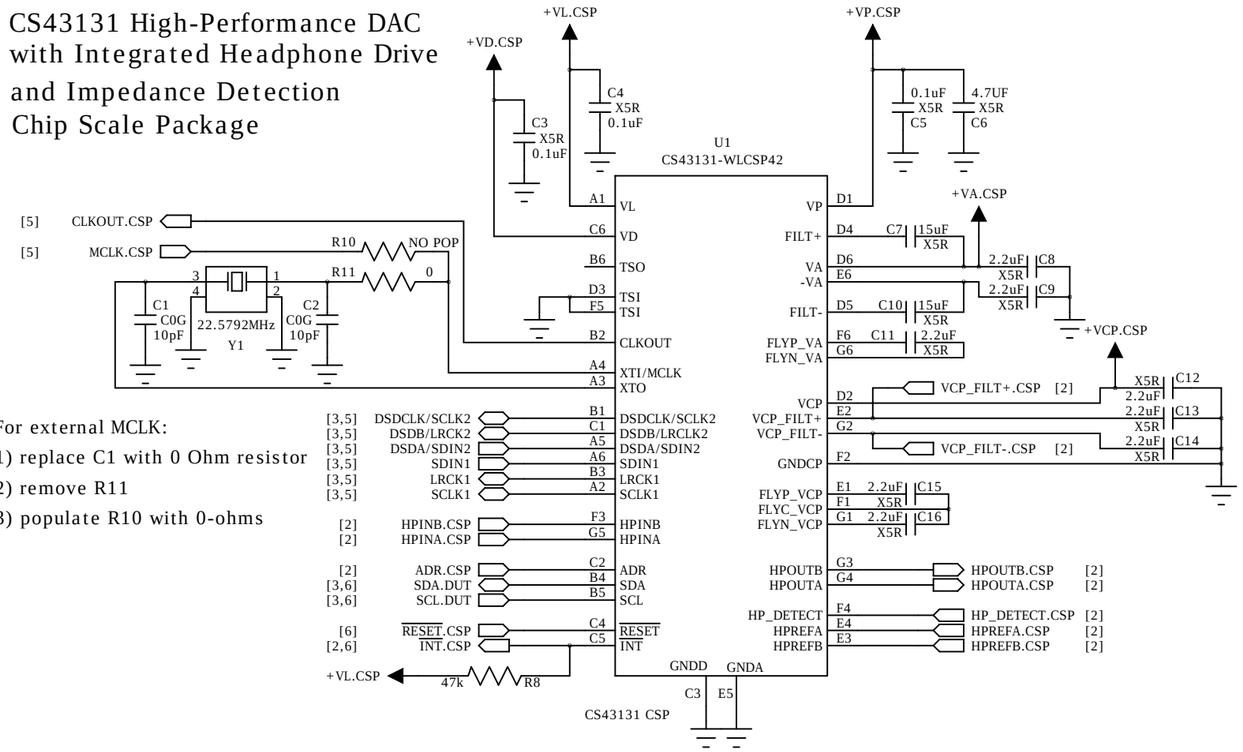
REV	DESCRIPTION	DATE
A0	INITIAL RELEASE	11/10/2017
B0	DEBOUNCE RESET ADDED	03/09/2018
B1	ADDED SCREW	03/29/2018

PCB DWG- 240-10301/B0
LBL SUBASSY PROD ID AND REV

CIRRUS LOGIC

SHEET TITLE	BLOCK-DIAGRAM		
PART #	CDB43131	Rev B1	
DRAWN BY	M. KUREK	ENGINEER M. KUREK	
DATE	7/10/2018	SHEET 1 OF 12	SHEET SIZE B

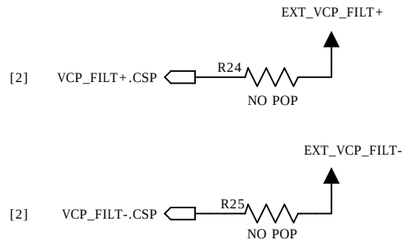
CS43131 High-Performance DAC with Integrated Headphone Drive and Impedance Detection Chip Scale Package



For external MCLK:

1) replace C1 with 0 Ohm resistor
2) remove R11
3) populate R10 with 0-ohms

External Amplifier Power

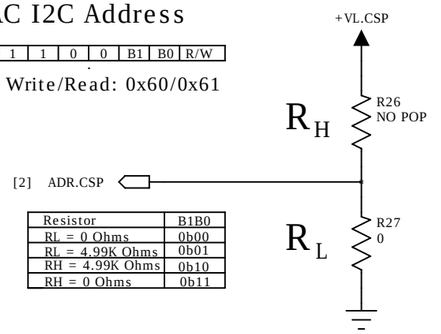


populate R24 and R25 with 0-ohms for external VCP_FILT +/- supplies

DAC I2C Address

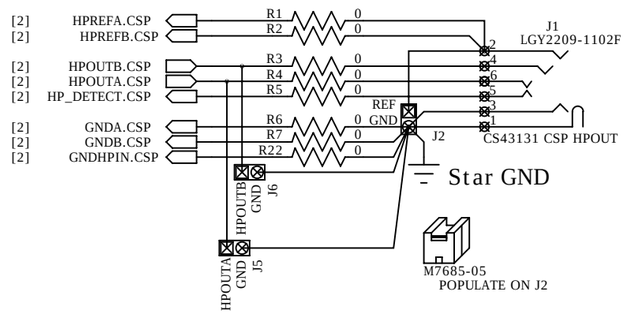
0	1	1	0	0	B1	B0	R/W

I2C Write/Read: 0x60/0x61

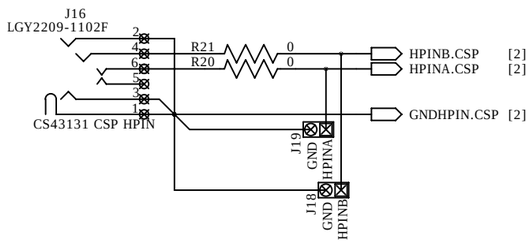


Resistor	B1B0
RL = 0 Ohms	0b00
RL = 4.99K Ohms	0b01
RH = 4.99K Ohms	0b10
RH = 0 Ohms	0b11

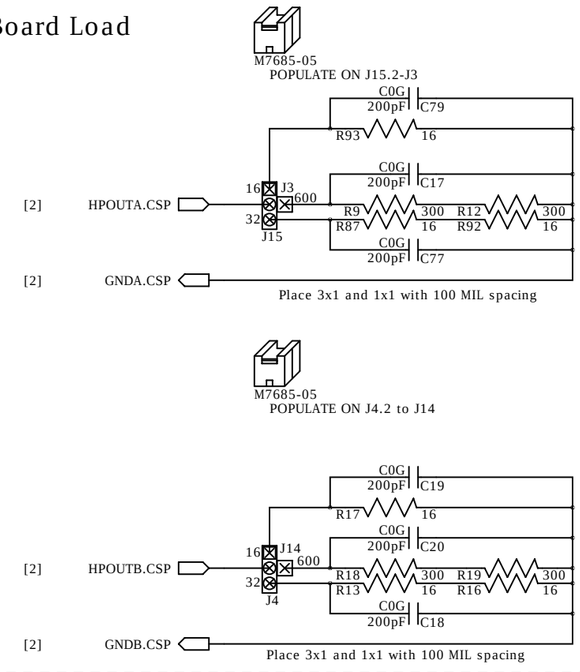
3.5mm Headset Jack



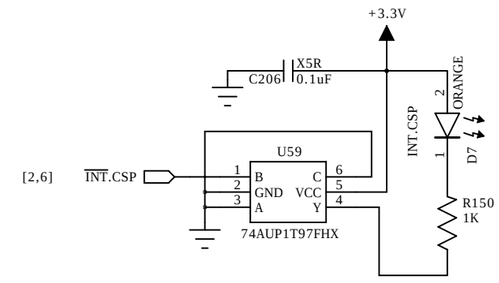
3.5mm Headphone Input Jack



On-Board Load



Interrupt LED

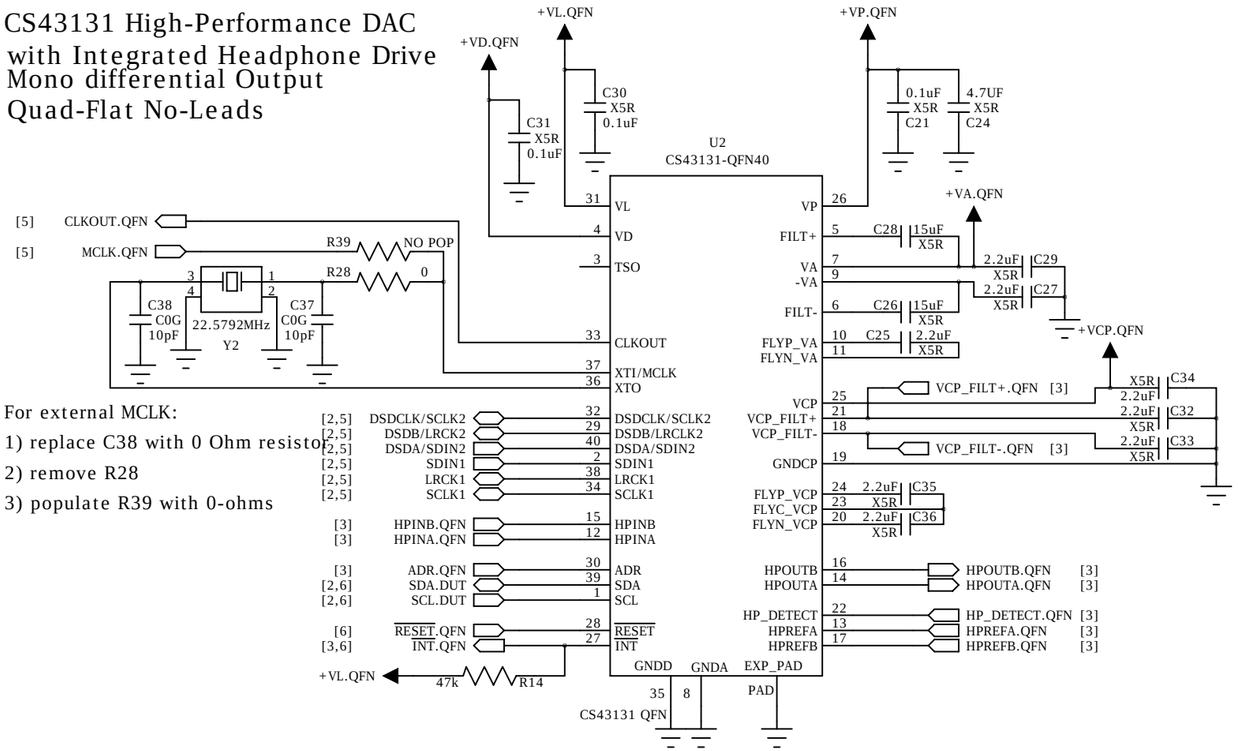


LED illuminated when $\overline{\text{INT}}$.CSP=0

CIRRUS LOGIC

SHEET TITLE	CS43131-CSP		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK	ENGINEER M. KUREK		
DATE 7/10/2018	SHEET 2 OF 12	SHEET SIZE B	

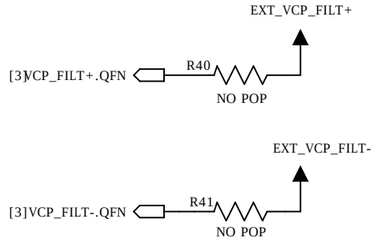
CS43131 High-Performance DAC with Integrated Headphone Drive Mono differential Output Quad-Flat No-Leads



For external MCLK:

1) replace C38 with 0 Ohm resistor
2) remove R28
3) populate R39 with 0-ohms

External Amplifier Power

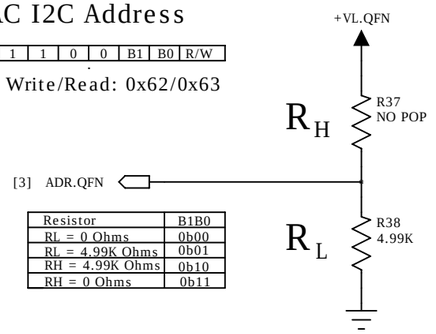


populate R40 and R41 with 0-ohms for external VCP_FILT +/- supplies

DAC I2C Address

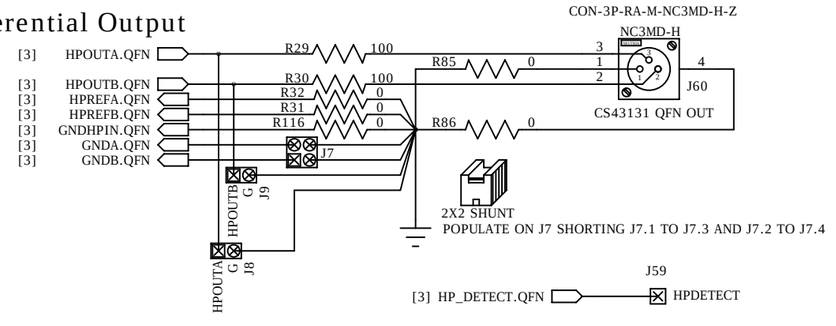
0	1	1	0	0	B1	B0	R/W

I2C Write/Read: 0x62/0x63

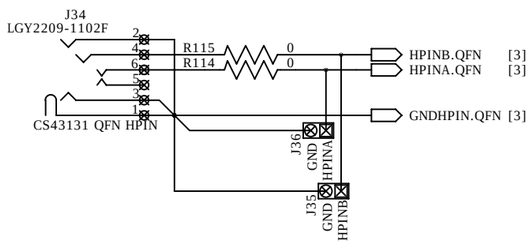


Resistor	B1B0
RL = 0 Ohms	0b00
RL = 4.99K Ohms	0b01
RH = 4.99K Ohms	0b10
RH = 0 Ohms	0b11

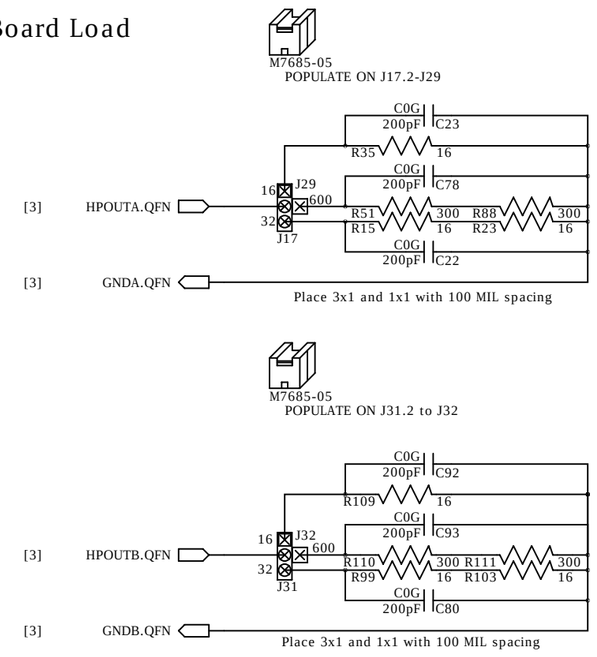
XLR Differential Output



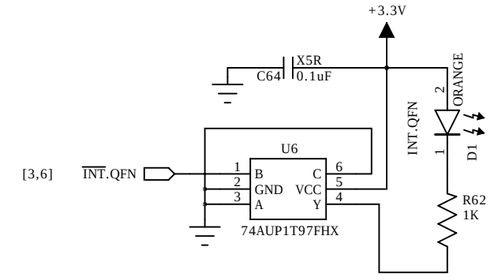
3.5mm Headphone Input Jack



On-Board Load



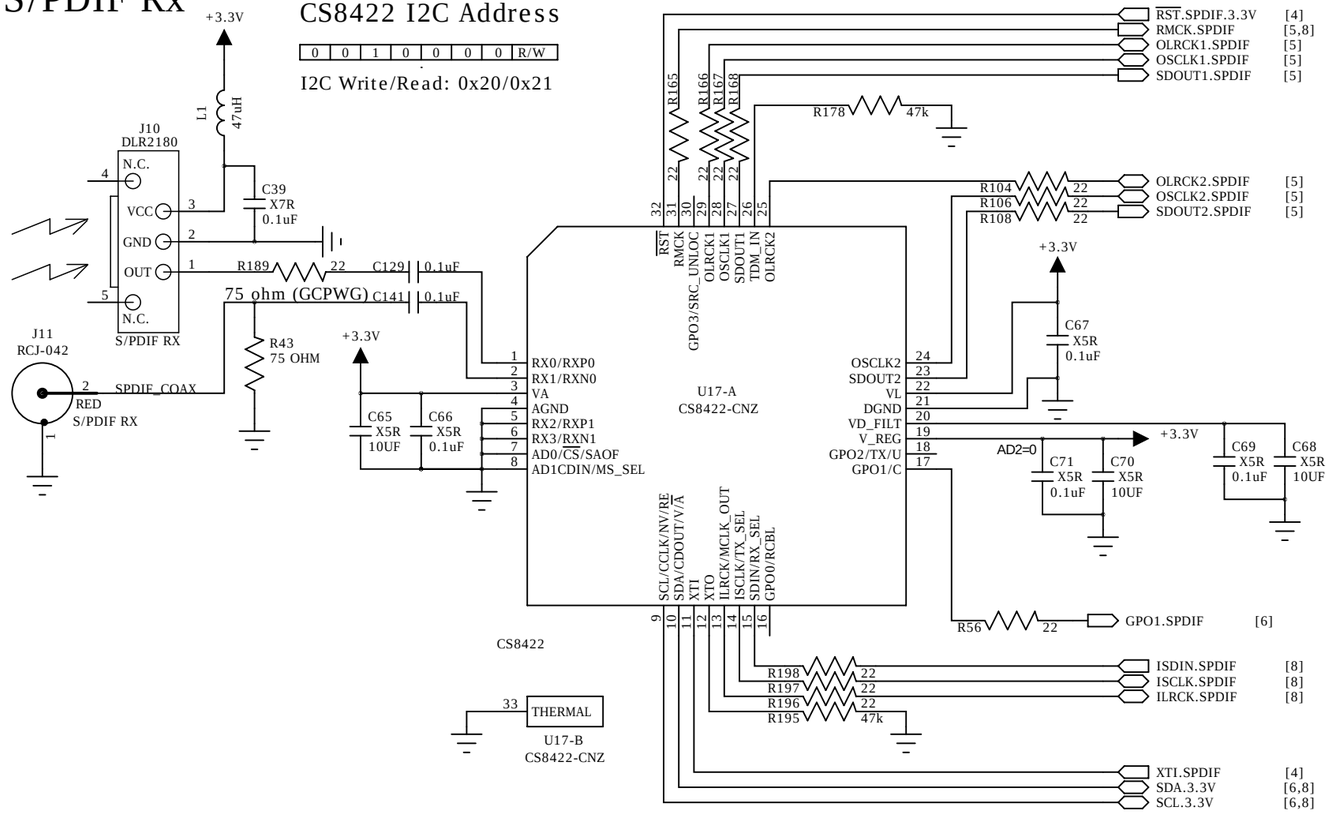
Interrupt LED



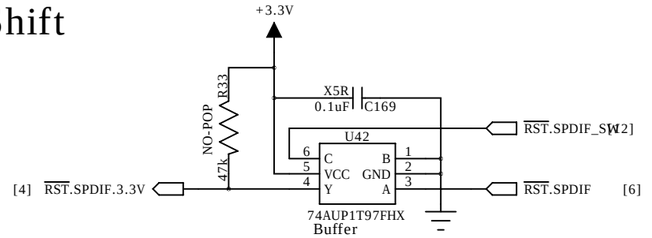
LED illuminated when $\overline{\text{INT}}$.QFN=0

CIRRUS LOGIC	
SHEET TITLE	CS43131-QFN
PART #	CDB43131 Rev B1
DRAWN BY	M. KUREK
ENGINEER	M. KUREK
DATE	7/10/2018
SHEET	3 OF 12
SHEET SIZE	B

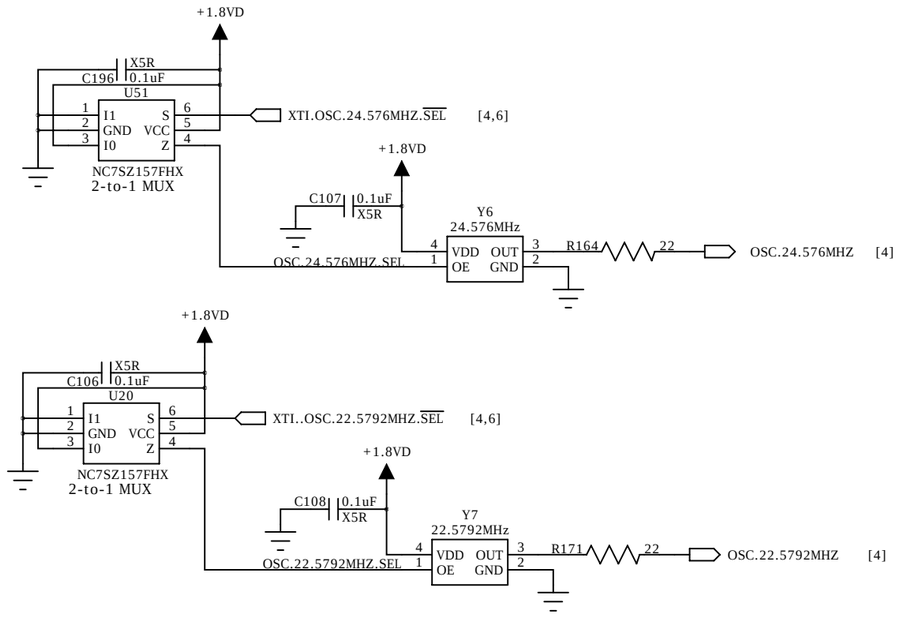
S/PDIF Rx



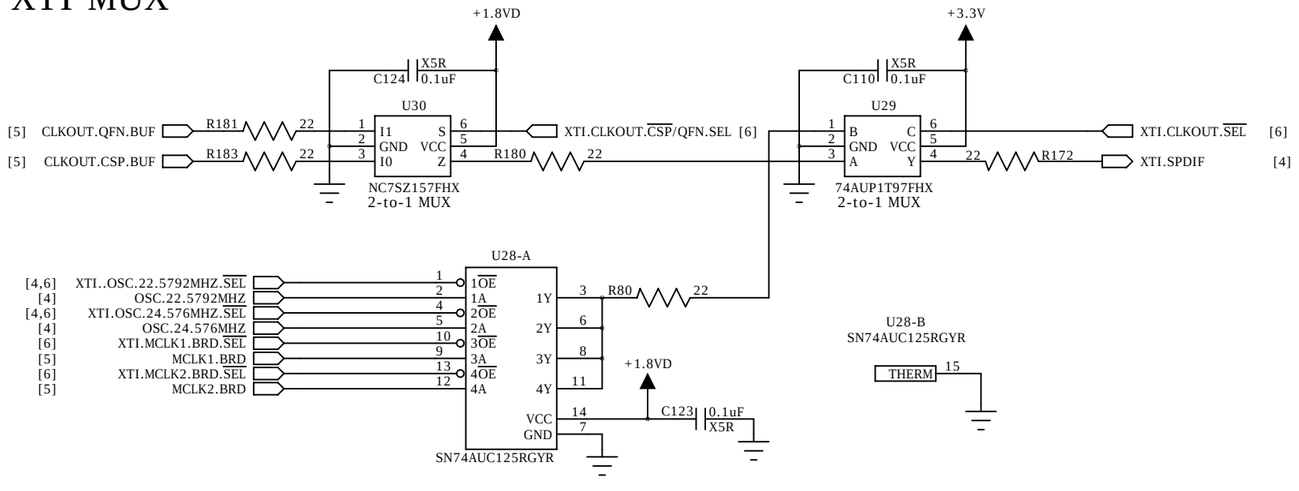
Level Shift



OSCILLATORS - only enable when using



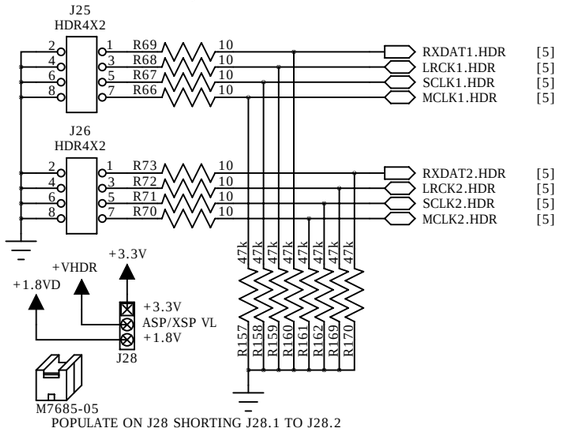
XTI MUX



CIRRUS LOGIC

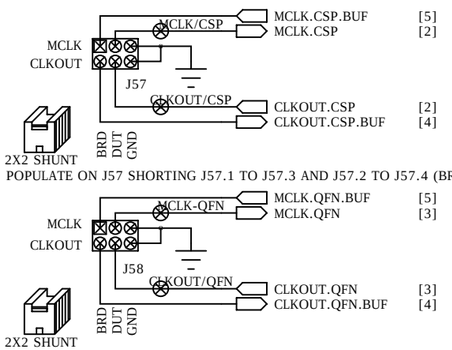
SHEET TITLE	S/PDIF-RX		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK		ENGINEER M. KUREK	
DATE 7/10/2018	SHEET 4 OF 12	SHEET SIZE B	

PCM, DOP, & DSD headers



POPULATE ON J28 SHORTING J28.1 TO J28.2

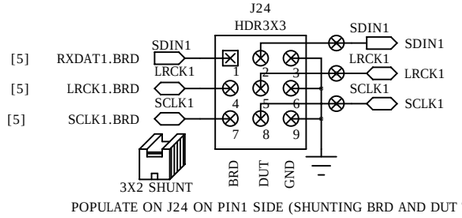
MCLK & CLKOUT direct header



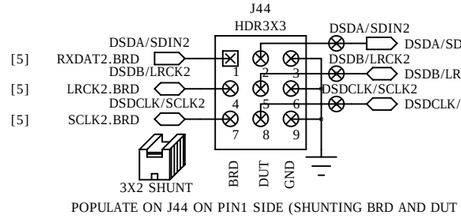
POPULATE ON J57 SHORTING J57.1 TO J57.3 AND J57.2 TO J57.4 (BRD TO DUT)

POPULATE ON J58 SHORTING J58.1 TO J58.3 AND J58.2 TO J58.4 (BRD TO DUT)

ASP & XSP direct header

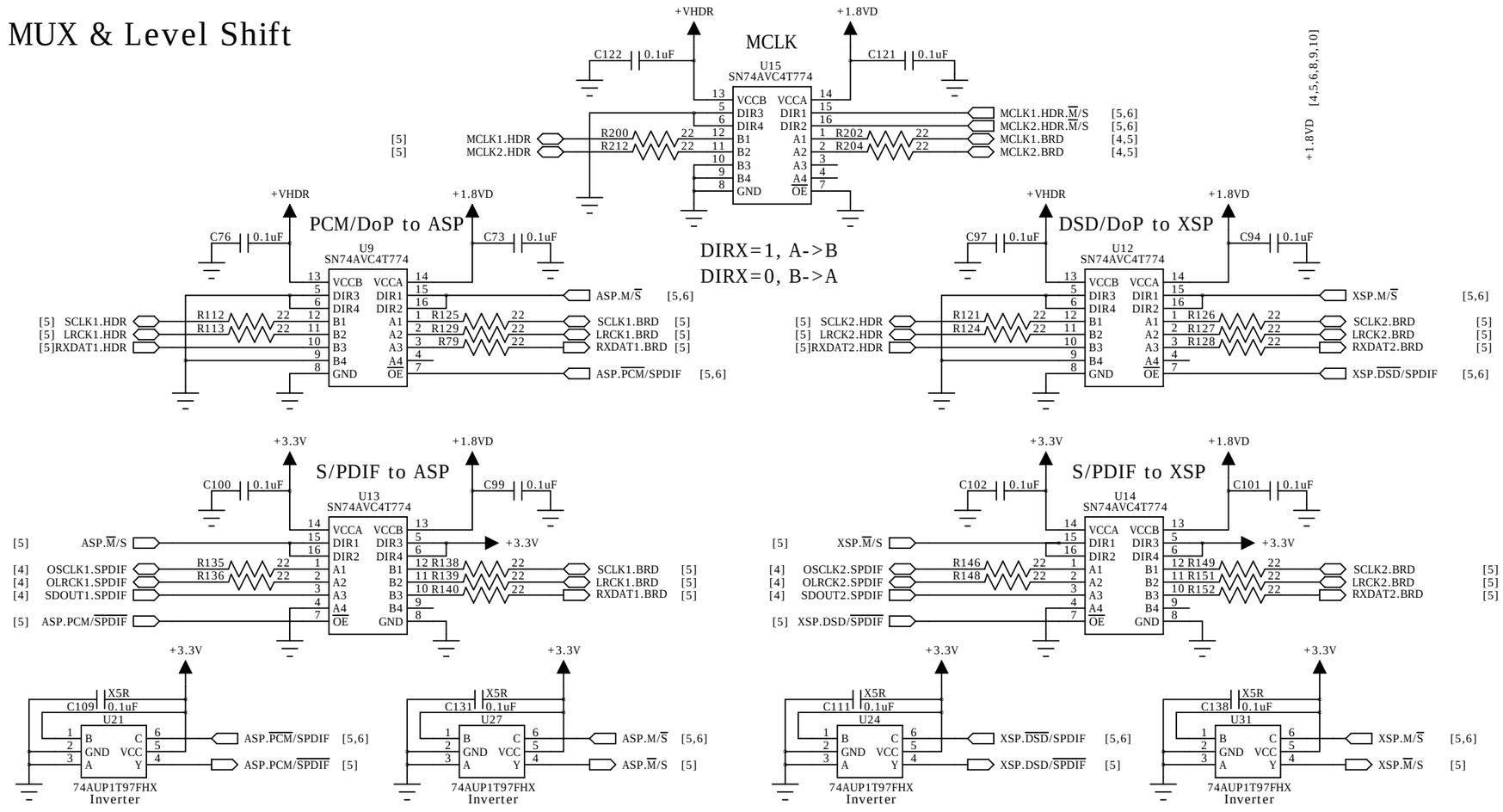


POPULATE ON J24 ON PIN1 SIDE (SHUNTING BRD AND DUT TOGETHER)

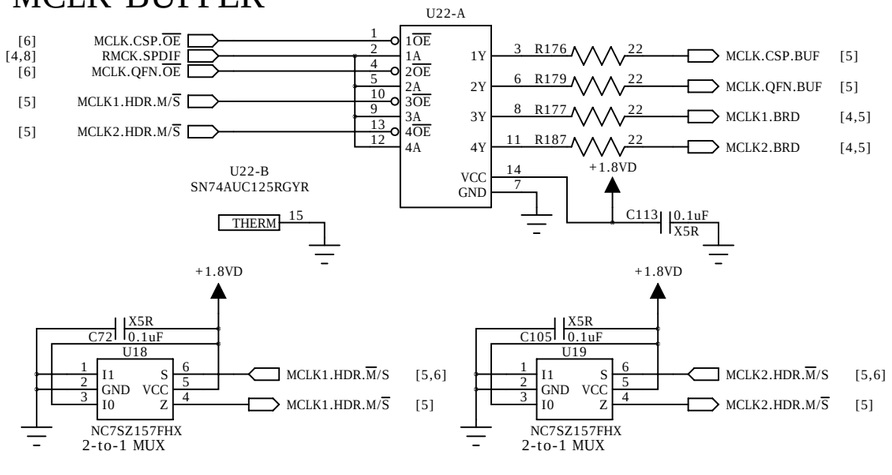


POPULATE ON J44 ON PIN1 SIDE (SHUNTING BRD AND DUT TOGETHER)

MUX & Level Shift

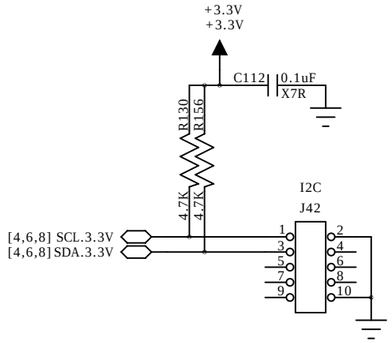


MCLK BUFFER

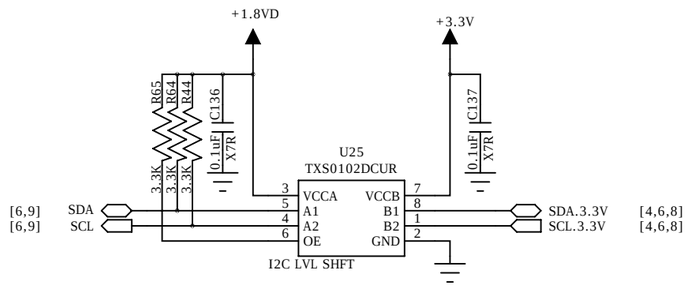


CIRRUS LOGIC			
SHEET TITLE	PCM-DSD-DOP		
PART #	CDB43131		Rev B1
DRAWN BY	M. KUREK	ENGINEER	M. KUREK
DATE	7/10/2018	SHEET 5 OF 12	SHEET SIZE B

Aardvark header



I2C level shifter

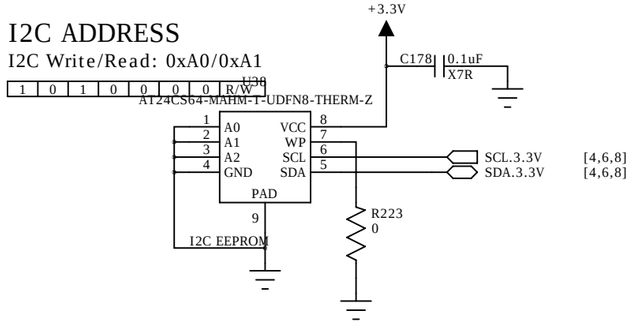


Device ID EEPROM with Unique S/N

I2C ADDRESS

I2C Write/Read: 0xA0/0xA1

1	0	1	0	0	0	0	R/W

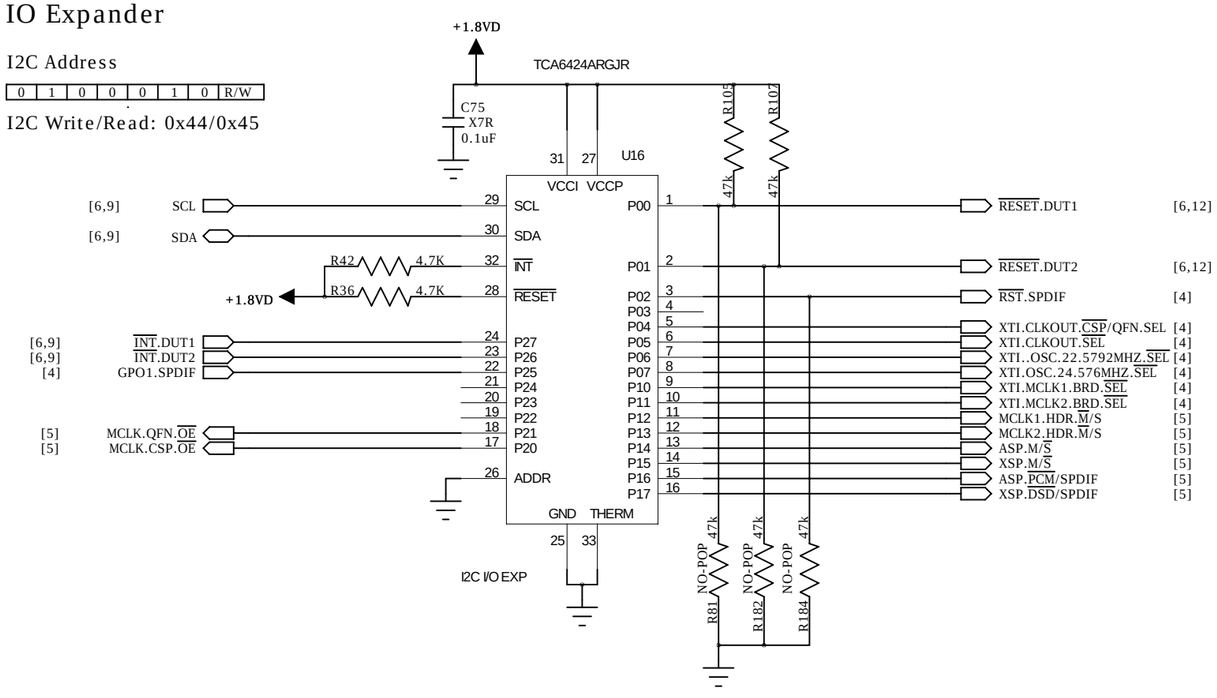


IO Expander

I2C Address

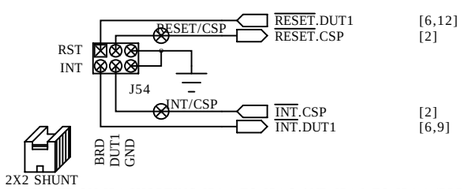
0	1	0	0	0	1	0	R/W

I2C Write/Read: 0x44/0x45



RST and INT HEADER

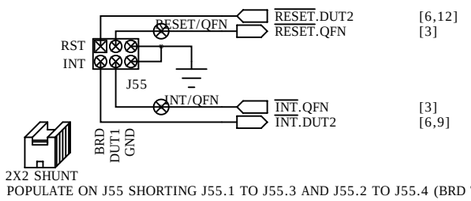
NOTE: External RST and INT will be unbuffered and needs to be at DUT I/O level



POPULATE ON J54 SHORTING J54.1 TO J54.3 AND J54.2 TO J54.4 (BRD TO DUT).

RST and INT HEADER

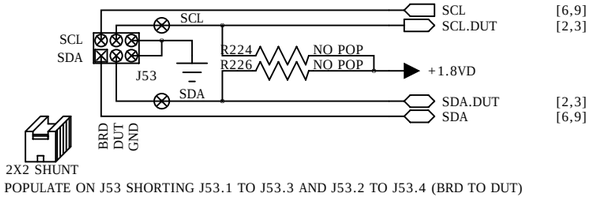
NOTE: External RST and INT will be unbuffered and needs to be at DUT I/O level



POPULATE ON J55 SHORTING J55.1 TO J55.3 AND J55.2 TO J55.4 (BRD TO DUT)

I2C HEADER

NOTE: External I2C will be unbuffered and needs to be at DUT I/O level

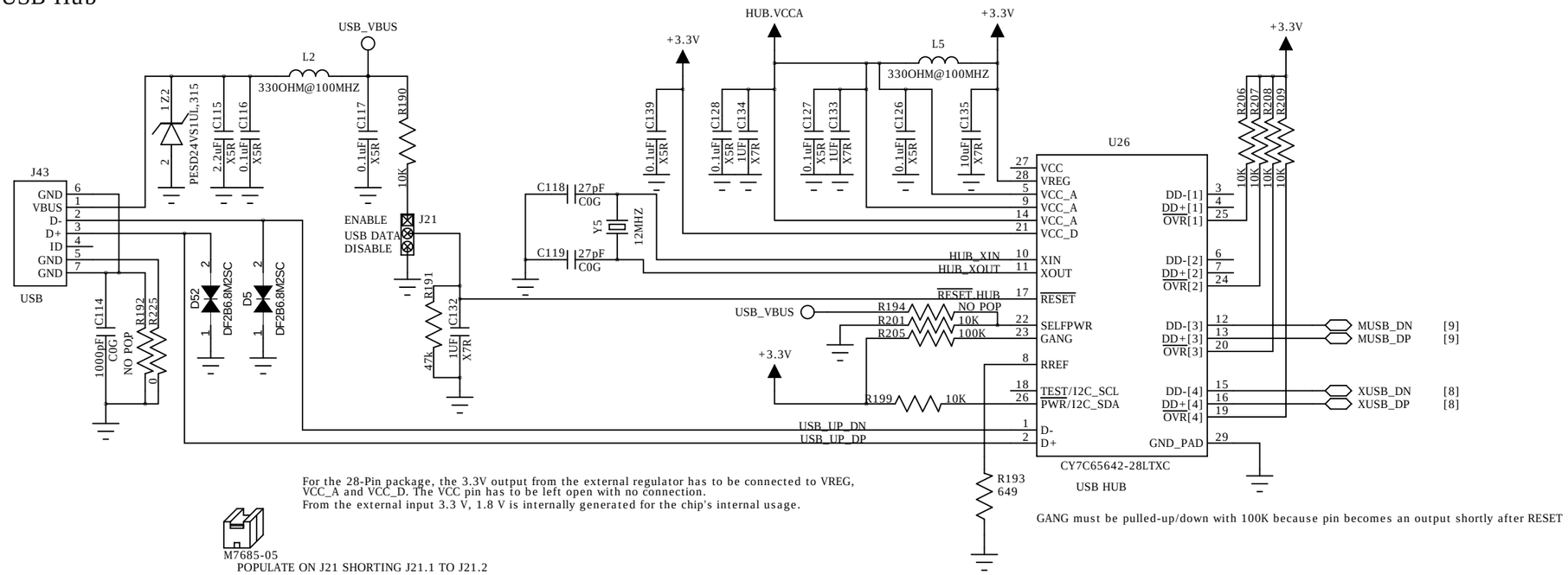


POPULATE ON J53 SHORTING J53.1 TO J53.3 AND J53.2 TO J53.4 (BRD TO DUT)

CIRRUS LOGIC

SHEET TITLE	I2C-GPIO-EXP		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK		ENGINEER M. KUREK	
DATE 7/10/2018	SHEET 6 OF 12		SHEET SIZE B

USB Hub



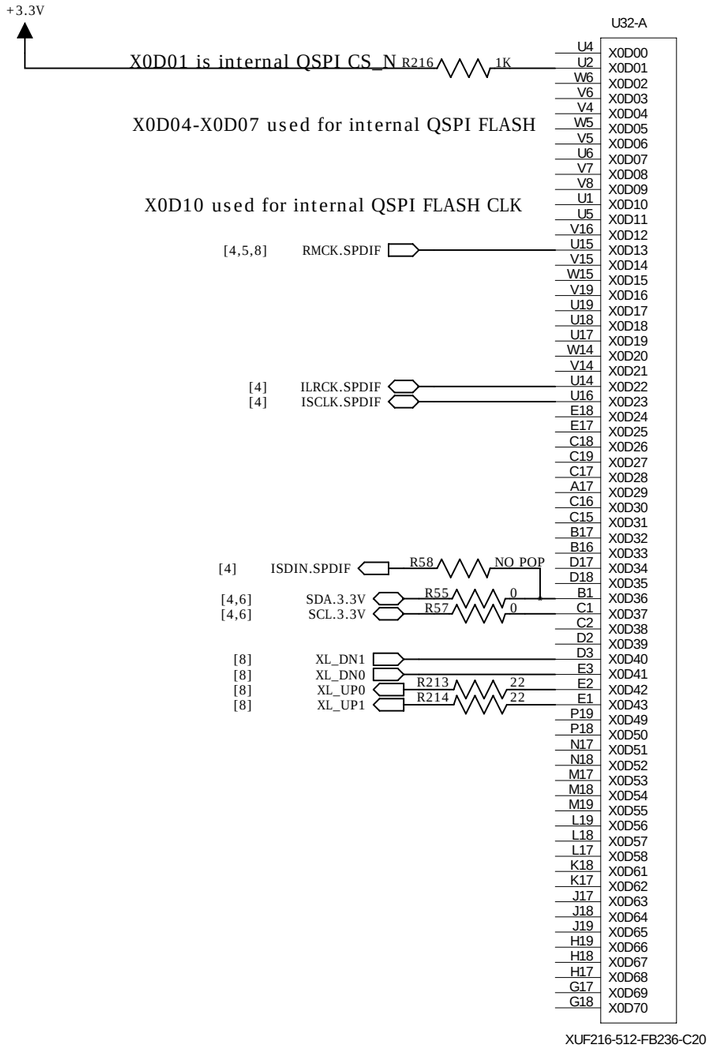
For the 28-Pin package, the 3.3V output from the external regulator has to be connected to VREG, VCC_A and VCC_D. The VCC pin has to be left open with no connection.
From the external input 3.3 V, 1.8 V is internally generated for the chip's internal usage.

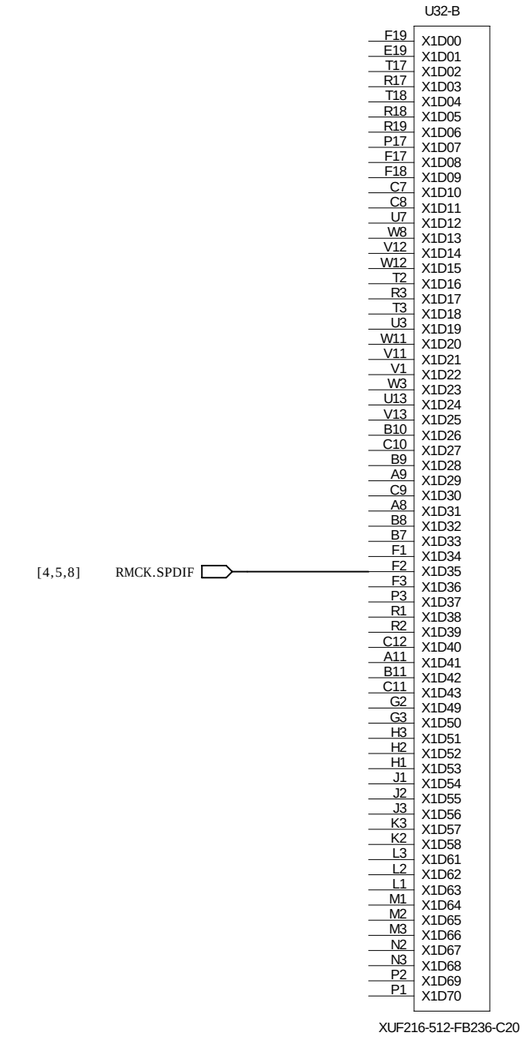
GANG must be pulled-up/down with 100K because pin becomes an output shortly after RESET

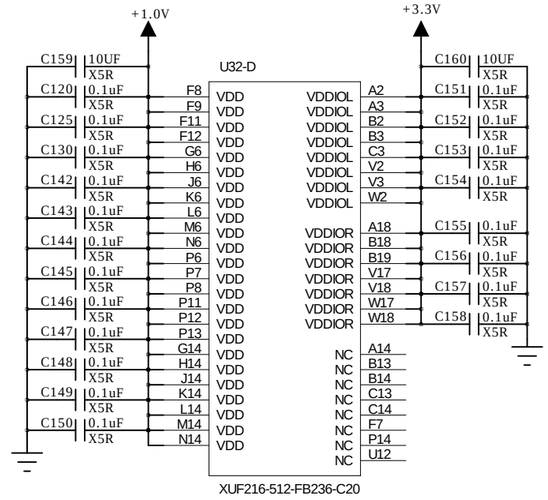
M7685-05
POPULATE ON J21 SHORTING J21.1 TO J21.2

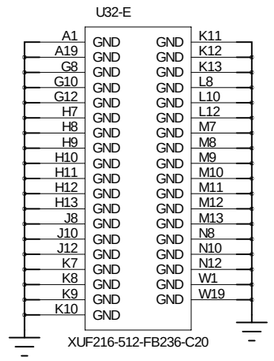
CIRRUS LOGIC

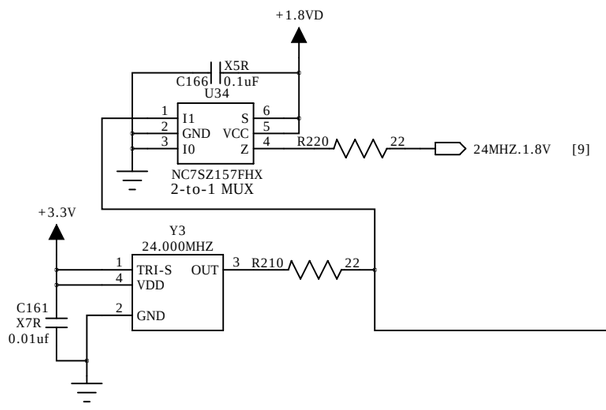
SHEET TITLE	USB-HUB		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK	ENGINEER M. KUREK		
DATE 7/10/2018	SHEET 7 OF 12	SHEET SIZE B	

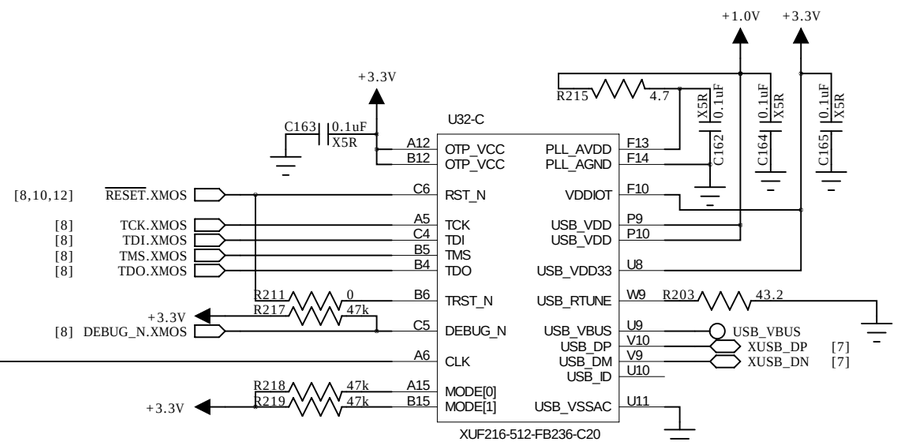


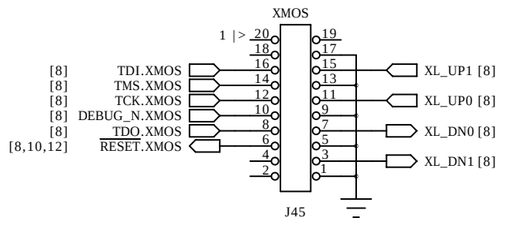








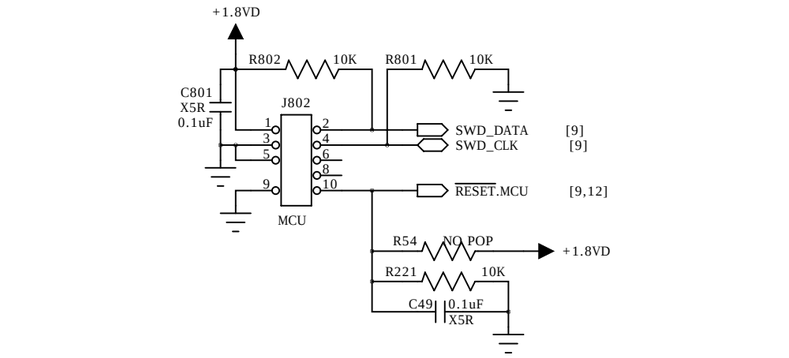


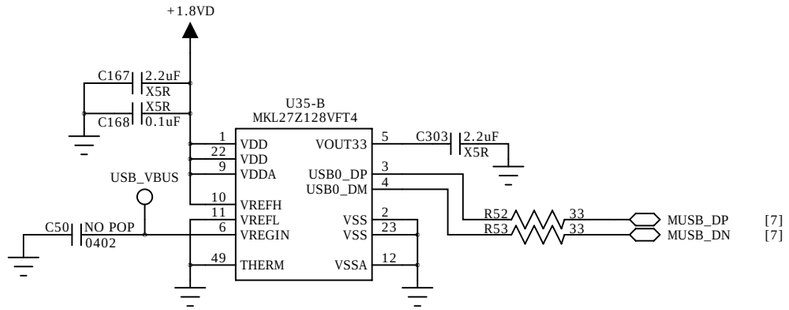


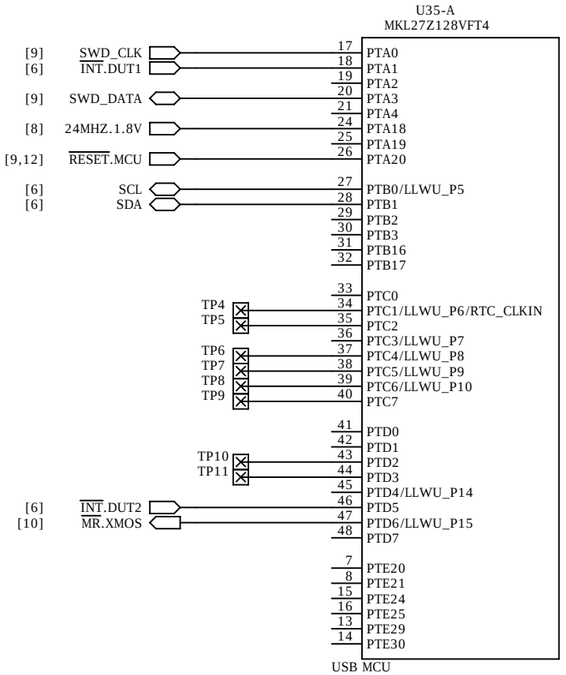
CIRRUS LOGIC

SHEET TITLE	USB-AUDIO		
PART #	CDB43131	Rev B1	
DRAWN BY	M. KUREK	ENGINEER M. KUREK	
DATE	7/10/2018	SHEET 8 OF 12	SHEET SIZE B

USB MCU



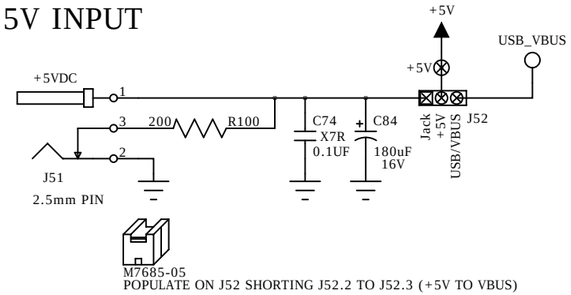




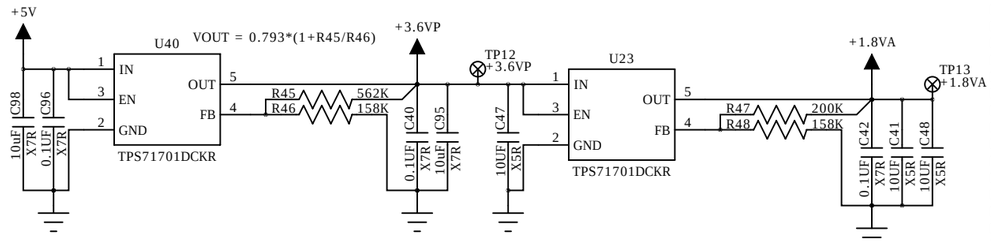
CIRRUS LOGIC

SHEET TITLE	USB-CONTROL		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK		ENGINEER M. KUREK	
DATE 7/10/2018		SHEET 9 OF 12	SHEET SIZE B

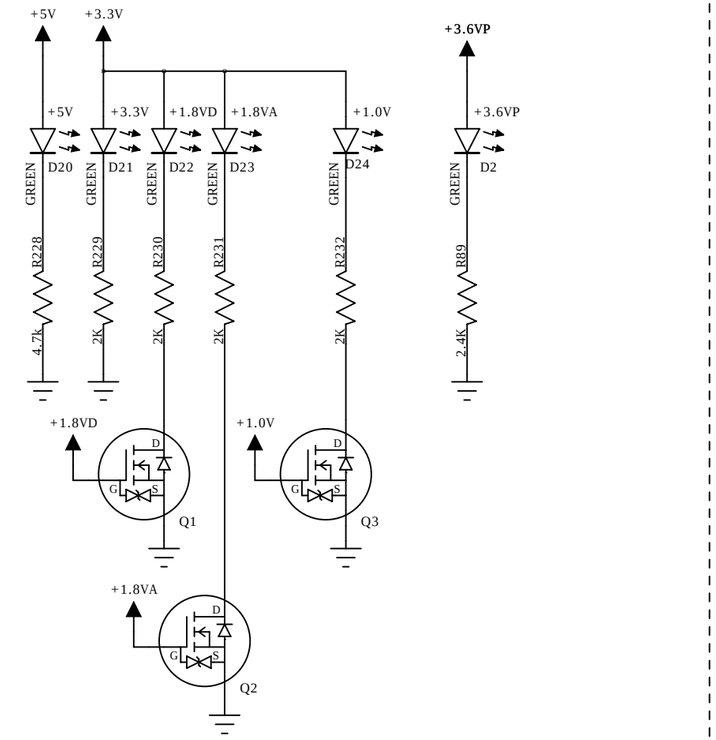
5V INPUT



CS43131 3.6V and 1.8V LDO

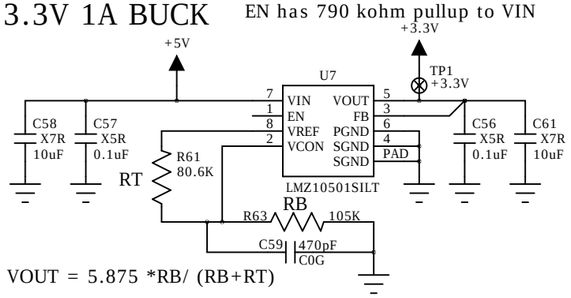


POWER INDICATORS



3.3V 1A BUCK

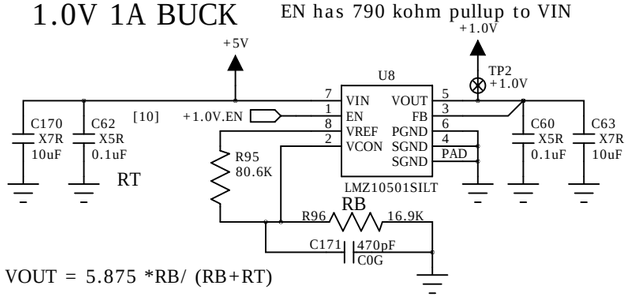
EN has 790 kohm pullup to VIN



VOUT = 5.875 *RB/ (RB+RT)

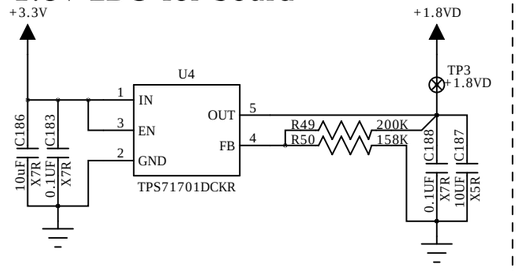
1.0V 1A BUCK

EN has 790 kohm pullup to VIN



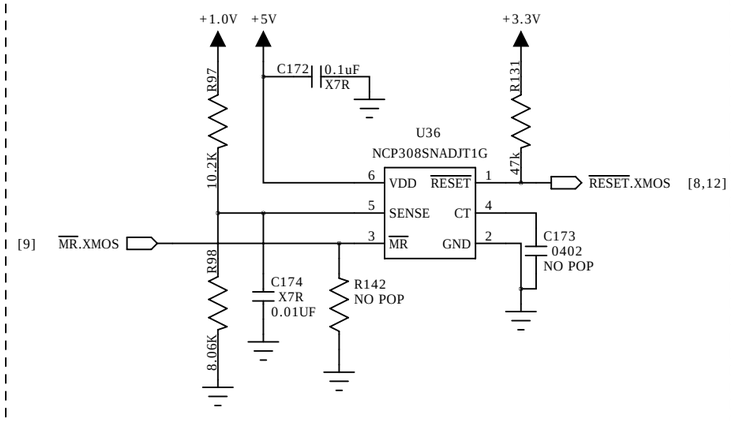
VOUT = 5.875 *RB/ (RB+RT)

1.8V LDO for board



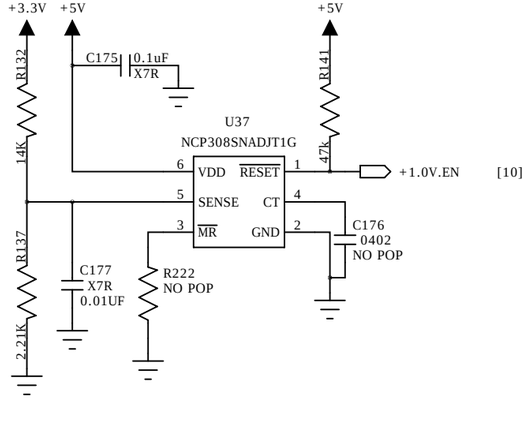
Programmable Delay Reset

$\overline{\text{RESET}}$ output valid at VDD of 0.8V (worst case)
$\overline{\text{RESET}}$ release delay = 20 ms
SENSE threshold (neg) = (10.2K/8.06K+1) x 0.405V = 0.9175V
SENSE threshold (pos, typ) = 0.9175V x 1.0175 = 0.9336V
SENSE threshold (pos, max) = 0.9175V x 1.0375 = 0.9519V
$\overline{\text{MR}}$ V_IL (max) = 0.3xVDD = 1.5V
$\overline{\text{MR}}$ V_IH (min) = 0.7xVDD = 3.5V
$\overline{\text{MR}}$ internal pull-up resistance = 90kOhms typ



Programmable Delay Reset

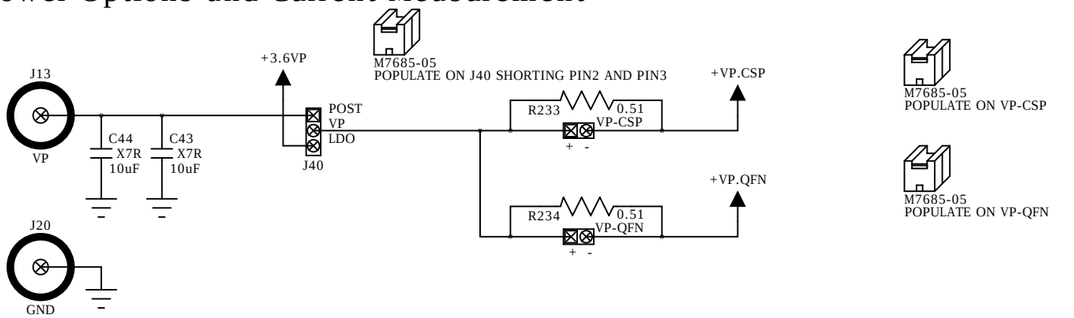
$\overline{\text{RESET}}$ output valid at VDD of 0.8V (worst case)
$\overline{\text{RESET}}$ release delay = 20 ms
SENSE threshold (neg) = (14K/2.21K+1) x 0.405V = 2.97V
SENSE threshold (pos, typ) = 2.97V x 1.0175 = 3.022V
SENSE threshold (pos, max) = 2.97V x 1.0375 = 3.135V
$\overline{\text{MR}}$ V_IL (max) = 0.3xVDD = 1.5V
$\overline{\text{MR}}$ V_IH (min) = 0.7xVDD = 3.5V
$\overline{\text{MR}}$ internal pull-up resistance = 90kOhms typ

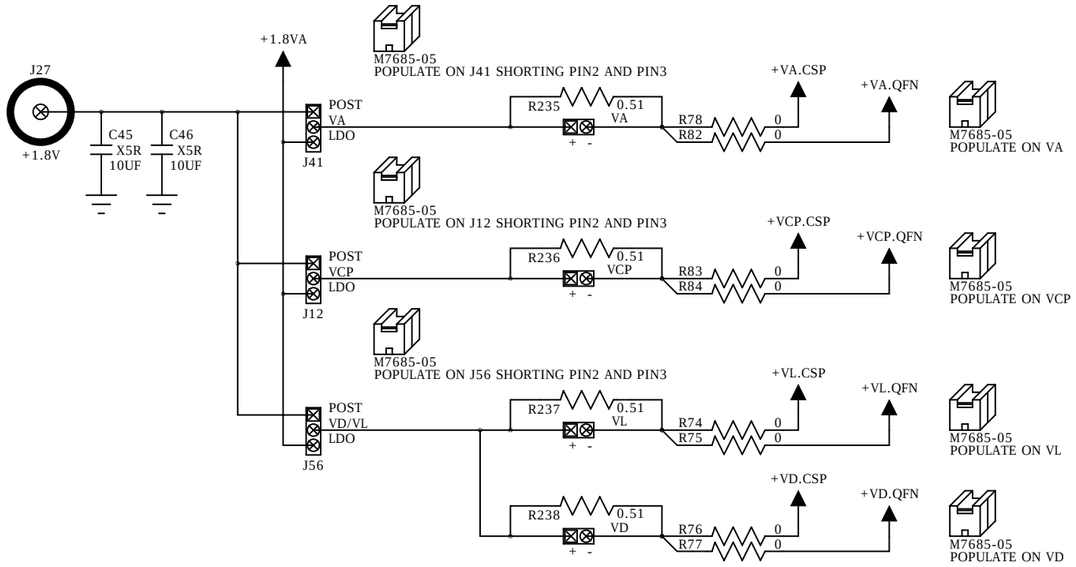


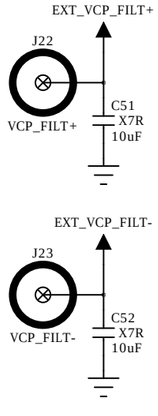
CIRRUS LOGIC

SHEET TITLE	POWER		
PART #	CDB43131		Rev B1
DRAWN BY	M. KUREK	ENGINEER	M. KUREK
DATE	7/10/2018	SHEET 10 OF 12	SHEET SIZE B

Power Options and Current Measurement



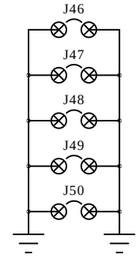




Hardware

MH1	MH5	SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
MH2	MH6	SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
MH3	MH7	SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
MH4	MH8	SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
		SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
		SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
		SCREW-PHILIPS-4-40THR-PH-5/16-L-Z	PMSSS 440 0031 PH
		SCREW-4-40THR-SS-1/4L	90190A106

Testpoints

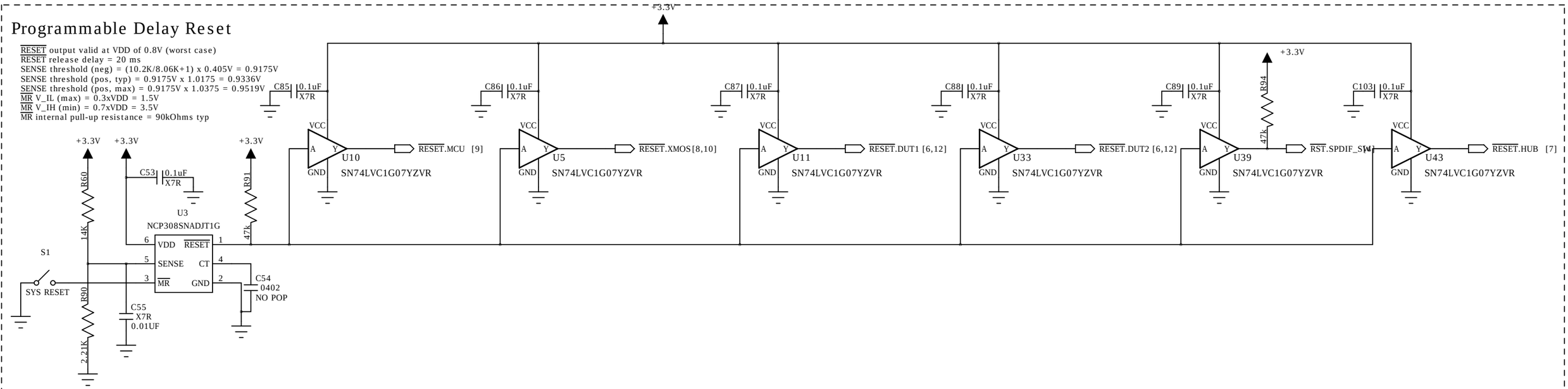


CIRRUS LOGIC

SHEET TITLE	EXT-POWER		
PART #	CDB43131	Rev B1	
DRAWN BY M. KUREK		ENGINEER M. KUREK	
DATE 7/10/2018	SHEET 11 OF 12	SHEET SIZE B	

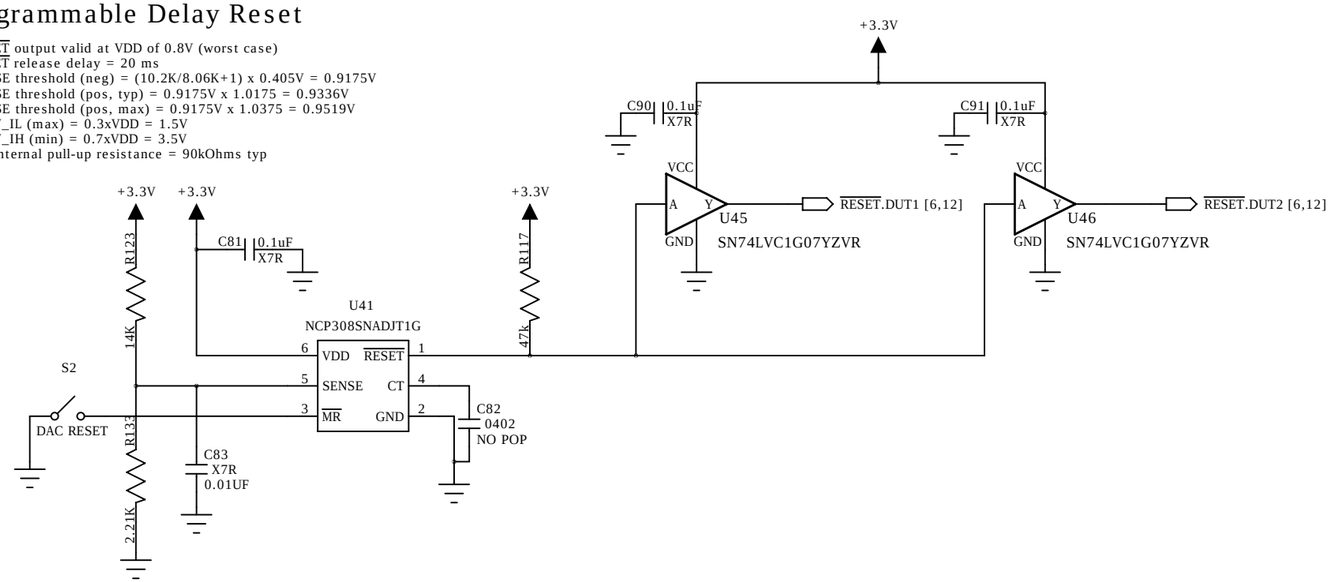
Programmable Delay Reset

$\overline{\text{RESET}}$ output valid at VDD of 0.8V (worst case)
$\overline{\text{RESET}}$ release delay = 20 ms
SENSE threshold (neg) = (10.2K/8.06K+1) x 0.405V = 0.9175V
SENSE threshold (pos, typ) = 0.9175V x 1.0175 = 0.9336V
$\overline{\text{SENSE}}$ threshold (pos, max) = 0.9175V x 1.0375 = 0.9519V
$\overline{\text{MR}}$ V_IL (max) = 0.3xVDD = 1.5V
$\overline{\text{MR}}$ V_IH (min) = 0.7xVDD = 3.5V
$\overline{\text{MR}}$ internal pull-up resistance = 90kOhms typ



Programmable Delay Reset

$\overline{\text{RESET}}$ output valid at VDD of 0.8V (worst case)
$\overline{\text{RESET}}$ release delay = 20 ms
SENSE threshold (neg) = (10.2K/8.06K+1) x 0.405V = 0.9175V
SENSE threshold (pos, typ) = 0.9175V x 1.0175 = 0.9336V
$\overline{\text{SENSE}}$ threshold (pos, max) = 0.9175V x 1.0375 = 0.9519V
$\overline{\text{MR}}$ V_IL (max) = 0.3xVDD = 1.5V
$\overline{\text{MR}}$ V_IH (min) = 0.7xVDD = 3.5V
$\overline{\text{MR}}$ internal pull-up resistance = 90kOhms typ



CIRRUS LOGIC

SHEET TITLE	DEBOUNCE-RESET		
PART #	CDB43131	Rev B1	
DRAWN BY	M. KUREK	ENGINEER M. KUREK	
DATE	7/10/2018	SHEET 12 OF 12	SHEET SIZE B