CX31988 USB Type-C Audio CODEC Datasheet

Hi-Res USB Type-C Compliant
Crystal-less Audio CODEC

PN: 505-000926-01 Rev 2

General Description

The Synaptics® AudioSmart™ CX31988 is a USB Type-C™ standard high-speed, low-power audio codec for USB Type-C headset applications without requiring external XTAL. With on-chip ADC and DAC, microphone preamplifiers and a capless headphone amplifier, the CX31988 is a true single-chip solution for applications that demand high audio quality and lower power consumption.

The key features of the CX31988 include:

- High performance playback
  - 384 kHz, 32-bit
  - 120 dB dynamic range
  - 130 dB SNR
  - -100 dB THD+N
- Mono high-performance audio ADC
  - 96 kHz, 24-bit
  - 115 dB dynamic range
  - -90 dB THD+N

Microphone performance is enhanced through programmable preamplifiers paired with a dedicated bias supply to eliminate crosstalk.

A ground-referenced output removes the need for capacitors on the headphone output, ensuring consistent performance with a wide variety of transducers.

An integrated DC-DC converter supports internal dynamic voltage scaling, and frequency scaling mechanisms to reduce power consumption. The converter can also provide power for all peripheral devices connected to the board.

Feature Summary

- ARM® Cortex® M0+ controller, up to 48 MHz operation
- Up to 96 KB in SRAM
- Skype and USB 2.0-compliant high-speed and full-speed device
- Internal oscillator generator
- One I²C master or one I²C slave
- On-chip 256 KB eFlash
- One watchdog timer
- Standard USB playback sample rate support of 8 kHz to 384 kHz
- Single wide range input power supply (2.85V–5.5V)
- Temperature range of –40°C to 85°C
- 49-pin, 2.610 x 4.135 mm eWLB package.

Applications

- USB Type-C headset

Contents

1. Introduction

The CX31988 device combines the exceptional low power, energy-efficient and easy-to-use ARM Cortex M0+ 32-bit MCU with a high-performance audio CODEC.

The device is an ideal SoC solution for many varied applications, such as advanced USB Type-C headsets.

Figure 1 shows the CX31988 system block diagram.

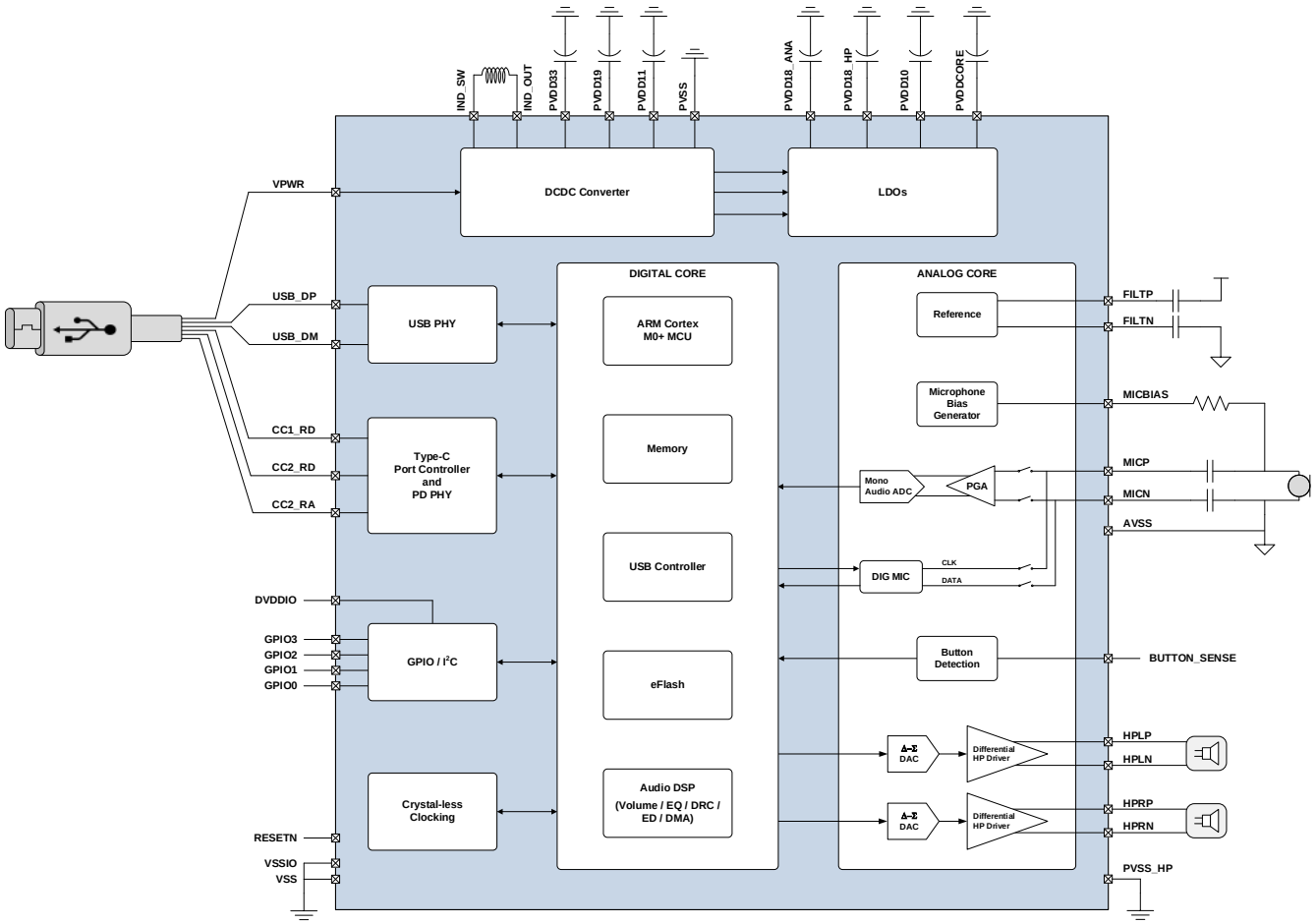


Figure 1. CX31988 system block diagram

2. Electrical Characteristics

Table 1. DC supply voltages

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Power supply	VPWR	2.85	5.00	5.50	V	Main IC input supply typically USB 5V
3.3V power	PVDD33	–	3.30	–	V	Generates 3.3V output
1.9V power	PVDD19	–	1.90	–	V	Generates 1.9V output
1.1V power	PVDD11	–	1.10	–	V	Generates 1.1V output
Analog power	PVDD18_ANA	–	1.80	–	V	Generates analog supply output
HP Driver power	PVDD18_HP	–	1.80	–	V	Generates HP supply output
Core power	PVDDCORE	–	1.10	–	V	Generates core output
1.0V power	PVDD10	–	1.00	–	V	Generates 1.0 output
IO power	DVDDIO	–	1.80 / 3.30	–	V	IO input voltage

Table 2. DC characteristics—TTL compatible (GPIOs and keypad interface)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input voltage low	VIL	0	—	0.3*DVDDIO	V	—
Input voltage high	VIH	DVDDIO*0.7	—	DVDDIO	V	—
Output voltage low	VOL	0	—	0.2*DVDDIO	V	—
Output voltage high	VOH	0.8*DVDDIO	—	DVDDIO	V	—
GPIO output sink current at VOL with DVDDIO=1.8V	IOL	—	—	8	mA	—
GPIO output sink current at VOL with DVDDIO=3.3V	IOL	—	—	14.7	mA	—
GPIO output source current at VOH with DVDDIO=1.8V	IOH	—	—	8	mA	—
GPIO output source current at VOH with DVDDIO=3.3V	IOH	—	—	14.6	mA	—

Table 3. DAC performance (32Ω load)

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
DAC Output Path (32Ω load, 24-bit, 48 kHz)					
Output Voltage Level	0 dB Gain Setting	–	1	–	V_RMS
Maximum Output Power	0 dB Gain Setting	–	31.25	–	mW
SNR	0 dBFS for signal measurement Silence for noise measurement	–	130	–	dB
Dynamic Range	-60 dBFS signal source	–	120	–	dB A-w
THD+N	0 dB signal source	–	−100	–	dB
Inter-channel Crosstalk	1 kHz 10 kHz	–	−90 −90	–	dB
Intermodulation Distortion (IMD)	−2 dB 60 Hz, −14 dB 7k	–	−83	–	dB
	−5 dB 60 Hz, −17 dB 7k	–	−84	–	dB
	−8 dB 60 Hz, −20 dB 7k	–	−86	–	dB
DC Offset	−100 dBFS source signal	–	50	–	µV DC
Pop Level	USB plug/unplug, audio jack plug/unplug, DAC enable/disable	–	−75	–	dBV
Phase Error	0 dBFS, 997 Hz source signal	–	0.01	–	Degrees
Frequency Response	20 Hz to 20 kHz 20 kHz to 40 kHz	–	+/−0.02 +/−0.05	–	dB
PSRR	217 Hz, −20 dBV to VPWR supply	100		–	dB
	1 kHz, −20 dBV to VPWR supply	100		–	dB
Output Capacitive Loading	–	–	–	1	nF

Test conditions (unless otherwise specified):

- Ambient temperature = 25° C
- VPWR = 5.0V and SWGND, VSS, VSSIO, AVSS and PVSS = 0V.
- Input signal is 0 dBFS, 997 Hz
- Measurement bandwidth: 20 Hz– 20 kHz
- Digital data bit width is 24-bit and sample rate is 48 kHz
- EQ and DRC disabled
- Digital volume set to 0 dB
- Headphone load = 32Ω

Table 4. ADC performance

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
ADC Input Path (24-bit 48 kHz)					
Maximum Full Scale Input	ADC Boost @ 0 dB (differential)	–	1.0	–	V_{RMS}
	ADC Boost @ 0 dB (single-ended)	–	0.5	–	V_{RMS}
	ADC Boost @ 6 dB	–	0.50	–	V_{RMS}
	ADC Boost @ 12 dB	–	0.25	–	V_{RMS}
Dynamic Range	ADC Boost @ 0 dB, −60 dBV input source	–	115	–	dB
	ADC Boost @ 6 dB, −66 dBV input source	–	112	–	dB
	ADC Boost @ 12 dB, −72 dBV input source	–	108	–	dB
THD+N −3 dBFS	ADC Boost @ 0 dB, −3 dBV input source	–	−90	–	dB
	ADC Boost @ 6 dB, −9 dBV input source	–	−90	–	dB
	ADC Boost @ 12 dB, −15 dBV input source	–	−90	–	dB
CMRR	1 kHz, −20 dBV common input, ADC Boost @ 0 dB	–	100	–	dB
	1 kHz, −20 dBV common input, ADC Boost @ 21 dB	–	71	–	dB
Input resistance	Programmable Default is 100k	–	50k	–	Ω
		–	100k	–	Ω
		–	500k	–	Ω
		–	1M		Ω
Gain Steps	0, 6-21 in 3 dB gain steps	–	3	–	dB

Test conditions (unless otherwise specified):

- Ambient temperature = 25°C
- VPWR = 5.0V and SWGND, VSS, VSSIO, AVSS and PVSS = 0V
- Measurement bandwidth: 20 Hz– 20 kHz
- Digital data bit width is 24-bit and sample rate is 48 kHz
- EQ disabled
- Digital volume set to 0 dB
- Microphone load = 3 kΩ

Table 5. Microphone Bias Parameters

Parameter	Test Conditions / Notes	Min	Typ	Max	Unit
Micbias Output Voltage Range	Controllable in 0.1V steps	1.8		3.1	V
Micbias Resistor Trim Range	Controllable in 50Ω steps	2000	2200	2400	Ω
Micbias Max Load Current	Typical Max load current		2		mA
Micbias Voltage Current Limit Range	Controllable	5, 10, 15, No Limiting			mA
Load Capacitance	For any setting of voltage or mic resistor, including resistor bypass	0	0.1	10	µF

Table 6. Power consumption

Case	USB High-Speed with LPM 5V at VP WR (mW)
Suspend	0.52
Idle	11.56
Stereo playback with no signal	19.78
Stereo playback at 0.1 mW per channel	27.80
Mono record at −60 dB of full scale	17.57

3. Analog Input Path

This section describes how to connect an analog microphone to the CX31988 device, and steps through the internal gain and processing blocks that the microphone signal passes through before being sent to the host.

3.1. Microphone Path Specifications

- Mono microphone input
- Boost = 0 dB, 6 dB, 9 dB, 12 dB, 15 dB, 18 dB, 21 dB
- Power-up/down click and pop suppression
- Dynamic range = 115 dBFS A-wt
- THD+N at –3 dBFS = –90 dB

3.2. Analog-to-Digital Converter Parameters

- Mono
- 16-bit/24-bit data path
- Sampling rates of 8 kHz, 16 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Digital gain = –69 dB to 24 dB in 0.5 dB steps

3.3. Microphone (Record) Signal Path

Figure 2 shows the full microphone path. The microphone signal goes through these stages:

1. Analog gain adjusted via the PGA (Programmable Gain Amplifier) block. This is typically a fixed setting, based on the microphone selected.
2. Converted to digital signal at the ADC.
3. High Pass Filter (HPF). This block allows for filtering unwanted low frequency noise.
4. Decimator and FIR filtering.
5. Digital Volume Adjustment. This block is tied to the host system's volume control.
6. 5-Band EQ block.

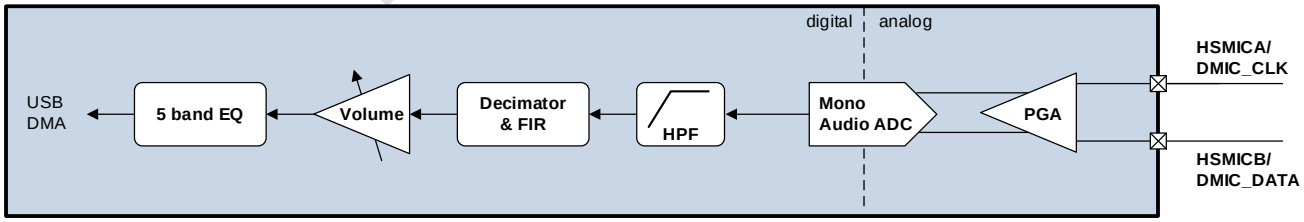


Figure 2. Microphone process path

3.4. Analog Microphone Input to the ADC

The audio input signal path supports single-ended and differential microphone signals. The following figures provide suggested configurations for each case.

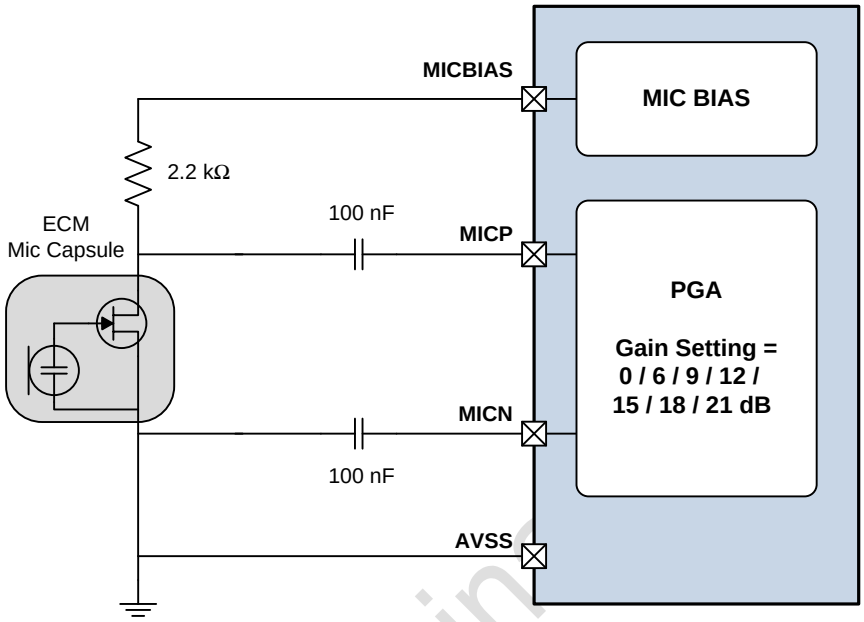


Figure 3. Single-ended ECM microphone biasing configuration

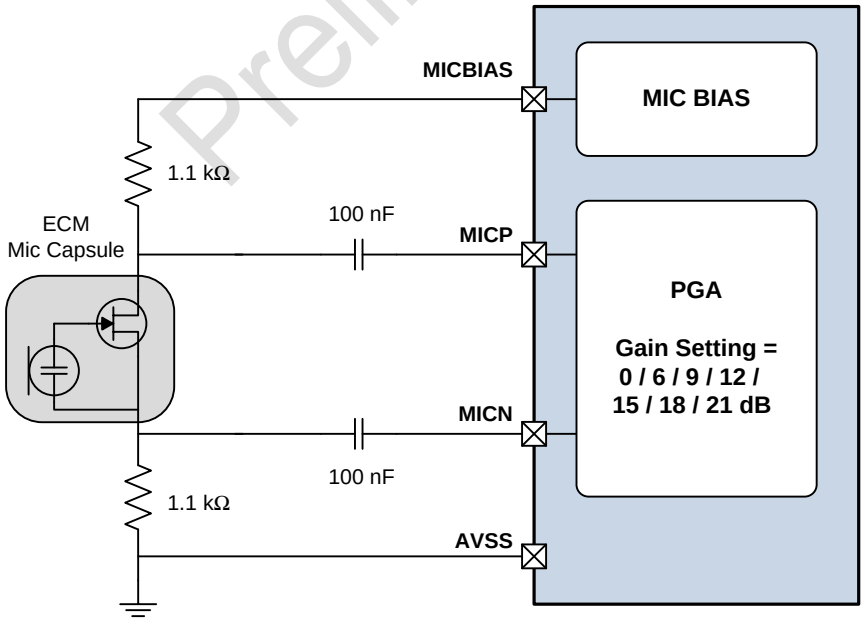


Figure 4. Differential ECM microphone biasing configuration

3.5. Microphone Bias Generator

The microphone bias generator supports both ECM and MEMS microphones. For AC-coupled ECM microphones, it provides a current bias by driving a fixed-voltage output through a series resistor. For MEMS microphones, the fixed output voltage can be directly used as a voltage supply.

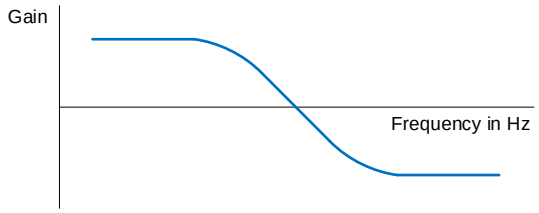
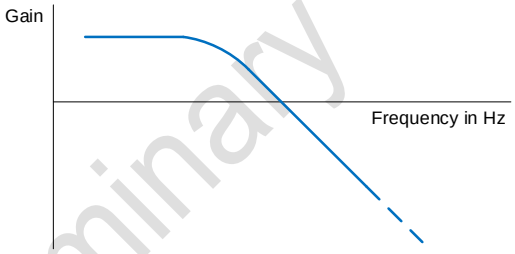
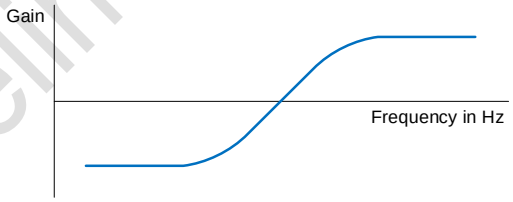
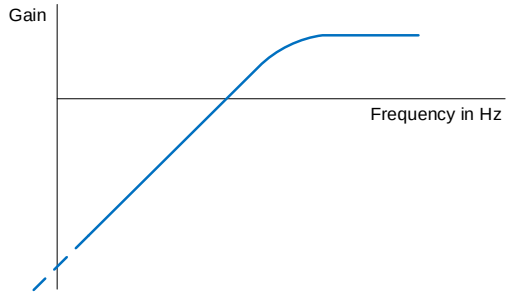
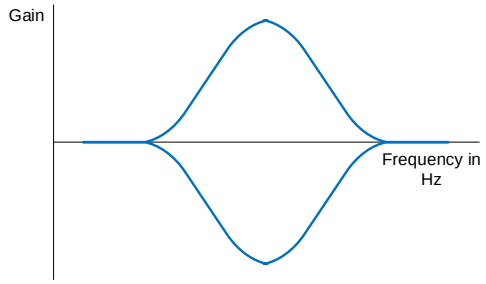
The microphone bias circuitry can supply an output current of up to 2 mA, which is suitable for traditional ECM microphones. Also, the feed resistance can be provided externally or via an internal on-chip 2.2 kΩ resistor. To accommodate the power supply requirements of most MEMS microphones, the microphone bias voltage is programmable from 1.8V to 3.1V in 0.1V steps.

3.6. Five Band Equalizer

The microphone input paths have a 5-band bi-quad IIR EQ (with bypass capability). Each equalizer (EQ) is arranged as a parametric (serial) cascade of independent second-order IIR filters. The function of the EQ is to adjust the frequency characteristics of the input to compensate for unwanted frequency characteristics in the microphone. It can also tailor the response according to user preferences.

Five EQ responses are selectable and tunable for each band. Gain, center frequency, and quality factor are tunable, as shown in Table 7.

Table 7. Five band EQ responses

EQ Response	Graph
Lo-shelf	
Lo-pass	
Hi-shelf	
Hi-pass	
Peaking	

Each EQ band stage is a second order IIR filter. Each IIR has 10 branches that perform multiplication between data and coefficients and an accumulator of the products. The multiplier calculates the 48-bit product of a 32-bit data value and a 16-bit coefficient value. The lowest seven bits of the product are removed before the product is summed into the accumulator. Each IIR stage has a shift parameter “G” that affects the output of its accumulator as specified:

- 0: −12 dB
- 1: −6 dB
- 2: 0 dB
- 3: +6 dB
- 4: +12 dB
- 5: +18 dB

4. Digital Microphone Characteristics

The CX31988 also supports the use of one digital microphone (DMIC). The MICP and MICN pins are muxed with the digital microphone clock and data signals (see Pin Descriptions for more information). Before testing the digital microphone functionality, please verify that firmware that supports this function is loaded on the device.

Note: The microphone can be configured for either left or right channel, as the CX31988 firmware can be configured to support either case.

The CX31988 supports digital microphones powered by 1.8V or 3.3V.

The CX31988 DMIC interface is used to accept PDM audio data from the integrated ADCs of the digital microphones. The DMIC characteristics are shown in Table 8.

Table 8. Digital microphone characteristics, 3.3V power

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DMIC DAT input High level	V_{IH}	2.0	–	VDDO	V
DMIC DAT input Low level	V_{IL}	0	–	35% of VDDO	V
DMIC CLK output High level	V_{OH}	VDDO-0.4	–	–	V
DMIC CLK output Low level	V_{OL}		–	0.4	V

5. Analog Output Path

This section describes the internal gain and processing blocks that the headphone signal passes through, starting as a USB or I²S digital signal, passing through gain, filter, and processing blocks, and finally converted to an analog signal and sent to headphone output pins.

5.1. Headphone Output Path Specifications

- Headphone/line driver = capless, stereo
- Single-ended line-out (1 V_{RMS} at 10 kΩ) or headphone (1 V_{RMS} at 32Ω, 31 mW)
- Frequency range = 20 Hz to 20 kHz (+/−0.02 dB), 20 kHz to 40 kHz (+/− 0.05 dB)
- THD+N at 0 dBFS = –100 dB at 32Ω load
- Dynamic range = 120 dBFS A-wt
- Crosstalk = –100 dB maximum
- The headphone maximum output can be limited. This is to comply with the GS Mark standard.

5.2. Digital-to-Analog Converter (DAC) Parameters

- Stereo 16-bit/24/32-bit data path
- Sampling rates of 8 kHz, 16 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz, and 384 kHz
- Digital gain = –73.5 dB to +6 dB in 0.5 dB steps

5.3. Headphone (Playback) Signal Path

Figure 5 shows the entire playback path. The headphone signal goes through the following stages:

1. 10-Band EQ
2. 3-Band dynamic range compression (DRC)
3. Interpolator and FIR filtering.
4. Digital Volume Adjustment. This block is tied to the host system's volume control.
5. High pass filter (HFP). This block allows for filtering unwanted low frequency noise.
6. Delta-Sigma DAC
7. Class-G Headphone amp driver

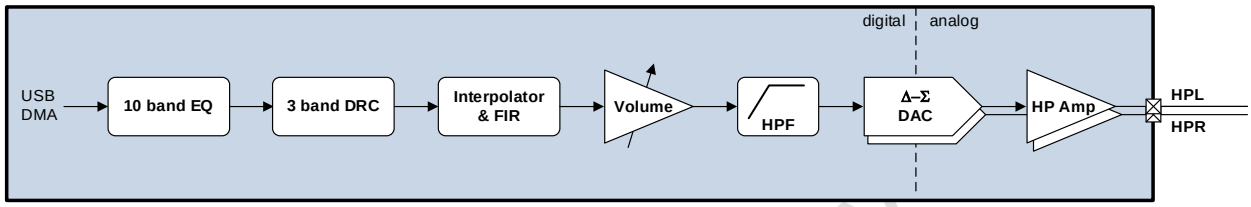
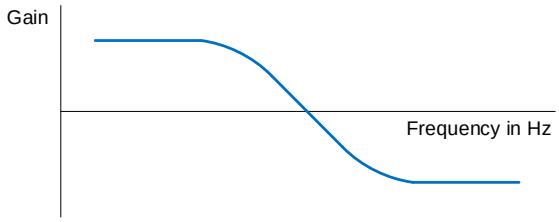
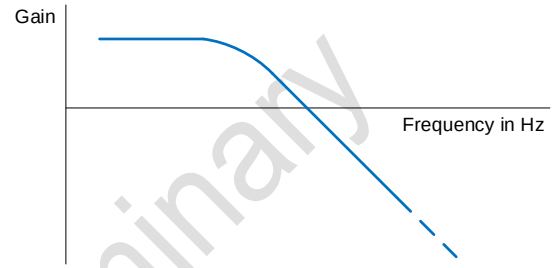
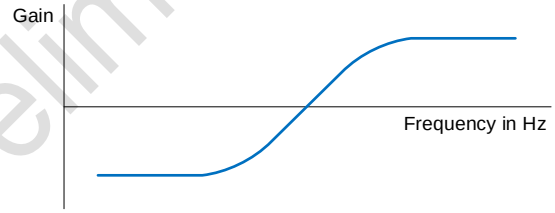
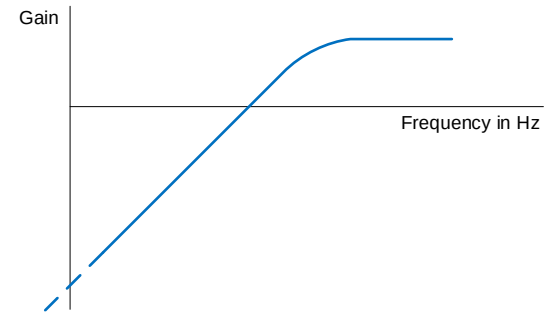
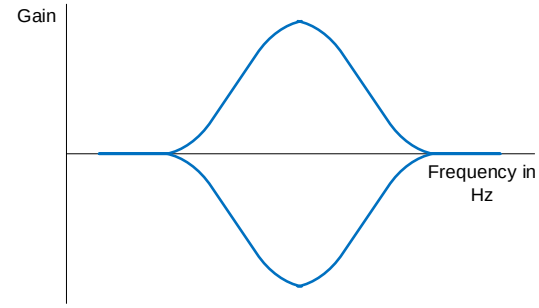


Figure 5. USB headphone process path

5.4. Ten Band Equalizer Architecture

The Speaker and Line Out paths have a 10-band bi-quad IIR EQ (with bypass capability). Each equalizer (EQ) is arranged as a parametric (serial) cascade of independent second-order IIR filters. The function of the EQ is to adjust the frequency characteristics of the output to compensate for unwanted frequency characteristics in the loudspeaker. The EQ can also be used to tailor the response according to user preferences. Ten EQ responses are selectable and tunable for each band. Gain, center frequency, and quality factor are tunable, as shown in Table 9.

Table 9. Ten band EQ responses

EQ Response	Graph
Lo-shelf	
Lo-pass	
Hi-shelf	
Hi-pass	
Peaking	

Each EQ band stage is a second order IIR filter. Each IIR has five branches that perform multiplication between data and coefficients and an accumulator of the products. The multiplier calculates the 48-bit product of a 32-bit data value and a 16-bit coefficient value. The lowest 7 bits of the product are removed before the product is summed into the accumulator. Each IIR stage has a shift parameter "G" that affects the output of its accumulator as specified:

- 0: −12 dB
- 1: −6 dB
- 2: 0 dB
- 3: +6 dB
- 4: +12 dB
- 5: +18 dB

5.5. Playback Path Dynamic Range Compression

The FCP Tuning Application enables complete DRC module tuning. Figure 6 shows the three frequency-banded DRCs and the overall DRC. Each banded DRC can be tuned, as discussed in Tuning Dynamic Range Compression. The low compression region of the overall DRC, used typically for expansion, is not required for performance and is not implemented.

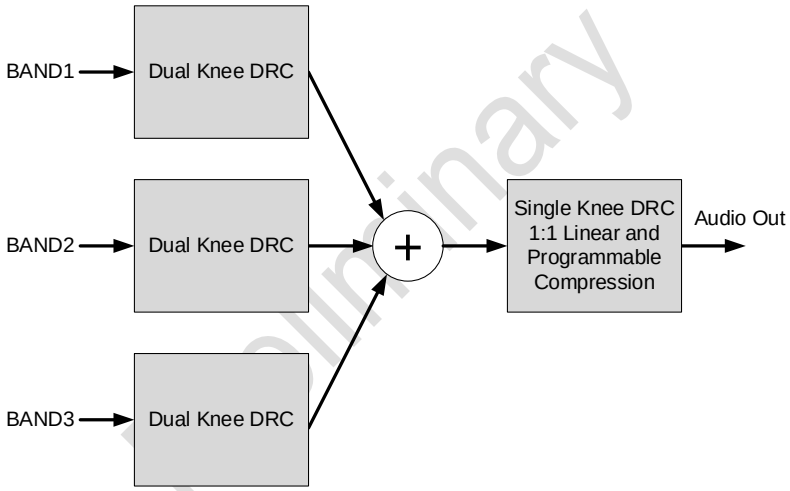


Figure 6. FCP tuning application DRC module block diagram

The playback path DRC module allows the signal level to be boosted while preventing clipping distortion. The DRC module consists of three frequency bands of DCR with summed output into one oval DRC. The DRC frequency bands allow compression of different scales to be applied in the different frequency bands. The overall DRC is applied to the entire signal after the individual DCR bands are summed together. The DCR blocks provide three regions of compression:

- CR_HI provides compression with adjustable knee KNEE_HI and adjustable compression ratio. This region is typically tuned for high input compression.
- CR_MID provides compression between KNEE_HI and KNEE_LO with adjustable compression ratio. This region is typically tuned for middle input linear gain.
- CR_LO provides compression with adjustable knee KNEE_LO and adjustable compression ratio. This region is typically tuned for low input expansion.

The frequency region of the bands and the time constants of the attack and release in and out of the linear region are tunable.

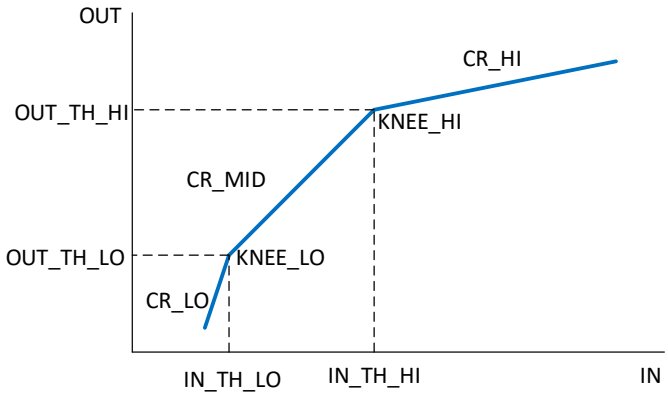


Figure 7. DRC curve

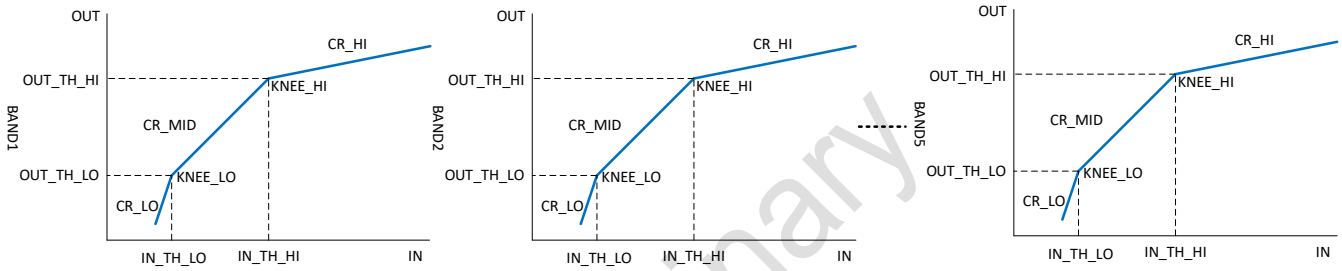


Figure 8. DRC compression bands

5.6. Stereo Hi-Fi Capless Differential Headphone Driver

The CX31988 output signal path provides a stereo capless headphone driver that can drive loads as low as 16Ω. The nominal load is 32Ω and includes the ability to operate safely in open circuits with capacitive loads of up to 1 nF single-ended to ground. A line-output mode is also provided where the headphone amplifier can conserve power by driving light loads such as a 10 kΩ line input load.

The headphone stereo drivers are capless amplifiers whose outputs are ground referenced. AC coupling capacitors are not required to connect to the headphone loads.

The CX31988 output signal path shown in Figure 9 consists of a 24-bit sigma delta DAC for high performance applications. The playback path is also optimized to minimize clicks and pops during various state transitions.

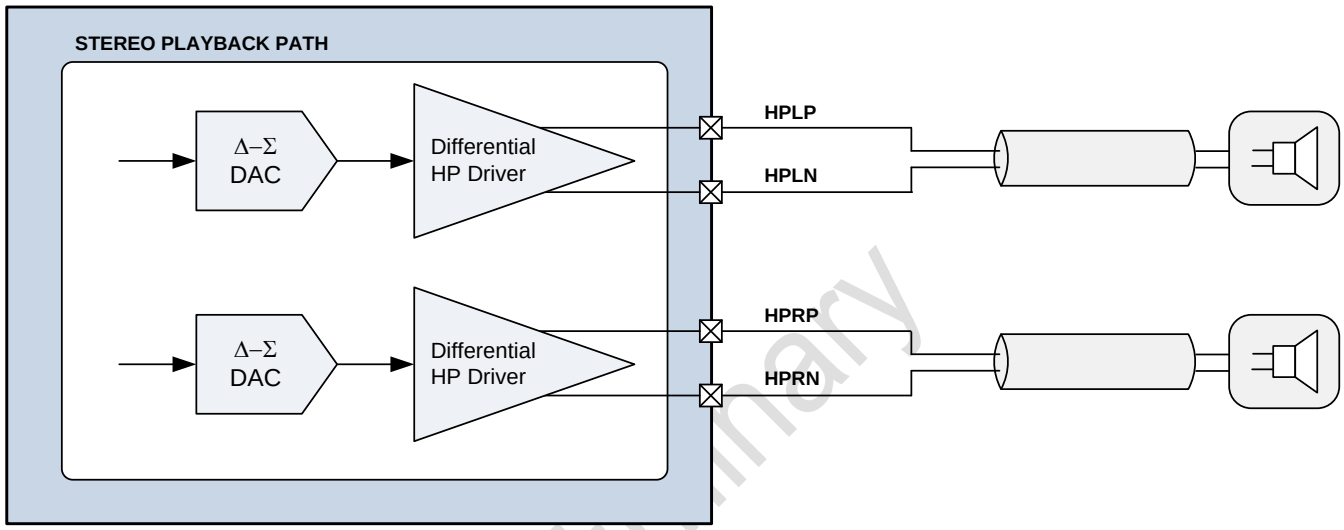


Figure 9. Output signal path

6. USB Digital Audio and Control Interface

The CX31988 USB function controller is a USB 2.0-compliant (USB 3.0-compatible) high-speed/full speed device with integrated transceiver and on-chip matching and pull-up resistors. The controller enumerates to the host as a standard USB audio device and HID consumer control supporting:

- USB digital audio out (audio playback device)
- USB digital audio in (microphone/recording device)
- HID consumer control handling standard volume and mute functionality

The CX31988 device includes USB device functionality, with the following features:

- Operates as a device (Upward Facing Data Port) only
- Supports full-speed and hi-speed operation
- Compatible with Type-C, as well as legacy connector types
- Supports Power Delivery (PD) communications
- With the addition of external power switching devices, supports PD-related functions such as power role reversal, and operation as a V_{CONN} Powered Device (VPD)
- Supports Link Power Management (LPM)
- Terminal connector detection and Interrupt end points
- HID support is fully compatible with Google specifications

6.1. USB Type-C Port Controller

The CX31988 uses a USB Type-C port controller for implementing an Upstream Facing Port (UFP) that sinks power for either a standard USB Type-C receptacle or plug and a PD PHY and controller for implementing a VPD. This includes:

- Configuration Channel support for USB Type-C receptacle or plug
  - Internal Rd and Ra pull-down resistors
  - V_{CONN} discharge function
  - CC monitoring for connect, cable orientation, and disconnect detection
- Power Delivery communication
  - PHY (baseband), protocol engine, and low-level policy manager in hardware for fast response
  - High level policy manager in firmware

6.2. USB Link Power Management

The integrated USB 2.0 controller and PHY support the USB Link Power Management sleep state (L1) that allows for significant system power savings by placing the bus into a low power state between bursts of audio data. Intervals of 2 ms, 4 ms, and 8 ms are supported. The LPM feature can be enabled or disabled depending on the host requirement.

6.2.1. *USB Audio Class and HID Support*

USB Audio Class (UAC) 2.0 and 3.0 are supported. The CX31988 can support multiple channels at a high sample rate and full bit depth. The device uses the USB client external clock to establish minimal jitter at the target device. The CX31988 supports the HID 1.11 Device Class Definition.

6.2.2. *USB Linear PCM Support*

The CX31988 supports linear PCM (Type 1) format (record stream) and linear PCM (Type 1) format (playback stream). On the stereo playback path, sample rates of 16-bit, 24-bit, and 32-bit are supported at sample rates of up to 384 kHz. On the mono record path, sample rates of 16-bit and 24-bit are supported at sample rates of up to 96 kHz.

7. ARM

7.1. ARM Cortex M0+ Microcontroller

The device core uses an energy-efficient ARM Cortex M0+ 32-bit microcontroller unit (MCU) that runs at up to 48 MHz. The ARM Cortex M0+ processor is a high-performance and energy-efficient ARM processor.

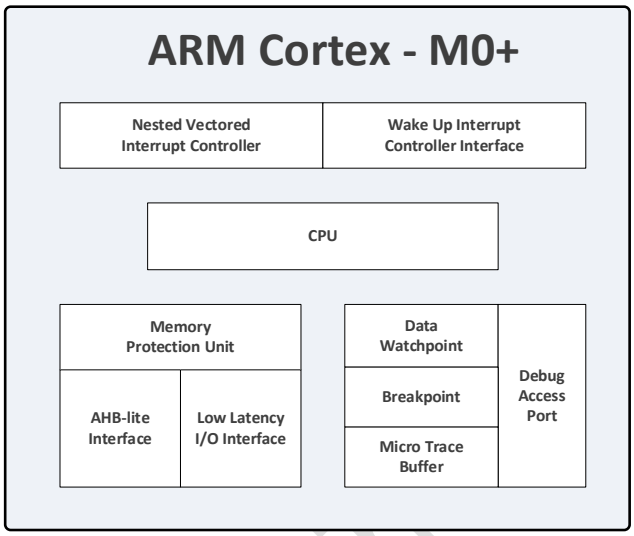


Figure 10. ARM Cortex core architecture

The ARM Cortex M0+ processor keeps the same 56 instructions of the Cortex-M0 processor, enabling simple and quick development. The Thumb® instruction set offers an unrivaled code-density while providing access to 32-bit computation performance.

- Processor power consumption as low as 9 µA/MHz
- Outstanding result: 1.77 CoreMark/MHz

7.2. Specifications

- ARMv6-M Thumb instruction set
- Thumb-2 technology
- ARMv6-M compliant 23-bit SysTick timer
- Fast single-cycle 32-bit hardware multiplier
- 96 kByte internal SRAM memory
- Support for either little-endian or byte invariant big-endian data accesses.
- Deterministic, fixed-latency, interrupt handling.
- Load/store multiple and multicycle multiply instructions that can be abandoned and restarted to facilitate rapid interrupt handling.
- Unprivileged/privileged support for improved system integrity.
- Uses the ARMv6-M, C-Application Binary Interface (C-ABI) compliant exception model, enabling use of pure C functions as interrupt handlers.
- Low-power sleep-model entry using Wait for Interrupt (WFI). Wait for Event (WFE) instructions, or the return from interrupt sleep-on-exit feature.

8. Headset and Button Control

8.1. Inline Button Detection

The CX31988 includes support for various button detection configurations, including an ECM mic module with an external microphone bias resistor, an ECM mic module with an internal microphone bias resistor, and a four button-only interface. Hardware configurations for each case are shown in Figure 11 and Figure 12.

The microphone element is modeled as a 1 kΩ or greater resistor. This is a reasonable model for common ECM microphones used in PCs and headsets. The CODEC is expected to provide a MICBIAS voltage between 1.8V and 3.1V for compatibility with common microphones.

The default configuration assumes that a specific resistance is placed in parallel with the microphone when a button is pressed. The range for each button resistance is shown in Table 10.

Table 10. Google® button resistance

Resistor	Minimum	Nominal	Maximum
Microphone	1 kΩ	—	—
Button 1	0	1	70Ω
Button 2	210Ω	240Ω	290Ω
Button 3	360Ω	470Ω	680Ω
Button 4	110Ω	135Ω	180Ω

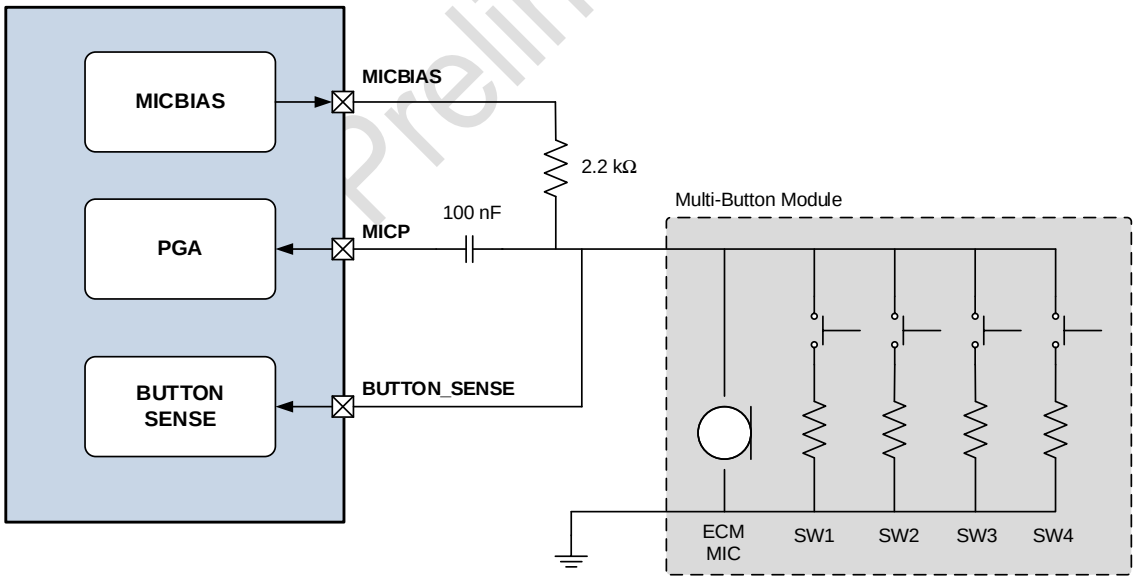


Figure 11. ECM microphone with multi-button network in parallel with external 2.2 kΩ microphone bias resistor

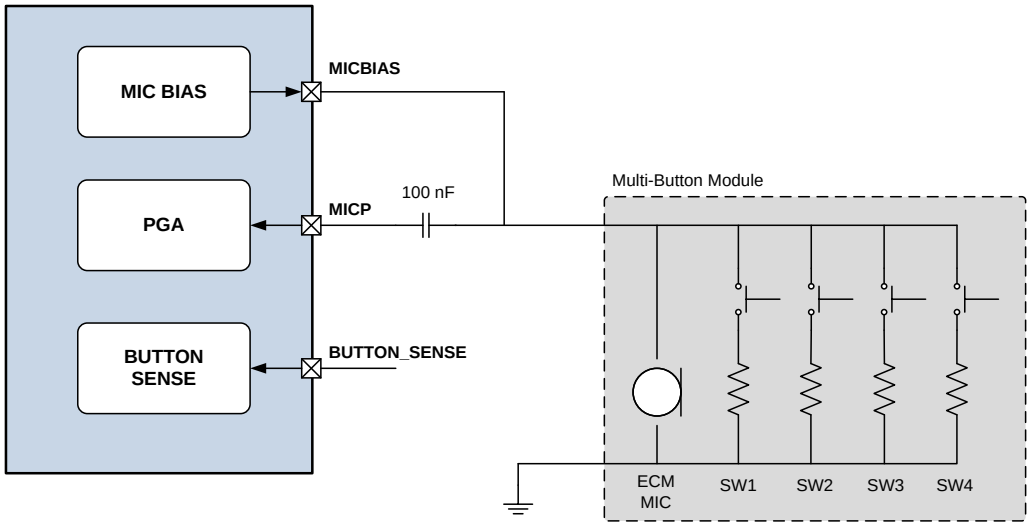


Figure 12. ECM microphone with multi-button network in parallel and an internal 2.2 kΩ microphone bias resistor

8.2. Headset Button Interface

The CX31988 also includes a dedicated button pin that allows for support of up to five buttons. Resistor values to be used for each button are shown in Table 11.

Table 11. Button Resistance

Resistor	Minimum	Nominal	Maximum
Button 1	–	0	–
Button 2	–	5.11k	–
Button 3	–	10.0kΩ	–
Button 4	–	20.0kΩ	–
Button 5	–	39.2k	–

The hardware configuration is shown in Figure 13.

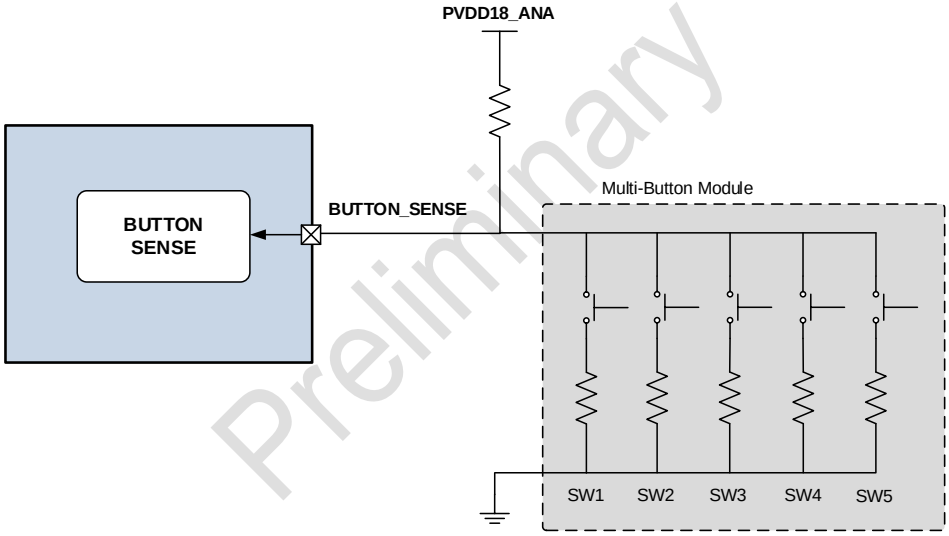


Figure 13. Four-button interface with PVDD18 reference

9. I²C Control Interface

The CX31988 supports I²C and USB HID interfaces for serial communications with the CX31988 registers for command and control.

9.1. I²C Slave

The CX31988 supports a single I²C slave interface. The I²C slave is a standard I²C slave with address hexadecimal 0x41. The I²C slave:

- Is used for USB/I²C tunneling and external co-processor control
- Supports 100 kHz, 400 kHz and 1 MHz

9.1.1. *Data Flow Diagram*

Complete the following steps to write to the CX31988 device:

8. Send a start sequence.
9. Send the I²C address of the slave.
10. Send the register address for the write (24-bit).
11. Send the data bytes (4-byte data).
12. Optional: Send any further data bytes (burst operation).
13. Send the stop sequence.

Complete the following steps to read from the CX31988 device:

14. Send a start sequence.
15. Send the I²C address of the slave.
16. Send the register address (24-bit).
17. Send a start sequence again (repeated start).
18. Read the data bytes (4-byte data).
19. *Optional:* Read any further data bytes in case of a burst read mode.
20. Send the stop sequence.

9.1.2. *Transferring Data on the I2C Bus*

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first, as shown in Figure 14.

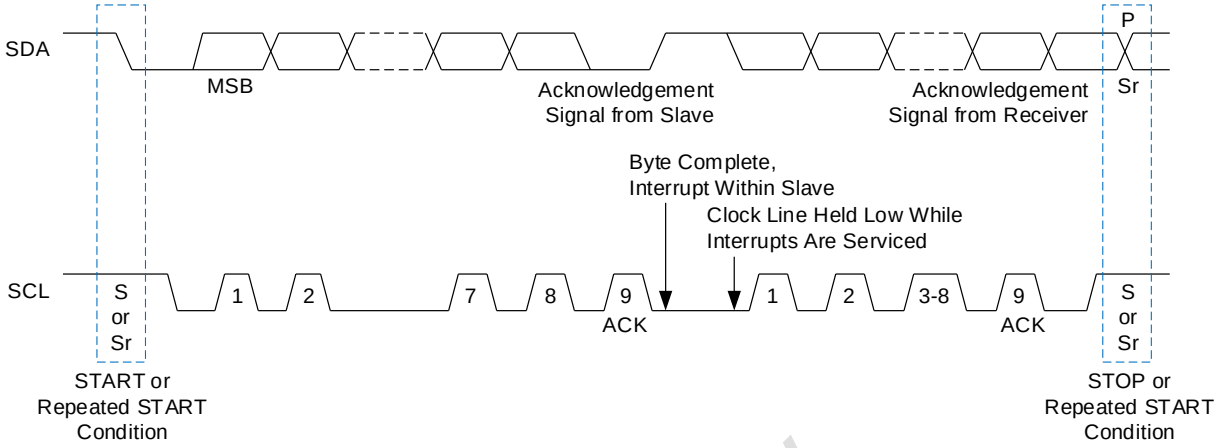


Figure 14. I²C bus transactions

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This state indicates a START condition. A LOW to HIGH transition on the SDA line, while SCL is HIGH, defines a STOP condition. The master always generates the START and STOP conditions. The bus is considered busy after the START condition. The bus is considered free again in a defined time after the STOP condition. The data transfer format on the I²C bus is shown in Figure 15.

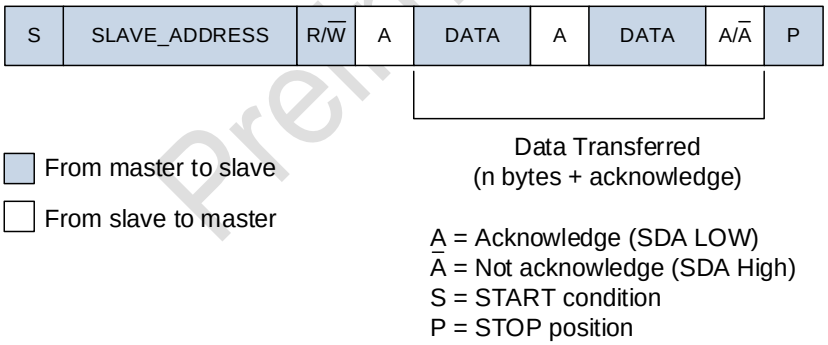


Figure 15. I²C data transfer format

9.1.3. I²C Slave Address Format

The I²C slave addressing format is shown in Table 12.

Table 12. I²C slave address format

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

9.1.4. I²C Interface Timing for 400 kHz Mode

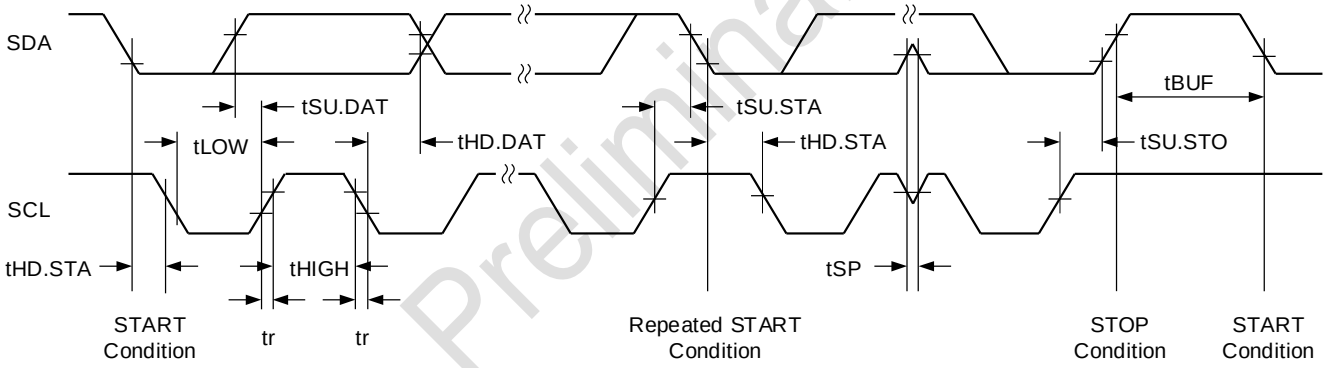


Figure 16. Interface timing requirements for 400 kHz transfer

Table 13. Interface timing requirements for 400 kHz transfer

I²C (400 kHz)	Symbol	Minimum	Maximum
Set-up Time Start Condition	tSU.STA	0.6 µs	–
Hold Time Start Condition	tHD.STA	0.6 µs	–
SCL Clock LOW Period	tLOW	1.3 µs	–
SCL Clock HIGH Period	tHIGH	0.6 µs	–
Data Set-up Time	tSU.DAT	100 ns	–
Data Hold Time	tHD.DAT	0	0.9 µs
Set-up Time for STOP Condition	tSU.STO	0.6 µs	–

10. General-Purpose Input/Outputs

The CX31988 supports four GPIOs. Alternately, these pins can be configured for UART or single-wire debug (SWD) functionality. The internal structure of each GPIO pin is shown in Figure 17.

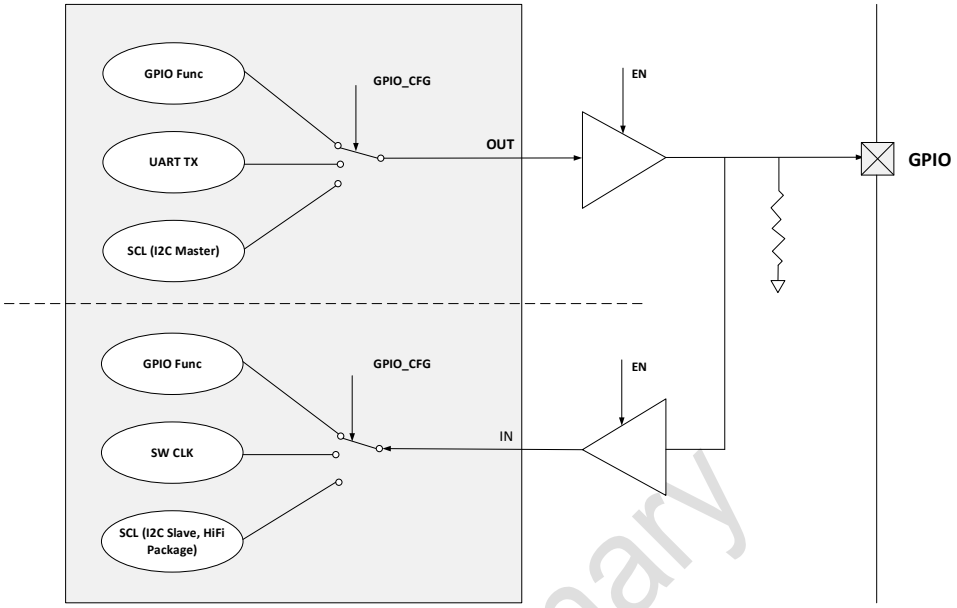


Figure 17. GPIO pins and alternative functions

Table 14. GPIO and alternative functions

I/O Name	Function	Direction	Settings
GPIO0	GPIO_0	IO	Default upon power up
	UART_TX	O	
	I²C Master SCL	O	
	I²C Slave SCL	I	
	SWD CLK	I	
GPIO1	GPIO_1	IO	Default upon power up
	UART_RX	I	
	I²C Master SDA	IO	
	I²C Slave SDA	IO	
	SWD DAT	IO	
GPIO2	GPIO_2	IO	Default upon power up
	UART_TX	O	
	SWD CLK	I	
GPIO3	GPIO_3	IO	Default upon power up
	UART_RX	I	
	SWD DAT	IO	

11. Power Management

The CX31988 can operate off a single power supply with a range of 2.85V to 5.5V. V_{BUS} can be used as the power source directly or a diode "OR" arrangement can be used to support V_{CONN}-powered USB devices that use either V_{BUS} or V_{CONN} as the power source. Within the CODEC is an advanced power management architecture that generates the different required power supplies. This architecture ensures an efficient and comprehensive system power consumption scheme while also optimizing performance.

Table 15. Power management definitions

Signal	Supply (V)	Function	Description
PVDD33	3.3	Output	Sourced from internal DCDC converter. Provides supply for USB PHY and microphone bias circuitry.
PVDD19	1.9	Output	Sourced from internal DCDC converter. Provides supply for PMU and LDOs for analog circuitry.
PVDD11	1.1	Output	Sourced from internal DCDC converter. Provides supply for LDOs for digital core and clocking circuitry.
PVDD18_ANA	1.8	Output	Derived from PVDD19 via an internal LDO. Provides supply for microphone and headphone analog circuity.
PVDD18_HP	1.8	Output	Derived from PVDD19 via an internal LDO. Provides supply for headphone drivers.
PVDD10	1.0	Output	Derived from PVDD11 via an internal LDO. Provides supply for clocking circuitry.
PVDDCORE	1.1 to 0.9	Output	Derived from PVDD11 via an internal LDO. Provides supply to digital core logic.
DVDDIO	1.8 or 3.3	Input	Input supply pin for digital IO pins. Typically connected to either 3.3V or 1.8V.

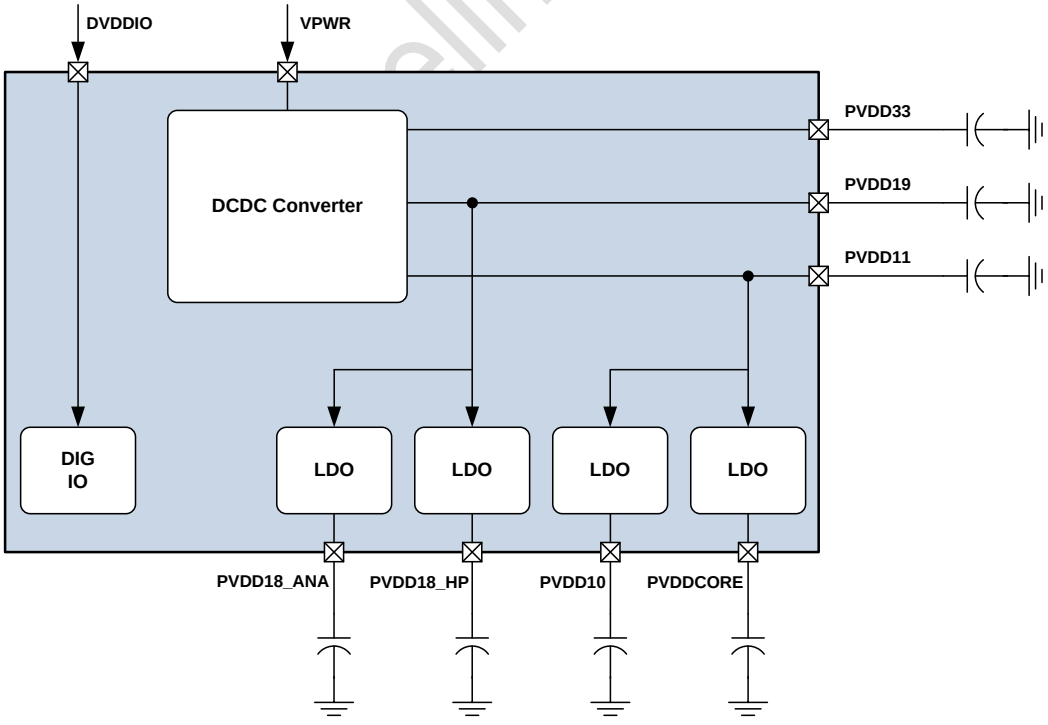


Figure 18. Power management architecture

The CX31988 can be taken out of suspend state with the following inputs:

- Button sense pin
- Inline mic multi-button
- All GPIO pins
- USB resume

12. Application Diagram

12.1. USB Type-C Headset with Android Button Support

The CX31988 provides a high quality, low-cost solution for wired USB Type-C Hi-Fi audio IC headsets used with smart phones, tablets or PCs. The CX31988 allows for the use of analog or digital microphones. The capless stereo output port supports all headphones with an impedance of 16Ω or greater. Four GPIO pins are available for LED support. Only 2.85V to 5.5V input power is required, and all other supplies are generated internally.

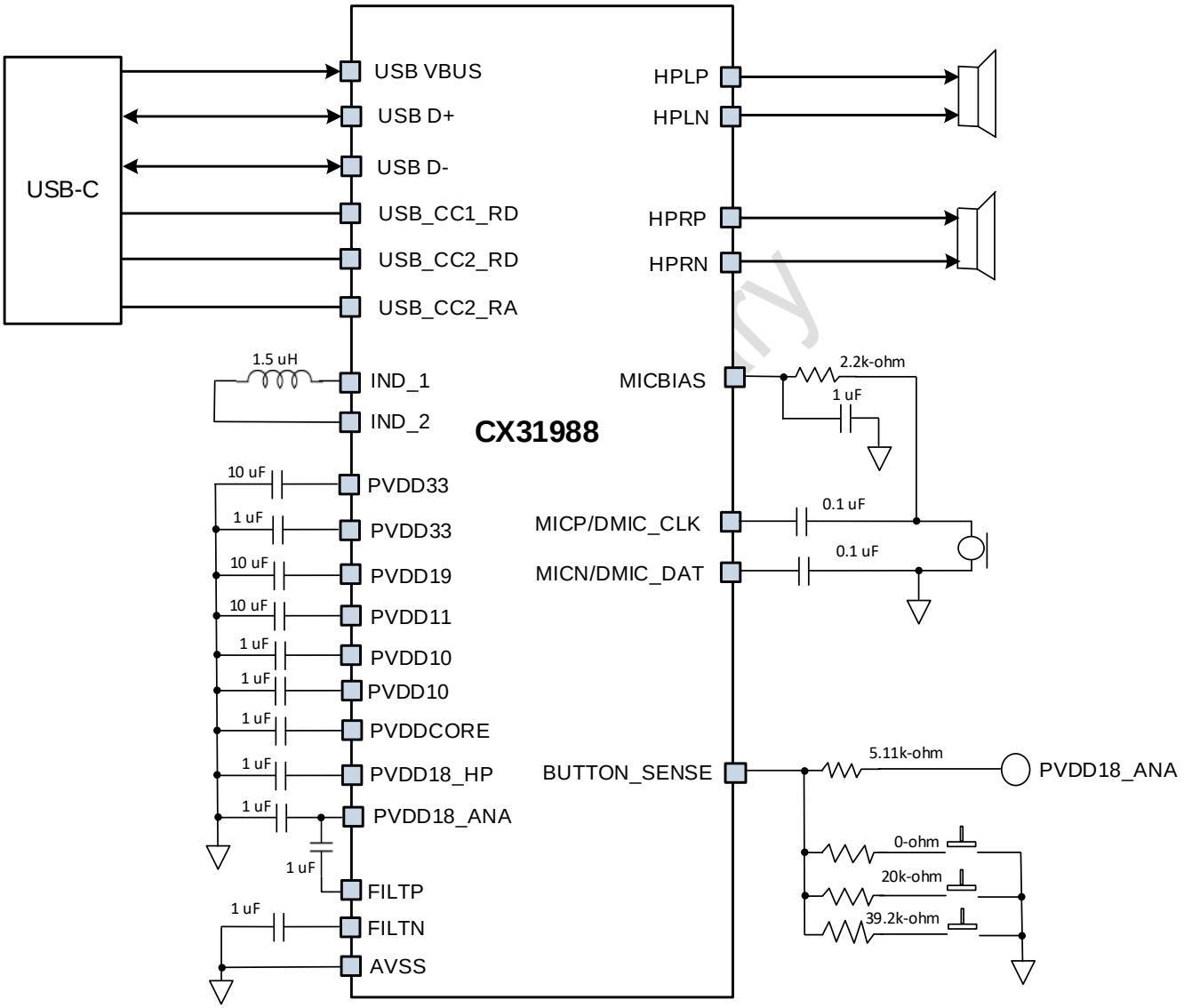


Figure 19. USB Type-C headset with Android button support block diagram

13. Tool and Firmware Flash Interface

The CX31988 is supported by several AudioSmart software tools. These include an Android® configuration application and Windows® firmware update application to be used by the end user. The Windows factory tool and the Windows tuning application tool are intended for development only.

13.1. Android Applications

The Android application can configure the CX31988 based headsets over USB. The application can be used for real time updates to the equalizers and DRC and for firmware updates. The application includes Synaptics branding by default, but can be updated with different branding and a different set of aesthetics. See the application reference documentation for more information about the CX31988 Android application.

13.2. eFlash Firmware Image Field Flashing

The Windows firmware update application can be used by the end user to update the firmware image. The user simply drags the update image and drops it on top of the application to start the update. The Windows update application includes Synaptics branding by default, but can be updated with different branding.

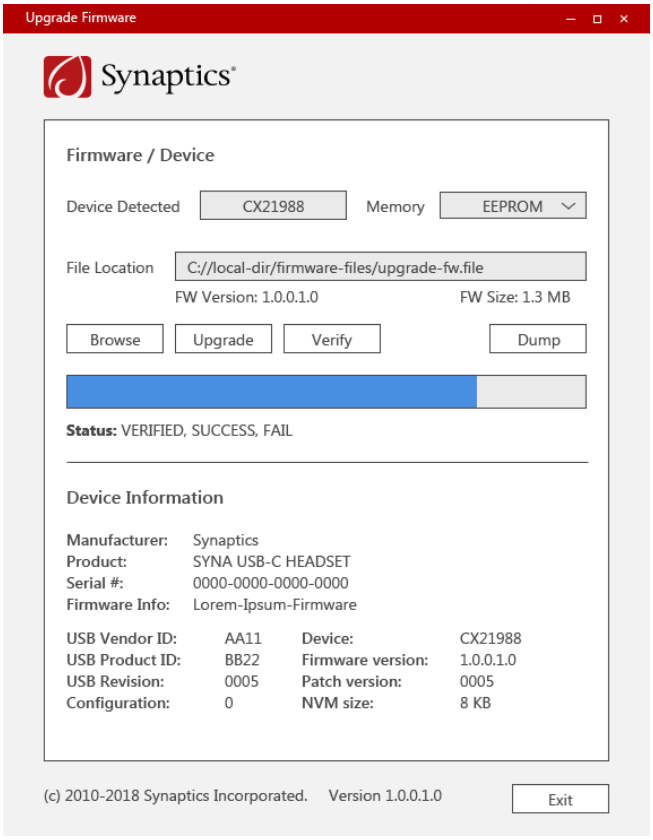


Figure 20. Upgrade firmware interface for image field flashing

13.3. Production Test Tool

The Production Test Tool enables validation of button, LED, and GPIO functionality in the factory. It also allows for programming a serial number onto each unit if desired.

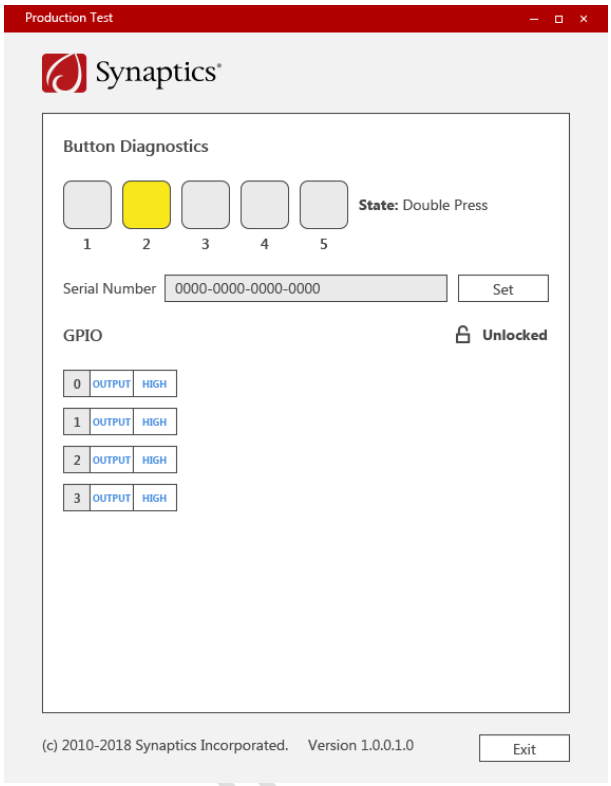


Figure 21. Production Test tool interface

13.4. FCP Tuning Application Tool and Interface

The Firmware Configuration Package (FCP) is a Windows toolset that allows the headset maker to tune and configure some features of the CX31988 based headset. More specifically, the equalizers and the DRCs can be tuned with a GUI tool in real time. The tuning can then be saved and used to generate a new firmware image with the new tuning. It is also possible to remap buttons, change USB Vendor/Product ID, and the product description strings. The FCP tools can then be used to create a new firmware image with the new settings. The FCP application also supports flashing of the firmware image directly from within the application.

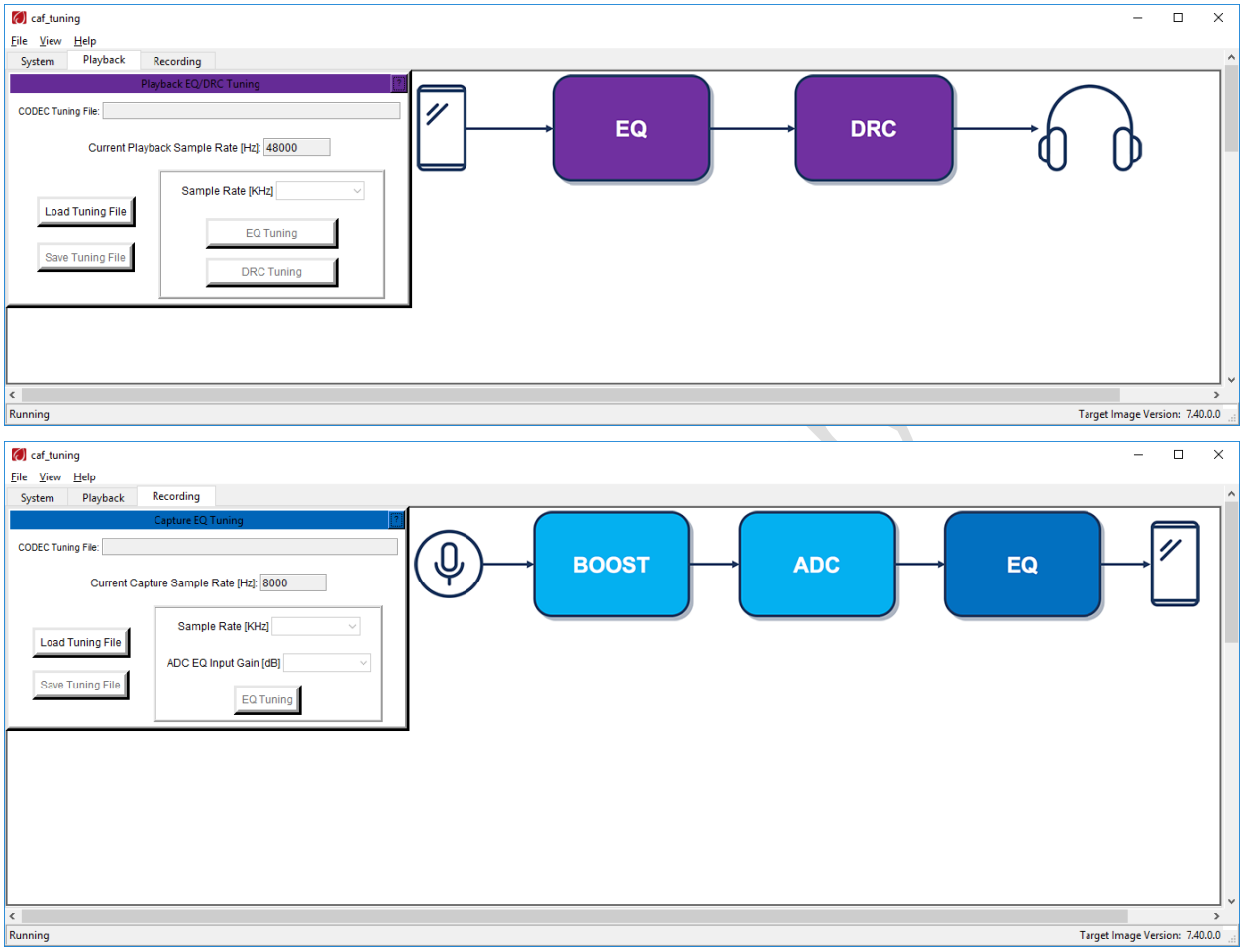


Figure 22. FCP tuning interface

13.4.1. *Tuning Equalizers*

The FCP tuning application graphical interface can be used to tune the equalizer interactively in real time. The tuning can be done by entering the equalizer parameters in text fields. The frequency and gain for each band can also be tuned interactively by moving the corresponding dots in the frequency response plot.

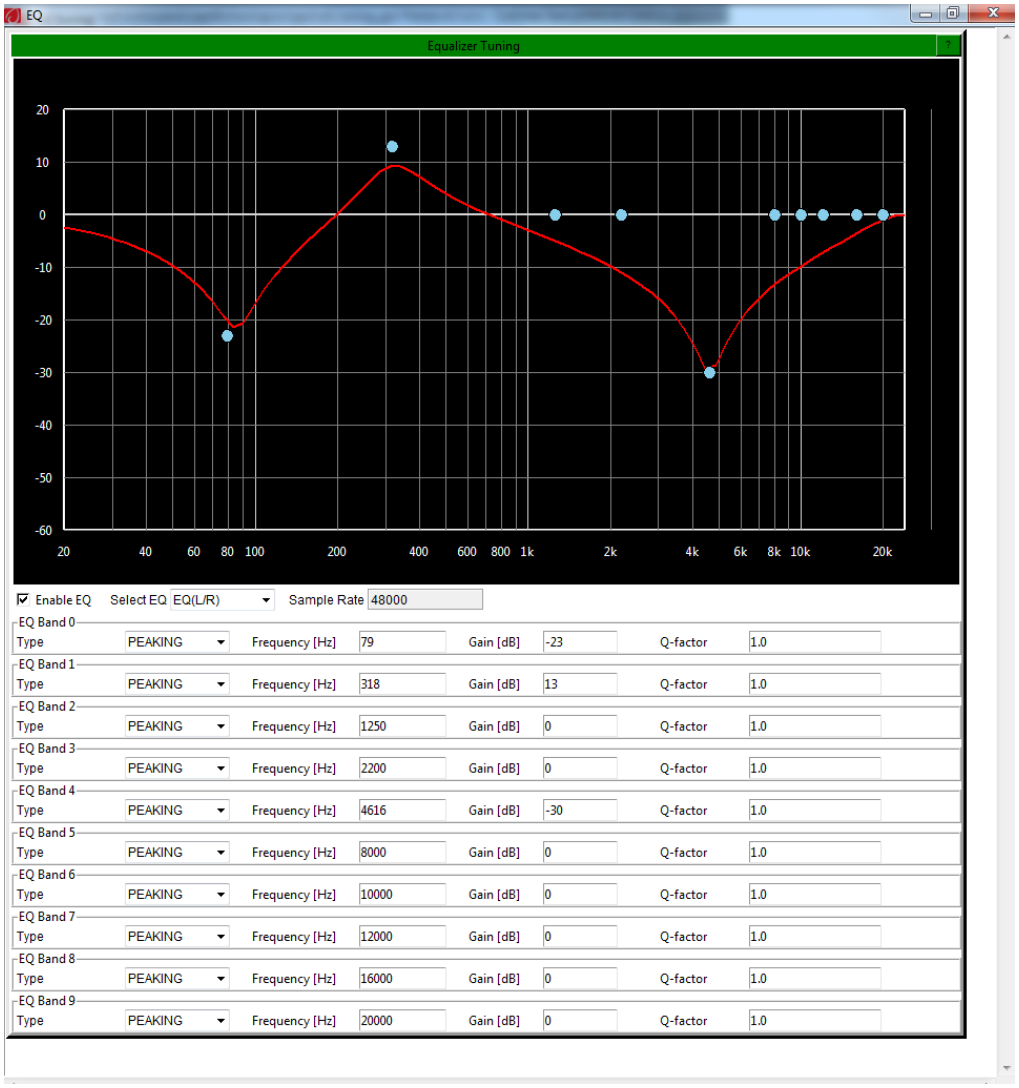


Figure 23. Tuning interface for equalizers in the FCP tuning application

13.4.2. *Tuning Dynamic Range Compression*

The FCP tuning application graphical interface can be used to tune the DRC interactively in real time. Tuning is performed by entering the DCR parameters in text fields. The input and output thresholds can also be tuned interactively by moving the corresponding dots in the response plot.

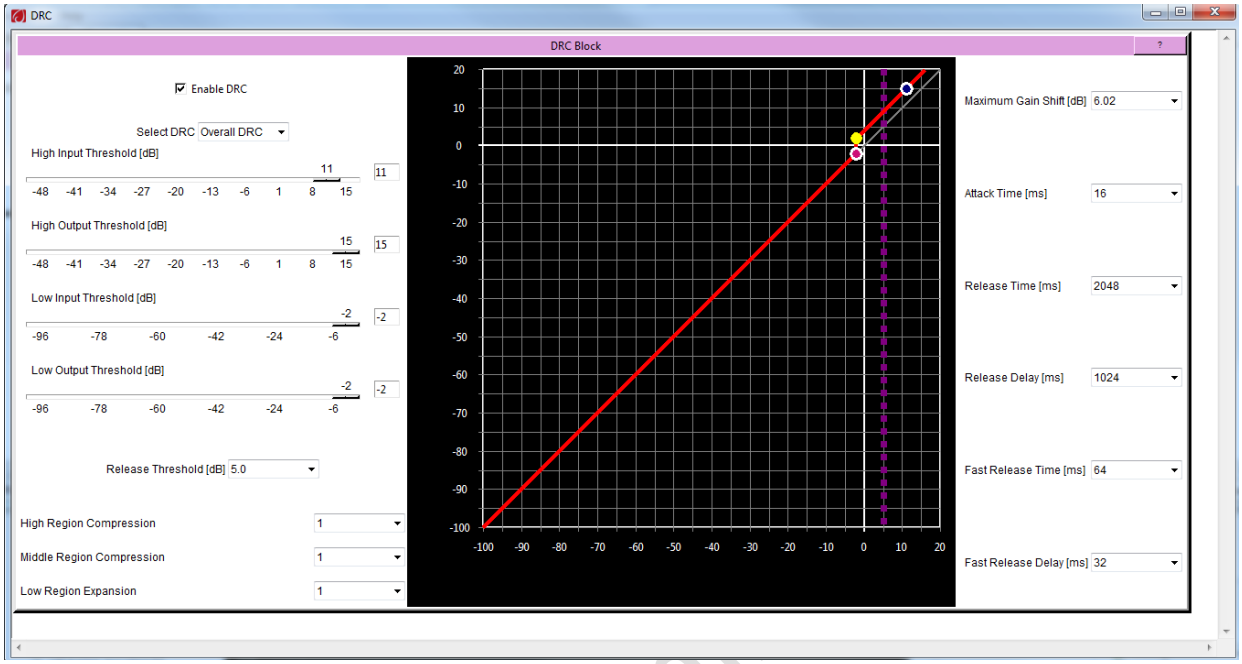


Figure 24. Tuning interface for DRC in the FCP tuning application

13.4.3. *Configure Firmware*

The FCP application can be used to reconfigure some key functionally in the firmware. The USB vendor ID (VID), product ID (PID), and product strings can be changed with the FCP application. The application can also be used to remap buttons.

13.4.4. *Creating a New Firmware Image*

The FCP application can create a new firmware image that includes all the tuning and configuration described above. This allows the headset designers to be more self-sufficient in making their own firmware images with their own tuning and configuration.

13.4.5. *Flashing Firmware Image from Tuning Application*

The FCP application can flash a new firmware image to the CX31988 device. This function makes it easier to perform iterative testing or A/B comparisons, and also allows headset designers to quickly flash their own firmware images with their own tuning and configuration settings.

14. Pin Descriptions

14.1. 49-Pin eWLB Pin Signals

Figure 25 shows the CX31988 pinout.

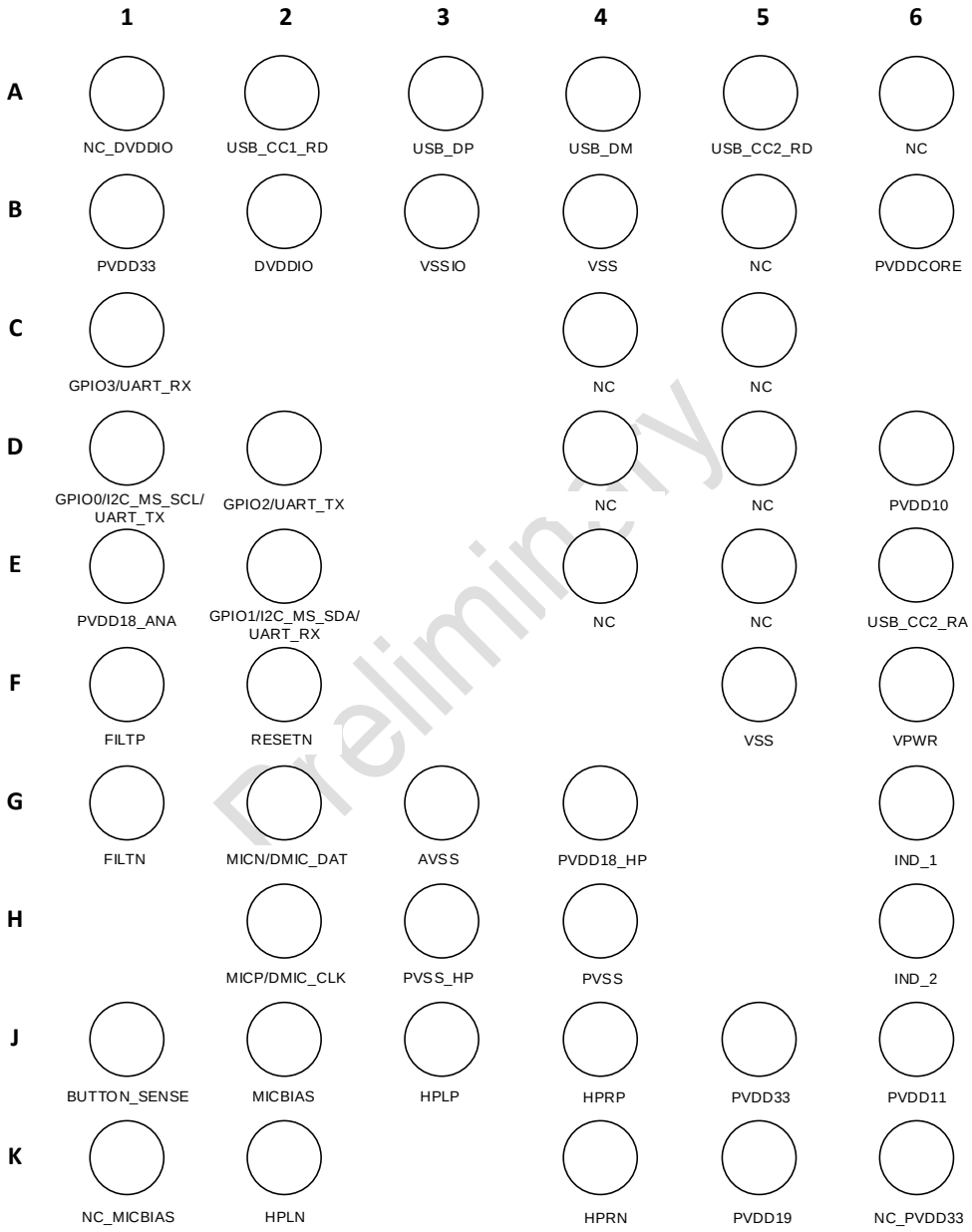


Figure 25. CX31988 49 e-WLB pin signals

Note:

Pin A1 is designated as NC_DVDDIO. The designer can route the PCB trace through this pad to Pin B2 DVDDIO.

Pin K1 is designated as NC_MICBIAS. The designer can route the PCB trace through this pad to Pin J2 MICBIAS.

Pin K6 is designated as NC_PVDD33. The designer can route the PCB trace through this pad to Pin J5 PVDD33.

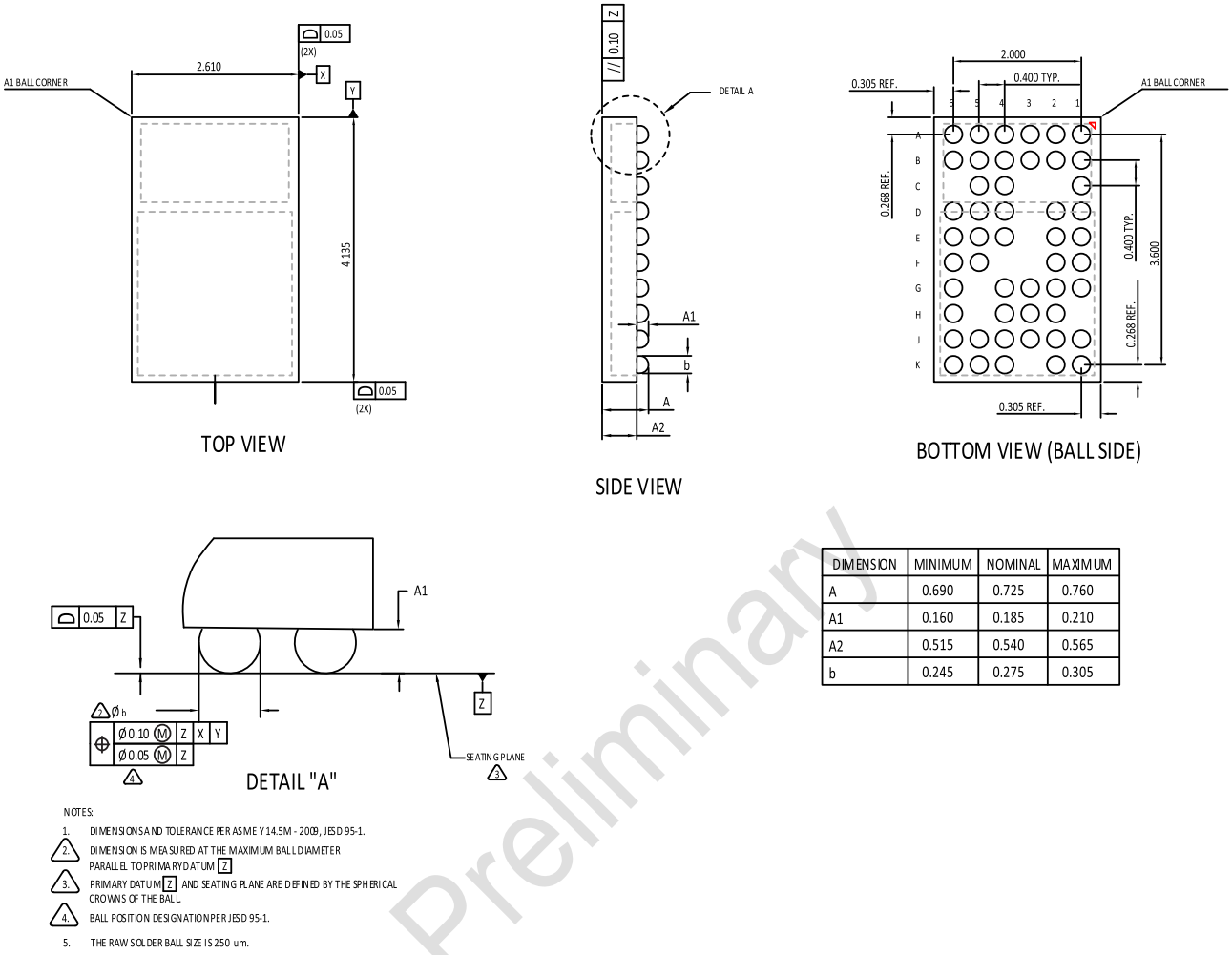
14.2. Hardware Signal Definitions

Table 16. Hardware signal definitions

Pin Name	Pin	I/O Type	Description
USB Signals			
USB_DP	A3	Digital I/O	USB differential data signal, positive
USB_DM	A4	Digital I/O	USB differential data signal, negative
USB_CC1_RD	A2	Passive	Source/sink charge control
USB_CC2_RA	E6	Passive	Pin for USB VCONN
USB_CC2_RD	A5	Passive	Source/sink charge control
Control Signals			
RESETN	F2	Digital in	Active low input asserted to initialize registers, sequencers, and signals to a consistent reset state. Internal pull-up resistor.
BUTTON_SENSE	J1	Analog in	ADC for resistive divider/button sensing
GPIO0/I2C_MS_SCL/ UART_TX	D1	Digital I/O	IO, programmable: In, out, bi, pull-up, pull- down, open-drain, tri-state, I2C, UART. Default state on power-up is tri-state.
GPIO1/ I2C_MS_SDA/ UART_RX	E2	Digital I/O	IO, programmable: In, out, bi, pull-up, pull- down, open-drain, tri-state, I2C, UART. Default state on power-up is tri-state.
GPIO2/UART_TX	D2	Digital I/O	IO, programmable: In, out, bi, pull-up, pull- down, UART Default state on power-up is tri-state.
GPIO3/UART_RX	C1	Digital I/O	IO, programmable: In, out, bi, pull-up, pull- down, UART. Default state on power-up is tri-state.
Microphone and Headphone Interfaces			
MICP/ DMIC_CLK	H2	Analog in Digital Out	Default function: Positive differential input for analog microphone Alternate function: Digital microphone clock output
MICN/ DMIC_DAT	G2	Analog in Digital In	Default function: Negative differential input for analog microphone Alternate function: Digital microphone data input, supporting up to 2 microphones on single line.
HPLP	J3	Analog out	Headphone left positive differential output
HPLN	K2	Analog out	Headphone left negative differential output
HPRP	J4	Analog out	Headphone left positive differential output
HPRN	K4	Analog out	Headphone right negative differential output
Power Supplies			
VPWR	F6	Power in	Typically powered from USB Type-C VBUS or VCONN. Supplies SIMO DCDC buck/boost
PVDD33	B1	Power out	Output of IMO DCDC buck/boost

Pin Name	Pin	I/O Type	Description
DVDDIO	B2	Power in	Input generally fed via PVDD33 or PVDD19
NC_DVDDIO	A1	Power in	This pin has no connection internally. But for best PCB signal routing, the DVDDIO net can route through this pin to get to DVDDIO pin B2.
PVDD10	D6	Power out	Output from LDO from PVDD11
PVDD11	J6	Power out	Output of SIMO DCDC buck/boost
PVDD18_ANA	E1	Power out	Output from LDO from PVDD19
PVDD19	K5	Power out	Output of SIMO DCDC buck/boost
PVDD33	J5	Power out	Output of SIMO DCDC buck/boost
NC_PVDD33	K6	Power out	Pin has no connection internally. For best PCB signal routing, the PVDD33 net can route through this pin to get to PVDD33 pin J5.
PVDDCORE	B6	Power out	Output from LDO from PVDD11
PVDD18_HP	G4	Power out	Headphone PVDD18
MICBIAS	J2	Power out	Microphone bias regulator output
NC_MICBIAS	K1	Power out	Pin has no connection internally. For best PCB signal routing, the MICBIAS net can route through this pin to get to MICBIAS pin J2.
IND_1	G6	Power out	Pin for SIMO DCDC buck/boost inductor
IND_2	H6	Power out	Pin for SIMO DCDC buck/boost inductor
FILTP	F1	Power passive	Filter capacitor pin for AVDD18_ANA power reference
FILTN	G1	Power passive	Filter capacitor pin for AVDD18_ANA power reference
Ground			
PVSS_HP	H3	Power ground	Headphone GND return
VSS	F5	Power ground	SIMO DCDC buck/boost ground
VSS	B4	Power ground	SIMO DCDC buck/boost ground
PVSS	H4	Power ground	SIMO DCDC buck/boost ground
VSSIO	B3	Power ground	I/O ground
AVSS	G3	Power ground	Analog ground
NC (no connect)	A6	Digital I/O	—
NC	D4	Digital I/O	—
NC	D5	Digital I/O	—
NC	B5	Digital I/O	—
NC	C4	Digital I/O	—
NC	C5	Digital I/O	—
NC	E4	Digital I/O	—
NC	E5	Digital I/O	—

15. Package Dimensions and Thermal Specifications



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.690	0.725	0.760
A1	0.160	0.185	0.210
A2	0.515	0.540	0.565
b	0.245	0.275	0.305

Figure 26. Package dimensions 49-pin eWLB 2.610 x 4.135 mm

Table 17. Thermal specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
Operating temperature range	T_A	–40	—	85	°C
Operating junction temperature	T_J	–40	—	125	°C
Thermal resistance[1, 2] (four layer)	θ_{JA}	—	49.9	—	°C/W
Thermal resistance[1, 3] (four layer)	θ_{JA}	—	19.82	—	°C/W

1. For a given power dissipation, die temperature can be calculated as follows: $T_J = T_A$ + (power dissipated • θ_{JA}).
2. Four-layer Synaptics board specification: PCB Dimension 19 mm × 59 mm and 0.99 mm thick FR-4, top and bottom layer thickness 0.04 mm, inner plane thickness 0.03 mm.
3. Four-layer Synaptics board specification: PCB Dimension 90 mm × 100 mm and 1.6 mm thick FR-4, top and bottom layer thickness 0.04 mm, inner plane thickness 0.03 mm.

16. References and Specifications

- USB Implementers Forum, USC Type-C Specification (see https://www.usb.org/documents)
- Android 3.5 mm Headset Jack: Device Specification (see https://source.android.com/devices/accessories/headset/jack-headset-spec)
- Arm Cortex Mo+ Specifications (see https://developer.arm.com/products/processors/cortex-m/cortex-m0-plus)
- Audio Headset Specification (http://source.android.com/accessories/headset-spec.html)

17. Ordering Information

Table 18. Ordering information

Part Number	Features	Package
CX31988-10*	I²C, USB interface	49-pin eWLB

* Available for shipping as tray or reel.

The devices in this publication are lead-free (Pb-Free) and China RoHS compliant .

Contact your local Synaptics sales office for advanced software options.

18. Revision History

Revision	Description
Rev 1	Initial version
Rev 2	Comprehensive update and reorganization of document.

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