YAMAHA

CONFIDENTIAL

DD-2SP/SPR-2 Firmware
DSE Mode
Manual

Version 1.00.00

Sep. 14, 2012

Yamaha Corporation
Semiconductor Division

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1 Overview

DSE mode is one of firmware modes that run on the MDSP2 in YDA174 (DD-2SP)/YSS952 (SPR-2). To run this mode, firmware codes need to be downloaded from a host controller.

This firmware provides the following functions: I/O activity detection, surround, band extension, acoustic compensation, master volume, loudness, crossover network, power limiter and soft clip. With the help of 10-band PEQ running on SDSP realizes equalizer function. In addition, it is also possible to generate sound with the built-in FM synthesizer.

While reading this manual, refer also to “YDA174 Application Manual” or “YSS952 Application Manual”.

This firmware and firmware coefficients assume the following:

- Audio I/O setting is set to normal mode (PIO=0 at 0x07 AIFMD).
- The memory mode of WRAM (MDSP2 Work RAM) is set to 20-bit mode (WRAMMD=0 at 0x0A MDSPMD).
- The word size of the runtime transfer data is set to 16 bits (WRAMRTMD=1 at 0x0A MDSPMD).

[Note]

- In this document, the two application manuals above may be referred to as “YDA174/YSS952 Application Manual”.

1.1 Firmware

This firmware handles 2 channel audio signals and is compatible with the sampling rate of 48 kHz.
The table below shows its functional description:

Firmware Name	Abbr.	Description
Top	-	Performs run-time transfer operation.
Input Level Detector	ILD	Reports to a host controller via a register when a small signal is continuously input for more than a specified time. It also controls the selection of input paths.
Spacious sound 3D	S3D	Heightens spatial effect and realistic sensation of stereo signal with the sound field simulation processing and the wide surround processing.
Harmonics enhancer Extended	HXT	Extends audio bandwidth by generating and adding harmonic components.
Acoustic total-linear EQ core	AC	Realizes core processing of acoustic compensation. It also has an output path to SDSP 10-band PEQ.
Smooth Volume	SV	Varies the master volume smoothly. Provides the loudness function and the FM sound mixing function. It has the input path from SDSP 10-band PEQ processing.
Crossover Filter	CF	Configures 1-way, 2-way, or 2.1 digital networks in accordance with the system configuration.
Limiter	LMT	Limits the output level for each signal that was divided by the Crossover filter. It also clips waveform of low frequency range singnal smoothly.

[Note]

- In this document, these abbreviated names may be used in place of Firmware Name.
- Hereafter, “Acoustic total-linear EQ” may be referred to as “AEQ”.
- SDSP 10-band PEQ will be used for equalizer and part of acoustic compensation processing. For details of SDSP 10-band PEQ, see “YDA174/YSS952 Application Manual”.

1.2 Firmware Coefficients

Common, ready-to-use firmware coefficients are provided on the on-chip ROM. The host controller can transfer the coefficients in its entirety or part from the ROM to CRAM (MDSP2 Coefficient RAM) by specifying a preset pattern number (described later).
Moreover the host controller can transfer coefficients in its memory space to CRAM. It is not necessary to prepare and maintain coefficients for each sampling rate as in conventional DSPs, but the host controller just need to keep coefficients for 48-kHz sampling rate only.

1.3 Preset Patterns

270 of firmware coefficients on the ROM as preset patterns can be used. One preset pattern number corresponds to one ROM block number, and by calling the block number the host controller can set the relevant firmware coefficients to CRAM immediately.

1.4 Floating-point Calculation

This firmware handles audio data in 32-bit floating-point precision and coefficient data in 16-bit or 28-bit fixed-point format. This allows an appropriate dynamic range to be secured in the signal processing calculation composed of multiple stages.

[Note]

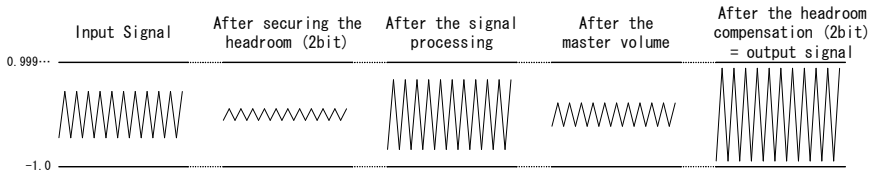
- With the Spacious sound 3D firmware, audio data is stored into the surround delay memory in 20-bit fixed-point precision.

1.5 Data Range

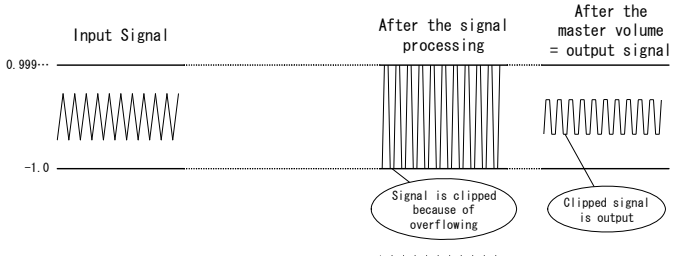
1.5.1 Audio Data

Audio data ranges from −1.0 to 1.0. In order to prevent the overflow during the arithmetic processing, appropriate headroom should be provided to the audio data. The allowable transient peaks in a series of arithmetic processing are set aside as a headroom and master volume adjustment is applied and then the headroom is restored as the last step.

An example of using headroom:



An example of not using headroom:



1.5.2 Coefficient Data

As with audio data, coefficient data also ranges from −1.0 to 1.0. Since many of firmware coefficients are beyond the range, coefficient data definition is scaled down previously. By shifting audio data up after the coefficient calculation, such scaling down is compensated.
For example, the gain coefficient at 1.0 (0dB max.) is defined by 1/2 scale as shown below.

0x0000: 0.0 (Mute)
:
0x2000: 0.25 (−6dB)
:
0x4000: 0.5 (0dB)

In this manual, such firmware coefficients are expressed as shown below:

1.6 Memory Data Transfer

The firmware and firmware coefficients can be transferred by the following methods.

On-chip RAM / Data Transfer	MPRAM (MDSP2 Command RAM)		CRAM (MDSP2 Coefficient RAM)	
	MDSP2 (inactive)	MDSP2 (active)	MDSP2 (inactive)	MDSP2 (active)
On-chip ROM → On-chip RAM (*1)	Y	N	Y	Y&R
Host → On-chip RAM	Y	N	Y	Y&R
On-chip RAM → Host	N	N	Y	Y&R

*1: When the host controller specifies a ROM block number (preset pattern), data is transferred from on-chip ROM to on-chip RAM.

Y: transfers allowed Y&R: runtime transfers allowed N: transfers not allowed

[Note]

- In the runtime transfer, firmware coefficients are read and written via WRAM0 (MDSP2 Work RAM0). The runtime transfer allows multiple words of firmware coefficients to be read and written at a time without sound interruption.
- For details of the access method to an on-chip RAM and of runtime transfer method, see "YDA174/YSS952 Application Manual" and "4.2 Runtime Transfer".

1.7 Processing Latency

This firmware processes the signal in every sampling period. The I/O delay of audio signals in MDSP2 is 1 sample time.
The table below shows the processing Latency of the whole DD-2SP/SPR-2.

Block	Processing	Latency (Decimation)	Latency (Interpolation)
AIF	-	2 [fsi]	
SDSP	SRC + De-emphasis	8±1 [fso]	(23±1) × fso / fsi [fso]
MDSP2	Processing before 10-bands PEQ	1 [fso]	
SDSP	10-bands PEQ	1 [fso]	
MDSP2	Processing after 10-bands PEQ	1 [fso]	
SDSP	DC block + OSF	23 [fso]	
DAIF	GAIN + PLIMIT + LPF	Approx. 1 [fso]	
Digital Amplifier	-	Approx. 6 μs (with LC filters), Approx. 1 μs (without LC filters)	

fsi: input sampling rate (to DD-2SP/SPR-2) fso: output sampling rate time (from DD-2SP/SPR-2) of 48 kHz

[Note]

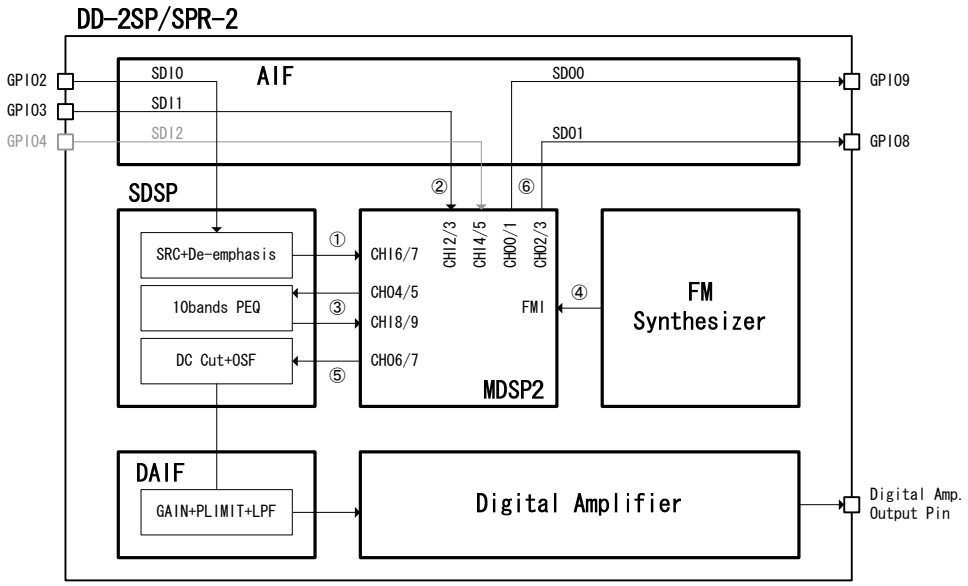
- In the above table, the latency of DC block + OSF Processing (SDSP), GAIN + PLIMIT + LPF Processing (DAIF), and Digital Amplifier arises only on analog output path in DD-2SP. (This latency will not be in its digital output path.)
- If FIR filter etc. exists in MDSP2 firmware, the latency of the output signals varies depending on the filter characteristics. Usually, delay of 128[fso] occurs in the FIR processing in Acoustic total-linear EQ core firmware.
- When a path not using SDSP 10-band PEQ is selected, the amount of SDSP 10-band PEQ delay becomes 0 and that of MDSP2 becomes 1[fso] in all.

2 Detailed Explanation

2.1 Audio Signal Input and Output

This chapter shows the audio signal flow in DD-2SP/SPR-2.

2.1.1 AIF Mode=0



① The audio signal from GPIO2 pin is input into MDSP2 through SRC+De-emphasis processing (SDSP).

② The audio signal from GPIO3 pin is directly input into MDSP2 (not via SDSP).
In this firmware MDSP's input stage selects either signal of ① or ②.

③ And it is output from MDSP2 once again and returned after 10-band PEQ processing (SDSP).

④ FM sound signals are mixed with it.

⑤ If all MDSP2 processings are completed, the following processings will be applied to audio signals in the SDSP: DC-block, OSF (over-sampling filter), and GAIN, PLIMIT, LPF (DAIF: Interface with the digital amplifier). And the result is output in analog format from the digital amplifier.

⑥ The audio signal is output from GPIO8 or GPIO9 pin in digital format.

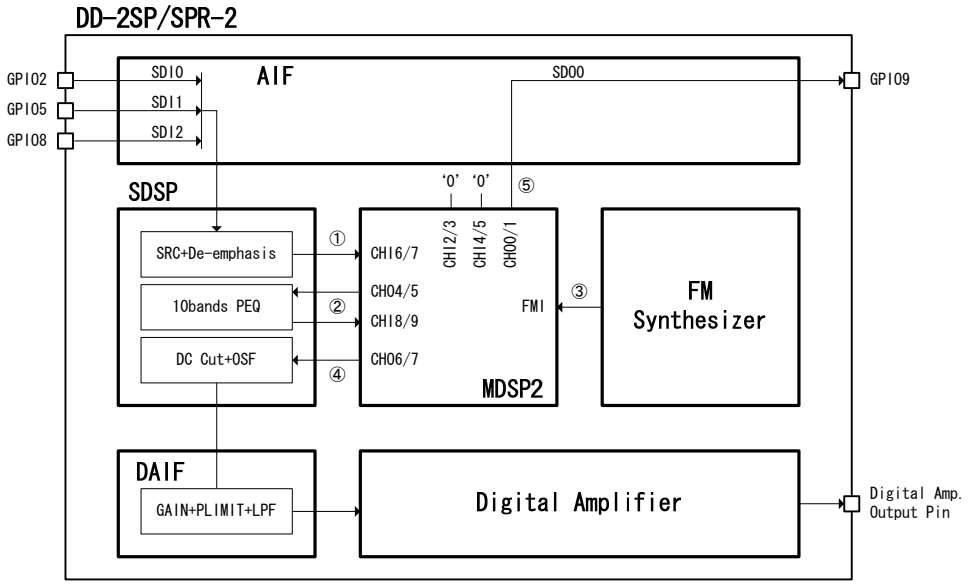
[Note]

- In SPR-2, an audio signal is not outputted from an analog output path (path of above ⑤).
- GPIO2 pin can receive an asynchronous audio signal with respect to DD-2SP/SPR-2. A synchronous audio signal (external A/D converter output etc.) with respect to DD-2SP/SPR-2 should be input into GPIO3 pins.

The table below shows the relationship between signals, GPIO I/O pins, and the digital amplifier output pin:

Signal	GPIO2	GPIO3	GPIO8	GPIO9	Digital Amp.
Input (via SRC)	✓				
Input (External A/D converter input etc.)		✓			
Output or high frequency range signal output				✓	✓
Low frequency range signal output			✓		

2.1.2 AIF Mode=1/2/3



① The audio signal from GPIO2, GPIO5, or GPIO8 pin is input into MDSP2 through SRC+De-emphasis processing (SDSP). The AIF mode setting selects one of the above three inputs.

② And it is output from MDSP2 once and returned after 10-band PEQ processing (SDSP).

③ FM sound signals are mixed with it.

④ If all MDSP2 processings are completed, the following processings will be applied to audio signals in the SDSP: DC-block, OSF (over-sampling filter), and DAIF (Interface with the digital amplifier). And the result is output in analog format from the digital amplifier.

⑤ The audio signal is output from GPIO9 pin in digital format.

[Note]

- In SPR-2, an audio signal is not outputted from an analog output path (path of above ④).

The table below shows the usage of GPIO pins and digital amplifier output pins:

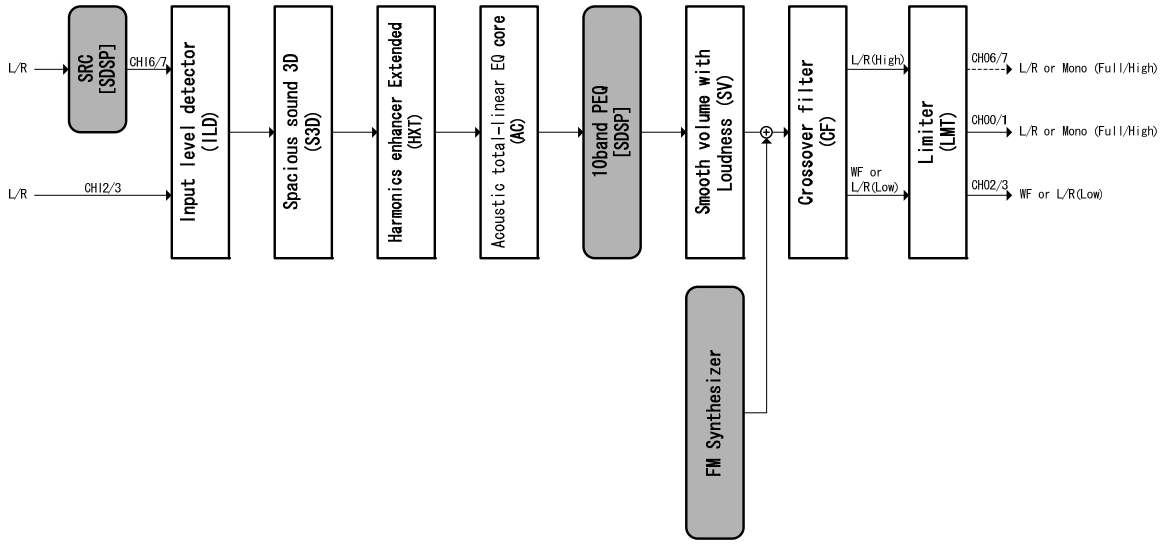
Signal	GPIO2	GPIO3	GPIO8	GPIO9	Digital Amp.
Input (via SRC)	✓	✓	✓		
Output or high frequency range signal output				✓	✓
Low frequency range signal output				✓	

2.2 Block Diagram

The figure below shows the block diagram of the firmware.

[Note]

- Top firmware not related to signal processing is omitted.
- The gray box shows processing except the MDSP2 firmware.
- 10-band PEQ block is used in acoustic compensation and equalizer.
- The dotted path line (to CHO6/7) is enabled in DD-2SP only.



2.3 Firmware

2.3.1 Overview

2.3.1-1 Instruction Codes

Write instruction codes of this firmware to MPRAM (MDSP2 program RAM).

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name
0	0x4400	H	39–00	-
1	0x4401	H	39–00	-
:	:	:	:	:
1,533	0x49FD	H	39–00	-
1,534	0x49FE	H	39–00	-

[Note]

- When DD-2SP/SPR-2 start up, all MPRAM area is zeroed.
- "H" in MDSP2 column indicates the bits should be transferred while MDSP2 is stopped.

2.3.2 Top

This is the firmware that realizes the runtime transfer function.
For details of the procedure to execute this runtime transfer, see "4.2 Runtime Transfer".

2.3.2-1 Control Register

0x13 MDSPREQ Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MDSPREQ7	MDSPREQ6	MDSPREQ5	MDSPREQ4	MDSPREQ3	MDSPREQ2	MDSPREQ1	MDSPREQ0

- **MDSPREQ[7:0]**

This register requests the runtime transfer.
(Initial value)
0x00
(When written)
0x02: This requests a write operation to CRAM
0x03: This requests a read operation from CRAM
Other values: Reserved
(When read)
0x00: a runtime transfer has been completed
0x02: data is now transferred to CRAM
0x03: data is now transferred from CRAM
Other values: Reserved

2.3.2-2 Control Data

The control data is located in WRAM0 (MDSP2 Work RAM0).

No.	On-chip RAM Address	Bit Position	Bit Name
0	0x0000	31–26	0
		25–16	RtStartAdr[9:0]
1	0x0001	31–20	0
		19–16	RtCnt[3:0]
2	0x0002	31–16	RtData0[15:0]
3	0x0003	31–16	RtData1[15:0]
4	0x0004	31–16	RtData2[15:0]
5	0x0005	31–16	RtData3[15:0]
6	0x0006	31–16	RtData4[15:0]
7	0x0007	31–16	RtData5[15:0]
8	0x0008	31–16	RtData6[15:0]
9	0x0009	31–16	RtData7[15:0]
10	0x000A	31–16	RtData8[15:0]
11	0x000B	31–16	RtData9[15:0]

[Note]

- Only the high-order 16 bits of WRAM0 is used. (WRAMRTMD=1 at 0x0A MDSPMD)
- "0" in the Bit Name column is the reserved bits. Write "0" into these bits during the write access. When reading the bit, an undefined value is read.

● RtStartAdr[9:0]

This bit specifies a start address of the write destination or read source on CRAM.

(Initial value)

0x000

(When written)

0x000: CRAM[0]

0x001: CRAM[1]

:

0x3FF: CRAM[1023]

(When read)

Hold data

(Note)

Specify an address not by CRAM internal address (0x4000 to 0x43FF) but by CRAM relative address (0x000 to 0x3FF).

● RtCnt[3:0]

This bit specifies the information of the number of words to transfer.

(Initial value)

0x0

(When written)

0x0: 1 word

0x1: 2 words

:

0x9: 10 words

Other values: Reserved

(When read)

Hold data

- **RtData*[15:0] (*=0–9)**

This bit is the buffer for the transferred data to be written or read.

(Initial value)

0x0000

(When written)

The content of this bit will be written into CRAM

(When read)

The content of this bit is read from CRAM

2.3.2-3 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name
0	0x4000	H	15–00	TopData0[15:0]
1	0x4001	H	15−00	TopData1[15:0]
2	0x4001	H	15−00	TopData2[15:0]
3	0x4003	H	15−00	TopData3[15:0]
4	0x4004	H	15−00	TopData4[15:0]
5	0x4005	H	15–00	TopData5[15:0]
6	0x43FF		15–00	FWMode[15:0]

[Note]

- "H" in the MDSP2 column indicates the bits should be transferred while MDSP2 is being stopped. A blank cell in the column indicates it can be transferred whether MDSP2 is stopped or not.
- The on-chip RAM address of No.5 and 6 are discontinuous.

● TopData*[15:0] (*=0/1/2/3/4/5)

Data required for this firmware operation should be written.

(Initial value)

0x0000

(When written)

The following value should be set to each bits.

TopData0[15:0]: 0x4000 (fixed)

TopData1[15:0]: 0x2000 (fixed)

TopData2[15:0]: 0x8000 (fixed)

TopData3[15:0]: 0xC000 (fixed)

TopData4[15:0]: 0x0008 (fixed)

TopData5[15:0]: 0x0001 (fixed)

(When read)

Hold data

(Note)

Set TopData*[15:0] bit only once when this firmware is initialized.

● FWMode[15:0]

A value peculiar to this firmware is displayed.

(Initial value)

0x0000

(When written)

Writing is prohibited.

(When read)

0x110E (fixed)

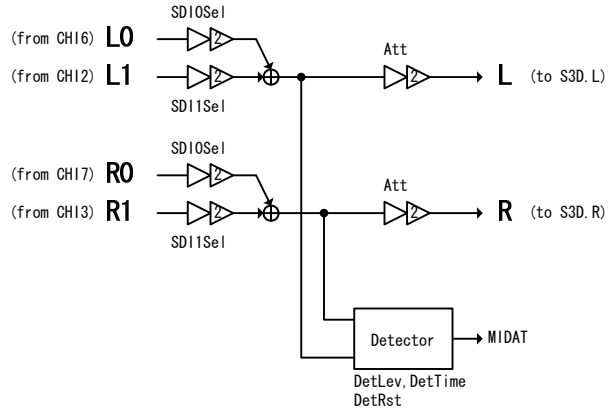
(Note)

After setting up instruction code and operating MDSP2, this bit value is displayed.

2.3.3 Input level detector

Input level detector will report to a host controller via a register if a small signal is continuously input for more than a specified time. It also controls the input signal selection.

2.3.3-1 Signal Flow



[Note]

- Detector will set valid values (input activity detected) to MIDAT[7:0] (0x16 MIDAT) if a signal lower than a detection level is input for more than a specified time; otherwise, Detector will set invalid values (no input activity detected) to MIDAT[7:0].

2.3.3-2 Control Register

0x16 MIDAT Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MIDAT7	MIDAT6	MIDAT5	MIDAT4	MIDAT3	MIDAT2	MIDAT1	MIDAT0

- **MIDAT[7:0]**

This register reports that a small signal is detected.

(Initial value)

0x00

(When written)

Writing is prohibited

(When read)

0x00: A small signal is not detected

0x01: A small signal is detected

Other values: Reserved

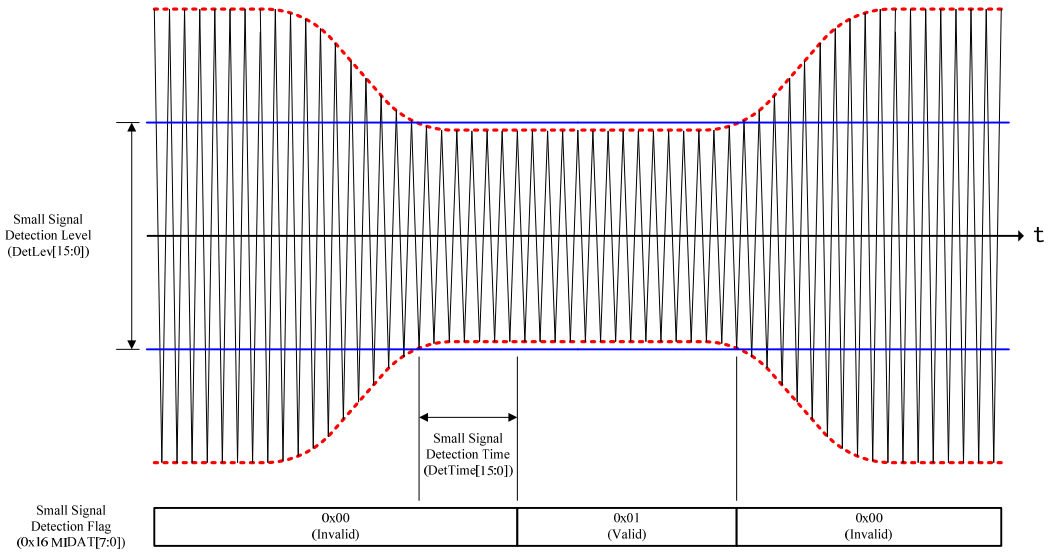
(Note)

- Small signal detecting conditions are as follows:

  Detected: A signal with the amplitude lower than the detection level (specified with DetLev[15:0] (described later)) is continuously being input for more than the period of time specified with DetTime[15:0] (described later).

  Not detected: Other then the above.

- The figures below show small signal detection.



2.3.3-3 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name
0	0x400B		15–00	SDI0Sel[15:0]
1	0x400C		15–00	SDI1Sel[15:0]
2	0x400D		15–00	Att[15:0]
3	0x400E		15–00	DetLev[15:0]
4	0x400F		15–00	DetTime[15:0]
5	0x4010		15–00	DetRst[15:0]

[Note]

- MDSP2 column without any letter (blank) indicates the bits can be transferred whether MDSP2 is stopped or not.

● SDI*Sel[15:0] (*=0/1)

This bit specifies an input gain value of SDI0 or SDI1 audio signals.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 (Mute) and 0x7FFF (+6 dB) as in;

0x0000: 0.00 (Mute)
0x0666: 0.05 (−20 dB)
0x0CCD: 0.10 (−14 dB)
0x1333: 0.15 (−10 dB)
0x199A: 0.20 (−8 dB)
0x2000: 0.25 (−6 dB)
0x2666: 0.30 (−4 dB)
0x2CCD: 0.35 (−3 dB)
0x3333: 0.40 (−2 dB)
0x399A: 0.45 (−1 dB)
0x4000: 0.50 (0 dB)
0x7FFF: 0.999 (+6 dB)

(When read)

Hold data

(Note)

- For usual applications, use 0x4000 for SDI0Sel[15:0], and 0x0000 for SDI1Sel[15:0] to use the SDI0 input signal.
- For usual applications, use 0x0000 for SDI0Sel[15:0], and 0x4000 for SDI1Sel[15:0] to use the SDI1 input signal.

● Att[15:0]

This bit specifies the headroom required for the processing after Input level detector firmware.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 and 0x4000 as in;

0x0001: 14-bit headroom

:

0x0800: 3-bit headroom

0x1000: 2-bit headroom

0x2000: 1-bit headroom

0x4000: No headroom

(When read)

Hold data

(Note)

- When this bit is set to 0x0000 (Initial value), Input level detector firmware output is muted.
- Use 0x0800 setting for usual applications.

● DetLev[15:0]

This bit specifies the detection level of a small signal or disables the detection of such signals.

(Initial value)

0x0000

(When written)

0x0000: Disables the detection of a small signal

0x0001: Enables the detection of a small signal. Its detection level is 2^{-15} (−90.3 dBFS)

:

0x4000: Enables the detection of a small signal. Its detection level is 0.5 (−6.02 dBFS)

:

0x7FFF: Enables the detection of a small signal. Its detection level is 0.999 (≒0 dBFS)

Other values: Reserved

(When read)

Hold data

(Note)

If the detection is disabled, MIDAT[7:0] will be automatically set to 0x00 and DetRst[15:0](described later) is automatically set to 0x0000.

- **DetTime[15:0]**

This bit specifies a threshold duration in sample unit for determining that a small signal is detected.

(Initial value)

0x0000

(When written)

0x0000: 1 sample (0.02 ms)

0x0001: 1 sample (0.02 ms)

:

0x0030: 48 sample (1ms)

:

0x7FFE: 32,766 sample (683 ms)

Other values: Reserved

(When read)

Hold data

(Note)

When this bit is set to 0x0000 (Initial value), the threshold duration is considered to be 1 sample (equivalent to 0x0001).

- **DetRst[15:0]**

This bit resets the small signal detection processing.

(Initial value)

0x0000

(When written)

0x0000: Resets the detection processing

Other values: Reserved

(When read)

Undefined value will be read.

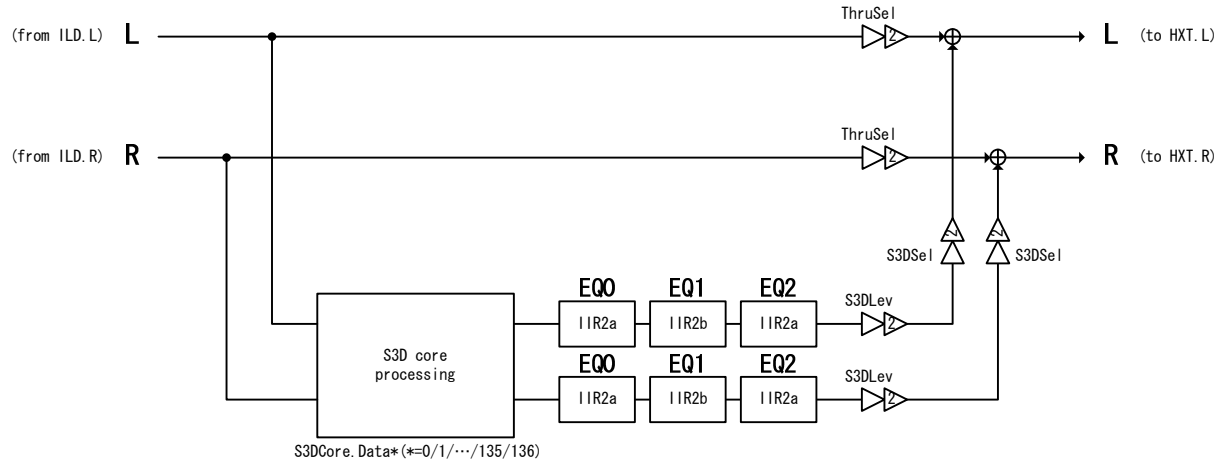
(Note)

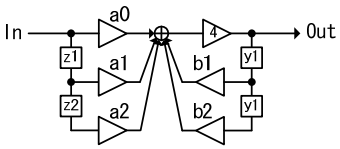
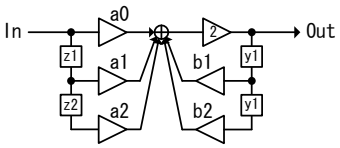
- If this bit is set to 0x0000 while DetLev[15:0] is set to a value other than 0x0000, the past information about the number of samples detected will be cleared and the detection processing will start from the beginning. At this time, the detection flag (MIDAT[7:0]) is set to 0x00 (not detected).
- This bit is automatically set to 0x0000 if DetLev[15:0] is set to 0x0000.

2.3.4 Spacious sound 3D

Spacious sound 3D enhances spatial effects and true to life perceptions of stereo signal with the sound field simulation processing and the wide surround processing.

2.3.4-1 Signal Flow



IIR2a		Out = {(a0 * In) + (a1 * z1) + (a2 * z2) + (b1 * y1) + (b2 * y2)} * 4
IIR2b		Out = {(a0 * In) + (a1 * z1) + (a2 * z2) + (b1 * y1) + (b2 * y2)} * 2

2.3.4-2 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x409D		15-00	S3DCore	Data0[15:0]
1	0x409E		15-00		Data1[15:0]
:	:	:	:		:
135	0x4124		15-00		Data135[15:0]
136	0x4125		15-00		Data136[15:0]
137	0x4126		15-00	EQ0	a0[15:0]
138	0x4127		15-00		a1[15:0]
139	0x4128		15-00		a2[15:0]
140	0x4129		15-00		b1[15:0]
141	0x412A		15-00		b2[15:0]
142	0x412B		15-00	EQ1	a0[15:0]
143	0x412C		15-00		a1[15:0]
144	0x412D		15-00		a2[15:0]
145	0x412E		15-00		b1[15:0]
146	0x412F		15-00		b2[15:0]
147	0x4130		15-00	EQ2	a0[15:0]
148	0x4131		15-00		a1[15:0]
149	0x4132		15-00		a2[15:0]
150	0x4133		15-00		b1[15:0]
151	0x4134		15-00		b2[15:0]
152	0x4135		15-00	S3DLev[15:0]	
153	0x4136		15-00	ThruSel[15:0]	
154	0x4137		15-00	S3DSel[15:0]	

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.
- The coefficients of a filter should be set at a time.

● S3DCore.Data*[15:0] (*=0/1/…/135/136)

These bits specify coefficients for S3D core processing block.

(When written)

The coefficients of our offer should be set.

(When read)

Hold data

● EQ*.a0[15:0], a1[15:0], a2[15:0], b1[15:0], b2[15:0] (*=0/2)

These bits specify EQ* filter coefficients.

(Initial value)

0x0000

(When written)

2nd-order IIR filter coefficient. Set the designed value multiplied by 1/4.

(When read)

Hold data

- **EQ1.a0[15:0], a1[15:0], a2[15:0], b1[15:0], b2[15:0]**

These bits specify EQ1 filter coefficients.

(Initial value)

0x0000

(When written)

2nd-order IIR filter coefficient. Set the designed value multiplied by 1/2.

(When read)

Hold data

- **S3DLev[15:0]**

This bit specifies output level of Spacious 3D processing signal.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6dB)

:

0x4000: 0.5 (0dB)

:

0x7FFF: 0.999… (+6dB)

Other values: Reserved

(When read)

Hold data

- **ThruSel[15:0], S3DSSel[15:0]**

These bits specify effect.

(Initial value)

0x0000

(When written)

ThruSel[15:0]=0x4000 (0dB), S3DSel[15:0]=0x0000 (Mute): Effect not applied

ThruSel[15:0]=0x0000 (Mute), S3DSel[15:0]=0x4000 (0dB): Effects applied

Other values: Reserved

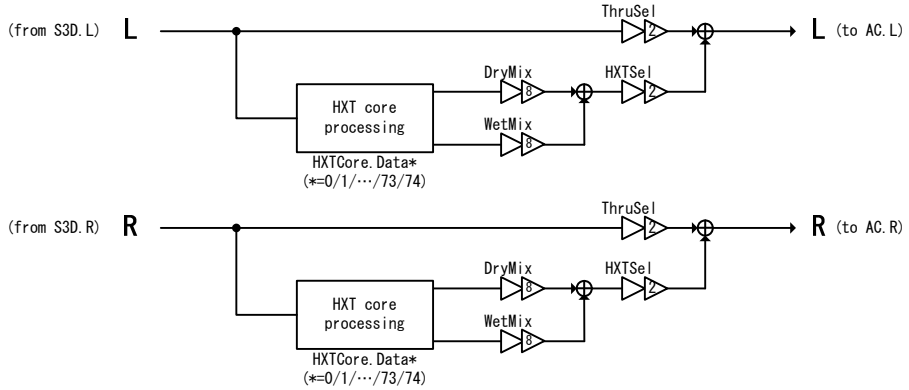
(When read)

Hold data

2.3.5 Harmonics enhancer Extended

Audio bandwidth is extended by generating and adding the harmonics components.

2.3.5-1 Signal Flow



[Note]

- HXT core processing blocks generate and output the harmonics components.

2.3.5-2 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x4149		15-00	HXTCore	Data0[15:0]
1	0x414A		15-00		Data1[15:0]
:	:	:	:		:
73	0x4192		15-00		Data73[15:0]
74	0x4193		15-00		Data74[15:0]
75	0x4194		15-00	DryMix[15:0]	
76	0x4195		15-00	WetMix[15:0]	
77	0x4196		15-00	ThruSel[15:0]	
78	0x4197		15-00	HXTSel[15:0]	

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.

● HXTCore.Data*[15:0] (*=0/1/2/.../73/74)

This bit specifies coefficients for HXT core processing block.

(Initial value)

0x0000

(When written)

The coefficients of our offer should be set.

(When read)

Hold data

● DryMix[15:0]

This bit specifies mix gain for audio signal that is output from HXT core processing block.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x1000: 0.125 (0dB)

:

0x4000: 0.5 (+12dB)

:

0x7FFF: 0.999 (+18dB)

Other values: Reserved

(When read)

Hold data

- **WetMix[15:0]**

This bit specifies mix gain for harmonics component that is output from HXT core processing block.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x1000: 0.125 (0dB)

:

0x4000: 0.5 (+12dB)

:

0x7FFF: 0.999 (+18dB)

Other values: Reserved

(When read)

Hold data

- **ThruSel[15:0], HXTSel[15:0]**

These bits specify effect.

(Initial value)

0x0000

(When written)

ThruSel[15:0]=0x4000 (0dB), HXTSel[15:0]=0x0000 (Mute): Effect not applied

ThruSel[15:0]=0x0000 (Mute), HXTSel[15:0]=0x4000 (0dB): Effect applied

Other values: Reserved

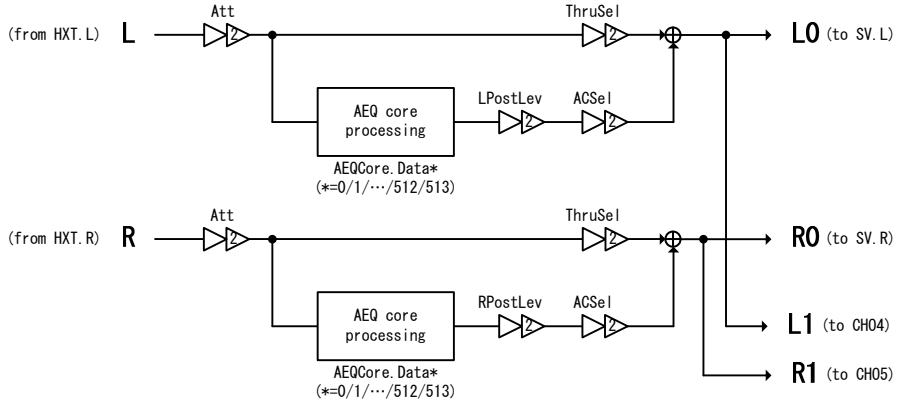
(When read)

Hold data

2.3.6 Acoustic total-linear EQ core

Acoustic total-linear EQ core firmware realizes core processing of acoustic compensation. And, it also has an output path to SDSP 10-band PEQ.

2.3.6-1 Signal Flow



2.3.6-2 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x41F2		15-00	Att[15:0]	
1	0x41F3		15-00	AEQCore	Data0[15:0]
2	0x41F4		15-00		Data1[15:0]
:	:	:	:		:
513	0x43F3		15-00		Data512[15:0]
514	0x43F4		15-00		Data513[15:0]
515	0x43F5		15-00	LPostLev[15:0]	
516	0x43F6		15-00	RPostLev[15:0]	
517	0x43F7		15-00	ThruSel[15:0]	
518	0x43F8		15-00	ACSel[15:0]	

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.

● Att[15:0]

This bit specifies the headroom required for processing after Acoustic total-linear EQ core firmware.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 and 0x4000 as in;

0x0001: 14-bit headroom

:

0x1000: 2-bit headroom

0x2000: 1-bit headroom

0x4000: No headroom

(When read)

Hold data

(Note)

- When this bit is set to 0x0000 (Initial value), Acoustic total-linear EQ core firmware output is muted.
- Use 0x0010 setting for usual applications.

● AEQCore.Data*[15:0] (*=0/1/2/.../512/513)

This bit specifies coefficients for AEQ core processing block.

(Initial value)

0x0000

(When written)

The coefficients of our offer should be set.

(When read)

Hold data

- ***PostLev[15:0] (*=L/R)**

This bit specifies an output gain.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x4000: 0.5 (0dB)

:

0x7FFF: 0.999 (+6dB)

Other values: Reserved

(When read)

Hold data

- **ThruSel[15:0], ACSel[15:0]**

These bits specify whether or not to bypass the processing in AEQ core processing block.

(Initial value)

0x0000

(When written)

ThruSel[15:0]=0x4000 (0dB), ACSel[15:0]=0x0000 (Mute): Bypass AEQ core processing

ThruSel[15:0]=0x0000 (Mute), ACSel[15:0]=0x4000 (0dB): Select AEQ core processing output

Other values: Reserved

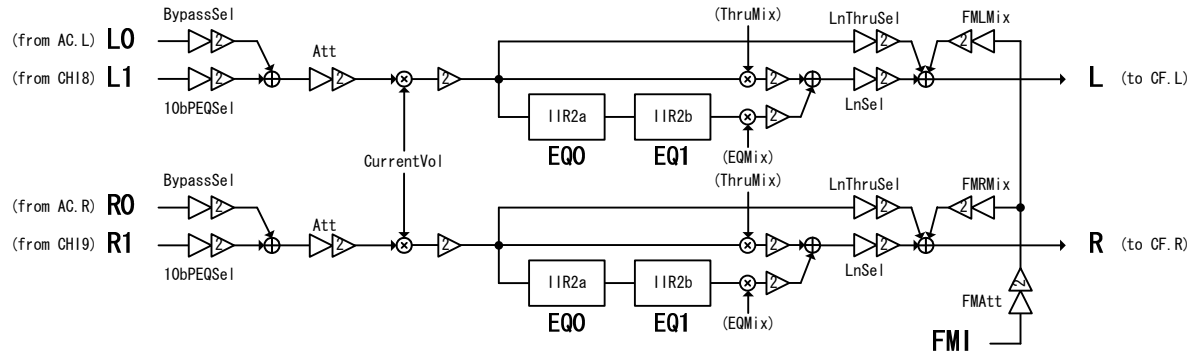
(When read)

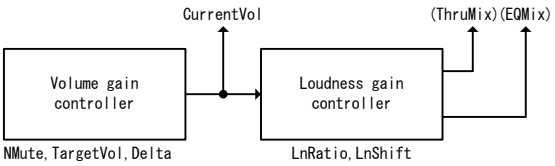
Hold data

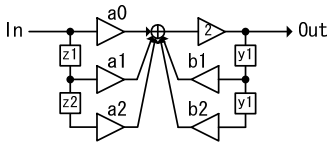
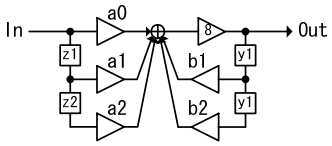
2.3.7 Smooth volume

This firmware varies the master volume smoothly. And it has the following functions as well: loudness function, FM sound mixing function. In addition, this firmware has the input paths from SDSP 10-band PEQ processing.

2.3.7-1 Signal Flow





IIR2a		Out = {(a0 * In) + (a1 * z1) + (a2 * z2) + (b1 * y1) + (b2 * y2)} * 2
IIR2b		Out = {(a0 * In) + (a1 * z1) + (a2 * z2) + (b1 * y1) + (b2 * y2)} * 8

[Note]

- The Volume gain controller shown above outputs the current volume value based on the target volume value and its change speed.
- The Loudness gain controller outputs the mix gain value for the loudness control (loudness-compensation equalizer) from the current volume value.
- The output level of the Smooth volume firmware is multiplied by 1/4. And, 4 times multiplication in the Crossover filter firmware will compensate this reduction.

2.3.7-2 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x4034		15–00	Att[15:0]	
1	0x4035		15–00	FMAtt[15:0]	
2	0x4036		15–00	FMLMix[15:0]	
3	0x4037		15–00	FMRMix[15:0]	
4	0x403B		15–00	NMute[15:0]	
5	0x403C		15–00	CurrentVol[27:12]	
6	0x403D		15–12 11–00	0 CurrentVol[11:0]	
7	0x403E		15–00	TargetVol[27:12]	
8	0x403F		15–12 11–00	0 TargetVol[11:0]	
9	0x4040		15–00	Delta[27:12]	
10	0x4041		15–12 11–00	0 Delta[11:0]	
11	0x4042		15–00	BypassSel[15:0]	
12	0x4043		15–00	10bPEQSel[15:0]	
13	0x4044		15–00	EQ0	a0[15:0]
14	0x4045		15–00		a1[15:0]
15	0x4046		15–00		a2[15:0]
16	0x4047		15–00		b1[15:0]
17	0x4048		15–00		b2[15:0]
18	0x4049		15–00	EQ1	a0[15:0]
19	0x404A		15–00		a1[15:0]
20	0x404B		15–00		a2[15:0]
21	0x404C		15–00		b1[15:0]
22	0x404D		15–00		b2[15:0]
23	0x404E		15–00	LnRatio[15:0]	
24	0x404F		15–00	LnShift[15:0]	
25	0x4050		15–00	LnSel[15:0]	
26	0x4051		15–00	LnThruSel[15:0]	

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.
- “0” in the Bit Name column is the reserved bits. Write “0” into these bits during the write access. When reading the bit, an undefined value is read.
- The coefficients of a filter should be set at a time.
- The on-chip RAM addresses are discontinuous between No.3 and No.4.

- **Att[15:0]**

This bit specifies the headroom required for the processing after Smooth volume firmware.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 and 0x4000 as in;

0x0001: 14-bit headroom

:

0x0800: 3-bit headroom

0x1000: 2-bit headroom

0x2000: 1-bit headroom

0x4000: No headroom

(When read)

Hold data

(Note)

- When this bit is set to 0x0000 (Initial value), Smooth volume firmware output is muted.
- Use 0x0800 setting for usual applications.

- **FMAtt[15:0]**

This value specifies the headroom for the FM sound signal.

It is meant to be matched to the corresponding value for the audio signal, to make their sound levels compatible to each other.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 and 0x4000 as in;

0x0001: 14-bit headroom

:

0x0010: 10-bit headroom

:

0x1000: 2-bit headroom

0x2000: 1-bit headroom

0x4000: No headroom

(When read)

Hold data

(Note)

- When this bit is set to 0x0000 (Initial value), the FM sound signal is muted.
- When mixing the audio signal and the FM sound signal, the audio signal level is getting smaller due to secured headroom (usually 8-bit) and scale down (usually 2-bit) by Smooth volume firmware. To clear this issue, total bit of headroom and scale down (usually 10-bit = 0x0010) should be set to this bit.

- **FM*Mix[15:0] (*=L/R)**

This bit specifies a L/R distribution gain of FM sound signals.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6dB)

:

0x4000: 0.5 (0dB)

Other values: Reserved

(When read)

Hold data

- **NMute[15:0]**

This bit specify whether or not to mute the volume.

(Initial value)

0x0000

(When written)

0x4000: The mute is released (The volume return to TargetVol[27:0] value).

0x0000: The volume is muted.

(When read)

Hold data

(Note)

When this bit is set to0x0000 (Initial value), Smooth volume firmware output is muted.

- **CurrentVol[27:0]**

This bit displays the current volume value.

(Initial value)

0x0000000

(When written)

Writing is prohibited.

(When read)

0x0000000: 0.0 (Mute)

0x0000001: 2^{-27} (−144dB)

:

0x1000000: 0.125 (0dB)

:

0x7FFFFFF: 0.999 (+18dB)

- **TargetVol[27:0]**

This bit specifies a target volume value.

(Initial value)

0x0000000

(When written)

0x0000000: 0.0 (Mute)

0x0000001: 2^{-27} (−144dB)

:

0x1000000: 0.125 (0dB)

:

0x7FFFFFF: 0.999 (+18dB)

(When read)

Hold data

(Note)

When NMute[15:0] bit is 0x4000, the volume increases and decreases at this bit value.

- **Delta[27:0]**

This bit specifies a volume change rate by an increasing or decreasing value for each sample time.

(Initial value)

0x0000000

(When written)

0x0000000: 0.0 (no change)

0x0000001: 2^{-27}

:

0x1000000: 0.125

:

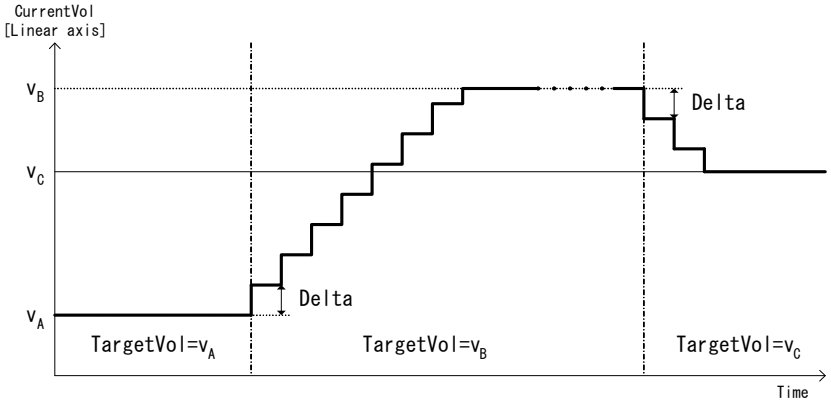
0x7FFFFFF: 0.999

(When read)

Hold data

(Note)

- When setting TargetVol[27:0] bit, Delta[27:0] value is added or subtracted to/from CurrentVol[27:0] value for each sample time until CurrentVol[27:0] value arrives TargetVol[27:0] value.



- When setting NMute[15:0] to 0x0000, Delta[27:0] value is subtracted from CurrentVol[27:0] value for each sample time until CurrentVol[27:0] value arrives Mute(0x0000000). When returning NMute[15:0] to 0x4000, Delta[27:0] value is added to CurrentVol[27:0] value for each sample time until CurrentVol[27:0] value arrives TargetVol[27:0] value. NMute[15:0] function is given priority over TargetVol[27:0] function.
- The time between a current volume value and a target volume value can be found by the following formula:

$$(\mathrm{ceil})\left\{\frac{(\mathrm{abs})(\mathrm{TargetVol}[27:0]-\mathrm{CurrentVol}[27:0])}{\mathrm{Delta}[27:0]}\right\}/48\mathrm{kHz}\ [\mathrm{s}]$$

"ceil" means it should be rounded up to the nearest integer, and "abs" means an absolute value.

For example, when the current volume value is 0dB (0x1000000), target volume value is mute (0x0000000), and change rate is 1.25×10^{-4} (0x0004189), the time becomes approx. 21 ms.

● BypassSel[15:0], 10bPEQSel[15:0]

These bits specify whether or not to bypass the SDSP 10-band PEQ processing.

(Initial value)

0x0000

(When written)

BypassSel[15:0]=0x4000 (0dB), 10bPEQSel[15:0]=0x0000 (Mute): Bypass SDSP 10-band PEQ processing

BypassSel[15:0]=0x0000 (Mute), 10bPEQSel[15:0]=0x4000 (0dB): Select SDSP 10-band PEQ processing output

Other values: Reserved

(When read)

Hold data

● EQ*.a0[27:0], a1[27:0], a2[27:0], b1[27:0], b2[27:0] (*=0/1)

These bits specify the filter coefficients of the loudness-tracking equalizer.

(Initial value)

0x0000

(When written)

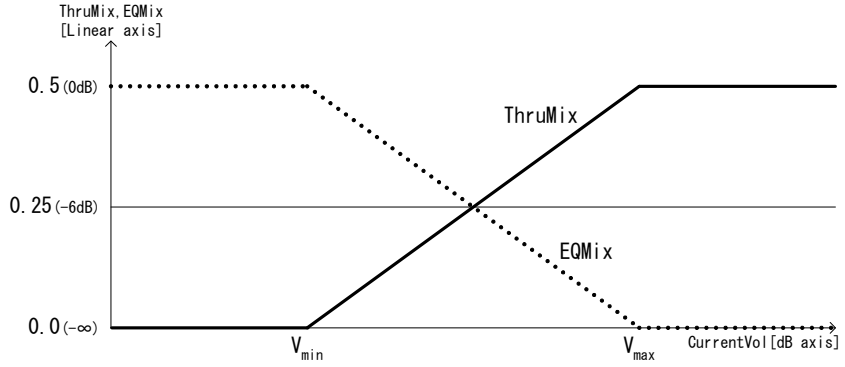
2nd-order IIR filter coefficient. Set the designed value multiplied by 1/2 for EQ0 and the designed value multiplied by 1/8 for EQ1.

(When read)

Hold data

(Note)

- The loudness-tracking equalizer can be made by setting any filter coefficient to these bits. To give the loudness feature, use a low-shelving filter coefficient and a high-shelving filter coefficient to EQ0 and EQ1, respectively.
- The figure below shows the operating characteristics of the Loudness gain controller. The loudness-tracking equalizer is made by varying the following gain values according to the current volume value with the relation "EQMix+ThruMix=0dB" kept unchanged: The gain EQMix for the equalizer processing path, the gain ThruMix for the straight path (no equalizer processing). V_{max} is the volume value at which the equalizer effect starts to work and V_{min} is the volume value at which the equalizer effect saturates.



- **LnRatio[15:0]**

These bits control the degree of the applied effect of the loudness-tracking equalizer.

(Initial value)

0x0000

(When written)

Set the value calculated with the following formula:

$$LnRatio[15:0] = 0.5/(V'_{max} - V'_{min}) * 0.25$$
$$V'_{max} = (V_{max} - 18.06)/96.33$$
$$V'_{min} = (V_{min} - 18.06)/96.33$$

V_{max}: a volume value (dB) at which the effect starts to work

V_{min}: a volume value (dB) at which the effect starts to be saturated

For example, at V_{max} =−20dB, V_{min} =−60dB, set 0x2688 (0.301…) to this bit.

(When read)

Hold data

- **LnShift[15:0]**

This bit control the volume value at which the effect of the loudness-tracking equalizer starts to work.

(Initial value)

0x0000

(When written)

Set the value calculated with the following formula:

$$LnShift[15:0] = -LnRatio[15:0] * V'_{min}$$
$$V'_{min} = (V_{min} - 18.06)/96.33$$

V_{min}: a volume value at which the effect is saturated.

For example, at LnRatio[15:0] = 0x2688 (0.301…), V_{min} = −60dB, set 0x1F39 (0.243…) to this bit.

(When read)

Hold data

- **LnSel[15:0], LnThruSel[15:0]**

These bits specify an effect of the loudness-tracking equalizer

(Initial value)

0x0000

(When written)

LnSel[15:0]=0x0000 (Mute), LnThruSel[15:0]=0x4000 (0dB): Effect not applied

LnSel[15:0]=0x4000 (0dB), LnThruSel[15:0]=0x0000 (Mute): Effects applied

Other values: Reserved

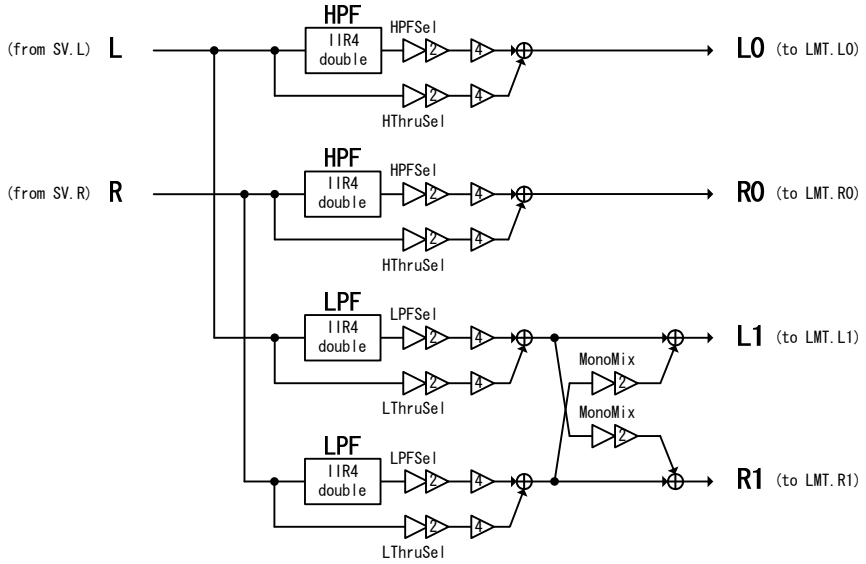
(When read)

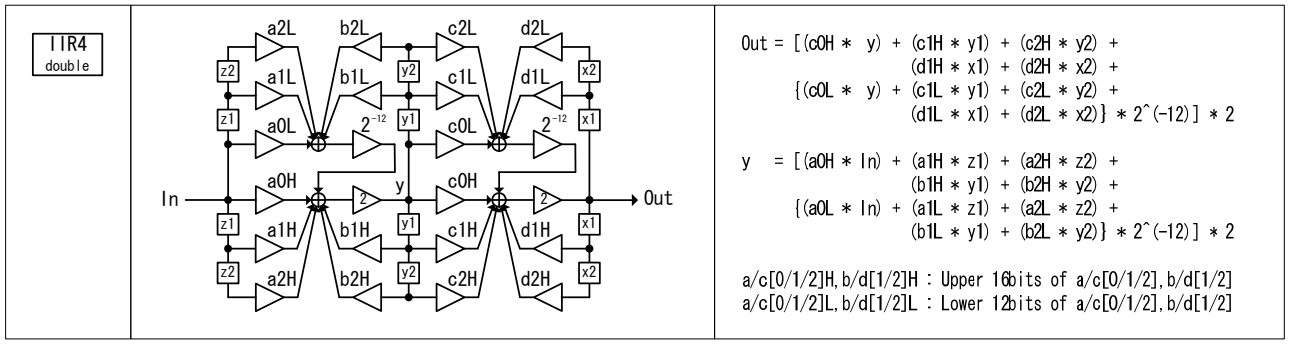
Hold data

2.3.8 Crossover Filter

The crossover filter makes one-way, two-way, or 2.1-channel digital network in accordance with your system configuration.

2.3.8-1 Signal Flow





[Note]

- As shown in the figure above, the 4 times multiplication (4) following HPFSel, HThruSel, LPFSel, or LThruSel compensates Smooth volume firmware output. The gain value is reduced to one-quarter.

2.3.8-2 Coefficient data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x41C3		15-00	HPF	a0[27:12]
1	0x41C4		15-12		0
			11-00		a0[11:0]
2	0x41C5		15-00		a1[27:12]
3	0x41C6		15-12		0
			11-00		a1[11:0]
4	0x41C7		15-00		a2[27:12]
5	0x41C8		15-12		0
			11-00		a2[11:0]
6	0x41C9		15-00		b1[27:12]
7	0x41CA		15-12		0
			11-00		b1[11:0]
8	0x41CB		15-00		b2[27:12]
9	0x41CC		15-12		0
			11-00		b2[11:0]
10	0x41CD		15-00		c0[27:12]
11	0x41CE		15-12		0
			11-00		c0[11:0]
12	0x41CF		15-00		c1[27:12]
13	0x41D0		15-12		0
			11-00		c1[11:0]
14	0x41D1		15-00		c2[27:12]
15	0x41D2		15-12		0
			11-00		c2[11:0]
16	0x41D3		15-00		d1[27:12]
17	0x41D4		15-12		0
			11-00		d1[11:0]
18	0x41D5		15-00		d2[27:12]
19	0x41D6		15-12		0
			11-00		d2[11:0]
20	0x41D7		15-00	LPF	a0[27:12]
21	0x41D8		15-12		0
			11-00		a0[11:0]
22	0x41D9		15-00		a1[27:12]
23	0x41DA		15-12		0
			11-00		a1[11:0]
24	0x41DB		15-00		a2[27:12]
25	0x41DC		15-12		0
			11-00		a2[11:0]
26	0x41DD		15-00		b1[27:12]
27	0x41DE		15-12		0
			11-00		b1[11:0]
28	0x41DF		15-00		b2[27:12]
29	0x41E0		15-12		0
			11-00		b2[11:0]
30	0x41E1		15-00		c0[27:12]

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
31	0x41E2		15-12		0
			11-00		c0[11:0]
32	0x41E3		15-00		c1[27:12]
33	0x41E4		15-12		0
			11-00		c1[11:0]
34	0x41E5		15-00		c2[27:12]
35	0x41E6		15-12		0
			11-00		c2[11:0]
36	0x41E7		15-00		d1[27:12]
37	0x41E8		15-12		0
			11-00		d1[11:0]
38	0x41E9		15-00		d2[27:12]
39	0x41EA		15-12		0
			11-00		d2[11:0]
40	0x41EB		15-00	MonoMix[15:0]	
41	0x41EC		15-00	HPFSel[15:0]	
42	0x41ED		15-00	HThruSel[15:0]	
43	0x41EE		15-00	LPFSel[15:0]	
44	0x41EF		15-00	LThruSel[15:0]	

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.
- “0” in the Bit Name column is the reserved bits. Write “0” into these bits during the write access. When reading the bit, an undefined value is read.
- The coefficients of a filter should be set every biquad filter coefficients (10 words) at once.

- **HPF/LPF.a0[27:0], a1[27:0], a2[27:0], b1[27:0], b2[27:0]**

These bits specify HPF or LPF filter coefficients.

(Initial value)

0x0000000

(When written)

4th-order IIR filter coefficient (double-precision coefficient). Set the designed value multiplied by 1/2.

(When read)

Hold data

- **MonoMix[15:0]**

This bit selects whether to transform the low frequency range signals into monaural signals or not.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute). No mixing is performed to the low frequency range signals.

0x4000: 0.5 (0dB). Low frequency range signals are transformed into monaural signals.

Other values: Reserved

(When read)

Hold data

- ***PFSel[15:0], *ThruSel[15:0] (*=H/L)**

These bits specify the HPF output gain, HPF Thru. gain, LPF output gain, and LPFThru. gain.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6dB)

:

0x4000: 0.5 (0dB)

Other values: Reserved

(When read)

Hold data

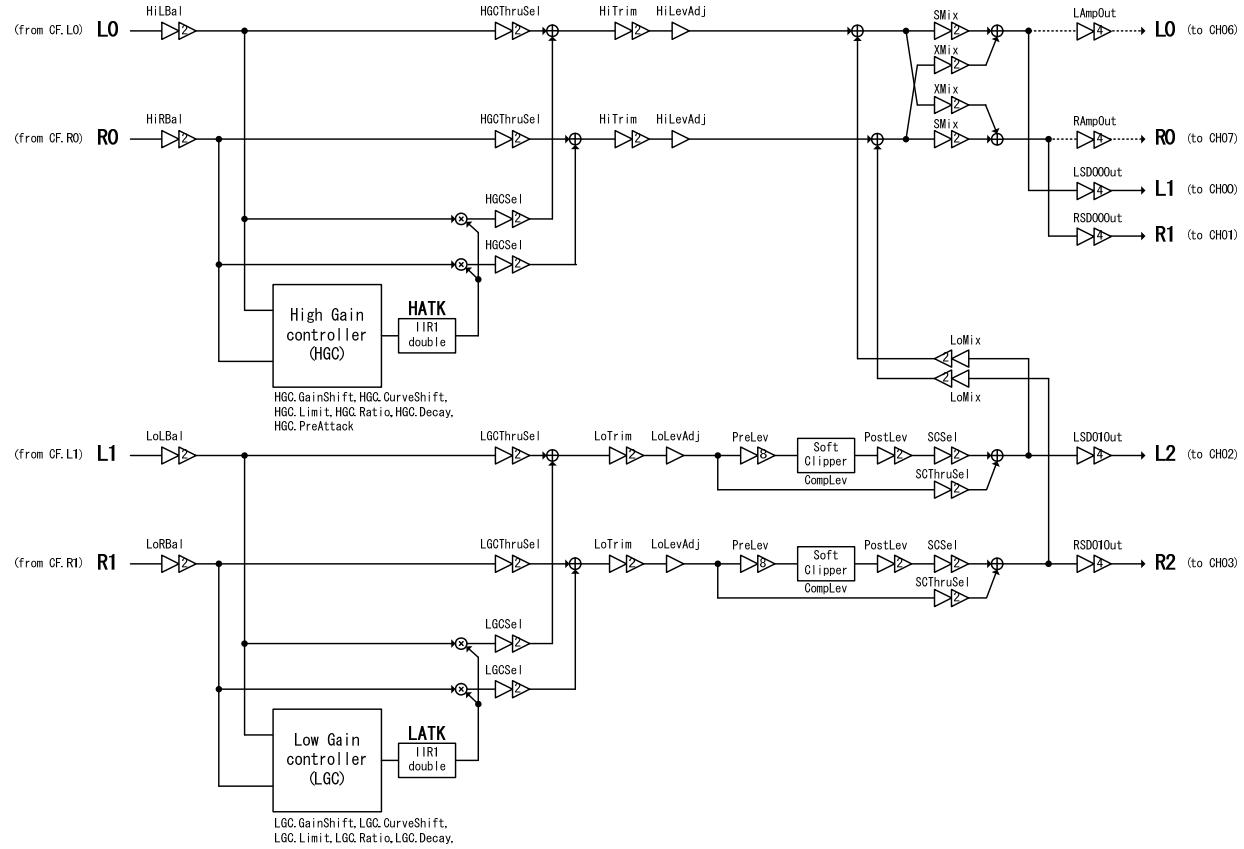
(Note)

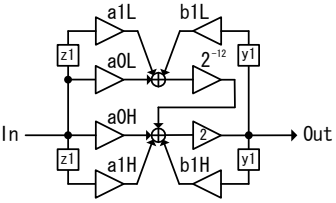
For usual applications, to use the HPF (LPF) output path, use 0x4000 for the HPFSel (LPFSel)[15:0] and 0x0000 for the HThruSel (LThruSel)[15:0], and to use the HPF (LPF) Thru path, use 0x0000 for the HPFSel (LPFSel)[15:0] and 0x4000 for the HThruSel (LThruSel)[15:0]. To adjust the gain values at a time, use the above value “0x4000” to any value.

2.3.9 Limiter

Limiter firmware limits the output level and compresses the dynamic range for each signal separated by Crossover filter firmware. And, it also clips waveform of low frequency range singnal smoothly.

2.3.9-1 Signal Flow



IIR1 double		Out = [(a0H * In) + (a1H * z1) + (b1H * y1) + {(a0L * In) + (a1L * z1) + (b1L * y1)} * 2^(-12)] * 2 a[0/1/2]H, b[1/2]H : Upper 16bits of a[0/1/2], b[1/2] a[0/1/2]L, b[1/2]L : Lower 12bits of a[0/1/2], b[1/2]

[Note]

- Dotted paths (L0/R0 output path) are valid in DD-2SP only.
- High/Low Gain controller outputs a gain value corresponding to the detected peak signal.
- Soft Clipper clips the waveform of an input signal smoothly and outputs it.

2.3.9-2 Coefficient Data

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name	
0	0x4066		15-00	HiLBal[15:0]	
1	0x4067		15-00	HiRBal[15:0]	
2	0x4068		15-00	LoLBal[15:0]	
3	0x4069		15-00	LoRBal[15:0]	
4	0x406A		15-00	HGC	GainShift[15:0]
5	0x406B		15-00		CurveShift[15:0]
6	0x406C		15-00		Ratio[15:0]
7	0x406D		15-00		Limit[15:0]
8	0x406E		15-00		Decay[15:0]
9	0x406F		15-00		PreAttack[15:0]
10	0x4070		15-00	HATK	a0[27:12]
11	0x4071		15-12 11-00		0 a0[11:0]
12	0x4072		15-00		a1[27:12]
13	0x4073		15-12 11-00		0 a1[11:0]
14	0x4074		15-00		b1[27:12]
15	0x4075		15-12 11-00		0 b1[11:0]
16	0x4076		15-00	LGC	GainShift[15:0]
17	0x4077		15-00		CurveShift[15:0]
18	0x4078		15-00		Ratio[15:0]
19	0x4079		15-00		Limit[15:0]
20	0x407A		15-00		Decay[15:0]
21	0x407B		15-00	LATK	a0[27:12]
22	0x407C		15-12 11-00		0 a0[11:0]
23	0x407D		15-00		a1[27:12]
24	0x407E		15-12 11-00		0 a1[11:0]
25	0x407F		15-00		b1[27:12]
26	0x4080		15-12 11-00		0 b1[11:0]
27	0x4081		15-00	HGCThruSel[15:0]	
28	0x4082		15-00	HGCSel[15:0]	
29	0x4083		15-00	LGCThruSel[15:0]	
30	0x4084		15-00	LGCSel[15:0]	
31	0x4085		15-00	HiTrim[15:0]	
32	0x4086		15-00	LoTrim[15:0]	
33	0x4087		15-04 03-00	0 HiLevAdj[3:0]	
34	0x4088		15-04 03-00	0 LoLevAdj[3:0]	
35	0x4089		15-00	PreLev[15:0]	
36	0x408A		15-00	PostLev[15:0]	

No.	On-chip RAM Address	MDSP2	Bit Position	Bit Name
37	0x408B		15-00	CompLev[15:0]
38	0x408C		15-00	SCThruSel[15:0]
39	0x408D		15-00	SCSel[15:0]
40	0x408E		15-00	LoMix[15:0]
41	0x408F		15-00	SMix[15:0]
42	0x4090		15-00	XMix[15:0]
43	0x4091		15-00	LAmpOut[15:0]
44	0x4092		15-00	RAmpOut[15:0]
45	0x4093		15-00	LSDO0Out[15:0]
46	0x4094		15-00	RSDO0Out[15:0]
47	0x4095		15-00	LSDO1Out[15:0]
48	0x4096		15-00	RSDO1Out[15:0]

[Note]

- A blank cell in the MDSP2 column indicates it can be transferred whether MDSP2 is stopped or not.
- "0" in the Bit Name column is the reserved bits. Write "0" into these bits during the write access. When reading the bit, an undefined value is read.
- The coefficients of a filter should be set at a time.

● *Bal[15:0] (*= HiL/HiR/LoL/LoR)

This bit adjusts L/R balance of the high or low frequency range signals.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6dB)

:

0x4000: 0.5 (0dB)

Other values: Reserved

(When read)

Hold data

● *GC.GainShift[15:0] (*=H/L)

This bit specifies amount of gain shifts used for the High or Low Gain controller.

(Initial value)

0x0000

(When written)

Shift value [dB] should be set after linear conversion with negative sign bit.

0x7FFF: ≒0 dB

:

0x4000: 6.02 dB

:

0x0001: 90.3 dB

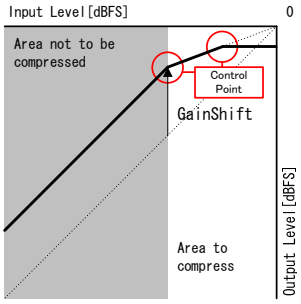
Other values: Reserved

(When read)

Hold data

(Note)

- The linear part of the input-output transfer curve, in which compression is not performed, shift upward by the value set here; however, in the compressing part in which compression is performed, the transfer curve bent downward toward the original curve from the first control point and from the second control point (when the second control point exists) are limited to a constant output level. See the description about *GC.Ratio[15:0] bit (described later) for the detail of changing points.
- Set a value according to "GainShift[dB] − CurveShift[dB] ≤ 18[dB]". For details of CurveShift, see "GC.CurveShift[15:0]" described later.



- The input signal level to the Limiter firmware becomes lower depending on the headroom size allocated for Input level detector firmware, Acoustic total-linear EQ core firmware, and Smooth volume firmware. In order to get designed specification, it is need to correct I/O characteristic for keeping headroom.
  1) Design I/O characteristic with Curve shift and compression ratio.
  2) Calculate gain shift with the following equation.

  Gain shift (Correction value) = Gain shift (Design value) + HR × (1 − compression ratio)

  Here, HR is a value in dB, which is the headroom allocated with Att[15:0] of Input level detector firmware and Att[15:0] of Acoustic total-linear EQ core firmware and Att[15:0] of Smooth volume firmware. See the description of *GC.Ratio[15:0] for details of the compression ratio.
  Then, I/O characteristic curve is corrected by correcting both Gain shift and Curve shift. Refer to hereinafter described "GC.CureveShift[15:0]" to understand I/O characteristic correction.

● *GC.CurveShift[15:0] (*=H/L)

This bit specifies the amount of curve shifts (total shifts of I/O characteristics curve) in the High or Low Gain controller.

(Initial value)

0x0000

(When written)

Shift value [dB] should be set after linear conversion with negative sign bit.

0x7FFF: ≒0 dB

:

0x4000: 6.02 dB

:

0x0006: 74.7 dB

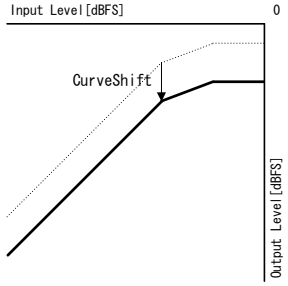
Other values: Reserved

(When read)

Hold data

(Note)

- The whole I/O characteristic curve shifts to the decreasing direction as much as the value set here.

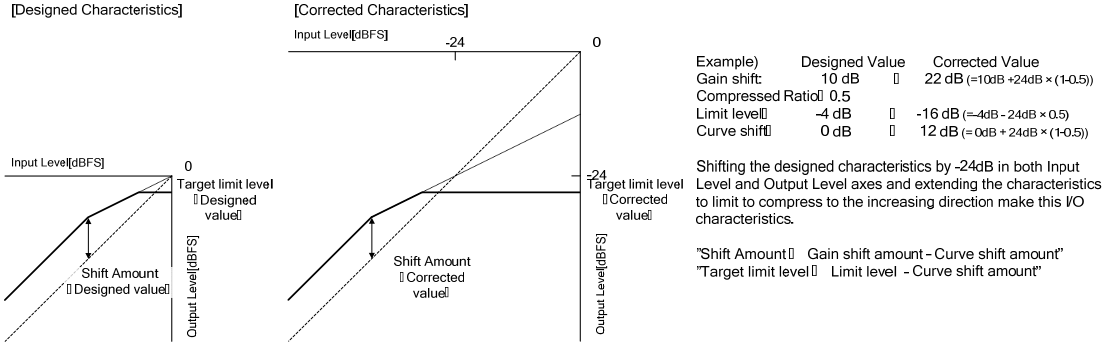


- Set a value according to "GainShift[dB] − CurveShift[dB] ≤ 18[dB]".
- Set a value according to "Limit[dB] − CurveShift[dB] > -78.3[dB]".
- The input signal level to the limiter firmware becomes lower depending on the headroom size secured with Input level detector firmware, Acoustic total-linear EQ core firmware, and Smooth volume firmware. In order to get designed specification, adjust I/O characteristic for keeping headroom.
  1) Design I/O characteristic with gain shift and compression ratio.
  2) Calculate Curve shift with following equation.

  Curve shift (Correction value) = Curve shift (Design value) + HR × (1 − compression ratio)

  Here, HR is a value in dB, which is the headroom secured with Att[15:0] of Input level detector firmware and Att[15:0] of Acoustic total-linear EQ core firmware and Att[15:0] of Smooth volume firmware. See the description of *GC.Ratio[15:0] for details of the compression ratio.

  The figure below shows an example of the correction characteristic with the headroom of 24 dB secured in Input level detector firmware, Acoustic total-linear EQ core firmware, and Smooth volume firmware.



● *GC.Ratio[15:0] (*=H/L)

This bit specifies a compression ratio in the High or Low Gain controller.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Compression ratio =0.0)

:

0x2000: 0.25 (Compression ratio =0.5)

:

0x3FFF: 0.5 (Compression ratio ≒1.0)

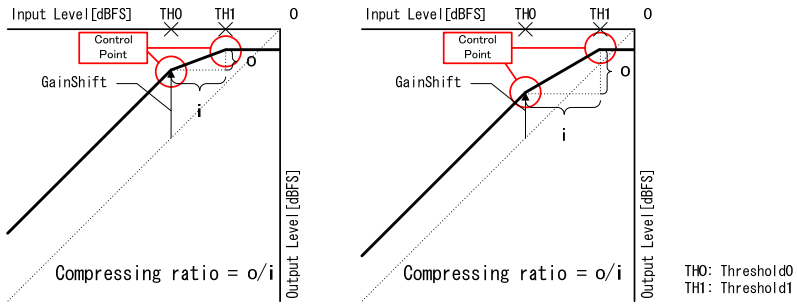
Other values: Reserved

(When read)

Hold data

(Note)

- The compression ratio is the slope of a line connecting the first control point and the second one in I/O characteristics.
  The input level of the first control point, being at the border between the part to compress and the part not to be compressed, is referred to as “Threshold0”. And the input level of the second control point at which the output limit will start being applied in the compression part is referred to as "Threshold1". See the description about *GC.Limit[15:0] (described later) for the details of Threshold1.



- The GainShift is found by the following formula, based on Threshold0 and Compression ratio.

  GainShift[dB] = Threshold0 × (Compression ratio −1.0)

  For example, when Threshold0 is −20 dB and Compression ratio is 0.5, the GainShift becomes 10 dB. In the above two figures, the Threshold0 is the same but its GainShift differs because of different compression ratio.

● *GC.Limit[15:0] (*=H/L)

This bit specifies a limit level in High Gain controller or Low Gain controller.

(Initial value)

0x0000

(When written)

Set a value linearly converted from a limit level [dB].

0x7FFF: Limit function is disabled (≒0dBFS)

:

0x4000: −6.02 dB

:

0x0005: −76.3 dB

Other values: Reserved

(When read)

Hold data

(Note)

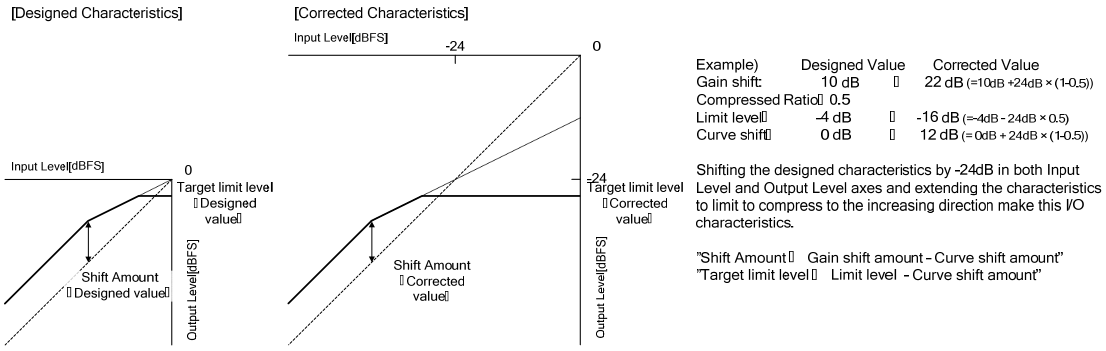
- If an input level is higher than Threshold1, the input signal will be compressed and the output level will be limited to the value specified with this bit. And, Gain controller functions so that a value calculated with the following expression becomes Threshold1.

  Threshold1 = Limit level [dB] / Compression ratio

- Set a value according to "Limit[dB] − CurveShift[dB] > -78.3[dB]".
- According to the amount of headroom secured with Input level detector, Acoustic total-linear EQ core, and Smooth volume firmware, an input signal to Limiter firmware becomes a lower level correspondingly. When specifying a limit level, consider the amount of headroom to correct the level. Adjust the limit level to a value calculated with the following expression:

  Limit level (corrected value) = Limit level (designed value) − HR × Compression ratio

  HR [dB] indicates the amount of total headroom allocated with the following bits: Att[15:0] bit in Input level detector firmware, Att[15:0] bit in Acoustic total-linear EQ core firmware, and Att[15:0] bit in Smooth volume firmware.
  And, I/O characteristics are adjusted by gain shift level, curve shift level, and limit level. For the detail of I/O characteristics adjustment, see the description about *GC.CurveShift[15:0] bit.
  The figure below shows an example of the correction characteristic with the headroom of 24 dB secured in Input level detector firmware, Acoustic total-linear EQ core firmware, and Smooth volume firmware.



- ***GC.Decay[15:0] (*=H/L)**

This bit specifies the decay time until input signal, which is held as a peak hold value by the High or Low Gain controller, attenuates by −8.69dB(e^{-1} times). This bit controls release time.

(Initial value)

0x0000

(When written)

Decay time $\fallingdotseq$ 1.943×10^{8} / (Decay[15:0]$\times2^{8}$) / 48kHz[s]

0x0000: Mute

0x0001: approx. 15.8 s

:

0x0100: approx. 61.8 ms

:

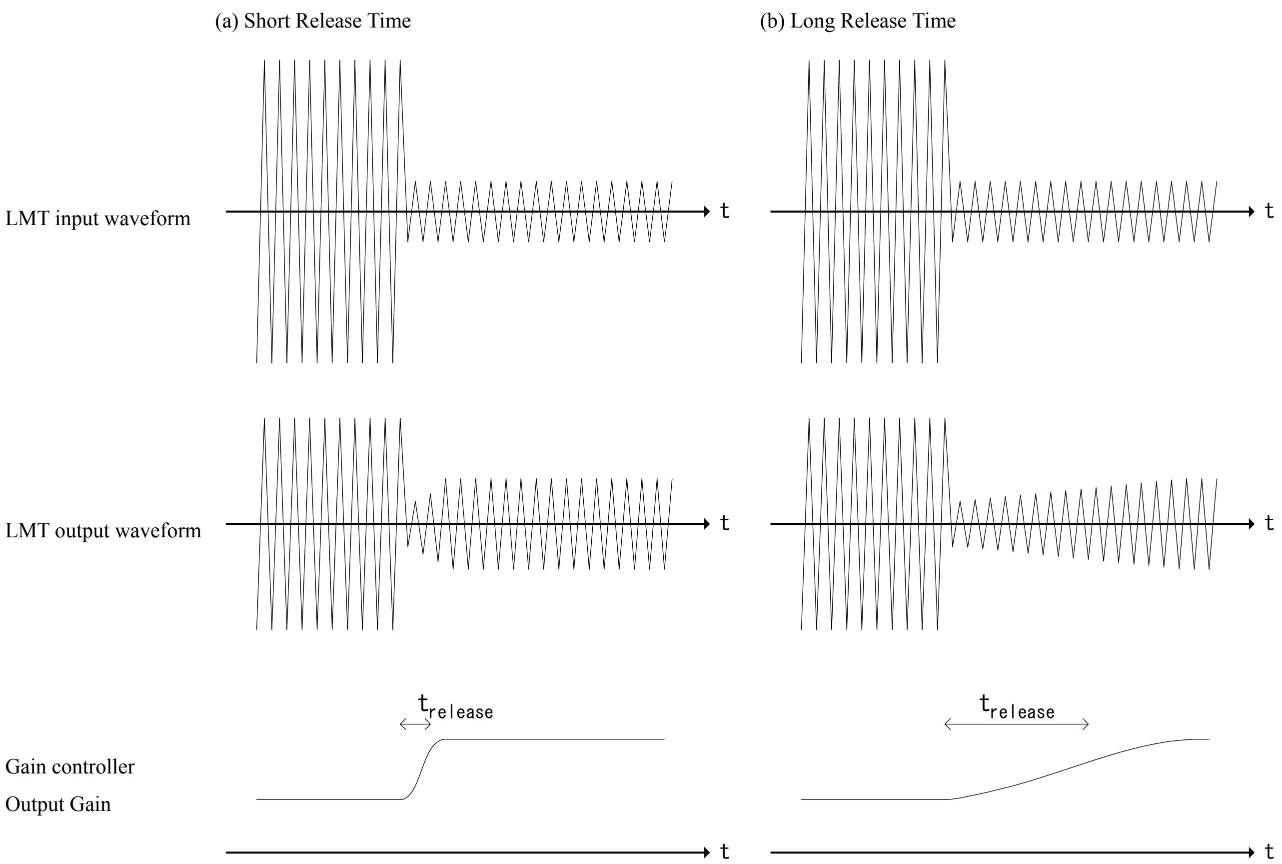
0xFFFF: $\fallingdotseq$0

(When read)

Hold data

(Note)

- When setting this bit to 0x0000 (Mute), input signal held as peak hold value does not attenuate.
- Release time is time required for output gain change in Gain controller when input signal is changed from large amplitude to small amplitude. The figures below show input and output waveforms and gain change of both short and long release times.



- ***GC.Hold[15:0] (*=H/L)**

This bit specifies a hold time of the gain for input signal in which the peak gain is held in the High or Low Gain controller.

(Initial value)

0x0000

(When written)

0x0000: 0

0x0001: 167 µs

:

0x0100: 42.8 ms

:

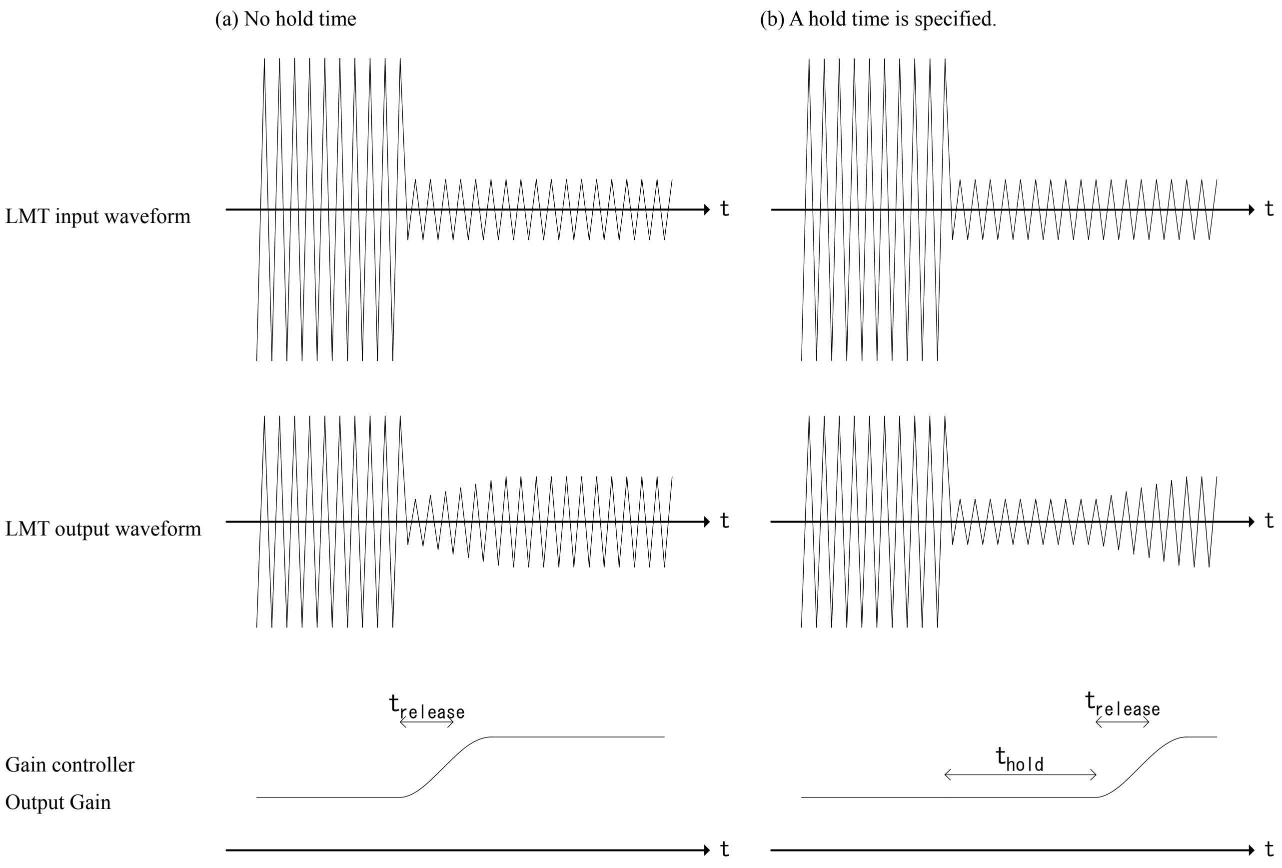
0x7FFF: 5.46 s

(When read)

Hold data

(Note)

Hold time is a period of time to hold output gain of Gain controller when input signal is changed from large amplitude to small amplitude. The figures below show input and output waveforms and gain change of the following cases: (a): no hold time is specified (Hold[15:0]=0x0000), (b): a certain hold time is specified.



- ***GC.PreAttack[15:0] (*=H/L)**

This bit specifies a time taken for an input signal (which is held as a peak-hold value in the High or Low Gain controller) to increase by 8.69 dB (*e* times). This bit adjusts a pre-attack time.

(Initial value)

0x0000

(When written)

Increased time ≒1.943×10^8 / (PreAttack[15:0] × 2^8) / 48kHz[s]

0x0317: approx. 20 ms

:

0x062E: approx.10 ms

:

0xFFFE: approx. 250 µs

0xFFFF: 0

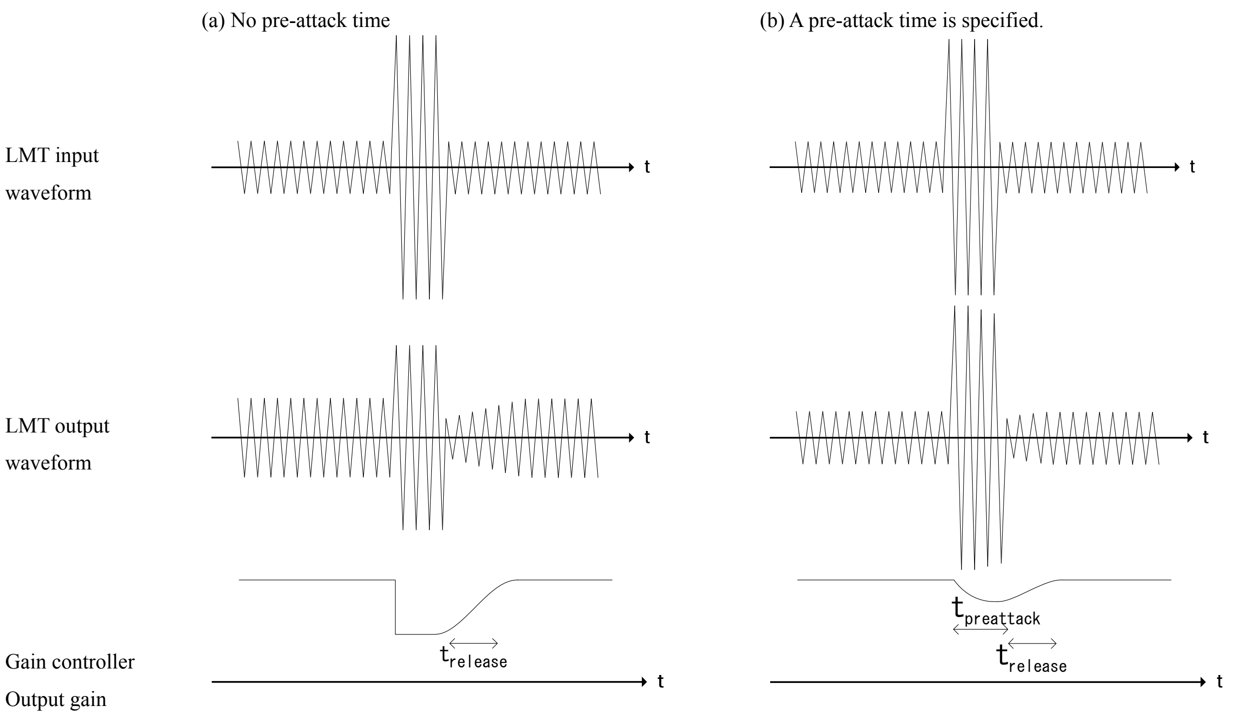
Other values: Reserved

(When read)

Hold data

(Note)

- Pre-attack time is a period of time taken for Gain controller's output gain to track the variation of its input signal from a small to a large amplitude. Setting a pre-attack time to a short period of time makes Gain controller insensitive to an instantaneous large amplitude input signal.
- The figures below show input and output waveforms and the output gain change of the following cases: (a) no pre-attack time is specified (PreAttack[15:0]=0xFFFF), (b) A pre-attack time is specified. In figure (b), because of a large amplitude input signal inputting for a short period of time, the compression is released before the specified compression level is attained, resulting in dull Gain controller's response. Another attack time (*ATK) described later makes Gain controller's output change (that is, attainment of the specified compression level) smooth but this pre-attack time controls the response of Gain controller.



● *ATK.a0[27:0], a1[27:0], a2[27:0], b1[27:0], b2[27:0] (*=H/L)

This bit specifies IIR filter coefficients by the HATK or LATK filter in order to control attack time.

(Initial value)

0x0000000

(When written)

Value indicates coefficient (double precision) of the 1st-order IIR filter. Set the designed coefficient value multiplied by 1/2.

(When read)

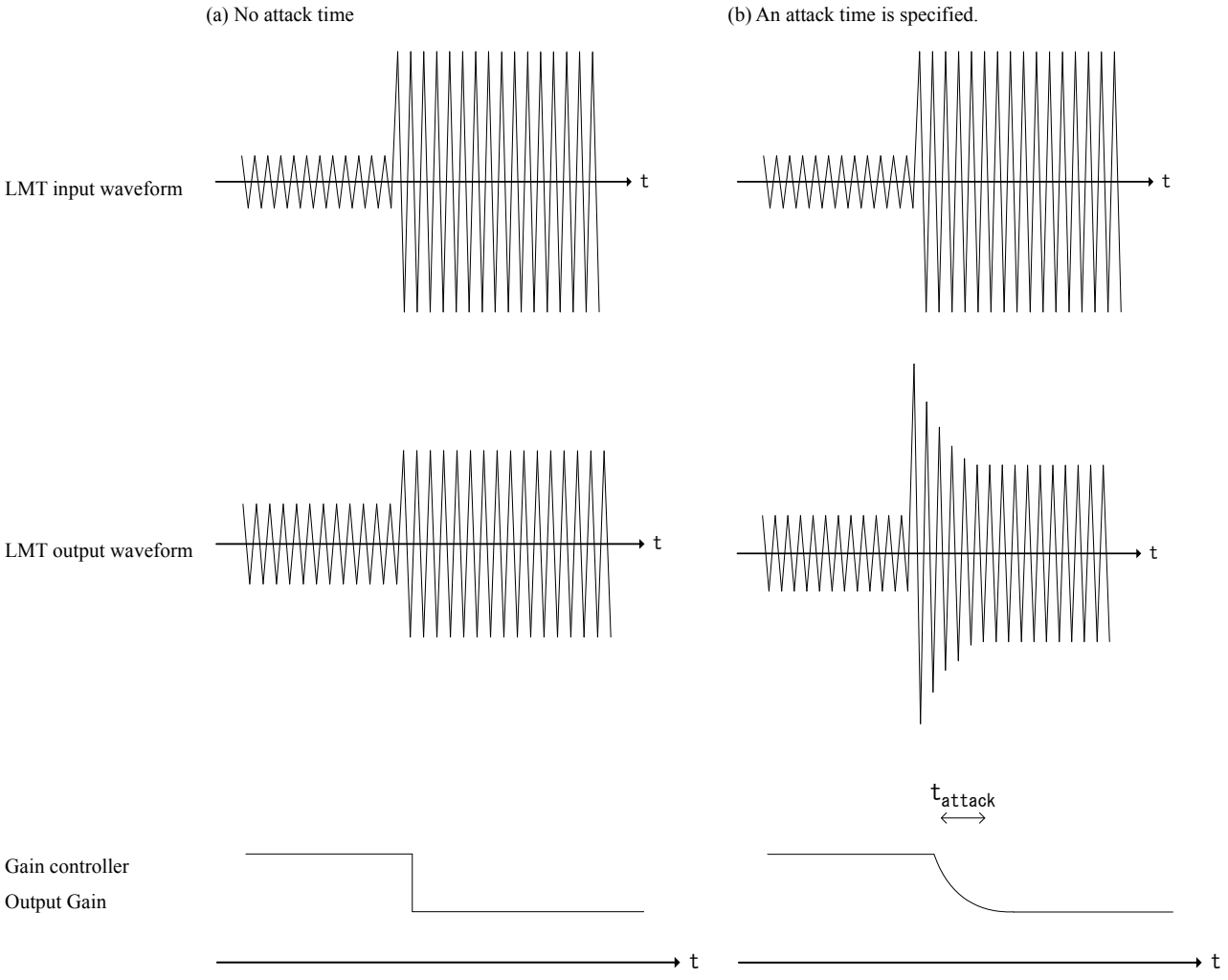
Hold data

(Note)

- Attack time is time required for output gain change when input signal is changed from small amplitude to large amplitude. By giving low-pass characteristics to filter, attack time can be controlled within 100 ms. Supposing attack time is t_a [s], cut-off frequency f_c [Hz] of low-pass filter can be calculated by the following formula.

$$f_c = \frac{1}{2 \pi t_a} \qquad \text{however, } t_a \leq 100\text{ms}$$

If filter is set to “Through”, attack time will be removed, and amplitude change of input signal is directly reflected to dynamic range control. The figures below show input and output waveforms and gain change of the following cases: (a): no attack time is specified, (b): a certain attack time is specified.



- This filter is applied to Gain controller outputs; therefore, when an attack time is specified, an input signal varies smoothly during attack time (Gain controller input signal’s amplitude varies from a small to a large amplitude) as well as an input signal during release time (Gain controller input signal’s amplitude varies from a large to a small amplitude).

● *ThruSel[15:0], *Sel[15:0] (*=HGC/LGC)

These bits select whether to perform the limit control in the path to L0/R0 output or L1/R1 output.

(Initial value)

0x0000

(When written)

*ThruSel[15:0]=0x4000(0dB), *Sel[15:0]=0x0000(Mute): No limit control.

*ThruSel[15:0]=0x0000(Mute), *Sel[15:0]=0x4000(0dB): The limit control is applied.

Other values: Reserved

(When read)

Hold data

● *Trim[15:0] (*=Hi/Lo)

This bit adjusts the sound volume level of high or low frequency range signals.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6dB)

:

0x4000: 0.5 (0dB)

Other values: Reserved

(When read)

Hold data

(Note)

- A headroom of 6dB or less, which cannot be cancelled by *LevAdj[3:0] bit (described later), can be cancelled by adjusting this bit.
- Slicer function can be used by setting an appropriate value to this bit and adjusting *LevAdj[3:0] and *Out[15:0] bits (described later).

● *LevAdj[3:0] (*=Hi/Lo)

This bit specifies the amount of the allocated headroom to high or low frequency range signals. The high or low frequency range signal is shifted up by the specified number of bits, resulting in the headroom cancellation. And, A headroom can be cancelled with an accuracy of 6dB by a combination of this bit and *Trim[15:0] bit (described above).

(Initial value)

0x0

(When written)

0x0: does not cancel the headroom.
0x1: cancels the headroom by 1-bit (+6dB)
0x2: cancels the headroom by 2-bits (+12dB)
0x3: cancels the headroom by 3-bits (+18dB)
0x4: cancels the headroom by 4-bits (+24dB)
:
0x7: cancels the headroom by 7-bits (+42dB)
0x8: cancels the headroom by 8-bits (+48dB)
:
0xF: cancels the headroom by 15-bits (+90dB)

(When read)

Hold data

(Note)

- Usually, when DD-2SP is used, HiLevAdj[3:0] bit and LoLevAdj[3:0] bit should be set to a value subtracted by 1 bit from a headroom that is secured with the following bits: Att[15:0] in Input level detector firmware, Att[15:0] bit in Acoustic total-linear EQ core firmware, Att[15:0] bit in Smooth volume firmware. 0x7 is set in this example. A headroom for the above 1 bit can be cancelled in the digital amplifier output path (L0/R0 output path) by setting AmpOut[15:0] (described later) to 0x2000 (0dB) and GAIN[1:0] (0x2F Gain) to 0x1 (+6dB). And, a headroom for the above 1 bit can be cancelled in the SDO* path (L1/R1, L2/R2 output path) by setting SDO*Out[15:0] to 0x4000 (+6dB).
- Usually, when SPR-2 is used, HiLevAdj[3:0] bit and LoLevAdj[3:0] bit should be set to a value subtracted by 1 bit from a headroom that is secured with the following bits: Att[15:0] in Input level detector firmware, Att[15:0] bit in Acoustic total-linear EQ core firmware, Att[15:0] bit in Smooth volume firmware. 0x7 is set in this example. A headroom for the above 1 bit can be cancelled in the SDO* path (L1/R1, L2/R2 output path) by setting SDO*Out[15:0] to 0x4000 (+6dB).

- **PreLev[15:0]**

PreLev adjusts the input signal level in Soft Clipper processing.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x1000: 0.125 (0 dB)

:

0x7FFF: 0.999 (+18 dB)

Other values: Reserved

(When read)

Hold data

(Note)

- Soft Clipper applies soft clipping to the input signal level as it gets closer to 0 dBFS, and leave the signal unchanged as the level gets farther away below 0 dBFS. To get Soft Clipper work for small level input signal, its signal level needs to be boosted to be around 0 dBFS using this PreLev[15:0].
- When Limiter firmware is in use to limit the output power, PreLev[15:0] value must be determined as follows.

  PreLev [15:0] value (in dB) = HR – Limit Level (design value)

  Where HR (in dB) is the headroom left after LoLevAdj[15:0] adjustment (as described previously). As for the Limit Level, see *GC.Limit[15:0] (in the previous section).

  For example, when the Limit Level is –2 dB and the adjusted headroom is one bit (= 6 dB), specify PreLev [15:0] as 8 dB (= 6 dB – (–2 dB)).
- When Limiter firmware is not in use, use the HR value (one bit is equivalent to 6 dB in this document) as PreLev [15:0] value.

- **PostLev[15:0]**

PostLev adjusts the output signal level of Soft Clipper processing.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x4000: 0.5 (0 dB)

:

0x7FFF: 0.999 (+6 dB)

Other values: Reserved

(When read)

Hold data

(Note)

This bit cancels audio signal amplitude at PreLev[15:0] bit. Set “- (PreLev[15:0] bit assigned value [dB])” to this bit for usual applications.

● CompLev[15:0]

CompLev specifies the degree of compression in Soft Clipper processing as a compression ratio for the 0 dBFS signal.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (No compression)

:

0x1000: 0.125 (Compressed level = 1.2dB)

:

0x2AAB: 0.333 (Compressed level = 3.5dB)

Other values: Reserved

(When read)

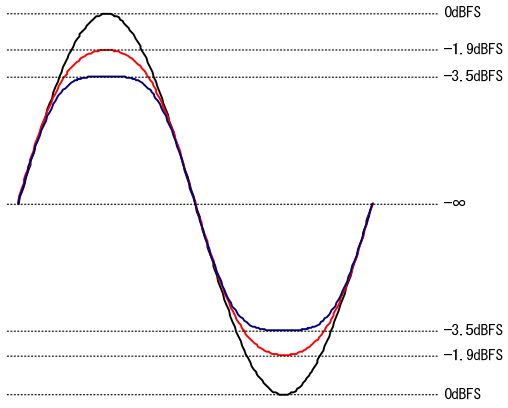
Hold data

(Note)

- Soft Clipper applies soft clipping to the input signal level as it gets closer to 0 dBFS, and leave the signal unchanged as the level gets farther away below 0 dBFS. To get Soft Clipper work for small level input signal, the level needs to be boosted to be around 0 dBFS using PreLev[15:0]. This amplitude is cancelled by PostLev[15:0] bit for usual applications.
- Compressed level is the attenuation of SoftClipper processing signal to 0dBFs. Compressed level is defined with CompLev[15:0] bit value.

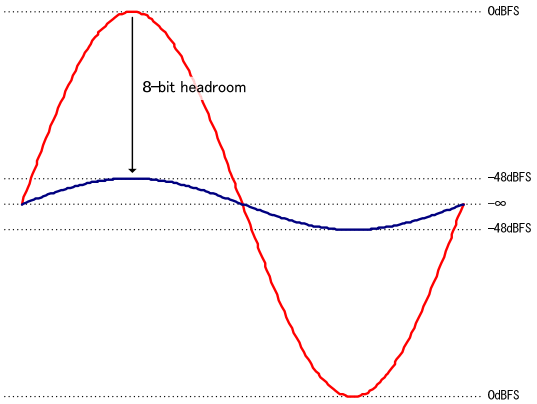
  CompLev[15:0] bit value = 1 - (linear conversion of minus compressed level [dB])

- Higher compression ratio (larger CompLev[15:0] values) results in smaller clipped signal level. Applying to a 0 dBFS sine wave input results in the output signals as shown below in black for no compression , red for CompLev[15:0] = 0.2, and blue for CompLev[15:0] = 0.333.



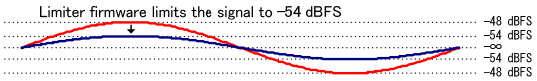
- Figures below show how a 0 dBFS input signal is processed until output through Soft Clipper and other processing. (In each figure, the incoming signal is shown in red and the outgoing signal, in blue). In this example, it assumes adjusting the amplitude of audio signal with compression by Low Gain controller, and clip by Soft clipper.

(1)



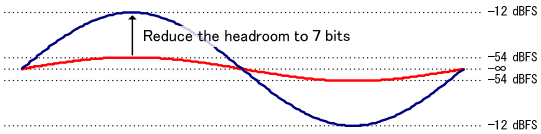
8-bit (= 48 dB) headroom provided for the input (the sine wave).

(2)



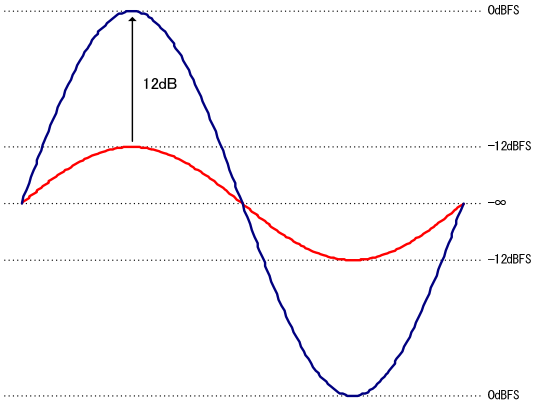
Limiter firmware reduces the signal level to limit the output power with the Low Gain controller (LGC) processing.
LGC reduces the signal level for 6 dBFS or less output power in this example (54 dBFS for this internal signal due to the headroom).

(3)



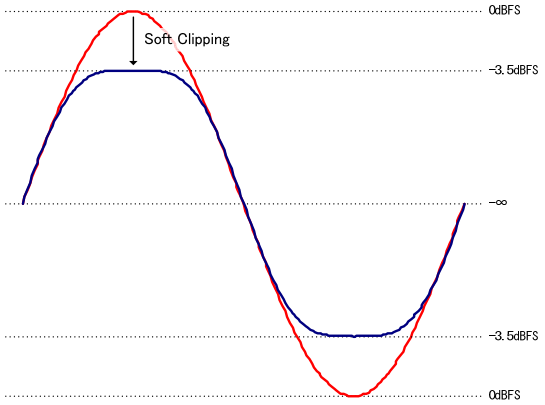
LoLevAdj[3:0] reduces the headroom by one bit to seven bit (42 dB) for the signal level in this example.

(4)



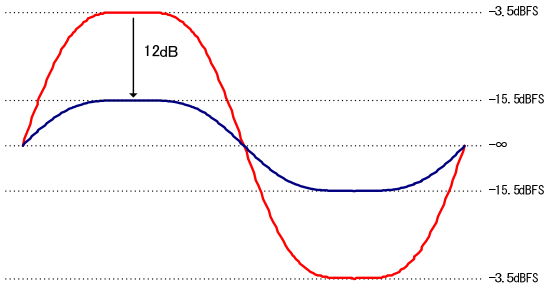
PreLev[15:0] boosts the signal level to 0 dBFS.
In this example, the signal level is boosted by 12 dB to compensate for −6 dB LGC compression in step (2), and −6 dB reduced headroom in step (3).

(5)



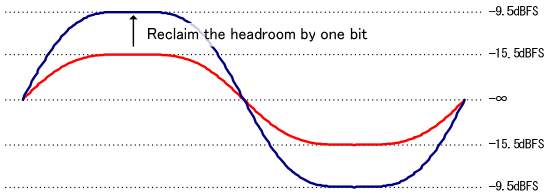
Apply soft clipping to the signal.
In this example, the signal is clipped to CompLev[15:0] = 0.333 level (−3.5 dBFS).

(6)



LMT.PostLev[15:0] cancels amplitude (12dB) of (4) LMT.PreLev[15:0].

(7)



SDO1Out[15:0] put back the reduced headroom in step (3) by one bit (6 dB).

- The above sample sets output limit (-6dBFS) and compressed level (3.5dB), output signal amplitude is below than -9.5dBFS. In case output signal amplitude sets -6dBFS or below, set output limit to -2.5dBFS at step (2), set gain 8.5dB (4) and -8.5dB (6). Other setting is as follows, keep the same setting step (2) and step (4), set -8.5dB at step (6). Output signal amplitude is -6dBFS or below, the output signal gains up 3.5dB comparing with Soft clipper disable signal.

● SCThruSel[15:0], SCSel[15:0]

Soft Clipper processing can be bypassed with SCThruSel and SCSel.

(Initial values)

0x0000

(When written)

SCThruSel [15:0] = 0x4000 (0 dB), SCSel [15:0] = 0x0000 (Mute): Bypass Soft Clipper processing

SCThruSel [15:0] = 0x0000 (Mute), SCSel [15:0] = 0x4000 (0 dB): Select Soft Clipper processing output

Other values: Reserved

(When read)

Hold data

● LoMix[15:0]

LoMix adjusts the mixing level of the low frequency range signal when mixing to the high frequency range signal.

(Initial value)

0x0000

(When written)

0xC000: −0.5 (0 dB in 180 degree out of phase)

:

0xE000: −0.25 (−6 dB in 180 degree out of phase)

:

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6 dB)

:

0x4000: 0.5 (0 dB)

Other values: Reserved

(When read)

Hold data

(Note)

- Use 0x0000 setting for most of applications.
- Adjusting this value achieves two-band limiter and two-band dynamic range compression for one-way speakers for advance applications.

● SMix[15:0], XMix[15:0]

SMix and XMix are used to adjust straight and cross channel mixing levels when making the high frequency range signal monaural.

(Initial value)

0x0000

(When written)

0x0000: 0.0 (Mute)

:

0x2000: 0.25 (−6 dB)

:

0x4000: 0.5 (0 dB)

Other values: Reserved

(When read)

Hold data

(Note)

- Use 0x4000 for SMix [15:0], and 0x0000 for XMix [15:0] for usual applications.
- Use 0x2000 for both SMix [15:0] and XMix [15:0] to make the high frequency range signal monaural.

● LAmpOut[15:0], RAmpOut[15:0]

LAmpOut, and RAmpOut adjust L0 and R0 source levels to the digital amplifier inputs.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 (Mute) and 0x4000 (+6 dB) as in;

0x0000: 0.00 (Mute)

:

0x2000: 0.25 (0 dB)

:

0x4000: 0.50 (+6 dB)

(When read)

Hold data

(Note)

・ For usual applications on DD-2SP device use the values listed below.

		LAmpOut [15:0]	RAmpOut [15:0]
For (stereo) audio applications	:	0x2000	0x2000
For (L0 source only) monaural audio applications	:	0x2000	0x0000
For (R0 source only) monaural audio applications	:	0x0000	0x2000

・ For usual applications on SPR-2 device use 0x0000 on both.

● LSDO0Out[15:0], RSDO0Out[15:0]

LSDO0Out and RSDO0Out adjust L1 and R1 source levels to the SDO0 outputs.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 (Mute) and 0x4000 (+6 dB) as in;

0x0000: 0.00 (Mute)

:

0x2000: 0.25 (0 dB)

:

0x4000: 0.50 (+6 dB)

(When read)

Hold data

(Note)

For usual applications, use the values listed below.

		LSDO0Out[15:0]	RSDO0Out[15:0]
For (stereo) audio applications	:	0x4000	0x4000
For (L1 source only) monaural audio applications	:	0x4000	0x0000
For (R1 source only) monaural audio applications	:	0x0000	0x4000

● LSDO1Out[15:0], RSDO1Out[15:0]

LSDO1Out and RSDO1Out adjust L2 and R2 source levels to the SDO1 outputs.

(Initial value)

0x0000

(When written)

Valid value range is between 0x0000 (Mute) and 0x4000 (+6 dB) as in;

0x0000: 0.00 (Mute)

:

0x2000: 0.25 (0 dB)

:

0x4000: 0.50 (+6 dB)

(When read)

Hold data

(Note)

For usual applications, use the values listed below.

		LSDO1Out[15:0]	RSDO1Out[15:0]
For (stereo) audio applications	:	0x4000	0x4000
For (L2 source only) monaural audio applications	:	0x4000	0x0000
For (R2 source only) monaural audio applications	:	0x0000	0x4000

3 Preset Pattern

The firmware coefficients are stored in the On-chip ROM as preset patterns. One preset pattern corresponds to one ROM block number, and by calling a block number a host controller can set the relevant firmware coefficients immediately.

3.1 Common

This is all-purpose coefficient values that can be transferred to an arbitrary CRAM address.

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
0	0x0E3(227)	Level Zero	RT	N	0.0000 is set.
1	0x0E4(228)	Level Low	RT	N	0.1250 (−12 dB × 1/2) is set.
2	0x0E5(229)	Level Midlow	RT	N	0.1768 (−9 dB × 1/2) is set.
3	0x0E6(230)	Level Mid	RT	N	0.2500 (−6 dB × 1/2) is set.
4	0x0E7(231)	Level Midhigh	RT	N	0.3536 (−3 dB × 1/2) is set.
5	0x0E8(232)	Level High	RT	N	0.5000 (0 dB × 1/2) is set.

[Note]

- A preset pattern with “RT” in the MDSP2 column should be executed during MDSP2 operation.
- With a preset pattern whose Transfer Destination column is “N”, a transfer destination start address needs to be specified. See “4.3 Preset Pattern Setting”.

Use Example:

- The audio signal input level can be adjusted to −9dB by transferring the coefficient set [229(0x0E5):Level Midlow] to the transfer start address “0x400B (IDL.SDI0Sel[15:0])”.

3.2 Input level detector

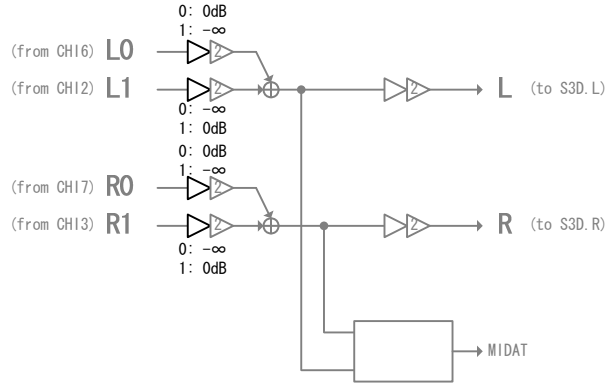
Coefficients for Input level detector firmware are transferred.

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
0	0x24D(589)	ILD SDI0 Sel	RT		Selects input signals (L0/R0) as they are (with a gain of 0dB).
1	0x24E(590)	ILD SDI1 Sel	RT		Selects input signals (L1/R1) as they are (with a gain of 0dB).

[Note]

- Preset patterns with “RT” in MDSP2 column should be executed when MDSP2 is operating.
- With the preset pattern whose Transfer Destination column is blank, a transfer destination start address needs not to be specified.

- **589−590: ILD SDI* Sel (*=0/1)**



3.3 Smooth volume

Smooth volume firmware coefficients are transferred.

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
0	0x2B2(690)	SV Immediate	RT		Maximizes the variation in speed of the volume.
1	0x2B3(691)	SV Curve Fast	RT		Selects the variation in speed (0dB →Mute) from the following three steps: Fast (approx.2ms), Mid (approx.20.9ms), Slow (approx.208ms)
2	0x2B4(692)	SV Curve Mid	RT		
3	0x2B5(693)	SV Curve Slow	RT		
4	0x2B6(694)	SV Ln DEQ0 Low	RT		Realizes the loudness characteristics by boosting the low and high frequencies with the loudness-compensation equalizer. Low: small effect, High: large effect
5	0x2B7(695)	SV Ln DEQ0 High	RT		
6	0x2B8(696)	SV Ln DEQ1 Low	RT		Cuts the low frequency band and boosts the audio frequency band with the loudness-compensation equalizer to make it easy for aged persons to catch the sound. Low: small effect, High: large effect
7	0x2B9(697)	SV Ln DEQ1 High	RT		
8	0x2BA(698)	SV Through	RT		Outputs input signals (L0/R0 and L2/R2) as they are (with a gain of 0dB). Maximizes the variation in speed of the volume.
9	0x2BB(699)	SV Ln Through	RT		Selects the bypass path of the loudness-compensation equalizer.
10	0x2BC(700)	SV Ln Active	RT		Selects the loudness-compensation equalizer path.
11	0x2BF(703)	SV +18.0dB	RT		Selects a target volume value ranging from +18.0dB to −128.0dB in 0.5dB steps (a volume value > −100.0dB) or 2dB steps (a volume value ≤ −100 dB).
12	0x2C0(704)	SV +17.5dB	RT		
13	0x2C1(705)	SV +17.0dB	RT		
14	0x2C2(706)	SV +16.5dB	RT		
15	0x2C3(707)	SV +16.0dB	RT		
16	0x2C4(708)	SV +15.5dB	RT		
17	0x2C5(709)	SV +15.0dB	RT		
18	0x2C6(710)	SV +14.5dB	RT		
19	0x2C7(711)	SV +14.0dB	RT		
20	0x2C8(712)	SV +13.5dB	RT		
21	0x2C9(713)	SV +13.0dB	RT		
22	0x2CA(714)	SV +12.5dB	RT		
23	0x2CB(715)	SV +12.0dB	RT		
24	0x2CC(716)	SV +11.5dB	RT		
25	0x2CD(717)	SV +11.0dB	RT		
26	0x2CE(718)	SV +10.5dB	RT		
27	0x2CF(719)	SV +10.0dB	RT		
28	0x2D0(720)	SV +9.5dB	RT		
29	0x2D1(721)	SV +9.0dB	RT		
30	0x2D2(722)	SV +8.5dB	RT		
31	0x2D3(723)	SV +8.0dB	RT		
32	0x2D4(724)	SV +7.5dB	RT		
33	0x2D5(725)	SV +7.0dB	RT		

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
34	0x2D6(726)	SV +6.5dB	RT		
35	0x2D7(727)	SV +6.0dB	RT		
36	0x2D8(728)	SV +5.5dB	RT		
37	0x2D9(729)	SV +5.0dB	RT		
38	0x2DA(730)	SV +4.5dB	RT		
39	0x2DB(731)	SV +4.0dB	RT		
40	0x2DC(732)	SV +3.5dB	RT		
41	0x2DD(733)	SV +3.0dB	RT		
42	0x2DE(734)	SV +2.5dB	RT		
43	0x2DF(735)	SV +2.0dB	RT		
44	0x2E0(736)	SV +1.5dB	RT		
45	0x2E1(737)	SV +1.0dB	RT		
46	0x2E2(738)	SV +0.5dB	RT		
47	0x2E3(739)	SV 0.0dB	RT		
48	0x2E4(740)	SV −0.5dB	RT		
49	0x2E5(741)	SV −1.0dB	RT		
50	0x2E6(742)	SV −1.5dB	RT		
51	0x2E7(743)	SV −2.0dB	RT		
52	0x2E8(744)	SV −2.5dB	RT		
53	0x2E9(745)	SV −3.0dB	RT		
54	0x2EA(746)	SV −3.5dB	RT		
55	0x2EB(747)	SV −4.0dB	RT		
56	0x2EC(748)	SV −4.5dB	RT		
57	0x2ED(749)	SV −5.0dB	RT		
58	0x2EE(750)	SV −5.5dB	RT		
59	0x2EF(751)	SV −6.0dB	RT		
60	0x2F0(752)	SV −6.5dB	RT		
61	0x2F1(753)	SV −7.0dB	RT		
62	0x2F2(754)	SV −7.5dB	RT		
63	0x2F3(755)	SV −8.0dB	RT		
64	0x2F4(756)	SV −8.5dB	RT		
65	0x2F5(757)	SV −9.0dB	RT		
66	0x2F6(758)	SV −9.5dB	RT		
67	0x2F7(759)	SV −10.0dB	RT		
68	0x2F8(760)	SV −10.5dB	RT		
69	0x2F9(761)	SV −11.0dB	RT		
70	0x2FA(762)	SV −11.5dB	RT		
71	0x2FB(763)	SV −12.0dB	RT		
72	0x2FC(764)	SV −12.5dB	RT		
73	0x2FD(765)	SV −13.0dB	RT		
74	0x2FE(766)	SV −13.5dB	RT		
75	0x2FF(767)	SV −14.0dB	RT		
76	0x300(768)	SV −14.5dB	RT		
77	0x301(769)	SV −15.0dB	RT		
78	0x302(770)	SV −15.5dB	RT		
79	0x303(771)	SV −16.0dB	RT		

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
80	0x304(772)	SV −16.5dB	RT		
81	0x305(773)	SV −17.0dB	RT		
82	0x306(774)	SV −17.5dB	RT		
83	0x307(775)	SV −18.0dB	RT		
84	0x308(776)	SV −18.5dB	RT		
85	0x309(777)	SV −19.0dB	RT		
86	0x30A(778)	SV −19.5dB	RT		
87	0x30B(779)	SV −20.0dB	RT		
88	0x30C(780)	SV −20.5dB	RT		
89	0x30D(781)	SV −21.0dB	RT		
90	0x30E(782)	SV −21.5dB	RT		
91	0x30F(783)	SV −22.0dB	RT		
92	0x310(784)	SV −22.5dB	RT		
93	0x311(785)	SV −23.0dB	RT		
94	0x312(786)	SV −23.5dB	RT		
95	0x313(787)	SV −24.0dB	RT		
96	0x314(788)	SV −24.5dB	RT		
97	0x315(789)	SV −25.0dB	RT		
98	0x316(790)	SV −25.5dB	RT		
99	0x317(791)	SV −26.0dB	RT		
100	0x318(792)	SV −26.5dB	RT		
101	0x319(793)	SV −27.0dB	RT		
102	0x31A(794)	SV −27.5dB	RT		
103	0x31B(795)	SV −28.0dB	RT		
104	0x31C(796)	SV −28.5dB	RT		
105	0x31D(797)	SV −29.0dB	RT		
106	0x31E(798)	SV −29.5dB	RT		
107	0x31F(799)	SV −30.0dB	RT		
108	0x320(800)	SV −30.5dB	RT		
109	0x321(801)	SV −31.0dB	RT		
110	0x322(802)	SV −31.5dB	RT		
111	0x323(803)	SV −32.0dB	RT		
112	0x324(804)	SV −32.5dB	RT		
113	0x325(805)	SV −33.0dB	RT		
114	0x326(806)	SV −33.5dB	RT		
115	0x327(807)	SV −34.0dB	RT		
116	0x328(808)	SV −34.5dB	RT		
117	0x329(809)	SV −35.0dB	RT		
118	0x32A(810)	SV −35.5dB	RT		
119	0x32B(811)	SV −36.0dB	RT		
120	0x32C(812)	SV −36.5dB	RT		
121	0x32D(813)	SV −37.0dB	RT		
122	0x32E(814)	SV −37.5dB	RT		
123	0x32F(815)	SV −38.0dB	RT		
124	0x330(816)	SV −38.5dB	RT		
125	0x331(817)	SV −39.0dB	RT		

No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
126	0x332(818)	SV −39.5dB	RT		
127	0x333(819)	SV −40.0dB	RT		
128	0x334(820)	SV −40.5dB	RT		
129	0x335(821)	SV −41.0dB	RT		
130	0x336(822)	SV −41.5dB	RT		
131	0x337(823)	SV −42.0dB	RT		
132	0x338(824)	SV −42.5dB	RT		
133	0x339(825)	SV −43.0dB	RT		
134	0x33A(826)	SV −43.5dB	RT		
135	0x33B(827)	SV −44.0dB	RT		
136	0x33C(828)	SV −44.5dB	RT		
137	0x33D(829)	SV −45.0dB	RT		
138	0x33E(830)	SV −45.5dB	RT		
139	0x33F(831)	SV −46.0dB	RT		
140	0x340(832)	SV −46.5dB	RT		
141	0x341(833)	SV −47.0dB	RT		
142	0x342(834)	SV −47.5dB	RT		
143	0x343(835)	SV −48.0dB	RT		
144	0x344(836)	SV −48.5dB	RT		
145	0x345(837)	SV −49.0dB	RT		
146	0x346(838)	SV −49.5dB	RT		
147	0x347(839)	SV −50.0dB	RT		
148	0x348(840)	SV −50.5dB	RT		
149	0x349(841)	SV −51.0dB	RT		
150	0x34A(842)	SV −51.5dB	RT		
151	0x34B(843)	SV −52.0dB	RT		
152	0x34C(844)	SV −52.5dB	RT		
153	0x34D(845)	SV −53.0dB	RT		
154	0x34E(846)	SV −53.5dB	RT		
155	0x34F(847)	SV −54.0dB	RT		
156	0x350(848)	SV −54.5dB	RT		
157	0x351(849)	SV −55.0dB	RT		
158	0x352(850)	SV −55.5dB	RT		
159	0x353(851)	SV −56.0dB	RT		
160	0x354(852)	SV −56.5dB	RT		
161	0x355(853)	SV −57.0dB	RT		
162	0x356(854)	SV −57.5dB	RT		
163	0x357(855)	SV −58.0dB	RT		
164	0x358(856)	SV −58.5dB	RT		
165	0x359(857)	SV −59.0dB	RT		
166	0x35A(858)	SV −59.5dB	RT		
167	0x35B(859)	SV −60.0dB	RT		
168	0x35C(860)	SV −60.5dB	RT		
169	0x35D(861)	SV −61.0dB	RT		
170	0x35E(862)	SV −61.5dB	RT		
171	0x35F(863)	SV −62.0dB	RT		

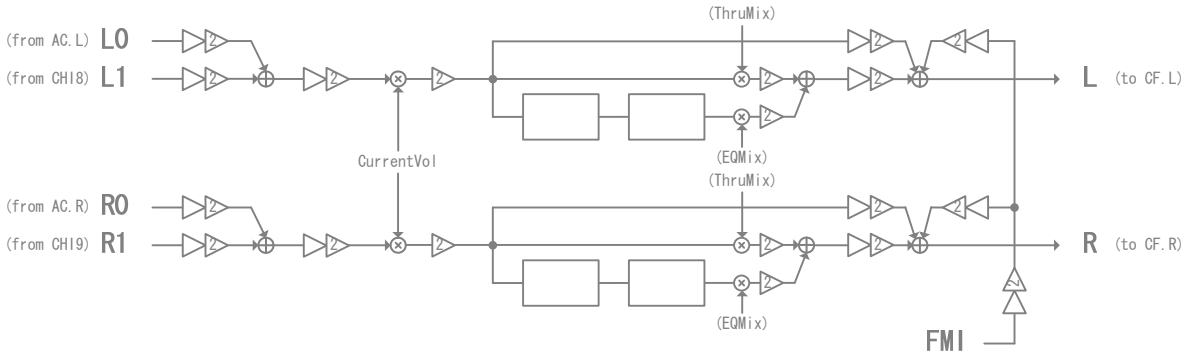
No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
172	0x360(864)	SV −62.5dB	RT		
173	0x361(865)	SV −63.0dB	RT		
174	0x362(866)	SV −63.5dB	RT		
175	0x363(867)	SV −64.0dB	RT		
176	0x364(868)	SV −64.5dB	RT		
177	0x365(869)	SV −65.0dB	RT		
178	0x366(870)	SV −65.5dB	RT		
179	0x367(871)	SV −66.0dB	RT		
180	0x368(872)	SV −66.5dB	RT		
181	0x369(873)	SV −67.0dB	RT		
182	0x36A(874)	SV −67.5dB	RT		
183	0x36B(875)	SV −68.0dB	RT		
184	0x36C(876)	SV −68.5dB	RT		
185	0x36D(877)	SV −69.0dB	RT		
186	0x36E(878)	SV −69.5dB	RT		
187	0x36F(879)	SV −70.0dB	RT		
188	0x370(880)	SV −70.5dB	RT		
189	0x371(881)	SV −71.0dB	RT		
190	0x372(882)	SV −71.5dB	RT		
191	0x373(883)	SV −72.0dB	RT		
192	0x374(884)	SV −72.5dB	RT		
193	0x375(885)	SV −73.0dB	RT		
194	0x376(886)	SV −73.5dB	RT		
195	0x377(887)	SV −74.0dB	RT		
196	0x378(888)	SV −74.5dB	RT		
197	0x379(889)	SV −75.0dB	RT		
198	0x37A(890)	SV −75.5dB	RT		
199	0x37B(891)	SV −76.0dB	RT		
200	0x37C(892)	SV −76.5dB	RT		
201	0x37D(893)	SV −77.0dB	RT		
202	0x37E(894)	SV −77.5dB	RT		
203	0x37F(895)	SV −78.0dB	RT		
204	0x380(896)	SV −78.5dB	RT		
205	0x381(897)	SV −79.0dB	RT		
206	0x382(898)	SV −79.5dB	RT		
207	0x383(899)	SV −80.0dB	RT		
208	0x384(900)	SV −80.5dB	RT		
209	0x385(901)	SV −81.0dB	RT		
210	0x386(902)	SV −81.5dB	RT		
211	0x387(903)	SV −82.0dB	RT		
212	0x388(904)	SV −82.5dB	RT		
213	0x389(905)	SV −83.0dB	RT		
214	0x38A(906)	SV −83.5dB	RT		
215	0x38B(907)	SV −84.0dB	RT		
216	0x38C(908)	SV −84.5dB	RT		
217	0x38D(909)	SV −85.0dB	RT		

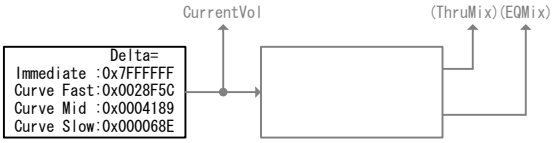
No.	On-chip ROM Block Number	Name	MDSP2	Transfer Destination	Description
218	0x38E(910)	SV −85.5dB	RT		
219	0x38F(911)	SV −86.0dB	RT		
220	0x390(912)	SV −86.5dB	RT		
221	0x391(913)	SV −87.0dB	RT		
222	0x392(914)	SV −87.5dB	RT		
223	0x393(915)	SV −88.0dB	RT		
224	0x394(916)	SV −88.5dB	RT		
225	0x395(917)	SV −89.0dB	RT		
226	0x396(918)	SV −89.5dB	RT		
227	0x397(919)	SV −90.0dB	RT		
228	0x398(920)	SV −90.5dB	RT		
229	0x399(921)	SV −91.0dB	RT		
230	0x39A(922)	SV −91.5dB	RT		
231	0x39B(923)	SV −92.0dB	RT		
232	0x39C(924)	SV −92.5dB	RT		
233	0x39D(925)	SV −93.0dB	RT		
234	0x39E(926)	SV −93.5dB	RT		
235	0x39F(927)	SV −94.0dB	RT		
236	0x3A0(928)	SV −94.5dB	RT		
237	0x3A1(929)	SV −95.0dB	RT		
238	0x3A2(930)	SV −95.5dB	RT		
239	0x3A3(931)	SV −96.0dB	RT		
240	0x3A4(932)	SV −96.5dB	RT		
241	0x3A5(933)	SV −97.0dB	RT		
242	0x3A6(934)	SV −97.5dB	RT		
243	0x3A7(935)	SV −98.0dB	RT		
244	0x3A8(936)	SV −98.5dB	RT		
245	0x3A9(937)	SV −99.0dB	RT		
246	0x3AA(938)	SV −99.5dB	RT		
247	0x3AB(939)	SV −100.0dB	RT		
248	0x3AC(940)	SV −102.0dB	RT		
249	0x3AD(941)	SV −104.0dB	RT		
250	0x3AE(942)	SV −106.0dB	RT		
251	0x3AF(943)	SV −108.0dB	RT		
252	0x3B0(944)	SV −110.0dB	RT		
253	0x3B1(945)	SV −112.0dB	RT		
254	0x3B2(946)	SV −114.0dB	RT		
255	0x3B3(947)	SV −116.0dB	RT		
256	0x3B4(948)	SV −118.0dB	RT		
257	0x3B5(949)	SV −120.0dB	RT		
258	0x3B6(950)	SV −122.0dB	RT		
259	0x3B7(951)	SV −124.0dB	RT		
260	0x3B8(952)	SV −126.0dB	RT		
261	0x3B9(953)	SV −128.0dB	RT		

[Note]

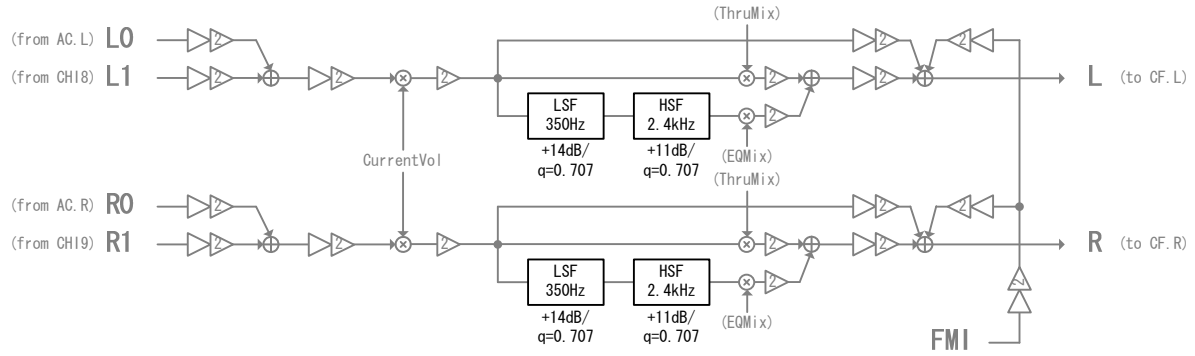
- The preset pattern with “RT” in the MDSP2 column should be executed during MDSP2 operation.
- With the preset pattern whose Transfer Destination column is blank, a transfer destination start address needs not to be specified.

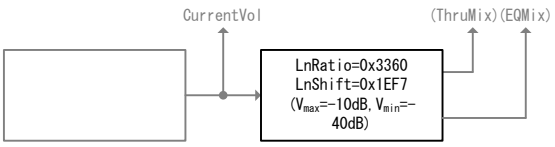
● 690−693: SV Immediate/SV Curve * (*=Fast/Mid/Slow)

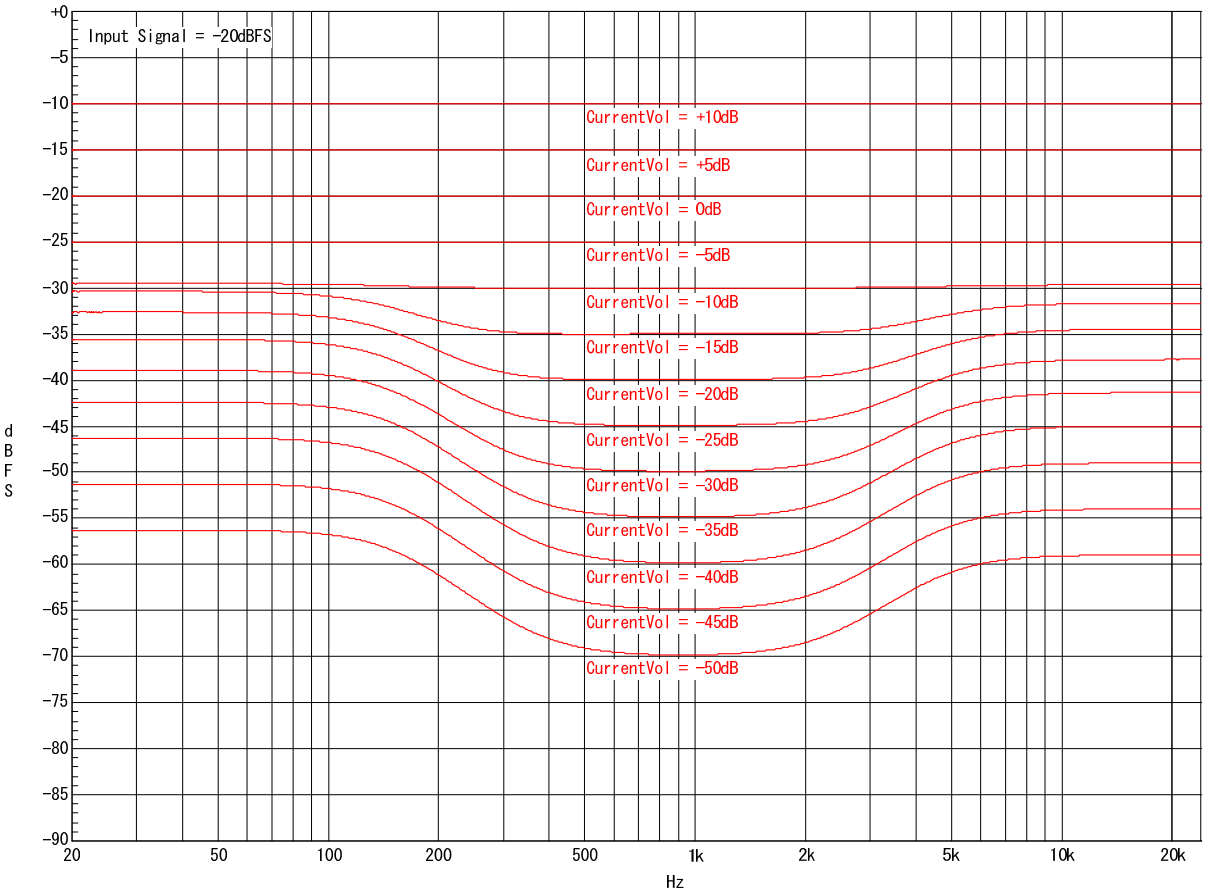




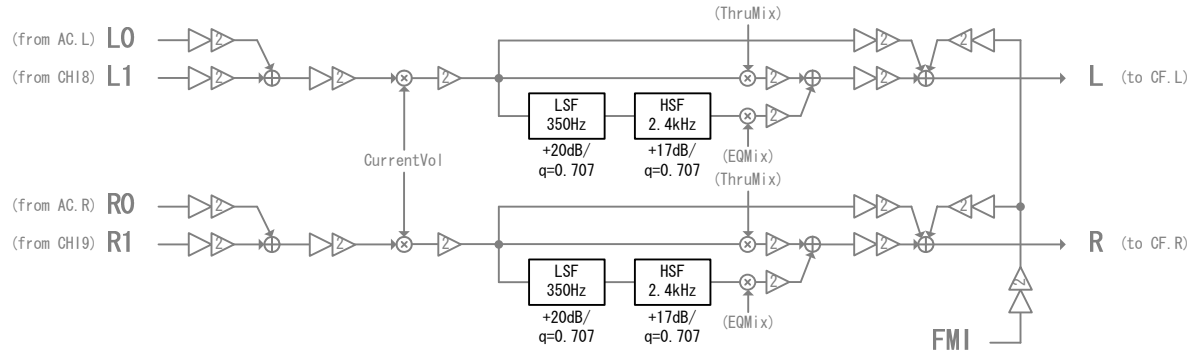
● 694: SV Ln DEQ0 Low

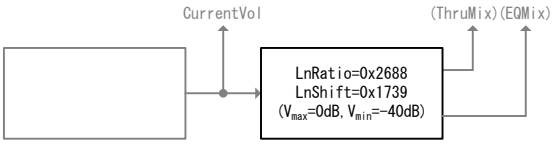


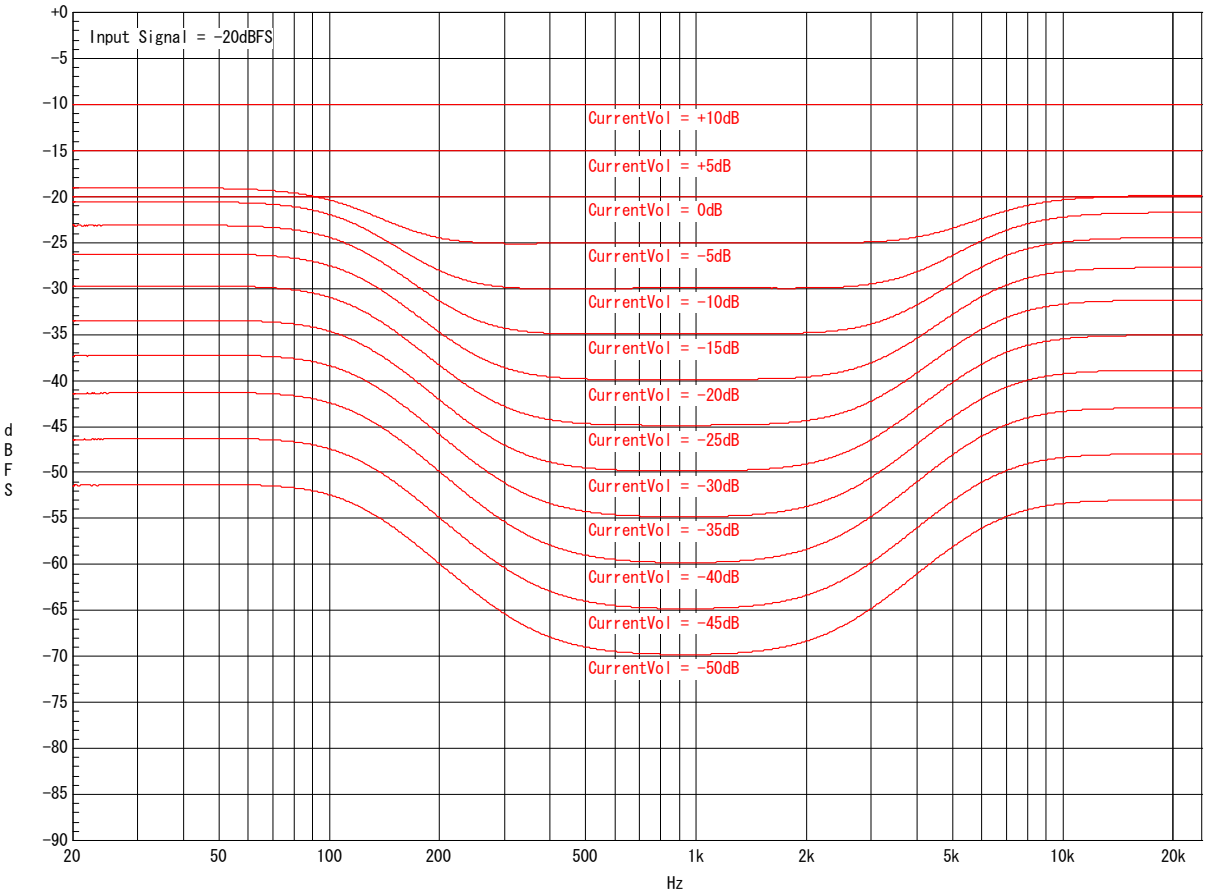




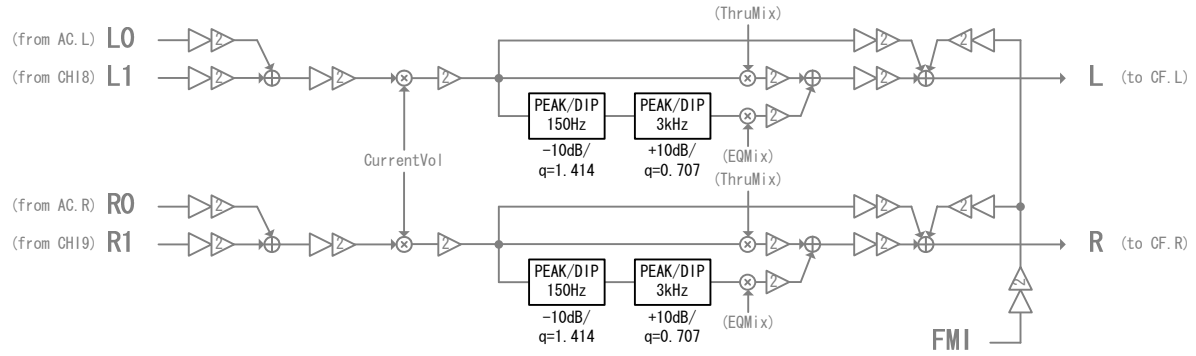
- **695: SV Ln DEQ0 High**

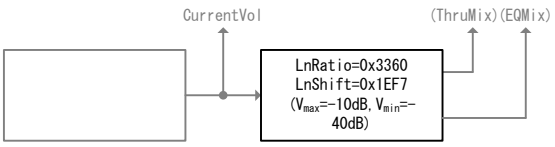


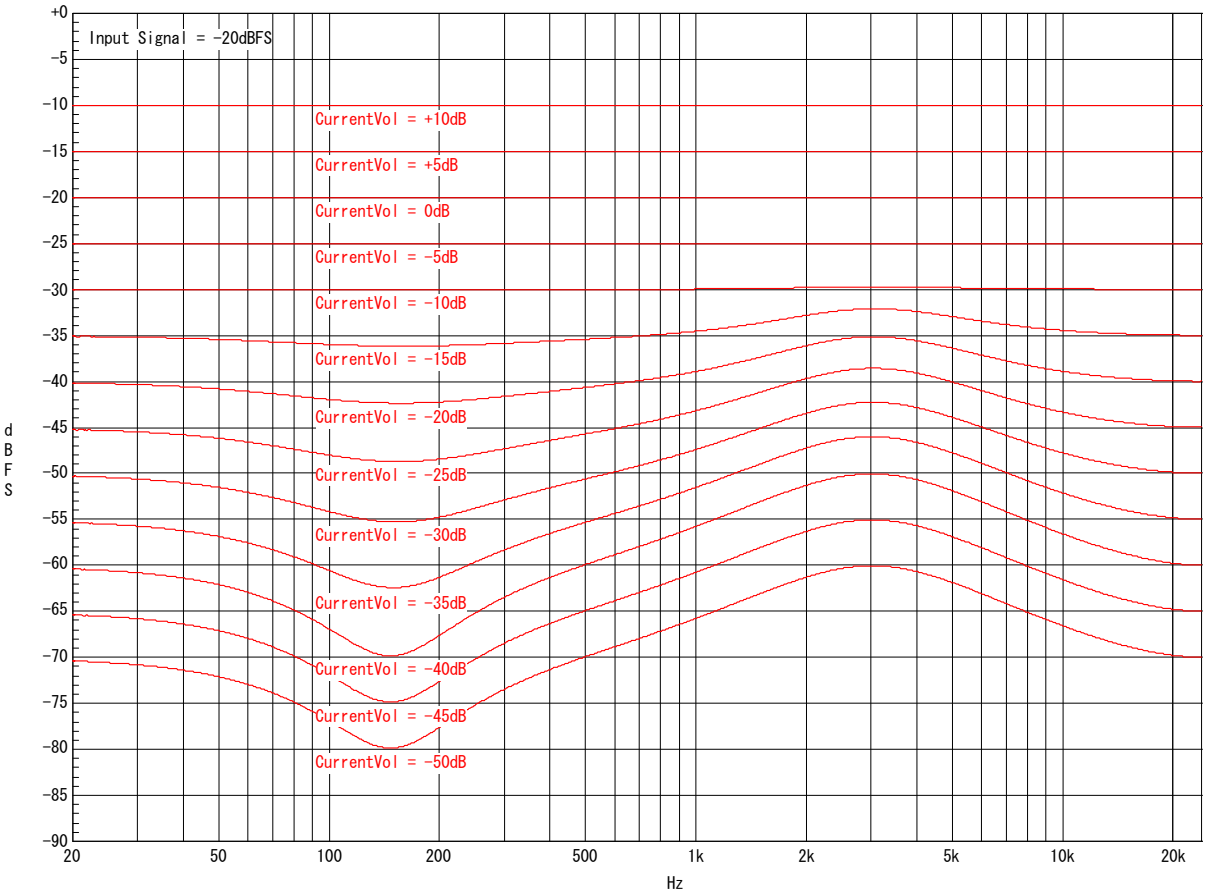




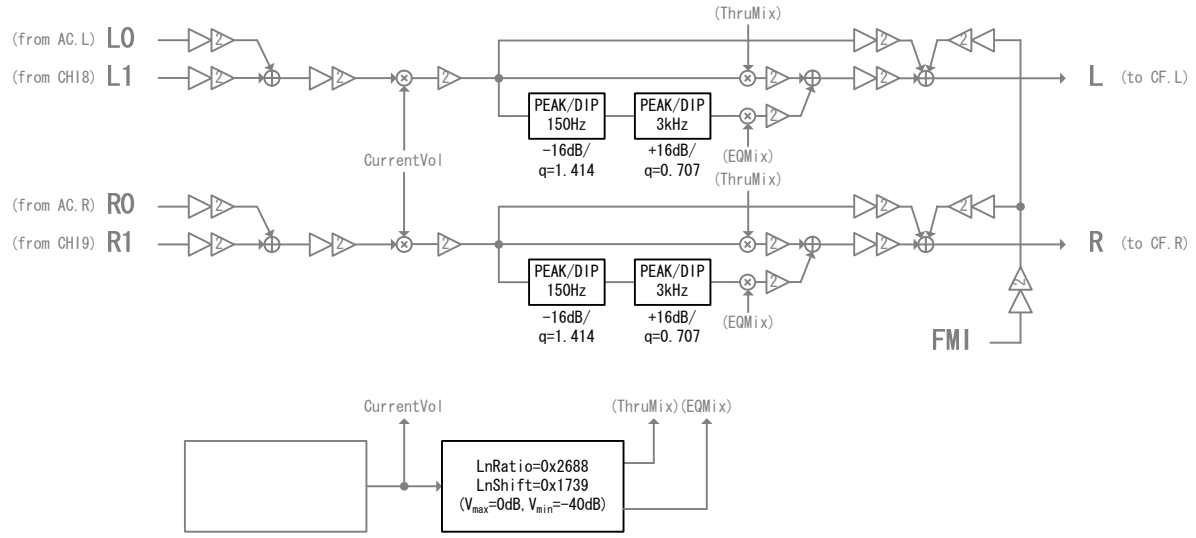
- **696: SV Ln DEQ1 Low**

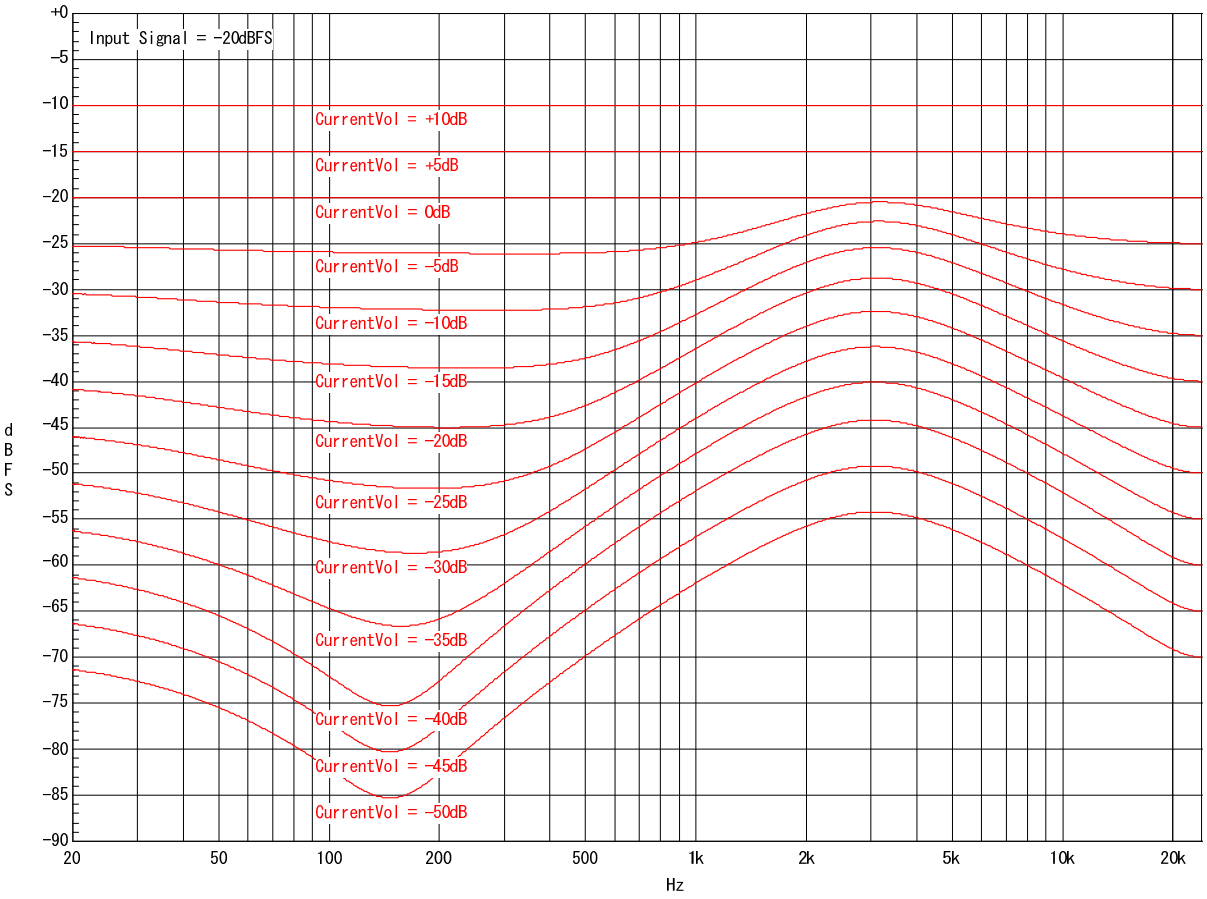




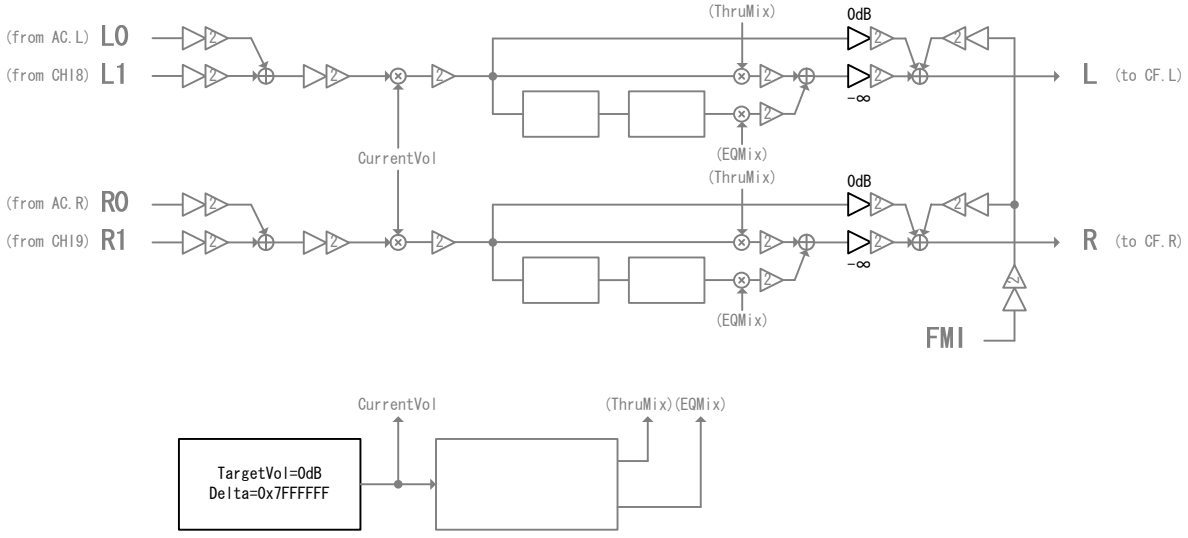


- **697: SV Ln DEQ1 High**

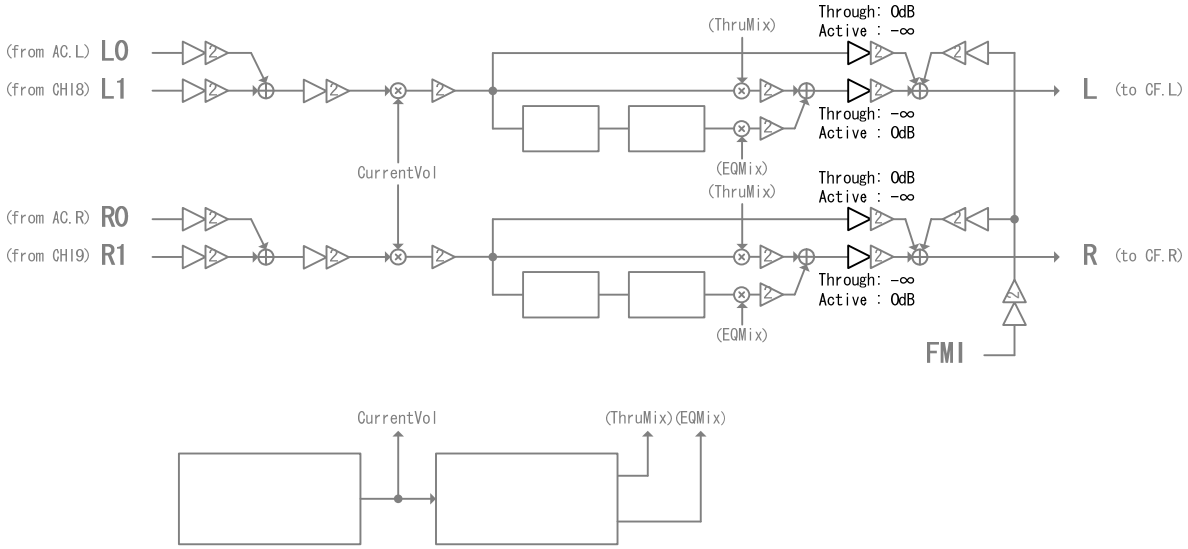




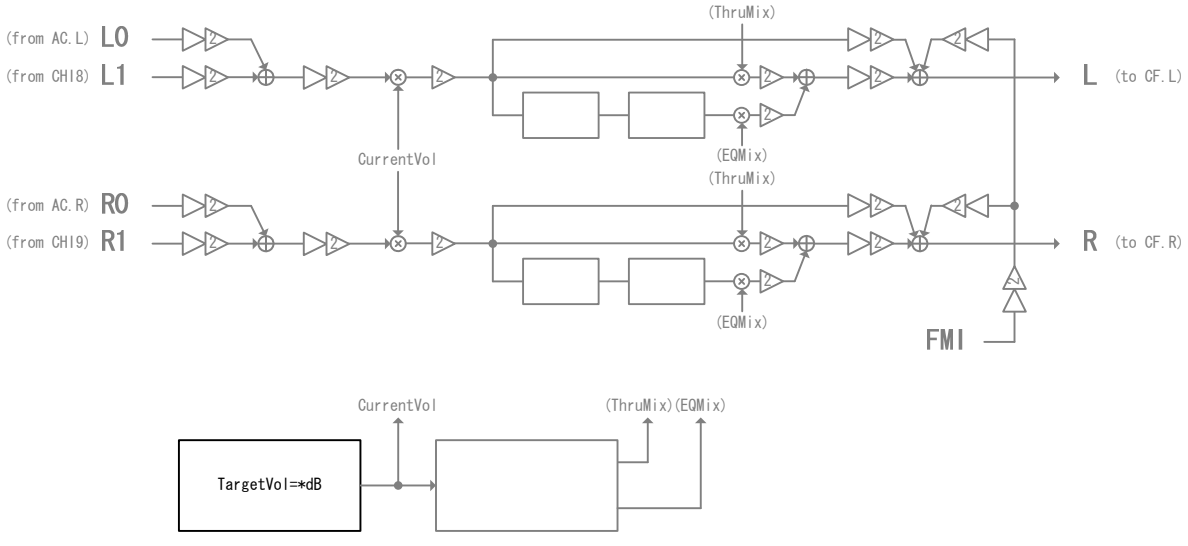
- **698: SV Through**



- **699−700: SV Ln Through/SV Ln Active**



- **703−953: SV *dB (*=+18 to −128)**



4 Control Method

4.1 Example of Basic Control

The following shows an example of host controller controls.

[Note]

- In the following tables, the microprocessor commands used for control is described in Host Access column. (WRITE, PRESETROM0, PRESETROM2, and PRESETROM3 are commands, and the codes of each command are WRITE=0x80, PRESETROM0=0x70, PRESETROM2=0x72, and PRESETROM3=0x73.) See "YDA174 /YSS952 Application Manual" for the detail of commands.

4.1.1 DD-2SP Initializations

An example of initializing DD-2SP is shown below (DSE mode is used as the firmware mode). Perform the following steps (1) to (18). Also, the firmware-related functions are set as follows:

- Secure 8-bit headroom.
- FM sound signals are mixed.
- The following functions or effects are disabled: small signal detection, surround, band expansion, acoustic compensation, loudness, output power limiter, and soft clip.
- The network configuration is the 2.1 channel configuration.
- The master volume is set to −30dB. The sound volume varies smoothly.

And, this example assumes the following:

- AIF mode is set to 0.
- The SRC input signal is processed. And the high frequency range signal is output to the digital amplifier, the low frequency range signal is output to the SDO1 path.

4.1.1-1 Hardware Start Up

No.	Controls		Host Access
(1)	Follow step (A) - (C) to start up the hardware.		
	(A)	Set IC_N pin and SLEEP_N pin to "L" to power up each power supply.	IC_N pin="L" SLEEP_N pin="L"
	(B)	Wait for more than 10 ms until the external clock and PLL are stabilized and make the transition from hardware reset mode to startup/reset setting mode.	IC_N pin="L"→"H"
	(C)	Wait for more than 1ms after the above (B) then shift to the ordinary state.	SLEEP_N pin="L"→"H"

4.1.1-2 Firmware Mode Setting

No.	Controls	Host Access
(2)	Set DSE mode firmware. Write instruction codes in the instruction codes file "EVB-DD2SP \Firmware\Instruction\DD-2inst_DSE.mdspcfg" from the top of MPRAM.	WRITE 0x4400 [1,535word × 40bit]

4.1.1-3 Firmware Coefficient Setting

No.	Controls		Host Access
(3)	Set Top firmware coefficients (Top.TopData0[15:0]=0x4000, Top.TopData1[15:0]=0x2000, Top.TopData2[15:0]=0x8000, Top.TopData3[15:0]=0xC000, Top.TopData4[15:0]=0x0008, Top.TopData5[15:0]=0x0001).		WRITE 0x4000 0x4000 0x2000 0x8000 0xC000 0x0008 0x0001
(4)	Set Input level detector firmware coefficients. In this example, execute step (A) - (C).		
	(A)	Select SRC path (ILD.SDI0Sel[15:0]=0x4000, ILD.SDI1Sel[15:0]=0x0000).	WRITE 0x400B 0x4000 0x0000
	(B)	Secure 3-bit headroom (ILD.Att[15:0]=0x0800).	WRITE 0x400D 0x0800
	(C)	Disable the small signal detection function (ILD.DetLev[15:0]=0x0000, ILD.DetTime[15:0]= 0x0001, ILD.DetRst[15:0]=0x0000).	WRITE 0x400E 0x0000 0x0001 0x0000
(5)	Set Spacious sound 3D firmware coefficients. In this example, execute step (A) and (B).		
	(A)	Set the S3D core coefficients, the filter coefficients and the gain coefficients (The coefficients S3D.S3DCore. Data0[15:0] through S3D.S3DLev[15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample\MDSP\DD-2coef_S3D_Natural. mdspcfg").	WRITE 0x409D [153word×16bit]
	(B)	Disable the effect (S3D.ThruSel[15:0]=0x4000, S3D.S3DSel[15:0]=0x0000).	WRITE 0x4136 0x4000 0x0000
(6)	Set Harmonics enhancer Extended firmware coefficients. In this example, execute step (A) and (B).		
	(A)	Set the HXT core coefficients and the gain coefficients (The coefficients HXT.HXTCore.Data0 [15:0] through HXT.WetMix[15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample\MDSP\DD-2coef_HXT_Bass+High1.mdspcfg").	WRITE 0x4149 [77word×16bit]
	(B)	Disable the effect (HXT.ThruSel[15:0]=0x4000, HXT.HXTSel[15:0]=0x0000).	WRITE 0x4196 0x4000 0x0000
(7)	Set Acoustic total-linear EQ core firmware coefficients. In this example, execute step (A) - (C).		
	(A)	Secure 2-bit headroom (AC.Att[15:0]=0x1000).	WRITE 0x41F2 0x1000
	(B)	Set the AEQ core coefficients and the gain coefficients (The coefficients AC.AEQCore. Data0[15:0] through AC.RPostLev[15:0] in the sample coefficients file "EVB-DD2SP \Firmware\Sample\MDSP\DD-2coef_AC_AEQOn.mdspcfg").	WRITE 0x41F3 [516word×16bit]
	(C)	Disable the effect (AC.ThruSel[15:0]=0x4000, AC.ACSel[15:0]=0x0000).	WRITE 0x43F7 0x4000 0x0000
(8)	Set Smooth volume firmware coefficients. In this example, execute step (A) - (F).		
	(A)	Set the following headrooms: - 3-bit headroom provided for the main signal (SV.Att[15:0]=0x0800). - 10-bit headroom provided for the FM sound signal (SV.FMAtt[15:0]=0x0010).	WRITE 0x4034 0x0800 0x0010
	(B)	Mix the FM sound signal (SV.FMLMix[15:0]=SV.FMRMix[15:0]=0x0800).	WRITE 0x4036 0x0800 0x0800
	(C)	Mute the master volume (SV.NMute[15:0]=0x0000).	WRITE 0x403B 0x0000
	(D)	Bypass SDSP 10-band PEQ processing (SV. BypassSel[15:0]=0x4000, SV.10bPEQSel [15:0]= 0x0000).	WRITE 0x4042 0x4000 0x0000
	(E)	Set the loudness coefficients (The coefficients SV.EQ0.a0[15:0] through SV.LnShift[15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample\MDSP\DD-2coef_SV_ VolumeLinkedEQOn.mdspcfg").	WRITE 0x4044 [12word×16bit]
	(F)	Disable the loudness effect (SV.LnSel[15:0]=0x0000, SV.LnThruSel[15:0]=0x4000).	WRITE 0x4050 0x0000 0x4000
(9)	Set Crossover filter firmware coefficients. In this example, set the network configuration to the 2.1 channel configuration. The crossover frequency is 280Hz. (The coefficients CF.HPF.a0[27:12] through CF.LThruSel[15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample \MDSP\DD-2coef_CF_2.1ChannelButterworth.mdspcfg".)		WRITE 0x41C3 [45word×16bit]

No.	Controls		Host Access
(10)	Set Limiter firmware coefficients. In this example, execute step (A) - (I).		
	(A)	Balance: Center position (LMT.HiLBal[15:0]=LMT.HiRBal[15:0]=LMT.LoLBal[15:0]= LMT.LoRBal[15:0]=0x4000).	WRITE 0x4066 0x4000 0x4000 0x4000 0x4000
	(B)	Set the gain control coefficients (The coefficients LMT.HGC.GainShift[15:0] through LMT.LATK.b1[11:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample \MDSP\DD-2coef_LMT_PowerLimit2.mdspcfg").	WRITE 0x406A [23word×16bit]
	(C)	Disable the gain control function (LMT.HGCThruSel[15:0]=LMT.LGCThruSel[15:0]= 0x4000, LMT.HGCSel[15:0]=LMT.LGCSel[15:0]=0x0000).	WRITE 0x4081 0x4000 0x0000 0x4000 0x0000
	(D)	Cancel 7-bit headroom for the high and low frequency range signal (LMT.HiTrim[15:0]= LMT.LoTrim[15:0]=0x4000, LMT.HiLevAdj[3:0]=LMT.LoLevAdj[3:0]=0x7).	WRITE 0x4085 0x4000 0x4000 0x0007 0x0007
	(E)	Set the soft clip coefficients (The coefficients LMT.PreLev[15:0] through LMT.CompLev [15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample\MDSP\DD-2coef_ LMT_SoftClip.mdspcfg").	WRITE 0x4089 [3word×16bit]
	(F)	Disable the soft clipping (LMT.SCThruSel[15:0]=0x4000, LMT.SCSel[15:0]= 0x0000).	WRITE 0x408C 0x4000 0x0000
	(G)	Don't mix the low frequency range signal with the high frequency range signal (LMT.LoMix [15:0]=0x0000).	WRITE 0x408E 0x0000
	(H)	Output the high frequency range signal with stereo (LMT.SMix[15:0]=0x4000, LMT.XMix[15:0]= 0x0000).	WRITE 0x408F 0x4000 0x0000
	(I)	Output the high frequency range signal to the digital amplifier, and output the low frequency range signal to the SDO1 path (LMT.LAmpOut[15:0]=LMT.RAmpOut[15:0]=0x2000, LMT.LSDO0Out[15:0]= LMT.RSDO0Out[15:0]=0x0000, LSDO1Out[15:0]=RSDO1Out[15:0]=0x4000).	WRITE 0x4091 0x2000 0x2000 0x0000 0x0000 0x4000 0x4000

4.1.1-4 SDSP 10-band PEQ Coefficient Setting

No.	Controls	Host Access
(11)	Set SDSP 10-band PEQ coefficients (The coefficients in the sample coefficients file "EVB-DD2SP\Firmware\Sample\SDSP\DD-2coef_AEQOn.sdspcfg").	WRITE 0x8000 [70word×24bit]

4.1.1-5 Hardware Setting

No.	Controls		Host Access
(12)	Set AIF mode to 0 (0x07 AIFMD: PI=1, PIO=0, AIFMD[3:0]=0).		0x07 0x20
(13)	Set WRAM memory mode to 20 bits (0x0A MDSPMD: WRAMMD=0). And, set the bit width of the runtime transfer data to 16 bits (0x0A MDSPMD: WRAMRTMD=1).		0x0A 0x02
(14)	Set the digital amplifier output gain to +6 dB (0x2F GAIN: GAIN[1:0]=01).		0x2F 0x01
(15)	Set other registers as needed. In this example, set (A) through (F).		
	(A)	Set the audio input format to I^2S format (0x08 AIFIFMT: SDIFMT[1:0]=10, SDIBIT[1:0]=00, SDIWCKP=1, SDIBCKP=1).	0x08 0x23
	(B)	Set the audio output format to I^2S format (0x09 AIFOFMT: SDOFMT[1:0]=10, SDOBIT[1:0]=00, SDOWCKP=1, SDOBCKP=1).	0x09 0x23
	(C)	Set SDSP operations as follows: ・Enable the DC-block filter (0x0B SDSPMD: DCCOFF=0). ・Disable the deemphasis filter (0x0B SDSPMD: DEMON=0). ・Set SRC operation for interpolation (0x0B SDSPMD: DCM=0).	0x0B 0x00
	(D)	Leave the digital amplifier carrier frequency unchanged (0x0C DAMPMD: PWMFHOP=0).	0x0C 0x60
	(E)	SDSP output sampling frequency is 48kHz (0x0E FSM: FSM[1:0]=00).	0x0E 0x00
	(F)	Enable the PLL error report (0x23 PLLERR: PLLERRE=1).	0x23 0x04

4.1.1-6 DSP Start Up

No.	Controls	Host Access
(16)	Activate both MDSP2 and SDSP (0x11 DSPSTART: MDSPSTART=1, SDSPSTART=1).	0x11 0x03

4.1.1-7 Preset Pattern Setting

No.	Controls		Host Access
(17)	Specify a coefficient set to be executed with a ROM block number as needed. In this example, execute step (A) and (B).		
	(A)	Make the change speed of the master volume smooth ([692(0x2B4):SV Curve Mid]).	PRESETROM2 0xB4
	(B)	Set the master volume to −30dB ([799(0x31F):SV -30.0dB]).	PRESETROM3 0x1F

4.1.1-8 Output Setting

No.	Controls		Host Access
(18)	Follow step (A) - (C) to start generating sound.		
	(A)	Wait until the digital amplifier startup sequence is completed (after waiting up to 107 ms after No. (1)-(C)).	-
	(B)	Cancel the mute state of MDSP2, SDSP, and the digital amplifier (0x10 MUTE: MDSPMUTEN=SDSPMUTEN=QMUTEN=1).	10 0x0B
	(C)	Cancel the mute of the master volume (SV.NMute[15:0]=0x4000).	WRITE 0x403B 0x4000

4.1.2 SPR-2 Initializations

An example of initializing SPR-2 is shown below (DSE mode is used as the firmware mode). Perform the following steps (1) to (18). Also, the firmware-related functions are set as follows:

- Secure 8-bit headroom.
- FM sound signals are mixed.
- The following functions or effects are disabled: small signal detection, surround, band expansion, acoustic compensation, loudness, output power limiter, and soft clip.
- The network configuration is the 2.1 channel configuration.
- The master volume is set to −12dB. The sound volume varies smoothly.

And, this example assumes the following:

- AIF mode is set to 0.
- The SRC input signal is processed. And the high frequency range signal is output to the SDO0 path, the low frequency range signal is output to the SDO1 path.

4.1.2-1 Hardware Start Up

No.	Controls		Host Access
(1)	Follow step (A) and (B) to start up the hardware.		
	(A)	Set IC_N pin to “L” to power up each power supply.	IC_N pin=“L”
	(B)	Wait for more than 10 ms until the external clock and PLL are stabilized and make the transition from hardware reset mode to startup/reset setting mode.	IC_N pin=“L”→“H”

4.1.2-2 Firmware Mode Setting

No.	Controls	Host Access
(2)	Set DSE mode firmware. Write instruction codes in the instruction codes file “EVB-SPR2 \Firmware\Instruction\DD-2inst_DSE.mdspcfg” from the top of MPRAM.	WRITE 0x4400 [1,535word × 40bit]

4.1.2-3 Firmware Coefficient Setting

No.	Controls		Host Access
(3)	Set Top firmware coefficients (Top.TopData0[15:0]=0x4000, Top.TopData1[15:0]=0x2000, Top.TopData2[15:0]=0x8000, Top.TopData3[15:0]=0xC000, Top.TopData4[15:0]=0x0008, Top.TopData5[15:0]=0x0001).		WRITE 0x4000 0x4000 0x2000 0x8000 0xC000 0x0008 0x0001
(4)	Set Input level detector firmware coefficients. In this example, execute step (A) - (C).		
	(A)	Select SRC path (ILD.SDI0Sel[15:0]=0x4000, ILD.SDI1Sel[15:0]=0x0000).	WRITE 0x400B 0x4000 0x0000
	(B)	Secure 3-bit headroom (ILD.Att[15:0]=0x0800).	WRITE 0x400D 0x0800
	(C)	Disable the small signal detection function (ILD.DetLev[15:0]=0x0000, ILD.DetTime[15:0]= 0x0001, ILD.DetRst[15:0]=0x0000).	WRITE 0x400E 0x0000 0x0001 0x0000
(5)	Set Spacious sound 3D firmware coefficients. In this example, execute step (A) and (B).		
	(A)	Set the S3D core coefficients, the filter coefficients and the gain coefficients (The coefficients S3D.S3DCore. Data0[15:0] through S3D.S3DLev[15:0] in the sample coefficients file "EVB-SPR2\Firmware\Sample\MDSP\DD-2coef_S3D_Natural. mdspcfg").	WRITE 0x409D [153word×16bit]
	(B)	Disable the effect (S3D.ThruSel[15:0]=0x4000, S3D.S3DSel[15:0]=0x0000).	WRITE 0x4136 0x4000 0x0000
(6)	Set Harmonics enhancer Extended firmware coefficients. In this example, execute step (A) and (B).		
	(A)	Set the HXT core coefficients and the gain coefficients (The coefficients HXT.HXTCore. Data0 [15:0] through HXT.WetMix[15:0] in the sample coefficients file "EVB-SPR2 \Firmware\Sample\MDSP\DD-2coef_HXT_Bass+High1.mdspcfg").	WRITE 0x4149 [77word×16bit]
	(B)	Disable the effect (HXT.ThruSel[15:0]=0x4000, HXT.HXTSel[15:0]=0x0000).	WRITE 0x4196 0x4000 0x0000
(7)	Set Acoustic total-linear EQ core firmware coefficients. In this example, execute step (A) - (C).		
	(A)	Secure 2-bit headroom (AC.Att[15:0]=0x1000).	WRITE 0x41F2 0x1000
	(B)	Set the AEQ core coefficients and the gain coefficients (The coefficients AC.AEQCore. Data0[15:0] through AC.RPostLev[15:0] in the sample coefficients file "EVB-SPR2 \Firmware\Sample\MDSP\DD-2coef_AC_AEQOn.mdspcfg").	WRITE 0x41F3 [516word×16bit]
	(C)	Disable the effect (AC.ThruSel[15:0]=0x4000, AC.ACSel[15:0]=0x0000).	WRITE 0x43F7 0x4000 0x0000
(8)	Set Smooth volume firmware coefficients. In this example, execute step (A) - (F).		
	(A)	Set the following headrooms: - 3-bit headroom provided for the main signal (SV.Att[15:0]=0x0800). - 10-bit headroom provided for the FM sound signal (SV.FMAtt[15:0]=0x0010).	WRITE 0x4034 0x0800 0x0010
	(B)	Mix the FM sound signal (SV.FMLMix[15:0]=SV.FMRMix[15:0]=0x0800).	WRITE 0x4036 0x0800 0x0800
	(C)	Mute the master volume (SV.NMute[15:0]=0x0000).	WRITE 0x403B 0x0000
	(D)	Bypass SDSP 10-band PEQ processing (SV. BypassSel[15:0]=0x4000, SV.10bPEQSel [15:0]= 0x0000).	WRITE 0x4042 0x4000 0x0000
	(E)	Set the loudness coefficients (The coefficients SV.EQ0.a0[15:0] through SV.LnShift[15:0] in the sample coefficients file "EVB-SPR2\Firmware\Sample\MDSP\DD-2coef_SV_ VolumeLinkedEQOn.mdspcfg").	WRITE 0x4044 [12word×16bit]
	(F)	Disable the loudness effect (SV.LnSel[15:0]=0x0000, SV.LnThruSel[15:0]=0x4000).	WRITE 0x4050 0x0000 0x4000
(9)	Set Crossover filter firmware coefficients. In this example, set the network configuration to the 2.1 channel configuration. The crossover frequency is 280Hz. (The coefficients CF.HPF.a0[27:12] through CF.LThruSel[15:0] in the sample coefficients file "EVB-DD2SP\Firmware\Sample \MDSP\DD-2coef_CF_2.1ChannelButterworth.mdspcfg".)		WRITE 0x41C3 [45word×16bit]

No.	Controls		Host Access
(10)	Set Limiter firmware coefficients. In this example, execute step (A) - (I).		
	(A)	Balance: Center position (LMT.HiLBal[15:0]=LMT.HiRBal[15:0]=LMT.LoLBal[15:0]= LMT.LoRBal[15:0]=0x4000).	WRITE 0x4066 0x4000 0x4000 0x4000 0x4000
	(B)	Set the gain control coefficients (The coefficients LMT.HGC.GainShift[15:0] through LMT.LATK.b1[11:0] in the sample coefficients file "EVB-SPR2\Firmware\Sample \MDSP\DD-2coef_LMT_PowerLimit2.mdspcfg").	WRITE 0x406A [23word×16bit]
	(C)	Disable the gain control function (LMT.HGCThruSel[15:0]=LMT.LGCThruSel[15:0]= 0x4000, LMT.HGCSel[15:0]=LMT.LGCSel[15:0]=0x0000).	WRITE 0x4081 0x4000 0x0000 0x4000 0x0000
	(D)	Cancel 7-bit headroom for the high and low frequency range signal (LMT.HiTrim[15:0]= LMT.LoTrim[15:0]=0x4000, LMT.HiLevAdj[3:0]=LMT.LoLevAdj[3:0]=0x7).	WRITE 0x4085 0x4000 0x4000 0x0007 0x0007
	(E)	Set the soft clip coefficients (The coefficients LMT.PreLev[15:0] through LMT.CompLev [15:0] in the sample coefficients file "EVB-SPR2\Firmware\Sample\MDSP\DD-2coef_ LMT_SoftClip.mdspcfg").	WRITE 0x4089 [3word×16bit]
	(F)	Disable the soft clipping (LMT.SCThruSel[15:0]=0x4000, LMT.SCSel[15:0]= 0x0000).	WRITE 0x408C 0x4000 0x0000
	(G)	Don't mix the low frequency range signal with the high frequency range signal (LMT.LoMix [15:0]=0x0000).	WRITE 0x408E 0x0000
	(H)	Output the high frequency range signal with stereo (LMT.SMix[15:0]=0x4000, LMT.XMix[15:0]= 0x0000).	WRITE 0x408F 0x4000 0x0000
	(I)	Output the high frequency range signal to the SDO0 path, and output the low frequency range signal to the SDO1 path (LMT.LAmpOut[15:0]=LMT.RAmpOut[15:0]=0x0000, LMT.LSDO0Out[15:0]= LMT.RSDO0Out[15:0]=0x4000, LSDO1Out[15:0]=RSDO1Out[15:0]=0x4000).	WRITE 0x4091 0x0000 0x0000 0x4000 0x4000 0x4000 0x4000

4.1.2-4 SDSP 10-band PEQ Coefficient Setting

No.	Controls	Host Access
(12)	Set SDSP 10-band PEQ coefficients (The coefficients in the sample coefficients file "EVB-SPR2\Firmware\Sample\SDSP\DD-2coef_AEQOn.sdspcfg").	WRITE 0x8000 [70word×24bit]

4.1.2-5 Hardware Setting

No.	Controls		Host Access
(13)	Set AIF mode to 0 (0x07 AIFMD: PI=1, PIO=0, AIFMD[3:0]=0).		0x07 0x20
(14)	Set WRAM memory mode to 20 bits (0x0A MDSPMD: WRAMMD=0). And, set the bit width of the runtime transfer data to 16 bits (0x0A MDSPMD: WRAMRTMD=1).		0x0A 0x02
(15)	Set other registers as needed. In this example, set (A) through (F).		
	(A)	Set the audio input format to I^2S format (0x08 AIFIFMT: SDIFMT[1:0]=10, SDIBIT[1:0]= 00, SDIWCKP=1, SDIBCKP=1).	0x08 0x23
	(B)	Set the audio output format to I^2S format (0x09 AIFOFMT: SDOFMT[1:0]=10, SDOBIT [1:0]=00, SDOWCKP=1, SDOBCKP=1).	0x09 0x23
	(C)	Set SDSP operations as follows: ・Disable the deemphasis filter (0x0B SDSPMD: DEMON=0). ・Set SRC operation for interpolation (0x0B SDSPMD: DCM=0).	0x0B 0x00
	(D)	SDSP output sampling frequency is 48kHz (0x0E FSM: FSM[1:0]=00).	0x0E 0x00
	(E)	Enable the PLL error report (0x23 PLLERR: PLLERRE=1).	0x23 0x04

4.1.2-6 DSP Start Up

No.	Controls	Host Access
(16)	Activate both MDSP2 and SDSP (0x11 DSPSTART: MDSPSTART=1, SDSPSTART=1).	0x11 0x03

4.1.2-7 Preset Pattern Setting

No.	Controls		Host Access
(17)	Specify a coefficient set to be executed with a ROM block number as needed. In this example, execute step (A) and (b).		
	(A)	Make the change speed of the master volume smooth ([692(0x2B4):SV Curve Mid]).	PRESETROM2 0xB4
	(B)	Set the master volume to −12dB ([[763(0x2FB):SV -12.0dB]).	PRESETROM2 0xFB

4.1.2-8 Output Setting

No.	Controls		Host Access
(18)	Follow step (A) and (B) to start generating sound.		
	(A)	Cancel the mute state of MDSP2, SDSP (0x10 MUTE: MDSPMUTEN=SDSPMUTEN=1).	10 0x03
	(B)	Cancel the mute of the master volume (SV.NMute[15:0]=0x4000).	WRITE 0x403B 0x4000

4.1.3 Effect ON/OFF

4.1.3-1 Surround

Perform the following step to activate the surround effect.

No.	Controls	Host Access
(1)	Enable the surround effect (S3D.ThruSel[15:0]=0x0000, S3D.S3DSel[15:0]= 0x4000).	WRITE 0x4136 0x0000 0x4000

Meanwhile, perform the following step to inactivate the surround effect.

No.	Controls	Host Access
(1)	Disable the surround effect (S3D.ThruSel[15:0]=0x4000, S3D.S3DSel[15:0]= 0x0000).	WRITE 0x4136 0x4000 0x0000

[Note]

- Set the S3D core coefficients and the gain coefficients by performing step (5)-(A) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.3-2 Band Extension

Perform the following step to activate the band extension effect.

No.	Controls	Host Access
(1)	Enable the band extension effect (HXT.ThruSel[15:0]=0x0000, HXT.HXTSel[15:0]=0x4000).	WRITE 0x4196 0x0000 0x4000

Meanwhile, perform the following step to inactivate the band extension effect.

No.	Controls	Host Access
(1)	Disable the band extension effect (HXT.ThruSel[15:0]=0x4000, HXT.HXTSel[15:0]=0x0000).	WRITE 0x4196 0x4000 0x0000

[Note]

- Set the HXT core coefficients and the gain coefficients by performing step (6)-(A) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.3-3 Acoustic Compensation

Perform the following step (1) and (2) to activate the acoustic compensation effect.

No.	Controls	Host Access
(1)	Select the AEQ core processing path output (AC.ThruSel[15:0]=0x0000, AC.ACSel[15:0]= 0x4000).	WRITE 0x43F7 0x0000 0x4000
(2)	Select the SDSP 10-band PEQ processing output (SV.BypassSel[15:0]=0x0000, SV.10bPEQSel [15:0]=0x4000).	WRITE 0x4042 0x0000 0x4000

Meanwhile, perform the following step (1) and (2) to inactivate the acoustic compensation effect.

No.	Controls	Host Access
(1)	Bypass the AEQ core processing (AC.ThruSel[15:0]=0x4000, AC.ACSel [15:0]=0x0000).	WRITE 0x43F7 0x4000 0x0000
(2)	Bypass the SDSP 10-band PEQ processing (SV.BypassSel[15:0]=0x4000, SV.10bPEQSel[15:0]= 0x0000).	WRITE 0x4042 0x4000 0x0000

[Note]

- Set the AEQ core coefficients and the gain coefficients by performing step (7)-(B) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously. And also, set SDSP 10-band PEQ coefficients by performing step (11) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.3-4 Loudness

Perform the following step to activate the loudness effect.

No.	Controls	Host Access
(1)	Enable the loudness enhancer effect (SV.LnSel[15:0]=0x4000, SV.LnThruSel[15:0]=0x0000).	WRITE 0x4050 0x4000 0x0000

Meanwhile, perform the following step to inactivate the loudness effect.

No.	Controls	Host Access
(1)	Disable the loudness enhancer effect (SV.LnSel[15:0]=0x0000, SV.LnThruSel[15:0]=0x4000).	WRITE 0x4050 0x0000 0x4000

[Note]

- Set the loudness coefficients by performing step (8)-(E) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.3-5 Output Power Limiter

Perform the following step to activate the output power limiter function.

No.	Controls	Host Access
(1)	Enale the output power limiter function (LMT.HGCThruSel[15:0]=LMT.LGCThruSel[15:0]= 0x0000, LMT.HGCSel[15:0]=LMT.LGCSel[15:0]=0x4000).	WRITE 0x4081 0x0000 0x4000 0x0000 0x4000

Meanwhile, perform the following step to inactivate the output power limiter function.

No.	Controls	Host Access
(1)	Disable the output power limiter function (LMT.HGCThruSel[15:0]=LMT.LGCThruSel[15:0]= 0x4000, LMT.HGCSel[15:0]=LMT.LGCSel[15:0]=0x0000).	WRITE 0x4081 0x4000 0x0000 0x4000 0x0000

[Note]

- Set the gain control coefficients by performing step (10)-(D) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.3-6 Soft clip

Perform the following step to activate the soft clip function.

No.	Controls	Host Access
(1)	Enale the soft clip function (LMT.SCThruSel[15:0]=0x0000, LMT.SCSel[15:0]=0x4000).	WRITE 0x408C 0x0000 0x4000

Meanwhile, perform the following step to inactivate the soft clip function.

No.	Controls	Host Access
(1)	Disable the soft clip function (LMT.SCThruSel[15:0]=0x4000, LMT.SCSel[15:0]=0x0000).	WRITE 0x408C 0x4000 0x0000

[Note]

- Set the gain control coefficients by performing step (10)-(E) of "4.1.1 DD-2SP Initializations" or "4.1.2 SPR-2 Initializations" previously.
- During the firmware operation, set coefficients via the runtime transfer.

4.1.4 Signal Detection

Perform the following step to activate the small signal detection.

No.	Controls	Host Access
(1)	Enable the small signal detection. In this example, if the signal less than -60dBFS is continuously input for more than 500ms (ILD.DetLev[15:0]=0x0020, ILD.DetTime[15:0]=0x5DC0, ILD.DetRst [15:0]= 0x0000), the detection is noticed (0x16 MIDAT 上 MIDAT[7:0]=0x01).	WRITE 0x400E 0x0020 0x5DC0 0x0000

Meanwhile, perform the following step to inactivate the small signal detection.

No.	Controls	Host Access
(1)	Disable the small signal detection (ILD.DetLev[15:0]=0x0000, ILD.DetTime[15:0]=0x0001, ILD.DetRst[15:0]=0x0000).	WRITE 0x400E 0x0000 0x0001 0x0000

[Note]

- During the firmware operation, set coefficients via the runtime transfer.

4.1.5 Use of FM Synthesizer

Perform the following step (1) to (6) while the firmware is operating.

No.	Controls	Host Access
(1)	Disable the sending of the FM sound playback end status bit through the interrupt request pin (IRQ_N pin) (0x1A FMST: STEN=0).	0x1A 0x00
(2)	Cancel the mute sate of the FM sound (0x10 MUTE: FMMUTEN=1).	DD-2SP 使用時:0x10 0x0F SPR-2 使用時: 0x10 0x07
(3)	When specifying the ROM block number of the FM sound to generate, the FM sound is played back . Specify [32(0x020):Power_On_01] in this example. And, the FM sound playback end status bit is automatically enabled (0x1A FMST: STEN=1).	PRESETROM0 0x20
(4)	Wait until the FM sound playback end status bit is output from IRQ_N pin (whose logic state changes from H to L).	-
(5)	Disable the sending of the FM sound playback end status bit through IRQ_N pin again (0x1A FMST: STEN=0).	0x1A 0x00
(6)	Set the mute state of FM sound (0x10 MUTE: FMMUTEN=0).	0x10 0x0B for DD-2SP 0x10 0x03 for SPR-2

[Note]

- Mix the audio signal with FM sound signal by performing step (8)-(B) of “4.1.1 DD-2SP Initializations” or “4.1.2 SPR-2 Initializations” previously.
- If the host controller does not detect the interrupt request signal via IRQ_N pin, step (1) needs not to be performed. And, substitute the following step (4’) for the above step (4).

No.	Controls	Host Access
(4’)	Wait until the FM sound is played back to the end（0x1A FMST: STFLG=0）.	-

- For details of the ROM block number, see “Appendix C Preset Pattern List” or “YDA174/YSS952 Application Manual”.

4.2 Runtime Transfer

This chapter describes two control examples of runtime transfers:

1. Writing firmware coefficients into CRAM from the host controller.
2. Reading of firmware coefficients on CRAM by the host controller.

For details of the example for writing firmware coefficients into CRAM from the ROM, see “4.3 Preset Pattern Setting”.

[Note]

- In the following tables, the microprocessor commands used for control is described in Host Access column. (WRITE and READ are commands and the code of each command is WRITE=READ=0x80.) See “YDA174 /YSS952 Application Manual” for the detail of commands.

4.2.1 Data Transfer from Host Controller to CRAM

No.	Controls	Host Access
(1)	Set runtime transfer control data as shown below: Here shows an example of the control data for writing EQ0, EQ1 filter coefficients of Smooth volume firmware. ・Write a transfer destination start address into RtStartAdr[9:0]. (Example: RtStartAdr[9:0]=0x044) ・Write the number of transfer data into RtCnt[3:0]. (Example: RtCnt[3:0]=0x9) ・Write transfer data into RtData[0–9][15:0] up to 10 words.	WRITE 0x0000 0x0044 0x0009 [10word×16bit]
(2)	Issue a write request (MDSPREQ[7:0]=0x02 at 0x13 MDSPREQ)	0x13 0x02
(3)	The data transfer will complete within 1 sample time and the write request is cleared. (MDSPREQ [7:0]=0x00 at 0x13 MDSPREQ)	-

[Note]

- When changing firmware coefficients in runtime transfer, discontinuous sound may occur because of significant signal level change etc.

4.2.2 Data Transfer from CRAM to Host Controller

No.	Controls	Host Access
(1)	Set runtime transfer control data as shown below: Here shows an example of the control data for reading EQ0, EQ1 filter coefficients of Smooth volume firmware. ・Write a transfer source start address into RtStartAdr[9:0]. (Example: RtStartAdr[9:0]=0x044) ・Write the number of transfer data into RtCnt[3:0]. (Example: RtCnt[3:0]=0x9)	WRITE 0x0000 0x0044 0x0009
(2)	Issue a read request (0x13 MDSPREQ: MDSPREQ[7:0]=0x03)	0x13 0x03
(3)	The data transfer will complete within 1 sample time and the read request is cleared (0x13 MDSPREQ: MDSPREQ [7:0]=0x00).	-
(4)	Read the transferred data from RtData[0–9][15:0] up to 10 words.	READ 0x0002 [10word×16bit]

4.3 Preset Pattern Setting

Execute the following step while keeping MDSP2 and SDSP operated.

No.	Controls	Host Access
(1)	Specifies a desired preset coefficient. [787(0x313):SV -24.0dB] is set in this example.	PRESETROM3 0x13

[Note]

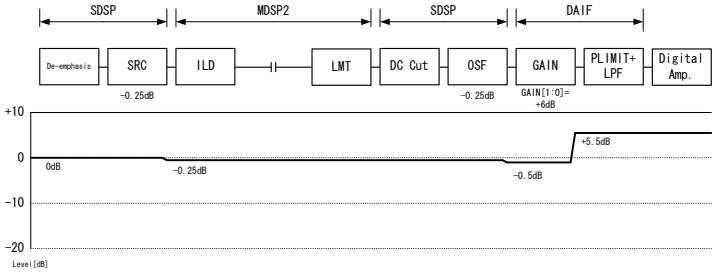
- The microprocessor commands used for control is described in Host Access column. (WRITE and PRESETROM3 is a command and the codes of each command are WRITE=0x80 and PRESETROM3=0x73.) See "YDA174 /YSS952 Application Manual" for the detail of commands.
- For coefficient set that can transfer firmware coefficients to an arbitrary CRAM address, execute the following step before the above step (1). Coefficient set, which can be transferred to arbitrary address, is the set with "N" at the Transfer Destination column in the tables ("3 Preset Pattern").

No.	Controls	Host Access
(0)	Writes a transfer destination start address into RtStartAdr[9:0]. An address specified with ILD.SDI0Sel[15:0] is written in this example.	WRITE 0x0000 0x000B

- As stated in the above (0), transfer destination start address should be specified not by on-chip RAM address but by CRAM relative address. For example, when specifying address of ILD.SDI0Sel[15:0] as a start address, write not 0x400B (on-chip RAM address) but 0x00B (CRAM's relative address).

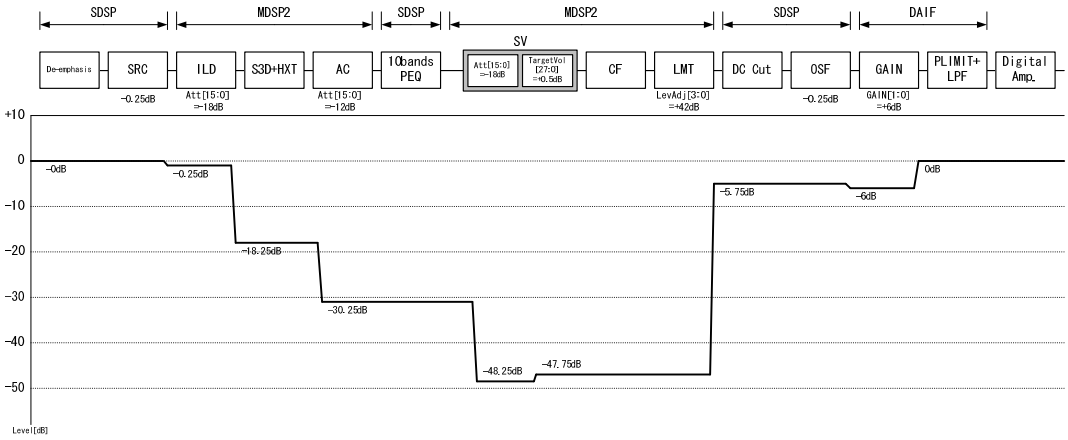
4.4 Output Gain Adjustment (DD-2SP only)

A full scale signal should be input to the digital amplifier in order for the amplifier to attain its maximum instantaneous output power (15W, PVDD=15V, R_L=8Ω). High harmonics distortions, which may be produced if saturations occurs in digital circuits, can be reduced by setting the output gain to +6dB (0x2F GAIN:GAIN[1:0]=01) in DAIF (interface with the digital amplifier) GAIN processing; however, as shown in the level diagram below, the output gain will be +5.5dB because the gain lowers in 0.25 dB steps with SRC and OSF processing in SDSP.



To account for the increase of gain with GAIN processing, a amount for headroom cancel (LMT.HiLevAdj[3:0]) should be set to a value subtracted by 1 bit from secured headroom. 0x7 is set in this example. And, to account for the decrease of gain with SRC and OSF processing, boost the master volume by +0.5 dB with Smooth volume firmware.

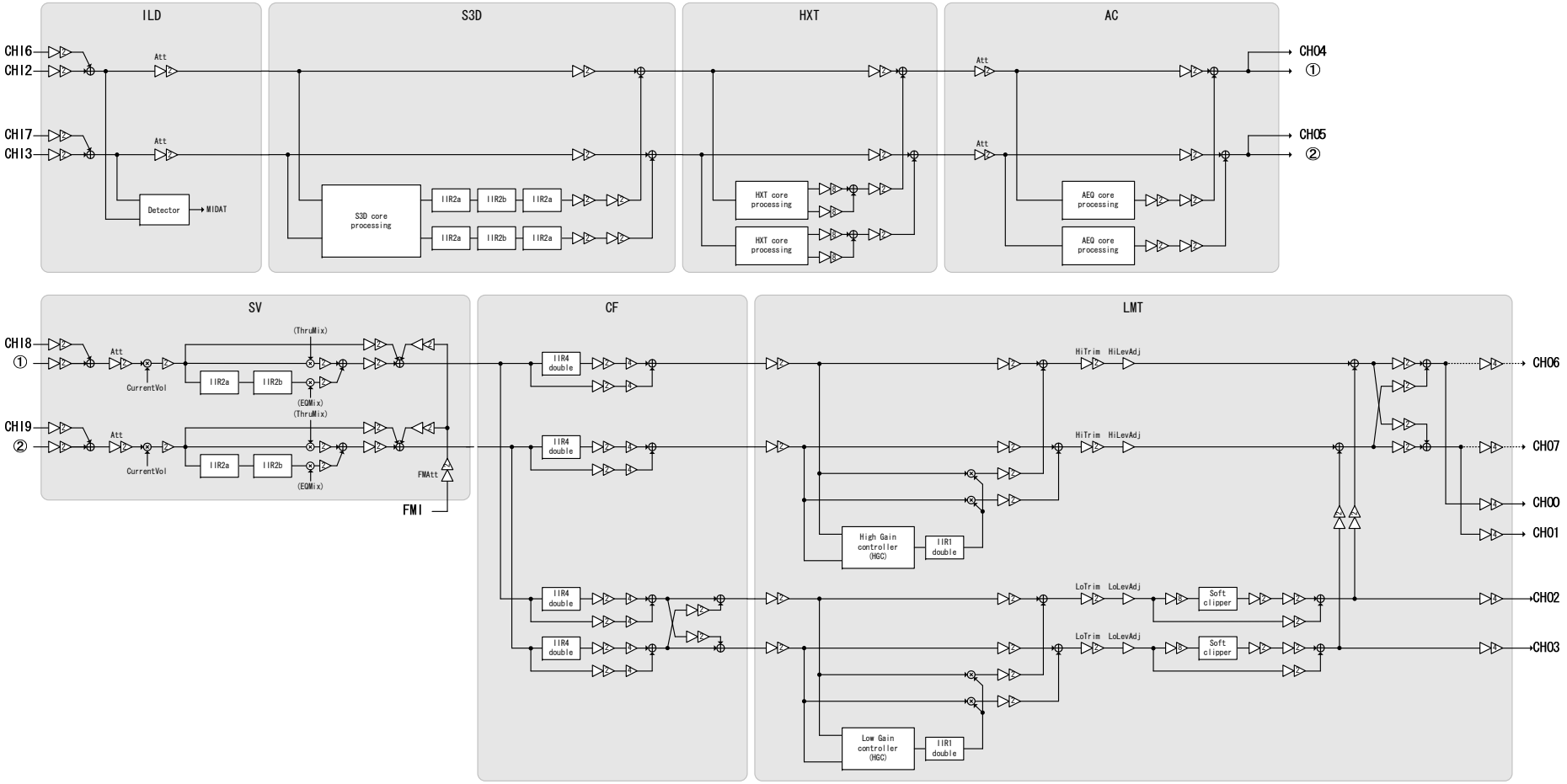
The figure below shows the level diagram with the above gain compensation applied. In this level diagram, 8-bit headroom is secured with the following bits: Att[15:0] in Input level detector firmware, Att[15:0] bit in Acoustic total-linear EQ core firmware, Att[15:0] bit in Smooth volume firmware (ILD.Att[15:0]=0x0800, AC.Att[15:0]=0x1000, SV.Att[15:0]=0x0800).



[Note]

- The output gain adjustment with OSF (SDSP) and GAIN (DAIF) processing is not applied to signals to be output to SDO0 and SDO1 paths.

Appendix A Overall Signal Flow Diagram



Appendix B Coefficient Data List

The below table shows the address map of firmware coefficients in this firmware:

[Note]

- The address with "(Reserved)" in Bit Name column is a reserved address. This address must not be written. An undefined value will be read.

On-chip RAM Address	Bit Name		Module Name	Remarks
0x4000	Top	Data0[15:0]	Top	
0x4001		Data1[15:0]		
0x4002		Data2[15:0]		
0x4003		Data3[15:0]		
0x4004		Data4[15:0]		
0x4005		Data5[15:0]		
0x4006	(Reserved)		-	
:				
0x400A	(Reserved)			
0x400B	SDI0Sel[15:0]		ILD	
0x400C	SDI1Sel[15:0]			
0x400D	Att[15:0]			
0x400E	DetLev[15:0]			
0x400F	DetTime[15:0]			
0x4010	DetRst[15:0]			
0x4011	(Reserved)		-	
:	:			
0x4033	(Reserved)			
0x4034	Att[15:0]		SV	
0x4035	FMAtt[15:0]			
0x4036	FMLMix[15:0]			
0x4037	FMRMix[15:0]			
0x4038	(Reserved)		-	
0x4039	(Reserved)			
0x403A	(Reserved)			
0x403B	NMute[15:0]		SV	
0x403C	CurrentVol[27:12]			
0x403D	CurrentVol[11:0]			
0x403E	TargetVol[27:12]			
0x403F	TargetVol[11:0]			
0x4040	Delta[27:12]			
0x4041	Delta[11:0]			
0x4042	ThruSel[15:0]			
0x4043	10bPEQSel[15:0]			
0x4044	EQ0	a0[15:0]		
0x4045		a1[15:0]		
0x4046		a2[15:0]		
0x4047		b1[15:0]		

On-chip RAM Address	Bit Name		Module Name	Remarks
0x4048		b2[15:0]		
0x4049	EQ1	a0[15:0]		
0x404A		a1[15:0]		
0x404B		a2[15:0]		
0x404C		b1[15:0]		
0x404D		b2[15:0]		
0x404E	LnRatio[15:0]			
0x404F	LnShift[15:0]			
0x4050	LnSel[15:0]			
0x4051	LnThruSel[15:0]			
0x4052	(Reserved)		-	
:	:			
0x4065	(Reserved)			
0x4066	HiLBal[15:0]		LMT	
0x4067	HiRBal[15:0]			
0x4068	LoLBal[15:0]			
0x4069	LoRBal[15:0]			
0x406A	HGC	GainShift[15:0]		
0x406B		CurveShift[15:0]		
0x406C		Ratio[15:0]		
0x406D		Limit[15:0]		
0x406E		Decay[15:0]		
0x406F		PreAttack[15:0]		
0x4070	HATK	a0[27:12]		
0x4071		a0[11:0]		
0x4072		a1[27:12]		
0x4073		a1[11:0]		
0x4074		b1[27:12]		
0x4075		b1[11:0]		
0x4076	LGC	GainShift[15:0]		
0x4077		CurveShift[15:0]		
0x4078		Ratio[15:0]		
0x4079		Limit[15:0]		
0x407A		Decay[15:0]		
0x407B	LATK	a0[27:12]		
0x407C		a0[11:0]		
0x407D		a1[27:12]		
0x407E		a1[11:0]		
0x407F		b1[27:12]		
0x4080		b1[11:0]		
0x4081	HGCThruSel[15:0]			
0x4082	HGCSel[15:0]			
0x4083	LGCThruSel[15:0]			
0x4084	LGCSel[15:0]			
0x4085	HiTrim[15:0]			
0x4086	LoTrim[15:0]			

On-chip RAM Address	Bit Name		Module Name	Remarks
0x4087	HiLevAdj[3:0]			
0x4088	LoLevAdj[3:0]			
0x4089	PreLev[15:0]			
0x408A	PostLev[15:0]			
0x408B	CompLev[15:0]			
0x408C	SCThruSel[15:0]			
0x408D	SCSel[15:0]			
0x408E	LoMix[15:0]			
0x408F	SMix[15:0]			
0x4090	XMix[15:0]			
0x4091	LAmpOut[15:0]			
0x4092	RAmpOut[15:0]			
0x4093	LSDO0Out[15:0]			
0x4094	RSDO0Out[15:0]			
0x4095	LSDO1Out[15:0]			
0x4096	RSDO1Out[15:0]			
0x4097	(Reserved)		-	
:	:			
0x409C	(Reserved)			
0x409D	S3DCore	Data0[15:0]	S3D	
0x409E		Data1[15:0]		
:		:		
0x4124		Data135[15:0]		
0x4125		Data136[15:0]		
0x4126	EQ0	a0[15:0]		
0x4127		a1[15:0]		
0x4128		a2[15:0]		
0x4129		b1[15:0]		
0x412A		b2[15:0]		
0x412B	EQ1	a0[15:0]		
0x412C		a1[15:0]		
0x412D		a2[15:0]		
0x412E		b1[15:0]		
0x412F		b2[15:0]		
0x4130	EQ2	a0[15:0]		
0x4131		a1[15:0]		
0x4132		a2[15:0]		
0x4133		b1[15:0]		
0x4134		b2[15:0]		
0x4135	S3DLev[15:0]			
0x4136	ThruSel[15:0]			
0x4137	S3DSel[15:0]			
0x4138	(Reserved)		-	
:	:			
0x4148	(Reserved)			

On-chip RAM Address	Bit Name		Module Name	Remarks
0x4149	HXTCore	Data0[15:0]	HXT	
0x414A		Data1[15:0]		
:		:		
0x4192		Data73[15:0]		
0x4193		Data74[15:0]		
0x4194	DryMix[15:0]			
0x4195	WetMix[15:0]			
0x4196	ThruSel[15:0]			
0x4197	HXTSel[15:0]			
0x4198	(Reserved)		-	
:	:			
0x41C2	(Reserved)			
0x41C3	HPF	a0[27:12]	CF	
0x41C4		a0[11:0]		
0x41C5		a1[27:12]		
0x41C6		a1[11:0]		
0x41C7		a2[27:12]		
0x41C8		a2[11:0]		
0x41C9		b1[27:12]		
0x41CA		b1[11:0]		
0x41CB		b2[27:12]		
0x41CC		b2[11:0]		
0x41CD		c0[27:12]		
0x41CE		c0[11:0]		
0x41CF		c1[27:12]		
0x41D0		c1[11:0]		
0x41D1		c2[27:12]		
0x41D2		c2[11:0]		
0x41D3		d1[27:12]		
0x41D4		d1[11:0]		
0x41D5		d2[27:12]		
0x41D6		d2[11:0]		
0x41D7	LPF	a0[27:12]		
0x41D8		a0[11:0]		
0x41D9		a1[27:12]		
0x41DA		a1[11:0]		
0x41DB		a2[27:12]		
0x41DC		a2[11:0]		
0x41DD		b1[27:12]		
0x41DE		b1[11:0]		
0x41DF		b2[27:12]		
0x41E0		b2[11:0]		
0x41E1		c0[27:12]		
0x41E2		c0[11:0]		
0x41E3		c1[27:12]		
0x41E4		c1[11:0]		

On-chip RAM Address	Bit Name		Module Name	Remarks
0x41E5		c2[27:12]		
0x41E6		c2[11:0]		
0x41E7		d1[27:12]		
0x41E8		d1[11:0]		
0x41E9		d2[27:12]		
0x41EA		d2[11:0]		
0x41EB	MonoMix[15:0]			
0x41EC	HPFSel[15:0]			
0x41ED	HThruSel[15:0]			
0x41EE	LPFSel[15:0]			
0x41EF	LThruSel[15:0]			
0x41F0	(Reserved)		-	
0x41F1	(Reserved)			
0x41F2	Att[15:0]		AC	
0x41F3	AEQCore	Data0[15:0]		
0x41F4		Data1[15:0]		
:		:		
0x43F3		Data512[15:0]		
0x43F4		Data513[15:0]		
0x43F5	LPostLev[15:0]			
0x43F6	RPostLev[15:0]			
0x43F7	ThruSel[15:0]			
0x43F8	ACSel[15:0]			
0x43F9	(Reserved)		-	
:	:			
0x43FE	(Reserved)			
0x43FF	FWMode[15:0]		Top	0x110E(fixed) is displayed.

Appendix C Preset Pattern List

The table below shows the list of preset patterns:

[Note]

- The preset pattern stored in the block number 0 is automatically executed when changing DD-2SP/SPR-2 operation mode from hardware reset mode to normal operation mode.
- FM contents are stored into the block numbers of 32 to 89. For details of FM contents, see "YDA174/YSS952 Application Manual".

On-chip ROM Block Number	Preset Pattern Name	
0x000(0)	-	
0x020(32)	FM contents	Power_On_01
0x021(33)		Power_Off_01
0x022(34)		Power_On_02
0x023(35)		Power_On_03
0x024(36)		Power_On_04
0x025(37)		Power_On_05
0x026(38)		Power_On_06
0x027(39)		Power_On_07
0x028(40)		Power_On_08
0x029(41)		Power_On_09
0x02A(42)		Power_On_10
0x02B(43)		Power_On_11
0x02C(44)		Power_On_12
0x02D(45)		Power_On_13
0x02E(46)		Power_On_14
0x02F(47)		Power_On_15
0x030(48)		Power_On_16
0x031(49)		Power_On_17
0x032(50)		Power_On_18
0x033(51)		Power_On_19
0x034(52)		Power_On_20
0x035(53)		Power_On_21
0x036(54)		Power_On_22
0x037(55)		Power_On_23
0x038(56)		Power_On_24
0x039(57)		Power_On_25
0x03A(58)		Power_On_26
0x03B(59)		Power_On_27
0x03C(60)		Power_On_28
0x03D(61)		Power_On_29
0x03E(62)		Power_On_30
0x03F(63)		Power_On_31
0x040(64)		Power_On_32
0x041(65)		Power_On_33
0x042(66)		Power_On_34
0x043(67)		Power_On_35

On-chip ROM Block Number	Preset Pattern Name	
0x044(68)		Power_On_36
0x045(69)		Power_On_37
0x046(70)		Power_On_38
0x047(71)		Power_On_39
0x048(72)		Operation_01
0x049(73)		Operation_02
0x04A(74)		Operation_03
0x04B(75)		Operation_04
0x04C(76)		Operation_05
0x04D(77)		Comical_01
0x04E(78)		Pafopafo_01
0x04F(79)		Chime_01
0x050(80)		Bicycle_01
0x051(81)		Telephone_01
0x052(82)		Announcement_01
0x053(83)		Announcement_02
0x054(84)		School_Bel_01
0x055(85)		Spring_01
0x056(86)		SL_01
0x057(87)		Cat_01
0x058(88)		Cuckoo_01
0x059(89)		Chime_02
0x0E3(227)	Level Zero	
0x0E4(228)	Level Low	
0x0E5(229)	Level Midlow	
0x0E6(230)	Level Mid	
0x0E7(231)	Level Midhigh	
0x0E8(232)	Level High	
0x24D(589)	ILD SDI0 Sel	
0x24E(590)	ILD SDI1 Sel	
0x2B2(690)	SV Immediate	
0x2B3(691)	SV Curve Fast	
0x2B4(692)	SV Curve Mid	
0x2B5(693)	SV Curve Slow	
0x2B6(694)	SV Ln DEQ0 Low	
0x2B7(695)	SV Ln DEQ0 High	
0x2B8(696)	SV Ln DEQ1 Low	

On-chip ROM Block Number	Preset Pattern Name
0x2B9(697)	SV Ln DEQ1 High
0x2BA(698)	SV Through
0x2BB(699)	SV Ln Through
0x2BC(700)	SV Ln Active
0x2BF(703)	SV +18.0dB
0x2C0(704)	SV +17.5dB
0x2C1(705)	SV +17.0dB
0x2C2(706)	SV +16.5dB
0x2C3(707)	SV +16.0dB
0x2C4(708)	SV +15.5dB
0x2C5(709)	SV +15.0dB
0x2C6(710)	SV +14.5dB
0x2C7(711)	SV +14.0dB
0x2C8(712)	SV +13.5dB
0x2C9(713)	SV +13.0dB
0x2CA(714)	SV +12.5dB
0x2CB(715)	SV +12.0dB
0x2CC(716)	SV +11.5dB
0x2CD(717)	SV +11.0dB
0x2CE(718)	SV +10.5dB
0x2CF(719)	SV +10.0dB
0x2D0(720)	SV +9.5dB
0x2D1(721)	SV +9.0dB
0x2D2(722)	SV +8.5dB
0x2D3(723)	SV +8.0dB
0x2D4(724)	SV +7.5dB
0x2D5(725)	SV +7.0dB
0x2D6(726)	SV +6.5dB
0x2D7(727)	SV +6.0dB
0x2D8(728)	SV +5.5dB
0x2D9(729)	SV +5.0dB
0x2DA(730)	SV +4.5dB
0x2DB(731)	SV +4.0dB
0x2DC(732)	SV +3.5dB
0x2DD(733)	SV +3.0dB
0x2DE(734)	SV +2.5dB
0x2DF(735)	SV +2.0dB
0x2E0(736)	SV +1.5dB
0x2E1(737)	SV +1.0dB
0x2E2(738)	SV +0.5dB
0x2E3(739)	SV 0.0dB
0x2E4(740)	SV −0.5dB
0x2E5(741)	SV −1.0dB
0x2E6(742)	SV −1.5dB
0x2E7(743)	SV −2.0dB
0x2E8(744)	SV −2.5dB

On-chip ROM Block Number	Preset Pattern Name
0x2E9(745)	SV −3.0dB
0x2EA(746)	SV −3.5dB
0x2EB(747)	SV −4.0dB
0x2EC(748)	SV −4.5dB
0x2ED(749)	SV −5.0dB
0x2EE(750)	SV −5.5dB
0x2EF(751)	SV −6.0dB
0x2F0(752)	SV −6.5dB
0x2F1(753)	SV −7.0dB
0x2F2(754)	SV −7.5dB
0x2F3(755)	SV −8.0dB
0x2F4(756)	SV −8.5dB
0x2F5(757)	SV −9.0dB
0x2F6(758)	SV −9.5dB
0x2F7(759)	SV −10.0dB
0x2F8(760)	SV −10.5dB
0x2F9(761)	SV −11.0dB
0x2FA(762)	SV −11.5dB
0x2FB(763)	SV −12.0dB
0x2FC(764)	SV −12.5dB
0x2FD(765)	SV −13.0dB
0x2FE(766)	SV −13.5dB
0x2FF(767)	SV −14.0dB
0x300(768)	SV −14.5dB
0x301(769)	SV −15.0dB
0x302(770)	SV −15.5dB
0x303(771)	SV −16.0dB
0x304(772)	SV −16.5dB
0x305(773)	SV −17.0dB
0x306(774)	SV −17.5dB
0x307(775)	SV −18.0dB
0x308(776)	SV −18.5dB
0x309(777)	SV −19.0dB
0x30A(778)	SV −19.5dB
0x30B(779)	SV −20.0dB
0x30C(780)	SV −20.5dB
0x30D(781)	SV −21.0dB
0x30E(782)	SV −21.5dB
0x30F(783)	SV −22.0dB
0x310(784)	SV −22.5dB
0x311(785)	SV −23.0dB
0x312(786)	SV −23.5dB
0x313(787)	SV −24.0dB
0x314(788)	SV −24.5dB
0x315(789)	SV −25.0dB
0x316(790)	SV −25.5dB

On-chip ROM Block Number	Preset Pattern Name
0x317(791)	SV −26.0dB
0x318(792)	SV −26.5dB
0x319(793)	SV −27.0dB
0x31A(794)	SV −27.5dB
0x31B(795)	SV −28.0dB
0x31C(796)	SV −28.5dB
0x31D(797)	SV −29.0dB
0x31E(798)	SV −29.5dB
0x31F(799)	SV −30.0dB
0x320(800)	SV −30.5dB
0x321(801)	SV −31.0dB
0x322(802)	SV −31.5dB
0x323(803)	SV −32.0dB
0x324(804)	SV −32.5dB
0x325(805)	SV −33.0dB
0x326(806)	SV −33.5dB
0x327(807)	SV −34.0dB
0x328(808)	SV −34.5dB
0x329(809)	SV −35.0dB
0x32A(810)	SV −35.5dB
0x32B(811)	SV −36.0dB
0x32C(812)	SV −36.5dB
0x32D(813)	SV −37.0dB
0x32E(814)	SV −37.5dB
0x32F(815)	SV −38.0dB
0x330(816)	SV −38.5dB
0x331(817)	SV −39.0dB
0x332(818)	SV −39.5dB
0x333(819)	SV −40.0dB
0x334(820)	SV −40.5dB
0x335(821)	SV −41.0dB
0x336(822)	SV −41.5dB
0x337(823)	SV −42.0dB
0x338(824)	SV −42.5dB
0x339(825)	SV −43.0dB
0x33A(826)	SV −43.5dB
0x33B(827)	SV −44.0dB
0x33C(828)	SV −44.5dB
0x33D(829)	SV −45.0dB
0x33E(830)	SV −45.5dB
0x33F(831)	SV −46.0dB
0x340(832)	SV −46.5dB
0x341(833)	SV −47.0dB
0x342(834)	SV −47.5dB
0x343(835)	SV −48.0dB
0x344(836)	SV −48.5dB

On-chip ROM Block Number	Preset Pattern Name
0x345(837)	SV −49.0dB
0x346(838)	SV −49.5dB
0x347(839)	SV −50.0dB
0x348(840)	SV −50.5dB
0x349(841)	SV −51.0dB
0x34A(842)	SV −51.5dB
0x34B(843)	SV −52.0dB
0x34C(844)	SV −52.5dB
0x34D(845)	SV −53.0dB
0x34E(846)	SV −53.5dB
0x34F(847)	SV −54.0dB
0x350(848)	SV −54.5dB
0x351(849)	SV −55.0dB
0x352(850)	SV −55.5dB
0x353(851)	SV −56.0dB
0x354(852)	SV −56.5dB
0x355(853)	SV −57.0dB
0x356(854)	SV −57.5dB
0x357(855)	SV −58.0dB
0x358(856)	SV −58.5dB
0x359(857)	SV −59.0dB
0x35A(858)	SV −59.5dB
0x35B(859)	SV −60.0dB
0x35C(860)	SV −60.5dB
0x35D(861)	SV −61.0dB
0x35E(862)	SV −61.5dB
0x35F(863)	SV −62.0dB
0x360(864)	SV −62.5dB
0x361(865)	SV −63.0dB
0x362(866)	SV −63.5dB
0x363(867)	SV −64.0dB
0x364(868)	SV −64.5dB
0x365(869)	SV −65.0dB
0x366(870)	SV −65.5dB
0x367(871)	SV −66.0dB
0x368(872)	SV −66.5dB
0x369(873)	SV −67.0dB
0x36A(874)	SV −67.5dB
0x36B(875)	SV −68.0dB
0x36C(876)	SV −68.5dB
0x36D(877)	SV −69.0dB
0x36E(878)	SV −69.5dB
0x36F(879)	SV −70.0dB
0x370(880)	SV −70.5dB
0x371(881)	SV −71.0dB
0x372(882)	SV −71.5dB

On-chip ROM Block Number	Preset Pattern Name
0x373(883)	SV −72.0dB
0x374(884)	SV −72.5dB
0x375(885)	SV −73.0dB
0x376(886)	SV −73.5dB
0x377(887)	SV −74.0dB
0x378(888)	SV −74.5dB
0x379(889)	SV −75.0dB
0x37A(890)	SV −75.5dB
0x37B(891)	SV −76.0dB
0x37C(892)	SV −76.5dB
0x37D(893)	SV −77.0dB
0x37E(894)	SV −77.5dB
0x37F(895)	SV −78.0dB
0x380(896)	SV −78.5dB
0x381(897)	SV −79.0dB
0x382(898)	SV −79.5dB
0x383(899)	SV −80.0dB
0x384(900)	SV −80.5dB
0x385(901)	SV −81.0dB
0x386(902)	SV −81.5dB
0x387(903)	SV −82.0dB
0x388(904)	SV −82.5dB
0x389(905)	SV −83.0dB
0x38A(906)	SV −83.5dB
0x38B(907)	SV −84.0dB
0x38C(908)	SV −84.5dB
0x38D(909)	SV −85.0dB
0x38E(910)	SV −85.5dB
0x38F(911)	SV −86.0dB
0x390(912)	SV −86.5dB
0x391(913)	SV −87.0dB
0x392(914)	SV −87.5dB
0x393(915)	SV −88.0dB
0x394(916)	SV −88.5dB
0x395(917)	SV −89.0dB
0x396(918)	SV −89.5dB

On-chip ROM Block Number	Preset Pattern Name
0x397(919)	SV −90.0dB
0x398(920)	SV −90.5dB
0x399(921)	SV −91.0dB
0x39A(922)	SV −91.5dB
0x39B(923)	SV −92.0dB
0x39C(924)	SV −92.5dB
0x39D(925)	SV −93.0dB
0x39E(926)	SV −93.5dB
0x39F(927)	SV −94.0dB
0x3A0(928)	SV −94.5dB
0x3A1(929)	SV −95.0dB
0x3A2(930)	SV −95.5dB
0x3A3(931)	SV −96.0dB
0x3A4(932)	SV −96.5dB
0x3A5(933)	SV −97.0dB
0x3A6(934)	SV −97.5dB
0x3A7(935)	SV −98.0dB
0x3A8(936)	SV −98.5dB
0x3A9(937)	SV −99.0dB
0x3AA(938)	SV −99.5dB
0x3AB(939)	SV −100.0dB
0x3AC(940)	SV −102.0dB
0x3AD(941)	SV −104.0dB
0x3AE(942)	SV −106.0dB
0x3AF(943)	SV −108.0dB
0x3B0(944)	SV −110.0dB
0x3B1(945)	SV −112.0dB
0x3B2(946)	SV −114.0dB
0x3B3(947)	SV −116.0dB
0x3B4(948)	SV −118.0dB
0x3B5(949)	SV −120.0dB
0x3B6(950)	SV −122.0dB
0x3B7(951)	SV −124.0dB
0x3B8(952)	SV −126.0dB
0x3B9(953)	SV −128.0dB