

**SNC7600 Datasheet**

Audio Codec SoC

# Version 1.1bHistory

|  |  |  |
| --- | --- | --- |
| **Version** | **Release Date** | **Description** |
| V1.0b | 06/08/2020 | Initial creation |
| V1.1b | 05/15/2021 | Fix the errors for descriptions of peripherals |
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1. **Introduction:**

SNC7600 is designed basing on Soundec filed noise reduction patents to provide best-in-class clear and enjoyable listening experience to end-users.

SNC7600 is a standalone single-chip with a high-quality audio Codec, a high-performance DSP, and a low power management unit. The high-level integration permits to achieve low application BOM cost.

It incorporates a HiFi3 DSP core, a stereo 24-bit/192Ksps ADC and DAC with 106 dB and 100dB dynamic range respectively; a headphone driver which doesn’t require coupling capacitors to reduce BOM cost; also, 4 DMIC inputs to extend its application scope. A full power management unit provides all power supply necessary in the chip with low power consumption. On-chip PLL generate all necessary clocks with different frequencies for function blocks.

It provides a rich set of interfaces such as I2S(Standard I2S, Left Justified, Right Justified), as well as I2C, UART, etc.

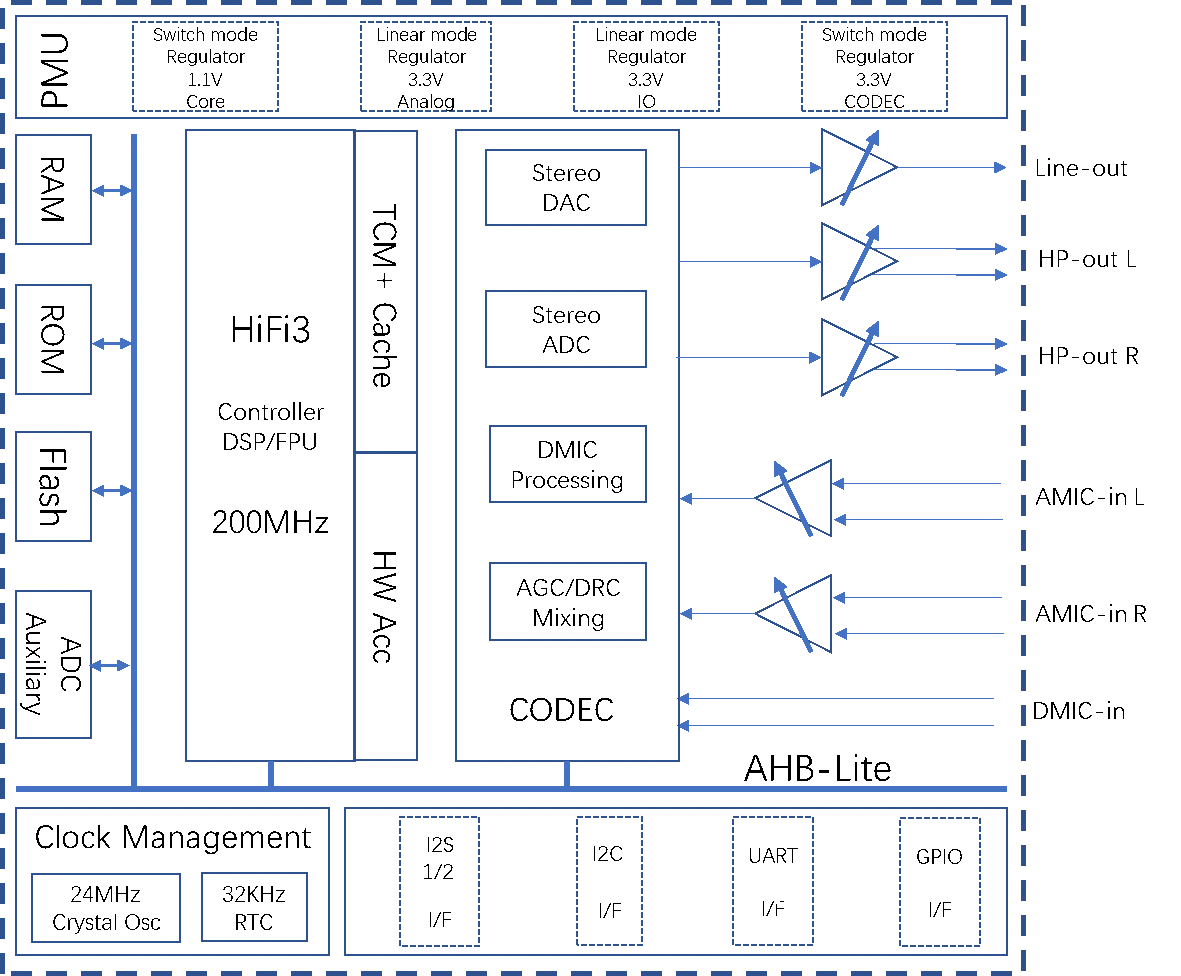
There is another dedicated circuit “front-end audio” which works together with this Codec SoC to form a complete and unique audio solution around Soundec patents. This front-end audio circuit is defined in a separate document.

1. **Key features:**

* Core:
  + HiFi3 core as the controller and audio DSP, up to 200MHz
  + MAC, vector FPU, SIMD
  + Proprietary hardware accelerators
  + 512KB zero-wait RAM
  + 48KB zero-wait cache RAM
  + On-chip 1MB NOR Flash memory
* Codec:
  + Stereo 24-bit ADC and DAC, with 106 dB and 110dB dynamic range respectively
  + Support sampling rate: 8k, 16k, 32k, 44.1k, 48k, 88.2k, 96k, 176.4k, 192k
  + 4 DMIC inputs
  + 2 AMIC inputs
  + Low power voice detection
  + Wind noise suppression
  + Audio local DSP: AGC, DRC, mixing
* Noise cancellation:
  + Patented noise cancellation for both near-end and far-end
  + Active echo cancellation
  + Active noise cancellation
* The on-chip ultra-low power management unit
  + One unique power supply from 3.3V to 5.5V
  + DC-DC regulators and LDOs for all on-chip supply voltages
  + POR-BOR, overvoltage protection
  + Always-on domain for ultra-low-power sleep mode
* Crystal oscillator reference clock plus PLL
  + Crystal oscillator @24MHz
  + PLL provides all necessary clocks to meet SoC proper operation
* Interface:
  + Two I2S, support ADC and DAC with the different sampling rate
  + one I2C interfaces for system setting
  + One UART for firmware update and system setting
  + 16 GPIO multiplexing with other interfaces
* Auxiliary ADC for button detection, battery monitor, other analog sensors

1. **Functional applications:**
   * Wireless headset with ANC, AEC, and ENC
   * Audio conference device
   * AIoT device with smart voice processing
   * Beamforming voice command product
2. **System block diagram:**

This figure shows SNC7600 system block diagram.



With on-chip 24-bits/192Ksps digital and analog interface, microphone preamplifiers, and a cap-less headphone amplifier, SNC7600 is a truly single-chip solution for applications that demand high audio quality and low power consumption.

SNC7600 integrates a Cadence HiFi3 core up to 200MHz for system control and digital signal processing, and a high-quality 24-bits/192Ksps Codec with stereo input and stereo output, 2 AMIC inputs, 4 DMIC inputs. It provides up to 512KB zero-wait RAM and a size configurable Flash memory(1MB by default). The on-chip power management unit provides all power supply to meet the on-chip requirements with one power input. There is one always-on domain to achieve ultra-low power consumption target. The peripheral complement includes two I2S, one I2C, one UART, GPIOs. The auxiliary ADC can be used for button recognition, analog sensor monitoring, etc.

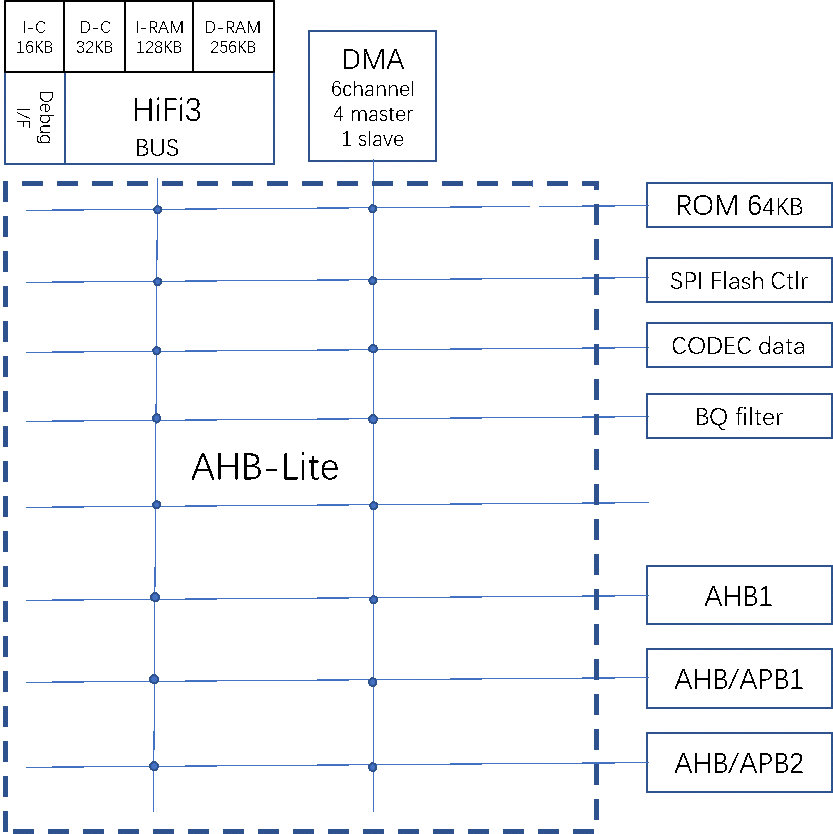
SNC7600 provides the digital processing power needed to maximize the features and performance of headsets and other audio products, including acoustic echo canceling, noise reduction, equalization, automatic gain control (AGC), and volume control.

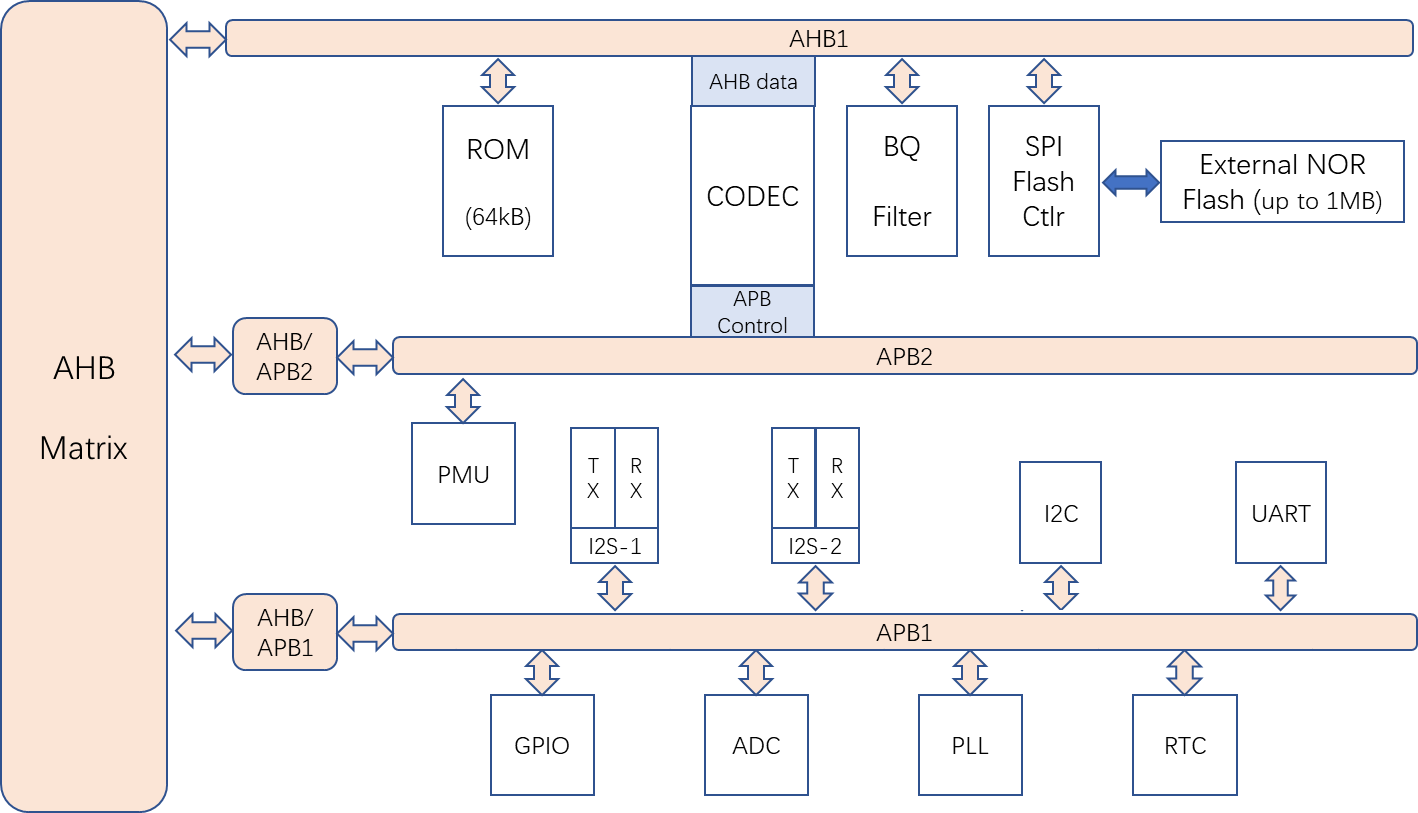
1. **Absolute maximum ratings:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
| Power | AVDPWR | -0.3 | 5.5 | V |
| AVDD | -0.3 | 3.63 | V |
| VDD\_IP33 | -0.3 | 3.63 | V |
| VDD\_IO33 | -0.3 | 3.63 | V |
| VDD\_OPM | -0.3 | 3.63 | V |
| Ambient Temperature | Ta | -20 | +80 | °C |
| ESD | HBM | -2000 | +2000 | V |
| CMD | -500 | +500 | V |

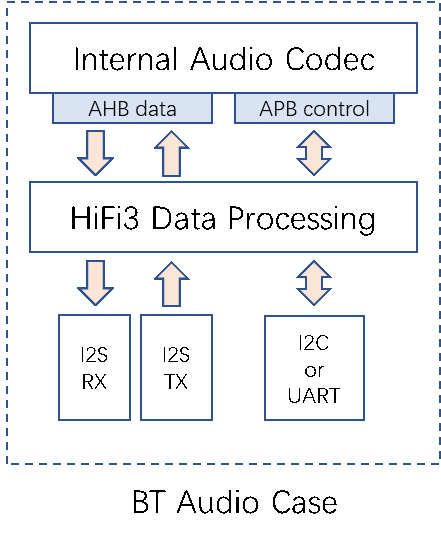
1. **System bus structure:**

The following figure shows the multi-layer bus matrix, where HiFi3, DMA, and ROM, SPI Flash controller, Codec data, BQ filter, and peripherals are slaves. I-RAM and D-RAM are TCM type SRAM with 1 cycle operation. 64KB ROM is used for system boot. The Hardware BQ filter is connected on the AHB bus.

Here are AHB and AHP peripherals:

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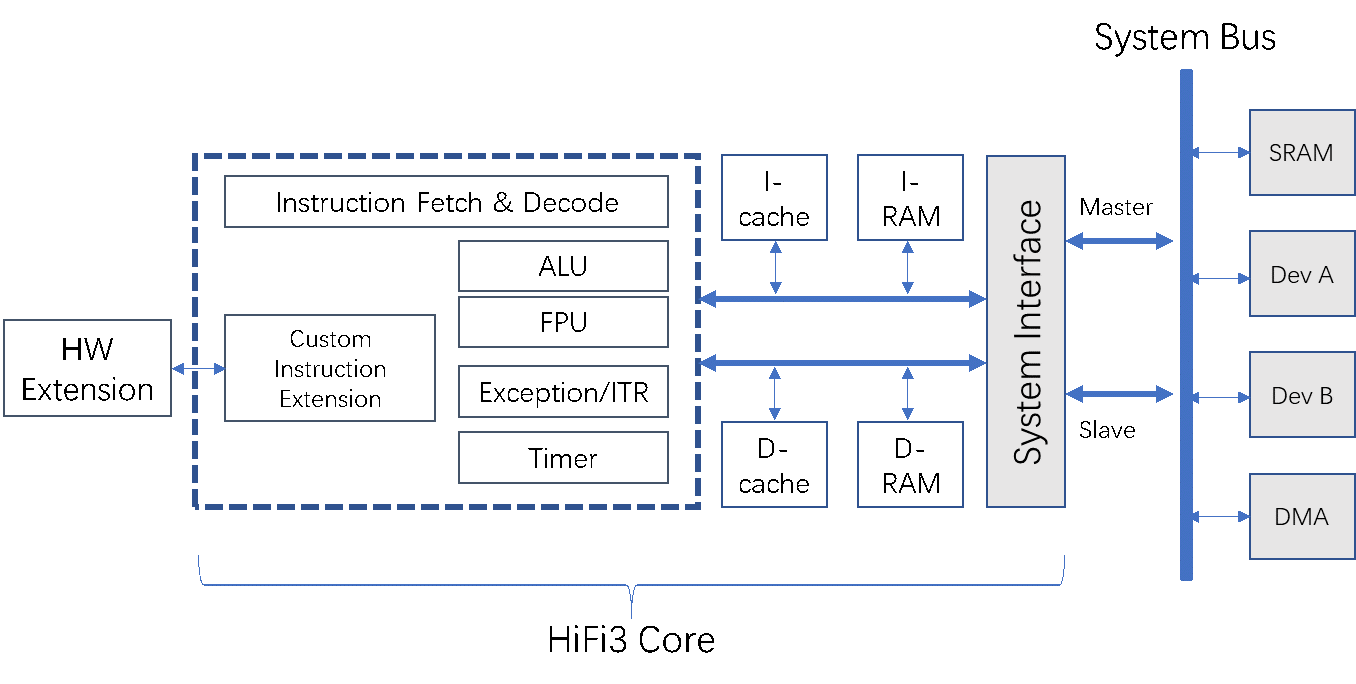
1. **Data processing flow:**



The above figure shows the data flow with I2S as the interface to HiFi3 core. This is the application case for Bluetooth headset, or the case of beamforming voice command product.

1. **HiFi3 core specification:**

A powerful Cadence H3Fi3 core is used for system control and audio digital signal processing. The following figure shows the HiFi3 architecture.



The following table shows the key features and configuration of the HiFi3 core:

|  |  |  |
| --- | --- | --- |
| Item | Specification | Comment |
| Core | Cadence HiFi3  32 bit instruction | As system controller and audio signal processing |
| Processor Clock | Up to 200 MHz |  |
| MAC | MAC |  |
| FPU | Vector FPU, half-precision |  |
| SIMD | Full type of operation |  |
| MIPS | 600 MIPS max | 3 slots in HiFi3 |
| I-RAM | 256KB | Local zero-wait RAM for instruction |
| D-RAM | 256KB | Local zero-wait RAM for data |
| I-Cache | 16 KB | 4 cache way, 64 Byte cache line |
| D-Cache | 32 KB | 4 cache way, 64 Byte cache line |
| Bus protocol | AHB-lite | 32-bit data width |
| Timer | 3 timers |  |

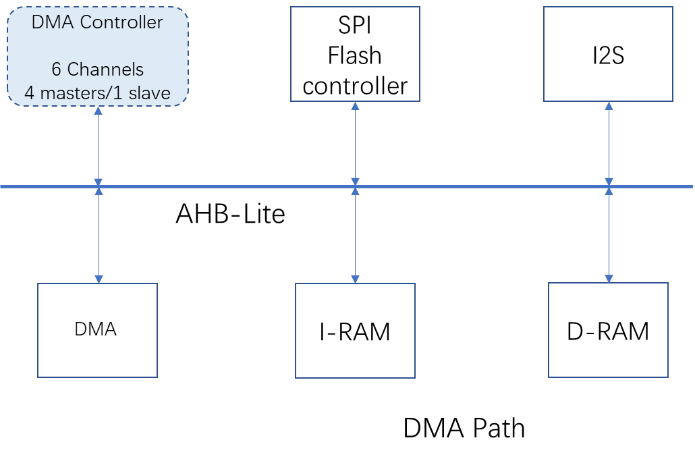
1. **Memory mapping:**

Memory usage over 4GB space:

|  |  |  |  |
| --- | --- | --- | --- |
| **Address range** | **General Use** | **Address range details and description** | |
| 0x0000 0000 to  0x6FFF FFFF | Not used | 0x0000 0000 - 0x6FFF FFFF | Not used |
| 0x7000 0000 to  0x7FFF FFFF | APB peripherals | 0x7000 0000 - 0x7FFF FFFF | APB1, APB2, AHB |
| 0x8000 0000 to  0x8FFF FFFF | Not used | 0x8000 0000 - 0x8FFF FFFF | Not used |
| 0x9000 0000 to  0x9FFF FFFF | ROM | 0x9000 0000 - 0x9001 FFFF | 64KB |
| dRAM | 0x9FF4 0000 - 0x9FF7 FFFF | 256KB |
| iRAM | 0x9FFC 0000 - 0x9FFF FFFF | 256KB |
| 0xA000 0000 to  0xAFFF FFFF | Flash memory | 0xA000 0000 - 0xA00F FFFF | External Flash memory, 1024 kB |
| Not used | 0xA010 0000 - 0xAFFF FFFF | Not used |
| 0xB000 0000 to  0xFFFF FFFF | Not used | 0x2000 0000 - 0x6FFF FFFF | Not used |

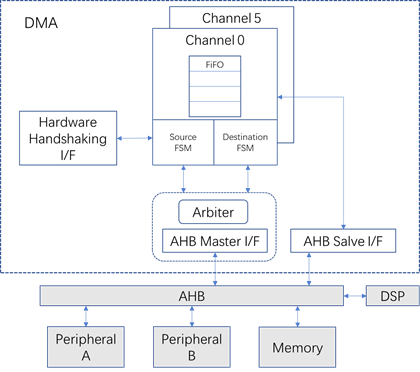
1. **DMA description:**

There is one DMA master controller connected to the AHB bus. Data can be transferred between RAM, Flash controller, and I2S through the DMA controller. The following figure shows the DMA function implementation.



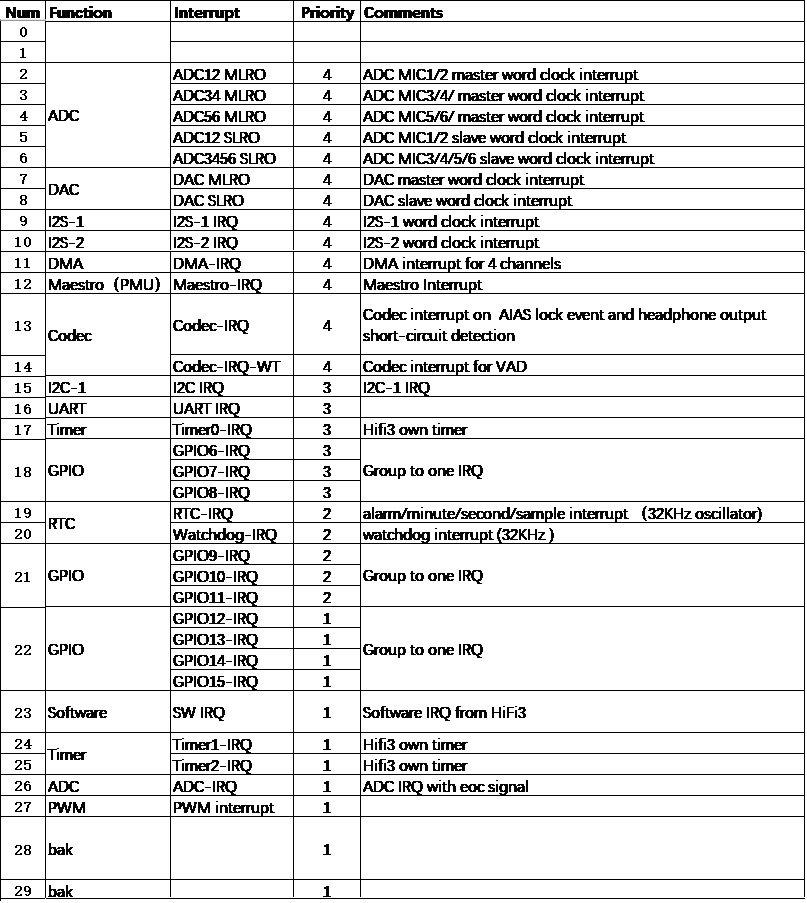
DMA is an AHB-Central DMA Controller core that transfers data from a source peripheral to a destination peripheral over one or more AHB bus, which consists of:

* DMA hardware request interface
* Up to six channels ..
* FIFO per channel for source and destination
* Arbiter
* AHB master interface
* AHB slave interface

The following figure shows the DMA block diagram.

1. **Interrupt description:**

HiFi3 supports 32 interrupts. There are 32 interrupts defined in the SoC, that are listed in the following table with priority, where higher-level number means higher priority.

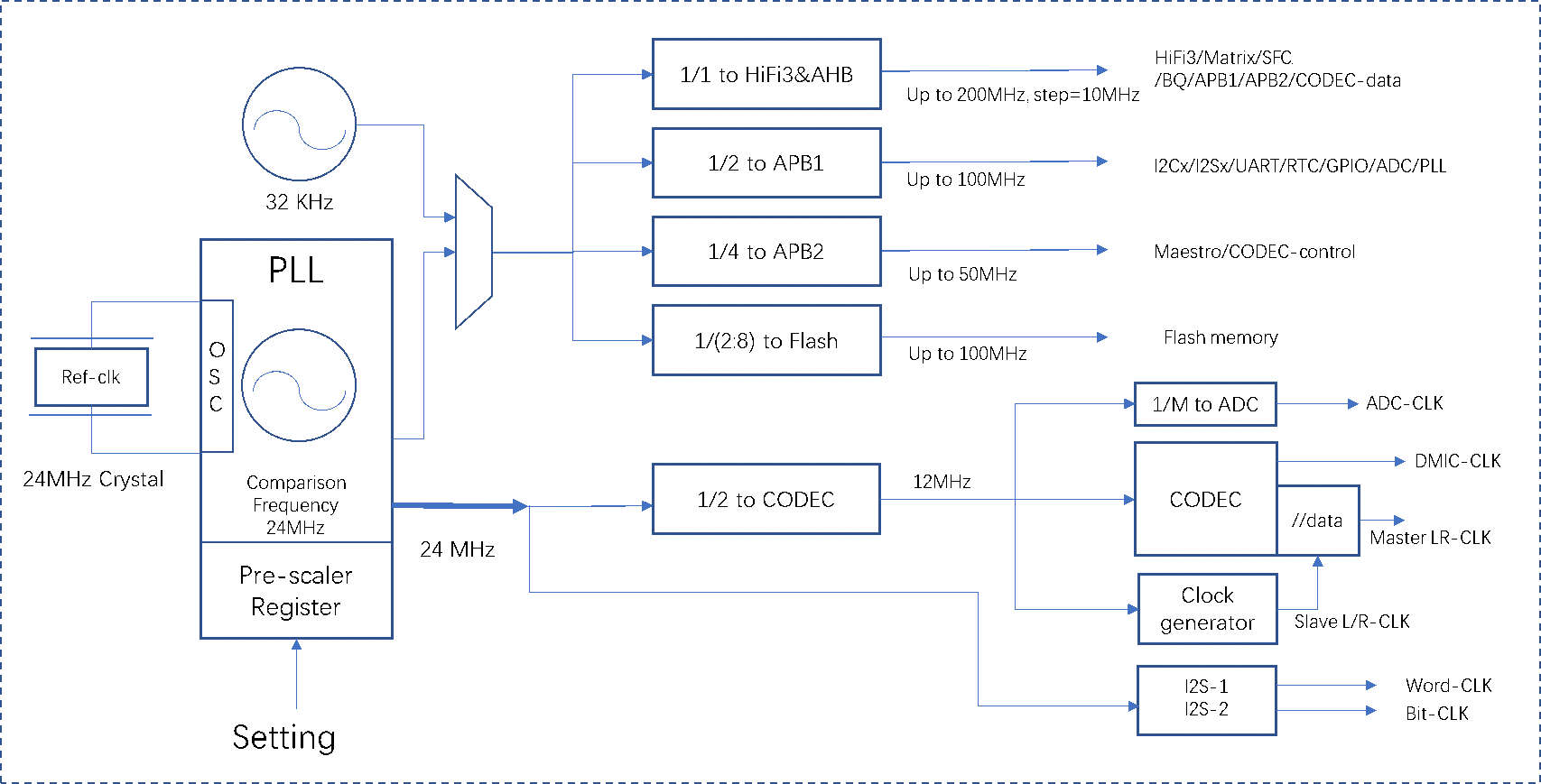


1. **Clock network description:**

The clock generation module includes PLL to provide clocks to HiFi3 core, Codec. and I2S, SPI, and other interfaces.

There are two reference oscillators. One is an on-chip 32kHz RC oscillator using during power-up and in low power mode. 24MHz crystal oscillator is used to provide reference clocks in active mode.

Codec master clock is 12MHz, the system clock can be up to 200MHz. SPI interface maximum clock is at 108MHz.

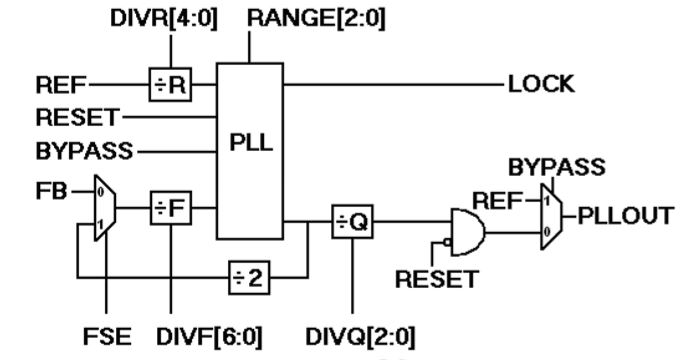


Clock request for each function block:

|  |  |  |  |
| --- | --- | --- | --- |
| **Clock** | **Active mode (max MHz)** | **Sleep mode (MHz)** | **Duty-cycle** |
| CPU/AHB | 200 | 0 | 45%-55% |
| APB1 | 50 | 0 | 45%-55% |
| APB2 | 100 | 0 |  |
| Flash | 108 | 0 | 45%-55% |
| Codec | 12 | 0 | 45%-55% |
| I2S | 24 | 0 | 45%-55% |
| PLL ref clk | 24 | 0 | 45%-55% |

1. **PLL description**

The following figure shows the PLL architecture where the reference clock is 24MHz.



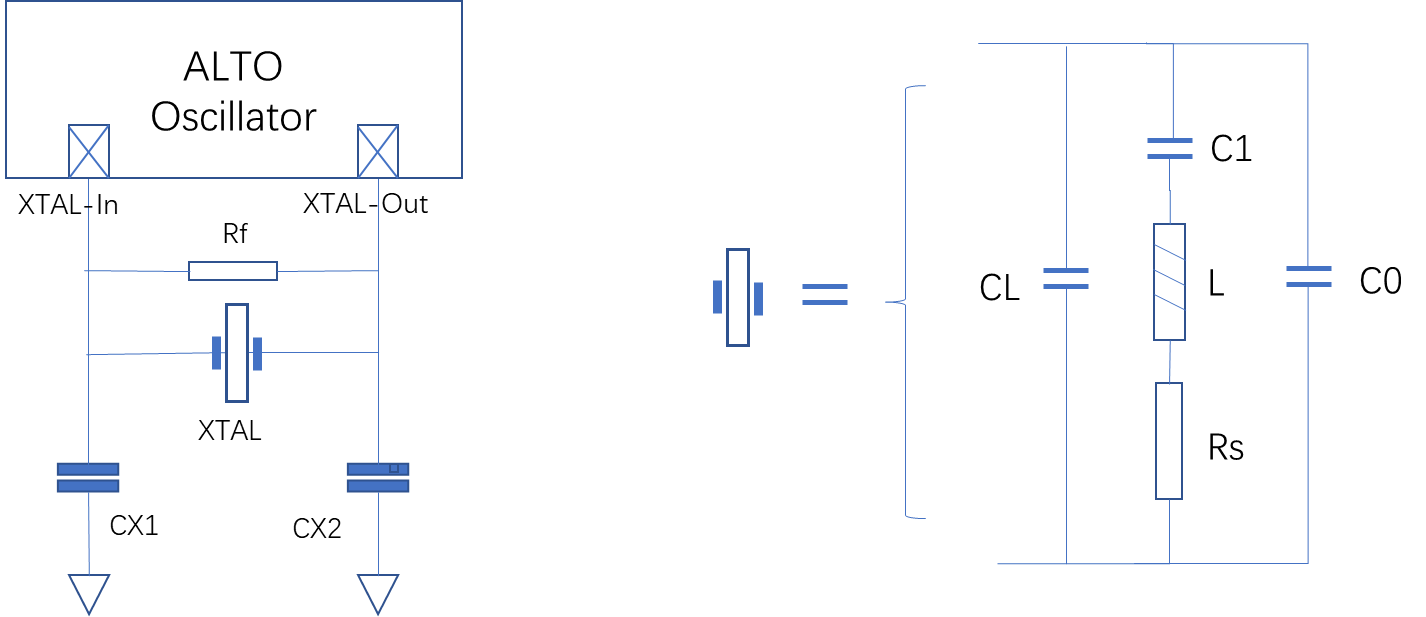
This table shows the signals for PLL operation:

|  |  |  |
| --- | --- | --- |
| **Signal** | **Usage** | **Limitation** |
| DIVR[4:0] | Reference Divider Value  (binary value + 1 : 00000 = ÷1) | Both REF and post-divide REF must be within the specified range |
| DIVF[6:0] | Feedback Divider Value  (binary value + 1 : 0000000 = ÷1) | VCO must be within the specified range |
| DIVQ[2:0] | Output Divider Value (2^ binary value)  001 = ÷2 100 = ÷16  010 = ÷4 101 = ÷32  011 = ÷8 110 = ÷64 |  |
| FSE | Chooses between internal and external input paths:  0 = FB pin input  1 = internal feedback |  |
| RANGE [2:0] | PLL Filter Range  000=BYPASS 100=26-42MHz 001=Reserved 101=42-68MHz  010=10-16MHz 110=68-110MHz 011=16-26MHz 111=110-200MH | This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance, or optimize with post-silicon characterization. |

This table shows the key parameters of PLL:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Description** | **Symbol** | **Min** | **Typ** | **Max** | **Units** |
| Input Frequency | Fref |  | 24 |  | MHz |
| VCO Frequency | Fvco | 1000 |  | 2000 | MHz |
| Output Frequency | Fout | 20 |  | 1000 | MHz |
| Output Duty Cycle | t-do | 45 |  | 55 | % |
| Maximum Lock Time | t-lock |  |  | 50 | µs |
| Reset Time | t-reset | 1 |  |  | µs |
| Maximum Long Term Jitter | LTJ | ±1% Divided-Ref Period | | | |
| Maximum Cycle to Cycle Jitte | CCJ | ±1% Output Period | | | |
| Total Power (unloaded) | IDD |  | 2 |  | mA |

1. **Crystal oscillator description:**



The above figure shows the crystal oscillator circuit and the crystal equivalent circuit. Only the crystal (XTAL) and the capacitances CX1 and CX2 need to be connected externally on XTAL-In and XTAL-Out. The oscillator has also a bypass mode where an external clock can be applied directly to the XTAL-In pin.

For the best results, it’s very critical to select a matching crystal for the on-chip oscillator. The load capacitance CL, series resistance Rs, and drive level DL are important parameters to consider while choosing the crystal. Rf is the feedback resistor important for the crystal to start oscillation. After selecting the proper crystal, the external load capacitor CX1 and CX2 values can be generally determined by the following expression:

CX1=CX2= CL – (Cpad + Cparasitic)

Where:

CL：Crystal load capacitance per terminal

Cpad: Pad capacitance of the XTAL-In and XTAL-Out pins

Cparasitic: Parasitic or stray capacitance of the external circuit.

This table shows the electrical characteristics of the crystal oscillator:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Description** | **Symbol** | **Min** | **Typ** | **Max** | **Units** |
| Frequency range (crystal mode) | Fref |  | 24 |  | MHz |
| Frequency range (bypass mode) | Fref |  | 24 |  | MHz |
| Frequency accuracy |  | -20 |  | +20 | ppm |
| Cycle-to-cycle Jitter | CCJ | -10 |  | +10 | ps |
| Output Duty Cycle | t-do | 40 | 50 | 60 | % |
| Equivalent Series Resistance |  |  |  | 40 | Ω |
| CL |  |  | 8 |  | pF |
| Rf |  |  | 1 |  | MΩ |
| Total Power (unloaded) | IDD |  | TBD |  | mA |

1. **Codec description:**

CODEC includes the following function blocks:

One stereo Analog to Digital Converter (ADC) and additional analog circuitry:

* Two single-ended or differential analog inputs with boost gain, which can be used either for line-in or mic-in application in cap-less conﬁguration.
  + The two-stage gain for record path: an analog boost gain from -2 dB to +24 dB with 2 dB step and a digitally programmable gain from -64 to +63 dB with 1 dB step.
* 4 mono or 2 stereo digital microphone interfaces with programmable DMIC clock frequency.

One stereo Digital to Analog Converter (DAC) and additional analog circuitry:

* One stereo differential cap-less headphone and line output.
* One dedicated mono differential line output

Built-in power regulation:

* One low noise linear voltage regulator to supply part of the analog circuits.
* Two microphone biasing outputs for driving up to two microphones.

Signal processing function:

* An Automatic Gain/Level Control (AGC) enables a self-adaptive recording of the sound level during recording.
* A Wind Noise ﬁlter (WNF), a programmable high pass ﬁlter feature enabling to reduce wind noise during recording in a windy environment or an open window vehicle.
* A digital WhisperTriggerTM for digital microphones which wake-up the chip when voice activity is detected.
* An Audio Interface Adaptive Synchronizer (AIAS) system enables to synchronize automatically the input data if the mean sample frequency is close to a standardized value (up to 3% difference).

Its main features include:

* Operating conditions
  + Main clock: 12MHz or 13MHz
  + Single 3.3 V (2.97 V to 3.63 V) analog power supply
  + Ambienttemperature range from -25°C to 80°C
* One stereo 24-bit/192Ksps ADC and One stereo 24-bit/192Ksps DAC
* Low BOM capacitor-less input and output
* 4 digital microphone interfaces with programmable DMIC clock frequency and support of low power mode
* Serial and parallel audio interface for digital audio data
* 24 to 16-bit signed linear PCM format, support sampling rate of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192kHz
* Embedded low noise linear regulator for high resilience to power supply noise
* Low power operating mode on the ADC path
* Reduction of audible glitches systems:
  + Soft mute mode
  + Zero-crossing gain change
* Automatic Gain/Level Control (AGC) with SNR optimizer feature
* Programmable Wind Noise Filter (WNF)
* WhisperTriggerTM, voice activity detection for digital microphone
* Slave mode interface on DAC with AIAS automatic data rate synchronization
* Slave mode interface on ADC with AIAS automatic data rate synchronization

1. **Codec characteristics:**
   1. **Frequencies:**

Sampling frequency and main clock frequency:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Description** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Fs | Sampling frequency in normal mode | 8 |  | 192 | kHz |
| Fs | Sampling frequency in low power consumption mode (ADC only) | 8 |  | 16 | kHz |
| Fmclk | Main clock frequency |  | 12 or 13 |  | MHz |
| Dmclk | Main clock duty cycle | 0.45 | 0.50 | 0.55 | - |

The relation between MCLK, DMIC\_CLK frequencies, and available Fs:

|  |  |  |  |
| --- | --- | --- | --- |
| **Clock division ratio (DMIC\_RATE)** | **DMIC-CLK: frequency (Fdmic≠clk) for Fmclk=12Mhz** | **DMIC-CLK: frequency (Fdmic≠clk) for Fmclk=13Mhz** | **Available Fs (kHz)** |
| 16 | 750 kHz | 812.5 kHz | 8, 11.025, 12, 16 |
| 12 | 1 MHz | 1.08 MHz | 8, 11.025, 12, 16 |
| 5 | 2.4 MHz | 2.6 MHz | 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192 |
| 4 | 3.0 MHz | 3.25 MHz | 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192 |

* 1. **Analog microphone/line input to ADC path:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Condition: - 40°C to +100°C, AVDD=3.3Vm DVDD=1.1V. Input sine wave with a frequency of 1 kHz, measurement bandwidth 20 Hz - Fs/2 for Fs < 48 kHz, measurement bandwidth 20 Hz - 20 kHz for Fs = 48 kHz to 192 kHz, normal mode, capacitor-less input conﬁguration, unless otherwise speciﬁed. | | | | | |
| **Parameter** | **Test condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Input level | Full Scale, Gain GID\* = 0 dB, boost gain GIM\* = 0 dB |  | 2.12 |  | Vpp |
| Full Scale, Gain GID\* = 0 dB, boost gain GIM\* = 20 dB |  | 0.212 |  | Vpp |
| THD+N | 1 kHz sine wave @ Full Scale -3 dB and gain GID\* = 0 dB, boost gain GIM\* = 0 dB, normal mode and low power mode |  | 88 |  | dB |
| Dynamic Range | A-weighted, 1 kHz sine wave, normal mode |  | 106.5 |  | dB |
| A-weighted, 1 kHz sine wave, low power mode |  | 103.5 |  | dB |
| SNR | A-weighted, 1 kHz sine wave, with activation of the SNR optimizer feature |  | 106 |  | dB |
| A-weighted, 1 kHz sine wave, gain GID\* = 0 dB, boost gain GIM\* = 0 dB, normal mode |  | 94.5 |  | dB |
| A-weighted, 1 kHz sine wave, gain GID\* = 0 dB, boost gain GIM\* = 0 dB, low power mode |  | 90.5 |  | dB |
| PSRR | 100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GID\* = 0 dB, boost gain GIM\* = 0 dB |  | 90 |  | dB |
| Input referred noise | A-weighted, 1 kHz sine wave @ Full Scale and gain GID\* = 0 dB, boost gain GIM\* = 20 dB, normal mode |  | 3.6 |  | uVrms |
| A-weighted, 1 kHz sine wave @ Full Scale and gain GID\* = 0 dB, boost gain GIM\* = 20 dB, low power mode |  | 5.0 |  | uVrms |
| Channel separation | 1 kHz sine wave @ Full Scale on one channel, no signal on the other channel and gain GID\* = 0 dB, boost gain GIM\* = 0 dB |  | 108 |  | dB |
| Inter-channel phase mismatch | 1 kHz sine wave @ Full Scale on two channels and gain GID\* = 0 dB, boost gain GIM\* = 0 dB, input bypass capacitor inter-channel mismatch = 10% max, master mode |  |  | 0.1 | ° |
| Gain range | Boost gain GIM\* when activated | -2 |  | +24 | dB |
| Digital gain GID\* | -64 |  | +63 | dB |
| Gain step | GIM\* @1kHz |  | 2 |  | dB |
| GID\* @1kHz |  | 1 |  | dB |
| Gain accuracy | GIM\* @1kHz | -1 |  | +1 | dB |
| GID\* @1kHz | -0.5 |  | +0.5 | dB |
| Input impedance (differential conﬁguration) | Boost gain GIM\* = 20 dB Includes 10 pF for ESD, bonding and package pins capacitances |  | 20 |  | pF |
| Input impedance (single-ended conﬁguration) | Boost gain GIM\* = 20 dB Includes 10 pF for ESD, bonding and package pins capacitances |  | 20 |  | pF |
| Polarity | AIP\*-AIN\* to DIL/R |  | +1 |  |  |

* 1. **DAC to headphone output path:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Condition: - 40°C to +100°C, AVDD=3.3Vm DVDD=1.1V. Input sinewave with a frequency of 1kHz, measurement bandwidth 20Hz-20kHz, unless otherwise speciﬁed. | | | | | |
| **Parameter** | **Test condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Output level | Full Scale, gain GOL/R = +6 dB, GODL/R = 0 dB, 10 kOhms load |  | 5.6 |  | Vpp |
| Full Scale, gain GOL/R = +6 dB, GODL/R = 0 dB, 200 Ohms load |  | 5.6 |  | Vpp |
| Full Scale, gain GOL/R = +6 dB, GODL/R = 0 dB, 32 Ohms load |  |  | 3.96 | Vpp |
| Output power | 200 Ohms load |  | 19.6 |  | mW |
| 32 Ohms load |  |  | 61.3 | mW |
| SNR | A-weighted, 1 kHz sine wave @ Full Scale, gain GOL/R = +6 dB, GODL/R = 0 dB, 10 kOhms load |  | 101 |  | dB |
| Dynamic Range | A-weighted, 1 kHz sine wave @ Full Scale, gain GOL/R = [-10 +6] dB, GODL/R = 0 dB, 10 kOhms load |  | 110 |  | dB |
| Idle Noise | A-weighted with no signal, gain GOL/R=-10dB, GODL/R = 0 dB, 10k Ohms load |  | -104.9 |  | dBV |
| THD+N | 1 kHz sine wave @ Full Scale -1 dB, gain GOL/R = +6 dB, GODL/R = 0 dB, 10 kOhms load |  | 87 |  | dB |
| 1 kHz sine wave @ Full Scale -1 dB, gain GOL/R = +6 dB, GODL/R = 0 dB, 200 Ohms load |  | 85 |  | dB |
| 1 kHz sine wave @ Full Scale -1 dB, gain GOL/R = -3 dB, GODL/R = 0 dB, 32 Ohms load |  | 79 |  | dB |
| PSRR | 100 mVpp 1 kHz is applied to AVD, input data is 0 and gain GOL/R = 0 dB, GODL/R = 0 dB, 10 kOhms load capacitor inter-channel mismatch = 10% max, master mode |  | 90 |  | dB |
| 100 mVpp 1kHz is applied to VDDAO, input data is 0 and gain GOL/R = 0 dB, GODL/R = 0 dB, 10 kOhms load |  | 70 |  | dB |
| Analog gain | Gain GOL/R | -19 |  | +12 | dB |
| Digital gain | Gain GODL/R | -31 |  | +32 | dB |
| Gain step | GOL/R, GODL/R @1 kHz |  | 1 |  | dB |
| Gain accuracy | GOL/R, GODL/R @1 kHz | -0.5 |  | +0.5 | dB |
| Pop-up Noise | Active <-> Inactive, 10 kOhms load |  | -60 |  | dBV |
| Active <-> Inactive, 16 Ohms load |  | -60 |  | dBV |
| Output load resistance (Rl) |  | 32 |  |  | ohms |
| Output load capacitance (Cp) |  |  |  | 200 | pF |

* 1. **DAC to line output path**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Condition: - 40°C to +100°C, AVDD=3.3Vm DVDD=1.1V. Input sinewave with a frequency of 1kHz, measurement bandwidth 20Hz-20kHz, unless otherwise speciﬁed. | | | | | |
| **Parameter** | **Test condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Output level | Full Scale and gain GODL/R = 0 dB | 2.3 | 2.55 | 2.8 | Vpp |
| SNR | A-weighted,1kHz sinewave @ Full Scale and gain GODL/R = 0 dB |  | 95 |  | dB |
| Dynamic Range | A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GODL/R = 0 dB |  | 95 |  | dB |
| THD+N | 1 kHz sine wave @ Full Scale -1 dB and gain GODL/R = 0 dB |  | 85 |  | dB |
| PSRR | 100 mVpp 1 kHz sine wave is applied to AVD and VDDAO, input data is 0 and gain GODL/R = 0 dB |  | 90 |  | dB |
| Output load resistance (Rl) |  | 100K |  |  | ohms |
| Output bypass capacitance (Cp) |  |  | 1 |  | uF |
| Output load capacitance (Cp) |  |  |  | 100 | pF |

* 1. **Digital microphone interface to decimating ﬁlter output path**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Condition: Input sine wave with a frequency of 1 kHz, MCLK = 12 MHz or 13 MHz, DMIC\_CLK = Fmclk/4, measurement bandwidth 20 Hz - Fs/2 for Fs = 8 to 32 kHz, measurement bandwidth 20 Hz - 20 kHz for Fs = 44.1 kHz to 192 kHz, unless otherwise speciﬁed. | | | | | |
| **Parameter** | **Test condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Input level | Full Scale max value, Gain GID\* = 0 dB |  | 85.6 |  | % |
| Full Scale min value, Gain GID\* = 0 dB |  | 14.4 |  | % |
| SNR | A-weighted,1kHz sinewave @Full Scale and gain GIDL, GIDR = 0 dB |  | 100 |  | dB |
| Dynamic Range | A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GID\* = 0 dB |  | 100 |  | dB |
| THD+N | 1kHz sinewave @Full Scale-1dB and gain GIDL, GIDR = 0 dB |  | 90 |  | dB |
| Digital gain | Gain GID\* when activated | -64 |  | 63 | dB |
| Gain step | GID\* @1 kHz |  | 1 |  | dB |
| Gain accuracy | GID\* @1 kHz | -0.25 | 1 | +0.25 | dB |

* 1. **Voice detection on digital microphone interface**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Test condition | Min. | Typ. | Max. | Unit |
| Detection Latency | Detection results based on MIWOK≠CTM r1.0, Far-Field conﬁguration, Power Level Sensitivity set to 5 dB, within 60% truncation of the ﬁrst phoneme |  | 25.7 |  | ms |
| VDV (Voice Detected as Voice) |  | 93.5 |  | % |
| NDV (Noise Detected as Voice) |  | 7 |  | % |
| VTE (Voice Trigger Efficiency) |  | 93.25 |  | % |
| Detection Latency | Detection results based on MIWOK≠CTM r1.0, Far-Field conﬁguration, Power Level Sensitivity set to 5 dB, within 60% truncation of the ﬁrst phoneme |  | 25.7 |  | ms |
| VDV (Voice Detected as Voice) |  | 98.5 |  | % |
| NDV (Noise Detected as Voice) |  | 7 |  | % |
| VTE (Voice Trigger Efficiency) |  | 95.75 |  | % |
| VDV (Voice Detected as Voice) | Detection results based on MIWOK≠CTM r1.0, Far-Field conﬁguration, Power Level Sensitivity set to 5 dB, within the word length |  | 100 |  | % |
| Minimum Absolute Detection Threshold |  |  |  | -80 | dBFS |
| Power Level Sensitivity |  | 0 |  | 31 | dB |
| Power Level Sensitivity |  |  | 1 |  | dB |

1. **I2S specification:**

There are three I2S interfaces, which are specified in the following table.

|  |  |  |  |
| --- | --- | --- | --- |
| Item | Unit | Specification | Comment |
| Interface number |  | 2 I2S interface, with word clock, bit clock, data-in, data-out |  |
| Word clock | kHz | Up to 192 | 8, 16, 32, 44.1, 48, 88.2, 96, 176.4, 192 |
| Data width | bits | 16/20/24 |  |
| Format |  | Standard, left-justified, right-justified |  |

I2S pin are GPIO reuse pins, GPIO mapping is described in the following table, where CLK is the bit clock, WS is the word clock, SDI is the input data, SDO is the output data.

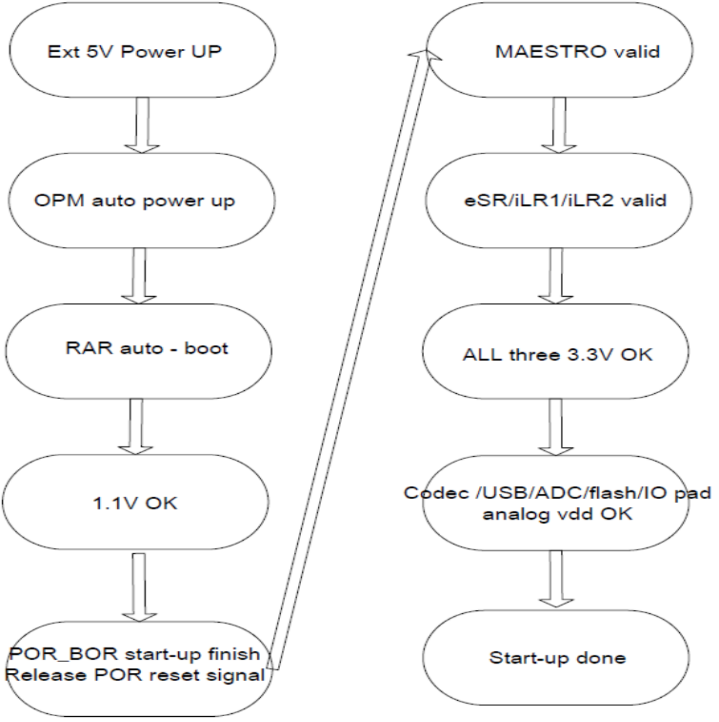
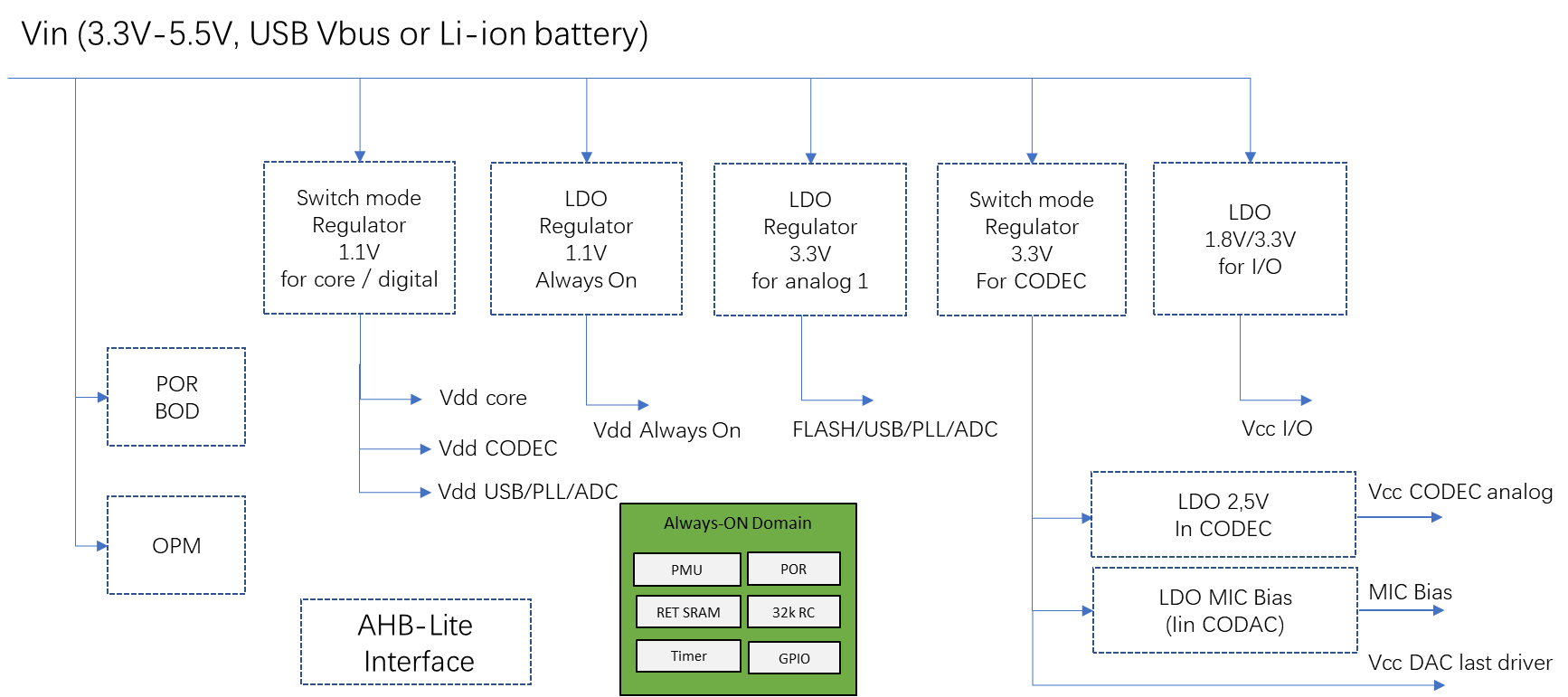
|  |  |  |  |
| --- | --- | --- | --- |
| I2S-1 | | I2S-2 | |
| I2S1\_clk | GPIO0 | I2S2\_clk | GPIO12 |
| I2S1\_ws | GPIO1 | I2S2\_ws | GPIO13 |
| I2S1\_sdi | GPIO2 | I2S2\_sdi | GPIO14 |
| I2S1\_sdo | GPIO3 | I2S2\_sdo | GPIO15 |

1. **PMU specification:**

One single power supply comes either from the host device VBUS either from Li-ion battery. The on-chip power management unit (PMU) provides all necessary voltage to run all functional blocks with low power consumption.

MIC bias for external microphones. 2.5V LDO for audio analog is included in Codec module. PMU includes also function for power-on-reset (POR) and brown-out-detect (BOD), also OVP/OCP/ULP protection. PMU should be programmable via APB bus to work in active mode, sleep mode, and power-down mode.

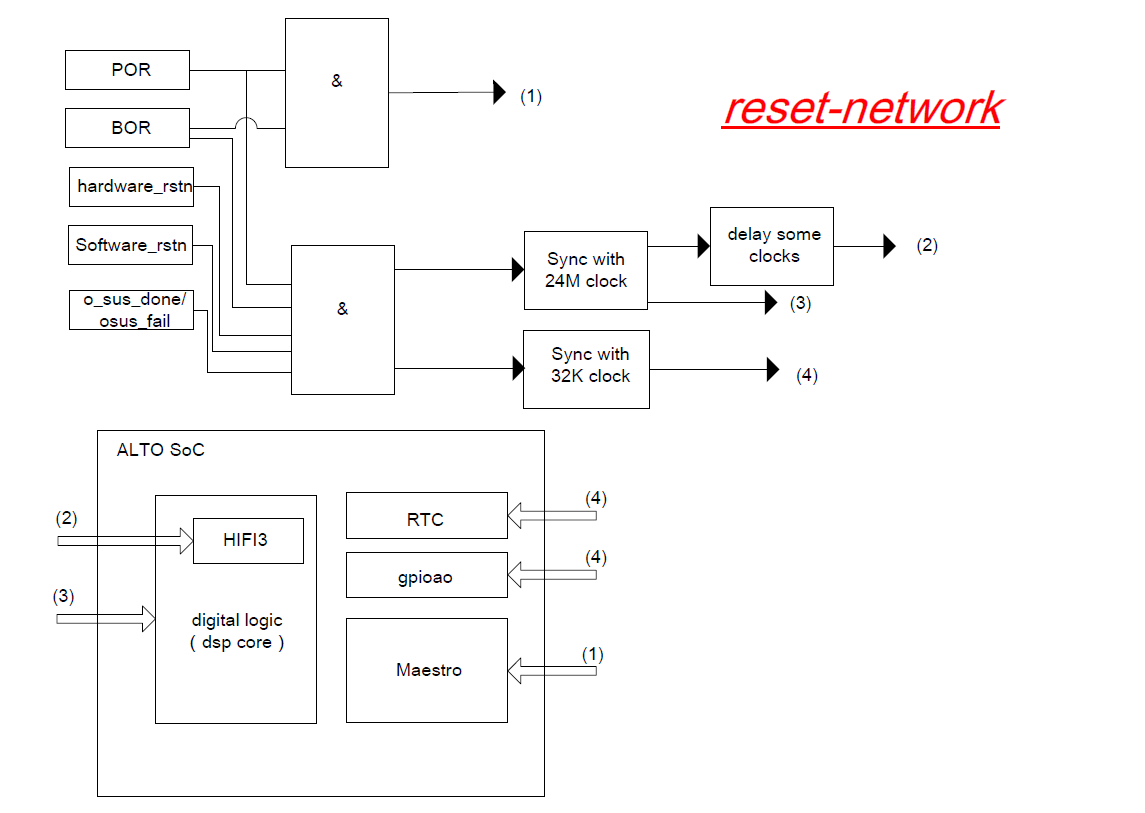
This figure shows the power tree architecture, where:

* Single power input from 3.3V to 5.5V
* One DC-DC regulator for Core and digital: 1.1V
* One Always-on ultra-low-power LDO for sleep-mode: 1.1V
* One DC-DC regulator for Codec analog part: 3.3V
* One LDO generate 3.3V power for other analog parts
* One LDO generate 3.3V power for digital IO
* Two Mic-bias for microphone biasing: 2.5V

The startup sequence is described in the left figure, where POR gives the general reset signal, and Maestro sets all regulators into the right states.

1. **Reset network:**

The following figure shows the reset network, where 4 reset signals reset different function blocks. Reset 1 is only generated by POR and BOR, the other 3 reset signals can be from POR/BOR, hardware reset and software reset, also from o\_sus\_done and o\_sus\_fail.



1. **I2C/UART:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Item | Quantity | Unit | Specification | Comment |
| UART | 1 | bps | Up to 3M | TX and RX |
| I2C | 1 | kbps | Up to 400 |  |

1. **Auxiliary ADC:**

This is a 12-bit SAR ADC, which can be used for headset button detection, battery monitor, or other analog sensor input measurement.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameters** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution |  | 12 |  | Bits |
| ENOB |  | 11 |  | Bits |
| Sampling rate |  | 5.0 |  | Msps |
| Channel |  | TBD |  |  |
| AVDD-aux-ADC |  | 3.3 |  | V |
| DVDD-aux-ADC |  | 1.1 |  | V |
| Input voltage range | 0 |  | 3.3 | V |
| INL accuracy | -2 |  | +2 | LSB |
| DNL accuracy | -1 |  | +1 | LSB |
| Offset | -2 |  | +2 | LSB |
| Gain error | -1 |  | 1 | % |
| Hardware conversion time |  | 1.0 |  | us |

1. **Pinout Name List:**

Pin name list with description and ball position:

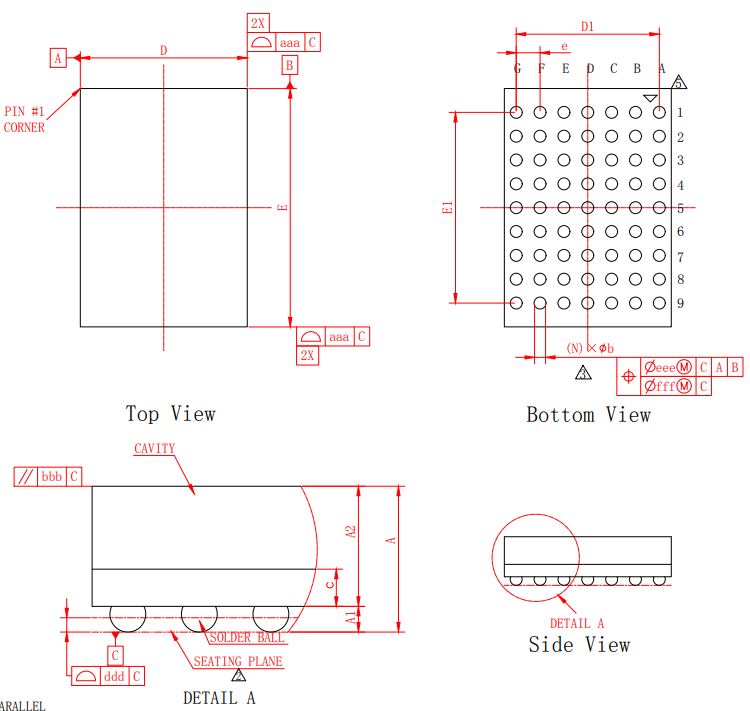
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Function | Pin name | 63 Ball BGA | Type | | Description | |
| Xtal Oscillator | XI | D1 | Analog | | 24MHz crystal port | |
| XO | C1 | Analog | | 24MHz crystal port | |
| PMU | VDD\_IP33 | D3 | Analog | | 3.3V for analog block | |
| VDD\_IO33 | E3 | Analog | | 3.3V for IO | |
| CODEC\_VDD | F8 | Analog | | 3.3V for Codec | |
| AVDPWR\_RAR | G3 | Analog | | External power supply | |
| AVDPWR\_ESR | G6 | Analog | | External power supply | |
| OPM\_VOUT | G7 | Analog | | Protection LDO output | |
| VDD\_CORE11 | F2,F7 | Analog | | 1.1V for digital core | |
| ESR\_LX | G4 | Analog | | DCDC2 switch pin | |
| VSENSE\_ESR | G5 | Analog | | DCDC2 sense pin | |
| RAR\_LX | G2 | Analog | | DCDC1 switch pin | |
| VSENSE-RAR | G1 | Analog | | DCDC1 sense pin | |
| NC | F6 | Analog | |  | |
| VREG | D7 | Analog | | Audio supply | |
| VCAP | D9 | Analog | | Audio biasing decap | |
| GPIO0 | B3 | I/O | | I2S1\_clk | |
| GPIO1 | B4 | I/O | | I2s1\_ws | |
| GPIO2 | A4 | I/O | | I2s1\_sdi | |
| GPIO3 | B5 | I/O | | I2s1\_sdo | |
| GPIO9 | B8 | I | |  | |
| DMIC\_IN2 | B7 | I | | DMIC3/4 input | |
| DMIC\_IN3 | B6 | I | | DMIC5/6 input | |
| GPIO8 | A7 | O | |  | |
| DMIC\_CLK21 | A6 | O | | DMIC3/4 clock | |
| DMIC\_CLK31 | A5 | O | | DMIC5/6 clock | |
| RST\_N | D8 | I | | Chip reset | |
| GPIOAO | F5 | I | | Always-on wake up | |
| UART\_TXD | F4 | O | | UART TX data | |
| UART\_RXD | F3 | I | | UART RX data | |
| DFU\_N | E8 | I | | Firmware update enable | |
| GPIO10 | D2 | I | | I2C\_CLK | |
| GPIO11 | C2 | I | | I2C\_SDA | |
| GPIO12 | B2 | I | | I2S2\_CLK | |
| GPIO13 | A1 | I | | I2S2\_WS | |
| GPIO14 | A2 | I | | I2S2\_SDI | |
| GPIO15 | A3 | I | | I2S2\_SDO | |
| TEST-EN | C6 |  | | Test mode enable | |
| Audio  Interface | AIP1 | A8 | Analog | | MIC1 input P port | |
| AIN1 | A9 | Analog | | MIC1 input N port | |
| AIP2 | C9 | Analog | | MIC2 input N port | |
| AIN2 | B9 | Analog | | MIC2 input P port | |
| MICBIAS1 | C8 | Analog | | Micbias 1 | |
| MICBIAS2 | D8 | Analog | | Micbias 2 | |
| AOHPLP | E9 | Analog | | Left DAC P port | |
| AOHPLN | F9 | Analog | | Left DAC N port | |
| AOHPRN | G9 | Analog | | Right DAC N port | |
| AOHPRP | G8 | Analog | | Right DAC P port | |
| Auxiliary ADC | VINP0\_ADC | B1 | Analog | | GPADC0 input | |
| NC | NC | E2 | Analog | | NC | |
| NC | F1 | Analog | |  | |
| NC | E1 | Analog | |  | |
| GND | VSSA\_ADC | C3 | Analog | | Analog GND | |
| VSSA | D4 | Analog | | Analog GND | |
| VSSD | C4,C5,D5 | Analog | | Digital GND | |
| VSSA\_AVS | D6 | Analog | | Codec analog GND | |
| AVS\_ESR | E6 | | Analog | | DCDC2 GND | |
| AVS\_RAR | E5 | | Analog | | DCDC1 GND | |
| GNDSENSE | E4 | | Analog | | All regulator GNDsenses | |
| VSSA\_A0 | E7 | | Analog | | DAC driver GND | |
| VREFN | C7 | | Analog | | Codec reference GND | |

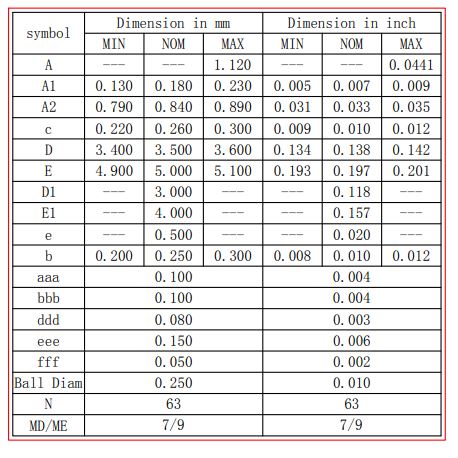
1. **Package information:**

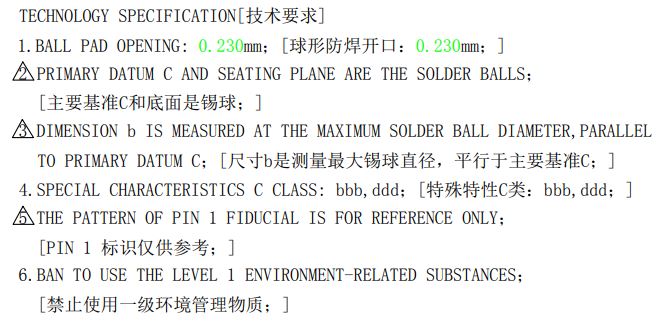
63 balls BGA: 0.5mm pitch for both x-direction and y-direction. Body size is 5.0 x 3.5mm.



BGA63 dimension information:







1. **Application BOM list:**

BOM list only convers electrical part, Mic & Speaker connection not included.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BOM list** | | | | |
| **Function** | **Description** | **R/L/C** | **Value** | **Comment** |
| CODEC | VCAP to VREFN | Cext1 | 10uF |  |
| Cext2 | 100nF |  |
| Vreg to VSSA | Cext3 | 4.7uF |  |
| Micbias1 to GND | CMic1 | 100nF | if Micbias1 in use |
| Micbias2 to GND | CMic2 | 100nF | if Micbias2 in use |
| Power-in | AVDPWR to GND | Cin1 | 10uF |  |
| DCDC1 | Switch inductor | L | 3.3uH |  |
| Vout to GND | C1 | 10uF |  |
| DCDC2 | Switch inductor | L | 3.3uH |  |
| Vout to GND | C1 | 10uF |  |
| LDO-IP33 | Vout to GND | C1 | 1uF |  |
| LDO-IO33 | Vout to GND | C1 | 1uF |  |
| LDO\_OPM | Vout to GND | C1 | 1uF |  |
| Xtal  Oscillator | XI to XO | Crystal | 24MHz |  |
| XI to GND | Cx1 | 8pF |  |
| XO to GND | Cx2 | 8pF |  |
| XI to XO | Rf | 1MΩ |  |
| **Total** |  | **17** | **part** |  |