Rose Epstein

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EDUCATION

Simon Fraser University — BASc. in Engineering Science **Graduation: Dec 2025**
Computer Engineering – *CGPA: 3.14* Burnaby, BC
University of Saskatchewan — BSc. in Biomedical Sciences **Sept 2016 — June 2020**
Physiology & Pharmacology – *Graduated with Great Distinction* Saskatoon, SK

TECHNICAL SKILLS

Programming Languages: C / C++, VHDL, SQL, MATLAB, Haskell
Tools, Frameworks & Technologies: Git, Visual Studio Code, Quartus Prime, Xilinx Vivado and Vitis, Linux, macOS, Windows
Relevant Courses: Embedded Systems, Digital Systems Design, Advanced Digital Systems, Programming for Heterogeneous Systems

WORK EXPERIENCE

Application Engineer **Jan — Apr 2022**
Epic Semiconductors Vancouver, BC

- Executed experiments for process and product development, including circuit analysis, populating PCBs with SMD soldering, followed by debugging and verification.
- Managed an ECG-signal producing PCB project for client demonstrations, including initial breadboard testing and circuit analysis, programming the chip to generate the ECG signal, designing and populating the PCB, and conducting extensive testing to achieve successful results.
- Designed and tested a gesture detection circuit to be used for future client demonstrations, conducting the initial circuit analysis to ensure functionality and extensively testing on a breadboard to determine the optimal design prior to implementation.

LEADERSHIP EXPERIENCE

Co-President **May 2022 — 2023**
Women in Engineering (WiE) Burnaby, BC

- Led and coordinated a team to manage various social, academic, internal and external responsibilities.
- Facilitated club meetings with club members, encouraging effective communication, and supporting a strong sense of teamwork and community.
- Built relationships with SFU faculty, SFU clubs, and external organizations to organize events, create networking opportunities, and secure funding and resources for female students at SFU and in the community.

PROJECT EXPERIENCE

Interrupt Driven Graphical Interface on FPGA with Vivado and Vitis: **Spring 2024**

- Designed interrupt-driven VGA graphics interface on Xilinx Zedboard, with push button input for real-time user interaction.
- Developped interrupt service routines to handle real-time GPIO events and signal snake movement or screen navigation to ensure proper handling of graphical displays for VGA output display.
- Thoroughly tested and integrated individual graphical elements, verifying visual accuracy and correct dunctionality of interrupt routines, ensuring smooth screen updates in response to GPIO inputs on VGA display.

Graphical 2D Game Application on FPGA with Vivado and Vitis: **Spring 2024**

- Developped a 2D Graphical Snake Game on Xilinx Zedboard utilizing Vivado and Vitis C/C++ tools, optimising memory usage and resource utilisation for smooth game performance.
- Implemented seamless gameplay mechanics (snake movement, reward collection, player controls) and menu navigation (setting selections and screen transitions), all with smooth real-time screen display updates.
- Integrated interrupt driven graphical interface with the VGA controller plus other crucial IP blocks and SoC, creating a seamless embeded system.
- Independently designed, implemented and tested the hardware, using Xilinx Vivado, and the software, using Xilinx Vitis.

Customized UART Protocol on FPGA with VHDL: **Summer 2023**

- Implemented UART protocol on Altera DE2 FPGA using VHDL, with baud rate generation, data framing and error detection.
- Coordinated with a group to design, implement, and optimize a UART protocol in VHDL on the FPGA board.
- Implemented the transmitter component to send data serially to the receiver, taking input data from the on-board switches and initiating transmission with a key press.
- Extensively tested the transmitter and receiver copmonents indiviudally, then together with the system with testbenches using ModelSim.