Rose Epstein

+1(306) 850 –7153 | rea13@sfu.ca | Rose–Epstein |

TECHNICAL SKILLS

Programming Languages: C / C++, VHDL, SQL, MATLAB, Haskell, Assembly
Tools, Frameworks & Technologies: Git, Visual Studio Code, Quartus Prime, Modelsim, Xilinx Vivado, Linux, macOS, Windows
Relevant Courses: Embedded Systems, Digital Systems Design, Advanced Digital Systems, Programming for Heterogeneous Systems

WORK EXPERIENCE

Application Engineer **Jan — Apr 2022**
Epic Semiconductors Vancouver, BC

- Executed experiments for process and product development, including circuit analysis, populating PCBs with surface mount device soldering, followed by debugging and verification.
- Designed and implemented a C program on to produce an ECG signal from a **low pass filter as a PWM circuit**.
- IDesigned, tested and implemented a heart-shaped PCB to house the ECG producing circuit, to be used for future client demonstrations.
- Designed and tested a **complex theremin gesture detection circuit** to be used for future client demonstrations.

PROJECT EXPERIENCE

Snake Game on Zedboard: **Spring 2024**

- Developed **interrupt-driven VGA graphics iterface for Snake Game on Xilinx Zedboard**, with push button input for real-time user interaction.
- Implemented the interrupt handler, and integrated this with the VGA controller and SoC, creating a seamless embeded system.
- Designed **game logic in software using C++**, and created all **custom graphics with GiMP**, including game screens, sprites and animations.
- Independently designed, implemented and tested the hardware, using Xilinx Vivado, and the software, using Xilinx Vitis.

Gaussian Elimination Kernel FPGA Optimization: **Fall 2023**

- Implement an **FPGA acceleration project** on the Gaussian Elimination kernel from GPU benchmark suite Rodinia using **High-Level Synthesis (HLS) C++.**
- **Optimized the data transfer** between the host and FPGA with memory coalescing optimizations

Customized UART Protocol in an FPGA: **Summer 2023**

- Implemented **UART protocol on the Altera DE2 FPGA** using VHDL, with baud rate generation, data framing and error detection.
- Coordinated with a group to design, implement, and optimize a UART protocol in VHDL on the FPGA board.
- Implemented the transmitter component to send data serially to the receiver, and extensively tested the entire system with a testbench using ModelSim.

Scrolling Message Display on FPGA **Fall 2021**

- Developed a VHDL program for the Altera DE2-115 board, to display a scrolling message on HEX display.
- Coordinated with a group of two to develop a **custom instruction set for ASIP** to meet the program requirements
- Implemented user interface for user input through the on board push-button to trigger different displays.

EDUCATION

Simon Fraser University - B.A.Sc., **Fall 2020 — Present**
B.A.Sc. Computer Engineering Burnaby, BC

- ***CGPA 3.16***

University of Saskatchewan **Fall 2016 — Summer 2020**
B.Sc. Physiology and Pharmacology Saskatoon, SK

- ***Graduated with great distinction***

LEADERSHIP EXPERIENCE

Co-President **May 2022 — 2023**
Women in Engineering (WiE) Burnaby, BC

- Organized and hosted club weekly meetings, and coordinated with members for **event planning**.
- Provided supports for new students and club members beginning their university career.
- Helped strengthen the community bond and support for **women in engineering at SFU**.