Rose Epstein

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EDUCATION AND TECHNICAL SKILLS

Simon Fraser University **Graduation: Dec 2025**
BASc. in Engineering Science, Computer Engineering Burnaby, BC
University of Saskatchewan **Sept 2016 — June 2020**
BSc. in Biomedical Sciences, Physiology and Pharmacology Saskatoon, SK

Programming Languages: C / C++, VHDL, SQL, MATLAB, Haskell
Tools, Frameworks & Technologies: Git, Visual Studio Code, Quartus Prime, Modelsim, Xilinx Vivado, Linux, macOS, Windows
Relevant Courses: Embedded Systems, Digital Systems Design, Advanced Digital Systems, Programming for Heterogeneous Systems

WORK EXPERIENCE

Application Engineer **Jan — Apr 2022**
Epic Semiconductors Vancouver, BC

- Executed experiments for process and product development, including circuit analysis, populating PCBs with SMD soldering, followed by debugging and verification.
- Developed a C program on to produce an ECG signal from a PWM circuit.
- Designed, tested and implemented a heart-shaped PCB to house the ECG producing circuit, to be used for future client demonstrations.
- Designed and tested a complex theremin gesture detection circuit to be used for future client demonstrations.

LEADERSHIP EXPERIENCE

Co-President **May 2022 — 2023**
Women in Engineering (WiE) Burnaby, BC

- Led and coordinated a team of 20 members to manage various social, academic, internal and external responsibilities.
- Facilitated club meetings with club members, encouraging effective communication, and supporting a strong sense of teamwork and community.
- Built relationships with SFU faculty, SFU clubs, and external organizations to organize events, create networking opportunities, and secure funding and resources for members and female students.

PROJECT EXPERIENCE

Snake Game on Xilinx Zedboard with Vivado: **Spring 2024**

- Developed interrupt-driven VGA graphics iterface for Snake Game on Xilinx Zedboard, with push button input for real-time user interaction.
- Implemented the interrupt handler, and integrated this with the VGA controller and SoC, creating a seamless embeded system.
- Designed game logic in software using C++, and created all custom graphics with GiMP, including game screens, sprites and animations.
- Independently designed, implemented and tested the hardware, using Xilinx Vivado, and the software, using Xilinx Vitis.

Gaussian Elimination Kernel FPGA Optimization with C++: **Fall 2023**

- Implement an FPGA acceleration project on the Gaussian Elimination kernel from GPU benchmark suite Rodinia using High-Level Synthesis (HLS) C++.
- Optimized the data transfer between the host and FPGA with memory coalescing optimizations

Customized UART Protocol in an FPGA with VHDL: **Summer 2023**

- Implemented **UART protocol on the Altera DE2 FPGA** using VHDL, with baud rate generation, data framing and error detection.
- Coordinated with a group to design, implement, and optimize a UART protocol in VHDL on the FPGA board.
- Implemented the transmitter component to send data serially to the receiver, and extensively tested the entire system with a testbench using ModelSim.

Scrolling Message Display on FPGA with VHDL **Fall 2021**

- Developed a VHDL program for the Altera DE2-115 board, to display a scrolling message on HEX display.
- Coordinated with a group of two to develop a **custom instruction set for ASIP** to meet the program requirements
- Implemented user interface for user input through the on board push-button to trigger different displays.