Rose Epstein

Vancouver, BC | +1(306) 850 7153 | rea13@sfu.ca | Rose–Epstein

EDUCATION

Simon Fraser University — BASc. in Engineering Science — **Graduation: Dec 2025**
Computer Engineering – *CGPA: 3.14* — Burnaby, BC

University of Saskatchewan — BSc. in Biomedical Sciences — **Sept 2016 — June 2020**
Physiology & Pharmacology – *Graduated with Great Distinction* — Saskatoon, SK

TECHNICAL SKILLS

Programming Languages: C / C++, VHDL, SQL, MATLAB, Haskell
Tools, Frameworks & Technologies: Git, Visual Studio Code, Quartus Prime, Xilinx Vivado and Vitis, Linux, macOS, Windows
Relevant Courses: Embedded Systems, Digital Systems Design, Advanced Digital Systems, Programming for Heterogeneous Systems

WORK EXPERIENCE

Application Engineer — **Jan — Apr 2022**
Epic Semiconductors — Vancouver, BC

- Executed experiments for process and product development, including circuit analysis, populating PCBs with SMD soldering, and performing debugging and verification.
- Managed an ECG-signal producing PCB project for client demonstrations, including breadboard testing and circuit analysis, programming for signal generation, PCB design and population, and extensive testing to achieve successful results.
- Designed and tested a gesture detection circuit for future client demonstrations, performing initial circuit analysis and extensively testing on a breadboard to optimize design prior to implementation.

LEADERSHIP EXPERIENCE

Co-President — **May 2022 — 2023**
Women in Engineering (WiE) — Burnaby, BC

- Led and coordinated a team to manage various social, academic, internal, and external responsibilities.
- Facilitated club meetings with club members, encouraging effective communication and supporting a strong sense of teamwork and community.
- Built relationships with SFU faculty, other SFU clubs, and external organizations to organize events, create networking opportunities, and secure funding and resources for female students at SFU and in the broader community.

PROJECT EXPERIENCE

Interrupt Driven Graphical Interface on FPGA: — **Spring 2024**

- Designed an interrupt-driven VGA graphical interface on Xilinx Zedboard, with push button input for real-time user interaction.
- Developed an interrupt service routine in C++ to handle real-time GPIO events to ensure proper graphical display for VGA output.
- Thoroughly tested and integrated graphical elements, verifying visual accuracy and smooth screen updates in response to GPIO inputs.

Graphical 2D Game Application on FPGA with Vivado and Vitis: — **Spring 2024**

- Developed a 2D Graphical Snake Game on Xilinx Zedboard utilizing Vivado and Vitis tools, optimizing memory usage and performance.
- Implemented seamless gameplay mechanics and menu navigation all with smooth real-time screen display updates.
- Integrated the interrupt-driven graphical VGA interface with the SoC, creating a seamless embedded system.
- Independently designed, implemented, and tested the hardware using Xilinx Vivado, the software using Xilinx Vitis.

Customized UART Protocol on FPGA with VHDL: — **Summer 2023**

- Implemented UART protocol on Altera DE2 FPGA using VHDL, with baud rate generation, data framing, and error detection.
- Collaborated with a team to design, implement, and optimize a UART protocol in VHDL.
- Developed the transmitter component to send data serially to the receiver, taking input data from the on-board switches, with transmission initiated by a key press.
- Extensively tested the transmitter and receiver components, both individually and in conjunction with the SoC, using testbenches in ModelSim.