SCHOOL OF COMPUTING AND ENGINEERING SCIENCES

BACHELOR OF SCIENCE IN INFORMATICS AND COMPUTER SCIENCE

END OF SEMESTER EXAMINATION

ICS 2104: COMPUTER ORGANIZATION AND ARCHITECTURE

DATE: 8th September 2021   Time: 2 HOURS

INSTRUCTIONS:

1. *This examination consists of **FIVE** questions*
2. *Answer **Question ONE (COMPULSORY)** and any other **TWO** questions*

QUESTION 1 - 30 MARKS

a) The following graph (Figure 1) captures different microprocessor trends over the years. Answer the following questions based on the Figure.
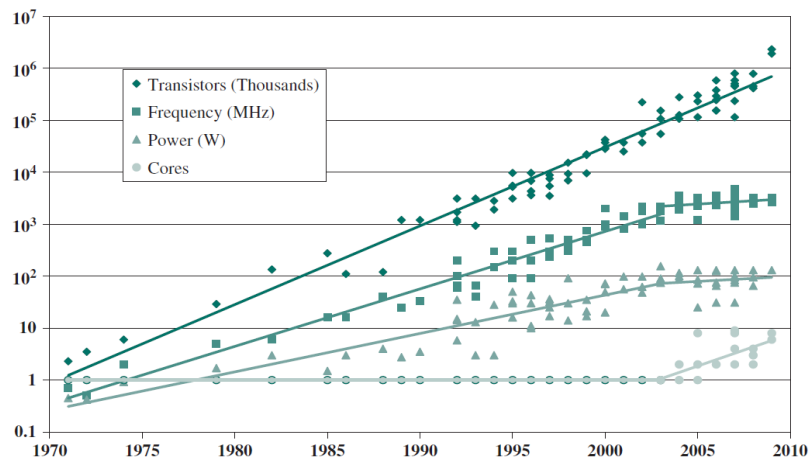

Figure 1: Processor Trends

i.   BRIEFLY DESCRIBE relationship between the cores and frequency trends (2 marks)

ii.   Sketch the behaviour of the transistor and power trends in Question One (a)(i) above from 2010 – 2021 (4 marks)

iii.   Explain the behaviour of your curves drawn in Question One (a)(ii) above (2 marks)

b) Assume a hypothetical compute X which has 7 address lines, 8 data lines, L1 cache (32 bytes) and block size of 8 bytes. This computer serves as a model or abstraction of the step-by-step behaviour of a real-life digital computer. Being only a model - and thus a simplification of reality - the hypothetical computer does not possess all the capabilities of a real-world general-purpose computer; however, it operates essentially the same way. In addition, the computer has the following specifications:

- *The Central Processing Unit (CPU): Control unit (CU): does the decoding (or interpreting) of instructions and sends out the electronic signals that cause an instruction to be executed.*

- *Arithmetic/logic unit (ALU): carries out the arithmetic calculations (e.g., adding) and logical calculations (e.g., comparing).*

- *Registers – ACC, B, C, D, E, Program Counter (PC), Stack Pointer (SP) – these are special, high-speed storage cells that are directly accessible by the CU and ALU*

- *The Accumulator (ACC) (8 bits) - holds data that has just been produced as the result of an instruction or that is about to be operated upon*

- *Instruction Set:*

    Opcode   Name   Effect

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    0010   WRITE   displays contents of ACC onto screen
    0011   LOAD   copies contents of memory address into ACC
    0101   STORE   copies contents of ACC into specified memory location
    0110   ADD   adds contents of specified register to ACC
    1000   SUB   subtracts contents of specified register from ACC
    1010   MOV Rd, Rs copies contents of register Rs to Register Rd

GIVING EXAMPLES based on **based on the above information**, answer the following questions.

    i.   Given TWO numbers – 100 and 80 - stored in memory location 20H & 25H respectively, WRITE a simple assembly program to subtract the numbers

(100-80) based on the given INSTRUCTION SET and display result on the screen (5 marks)

    ii.   How many bytes of data in RAM is accessible to the computer X? Briefly explain how you arrived at your answer (3 marks)

    iii.   Calculate the block index and cache index (4 marks)

    iv.   ILLUSTRATE the Direct Cache Mapping scheme (6 marks)

c) Since the invention of transistors in 1950's, microprocessor design has evolved over time. Certain technologies have been embraced by microprocessor manufacturing entities which has resulted in a significant **increase in performance**. *Basing your argument(s) on computer X or a practical example*, **ILLUSTRATE** *how* each of the following microprocessor design technologies have contributed to better performance over time (4 marks)

    i.   Branch prediction

    ii.   Pipelining

QUESTION 2 - 15 MARKS

In computing, cache algorithms – also called cache replacement algorithms or cache replacement policies – manages frequently required instructions/data required by the processor. Caching improves performance by keeping recent or often-used data items in memory locations that are faster or computationally cheaper to access than normal memory stores. When the cache is full, the caching algorithm must choose which items to discard to make room for the new ones.

a) USING AN EXAMPLE, illustrate how cache can be updated using Least Recently Used (LRU) policy (4 marks)

b) BASING YOUR ARGUMENT in Question 1 (iv), ILLUSTRATE the difference between a cache hit and a cache miss based on any input sequence of your choice (6 marks)

c) LIST & EXPLAIN any THREE similarities between L1 & L2 cache (3 marks)

d) In terms of CACHE HIT RATE, Set Associative Mapping is more efficient as compared to Direct Mapping. True or False? Support your answer (2 marks)

QUESTION 3 - 15 MARKS

a) Error detection and correction is a key process in computer systems. The transmitted data can be corrupted during communication or storage thus the input data may not be the same as the output data. This kind of mismatch is known as "error."
   i.   List ANY TWO external storage devices (2 marks)
   ii.   List and explain ANY two common sources of errors (4 marks)

b) Computer system components are interconnected by communication pathways called buses. With aid of practical example(s), BRIEFLY highlight the role of each of the following buses while stating some of the factors which influence their size and features (9 marks) *Note: you can base your arguments on computer X described in Question ONE or any other computer of your choice*
   i.   Data bus
   ii.   Control bus
   iii. Address bus

QUESTION 4 - 15 MARKS

a) DESCRIBE any two roles of Memory Management Unit (MMU) (4 marks)

b) *Basing your argument(s) on the INTERRUPT HANDLING PROCESS*, BRIEFLY describe what happens when you plug in an external device such as keyboard or mouse into a computer through the I/O port (7 marks)

c) BRIEFLY DESCRIBE any FOUR I/O control methods *giving an example* in each case (4 marks)

The Figure 2 below shows a hypothetical Random Access Memory (RAM). It is divided into locations numbered from (row) 1: (column) 1 to (row) 6: (column) 4.
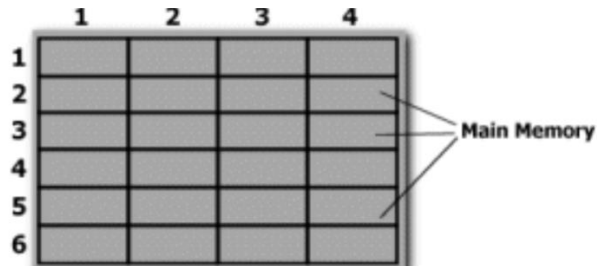

Figure 2: Hypothetical RAM

The Control Processing Unit (CPU) is responsible for carrying out all the computations such as arithmetic and logical operations. The CPU can only operate on data that has been loaded into one of its available six registers (A, B, C, D, E, or F). Computing the difference of two numbers - one stored in location 2:3 and another stored in location 5:2 - and then storing the result back in the location 2:3 can be achieved by either through the CISC or RISC approach as shown in the Table 1 below. Based on the given information, answer the following questions.

CISC Approach	RISC Approach
SUB 2:3, 5:2	LOAD A, 2:3
	LOAD B, 5:2
	SUB A, B
	STORE 2:3, A

Table 1: CISC vs RISC

i. STATE and EXPLAIN any THREE differences between CISC & RISC architecture (6 marks)

ii. Between CISC and RISC, which architecture would you choose if you had a company focussing on designing a new computer processor for local desktop computer manufacturing? Give reason(s) to support your argument? (6 marks)

iii. STATE and EXPLAIN any **TWO** variations of RAM (3 marks)