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THE RAM

How to improve the performance of the RAM

PREPARED BY

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INTRODUCTION.

The rate of improvement of a processor/microprocessor's speed is determined by the speed of the Random Access Memory (RAM). The main reason why the CPU is faster than the RAM is because CPUs have a cache on them where all the data access takes place. If there is data that is in memory but not in cache, it must be loaded into the cache first. Hence computer designers are faced with an increasing Processor-Memory Performance Gap. This is the primary obstacle to improve computer system performance. The performance of a computer depends on the interface between the processor and the memory.

There are 2 main types of RAM i.e., Static Random Access Memory (SRAM) and the Dynamic Random Access Memory (DRAM). In the SRAM, data is stored using the state of a six-transistor memory cell, it is mostly used as a cache memory for the processor. On the other hand, the DRAM allows the storage of each bit of data in a separate capacitor within a specific integrated circuit. It is however volatile and needs to be refreshed regularly else it loses the information stored on it.

Other types of RAM include;

Fast Page Mode Dynamic Random Access Memory (FPM DRAM)

Synchronous Dynamic Access Memory (SDR RAM)

Rambus Dynamic Random Access Memory (RD RAM)

Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM)

A. WAYS OF IMPROVING THE PERFORMANCE OF THE DRAM.

Introducing QSOI capacitorless dynamic random access memory Cell.

QSOI is an acronym for Quasi Silicon-on-insulator.

The QSOI DRAM Cell with bulk substrate is based on the promising highly scalable QSOI device structure. The deep L-shape layer of proposed QSOI cell provides isolation between adjacent cells along bit line without increasing the area the cell area.

The electrical performance of this structure ensures longer retention time and larger sensing margin due to the suppressed leakage current.

Introducing a Highly Scalable Capacitor-Less Cell Having Doubly Gated Vertical Channel

A doubled-gate transistor structure with a vertical channel is suited well for the DRAM for it occupies only 4F^2 area. This is good for it provides good retention characteristics. It is also compatible with conventional memory process flows for stand-alone DRAM.

DGVC is more scalable compared to the previous cell designs.

Using Magneto resistive Random-Access Memory Technology.

The MRAM technology combines a spintronic device with standard silicon-based microelectronics to obtain attributes not found in other memory technologies.

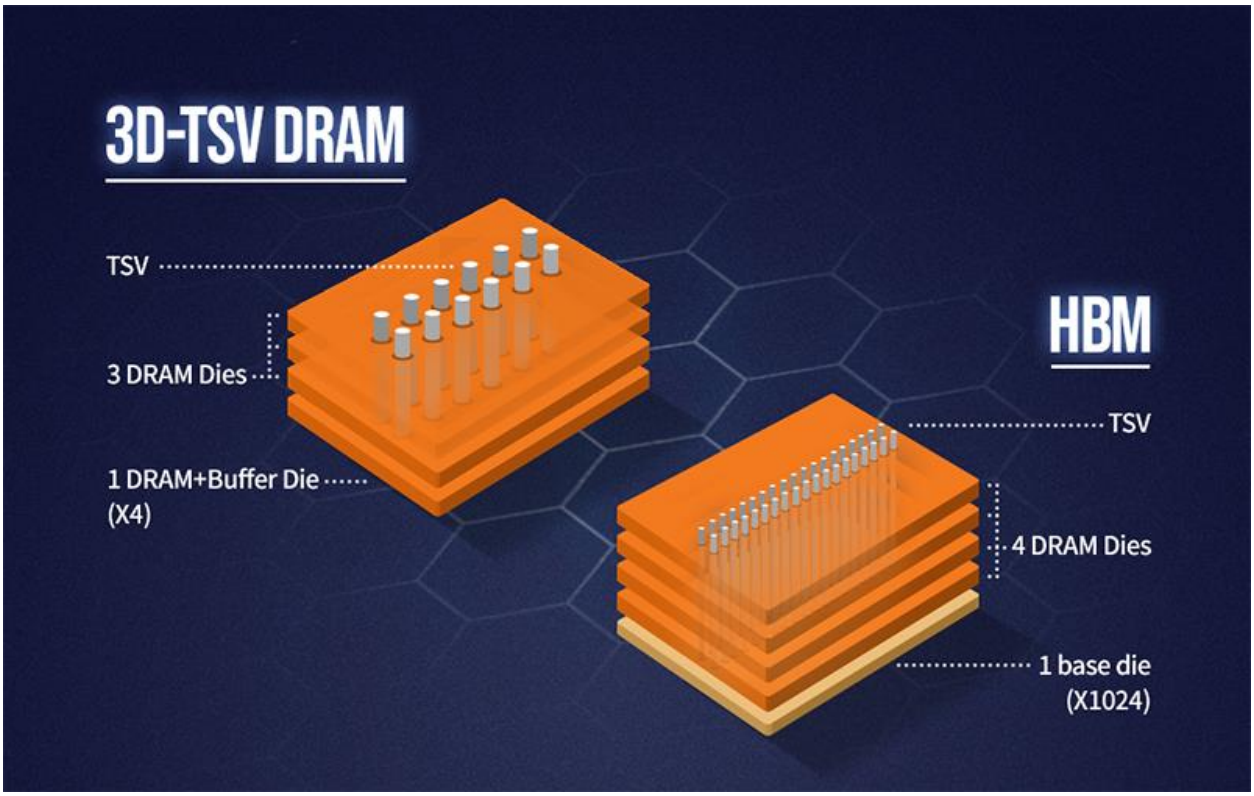
The key attributes of MRAM technology are nonvolatility and unlimited read and write endurance.

Supriya Chakraborty, Manan Suri, "Experimental Study of Adversarial Magnetic Field Exposure Attacks on Toggle MRAM Chips", *IEEE Transactions on Electron Devices*, vol.69, no.3, pp.1480-1485, 2022.

Scaling of the DRAM using Through Silicon-Vias (TSVs)

With the rapid growth and vast expansion of AI, machine learning, high-performance computing and network applications, there is demand for higher performance of the memory. Unfortunately, the traditional main memory DRAM alone has not been sufficient this need.

Through TSVs in memories there is an efficient foundational technology for capacity expansion and bandwidth extension. The vias are perforated through the entire silicon wafer thickness. This ensures formation of thousands of vertical interconnections from the front to the backside of the die and vice versa.



B. WAYS OF IMPROVING THE PERFORMANCE OF THE SRAM.

The SRAM based cache memory is an essential part of electronic devices. The major problem affecting the SRAM is power loss and stability.

The following are some ideas on how to improve the performance of the SRAM.

Designing a stable low power 11-T Static Random-Access Memory Cell

The 11-T has a low power dissipation while upholding the stability and moderate performance. The 11-T has 10.63% improved read signal to noise margin and 33.09% improved write signal to noise margin. The proposed 11-T SRAM consumes less energy compared to other topologies. It also occupies 13.11%lesser area.

(Wai.K (2005) Journal of Circuits, Systems and Computers)

Widening both the DRAM and SRAM

One way of making the memory faster is widening the memory system. Instead of having just 2 rows of DRAM, multiple rows can be created. Now on every100-ns cycle, we get 32 contiguous bits and cache-line are 4 times faster. We can improve the performance of the memory by increasing the width of the memory system up to the length of the cache line, at which we can fill the entire line in a single memory cycle.

Although this is a good idea it has one disadvantage, the DRAMs must be added in multiples.

Large Cache

As I've mentioned before, the disparity between the CPU speed and memory is growing. However, having a large enough cache improves the performance of the PC. Having a program that is too large for the cache causes the performance to drop off considerably with a factor of 10 or more depending on the access patterns. (Kevin Dowd,2010)

Improving security with encrypted DRAM and SRAM.

The DRAM and SRAM have recently shown to be vulnerable to physical attacks. The Cryptkeeper is a software-encrypted virtual manager that mitigates data exposure when used with a secure key-hiding mechanism.

The cryptkeeper reduces the amount of cleartext data in the memory system by dividing the DRAM and SRAM into smaller, cleartext working set and a larger, encrypted area. This extends the standard memory model and provides encrypted swap as a side effect. (Kevin Dowd,2010)

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