



```
module FullAdder(output s, co, input a, b, ci);  
  logic axorb;  
  assign axorb = a ^ b;  
  assign s = axorb ^ ci;  
  always @ (b,ci,axorb)  
  begin  
    if (axorb)  
      co = ci;  
    else  
      co = b;  
    end  
  end  
endmodule: FullAdder
```

SystemVerilog for Digital Circuit Modelling

Roshan Weerasekera

roshanw@gmail.com