

Analogue Circuit Design using BJTs

Dr. Roshan Weerasekera

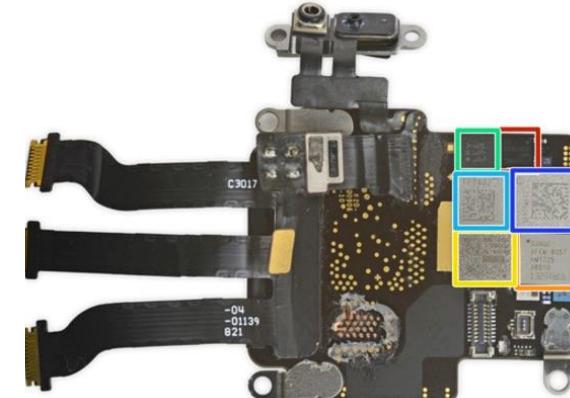


Source: <https://www.analog.com/en/analog-dialogue/raqs/raq-issue-164.html>

Analogue Electronic Design



<https://hackaday.com/2016/05/30/gutting-and-rebuilding-a-classic-watch/>



<https://www.iphoneincanada.ca/news/apple-watch-series-3-teardown/>

The world is Analog(ue)!

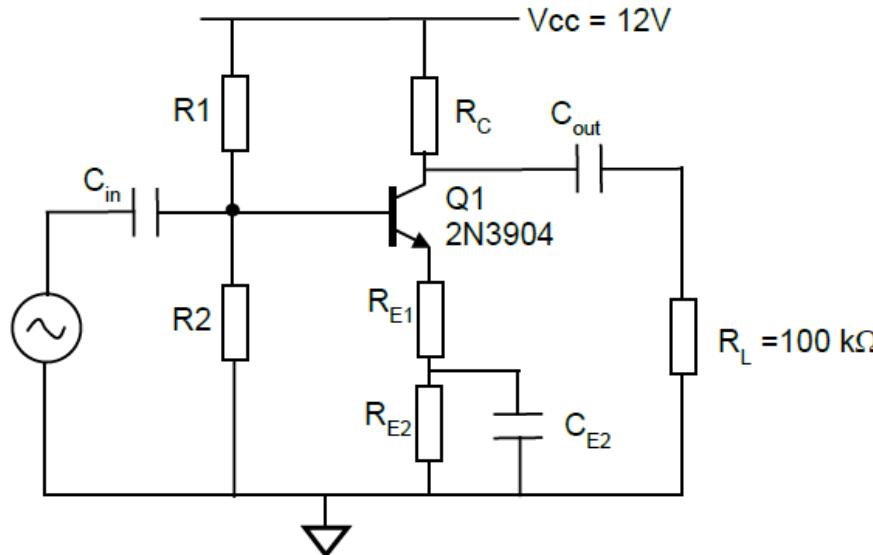
Natural things are Analogue not Digital; our brains are analogue yet powerful than digital computers!

“sounds are analog signals; they are continuous time and continuous value. Our ears listen to analog signals and we speak with analog signals. Images, pictures, and video are all analog at the source and our eyes are analog sensors. Measuring our heartbeat, tracking our activity, all requires processing analog sensor information.”

https://www.ee.columbia.edu/~kinget/WhyAnalog/circuitcellar_The_World_Is_Analog_201410.pdf

What Should My Circuit Do?

- ❑ The very first step to any simulation is to know how your circuit should behave.
Simulation is a verification tool **NOT A CIRCUIT SOLVER**.
- ❑ So how should this circuit behave?

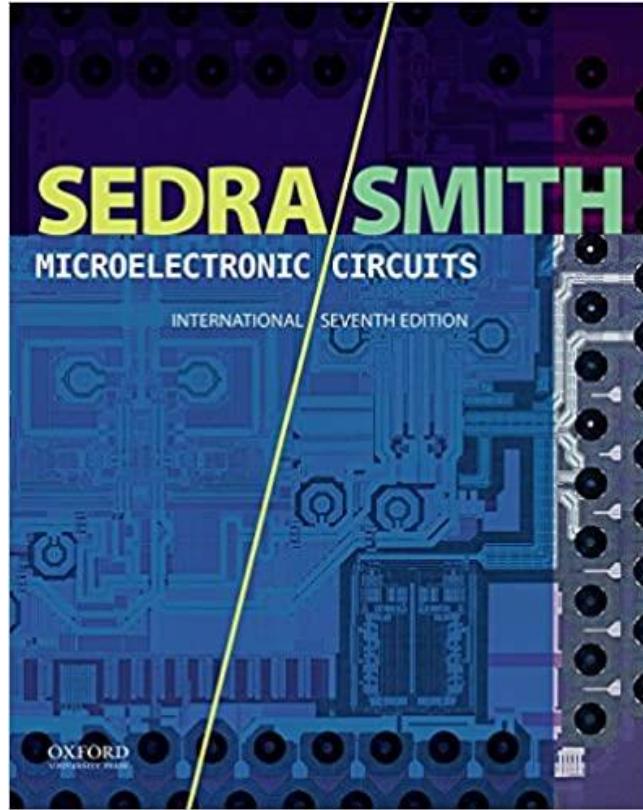
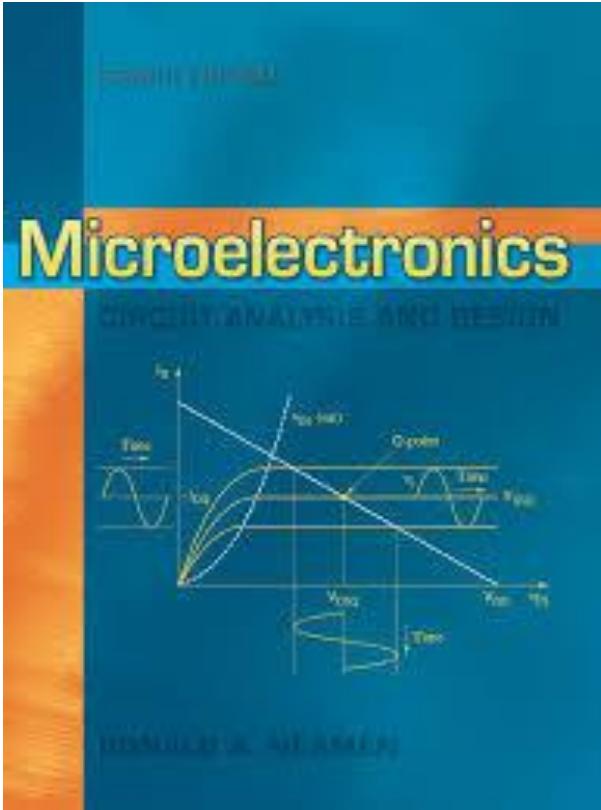


Computer Simulations: the problem



Need Equations to Understand the circuit behaviour and validate!

Main References



Content

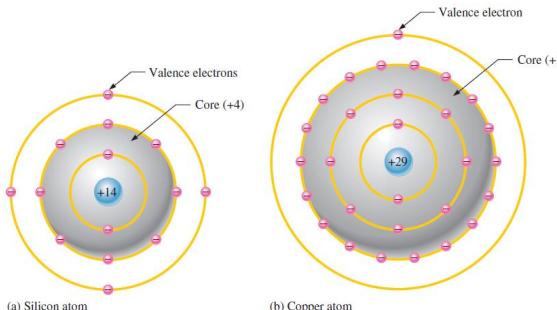
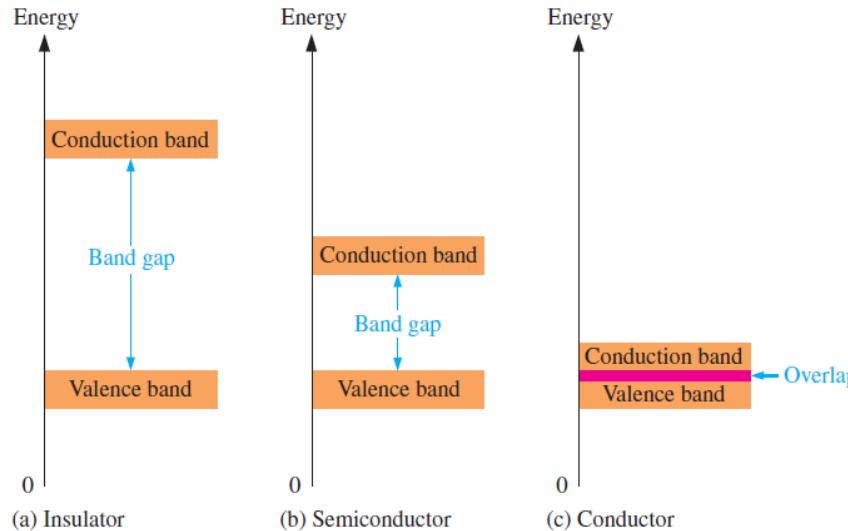
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1	<u>Introduction to Semiconductors</u>
2	<u>Bipolar Junction Transistors (BJT) and BJT Circuits at DC</u>
3	<u>BJT Small-Signal Model</u>
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1. Introduction to Semiconductors

Electrical Behaviour of Materials

- ❑ Conductors: Capable of carrying electric current
 - material has mobile charge carriers (electrons, ions)
 - With increasing temperature, conductivity reduces
- ❑ Insulators: materials with no or very few free charge carriers
 - E.g. Quartz, plastics
 - With increasing temperature, conductivity increases
- ❑ Semiconductors: materials with conductivity between that of conductors and insulators
 - E.g. Silicon (Si), Germanium (Ge), GaAS, GaP, InP
 - With increasing temperature, conductivity increases
- ❑ superconductors: certain materials have zero resistivity at very low temperature.

Energy Bands



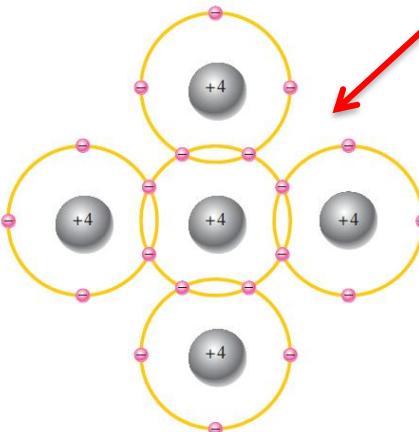
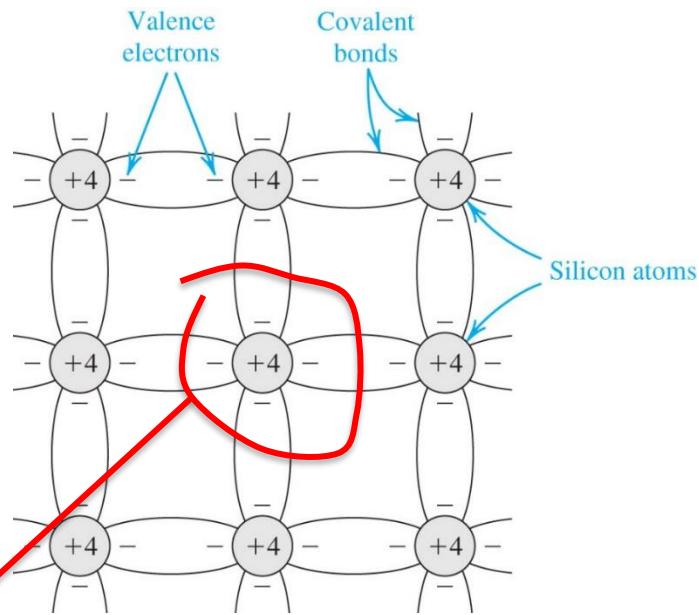
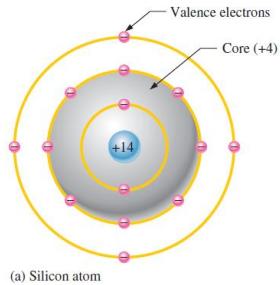
Semiconductors: Silicon

- Metal
- Semi-Metal
- Non-metal

	13	14	15	16
11	B Boron	C Carbon	N Nitrogen	O Oxygen
12	Al Aluminum	Si Silicon	P Phosphorus	S Sulfur
Cu Copper	Zn Zinc	Ga Gallium	Ge Germanium	As Arsenic
Ag Silver	Cd Cadmium	In Indium	Sn Tin	Sb Antimony
Au Gold	Hg Mercury	Tl Thallium	Pb Lead	Bi Bismuth
Rg Rutherfordium	Uub Ununbium	Uut Ununtrium	Uuq Ununquadium	Uup Ununpentium

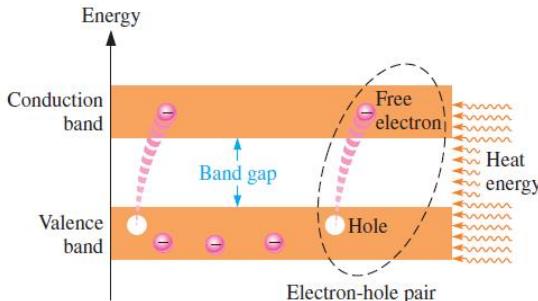
Dy Dysprosium	67 Holmium	7648.9 Praseodymium	68 Europium	167.0 Thulium	69 Ytterbium	70 Yttrium	71 Lutetium
Cf Cf	Es Einsteinium	Fm Fermium	Md Mendelevium	No Neptunium	Lu Lanthanum		

© One-

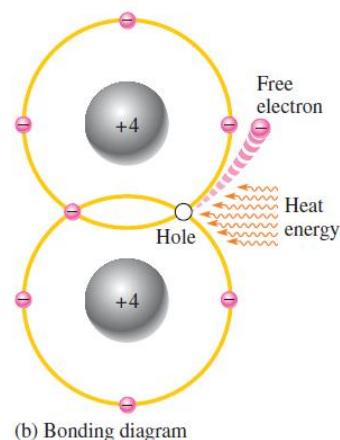


Silicon

- ❑ There are no free electrons to conduct electric current in Silicon.
- ❑ As temperature increases, covalent bonds breaks loose and it becomes mobile and can conduct electrical current.



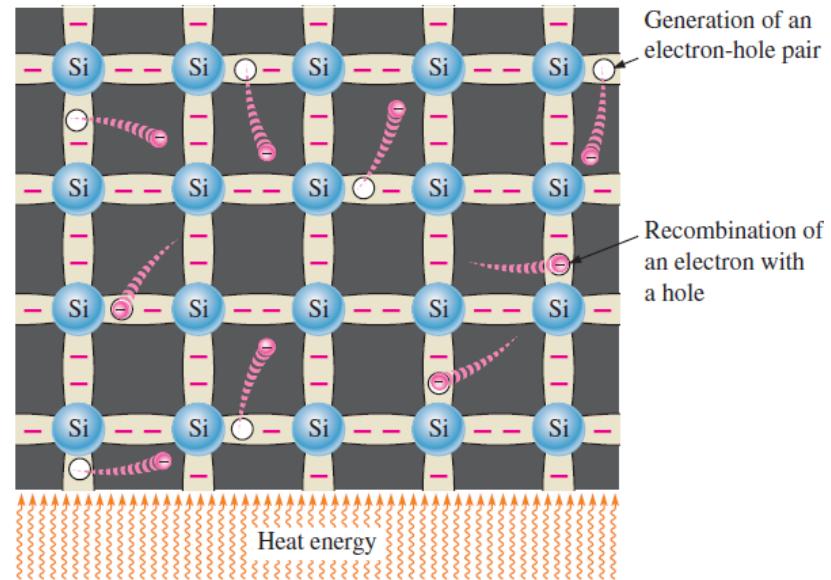
(a) Energy diagram



(b) Bonding diagram

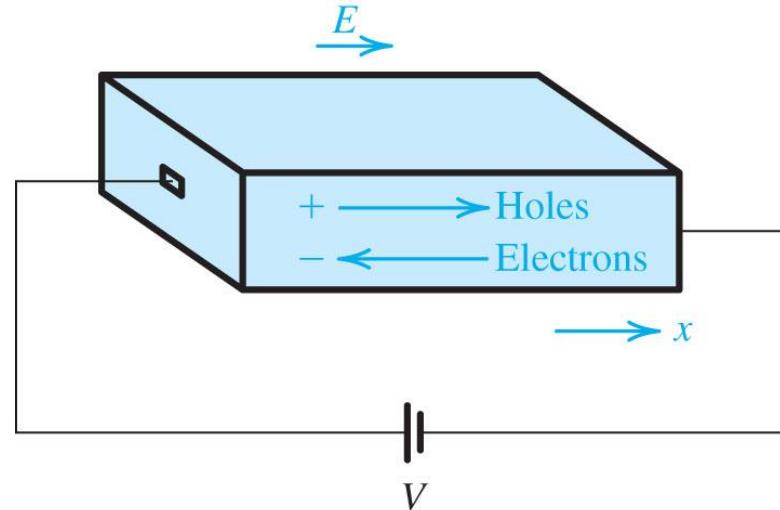
Carrier Concentration of Si = $\sim 10^{10}$ cm⁻³

- Two types of current carriers
- Holes
 - Electrons

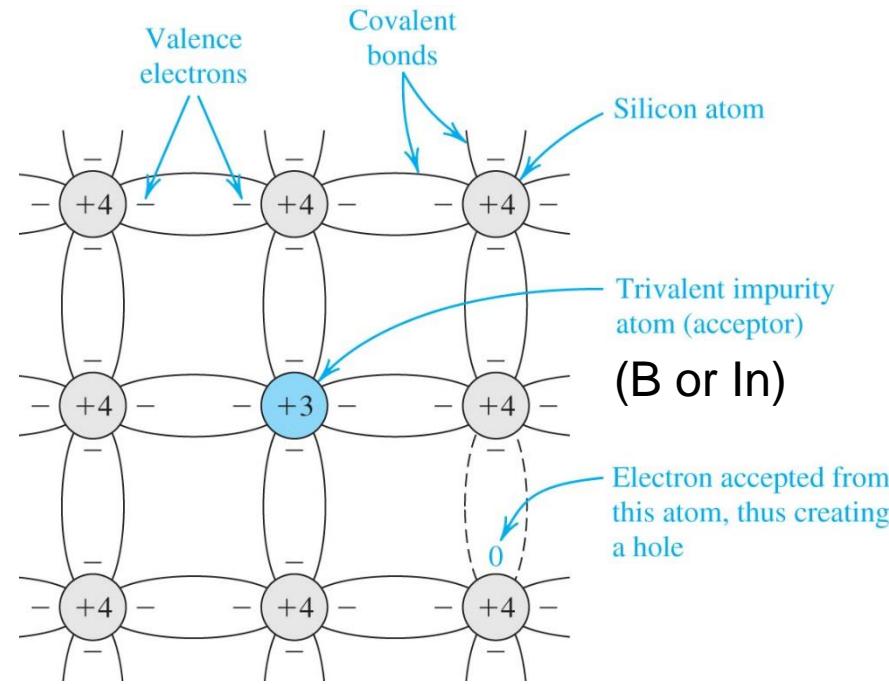
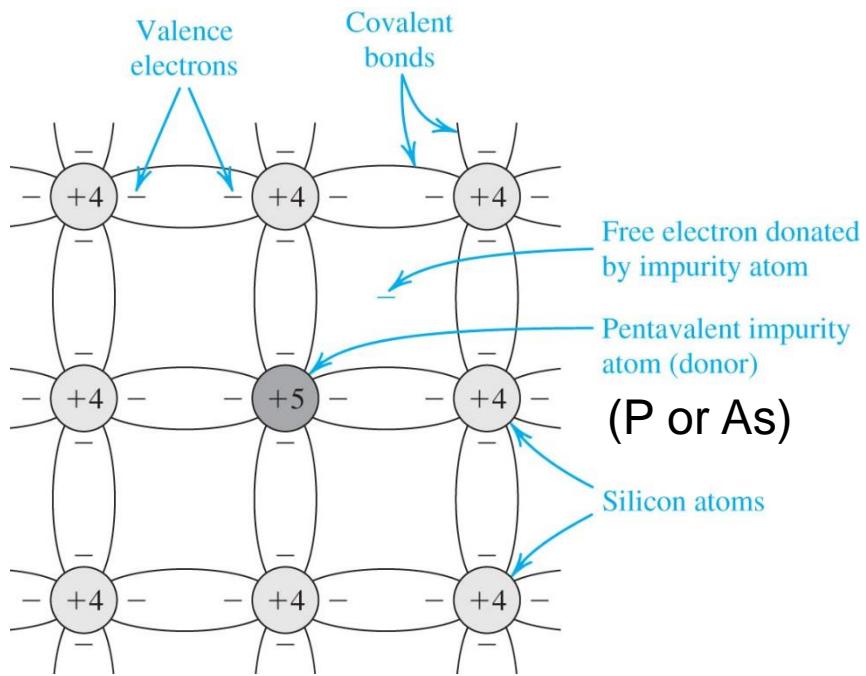


Applying a bias to a semi-conductor

- When a voltage is applied across a piece of intrinsic silicon the thermally generated free electrons in the conduction band, which are free to move randomly in the crystal structure, are now easily attracted toward the positive end.
- This movement of free electrons is one type of **current** in a semiconductive material and is called *electron current*.



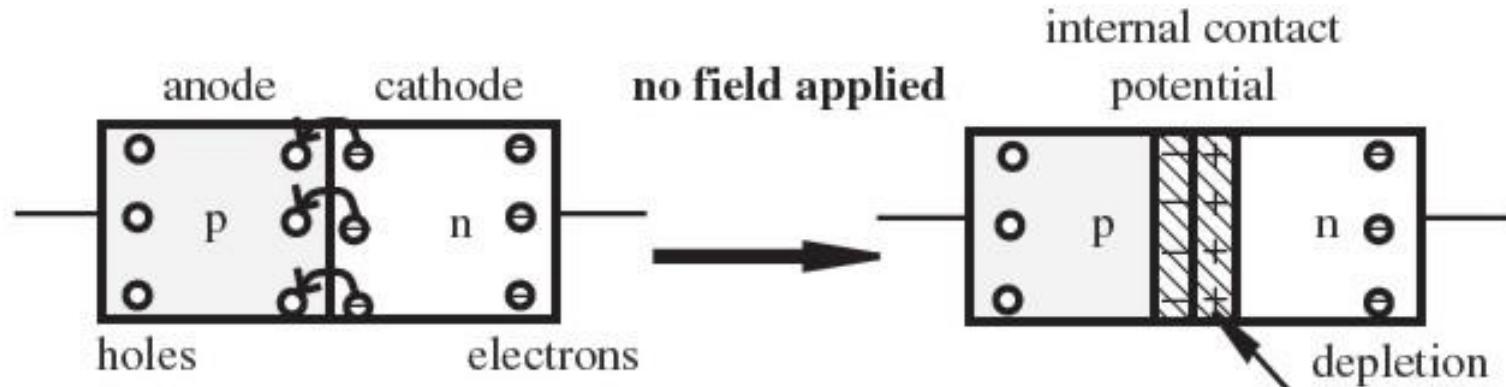
N-type and P-type Silicon



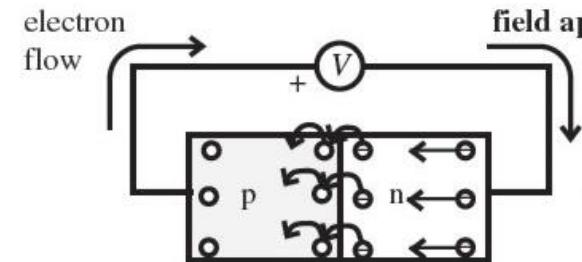
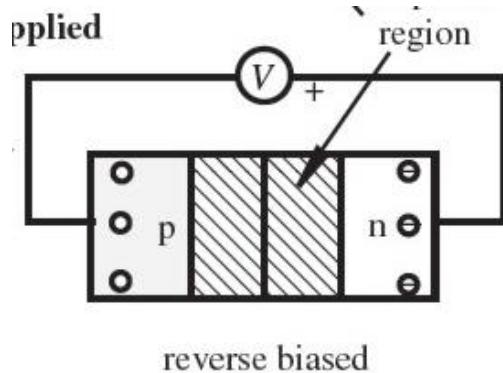
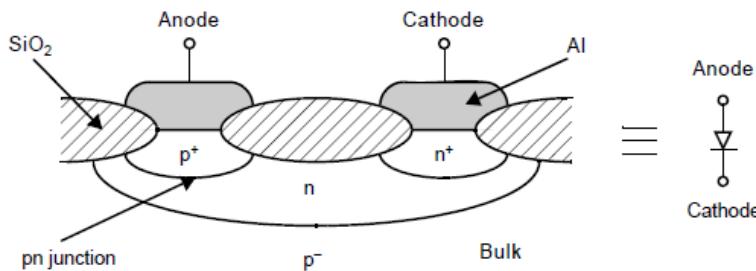
After doping Carrier Concentration $\sim 10^{16} \text{ cm}^{-3}$

P-N Junction

- ❑ semiconductor in which impurity changes abruptly from p-type to n-type
- ❑ holes “diffuse” towards and across boundary into n-type and capture electrons
- ❑ electrons diffuse across boundary, fall into holes (“recombination of majority carriers”)
- ❑ The space charge due to immobile ions in the depletion region establishes an electric field that opposes carrier diffusion.

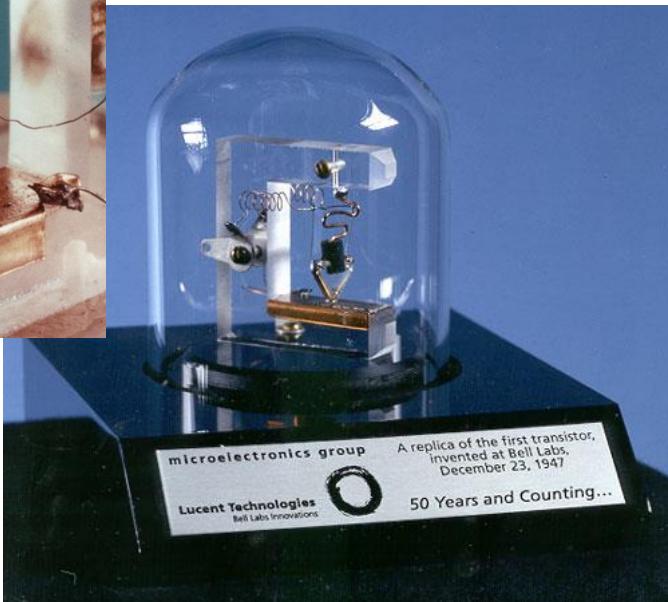
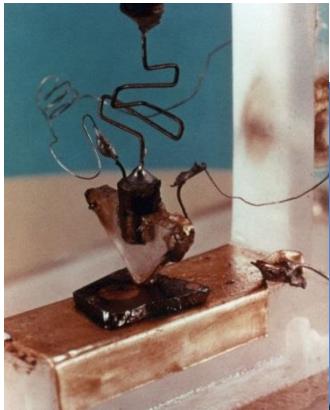


P-N Junction behaviour



2. Bipolar Junction Transistors (BJTs)

Bipolar Junction Transistor (BJT)



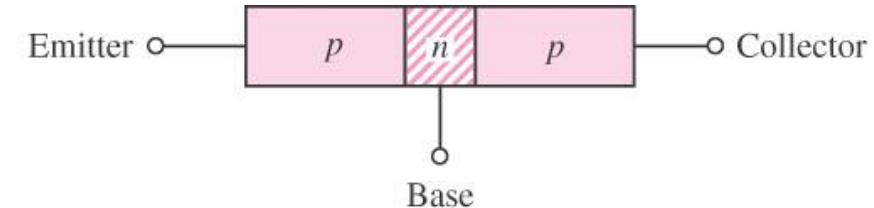
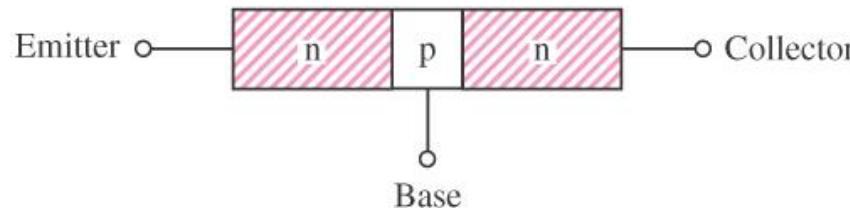
... led to electronics changing the way we work, play, and indeed, live.



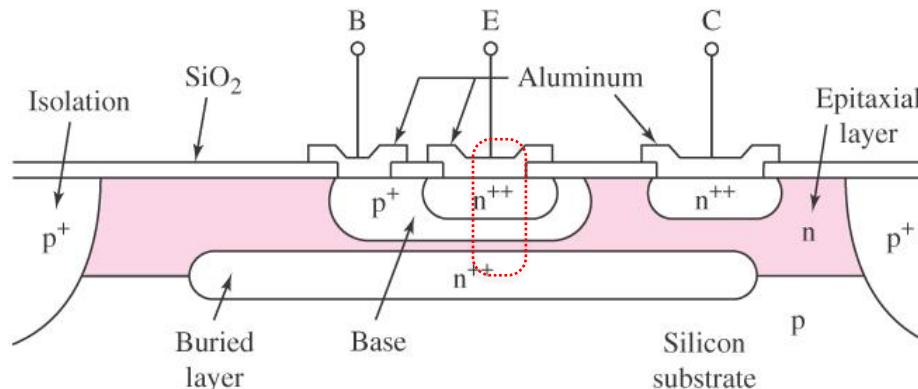
John Bardeen, William Shockley and Walter Brattain at Bell Labs, 1948.

BJT Structure

- There are two types of bipolar transistors: npn and pnp.

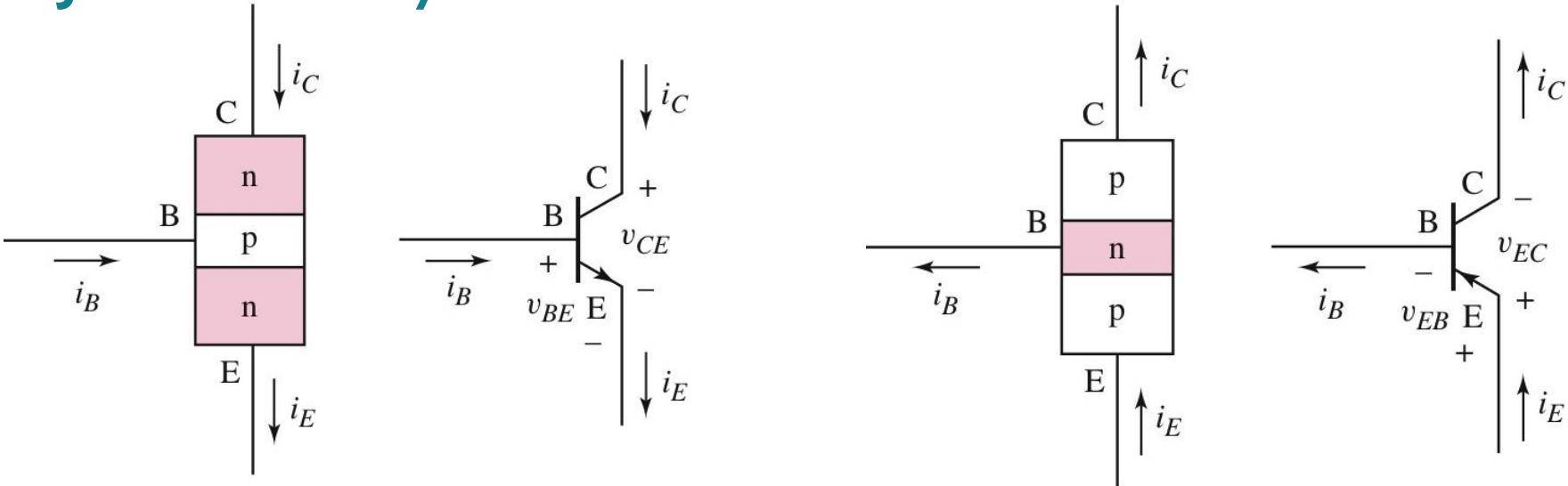


the device is not symmetrical electrically



Thin layer between E & B

BJT Circuit Symbols and Current Conventions

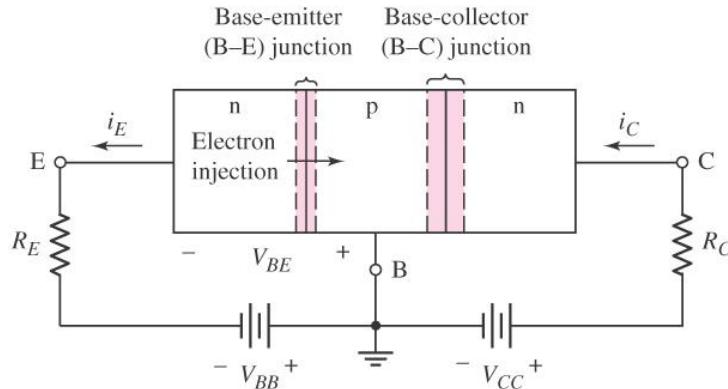


Variable	Meaning
i_B, v_{BE}	Total instantaneous values
I_B, V_{BE}	DC values
i_b, v_{be}	Instantaneous ac values
I_b, V_{be}	Phasor values

- A lowercase letter with an uppercase subscript, such as i_B or v_{BE} , indicates *total instantaneous values*.
- An uppercase letter with an uppercase subscript, such as I_B or V_{BE} , indicates *DC quantities*.
- A lowercase letter with a lowercase subscript, such as i_b or v_{be} , indicates *instantaneous values of ac signals*.

Basic BJT Operation

- the voltage between two terminals controls the current through the third terminal.



If BE junction is forward biased, the current through this junction to be an exponential function of BE voltage

$$i_E = I_{E0} \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_{E0} e^{V_{BE}/V_T}$$

I_{E0} ranges from 10^{-12} to 10^{-16} A; $V_T = kT/e$ is thermal voltage (about 26 mV). k is Boltzmann Constant, T room temperature in (K) and e electron charge.

Since the base is thin, the electrons get near B-C junction and are swept into the collector if $V_{CB} > 0$.

The collector current can be written as:

$$i_C = I_S e^{V_{BE}/V_T}$$

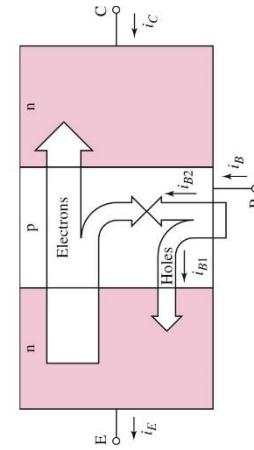
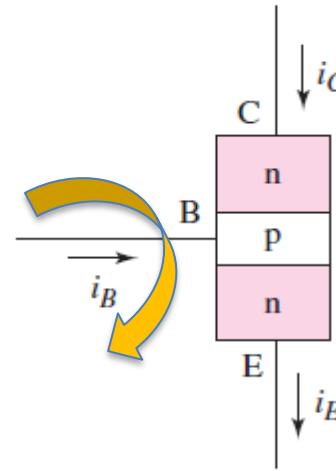
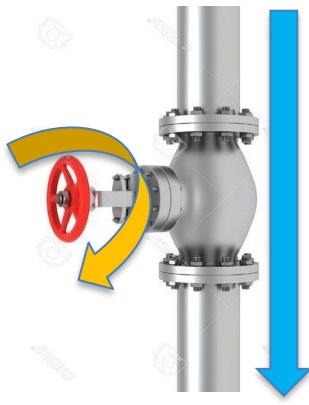
where $I_S = \alpha I_{E0}$ and α is slightly less than 1.

$$i_C = \beta i_B$$

β is the common-emitter current gain, which can be $50 < \beta < 200$

BJT Operation Modes

- Valve is closed
- Valve is open

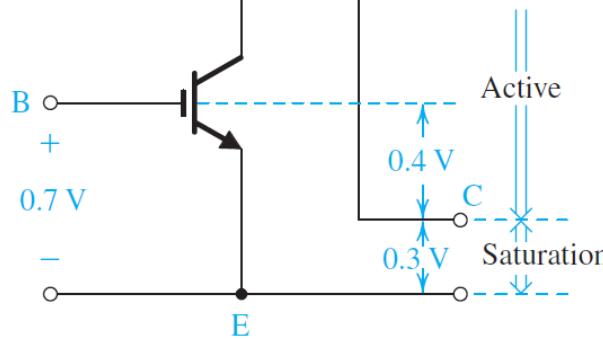


□ B-E junction turns on when $V_{BE} \geq 0.7 V$ (for Si) similar to a diode.

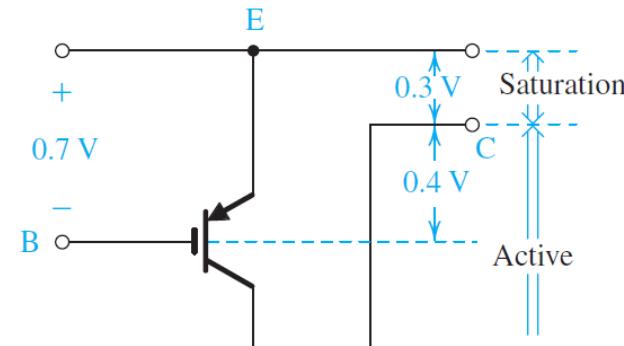
- $i_B = 0 \rightarrow i_c = 0 \rightarrow$ **cut-off** (Value is closed)
- $i_B > 0$
 - $i_c = \beta i_B \rightarrow$ **active mode** (valve is partially opened) controlled current source
 - $i_c < \beta i_B \rightarrow$ **saturation mode** (valve is fully opened) increasing i_B does not change i_c . It will depend on the external circuit.

BJT Operation: Active and Saturation Modes

For $i_c > 0$ we expect that $v_{CB} \geq 0$. But, the PN junction does not effectively become forward biased until the voltage exceeds approximately 0.2-0.3 V.



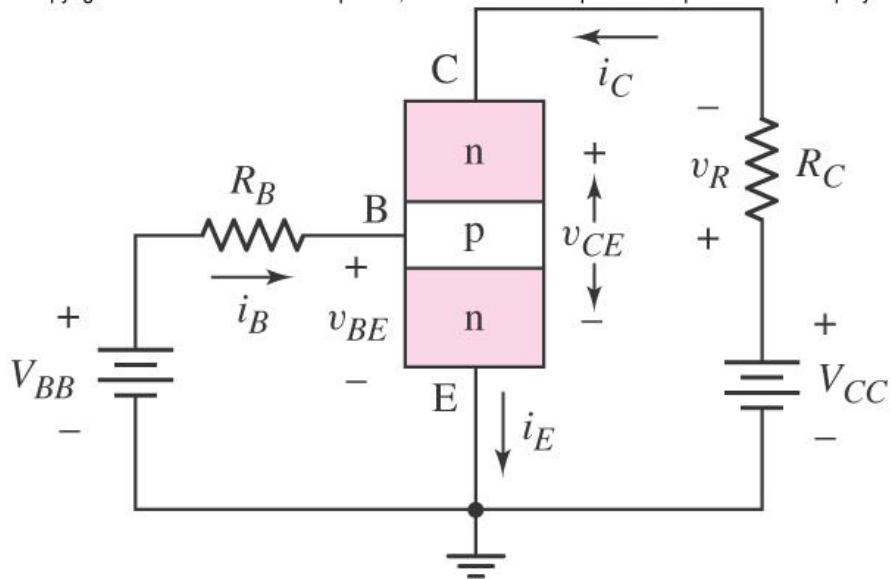
(a) *npn*



(b) *pnp*

active-mode operation of an *npn* transistor is still possible for $v_{CB} \approx -0.2/-0.3$ V.

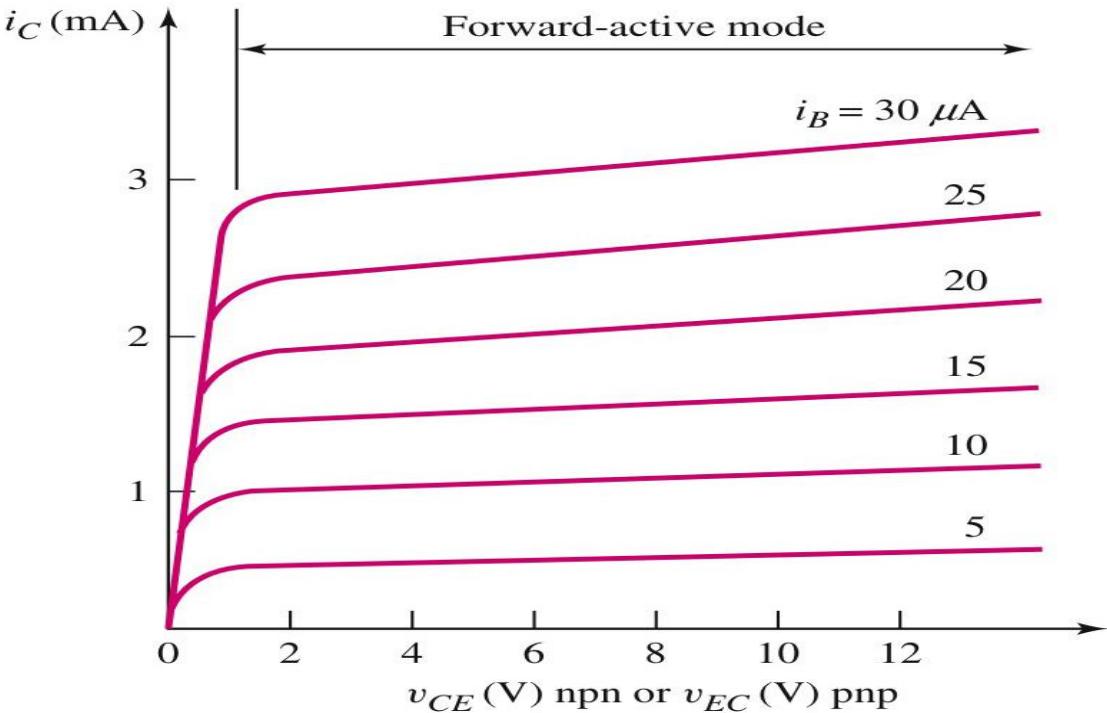
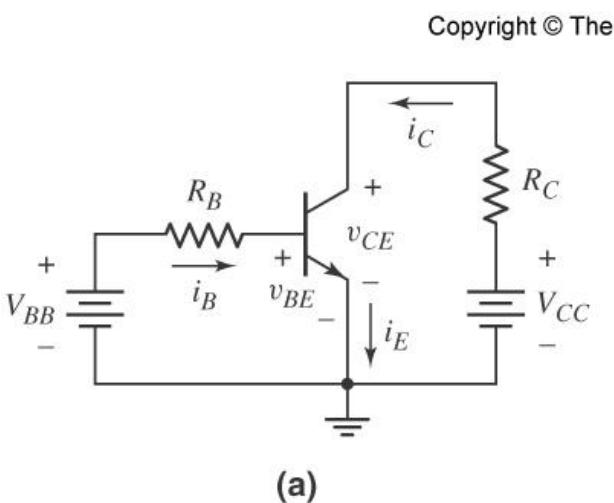
BJT Circuit Equations



$$i_E = i_C + i_B \quad \text{Common-Emitter current gain}$$
$$i_C = \beta i_B \quad (\text{beta})$$
$$i_E = (1 + \beta i_B)$$
$$i_C = \alpha i_E \quad \text{Common-base current gain}$$
$$\alpha = \frac{\beta}{1 + \beta}$$

- ❑ β is a function of i_C and temperature. However, we will generally treat it as a constant, a useful approximation to simplify things and still get a good insight.
- ❑ β is typically 100-250, but can be as high as 2000.

Current-Voltage Characteristics



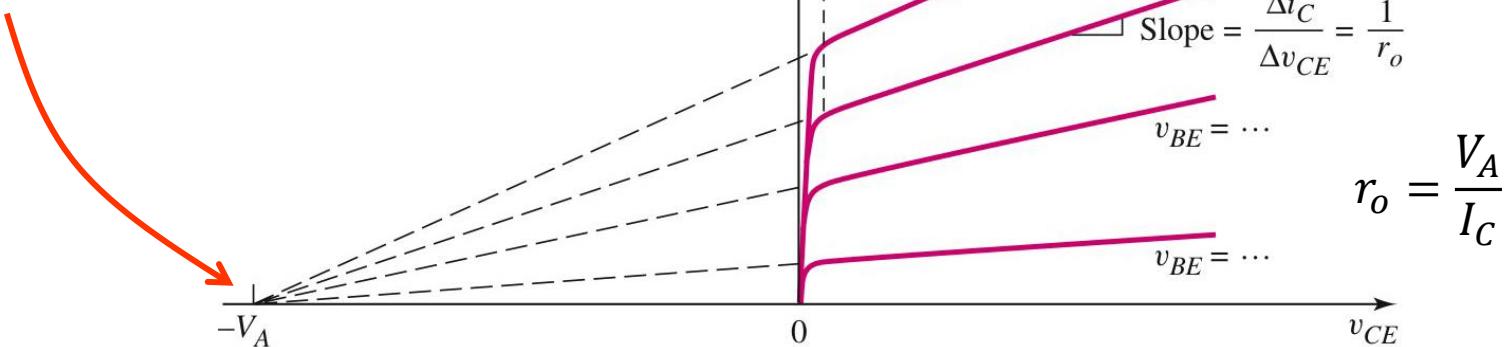
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Early Effect

- In Forward active region, I_C is not constant as V_{CE} increases. due to an effect called base-width modulation that was first analyzed by J. M. Early.

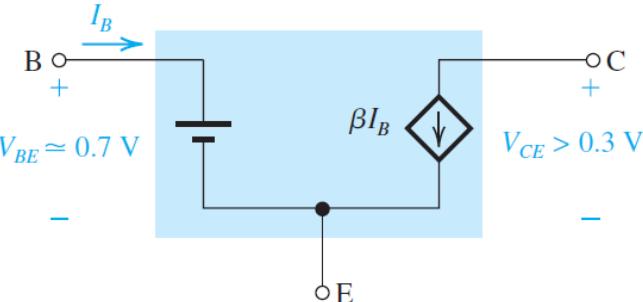
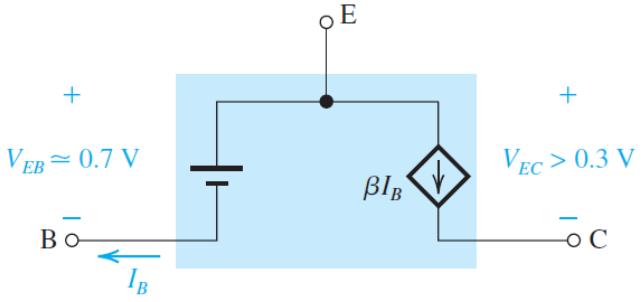
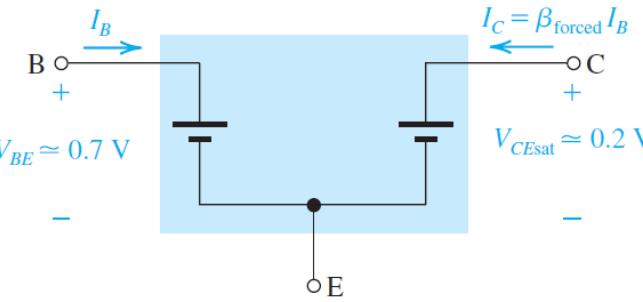
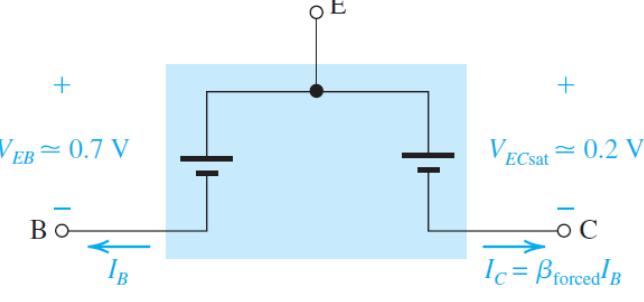
Lines of i_C vs v_{CE} for different i_B (or v_{BE}) coincide at $-V_A$ (the Early voltage). Usually it is $50 < V_A < 300$

V.



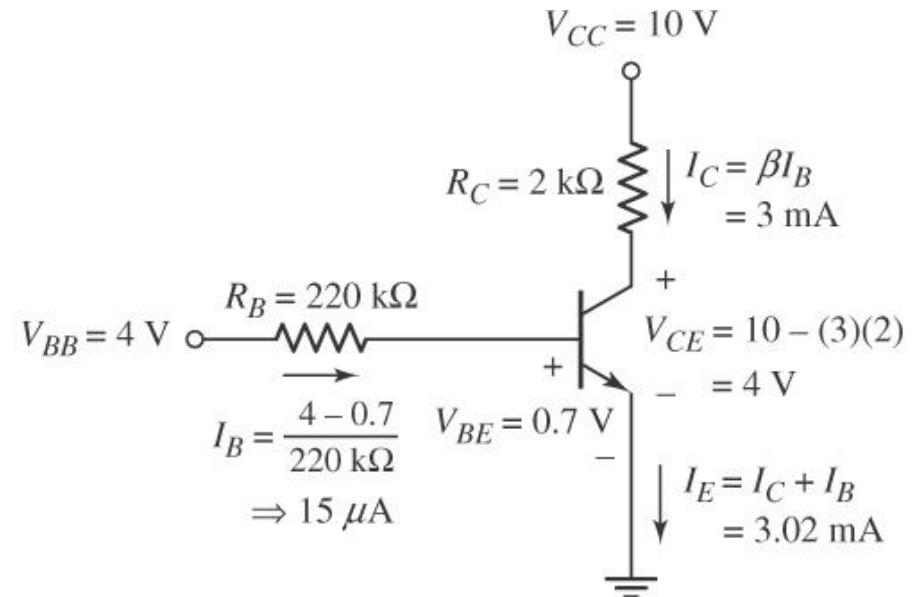
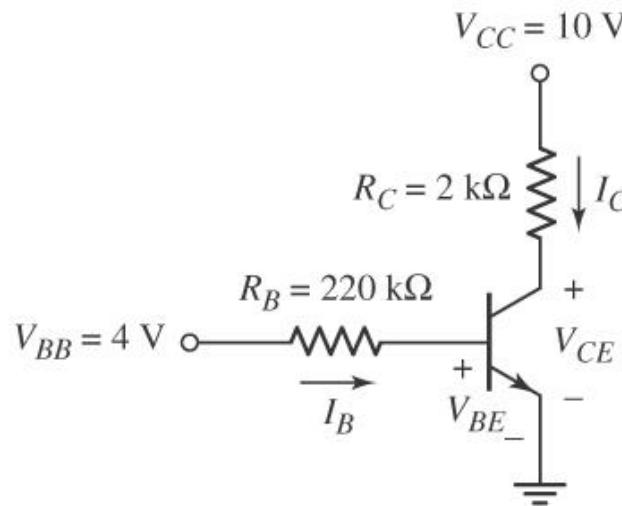
$$i_C = I_S(e^{v_{BE}/V_T}) \cdot \left(1 + \frac{v_{CE}}{V_A}\right)$$

BJT DC Circuit Model

	NPN	PNP
Active	 <p>$V_{BE} \approx 0.7 \text{ V}$</p> <p>$V_{CE} > 0.3 \text{ V}$</p>	 <p>$V_{EB} \approx 0.7 \text{ V}$</p> <p>$V_{EC} > 0.3 \text{ V}$</p>
Saturation	 <p>$I_C = \beta_{\text{forced}} I_B$</p> <p>$V_{BE} \approx 0.7 \text{ V}$</p> <p>$V_{C_{\text{Esat}}} \approx 0.2 \text{ V}$</p>	 <p>$I_C = \beta_{\text{forced}} I_B$</p> <p>$V_{EB} \approx 0.7 \text{ V}$</p> <p>$V_{E_{\text{Csat}}} \approx 0.2 \text{ V}$</p>

Eg.

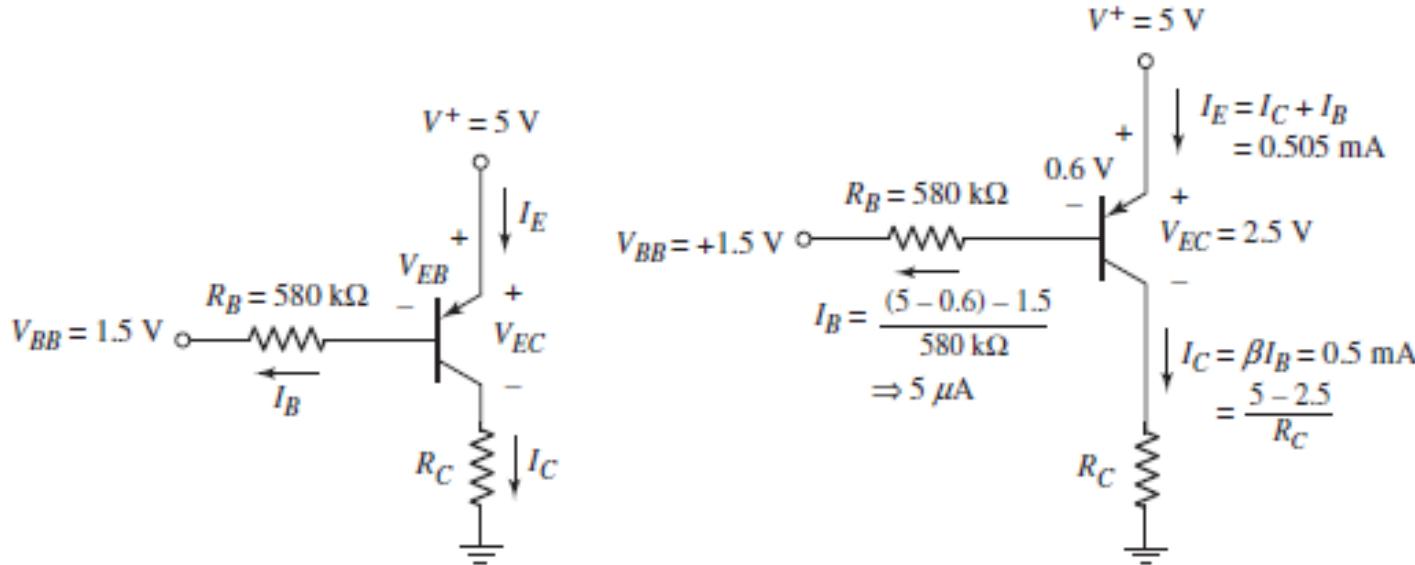
- Calculate the base, collector, and emitter currents and the C-E voltage for a common-emitter circuit. Calculate the transistor power dissipation.



$$P_T = I_B V_{BE}(\text{on}) + I_C V_{CE} = (0.015)(0.7) + (3)(4) \cong I_C V_{CE}$$

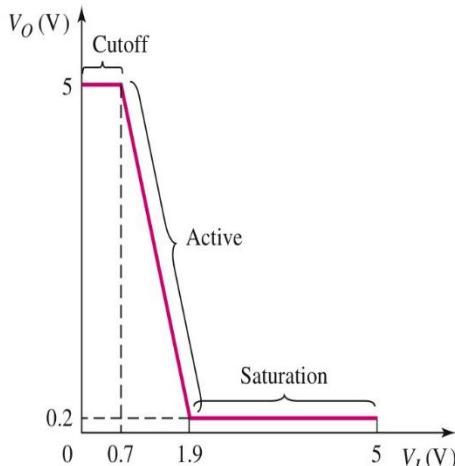
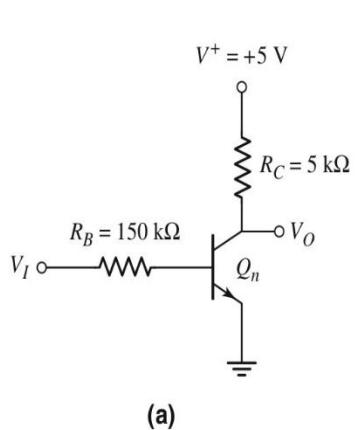
Objective: Analyze the common-emitter circuit with a pnp transistor.

For the circuit shown in Figure 5.22(a), the parameters are: $V_{BB} = 1.5$ V, $R_B = 580$ k Ω , $V^+ = 5$ V, $V_{EB}(\text{on}) = 0.6$ V, and $\beta = 100$. Find I_B , I_C , I_E , and R_C such that $V_{EC} = \left(\frac{1}{2}\right)V^+$.



BJT Voltage Transfer Characteristics

- A plot of the output voltage versus input voltage to visualize the operation of a circuit or the state of a transistor.



Solution (npn Transistor Circuit): For $V_I \leq 0.7$ V, the transistor Q_n is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = V^+ = 5$ V.

For $V_I > 0.7$ V, the transistor Q_n turns on and is initially biased in the forward-active mode. We have

$$I_B = \frac{V_I - 0.7}{R_B}$$

and

$$I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

Then

$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7) R_C}{R_B}$$

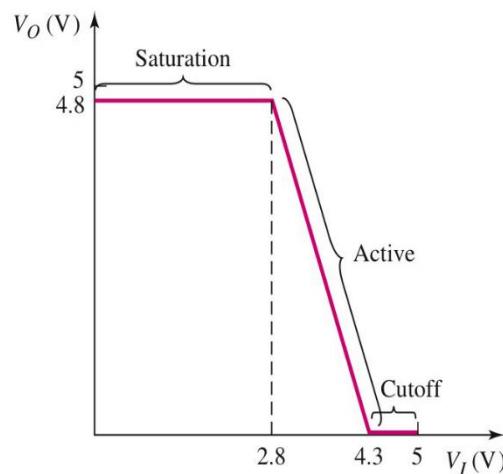
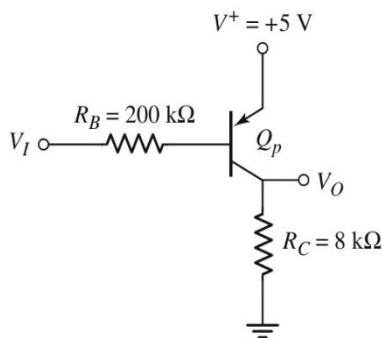
This equation is valid for $0.2 \leq V_O \leq 5$ V. When $V_O = 0.2$ V, the transistor Q_n goes into saturation. When $V_O = 0.2$ V, the input voltage is found from

$$0.2 = 5 - \frac{(120)(V_I - 0.7)(5)}{150}$$

which yields $V_I = 1.9$ V. For $V_I \geq 1.9$ V, the transistor Q_n remains biased in the saturation region.

Carry out simulations to draw this curve!

BJT Voltage Transfer Characteristics (PNP)



Solution (pnp transistor circuit): For $4.3 \leq V_I \leq 5 \text{ V}$, the transistor Q_p is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = 0$.

For $V_I < 4.3 \text{ V}$, the transistor Q_p turns on and is biased in the forward-active mode. We have

$$I_B = \frac{(5 - 0.7) - V_I}{R_B}$$

and

$$I_C = \beta I_B = \beta \left[\frac{(5 - 0.7) - V_I}{R_B} \right]$$

The output voltage is then

$$V_O = I_C R_C = \beta R_C \left[\frac{(5 - 0.7) - V_I}{R_B} \right]$$

This equation is valid for $0 \leq V_O \leq 4.8 \text{ V}$. When $V_O = 4.8 \text{ V}$, the transistor Q_p goes into saturation.

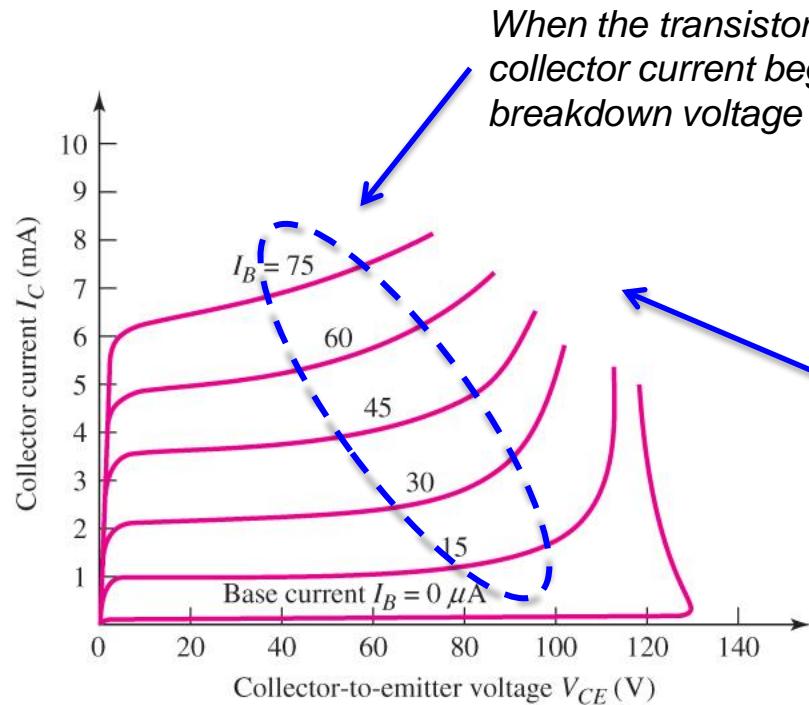
When $V_O = 4.8 \text{ V}$, the input voltage is found from

$$4.8 = (80)(8) \left[\frac{(5 - 0.7) - V_I}{200} \right]$$

which yields $V_I = 2.8 \text{ V}$. For $V_I \leq 2.8 \text{ V}$, the transistor Q_p remains biased in the saturation mode.

BJT Maximum Voltage limit

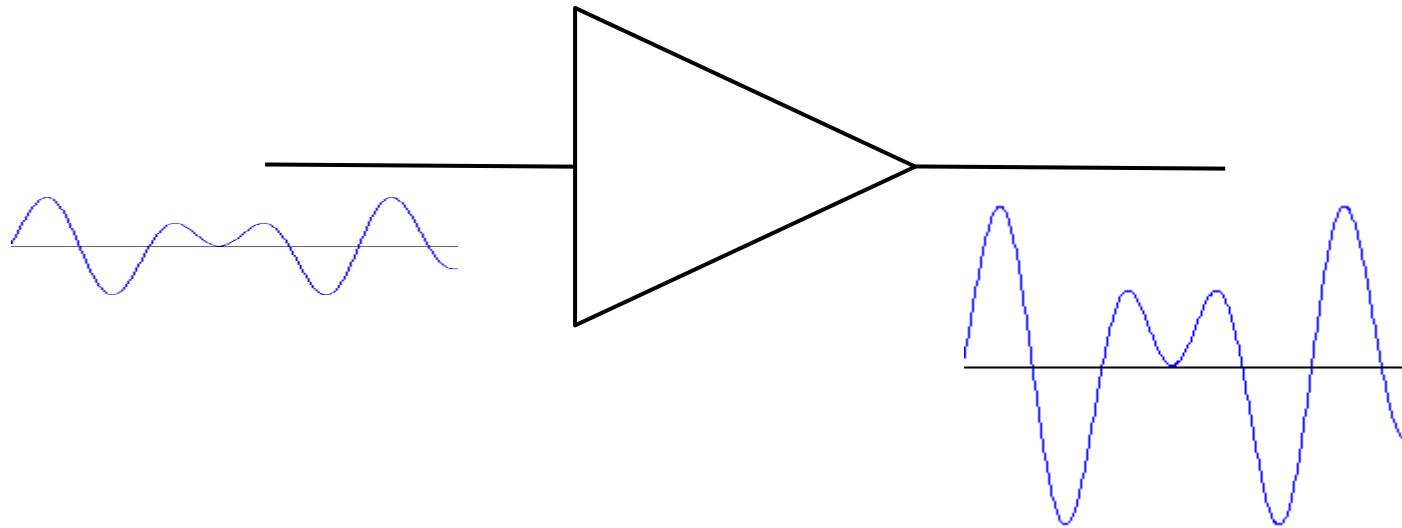
- generally associated with avalanche breakdown in the reverse-biased base–collector junction



When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CEO} is reached

all the curves tend to merge to the same V_{CE} voltage once breakdown has occurred.
The voltage at which these curves merge is denoted $V_{CE}(\text{sus})$ and is the minimum voltage necessary to sustain the transistor in breakdown.

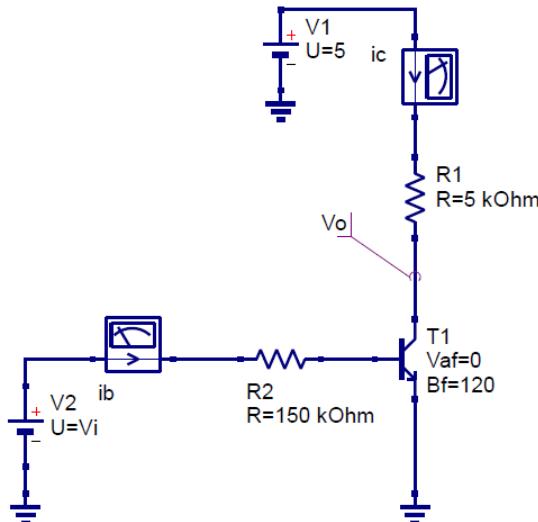
What is an Amplifier?



BJT as an Amplifier

□ Two observations:

1. $I_C = I_S e^{V_{BE}/V_T} \rightarrow$ collector current is independent of v_{CE}
2. A smaller change in i_B produces a larger i_C

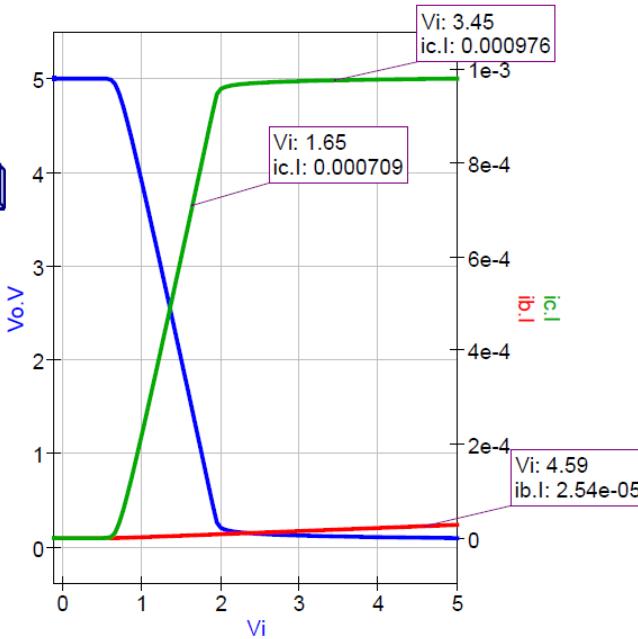


dc simulation

DC1

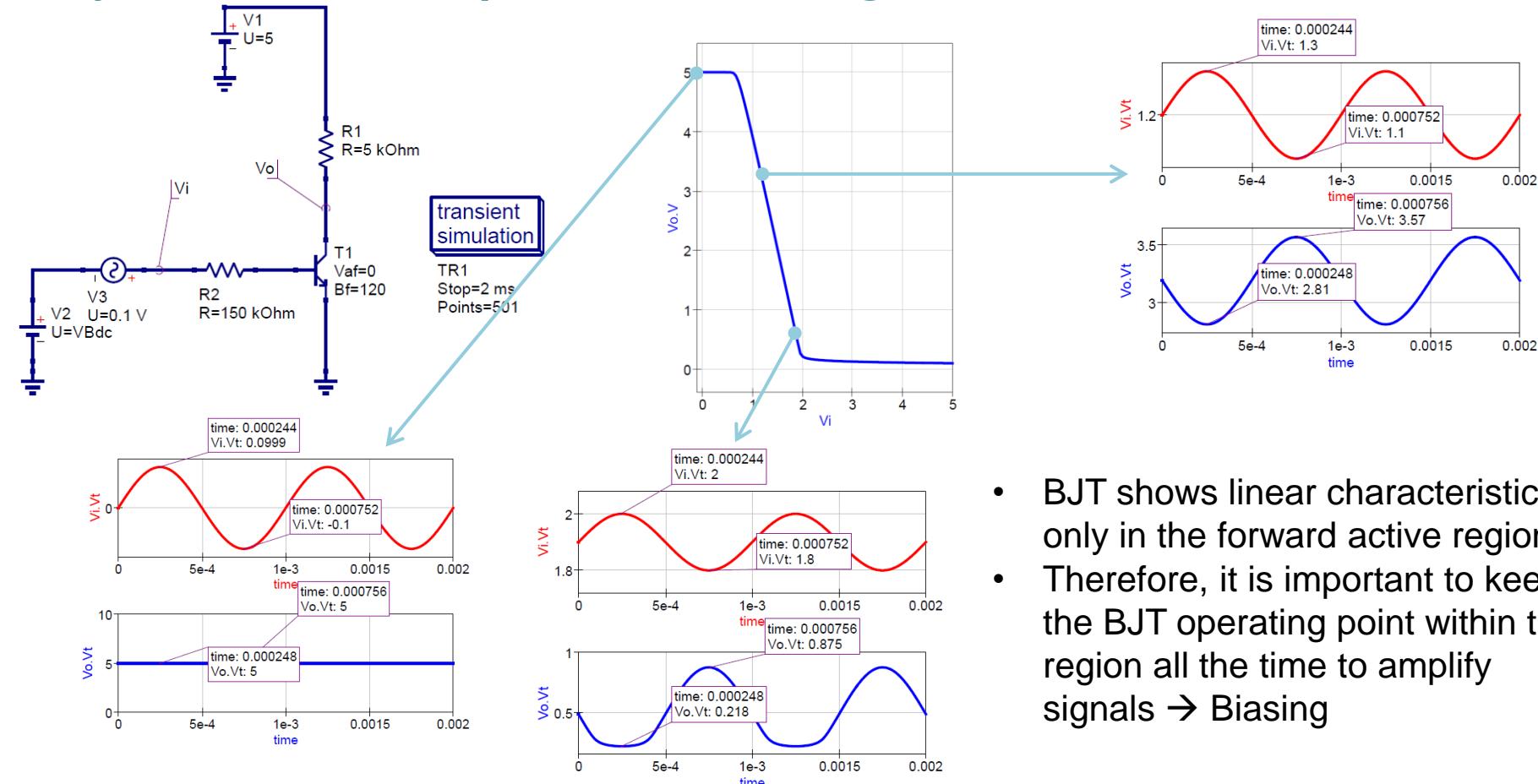
Parameter
sweep

SW1
Sim=DC1
Param=Vi
Type=lin
Start=-0.1
Stop=5
Points=100



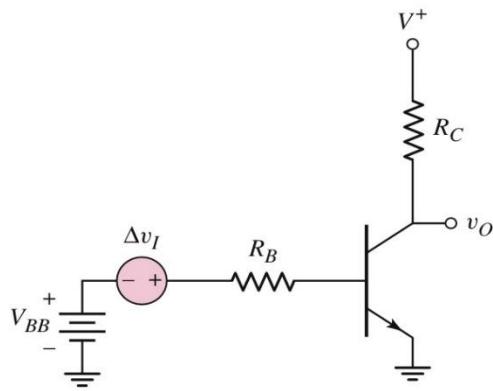
Common Emitter Configuration

BJT Linear Amplification Region

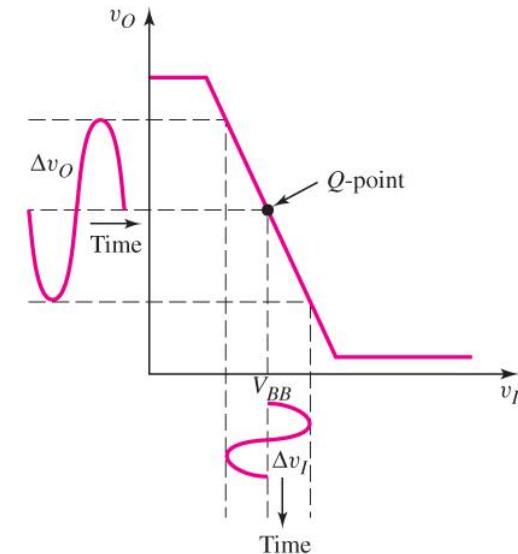
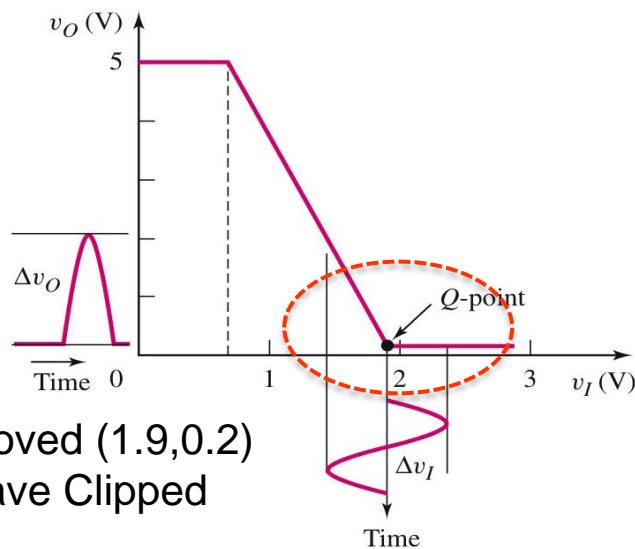


- BJT shows linear characteristics only in the forward active region.
- Therefore, it is important to keep the BJT operating point within that region all the time to amplify signals → Biasing

Idea of Biasing and Quiescent (Q) point



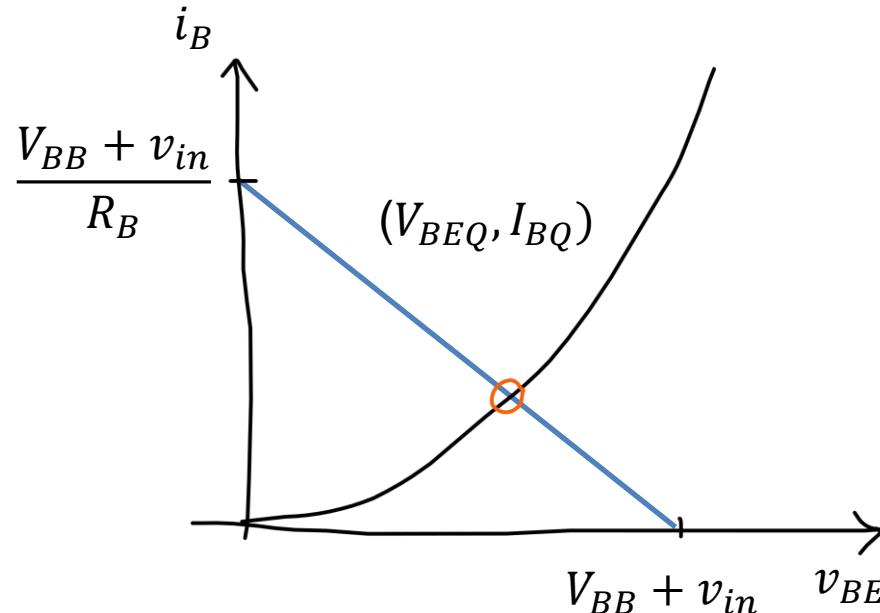
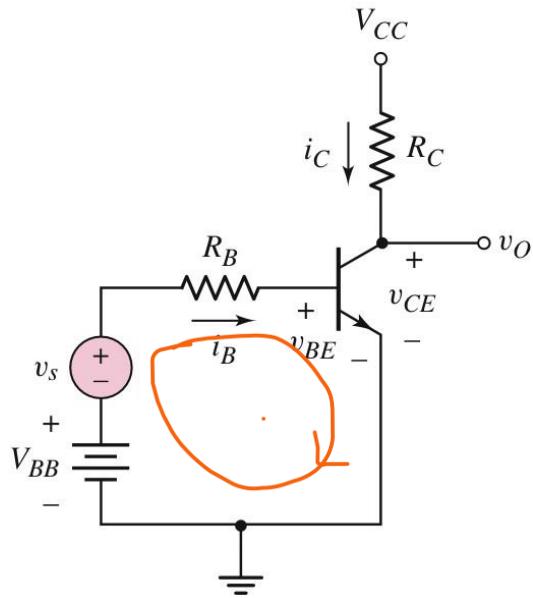
Q-point Moved (1.9,0.2)
Output Wave Clipped



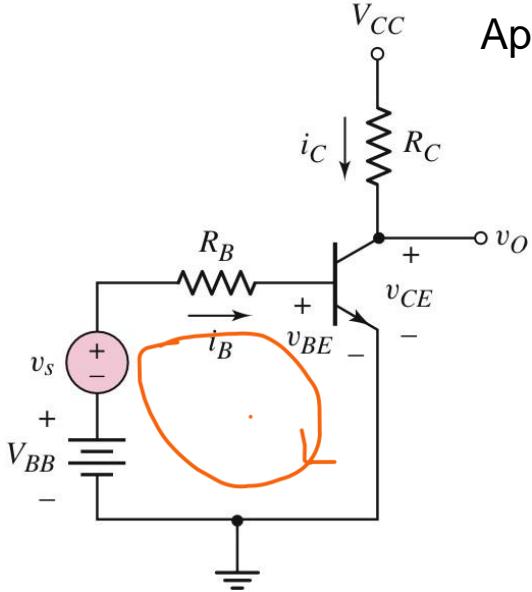
Input Q-point and the Load Line

Applying KVL for the input: $V_{BB} + v_{in} = R_B i_B + v_{BE}$

$$i_B = \frac{V_{BB} + v_{in}}{R_B} - \frac{1}{R_B} v_{BE}$$

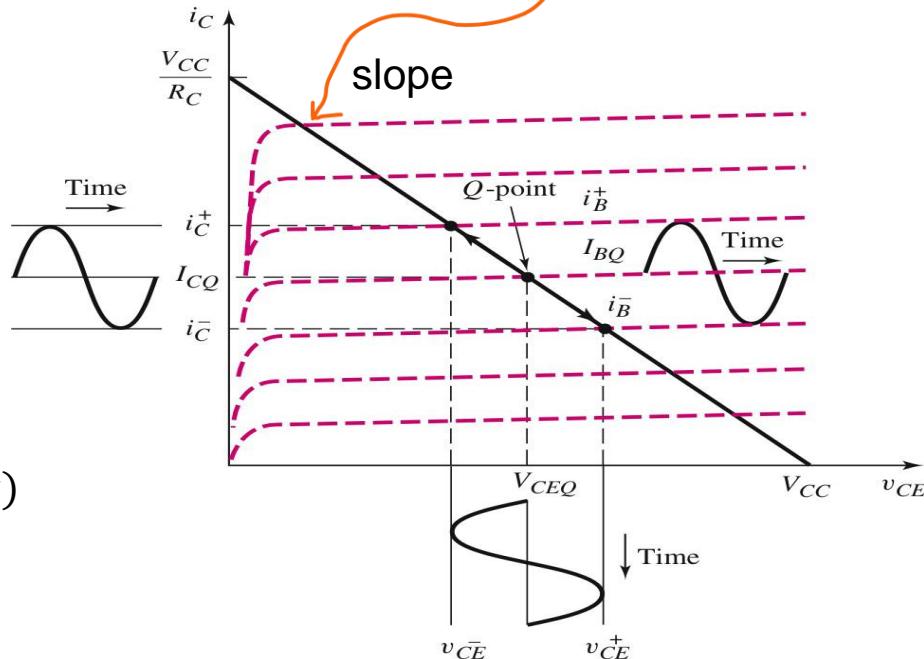


Output Q-point and the Load Line



Applying KVL to the output circuit: $V_{CC} = R_C i_C(t) + v_{CE}(t)$

$$i_C(t) = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}(t)$$

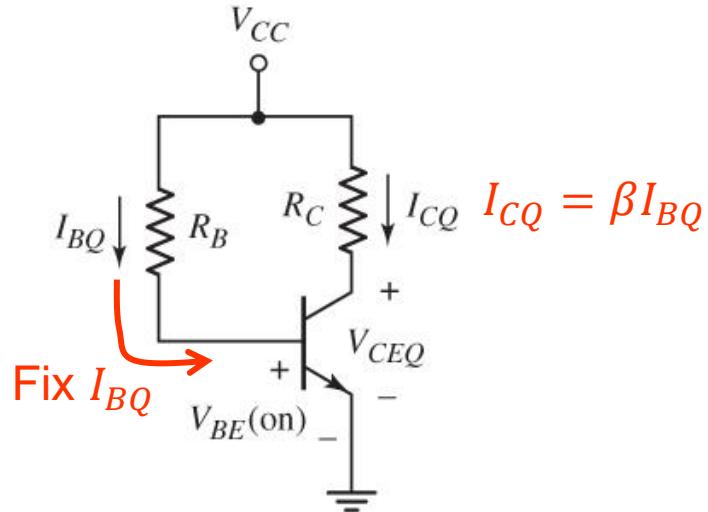
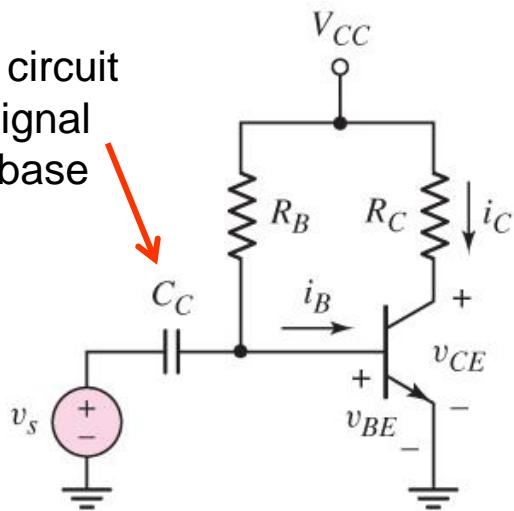


Applying KVL for the input:

$$V_{BB} + v_{in}(t) = R_B i_B(t) + v_{BE}(t)$$

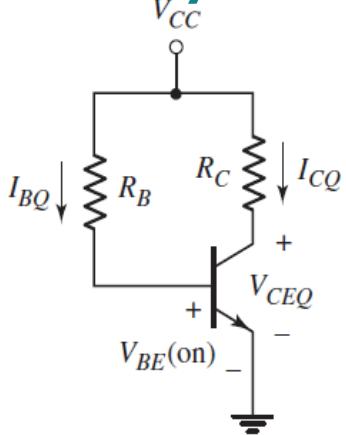
Biasing Method I/3: Single Base Resistor Biasing

C_C acts as an open circuit to DC isolates the signal source from the dc base current.



- ❑ But β varies with temperature. It also changes with device to device
- ❑ V_{BE} decreases by about 2 mV/ $^{\circ}\text{C}$. This increases I_C , which heats up the transistor, which further decreases V_{BE} , , which increases I_C even more ...

Analysis of Single Base Resistor Biasing



Objective: Design a circuit with a single-base resistor to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.51(b). The circuit is to be biased with $V_{CC} = +12$ V. The transistor quiescent values are to be $I_{CQ} = 1$ mA and $V_{CEQ} = 6$ V.

Choices: The transistor used in the design has nominal values of $\beta = 100$ and $V_{BE(on)} = 0.7$ V, but the current gain for this type of transistor is assumed to be in the range $50 \leq \beta \leq 150$ because of fairly wide fabrication tolerances. We will assume, in this example, that the designed resistor values are available.

Solution: The collector resistor is found from

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{1} = 6 \text{ k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1 \text{ mA}}{100} \Rightarrow 10 \mu\text{A}$$

and the base resistor is determined to be

$$R_B = \frac{V_{CC} - V_{BE(\text{on})}}{I_{BQ}} = \frac{12 - 0.7}{10 \mu\text{A}} = 1.13 \text{ M}\Omega$$

The transistor characteristics, load line, and Q -point for this set of conditions are shown in Figure 5.52(a).

Trade-offs: In this example, we will assume that the resistor values are fixed and will investigate the effects of the variation in transistor current gain β .

The base current is given by

$$I_{BQ} = \frac{V_{CC} - V_{BE(\text{on})}}{R_B} = \frac{12 - 0.7}{1.13 \text{ M}\Omega} = 10 \mu\text{A} \text{ (unchanged)}$$

The base current for this circuit configuration is independent of the transistor current gain.

The collector current is

$$I_C = \beta I_{BQ}$$

and the load line is found from

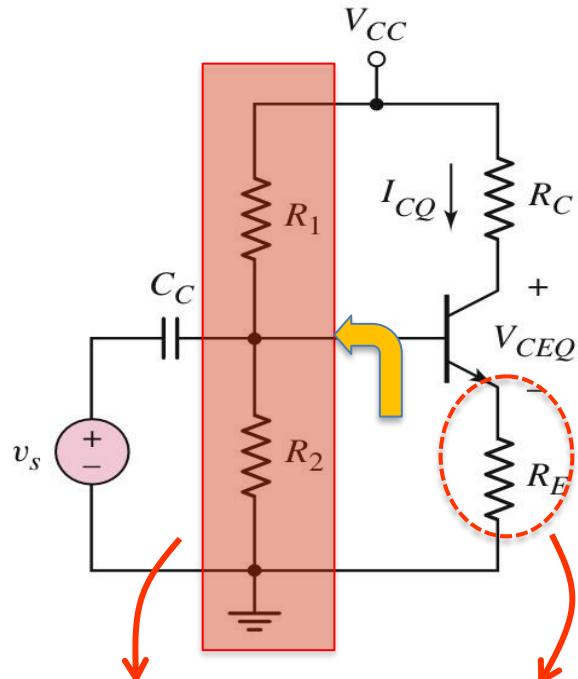
$$V_{CE} = V_{CC} - I_C R_C = 12 - I_C(6)$$

The load line is fixed. However, the Q -point will change. The transistor Q -point values for three values of β are given as:

β	50	100	150
Q -point values	$I_{CQ} = 0.50 \text{ mA}$ $V_{CEQ} = 9 \text{ V}$	$I_{CQ} = 1 \text{ mA}$ $V_{CEQ} = 6 \text{ V}$	$I_{CQ} = 1.5 \text{ mA}$ $V_{CEQ} = 3 \text{ V}$

the Q-point is not stabilized
against variations in β

Biasing Method 2/3: Voltage Divider Biasing

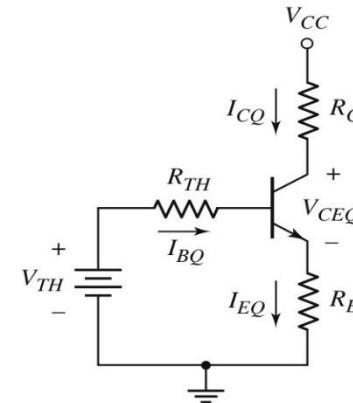


Provides a bias voltage

Stabilizes Q-point against variations in β , temperature, . . .

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TH} = V_{CC} \frac{R_2}{R_1 + R_2}$$



Applying Kirchhoff's law around the B-E loop, we obtain

$$V_{TH} = I_B Q R_{TH} + V_{BE(\text{on})} + I_E Q R_E$$

If the transistor is biased in the forward-active mode, then

$$I_E Q = (1 + \beta) I_B Q$$

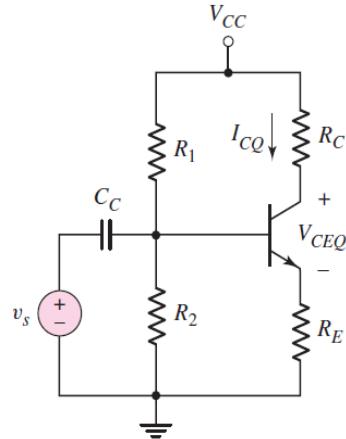
and the base current, from Equation (5.37), is

$$I_B Q = \frac{V_{TH} - V_{BE(\text{on})}}{R_{TH} + (1 + \beta) R_E}$$

The collector current is then

$$I_C Q = \beta I_B Q = \frac{\beta (V_{TH} - V_{BE(\text{on})})}{R_{TH} + (1 + \beta) R_E}$$

Analysis of Voltage-Divider Bias Circuit

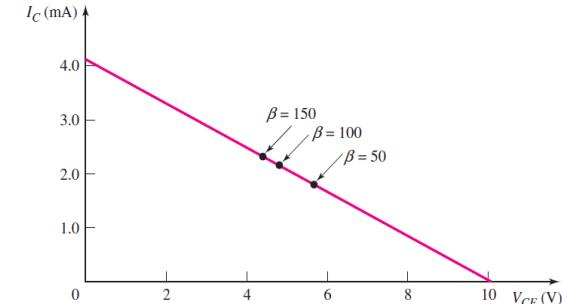


Objective: Analyze a circuit using a voltage divider bias circuit, and determine the change in the Q -point with a variation in β when the circuit contains an emitter resistor.

For the circuit given in Figure 5.54(a), let $R_1 = 56 \text{ k}\Omega$, $R_2 = 12.2 \text{ k}\Omega$, $R_C = 2 \text{ k}\Omega$, $R_E = 0.4 \text{ k}\Omega$, $V_{CC} = 10 \text{ V}$, $V_{BE(\text{on})} = 0.7 \text{ V}$, and $\beta = 100$.

If the current gain of the transistor were to decrease to $\beta = 50$ or increase to $\beta = 150$, we obtain the following results:

β	50	100	150
Q -point values	$I_{BQ} = 35.9 \mu\text{A}$ $I_{CQ} = 1.80 \text{ mA}$ $V_{CEQ} = 5.67 \text{ V}$	$I_{BQ} = 21.6 \mu\text{A}$ $I_{CQ} = 2.16 \text{ mA}$ $V_{CEQ} = 4.81 \text{ V}$	$I_{BQ} = 15.5 \mu\text{A}$ $I_{CQ} = 2.32 \text{ mA}$ $V_{CEQ} = 4.40 \text{ V}$



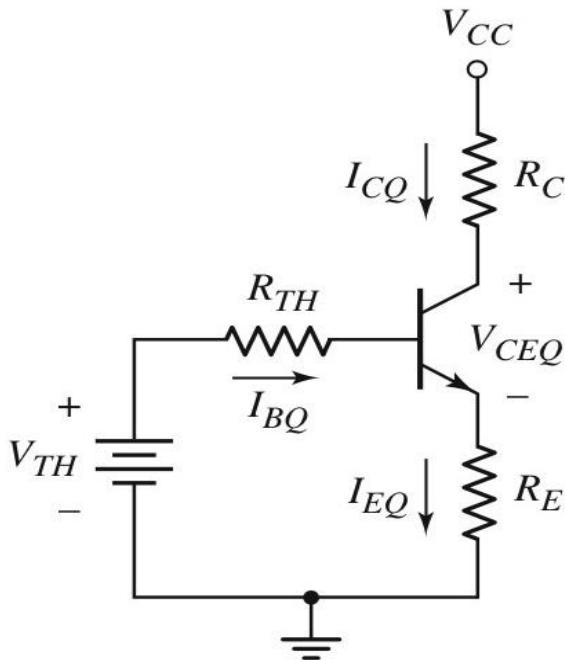
- ❑ Voltage divider circuit uses resistor values in the low kilohm range. Single resistor biasing requires a resistor in the megohm range.
- ❑ The change in I_{CQ} , V_{CEQ} with a change in β has been substantially reduced.
- ❑ R_E has tended to **stabilize** the Q -point with respect to variations in β . Including the resistor R_E introduces negative feedback.

Design requirement for bias stability

- We know $I_{CQ} = \frac{\beta(V_{TH} - V_{BE(on)})}{R_{TH} + (1 + \beta)R_E}$ → I_{CQ} is proportional to β .
- Make $R_{TH} \ll (1 + \beta)R_E$. That will make $I_{CQ} = \frac{\beta(V_{TH} - V_{BE(on)})}{(1 + \beta)R_E} = \underbrace{\frac{\beta}{1 + \beta}}_{\approx 1} \frac{(V_{TH} - V_{BE(on)})}{R_E}$
- Since $\beta \gg 1$, $\frac{\beta}{1 + \beta} \approx 1$.
- Now, $I_{CQ} = \frac{(V_{TH} - V_{BE(on)})}{R_E}$, which is independent of beta.
- General rule: a circuit is considered bias-stable when $R_{TH} \cong 0.1 (1 + \beta)R_E$

Voltage Divider Bias: Design Objective

- How to make Q-point insensitive to PVT variations?

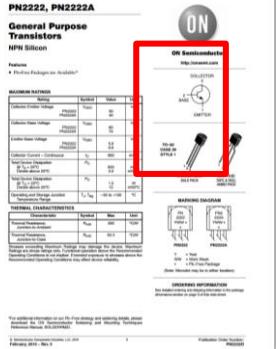


$$I_{EQ} = \frac{V_{TH} - V_{BE} - R_{TH}I_B}{R_E}$$

$\propto V_{CC}$ $\propto \text{Temp}$ $\propto \beta$

- For IE to be less sensitive to IB (thus β)
 - $R_{TH}I_B \ll V_{TH} - V_{BE}$
 - Large currents through R1 and R2 (10x)
- For IE to be less sensitive to VBE (due to temperature change) $V_{TH} \gg V_{BE}$

BJT Datasheet

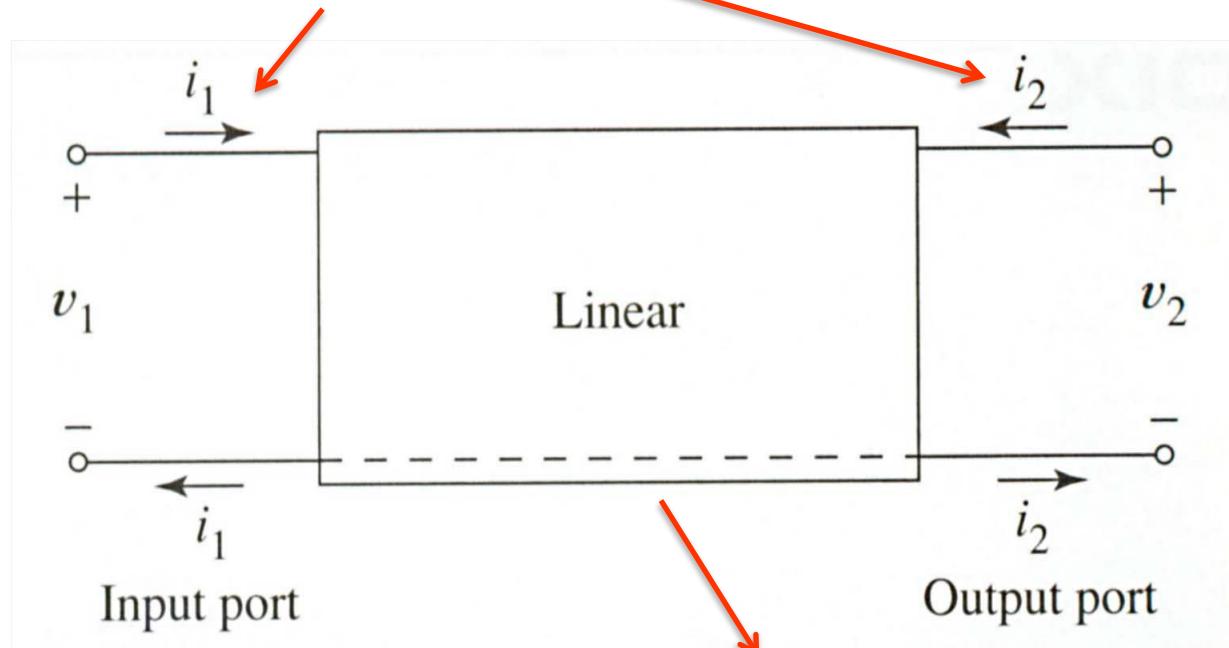


V _{CEO}	Collector emitter voltage with base open circuit
V _{CBO}	Collector base voltage with the emitter open circuit
V _{EBO}	Emitter base voltage with collector open circuit
I _C	Collector current
I _{CM}	Peak collector current
I _{BM}	Peak base current
P _{TOT}	Total power dissipation - this is normally for an ambient temperature of 25C. It is the maximum value of power that can safely be dissipated for that transistor with its stated package.
T _j	Junction temperature
T _{amb}	Ambient temperature
T _{stg}	Storage temperature.
I _{CBO}	Collector base cut-off current
I _{EBO}	Emitter base cut-off current
h _{FE}	Forward current gain
V _{CEsat}	Collector emitter saturation voltage
V _{BEsat}	Base emitter saturation voltage
C _c	Collector capacitance
C _e	Emitter capacitance
F _t	Frequency Transition

3. BJT Small Signal Model

Two-Port Conventions

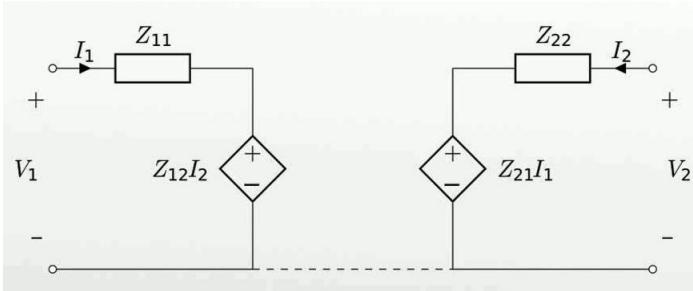
Note polarities of voltages and directions and currents



The broken line means points may be connected, but this is not a requirement for being a two-port.

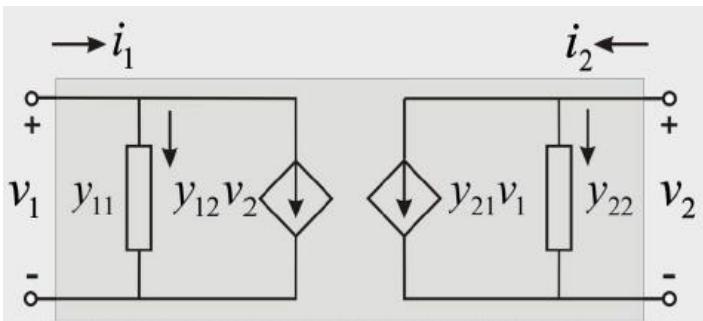
Z and Y Parameters

Both input variables are currents



$$Z_{11} = \frac{V_1}{I_1} \Big|_{I_2=0} \quad Z_{12} = \frac{V_1}{I_2} \Big|_{I_1=0}$$

$$Z_{21} = \frac{V_2}{I_1} \Big|_{I_2=0} \quad Z_{22} = \frac{V_2}{I_2} \Big|_{I_1=0}$$



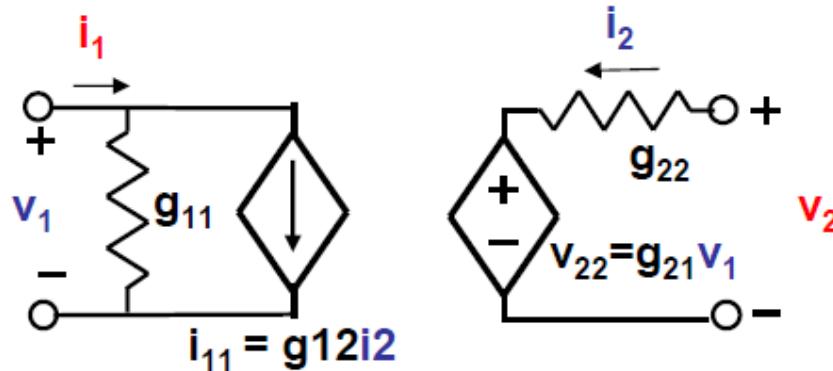
Both input variables are voltages

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

$$Y_{11} = \frac{I_1}{V_1} \Big|_{V_2=0} \quad Y_{12} = \frac{I_1}{V_2} \Big|_{V_1=0}$$
$$Y_{21} = \frac{I_2}{V_1} \Big|_{V_2=0} \quad Y_{22} = \frac{I_2}{V_2} \Big|_{V_1=0}$$

g-parameters

- To represent a voltage amplifier we require that a voltage driving port 1 results into a voltage developed on port 2.



$$\begin{aligned} i_1 &= g_{11}v_1 + i_{11} = g_{11}v_1 + g_{12}i_2 \\ v_2 &= v_{22} + g_{22}i_2 = g_{21}v_1 + g_{22}i_2 \end{aligned} \quad \Rightarrow$$

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} \Rightarrow \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \mathbf{G} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$$

Terminology:

g_{11} : Input admittance

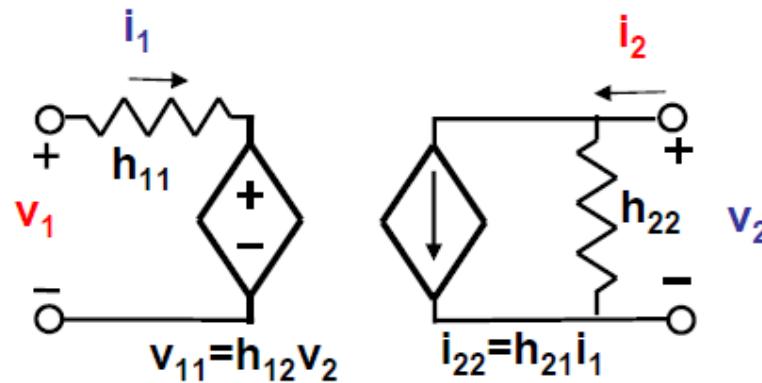
g_{12} : Reverse current gain

g_{21} : Voltage gain

g_{22} : Output impedance

h-parameters

- A current amplifier has current input at port 1 and current and output at port 2. The representation choice is the inverse of that of a voltage amplifier:



$$\left. \begin{aligned} v_1 &= h_{11} i_1 + v_{11} = h_{11} i_1 + h_{12} v_2 \\ i_2 &= i_{22} + h_{22} v_2 = h_{21} i_1 + h_{22} v_2 \end{aligned} \right\} \Rightarrow$$

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \mathbf{H} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$$

Terminology

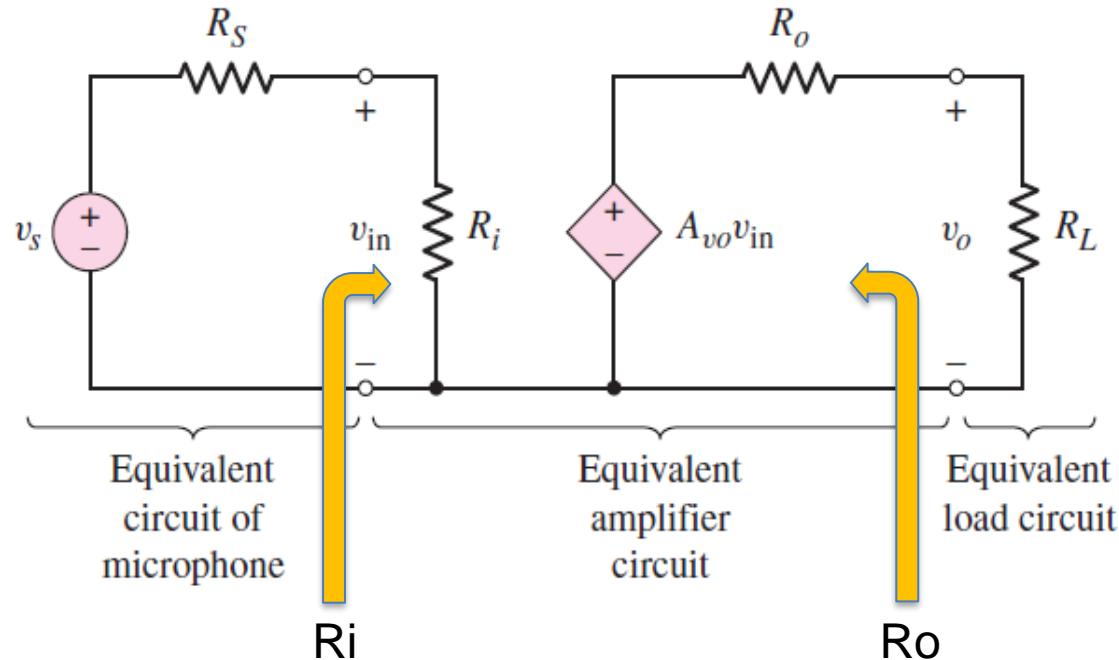
h_{11} : Input impedance

h_{12} : Reverse voltage gain

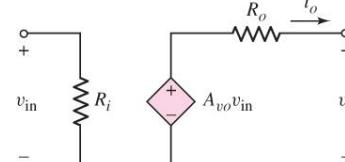
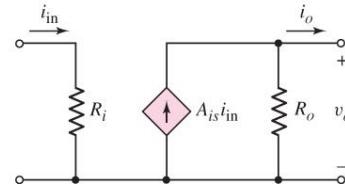
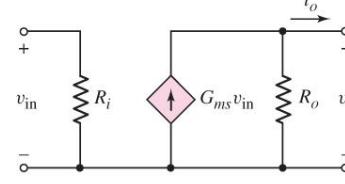
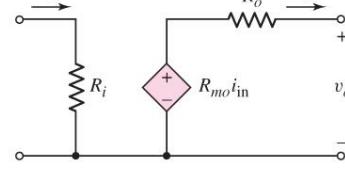
h_{21} : Current gain

h_{22} : Output admittance

Two Port Model of an Amplifier



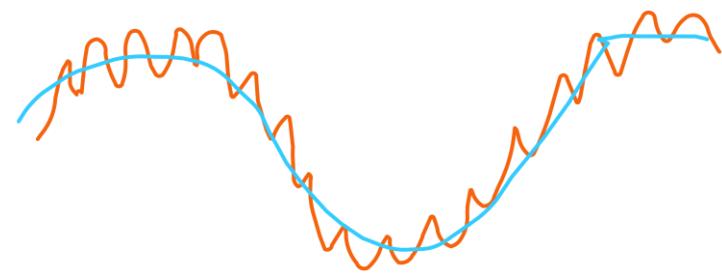
Types of Amplifiers

Type	Equivalent circuit	Gain property
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

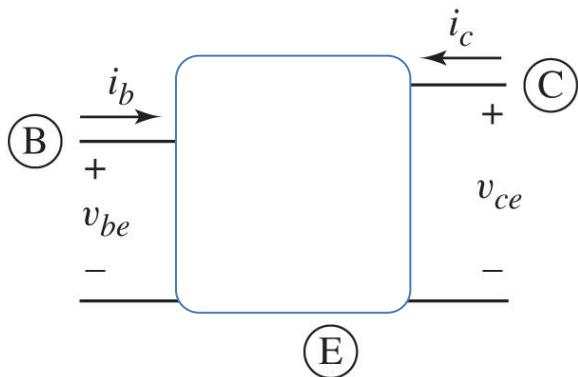
AC Equivalent Circuit

- From the concept of small signal (small amplitude, fast changing), all the time-varying signals will be linearly related and are superimposed on dc values.

Element	I-V relationship	DC model	AC model
Resistor	$I_R = \frac{V}{R}$	R	R
Capacitor	$I_C = sCV$	Open —○—○—	C
Inductor	$I_L = \frac{V}{sL}$	Short —○—○—	L
Diode	$I_D = I_S(e^{v_D/V_T} - 1)$	$+V_\gamma - r_f$	$r_d = V_T/I_D$ —~~~~~—
Independent voltage source	$V_S = \text{constant}$	$+V_S -$ — —	Short —○—○—
Independent current source	$I_S = \text{constant}$	I_S —→○—	Open —○—○—



BJT Small-Signal (Hybrid π) Model



$$V_{BE} = V_{BE} + \sigma_{be}$$

We know

$$i_c = I_s e^{(V_{BE} + \sigma_{be})/V_T}$$

$$= I_s e^{\sigma_{be}/V_T} e^{V_{BE}/V_T}$$

$$= I_c e^{\sigma_{be}/V_T}$$

If $\sigma_{be} \ll V_T$ (V_{be} in the range of 5mV-10mV)

$$i_c \approx I_c \left(1 + \frac{\sigma_{be}}{V_T} \right)$$

$$= I_c + \frac{I_c}{V_T} \sigma_{be}$$

\downarrow

DC component (i_c)

$$i_c = \frac{I_c}{V_T} \sigma_{be}$$

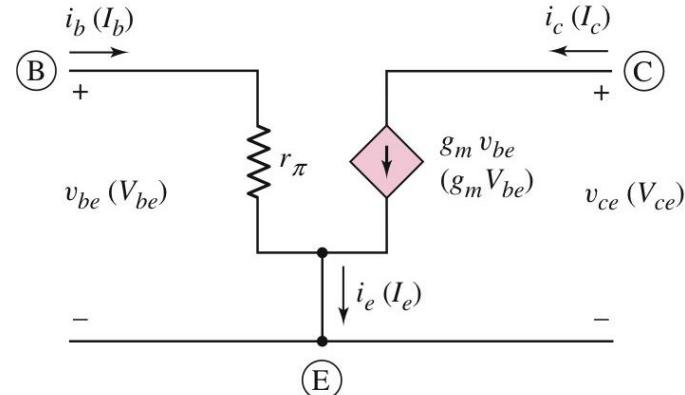
\downarrow

$g_m \rightarrow$ transconductance

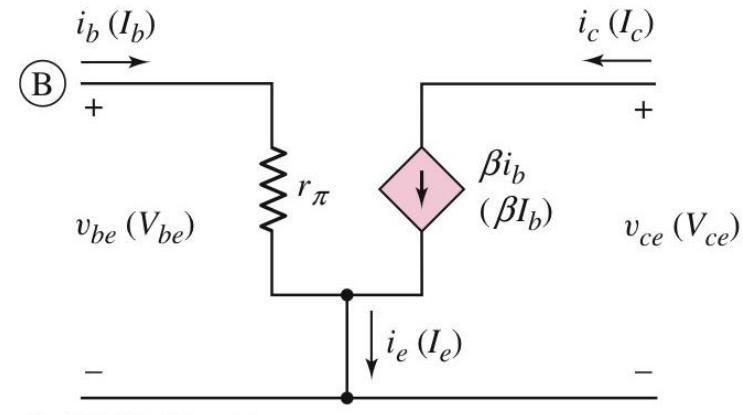
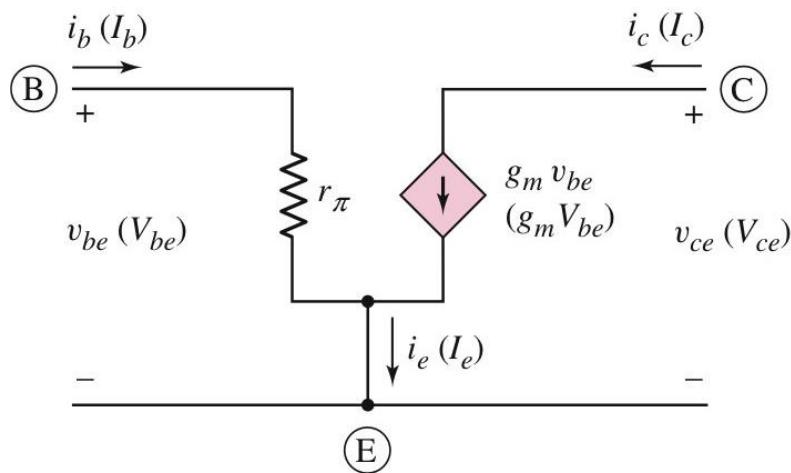
$$i_B = \frac{i_c}{\beta} = \underbrace{\frac{I_c}{\beta}}_{I_B} + \underbrace{\frac{1}{\beta} \frac{I_c}{V_T} \sigma_{be}}_{i_b}$$

$$i_b = g_m \sigma_{be} \Rightarrow \sigma_{be} = \frac{\beta}{g_m} i_b$$

r_π



BJT Small-Signal (Hybrid π) Model

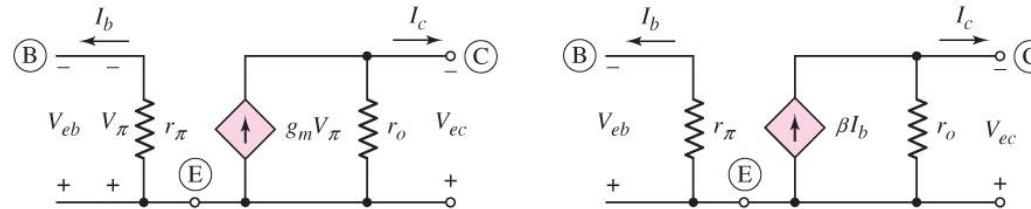
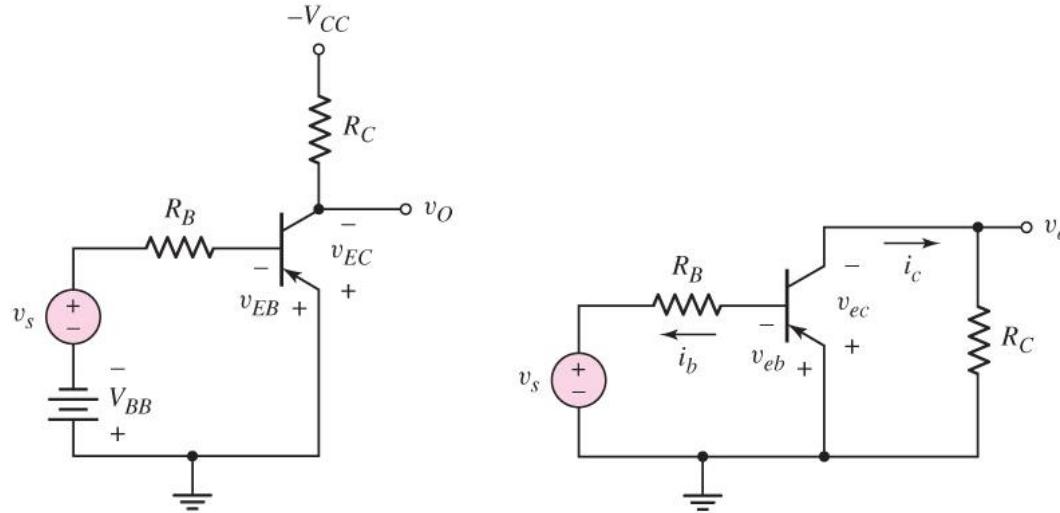


$$g_m = \frac{I_{CQ}}{V_T}; r_\pi = \frac{\beta V_T}{I_{CQ}}; g_m r_\pi = \beta$$

$V_T \sim 26 \text{ mV}$ at room temp.
 $gm \sim 40$ ICQ at room temp

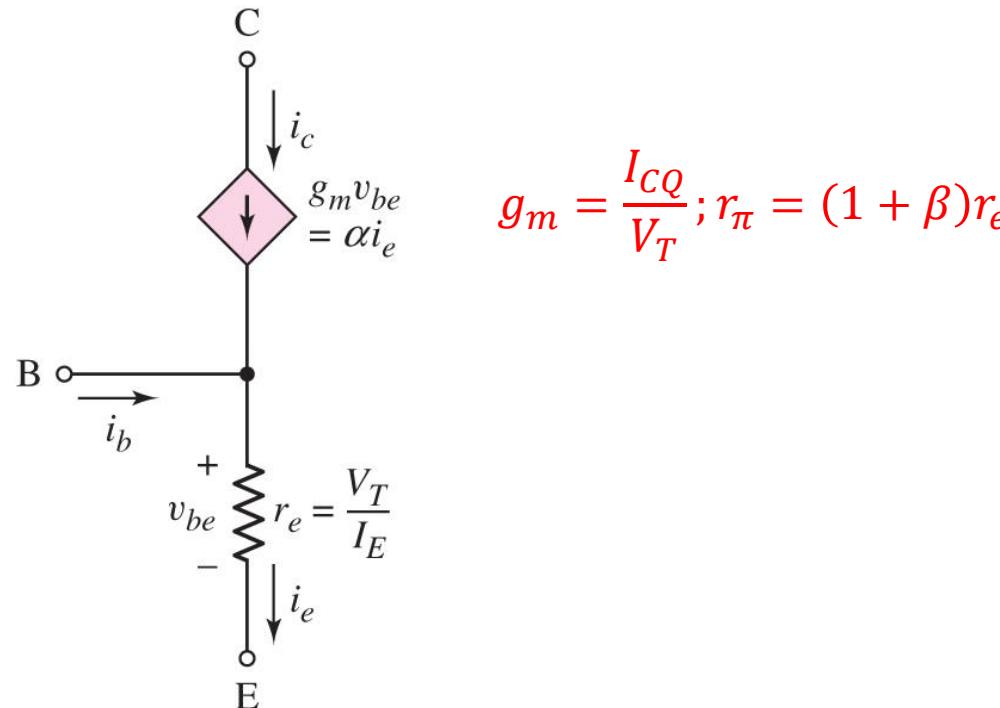
- This model is true only for $v_{be} \ll V_T$ (read 6.2.1 Neaman for more details). Usual rule of thumb is $v_{be} < 10 \text{ mV}$.

Small Signal Model (PNP)

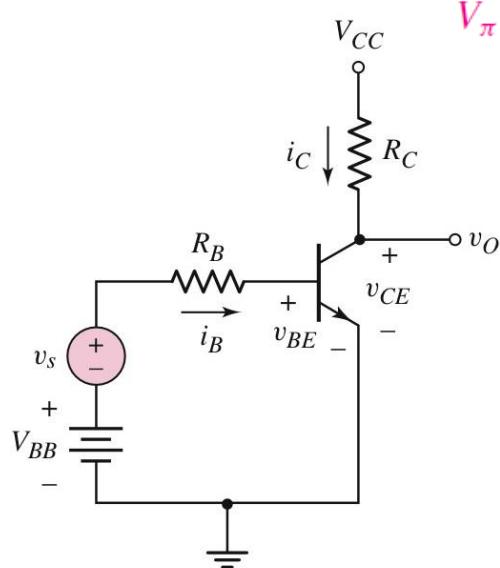


BJT T-Model

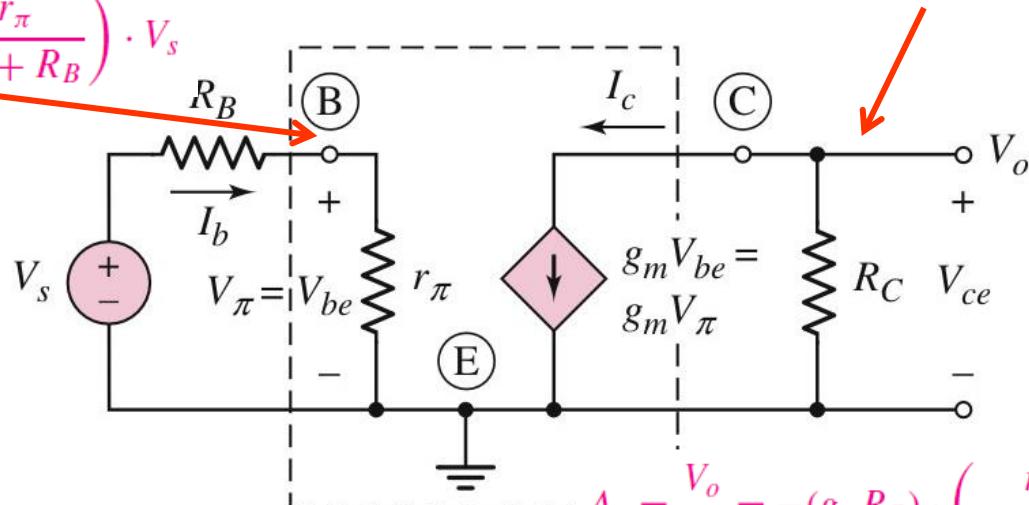
- there are situations in which an alternative model is much more convenient than hybrid pi model



Small-Signal Gain CE Amplifier



$$V_\pi = \left(\frac{r_\pi}{r_\pi + R_B} \right) \cdot V_s$$



$$V_o = V_{ce} = -(g_m V_\pi) R_C$$

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B} \right)$$

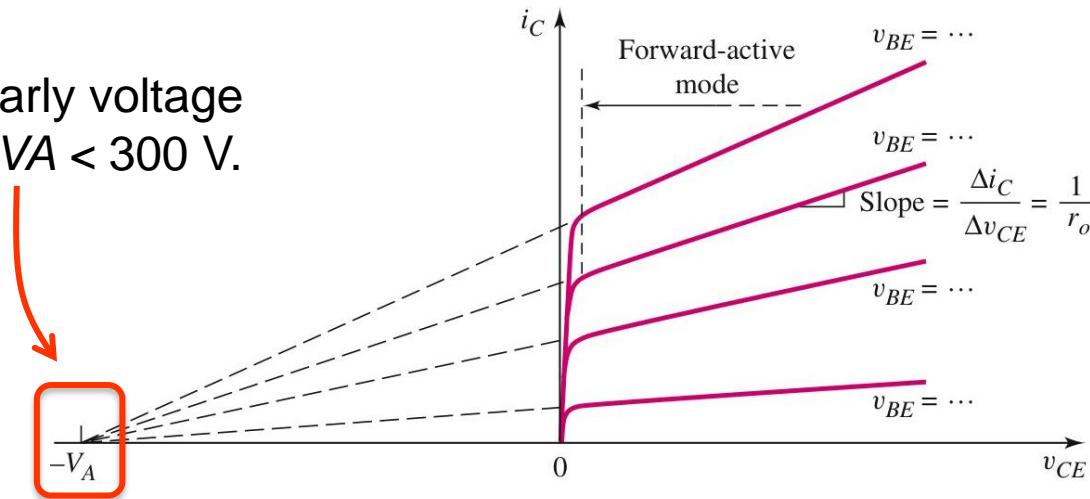
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□ Why A_v is negative?

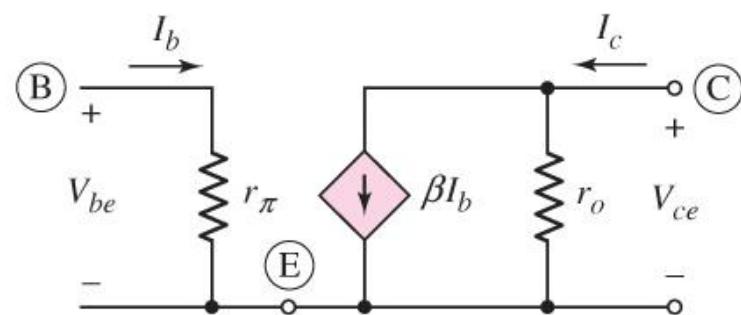
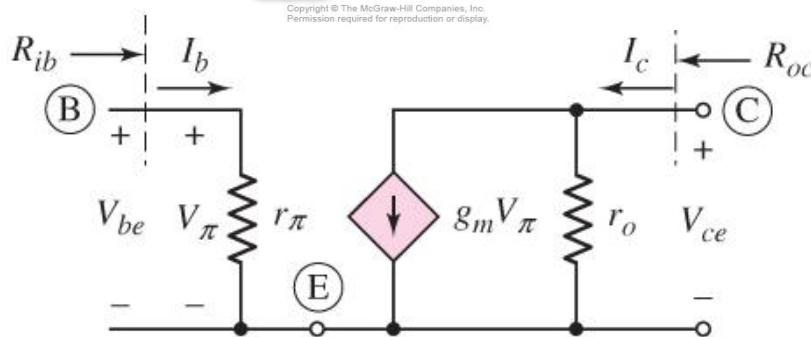
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Hybrid- π Model for NPN with Early Effect

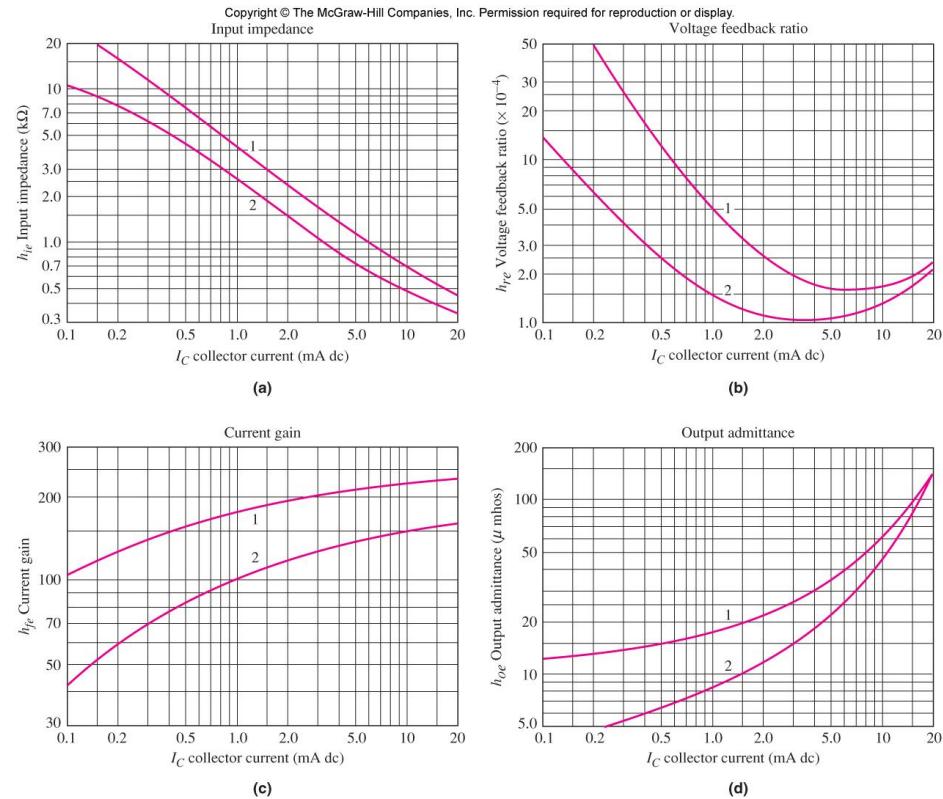
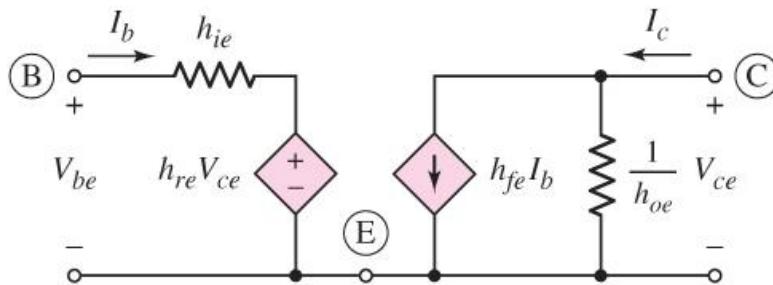
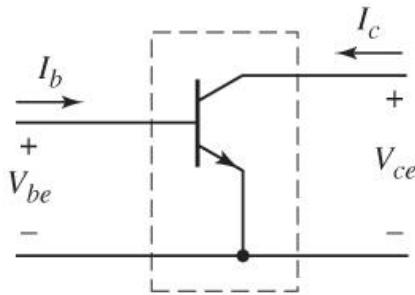
the Early voltage
 $50 < V_A < 300$ V.



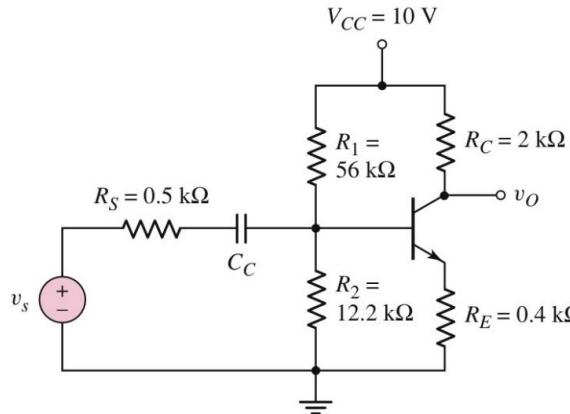
$$r_o = \frac{V_A}{I_C}$$



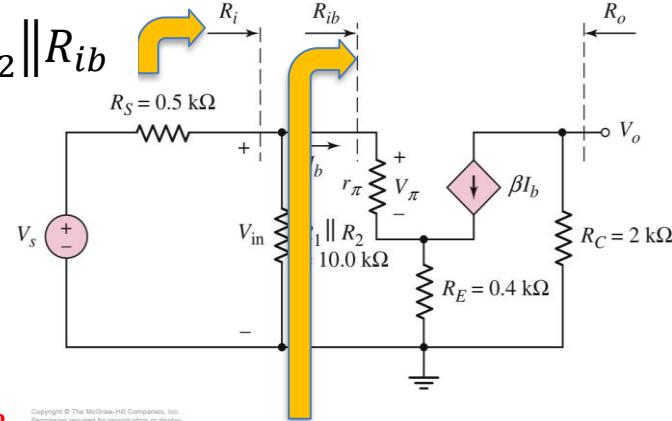
BJT h-parameters



Small Signal Gain with a Emitter Resistor



$$R_i = R_1 \parallel R_2 \parallel R_{ib}$$



$$A_v = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E} \left(\frac{R_i}{R_i + R_S} \right) \cong -\frac{R_C}{R_E} \left(\frac{R_i}{R_i + R_S} \right) \cong -\frac{R_C}{R_E}$$

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$$R_{ib} = r_\pi + (1 + \beta)R_E$$

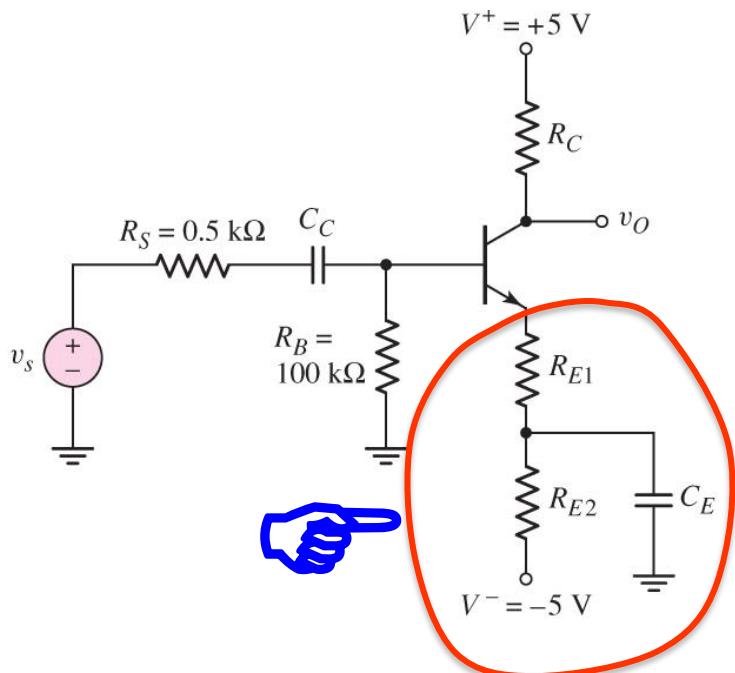
□ AC gain is less dependent of BJT parameters!

□ Having a R_E

- stabilizes the Q-point ($I_B \uparrow, I_C \uparrow, I_E \uparrow, V_{BE} \downarrow, I_B \downarrow$)
- but reduces the AC Gain substantially.

Circuit with Emitter Bypass Capacitor

- RE must be large dc design, but degrades the small-signal voltage gain too severely.



Use bypass capacitor to effectively short out a portion or all of the emitter resistance as seen by the ac signals.

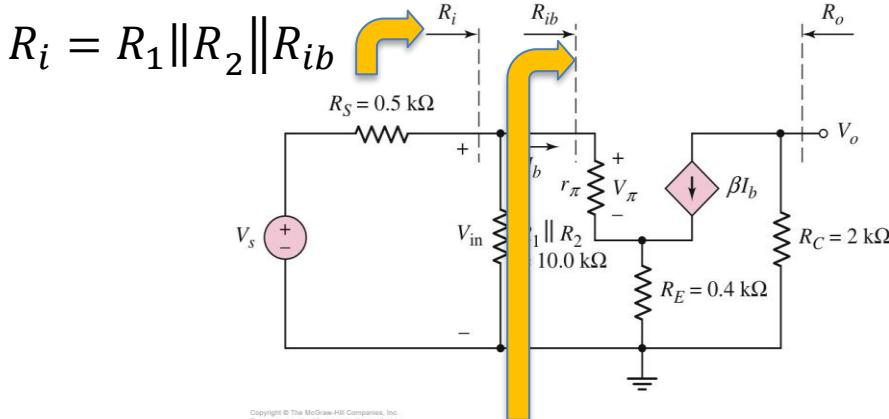
$$\text{For DC: } R_E = R_{E1} + R_{E2}$$

$$\text{For AC : } R_E = R_{E1}$$

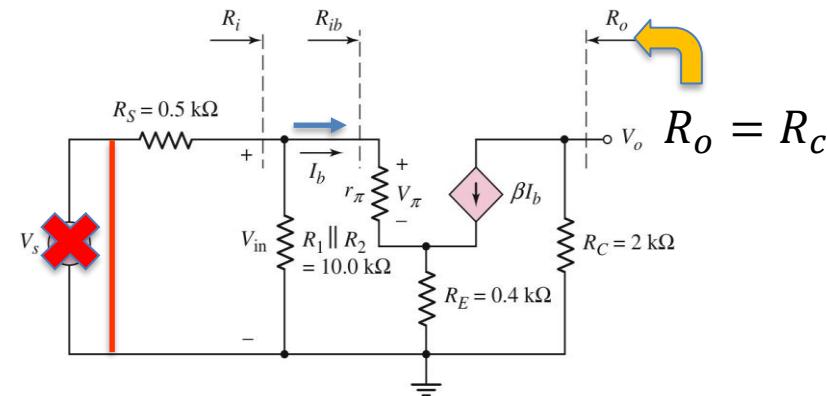
Small-Signal Performance Parameters

□ In AC analysis, we mainly look at the following parameters:

- Gain → Voltage (V_o/V_i) or Current (i_o/i_{in})
- Input resistance (R_i) → the total resistance looking into the amplifier
- Output resistance (R_o) → the total resistance looking into the output of the amplifier. To find R_o , the input source is set to zero (0) and a test source is applied at the output.
- Input Signal Range → small signal model is valid only for $v_{be} \ll V_T$ or $v_{be} < 10 \text{ mV}$

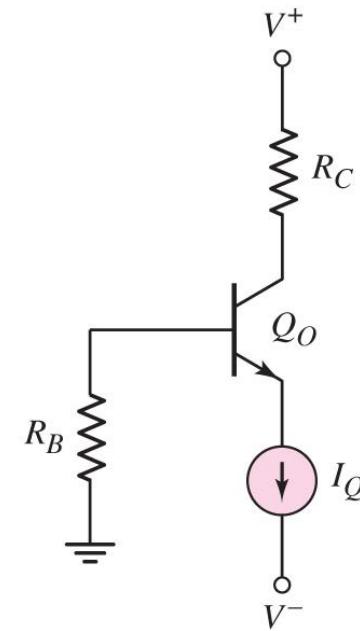


$$R_{ib} = r_\pi + (1 + \beta)R_E$$

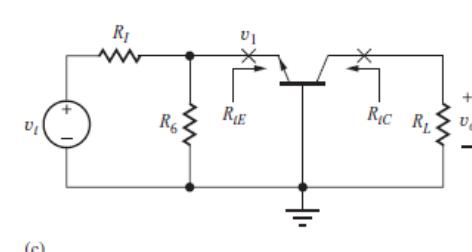
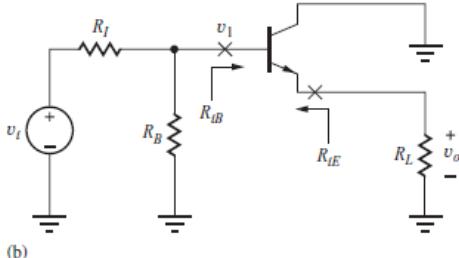
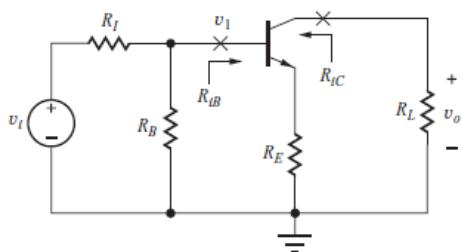


Biassing Method 3/3: Current Source Biassing

- For integrated circuits, resistors are expensive → they require a larger surface area than transistors.
- BJTs can be biassed with a current-source (I_Q)
 - I_E is independent of β
 - R_B , I_C and V_{CE} independent of transistor current gain, for
 - R_B can be increased, thus increasing the input resistance jeopardizing the bias stability.



BJT Amplifier Family



COMMON-EMITTER AMPLIFIER

$$\text{Terminal voltage gain } A_{vt} = \frac{v_o}{v_i} \cong -\frac{g_m R_L}{1 + g_m R_E}$$

Signal-source voltage gain

$$A_v = \frac{v_o}{v_i} = -\frac{g_m R_L}{1 + g_m R_E} \left[\frac{R_B \| R_{iB}}{R_I + (R_B \| R_{iB})} \right]$$

Input terminal resistance

$$r_\pi + (\beta_o + 1)R_E \\ \cong r_\pi (1 + g_m R_E)$$

Output terminal resistance

$$r_o(1 + g_m R_E)$$

Input signal range

$$\cong 0.005(1 + g_m R_E)$$

Terminal current gain

$$-\beta_o$$

COMMON-COLLECTOR AMPLIFIER

$$\cong +\frac{g_m R_L}{1 + g_m R_L} \cong +1$$

$$+ \frac{g_m R_L}{1 + g_m R_L} \left[\frac{R_B \| R_{iB}}{R_I + (R_B \| R_{iB})} \right] \cong +1$$

$$+ \frac{g_m R_L}{1 + g_m (R_I \| R_4)} \left(\frac{R_6}{R_I + R_6} \right)$$

$$r_\pi + (\beta_o + 1)R_L \\ \cong r_\pi (1 + g_m R_L)$$

$$\frac{\alpha_o}{g_m} \cong \frac{1}{g_m}$$

$$r_o [1 + g_m (R_I \| R_4)]$$

$$\frac{\alpha_o}{g_m} + \frac{R_{th}}{\beta_o + 1}$$

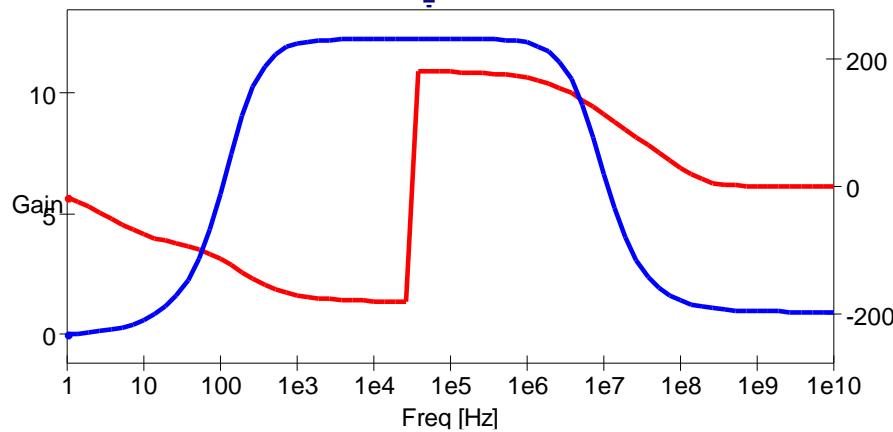
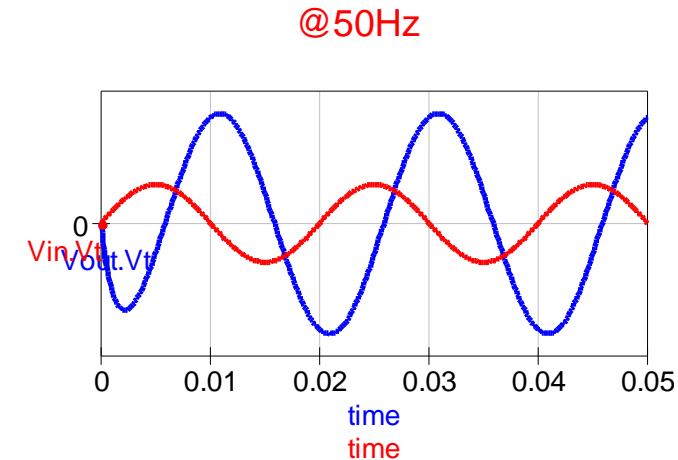
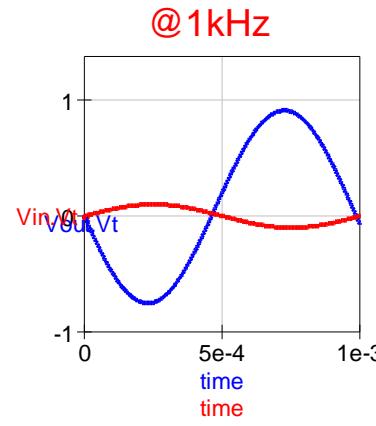
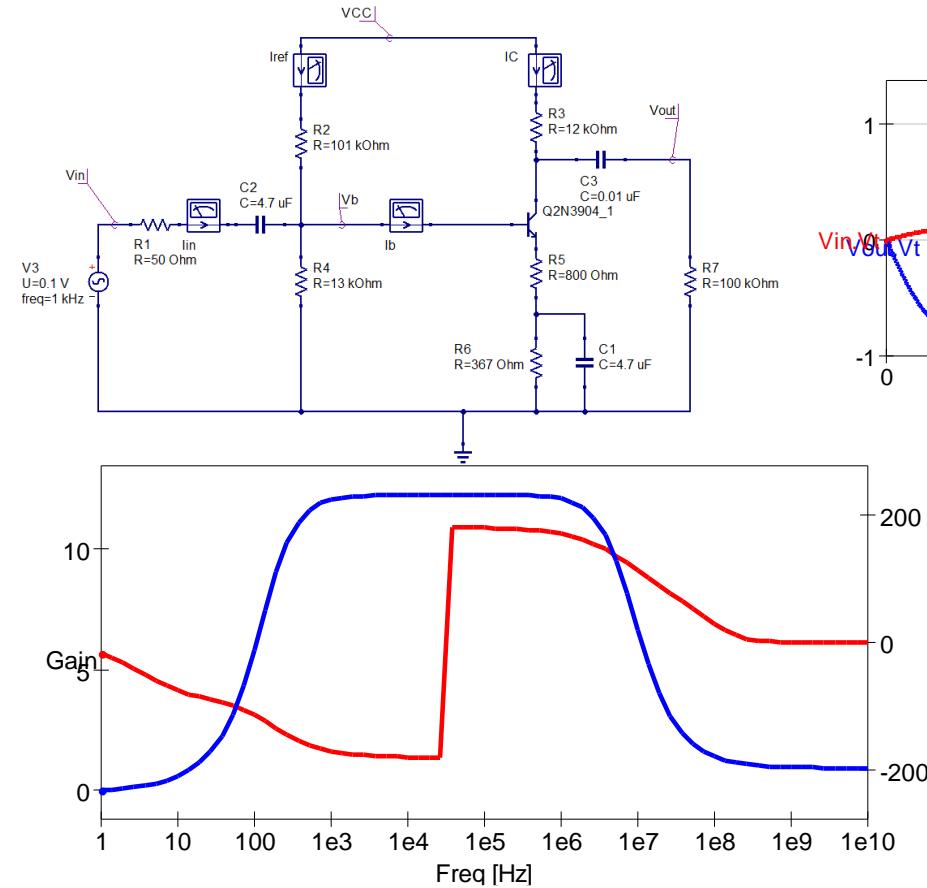
$$\cong 0.005(1 + g_m R_L)$$

$$\cong 0.005[1 + g_m (R_I \| R_6)]$$

$$\alpha_o \cong +1$$

4. BJT Amplifier Frequency Response

Introduction - CE Amplifier Freq response

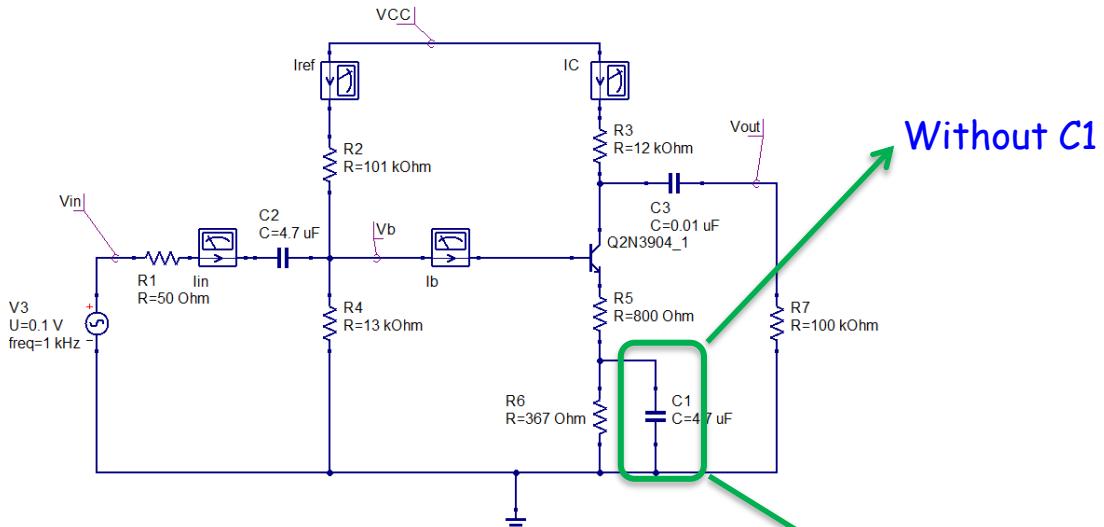


Gain starts increasing at about 10 Hz and then starts to decrease at about 1 MHz.

We know C_2 and C_3 are to block DC and low-freq components in the signal.

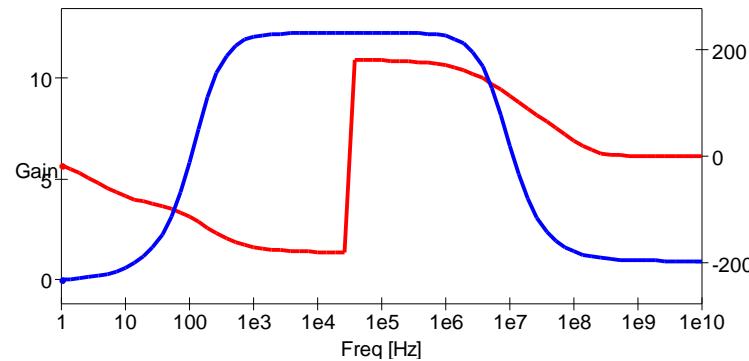
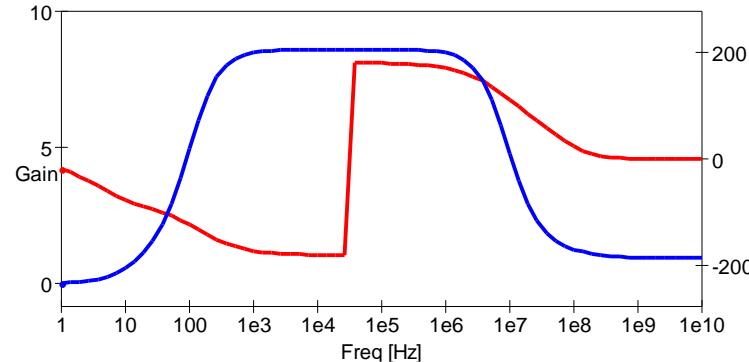
How about C_1 - the emitter by-pass capacitor?

Introduction - CE Amplifier Freq response



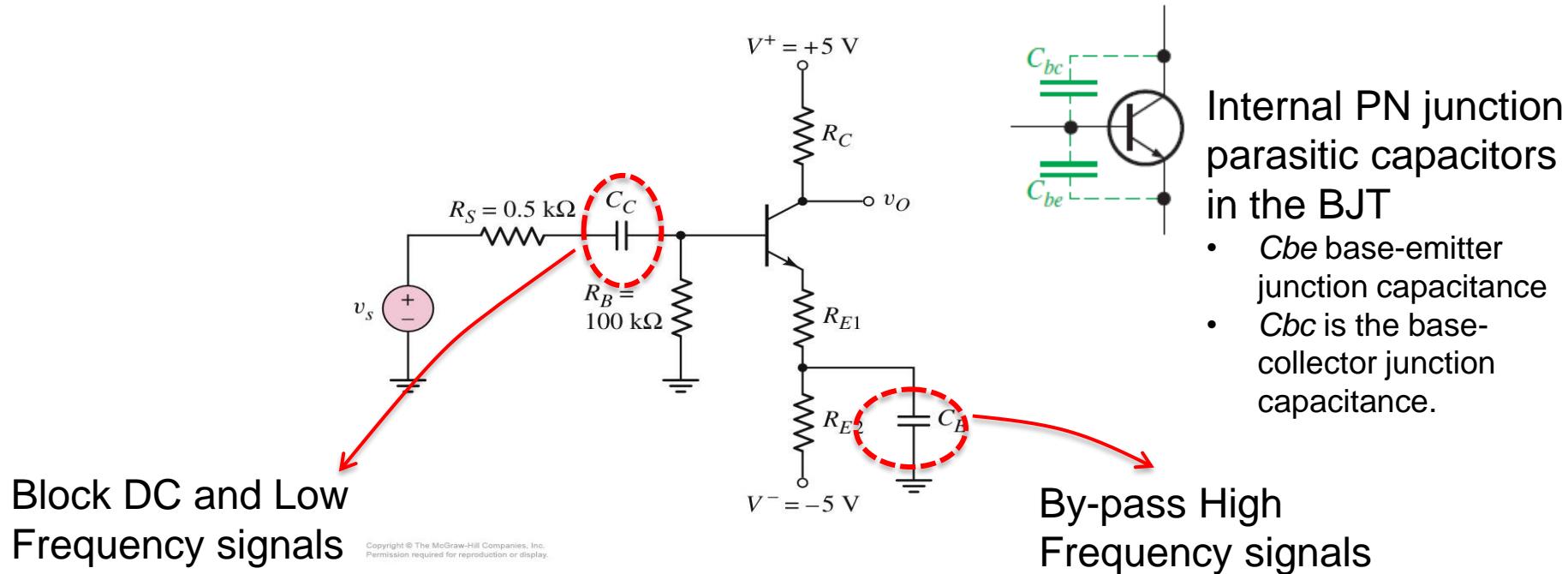
Without $C1$

With $C1$

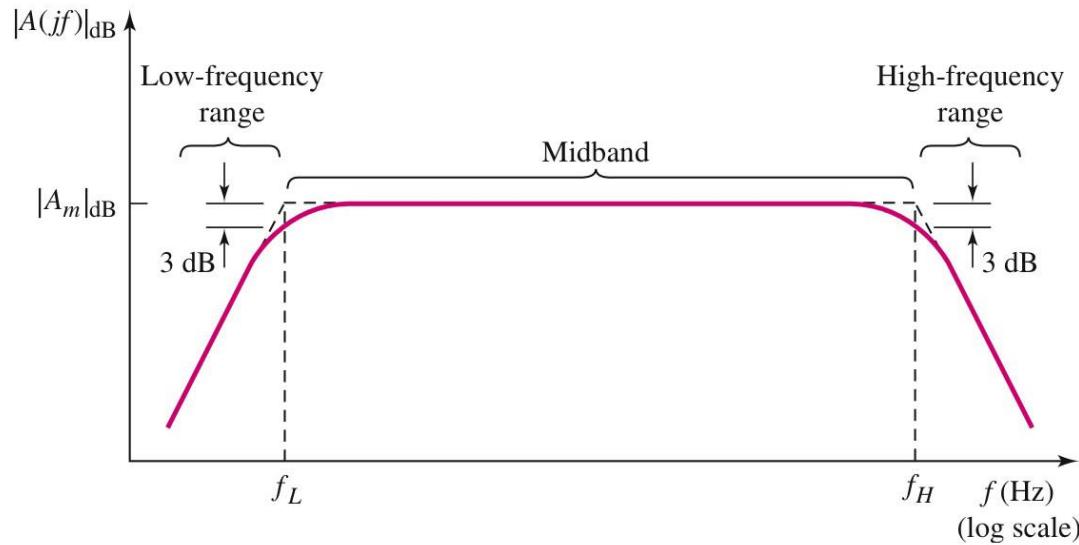


BJT High Frequency Dependence

- All the factors for amplifier gain are functions of signal frequency. What are assumptions we made about capacitors?



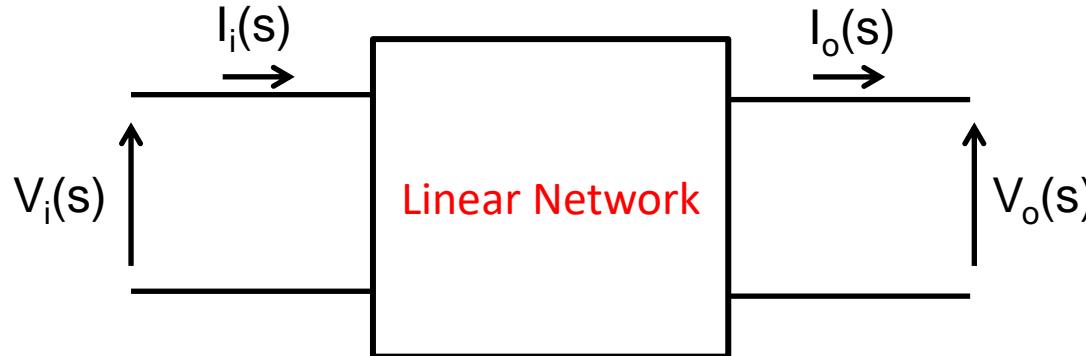
Typical Amplifier Transfer Function



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- For an Audio amplifier, signals are in the range of 20Hz to 20kHz

System Transfer Functions

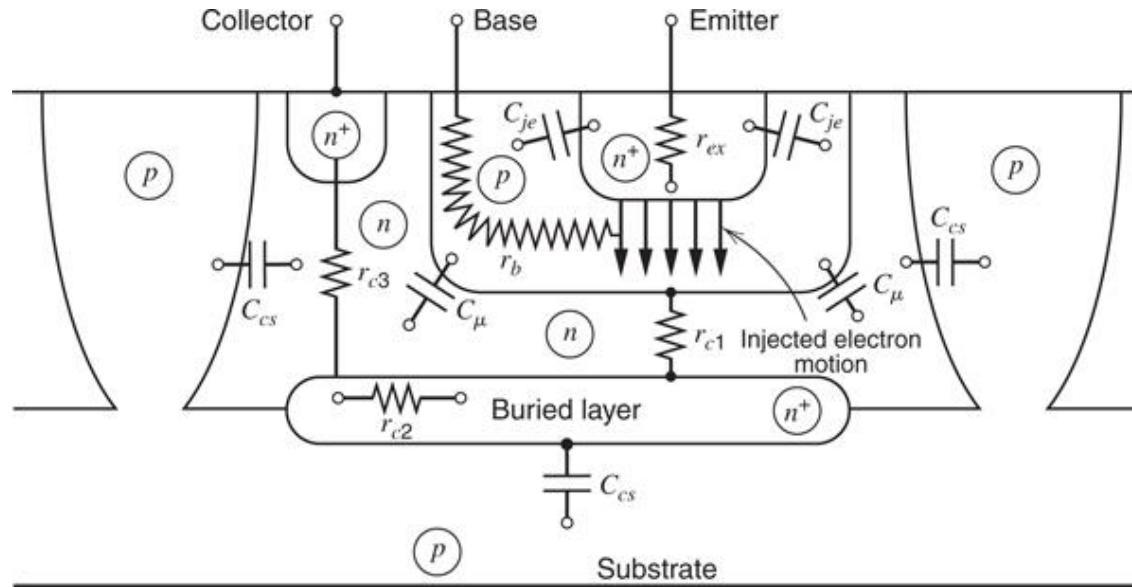


- The transfer function of a circuit is the s-domain ratio of an output (voltage or current) to an input (voltage or current) :

- Voltage transfer function $\frac{V_o(s)}{V_i(s)}$
- Current transfer function $\frac{I_o(s)}{I_i(s)}$
- Trans-resistance function $\frac{V_o(s)}{I_i(s)}$
- Trans-conductance function $\frac{I_o(s)}{V_i(s)}$

Real BJT Model

- We analysed the frequency response of circuits as a function of external resistors and capacitors, and we have assumed the transistor to be ideal.
- However, BJTs have internal capacitances that influence the high-frequency response of circuits.



Real BJT Model

the base spreading resistance and represents the resistance of the base-emitter junction

$$r_\pi = \frac{V_T}{I_Q}$$

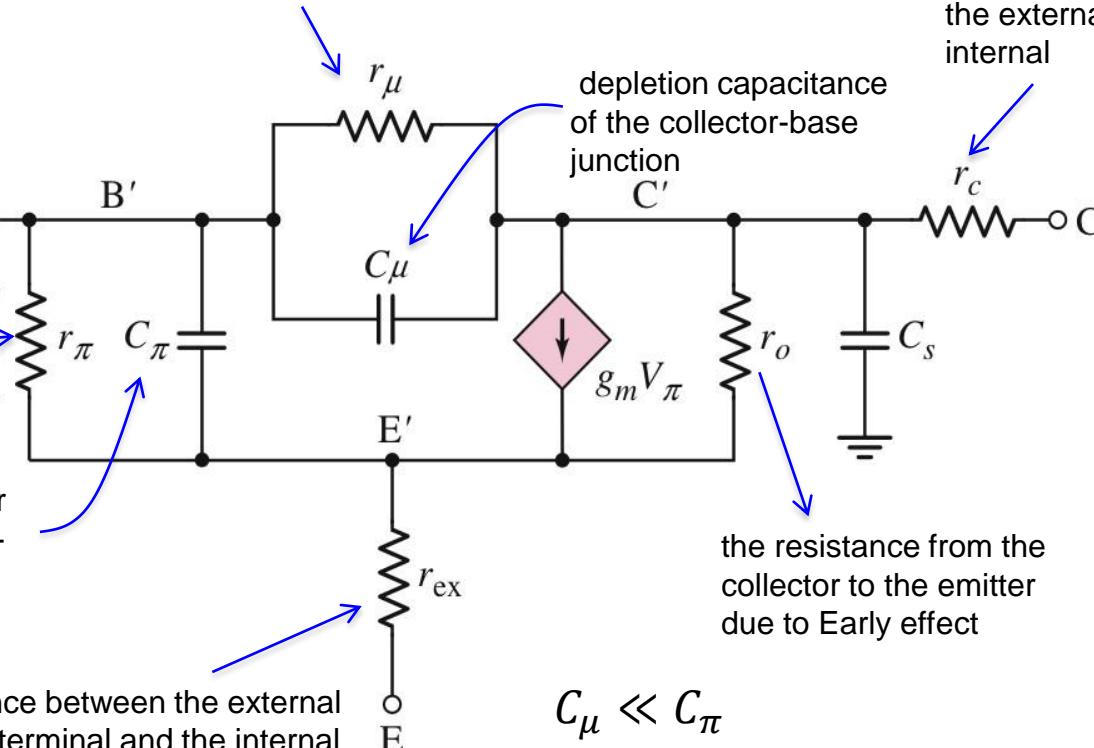
capacitance of the base-emitter junction and depends on the Q-point

resistance between the external emitter terminal and the internal emitter region. This is very small.

the feedback from the collector to the base.
Usually in M Ω s \rightarrow can be neglected.

$$C_\mu \ll C_\pi$$

Typically $C_\mu = 0.05 \text{ pF}$

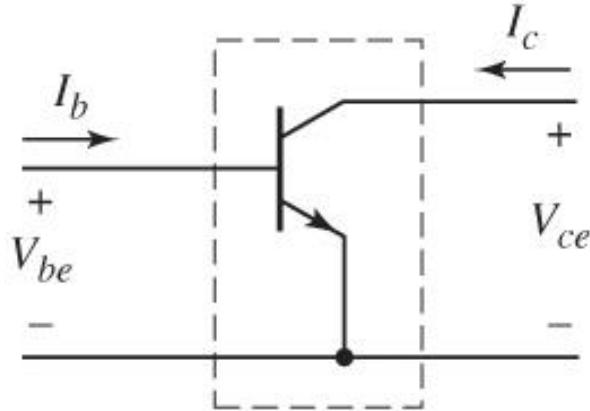


3904 Datasheet

SMALL-SIGNAL CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 20 \text{ V}_\text{dc}$, $f = 100 \text{ MHz}$)	2N3903 2N3904	f_T	250 300	- -	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ V}_\text{dc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)		C_{obo}	-	4.0	pF
Input Capacitance ($V_{EB} = 0.5 \text{ V}_\text{dc}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)		C_{ibo}	-	8.0	pF
Input Impedance ($I_C = 1.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}_\text{dc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{ie}	1.0 1.0	8.0 10	k Ω
Voltage Feedback Ratio ($I_C = 1.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}_\text{dc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small-Signal Current Gain ($I_C = 1.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}_\text{dc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{fe}	50 100	200 400	-
Output Admittance ($I_C = 1.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}_\text{dc}$, $f = 1.0 \text{ kHz}$)		h_{oe}	1.0	40	μhos
Noise Figure ($I_C = 100 \mu\text{A}_\text{dc}$, $V_{CE} = 5.0 \text{ V}_\text{dc}$, $R_S = 1.0 \text{ k } \Omega$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	NF	- -	6.0 5.0	dB

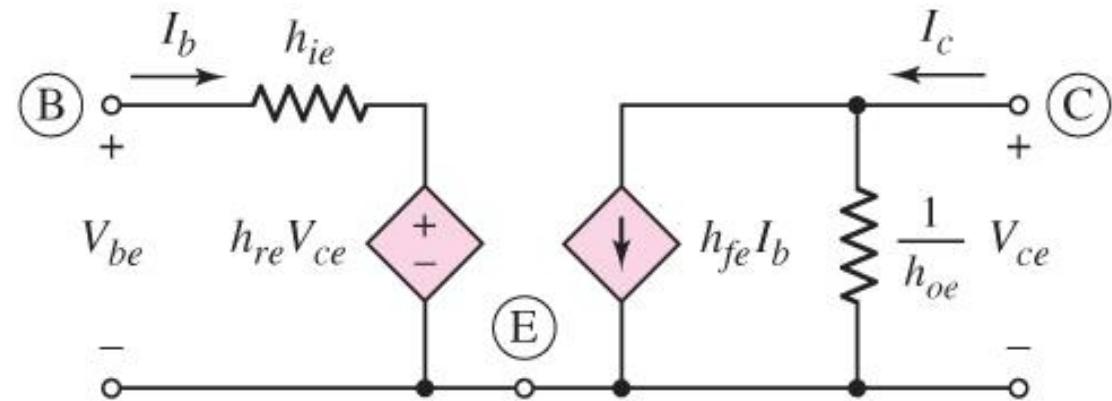
BJT h-parameters



$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$$

$$h_{ie} = r_b + r_\pi \parallel r_\mu$$

$$h_{fe} = \beta$$



$$\begin{bmatrix} v_{be} \\ i_c \end{bmatrix} = \begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} \begin{bmatrix} i_b \\ v_c \end{bmatrix}$$

$$h_{re} \cong \frac{r_\pi}{r_\mu}$$

$$h_{oe} = \frac{1 + \beta}{r_\mu} + \frac{1}{r_o}$$

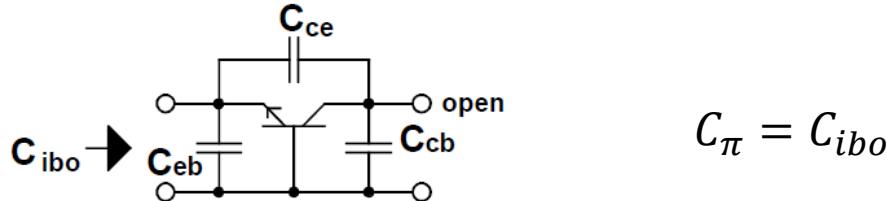
3904 Datasheet

SMALL-SIGNAL CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 20 \text{ V}_\text{dc}$, $f = 100 \text{ MHz}$)	2N3903 2N3904	f_T	250 300	-	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ V}_\text{dc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)		C_{obo}	-	4.0	pF
Input Capacitance ($V_{EB} = 0.5 \text{ V}_\text{dc}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)		C_{ibo}	-	8.0	pF

C_{ibo}

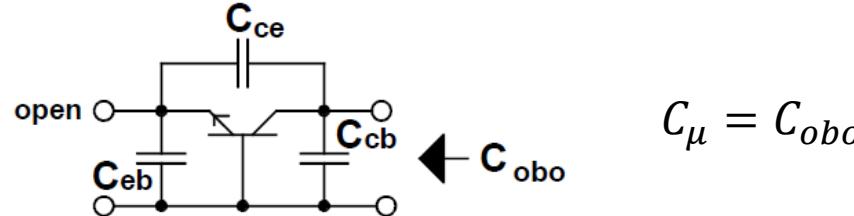
Capacitance, **I**nput,
Common-**B**ase, **O**utput open
 $C_{ibo} = C_{eb} + (C_{ce} \times C_{cb}) / (C_{ce} + C_{cb})$
 also known as: C_{ib} , C_{ebo} , C_e



$$C_\pi = C_{ibo}$$

C_{obo}

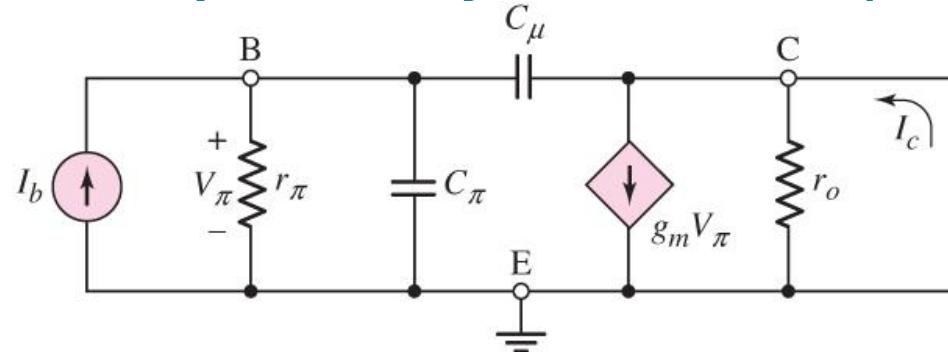
Capacitance, **O**utput,
Common-**B**ase, **O**utput open
 $C_{obo} = C_{eb} + (C_{ce} \times C_{eb}) / (C_{ce} + C_{eb})$
 also known as: C_{ob} , C_{cbo} , C_c



$$C_\mu = C_{obo}$$

<https://www.infineon.com/dgdl/AN024.pdf?fileId=db3a30431400ef6801142715ee7106d3>

Simplified BJT Model: h_{fe} vs freq.

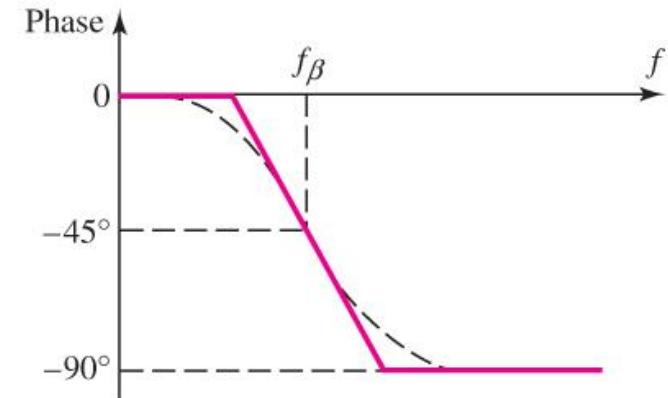
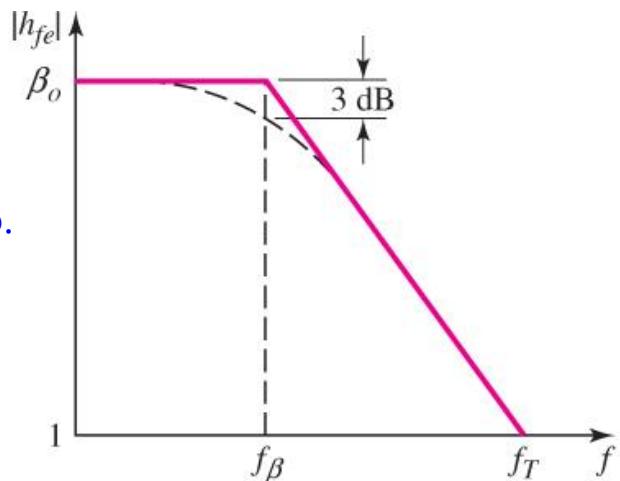


$$A_i = \frac{I_C}{I_b} = \frac{g_m - j\omega C_\mu}{\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)} \approx \frac{g_m r_\pi}{1 + j\omega r_\pi(C_\pi + C_\mu)}$$

$$A_i = \frac{\beta_o}{1 + j\frac{f}{f_\beta}} \quad f_\beta = \frac{1}{2\pi r_\pi(C_\pi + C_\mu)}$$

BW of the transistor

Low freq current gain is just β .

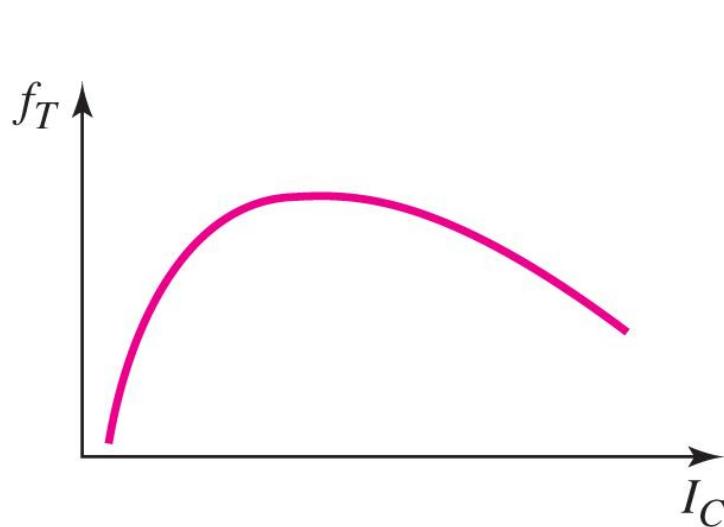


BJT unity-gain BW (f_T)

$$h_{fe} = \frac{\beta_o}{1 + j \frac{f}{f_\beta}}$$

At the cut-off freq. ($f = f_T$), $|h_{fe}| = 1$ and assuming that $\beta_o \gg 1$.

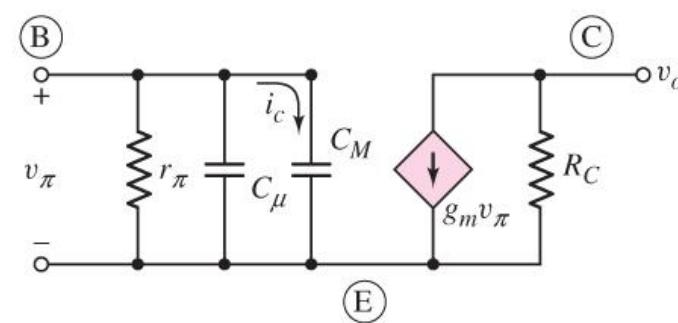
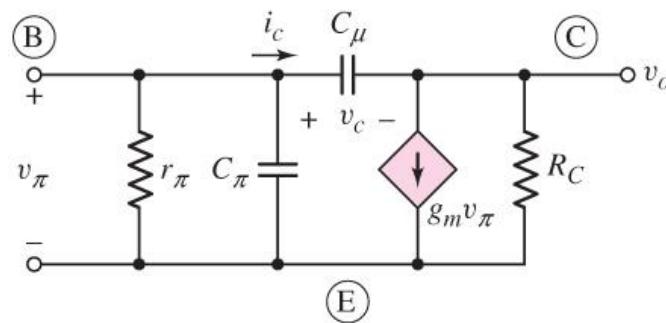
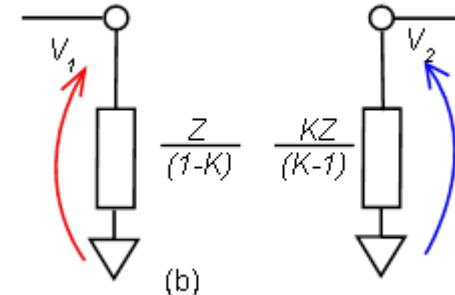
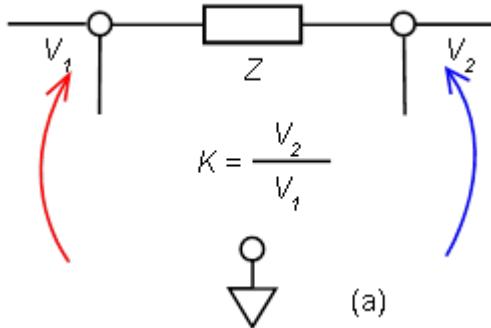
$f_T = \beta_o f_\beta \rightarrow$ gain-BW product of the transistor (unity-gain BW) usually specified on the device data sheets



$$f_T = \frac{\beta_o}{2\pi r_\pi(C_\pi+C_\mu)} = \frac{g_m}{2\pi (C_\pi+C_\mu)}$$

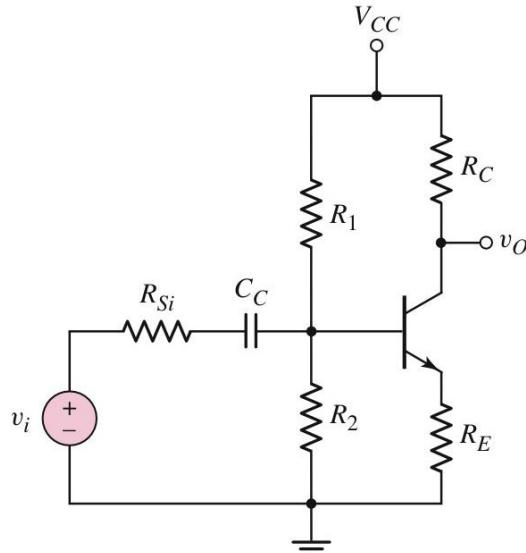
- lower at low collector current levels.
- Also decreases at high current levels (the same ways as β decreases at large currents)

Miller Capacitance



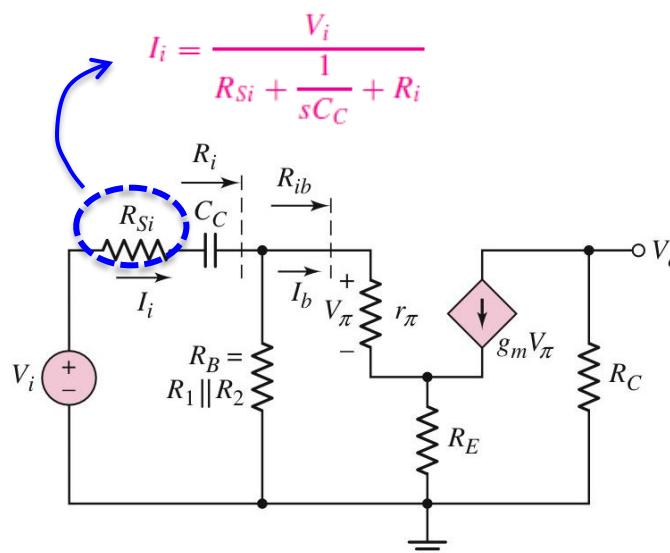
$$C_M = C_\mu(1 + A)$$

CE Amplifier Input Coupling Capacitor



$$A_v(s) = \frac{V_o(s)}{V_i(s)} = -g_m r_\pi R_C \left(\frac{R_B}{R_B + R_{ib}} \right) \left(\frac{sC_C}{1 + s(R_{Si} + R_i)C_C} \right)$$

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$$I_i = \frac{V_i}{R_{Si} + \frac{1}{sC_C} + R_i}$$

$$R_i = R_B \parallel [r_\pi + (1 + \beta)R_E] = R_B \parallel R_{ib}$$

$$I_b = \left(\frac{R_B}{R_B + R_{ib}} \right) I_i$$

and then

$$V_\pi = I_b r_\pi$$

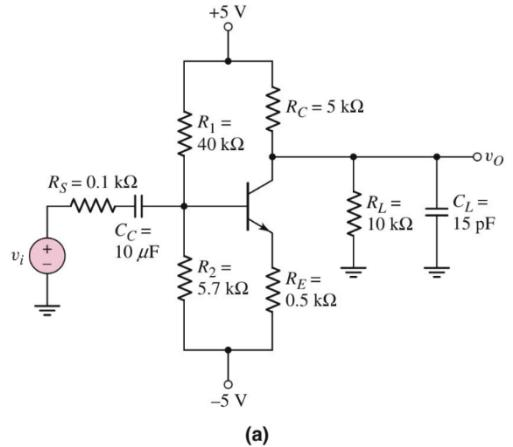
$$V_o = -g_m V_\pi R_C$$

$$f_L = \frac{1}{2\pi(R_{Si} + R_i)C_C}$$

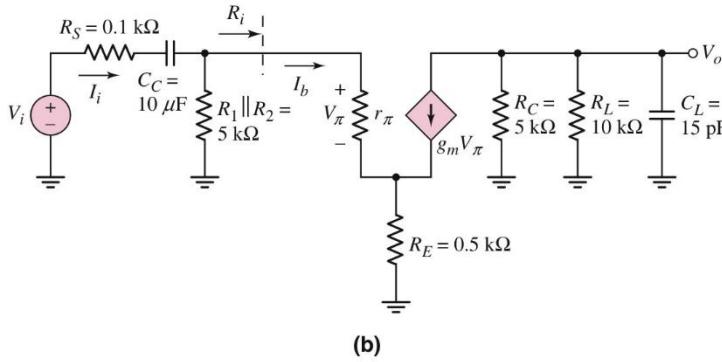
- If we set the independent voltage source equal to zero, the equivalent resistance seen by the coupling capacitor C_C is $(R_{Si} + R_i)$. The time constant is then

$$\tau_s = (R_{Si} + R_i)C_C$$

Coupling and Parallel Load Capacitors



(a)



(b)

The Bode plot of the voltage gain magnitude is similar to that shown in Figure 7.11. The lower corner frequency f_L is given by

$$f_L = \frac{1}{2\pi\tau_S} \quad (7.47)$$

where τ_S is the time constant associated with the coupling capacitor C_C , and the upper corner frequency f_H is given by

$$f_H = \frac{1}{2\pi\tau_P} \quad (7.48)$$

where τ_P is the time constant associated with the load capacitor C_L . It should be emphasized that Equations (7.47) and (7.48) are valid only as long as the two corner frequencies are far apart.

Using the small-signal equivalent circuit in Figure 7.26(b), we set the signal source equal to zero to find the equivalent resistance associated with the coupling capacitor. The related time constant is

$$\tau_S = [R_S + (R_1 \| R_2 \| R_i)C_C] \quad (7.49)$$

where

$$R_i = r_\pi + (1 + \beta)R_E \quad (7.50)$$

Similarly, the time constant related to C_L is

$$\tau_P = (R_C \| R_L)C_L \quad (7.51)$$

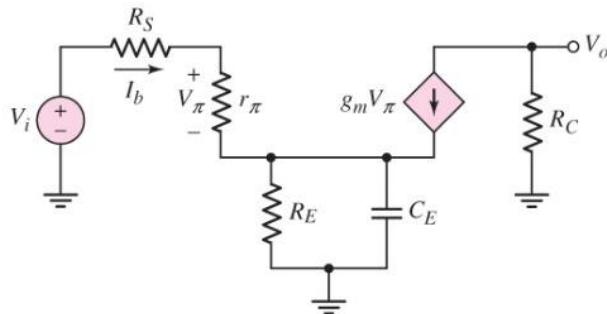
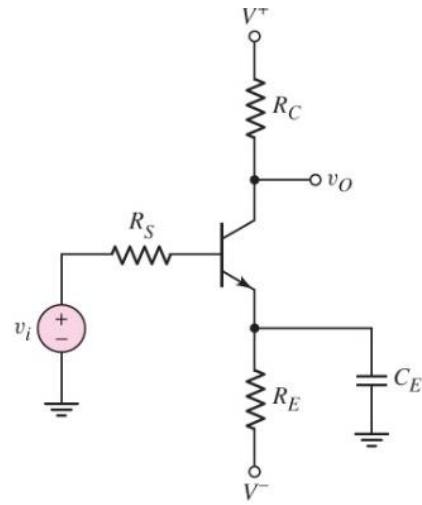
Since the two corner frequencies are far apart, the gain will reach a maximum value in the frequency range between f_L and f_H , which is the midband. We can calculate the midband gain by assuming that the coupling capacitor is a short circuit and the load capacitor is an open circuit.

Using the analysis techniques from the last chapter, we find the magnitude of the midband gain as follows:

$$\begin{aligned} |A_V| &= \left| \frac{V_o}{V_i} \right| \\ &= g_m r_\pi (R_C \| R_L) \left(\frac{R_1 \| R_2}{(R_1 \| R_2) + R_i} \right) \left(\frac{1}{[R_S + (R_1 \| R_2 \| R_i)]} \right) \end{aligned} \quad (7.52)$$

Bypass capacitor Effect

- The bypass capacitors are assumed to act as short circuits at the signal frequency.
- How about the circuit response in the frequency range where these capacitors are neither open nor short circuits.

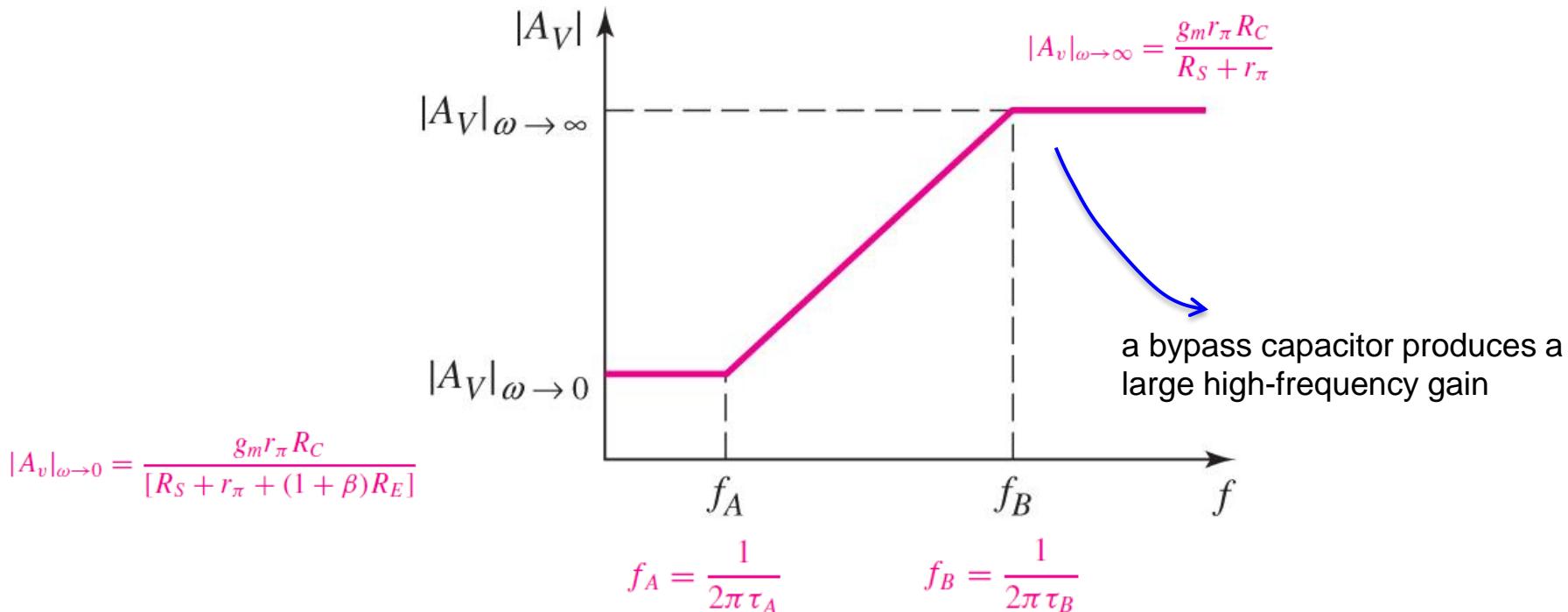


$$A_v = \frac{-g_m r_\pi R_C}{[R_S + r_\pi + (1 + \beta)R_E]} \times \left\{ 1 + \frac{s R_E (R_S + r_\pi) C_E}{[R_S + r_\pi + (1 + \beta)R_E]} \right\}$$

Bypass capacitor Effect

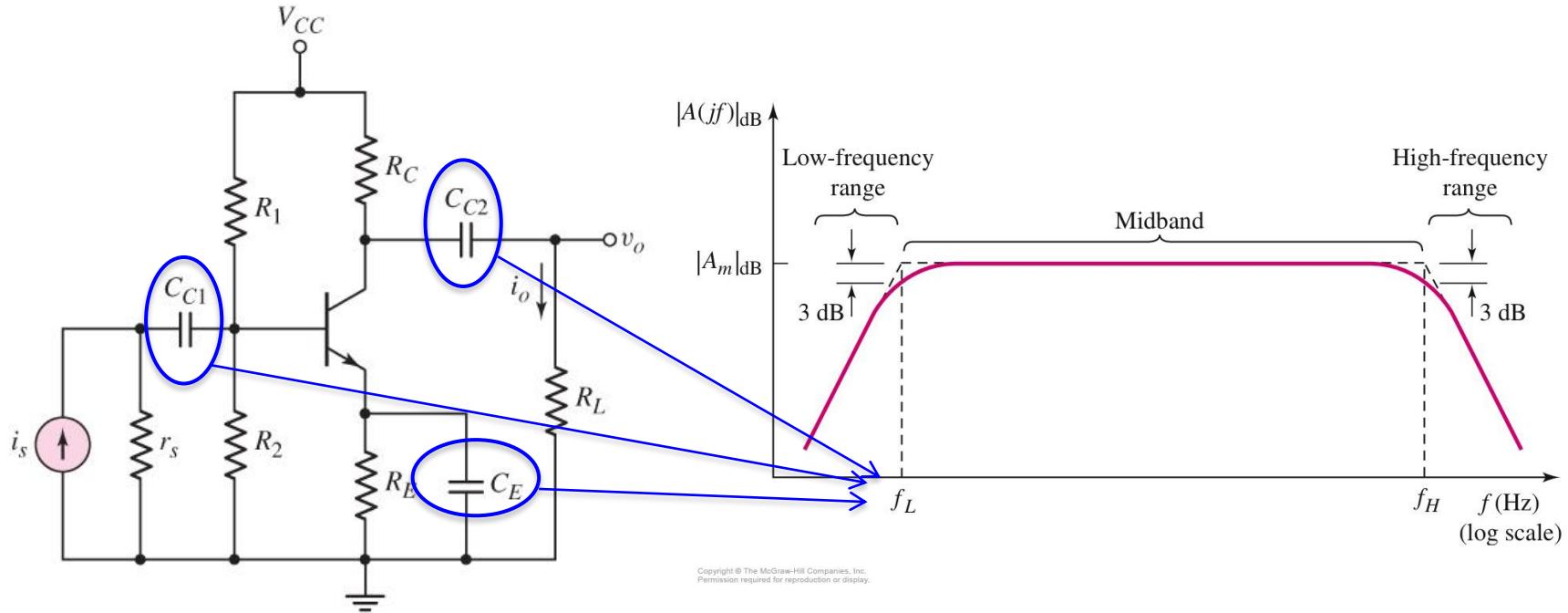
$$A_v = \frac{-g_m r_\pi R_C}{[R_S + r_\pi + (1 + \beta)R_E]} \times \left\{ 1 + \frac{s R_E (R_S + r_\pi) C_E}{[R_S + r_\pi + (1 + \beta)R_E]} \right\}$$

$$A_v = \frac{-g_m r_\pi R_C}{[R_S + r_\pi + (1 + \beta)R_E]} \left\{ \frac{1 + s \tau_A}{1 + s \tau_B} \right\}$$



Combined Effects: Coupling and Bypass Capacitors

- When a circuit contains multiple capacitors, the frequency response analysis becomes more complex. → which capacitor is the dominant!



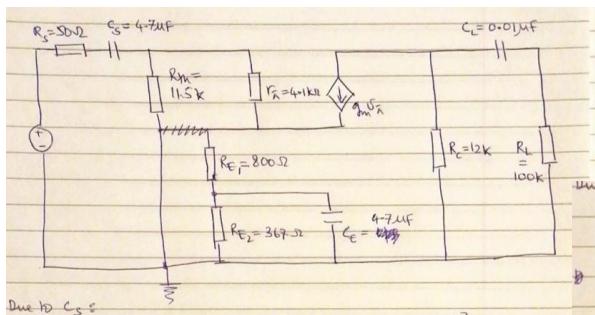
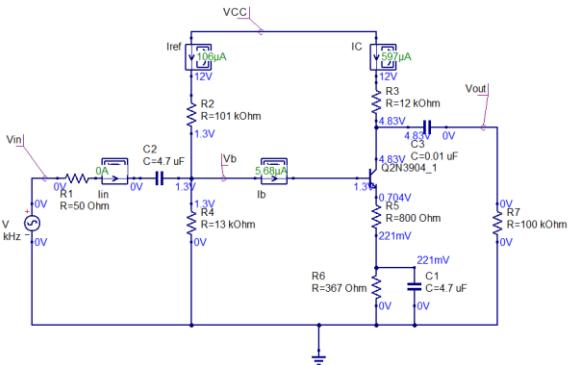
Estimate f_L : Short-Circuit Time Constant Method

- ❑ Lower cut-off frequency for a network with n coupling and bypass capacitors can be estimated by:

$$\omega_L \approx \sum_{i=1}^n \frac{1}{R_{eff} C_i}$$

- ❑ R_{eff} is the resistance at terminal of i^{th} capacitor C_i with all other capacitors replaced by short circuits
- ❑ $R_{eff} C_i$ is the short-circuit time constant with C_i

Estimate f_L : Example



Due to C_S

$$T_S = 4 \times 10^{-6} \times [R_s + (11.5k \parallel 4.1k + 100k \times 800)]$$

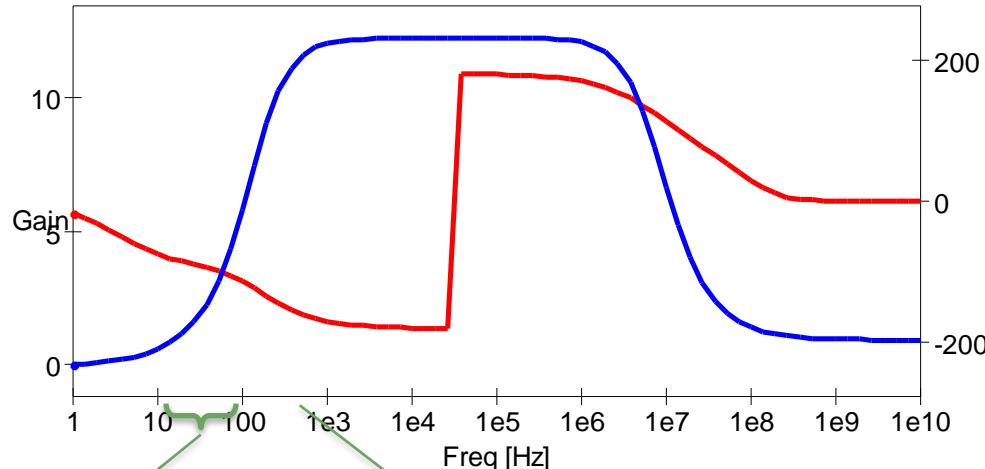
$$= [50 + \frac{11.5 \times 84.1}{11.5 + 84.1}] = 4.7 \times (50 + 10k)$$

$\zeta_S = 0.047 \Rightarrow \omega_S = \frac{1}{\zeta_S} \Rightarrow f_S = \frac{1}{2\pi \times 0.047} = 33 \text{ Hz}$

Due to Load Cap:

$$\zeta_L = 0.01 \times 10^{-6} [R_L + (R_c \parallel r_o)] = 0.01 \times 10^{-6} [100k + 12k]$$

$\zeta_L = 0.00112 \Rightarrow f_L' = \frac{1}{2\pi \times 0.00112} = 142 \text{ Hz}$



Due to load cap:

Effective R from emitter: $r_n + (R_m \parallel R_s)$
 $(R_{out,E}) = 40k + (11.5k \parallel 50) \approx 47.9$
 $\approx 47.9 \text{ k}\Omega$

$$\zeta_E = \frac{R_E \times 10^{-12}}{R_{out,E} \parallel (R_L + 800)}$$

$$= 4.7 \times 10^{-12} \times [4140 \parallel 4140] =$$

$$= 4.7 \times 10^{-12} \times 367 \rightarrow 6.2 \times 10^{-12}$$

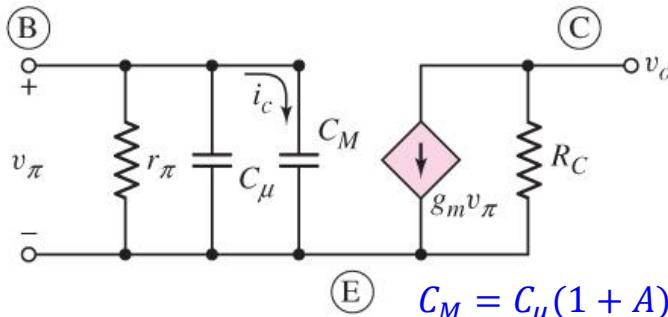
$$= 3.4 \times 10^{-12} \times 341 \rightarrow 6.2 \times 10^{-12}$$

$$f_E = \frac{1}{2\pi \times 0.0016} = 624 \text{ Hz}$$

Estimate f_H : BJT only

SMALL-SIGNAL CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = 10 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ MHz}$)	2N3903 2N3904	f_T	250 300	-	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)		C_{obo}	-	4.0	pF
Input Capacitance ($V_{EB} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)		C_{ibo}	-	8.0	pF
Input Impedance ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{ie}	1.0 1.0	8.0 10	k Ω
Voltage Feedback Ratio ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small-Signal Current Gain ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{fe}	50 100	200 400	-
Output Admittance ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)		h_{oe}	1.0	40	μmhos
Noise Figure ($I_C = 100 \mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$, $R_S = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	NF	- -	6.0 5.0	dB

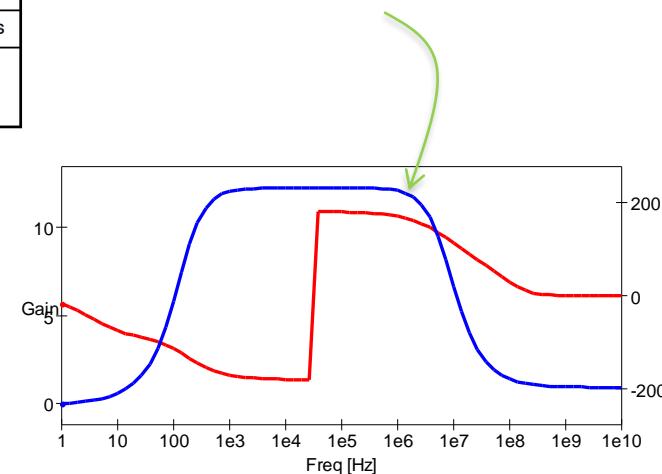


$$f_T = \frac{\beta_o}{2\pi r_\pi(C_\pi + C_\mu)} = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

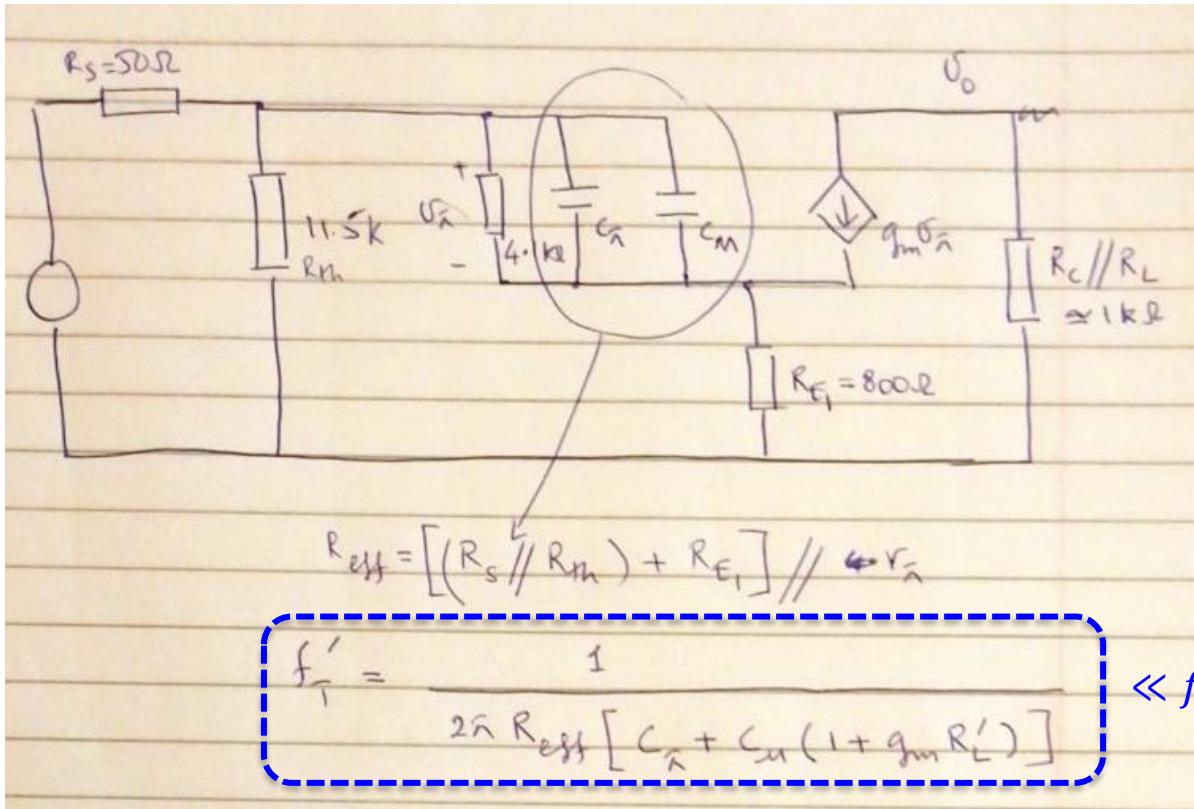
$f_T = 300 \text{ MHz}$ for 2N3904

$$f_\beta = \frac{300}{\beta} \text{ MHz}$$

$0.75 \text{ MHz} < f_\beta < 3 \text{ MHz}$



Estimate f_H : Net value



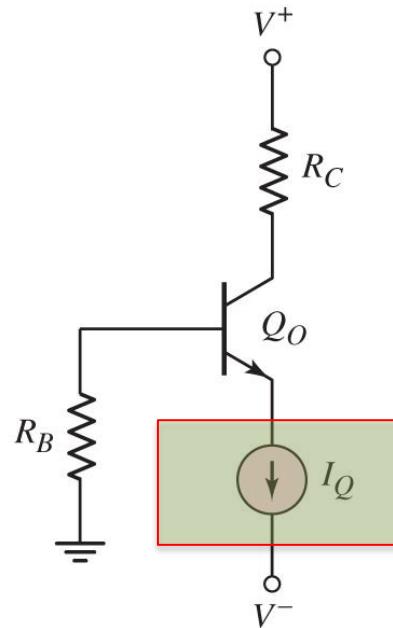
Need C_{π} to calculate

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5. BJT Current Mirrors and Active Loads

Current-Source Biasing

- ❑ Another way to bias a BJT small signal amplifier is to use one voltage source and one current source.
- ❑ The main advantage is: The DC emitter current is independent of β or BJT temperature!



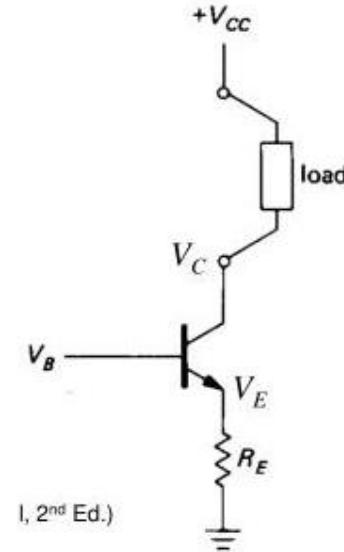
Single BJT Current Source

- Ideally, the collector current does not depend on the collector to emitter voltage. This property allows the transistor to behave as a constant current source when its base-emitter voltage is fixed.

$$I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7}{R_E}$$

$$V_E = V_B - 0.7$$

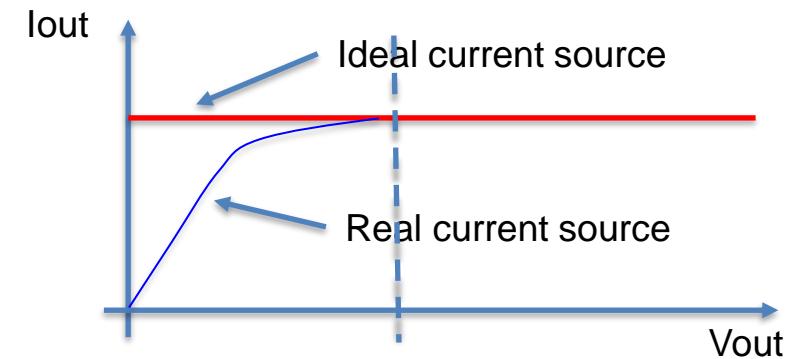
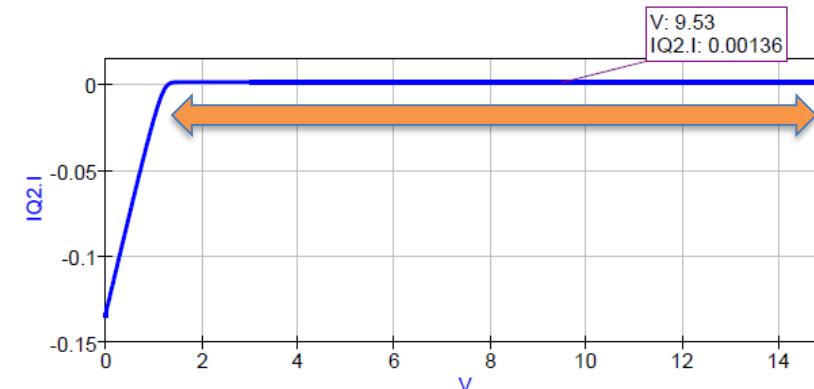
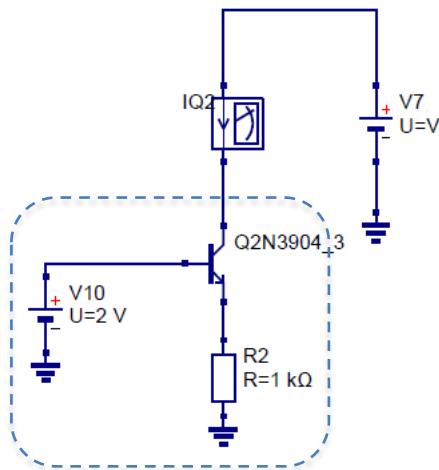
$$I_C \cong I_E = \frac{V_B - 0.7}{R_E}$$



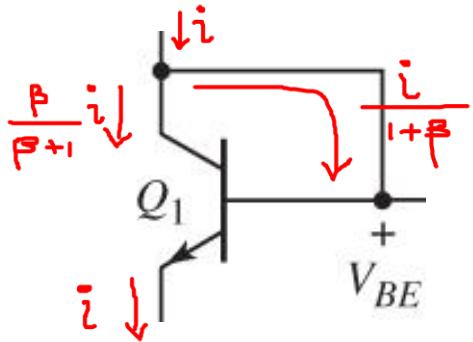
- I_c will be independent of V_c as long as V_{ce} > 0.2 V (transistor is not saturated)

Single BJT Current Source

- The output voltage range over which I_C is constant is called *output compliance*

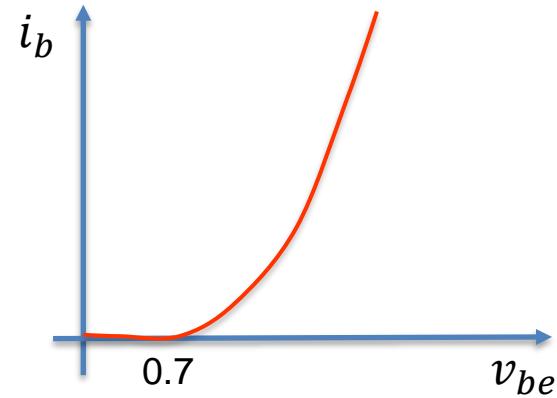
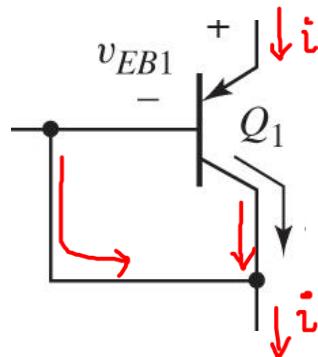


Diode Connected Transistor

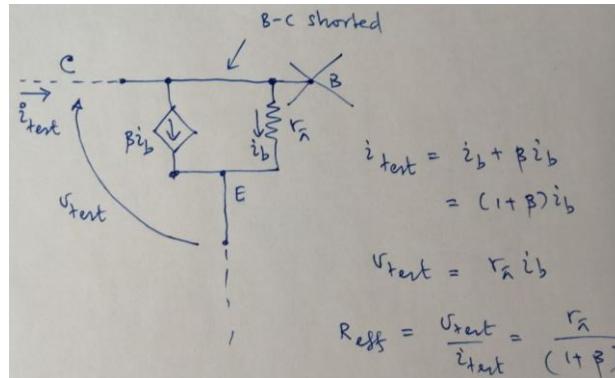


B and C of a BJT is shorted together.
 $V_{cb} = 0 \rightarrow Q_1$ is in FA mode.

A diode-connected transistor can be considered as a resistor $\frac{r_\pi}{1+\beta}$.



The characteristics of this transistor is similar to $i_b - v_{be}$ characteristic of BJT \rightarrow similar to a diode



Two-Transistor Current Source

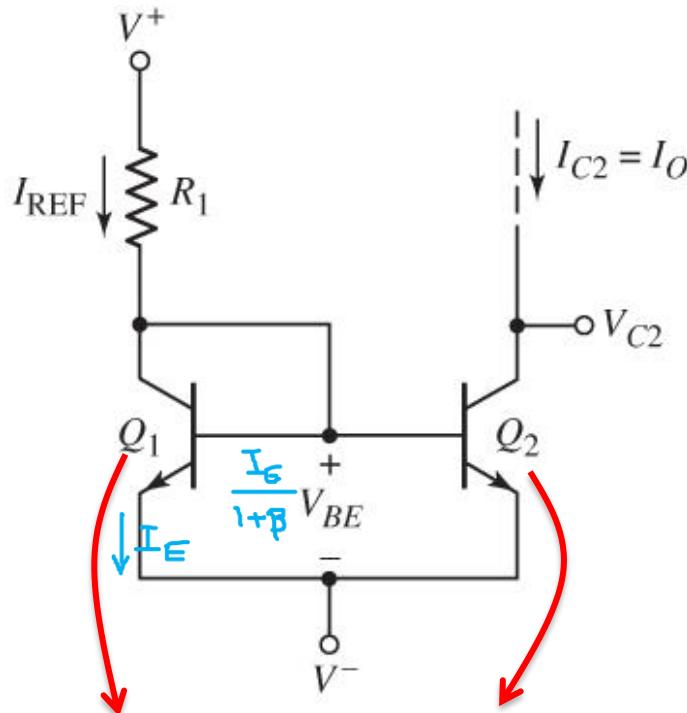


Figure 10.2(a) shows the currents in the two-transistor current source. Since V_{BE} is the same in both devices, and the transistors are identical, then $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. Transistor Q_2 is assumed to be biased in the forward-active region. If we sum the currents at the collector node of Q_1 , we have

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2} \quad (10.2)$$

Replacing I_{C1} by I_{C2} and noting that $I_{B2} = I_{C2}/\beta$, Equation (10.2) becomes

$$I_{REF} = I_{C2} + 2\frac{I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right) \quad (10.3)$$

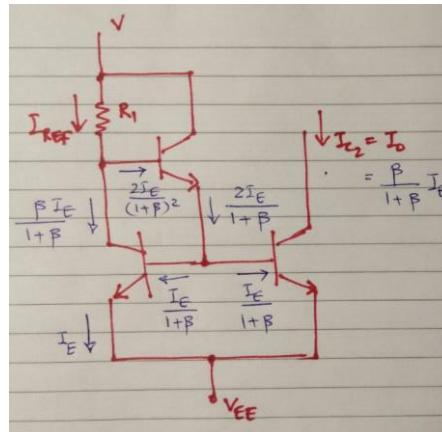
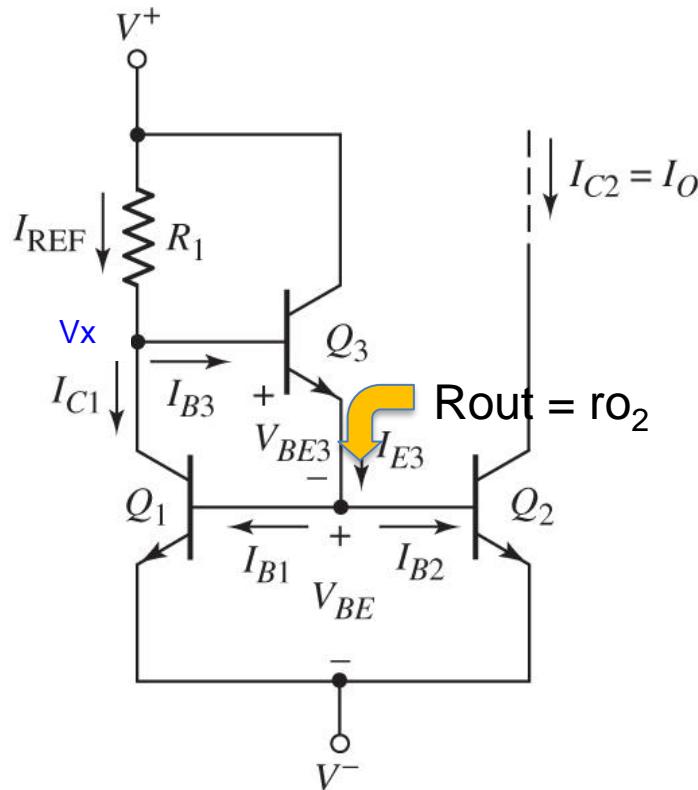
The output current is then

$$I_{C2} = I_O = \frac{I_{REF}}{1 + \frac{2}{\beta}} \quad (10.4)$$

$I_O \approx I_{REF}$ for $\beta \gg 1$. $\beta = 100$, results in 2% error

What is the minimum value of V_{C2} for $I_{C2} = I_{REF}$?

Three-Transistor Current Source



$$I_{REF} = \frac{\beta I_E}{1+\beta} + \frac{2 I_E}{(1+\beta)^2}$$

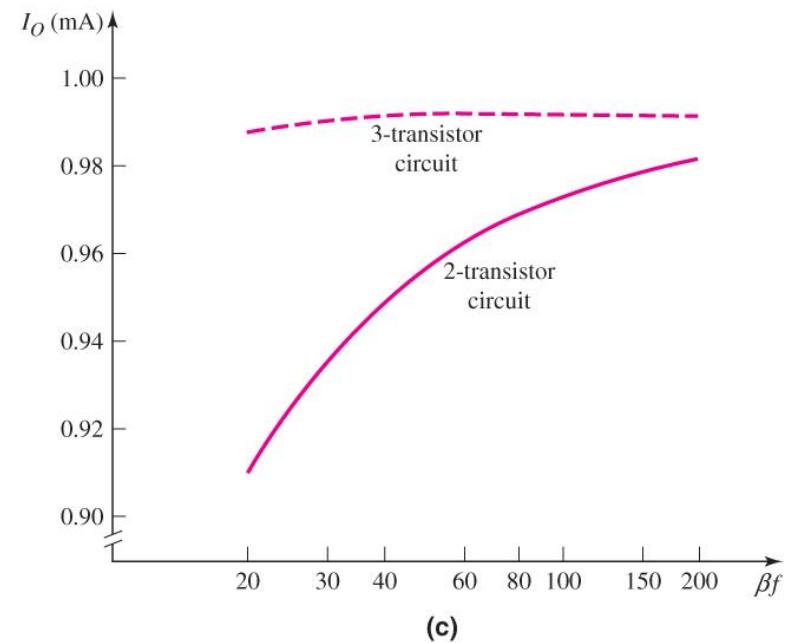
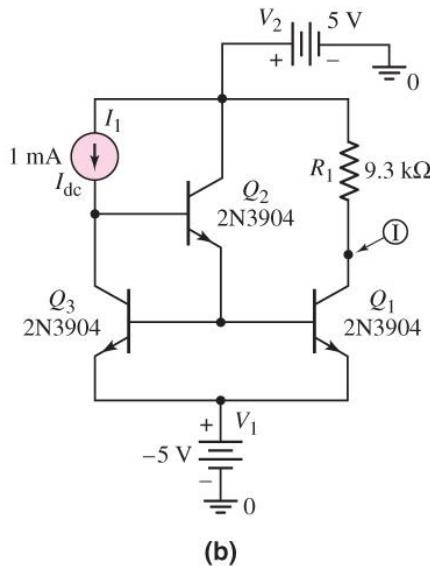
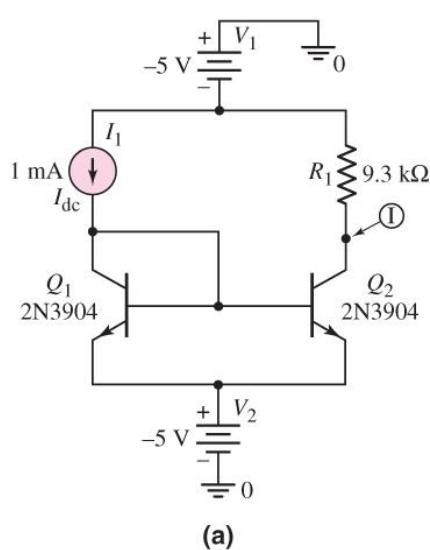
$$I_O = \frac{\beta}{1+\beta} I_E$$

$$I_O = \frac{I_{REF}}{1 + 2/(\beta^2 + \beta)}$$

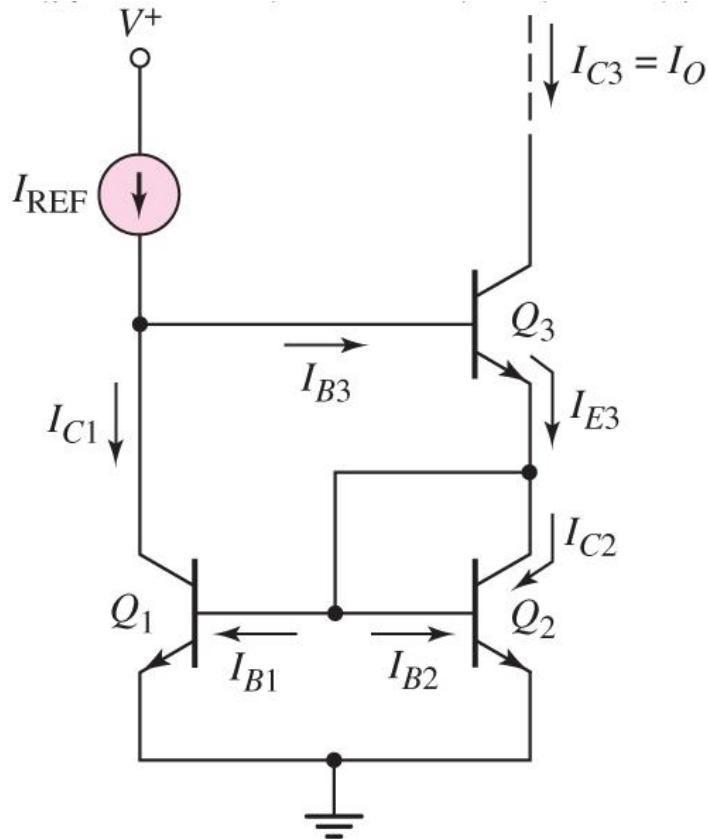
$$I_O \approx \frac{1}{1 + 2/\beta^2}$$

Error due to finite β has been reduced from $2/\beta$ to $2/\beta^2$!

Two/Three-Transistor Current Mirror Example



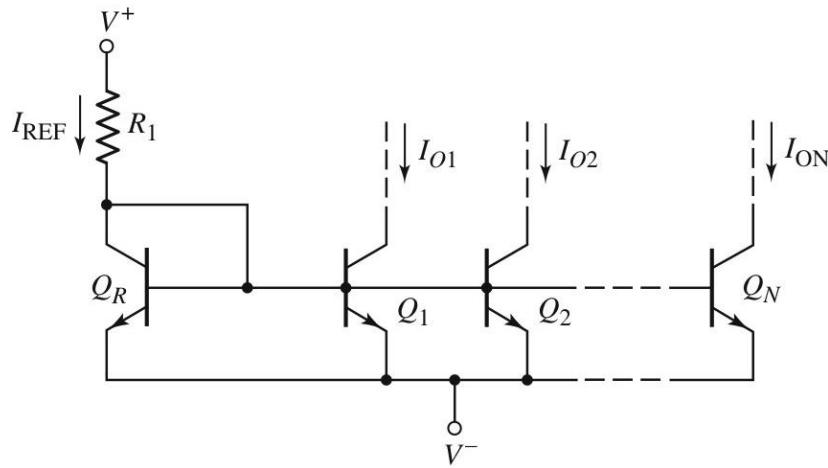
Wilson Current Source



$$I_{C3} = I_O = I_{\text{REF}} \times \frac{1}{1 + \frac{2}{\beta(2 + \beta)}}$$

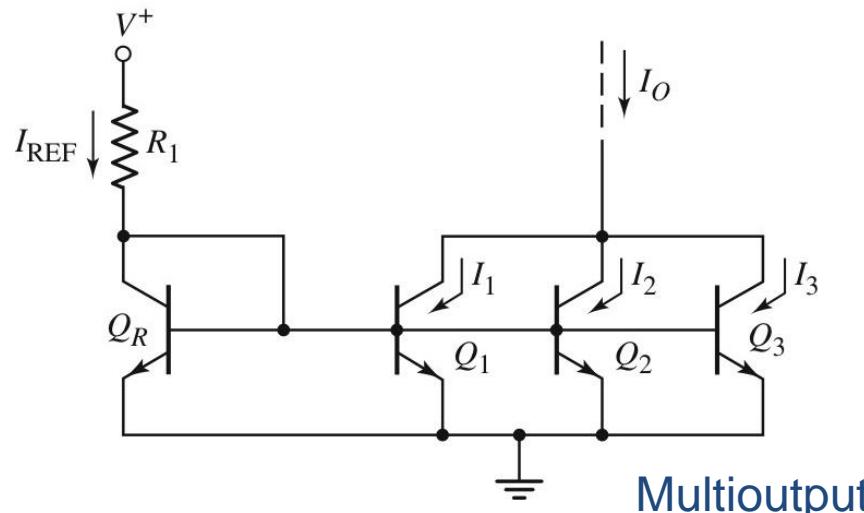
Expression is similar to 3-transistor current source

Multi-transistor/Multioutput Current Mirrors



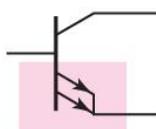
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Multitransistor

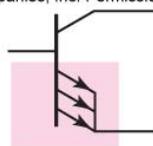


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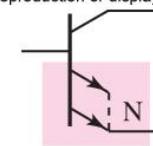
Multioutput



(a)

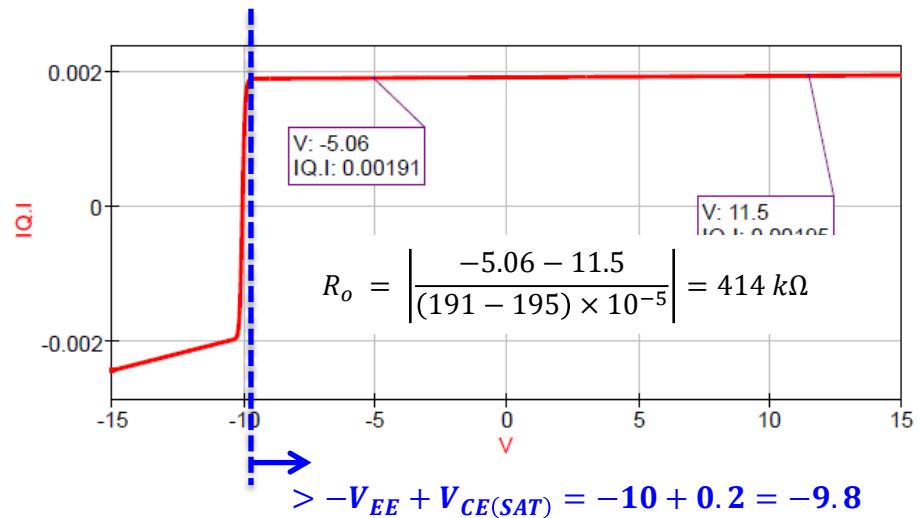
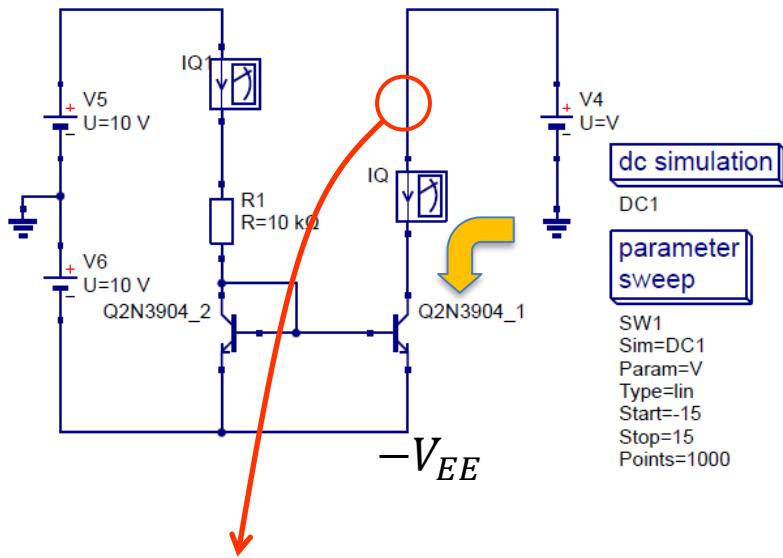


(b)



(c)

Issues with BJT Current Sources



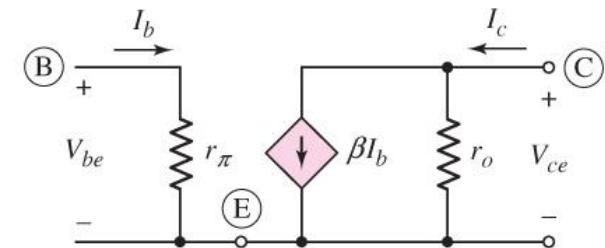
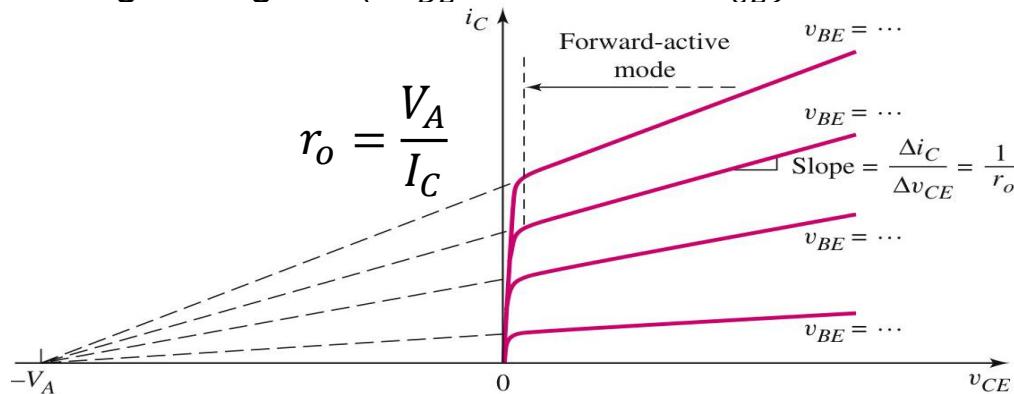
Voltage at this point should be larger than $-V_{EE} + V_{CE(SAT)}$ to keep the BJT in the active region

Then, I_Q will become I_{REF}

Issues in BJT Current Sources

- The current will vary even when the transistor is in FA mode

- The Early effect:** for a given V_{BE} the collector current will be higher if the collector voltage is higher. ($\Delta V_{BE} \approx -0.0001 \Delta V_{CE}$)



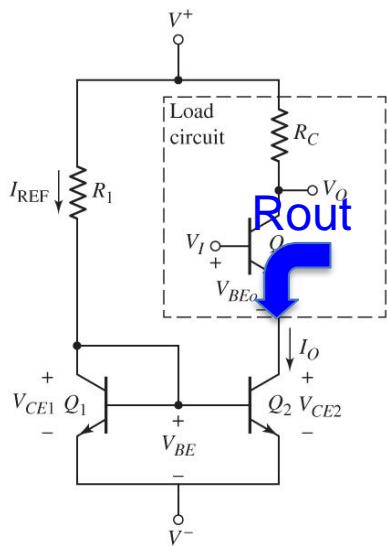
What is the requirement of R_{out} ?

- V_{BE} and β depend on temperature
 - $\Delta V_{BE} \approx -2.1 \text{ mV}/{}^\circ\text{C}$

- In order to minimize these two effects, choose $V_E \geq 1V$. Then, a 10mV change in V_{BE} does not affect the voltage across RE.

Two-Transistor Current Source: Rout

- In actual transistors, the Early voltage is finite, which means that the collector current is a function of the collector–emitter voltage. The stability of a load current generated in a constant-current source is a function of the output resistance looking back into the output transistor.



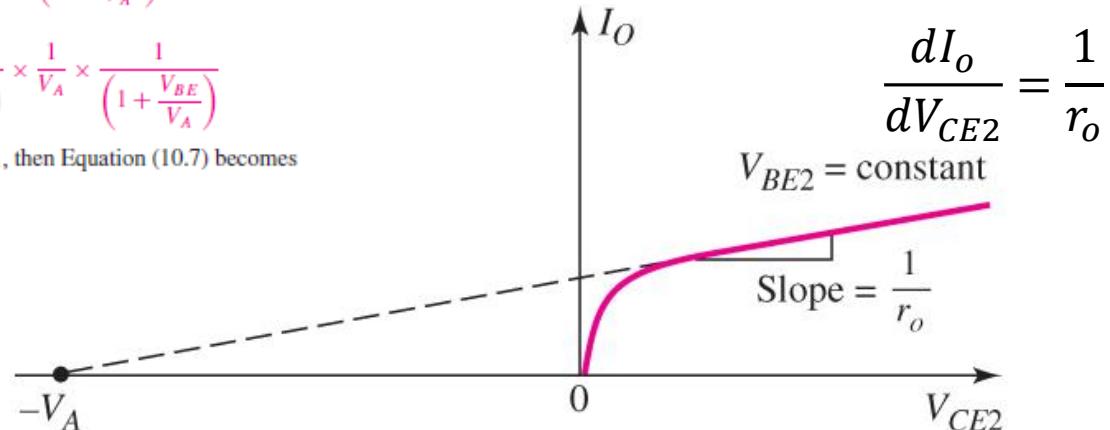
$$\frac{I_O}{I_{\text{REF}}} = \frac{1}{\left(1 + \frac{2}{\beta}\right)} \times \frac{\left(1 + \frac{V_{CE2}}{V_A}\right)}{\left(1 + \frac{V_{CE1}}{V_A}\right)}$$

A change in V_I , changes $V_{c2} \rightarrow V_{CE2} \rightarrow I_O$

$$\frac{dI_O}{dV_{CE2}} = \frac{I_{\text{REF}}}{\left(1 + \frac{2}{\beta}\right)} \times \frac{1}{V_A} \times \frac{1}{\left(1 + \frac{V_{BE}}{V_A}\right)}$$

If we assume $V_{BE} \ll V_A$, then Equation (10.7) becomes

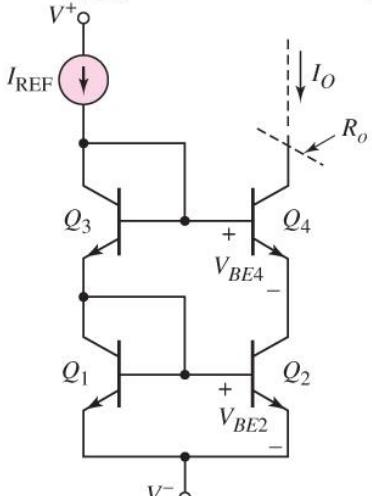
$$\frac{dI_O}{dV_{CE2}} \cong \frac{I_O}{V_A} = \frac{1}{r_o}$$



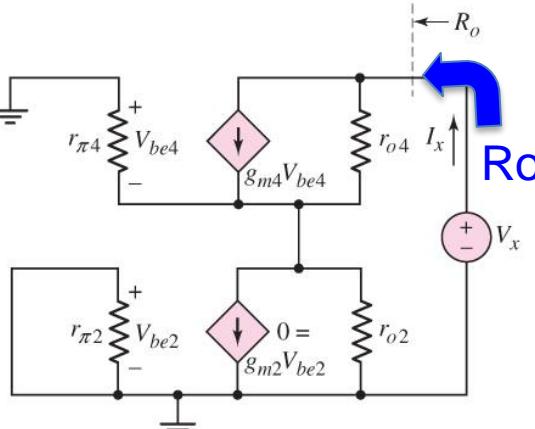
Design Aspect: Keep Rout as high as possible

Cascode Current Source

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(a)



(b)

The equivalent circuit is then shown in Figure 10.7(b). Since $g_{m2}V_{be2} = 0$, then $V_{be4} = -I_x(r_{o2}\|r_{\pi4})$. Summing currents at the output node yields

$$\begin{aligned} I_x &= g_{m4}V_{be4} + \left(\frac{V_x - I_x(r_{o2}\|r_{\pi4})}{r_{o4}} \right) \\ &= -g_{m4}I_x(r_{o2}\|r_{\pi4}) + \left(\frac{V_x - I_x(r_{o2}\|r_{\pi4})}{r_{o4}} \right) \end{aligned} \quad (10.19)$$

Combining terms and assuming $r_{\pi4} \ll r_{o2}$, we find

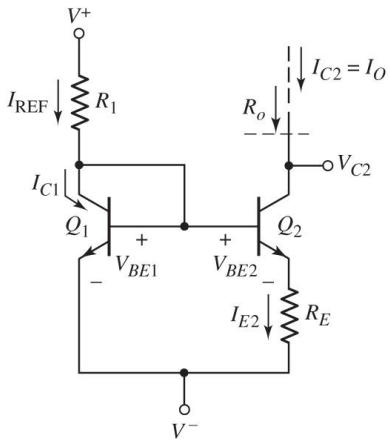
$$R_o = \frac{V_x}{I_x} = r_{o4}(1 + \beta) + r_{\pi4} \cong \beta r_{o4} \quad (10.20)$$

The output resistance has increased by a factor of β compared to the two-transistor current source, which increases the stability of the current source with changes in output voltage.

- R_o has increased by a factor of β (from r_o to βr_o)

Widlar Current Source

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Current Relationship

If $\beta \gg 1$ for Q_1 and Q_2 , and if the two transistors are identical, then

$$I_{\text{REF}} \cong I_{C1} = I_S e^{V_{BE1}/V_T}$$

and

$$I_O = I_{C2} = I_S e^{V_{BE2}/V_T}$$

Solving for the B-E voltages, we have

$$V_{BE1} = V_T \ln\left(\frac{I_{\text{REF}}}{I_S}\right)$$

and

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

Combining Equations (10.27(a)) and (10.27(b)) yields

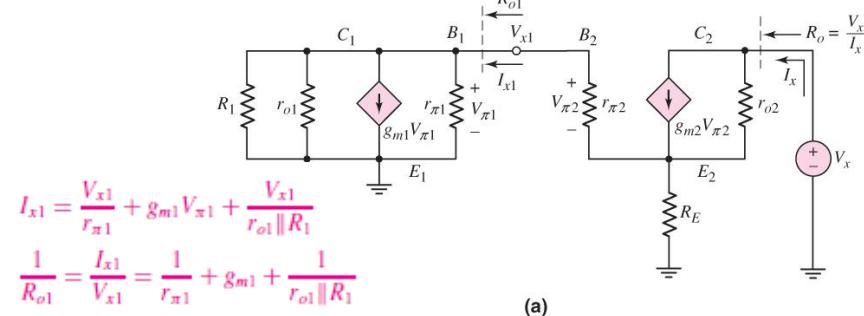
$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{\text{REF}}}{I_O}\right)$$

From the circuit, we see that

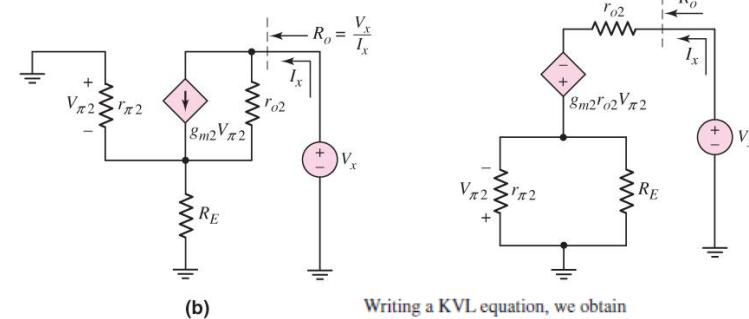
$$V_{BE1} - V_{BE2} = I_E R_E \cong I_O R_E$$

When we combine Equations (10.28) and (10.29), we obtain:

$$I_O R_E = V_T \ln\left(\frac{I_{\text{REF}}}{I_O}\right)$$



$R_{o1} \ll r_{\pi 2}$, we can neglect the effect of R_{o1} ,



Writing a KVL equation, we obtain

$$V_x = I_x r_{o2} - g_{m2} r_{o2} V_{\pi 2} + I_x R'_E$$

Substituting Equation (10.34) into (10.35) yields

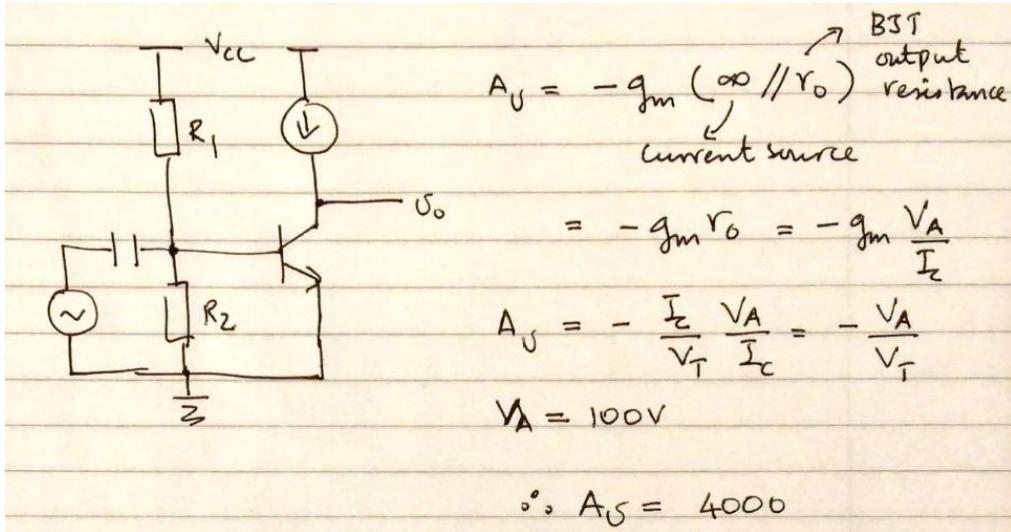
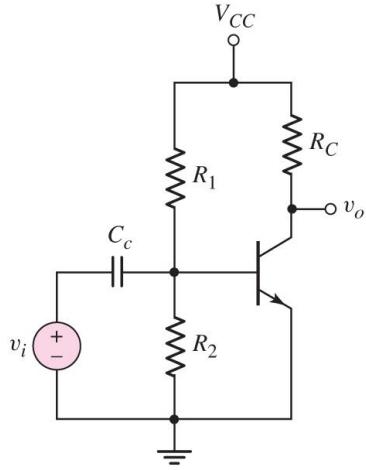
$$\frac{V_x}{I_x} = R_o = r_{o2} \left[1 + R'_E \left(g_{m2} + \frac{1}{r_{o2}} \right) \right]$$

Normally, $(1/r_{o2}) \ll g_{m2}$; therefore,

$$R_o \cong r_{o2} (1 + g_{m2} R'_E)$$

Output impedance $R_o \cong (1 + g_m(R_E//r_\pi))r_o \rightarrow \text{increased!}$

Circuits with Active Loads



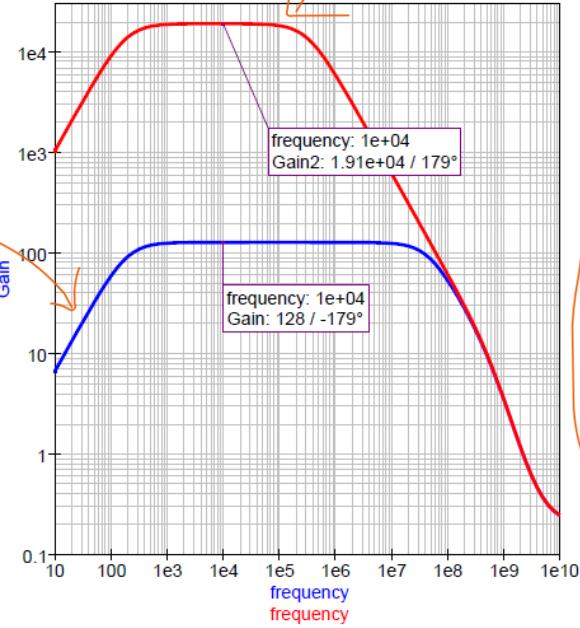
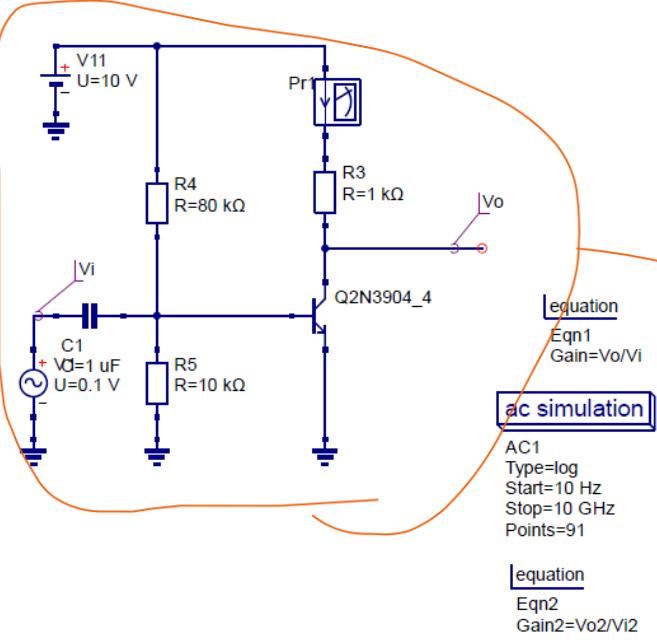
□ AC gain for this amplifier is:

$$A_v = -g_m R_C \text{ where } g_m = \frac{I_{CQ}}{V_T}$$

$$A_v = -\frac{I_{CQ}}{V_T} R_C$$

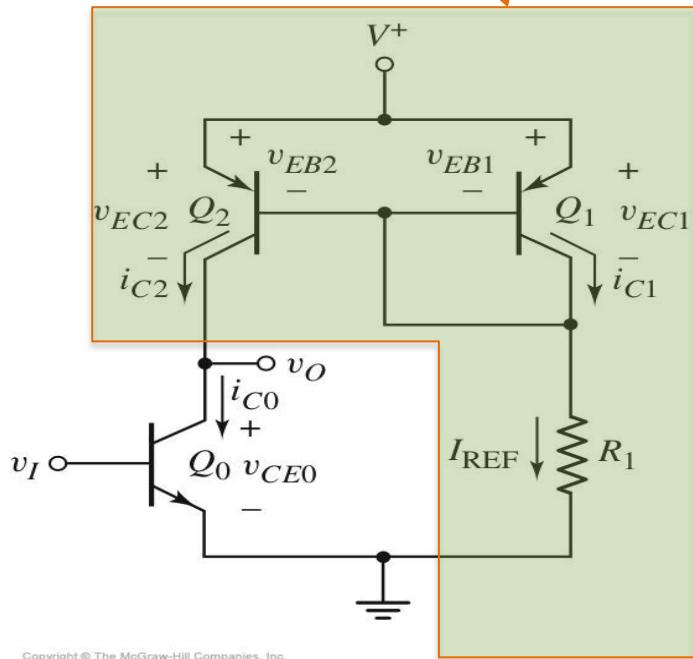
For a higher gain there should be a larger voltage drop across R_C

$$I_c = 6 \text{ mA} \quad R_c = 5 \text{ k}\Omega$$
$$A_{vS} = -\frac{6 \times 81}{26 \text{ m}}$$
$$A_{vS} \approx -230$$

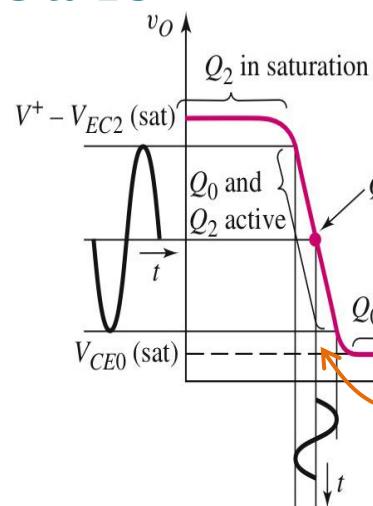


Circuits with Active Loads

PNP version of the 2-transistor current mirror



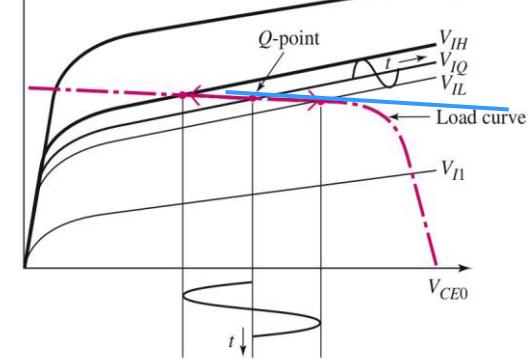
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Input signal region where Q0 and Q2 are in active region is very small. What is the effect of this type equation here.?

Load line for a discrete resistor of value

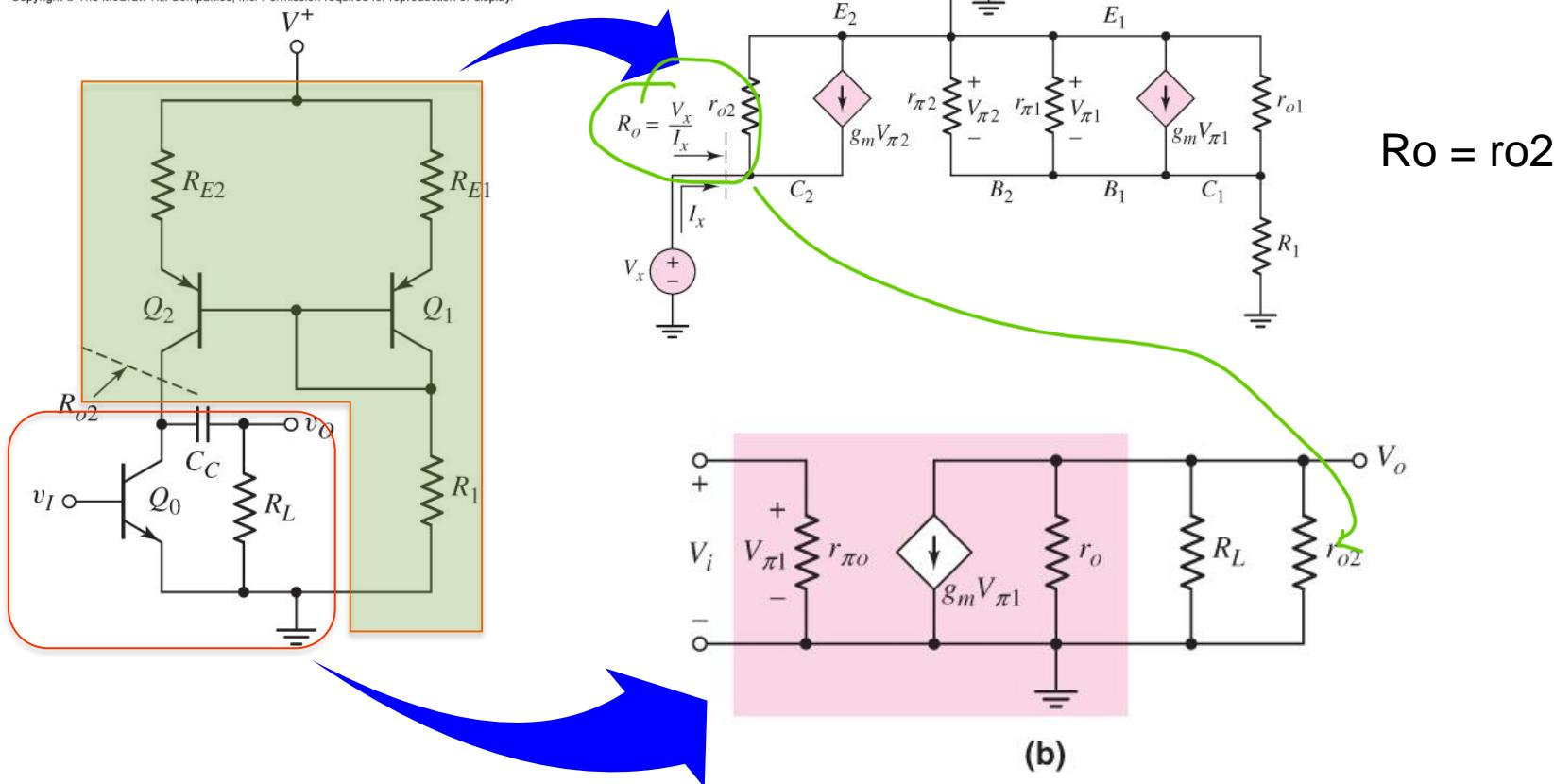
$$A_v = \frac{dv_o}{dv_i}$$



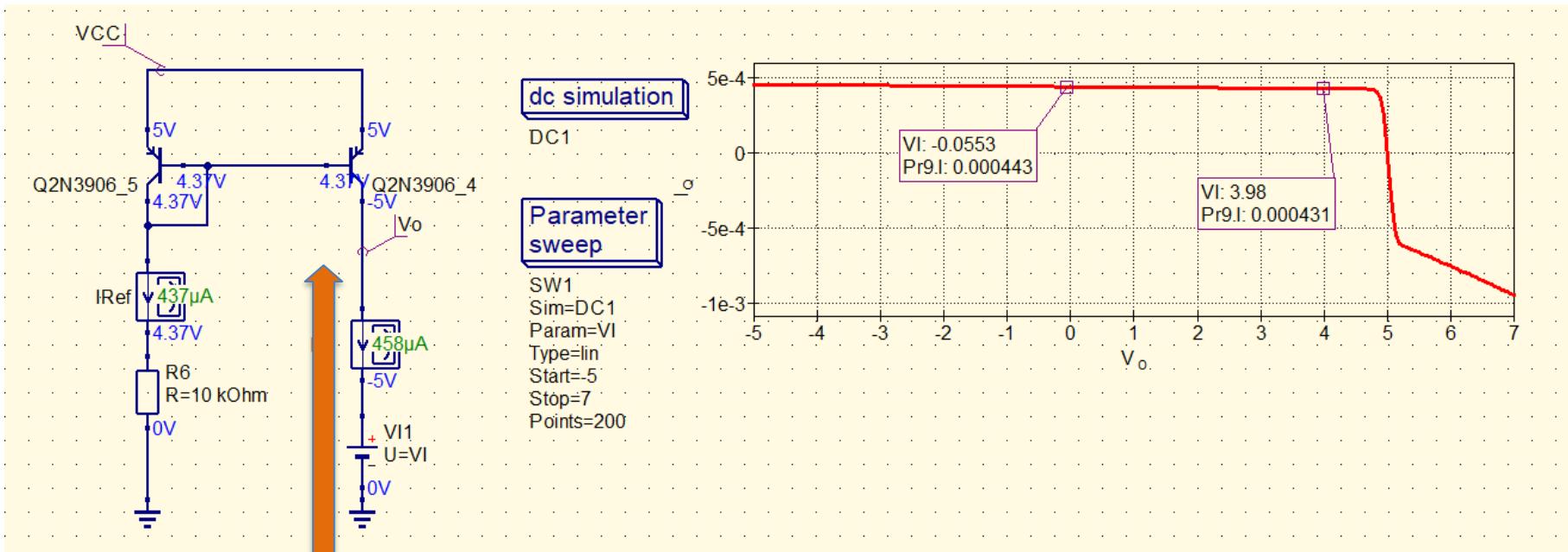
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Active Load Circuits: small-signal analysis

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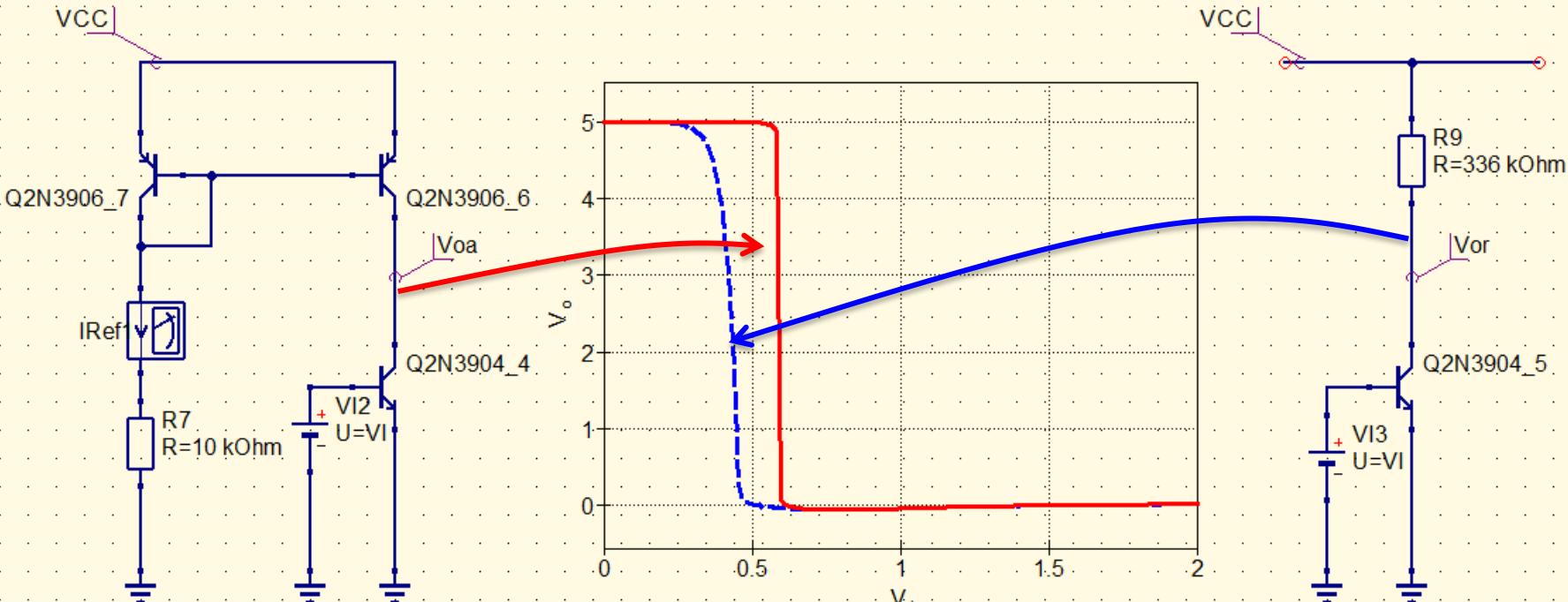


Active Load R_{in}



$$R_o = \left| \frac{-0.0553 - 3.98}{(443 - 431) \times 10^{-6}} \right| = 336 \text{ k}\Omega$$

CE Amplifier with an Active Load



$$A_v = \frac{dv_o}{dv_I}$$

6. Differential Amplifiers

Introduction

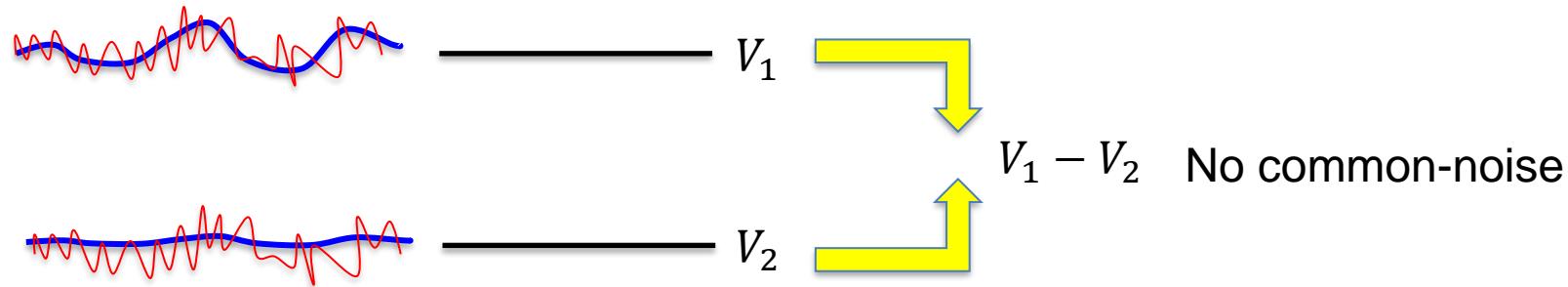
- Differential amplifiers are pervasive in analog electronics
 - Low/High frequency amplifiers
 - Operational amplifiers – the first stage is a differential amplifier
 - Analog modulators
 - Logic gates

□ Advantages

- Large input resistance;
- High gain;
- Differential input
- Good bias stability
- Excellent device parameter tracking in IC implementation

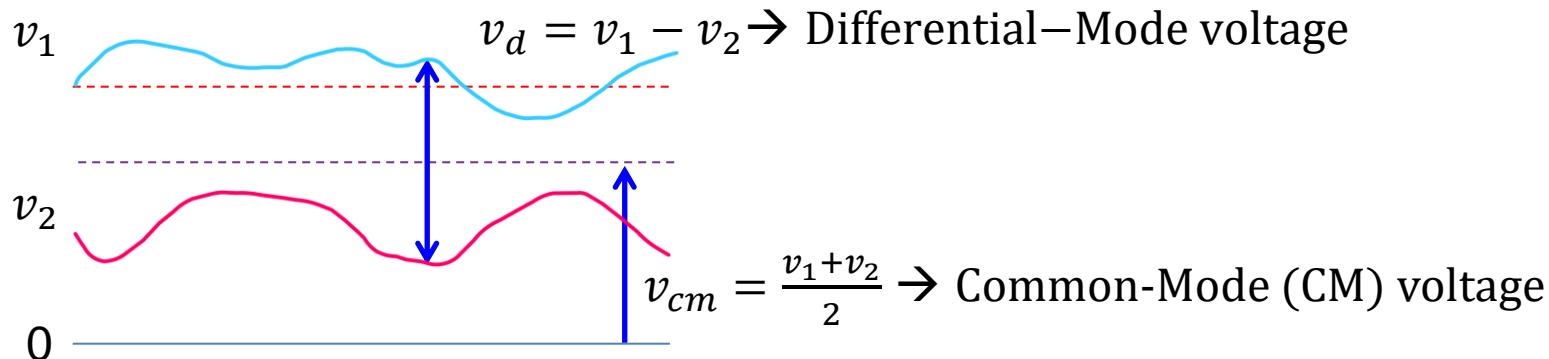
Why differential?

- Differential circuits are much less sensitive to noise and interferences



- Differential configuration enables us to bias amplifiers and connect multiple stages without using coupling or bypass capacitors
- Differential amplifiers are widely used in IC's
 - Excellent matching of transistors, which is critical for differential circuits
 - Differential circuits require more transistors à not an issue for IC

Differential Amplifier (DA): Input voltages

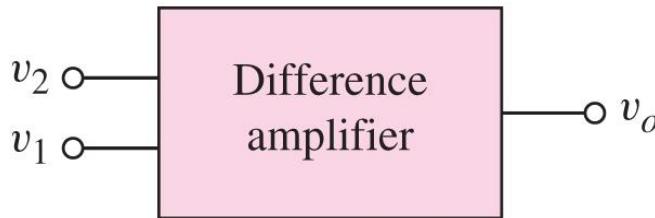


- ❑ If $v_1 = 10 \mu V$, $v_2 = -10 \mu V$, then $v_d = 20 \mu V$ and $v_{cm} = 0$
- ❑ If $v_1 = 110 \mu V$, $v_2 = 90 \mu V$, then $v_d = 20 \mu V$ and $v_{cm} = 100 \mu V$

If each pair of inputs applied to ideal diff. amplifier, v_o for each case would exactly be the same.

Amplifiers are not ideal, the CM signal does affect the output.

Differential Amplifier



From $v_d = v_1 - v_2$ and $v_{cm} = \frac{v_1 + v_2}{2}$,
we get $v_1 = v_{cm} + \frac{v_d}{2}$ and $v_2 = v_{cm} - \frac{v_d}{2}$

Assume that gain for v_1 and v_2 are different, and using linear approximation

$$v_o = A_1 v_1 + A_2 v_2$$

$$v_o = \underline{(A_1 + A_2)} v_{cm} + \underline{\frac{A_1 - A_2}{2}} v_d = A_{cm} v_{cm} + A_d v_d$$

Common Mode Gain (A_{cm})

Differential Mode gain (A_d)

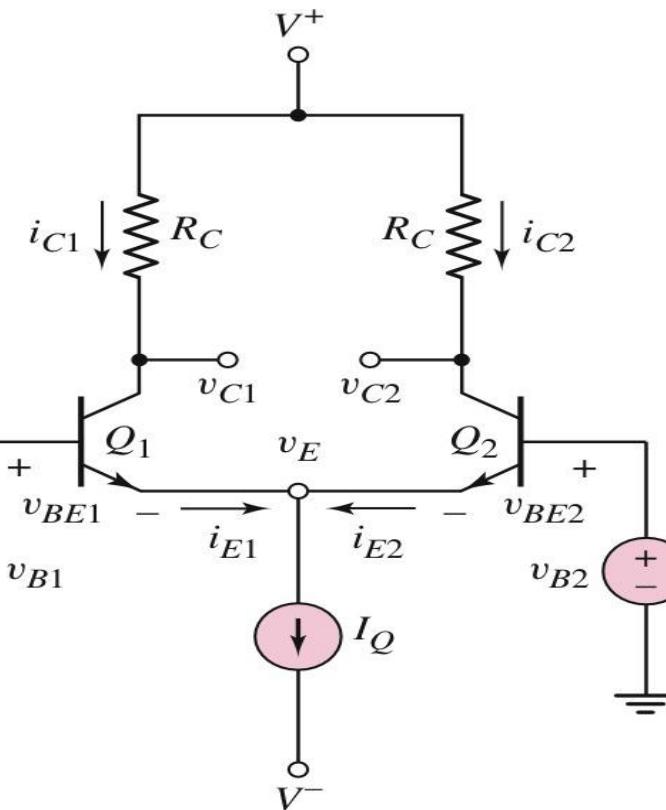
- From an Differential Amplifier, we expect, A_{cm} to be zero. In reality, it is not.
- We define **Common Mode Rejection Ratio (CMRR)** = $\left| \frac{A_d}{A_{cm}} \right|$ usually given in dB

BJT Differential Amplifier Topology

Two matched transistors (Q1 and Q2) joined and biased by a constant current source I which is implemented by current mirror

Q1 and Q2 must stay in active region

No C_c 's for inputs.
The amplifier is current biased.



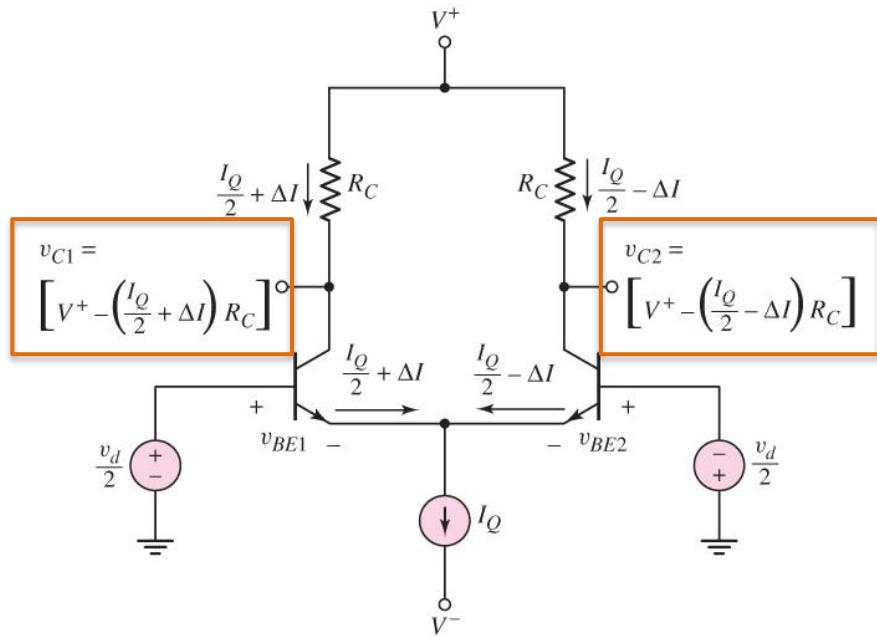
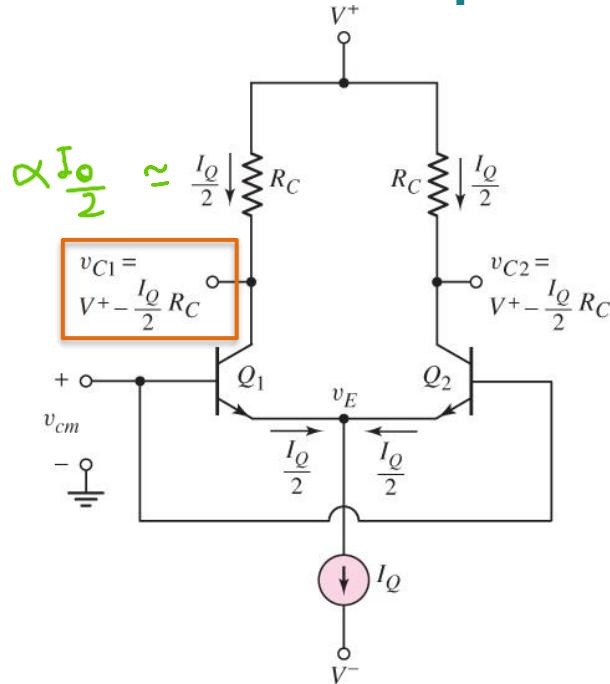
$$V_{B1} = \frac{v_d}{2} \text{ and } V_{B2} = -\frac{v_d}{2}$$

Assuming $V_b \approx 0$,
Q1 and Q2 are FA due to
current source
 $V_E \approx -0.7V$

Base currents are negligible.

$$I_{E2} = I_{E1} = \frac{I_Q}{2}$$

CM and DM outputs



$$v_{C2} - v_{C1} = \left[V^+ - \left(\frac{I_{CQ}}{2} - \Delta I \right) R_C \right] - \left[V^+ - \left(\frac{I_{CQ}}{2} + \Delta I \right) R_C \right] = 2\Delta I R_C$$

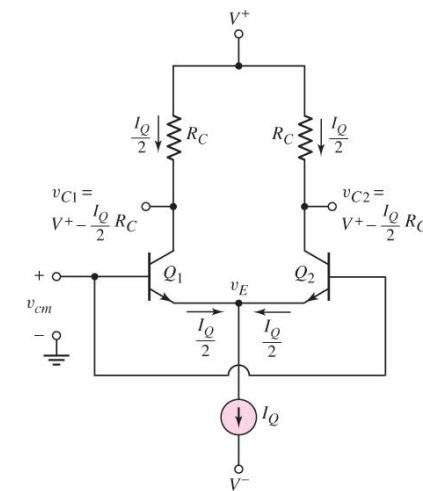
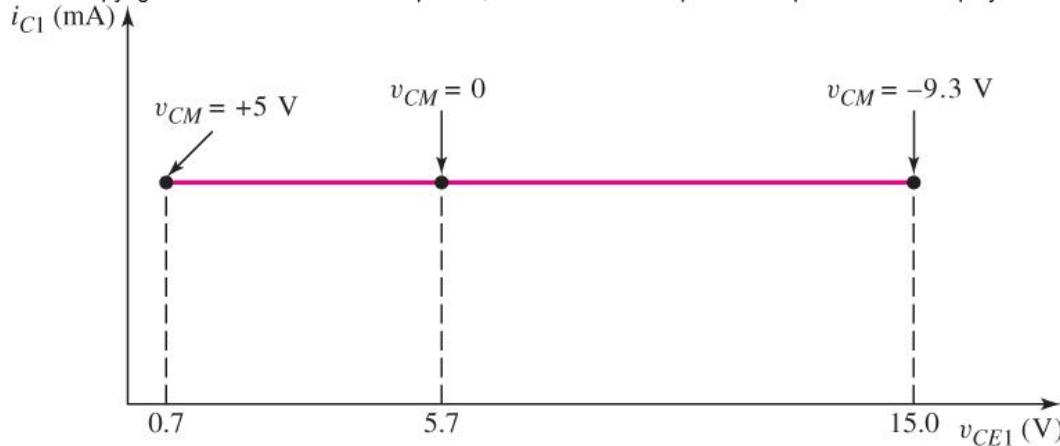
A voltage difference is created for a differential input!

CM input limitation

Objective: Determine the quiescent collector current and collector-emitter voltage in a difference amplifier.

Consider the diff-amp in Figure 11.2, with circuit parameters: $V^+ = 10$ V, $V^- = -10$ V, $I_Q = 1$ mA, and $R_C = 10$ k Ω . The transistor parameters are: $\beta = \infty$ (neglect base currents), $V_A = \infty$, and $V_{BE}(\text{on}) = 0.7$ V. Determine i_{C1} and v_{CE1} for common-mode voltages $v_{B1} = v_{B2} = v_{CM} = 0, -5$ V, and $+5$ V.

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As the v_{CM} varies, V_{CE} changes.
Q-point changes.

There is a limit in v_{CM} over which Q1 and Q2 remains in Active region

If $v_{CM} > 5$ V, Q1 and Q2 would be driven into saturation

DA DC transfer characteristics

$$i_{c_1} = I_s e^{\frac{v_{BE1}}{V_T}}$$

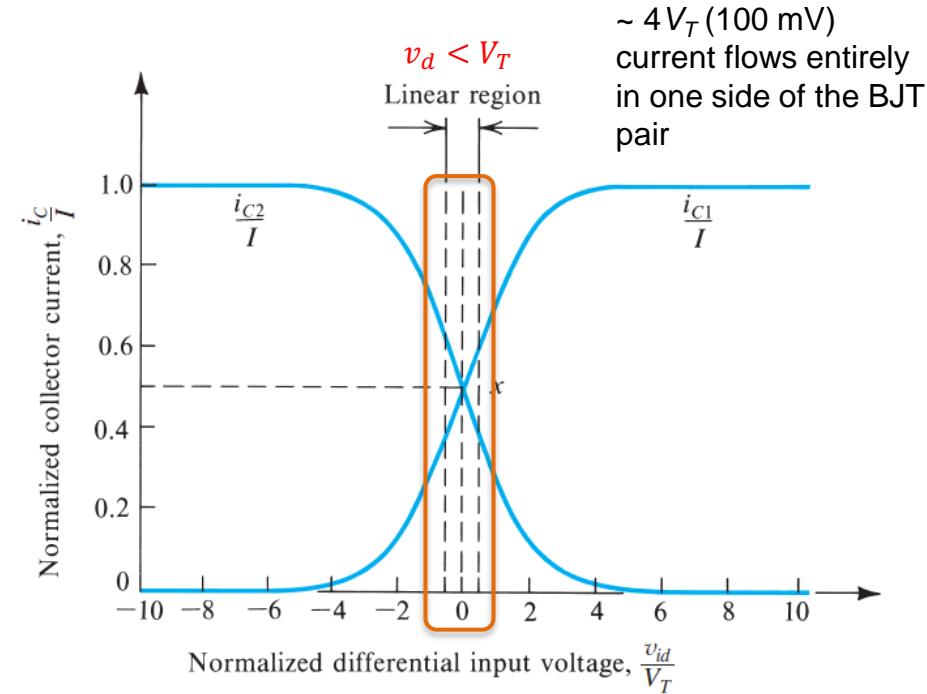
$$i_{c_2} = I_s e^{\frac{v_{BE2}}{V_T}}$$

$$I_a \approx i_{c_1} + i_{c_2} = I_s [e^{\frac{v_{BE1}}{V_T}} + e^{\frac{v_{BE2}}{V_T}}]$$

Now $\frac{i_{c_1}}{I_a} = \frac{1}{1 + e^{\frac{(v_{BE2} - v_{BE1})}{V_T}}}$

$\frac{i_{c_1}}{I_a} = \frac{1}{1 + e^{-\frac{v_d}{V_T}}}$

Similarly $i_{c_2} = \frac{I_a}{1 + e^{\frac{v_d}{V_T}}}$



6 Transfer characteristics of the BJT differential pair of Fig. 9.14 assuming $\alpha \approx 1$.

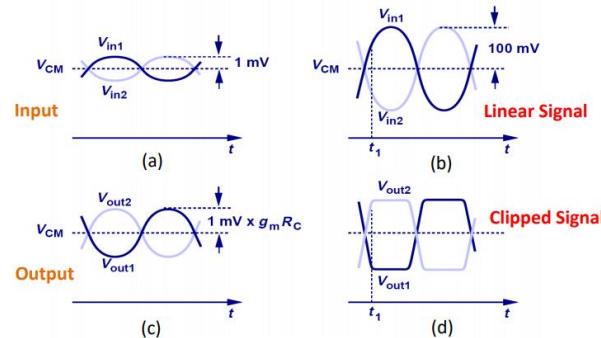
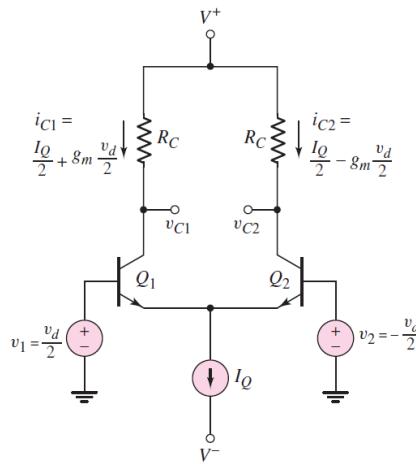
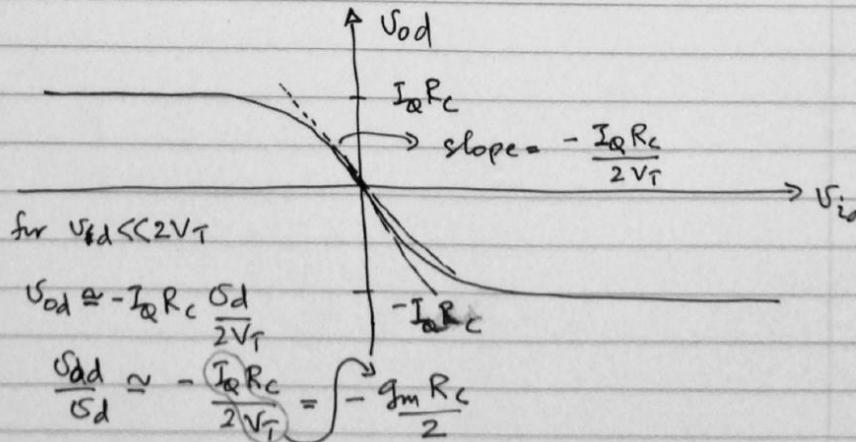
Optimum DC Operating region for Amplification

DA DC transfer characteristics

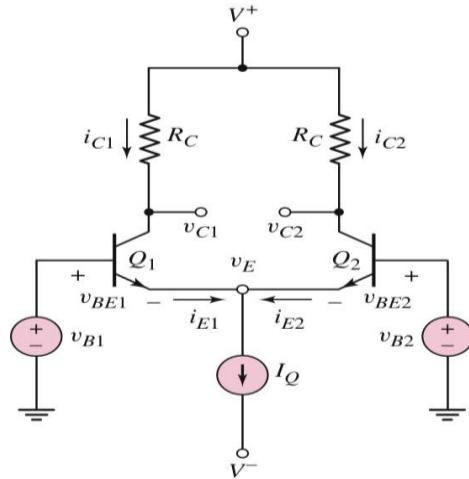
$$i_{E_1} = \frac{I_Q}{1 + e^{-\frac{V_d}{2V_T}}} \quad \text{and} \quad i_{E_2} = \frac{I_Q}{1 + e^{\frac{V_d}{2V_T}}}$$

$$i_{E_1} - i_{E_2} = I_Q \tanh\left(\frac{V_d}{2V_T}\right)$$

$$V_{od} = V_{c_2} - V_{c_1} = -I_Q R_C \tanh\left(\frac{V_d}{2V_T}\right)$$



Differential Amplifier AC Analysis: Emitter Voltage



$$r_{\pi 1} = r_{\pi 2} \equiv r_{\pi} \quad \text{and} \quad g_{m1} = g_{m2} \equiv g_m$$

Writing a KCL equation at node V_e , using phasor notation, we have

$$\frac{V_{\pi 1}}{r_{\pi}} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_{\pi}} = \frac{V_e}{R_o} \quad (1)$$

or

$$V_{\pi 1} \left(\frac{1 + \beta}{r_{\pi}} \right) + V_{\pi 2} \left(\frac{1 + \beta}{r_{\pi}} \right) = \frac{V_e}{R_o} \quad (1)$$

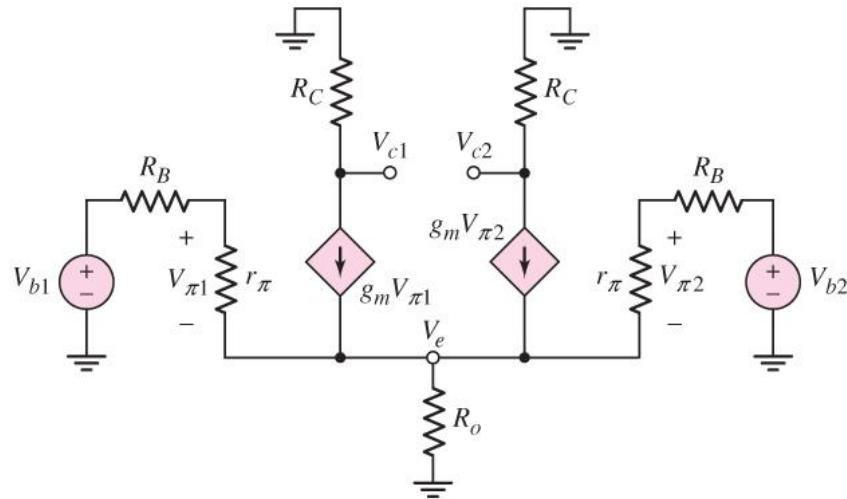
where $g_m r_{\pi} = \beta$. From the circuit, we see that

$$\frac{V_{\pi 1}}{r_{\pi}} = \frac{V_{b1} - V_e}{r_{\pi} + R_B} \quad \text{and} \quad \frac{V_{\pi 2}}{r_{\pi}} = \frac{V_{b2} - V_e}{r_{\pi} + R_B}$$

Solving for $V_{\pi 1}$ and $V_{\pi 2}$ and substituting into Equation (1), we find

$$(V_{b1} + V_{b2} - 2V_e) \left(\frac{1 + \beta}{r_{\pi} + R_B} \right) = \frac{V_e}{R_o}$$

Solving for V_e , we obtain

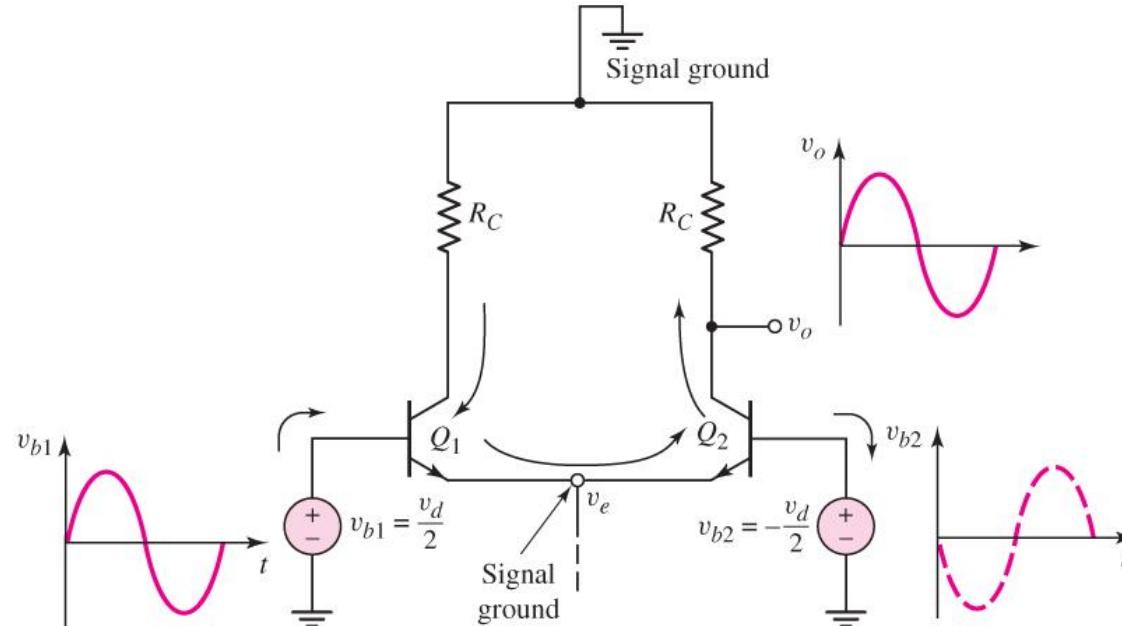


$$V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_{\pi} + R_B}{(1 + \beta)R_o}}$$

DM Inputs and Emitter Voltage

$$V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{(1 + \beta)R_o}}$$

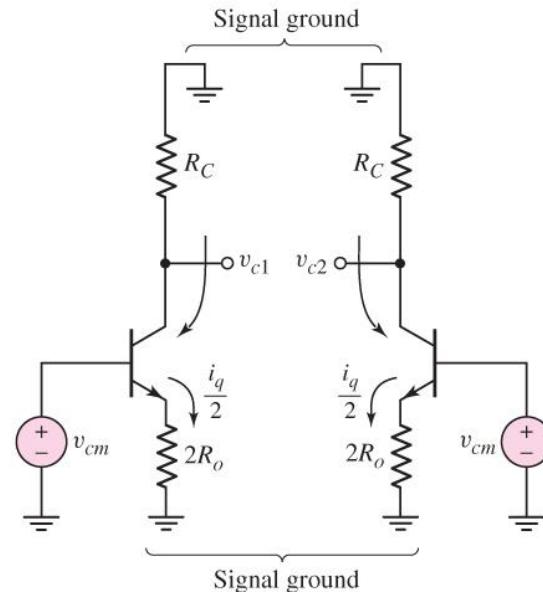
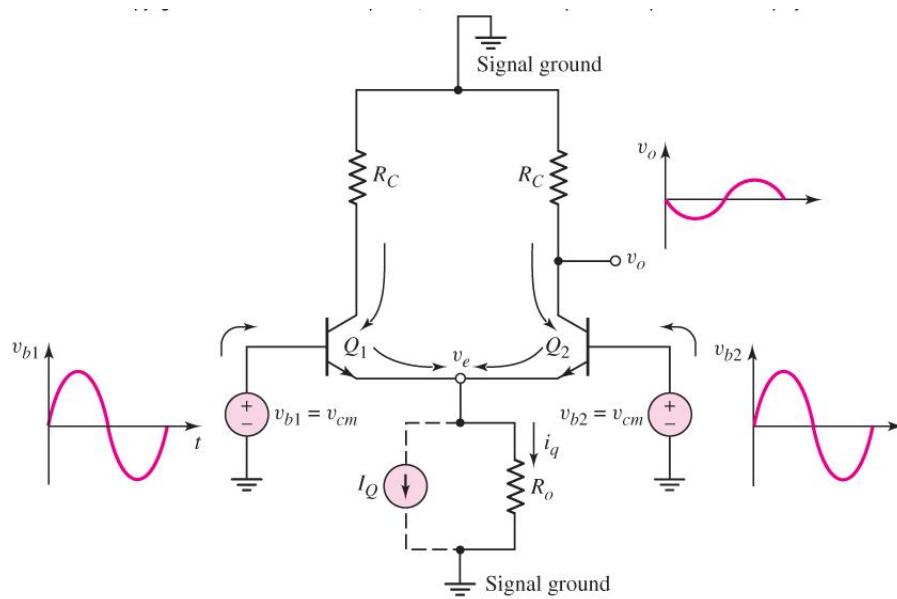
For DM inputs: $V_{b1} = -V_{b2} = \frac{V_d}{2} \rightarrow V_e \approx 0$
(emitter node is a virtual GND for DM signals)



CM Inputs and Emitter Voltage

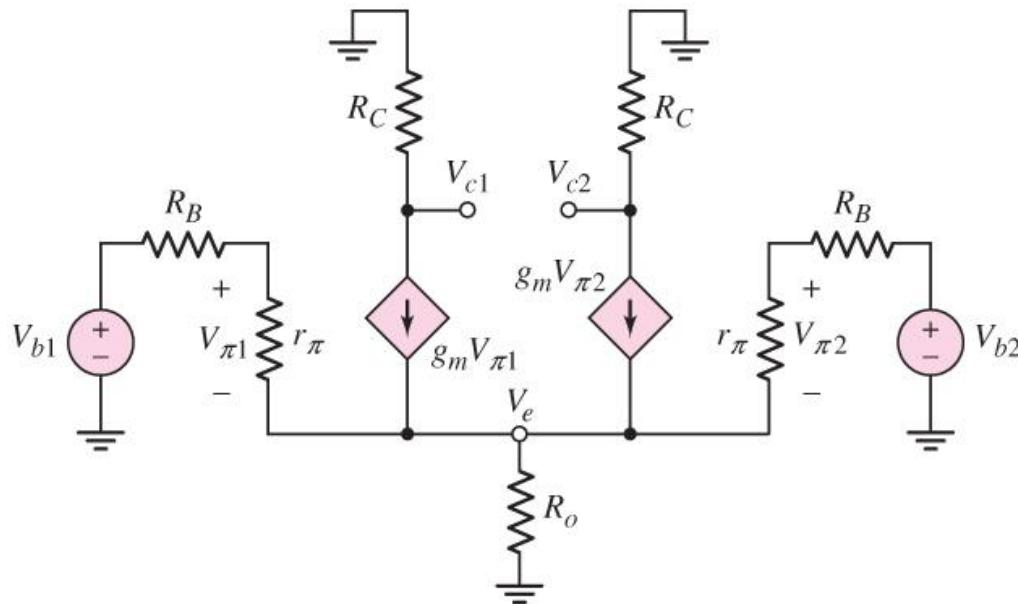
$$V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{(1 + \beta)R_o}}$$

For CM inputs: $V_{b1} = V_{b2} = V_{CM} \rightarrow V_e \neq 0$



Voltage Gain for Two-sided output

- For two-sided outputs: $V_o = V_{c2} - V_{c1}$

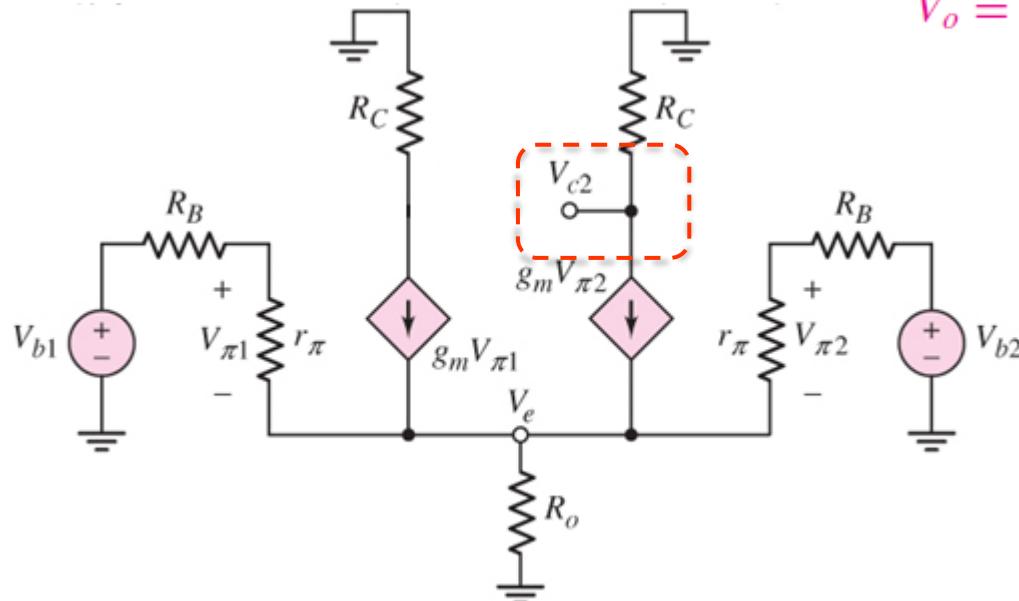


$$A_d = \frac{\beta R_C}{r_\pi + R_B}$$

$$A_{cm} = 0$$

Voltage Gain for Single-Sided Output

- If either v_{c1} or v_{c2} is used alone as output, output is said to be single-ended.



$$V_o = V_{c2} = -(g_m V_{\pi 2}) R_C = -\frac{\beta R_C (V_{b2} - V_e)}{r_\pi + R_B}$$

Assuming $R_o \rightarrow \infty$

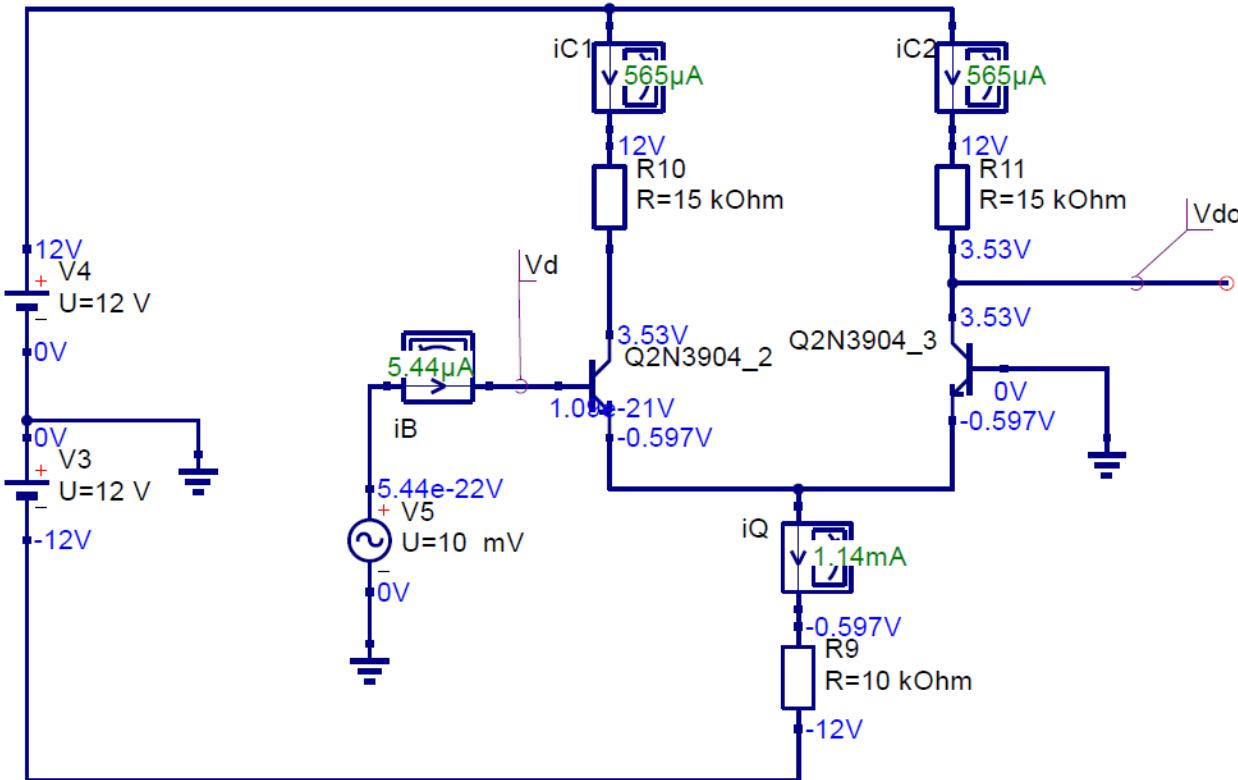
$$V_o = -\frac{\beta R_C (V_{b2} - V_{b1})}{2(r_\pi + R_B)}$$

$$A_d = \frac{V_o}{V_d} = \frac{\beta R_C}{2(r_\pi + R_B)}$$

$$A_{cm} = \frac{-\beta R_C}{r_\pi + R_B + 2(1 + \beta)R_o}$$

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = \frac{1}{2} \left[1 + \frac{2(1 + \beta)R_o}{r_\pi + R_B} \right]$$

Simulation Case-Study: DC Analysis



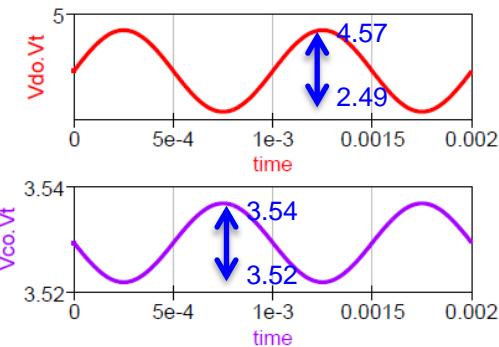
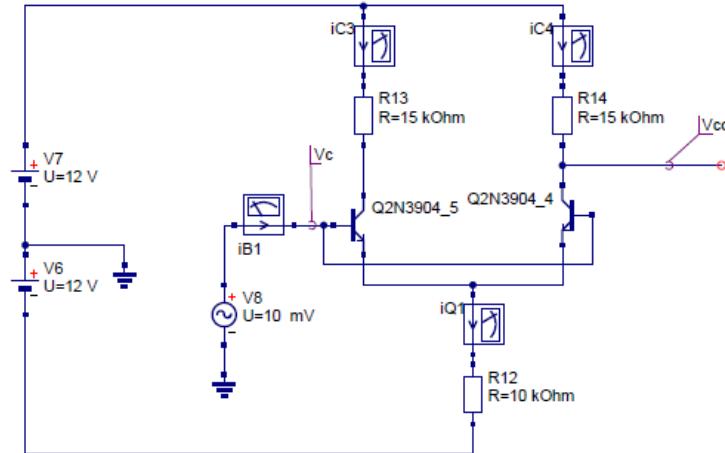
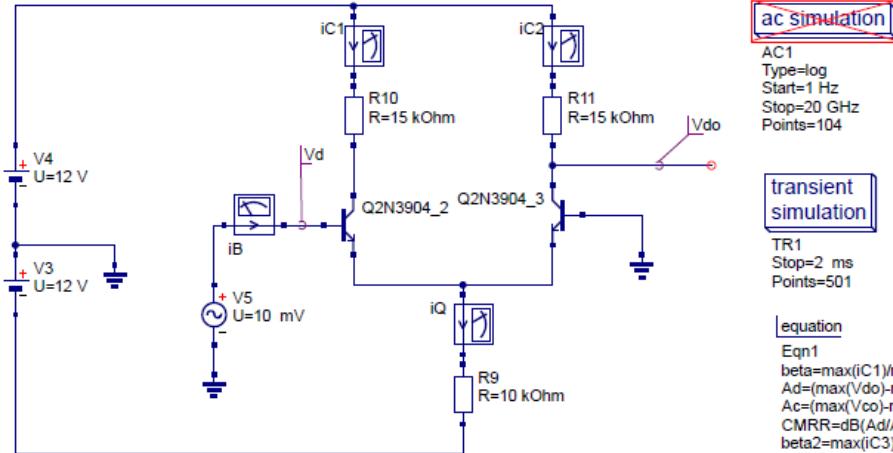
From Calculations:

$$\beta = 565/5.44 = 129$$

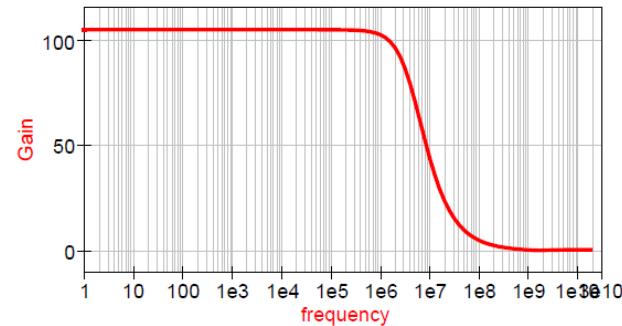
$$I_Q = 1.14 \text{ mA}$$

$$I_C = 0.565 \text{ mA}$$

Simulation Case-Study: AC Analysis

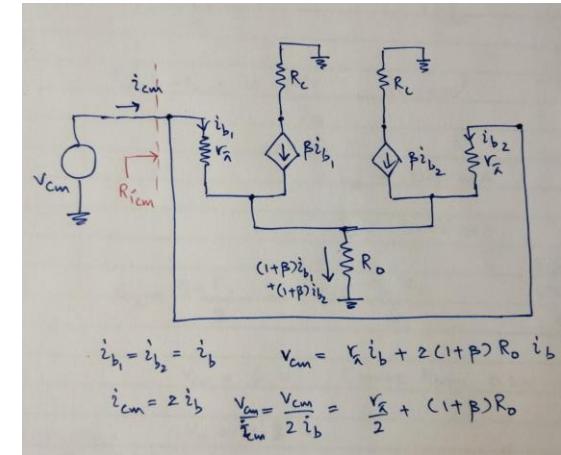
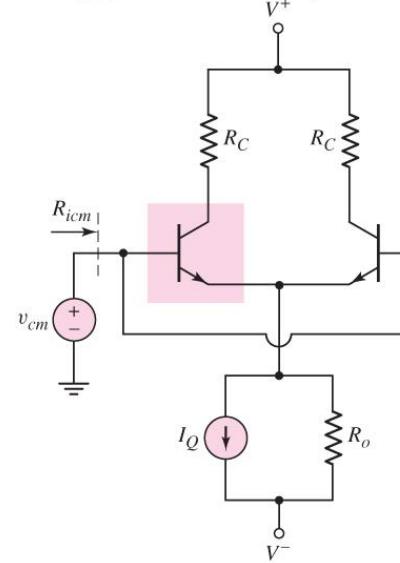
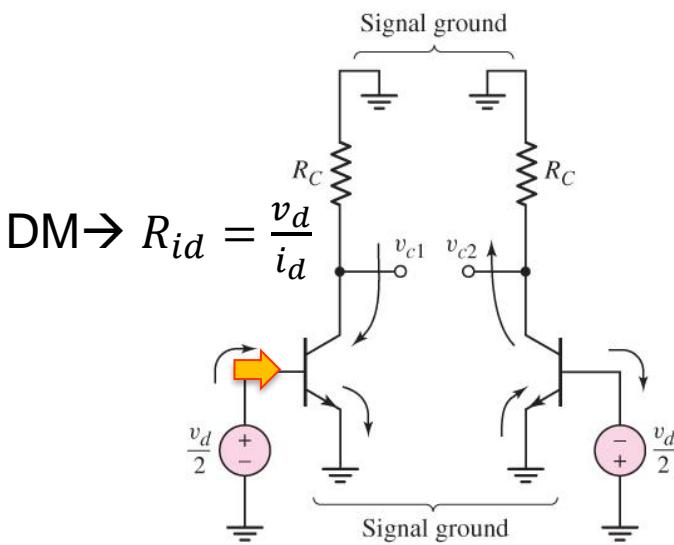


	Model	Simulation
A_{dm}	163	105
A_{cm}	0.525	0.742
$CMRR$	49.8 dB	43 dB



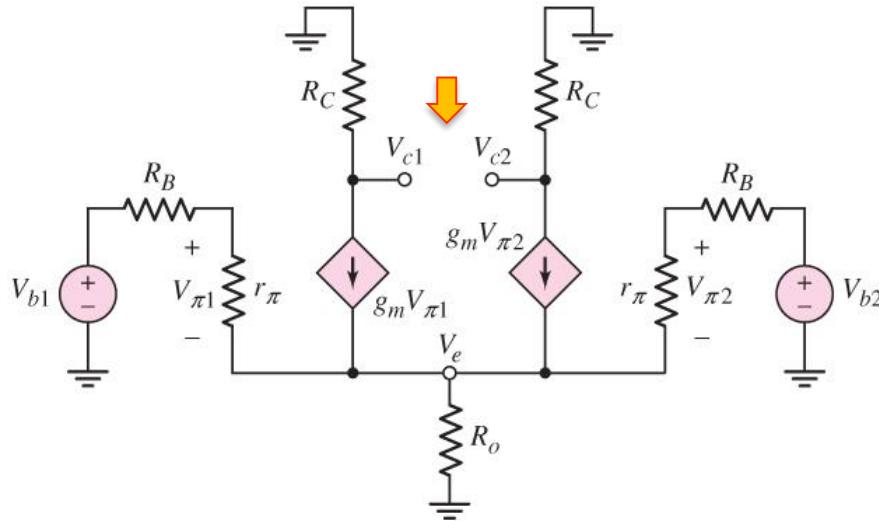
Differential- and Common-Mode Input Impedances

- R_{in} of an amplifier is as important a property as the voltage gain.
 - determines the loading effect of the circuit on the signal source.

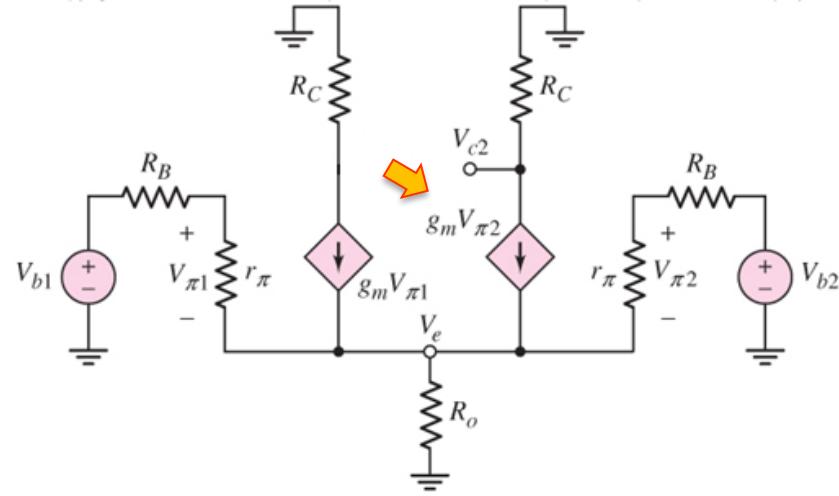


Output Impedances

- R_o is the impedance seen by the output

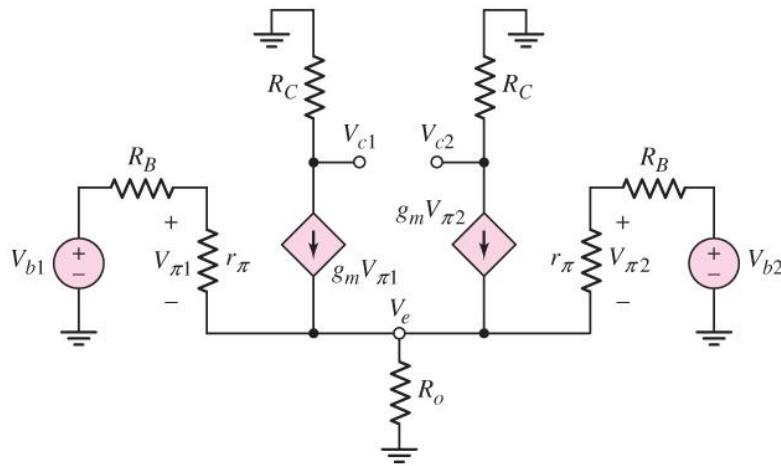


In DM $\rightarrow R_o$ is the resistance seen by
between V_{c1} and V_{c2}
 $R_{od} = 2(R_c // R_o) \approx 2R_c$



In SE $\rightarrow R_o$ is the resistance seen by
between V_{c1} (or V_{c2})
 $R_{od} = (R_c // R_o) \approx R_c$

Effect of RC Mismatch—Two-Sided Output



Effect of R_C Mismatch—Two-Sided Output

We assume that R_{C1} and R_{C2} are the resistors in the collectors of Q_1 and Q_2 . If the two resistors are not matched, we assume that we can write $R_{C1} = R_C + \Delta R_C$ and $R_{C2} = R_C - \Delta R_C$. For simplicity, let $R_B = 0$.

From Figure 11.9, the output voltage for a two-sided output is given by

$$V_o = V_{c2} - V_{c1} = (-g_m V_{\pi 2} R_{C2}) - (-g_m V_{\pi 1} R_{C1}) \quad (11.37)$$

We also see from the figure (with $R_B = 0$) that $V_{\pi 1} = V_{b1} - V_e$ and $V_{\pi 2} = V_{b2} - V_e$. Using the expressions for V_e (Equation (11.24)), V_{b1} (Equation (11.29(a))), and V_{b2} (Equation (11.29(b))), we find the differential voltage gain as

$$A_d = g_m R_C \quad (11.38)$$

and the common-mode gain as

$$A_{cm} = g_m (2\Delta R_C) \cdot \frac{1}{\left[1 + \frac{2(1+\beta)R_o}{r_{\pi}} \right]} \quad (11.39)$$

In general, $2(1+\beta)R_o/r_{\pi} \gg 1$, so that

$$A_{cm} \cong g_m (2\Delta R_C) \cdot \frac{r_{\pi}}{2(1+\beta)R_o} \quad (11.40(a))$$

Noting that $g_m r_{\pi} = \beta$ and $\beta/(1+\beta) \cong 1$, we have the common-mode gain as

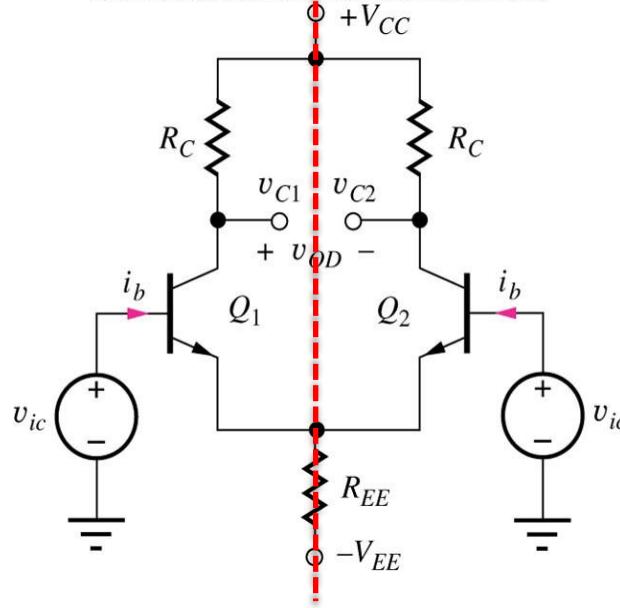
$$A_{cm} \cong \frac{\Delta R_C}{R_o} \quad (11.40(b))$$

Resistor mismatch affects the A_{cm}

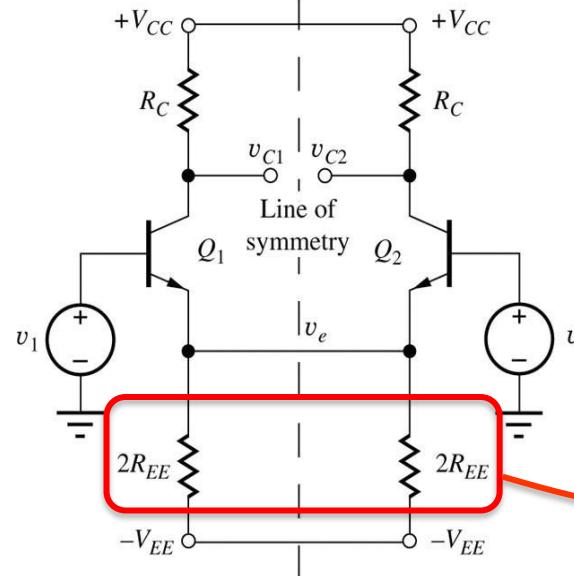
Therefore, for good CMRR
 R_o should be maximised.

Half-Circuit Analysis

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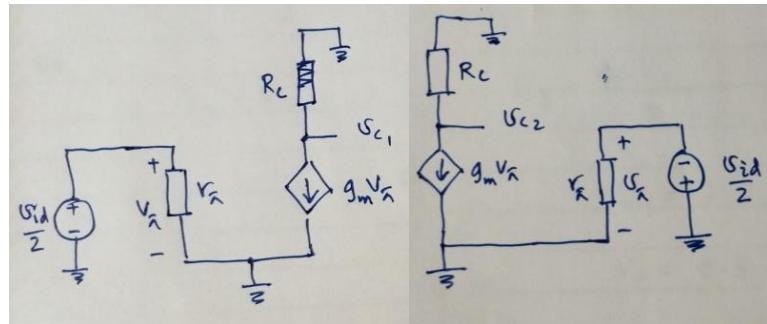
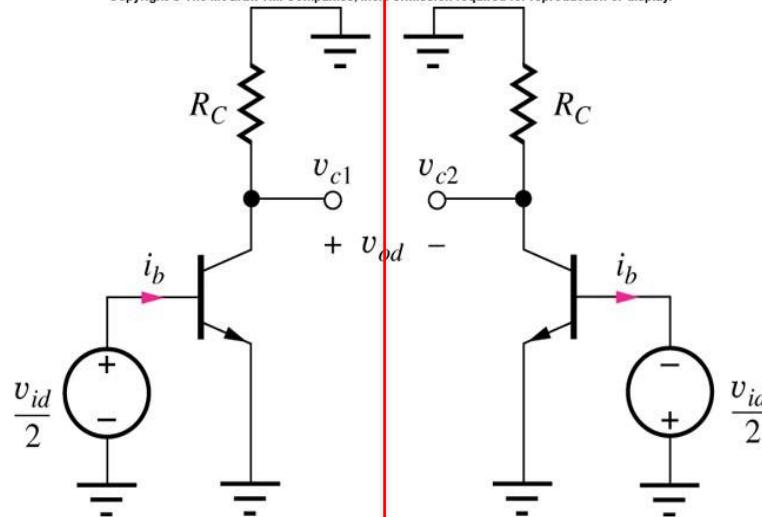
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- ❑ For DM analysis: Node v_e , V_{CC} and V_{EE} are grounds.
- ❑ For CM analysis: Take only one half of the circuit through the symmetrical line.

Half-Circuit Analysis: Differential Mode

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Node Ve, VCC and VEE are grounds.

$$v_{c1} = -g_m v_A R_C = -g_m R_C \frac{v_{id}}{2}$$

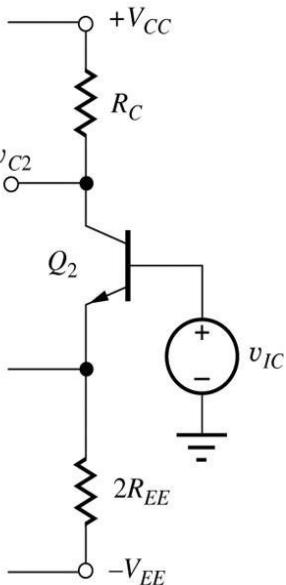
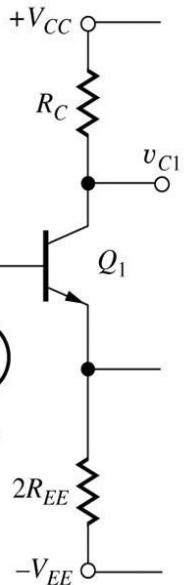
$$v_{c2} = g_m R_C \frac{v_{id}}{2}$$

$$A_d = \frac{v_{c1} - v_{c2}}{\frac{v_{id}}{2} - (-\frac{v_{id}}{2})} = \frac{v_{c1} - v_{c2}}{v_{id}}$$

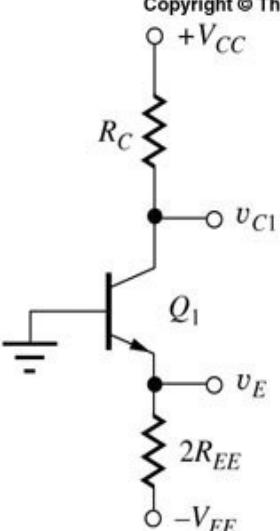
$$A_d = -g_m R_C$$

Half-Circuit Analysis: Common Mode

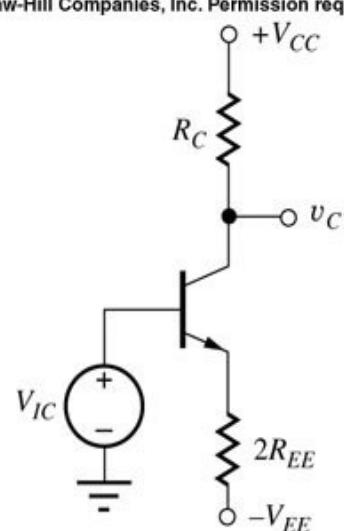
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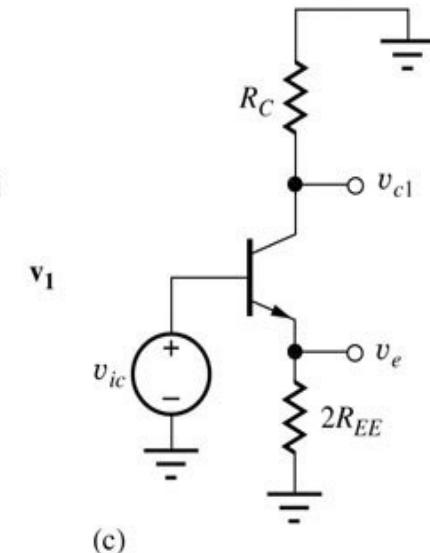


(a)



(b)

DC circuit

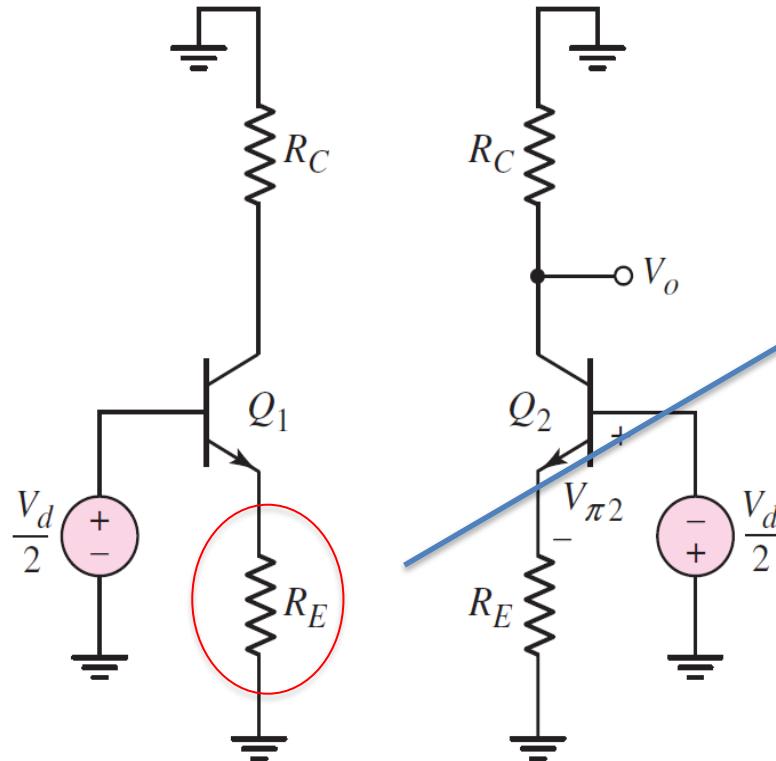


(c)

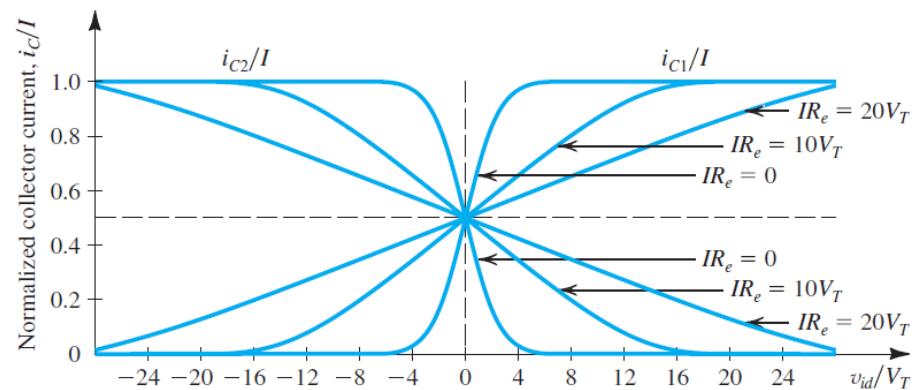
AC circuit

- Similar to a CE Amplifier → AC-gain = $\frac{R_C}{2R_{EE}}$

Differential Amplifier with Emitter Degeneration

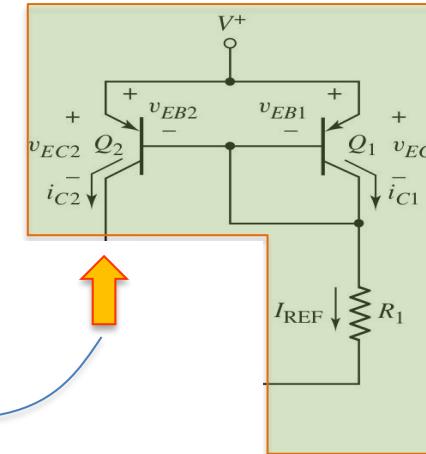
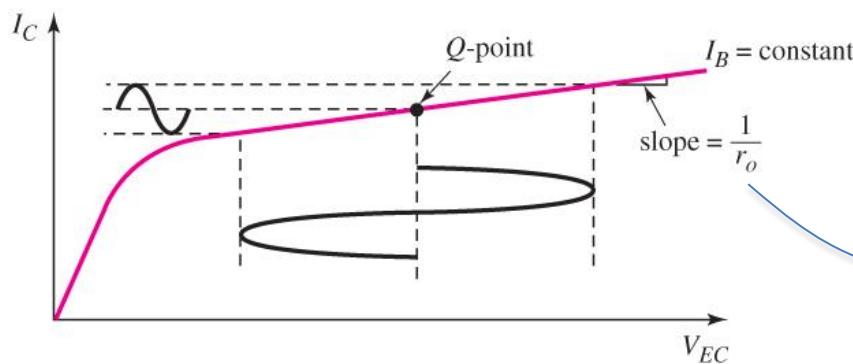


Additional Emitter resistance. Why?
What are the advantages and
disadvantages?



Differential Amplifier with Active Load

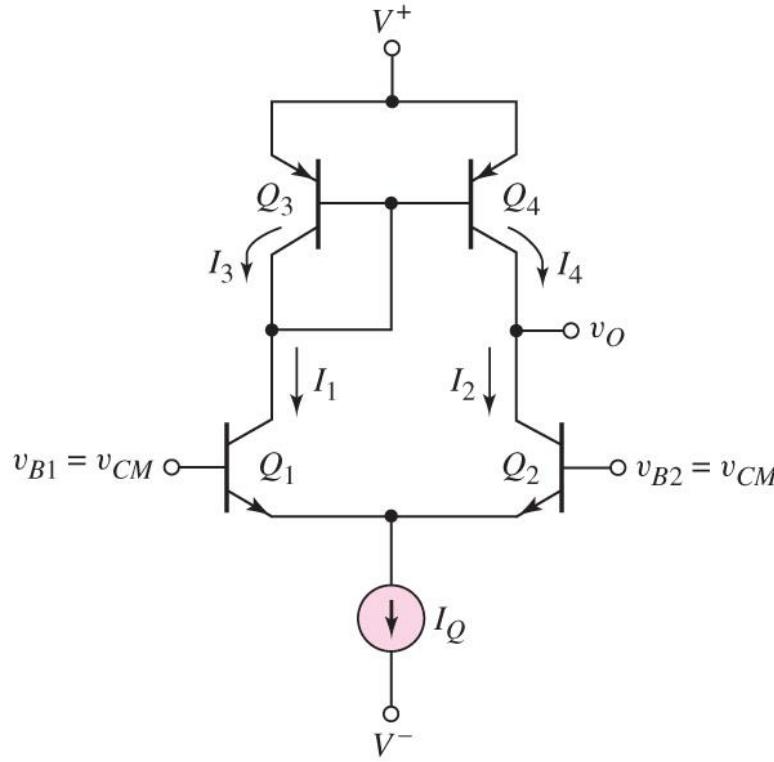
- Active loads can also be used in diff-amp circuits to increase the differential-mode gain ($A_d \propto R_c$).



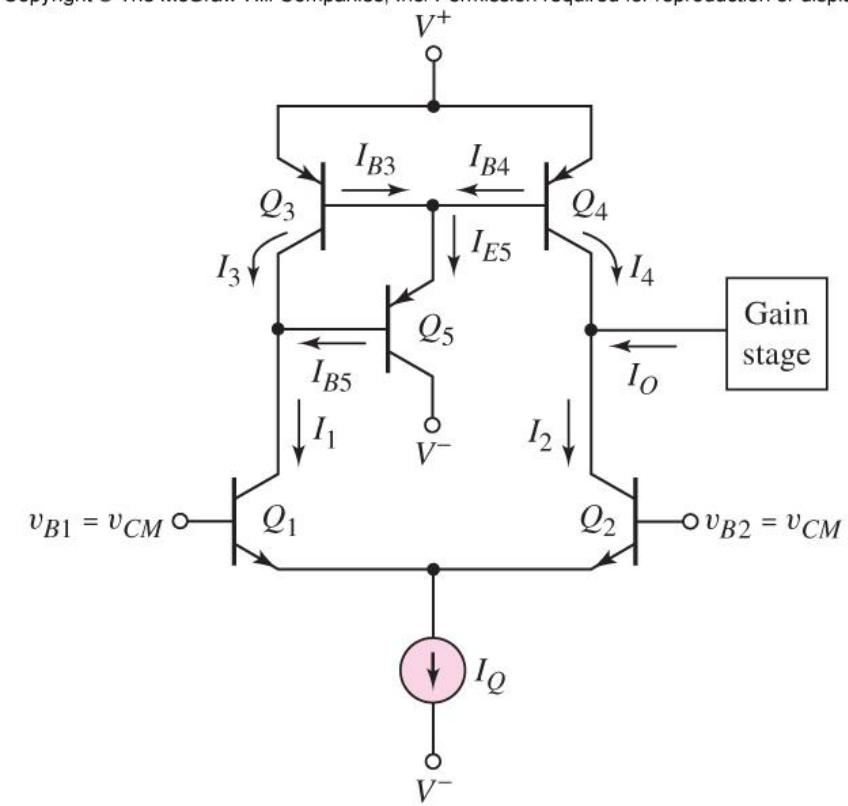
Typically, r_o is much larger than that of a discrete resistive load, so A_d will be larger with the active load.

Differential Amplifier with Active Load

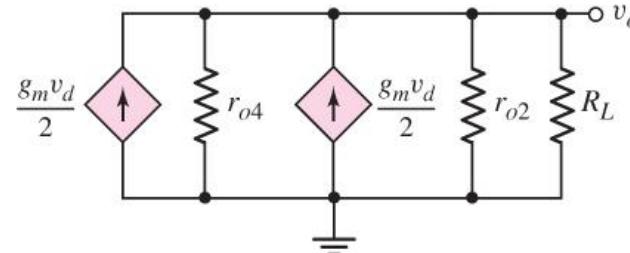
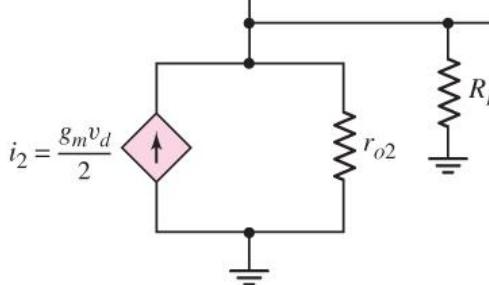
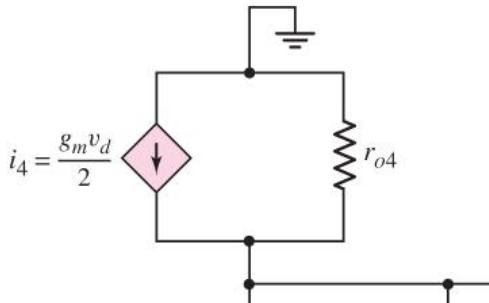
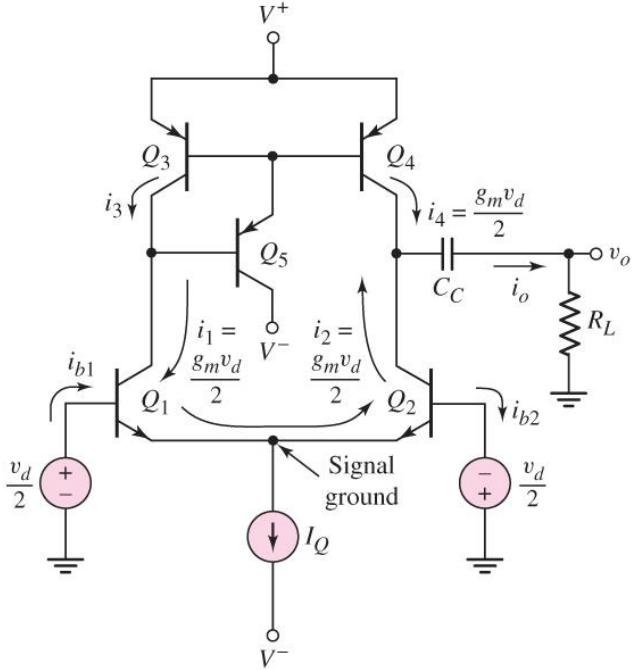
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Small-Signal Analysis of BJT Active Load



$$v_o = 2 \left(\frac{g_m v_d}{2} \right) (r_{o2} \| r_{o4} \| R_L)$$

and the small-signal differential-mode voltage gain is

$$A_d = \frac{v_o}{v_d} = g_m (r_{o2} \| r_{o4} \| R_L)$$

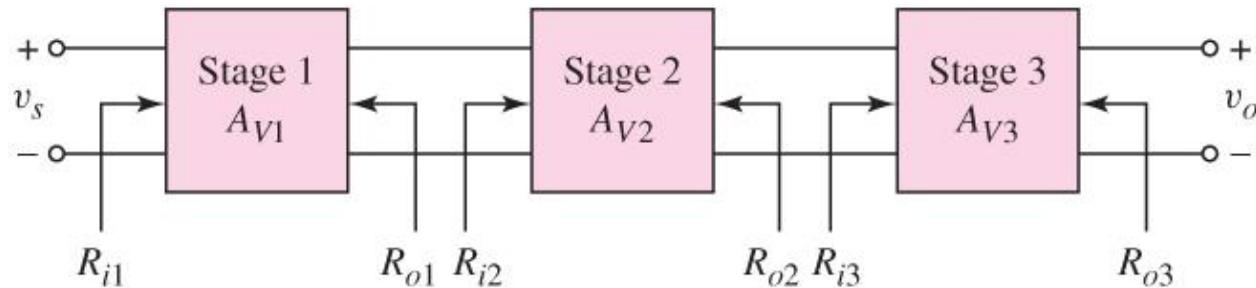
Equation (11.99) can be rewritten in the form

$$A_d = \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}} + \frac{1}{R_L}} = \frac{g_m}{g_{o2} + g_{o4} + G_L}$$

7. Multistage Amplifiers

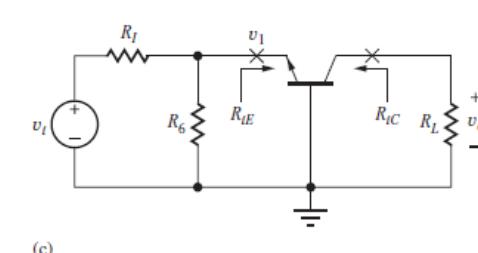
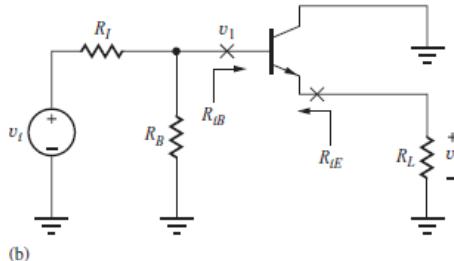
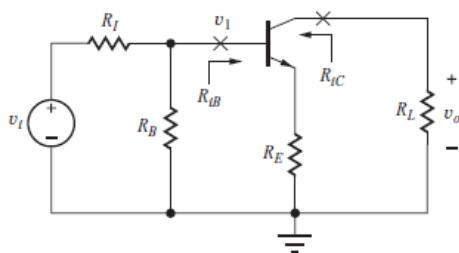
Multistage Amplifiers

- ❑ Amplifier circuits can be connected in series, or cascaded.
- ❑ To achieve
 - a gain which is not possible from a single stage
 - input/output resistance



- ❑ It is important to note that the input resistance of the follow-on stage becomes the load of the previous stage
- ❑ Overall gain $(A_v) = A_{v1} \dots A_{vn}$?

BJT Amplifier Family



COMMON-EMITTER AMPLIFIER

$$\text{Terminal voltage gain } A_{vt} = \frac{v_o}{v_i} \cong -\frac{g_m R_L}{1 + g_m R_E} > 1$$

Signal-source voltage gain

$$A_v = \frac{v_o}{v_i} = -\frac{g_m R_L}{1 + g_m R_E} \left[\frac{R_B \| R_{iB}}{R_I + (R_B \| R_{iB})} \right]$$

Input terminal resistance

$$r_\pi + (\beta_o + 1)R_E \quad \text{High}$$

$$\cong r_\pi (1 + g_m R_E)$$

Output terminal resistance

$$r_o(1 + g_m R_E) \quad \text{Medium}$$

Input signal range

$$\cong 0.005(1 + g_m R_E)$$

Terminal current gain

$$-\beta_o > 1$$

COMMON-COLLECTOR AMPLIFIER

$$\cong +\frac{g_m R_L}{1 + g_m R_L} \cong +1$$

$$+ \frac{g_m R_L}{1 + g_m R_L} \left[\frac{R_B \| R_{iB}}{R_I + (R_B \| R_{iB})} \right] \cong +1$$

COMMON-BASE AMPLIFIER

$$+g_m R_L > 1$$

$$+ \frac{g_m R_L}{1 + g_m (R_I \| R_4)} \left(\frac{R_6}{R_I + R_6} \right)$$

$$\frac{\alpha_o}{g_m} \cong \frac{1}{g_m} \quad \text{Low}$$

$$r_\pi + (\beta_o + 1)R_L \quad \text{High}$$

$$\cong r_\pi (1 + g_m R_L)$$

$$r_o [1 + g_m (R_I \| R_4)] \quad \text{Medium}$$

$$\frac{\alpha_o}{g_m} + \frac{R_{th}}{\beta_o + 1} \quad \text{Low}$$

$$\cong 0.005[1 + g_m (R_I \| R_6)]$$

$$\beta_o + 1 > 1$$

$$\alpha_o \cong +1$$

Multi-Stage Amplifier Gain

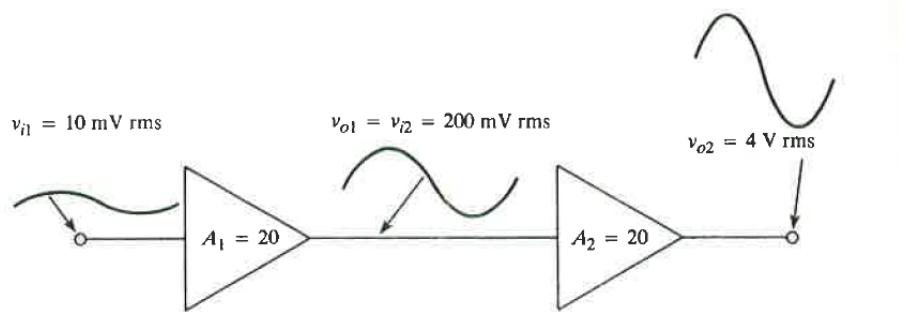
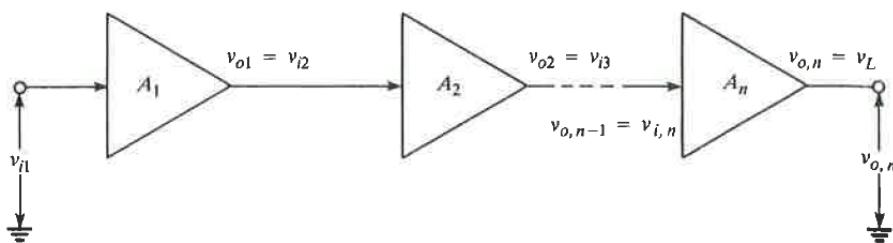


Figure 11.1 Two amplifier stages connected in cascade



- Why gain is usually given in dB ?

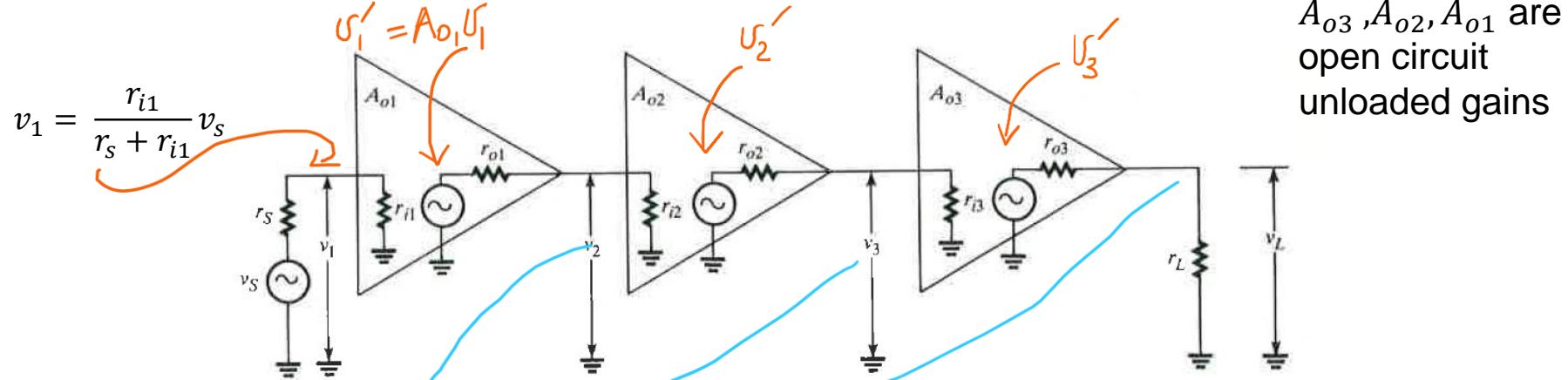
$$A_v = A_{v1} A_{v2} \dots A_{vn}?$$

$$20 \log A_S = 20 \log (A_{S1} A_{S2} \dots A_{Sn})$$

$$= 20 \log (A_{S1}) + \dots + 20 \log (A_{Sn})$$

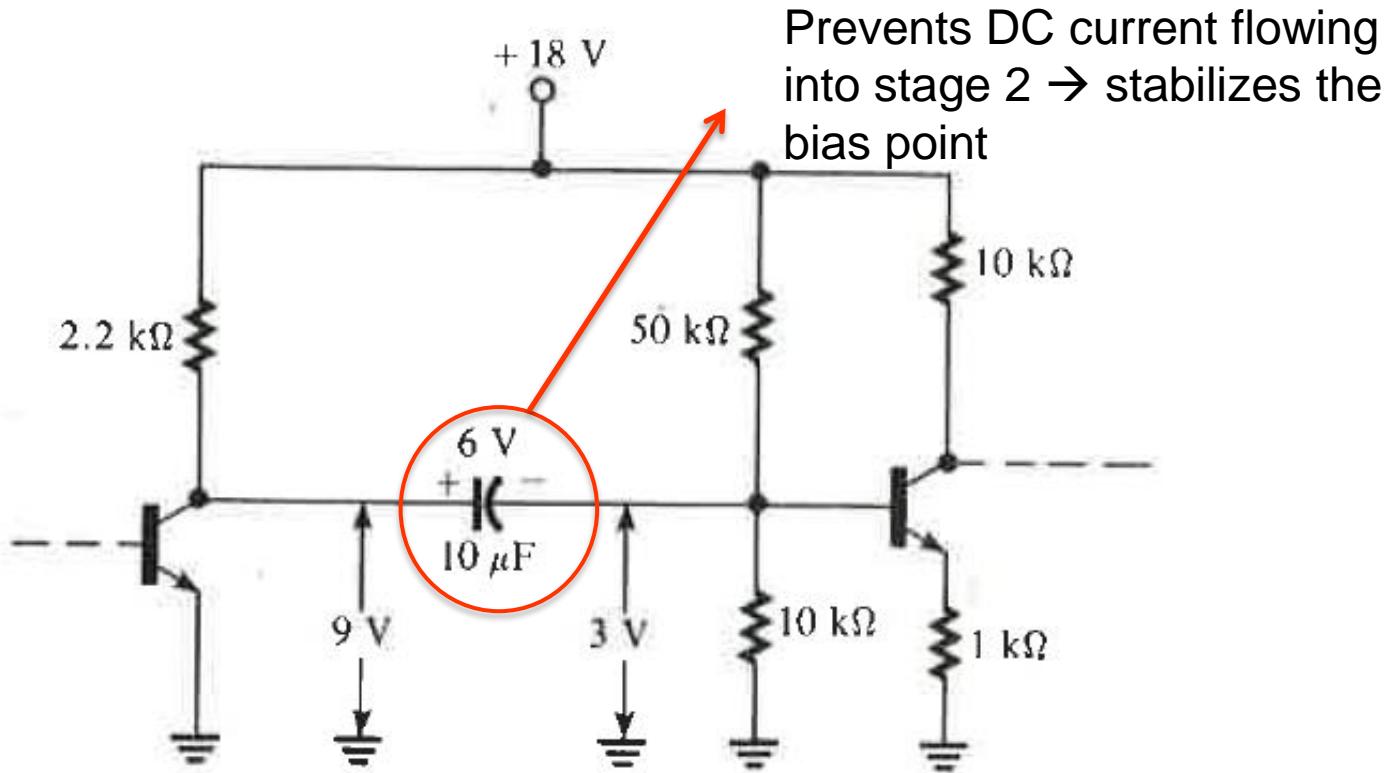
↓
stage 1 gain in dB + stage 2 gain in dB + ... + ..

Overall Gain Estimation

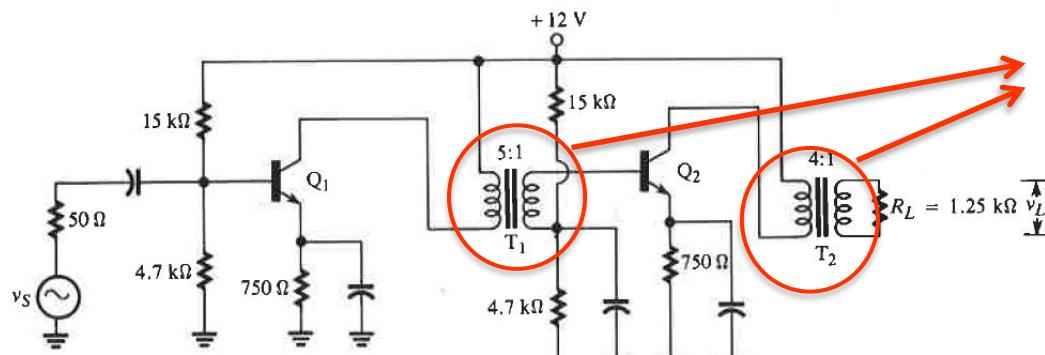


If $r_{i3}, r_{i2}, r_{i1} \gg$ and $r_{o3}, r_{o2}, r_{o1} \ll$, then $A = A_{o3} A_{o2} A_{o1}$

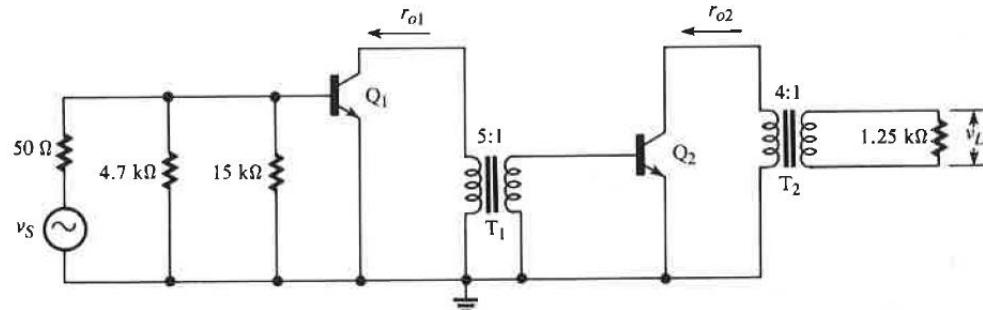
Multi-Stage RC Coupling



Multi-Stage Transformer Coupling



(a) Note that the $4.7\text{-k}\Omega$ base biasing resistor of Q_2 is bypassed and that the $1.25\text{-k}\Omega$ load is isolated from the rest of the circuit.



(b) The ac equivalent circuit of (a)

Prevents DC current flowing into next stage → stabilizes the bias point

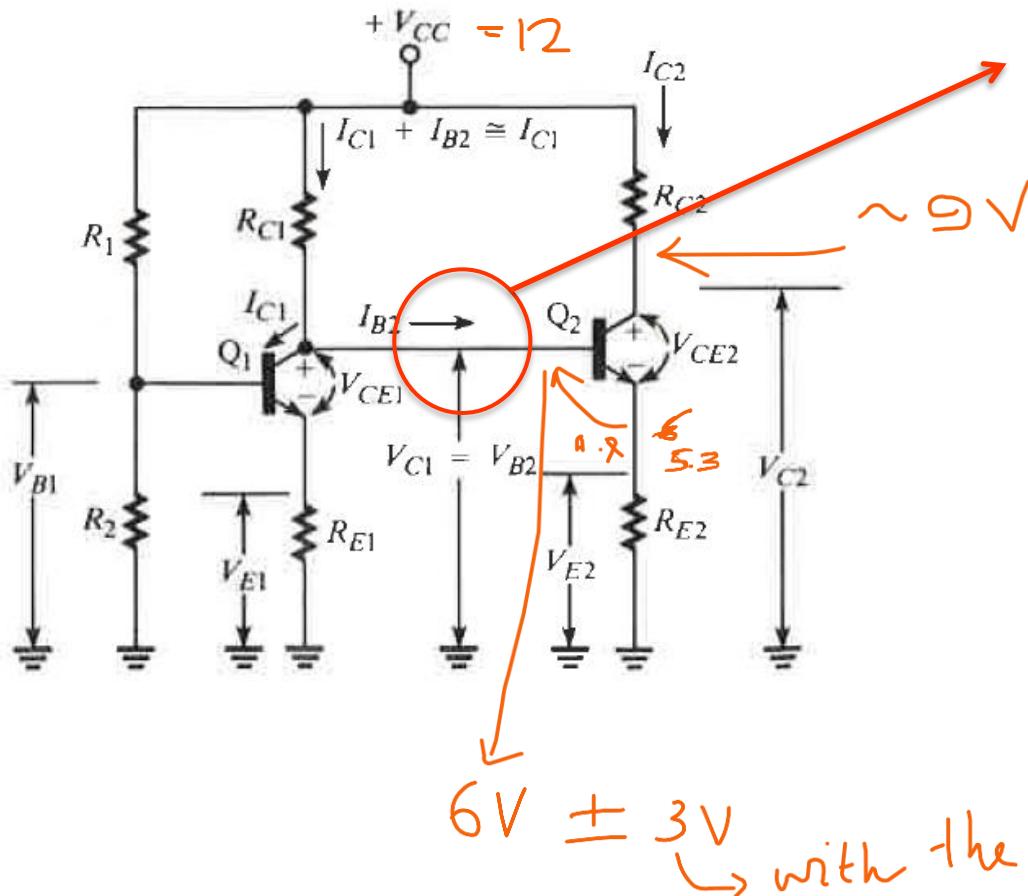
Advantages:

- Low DC power dissipation
- Maximum Power transfer using the turns ratio

Disadvantages:

- Bulky
- Cost of transformers
- Poor frequency response

Multi-Stage Direct Coupling



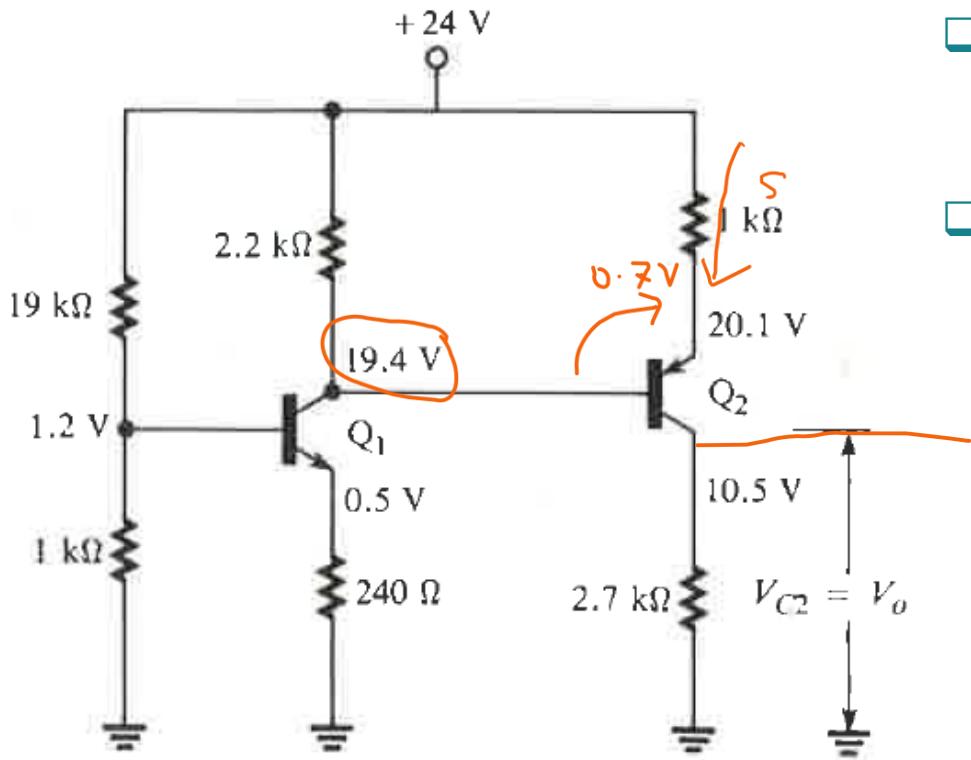
Directly coupled. Both DC and AC voltages/currents are identical

the output bias level of each stage increases to maintain the collector more positive than the base

If this voltage “stacking” is severe, little head room is left in the final stages of the cascade.

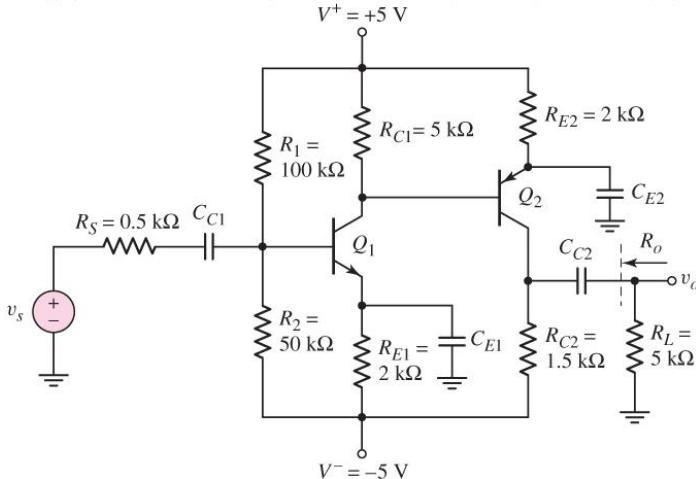
$$A_2 \approx - \frac{I_{C2} R_{C2}}{I_{C2} R_{E2}}$$

Multi-Stage Direct Coupling



- By using complementary devices, active level shifting can be combined with amplification
- The p-stage collector DC operating point tends to cancel the bias level “stacking” issue we encountered in the all NPN CE amplifier

Multistage Analysis: Cascade Configuration

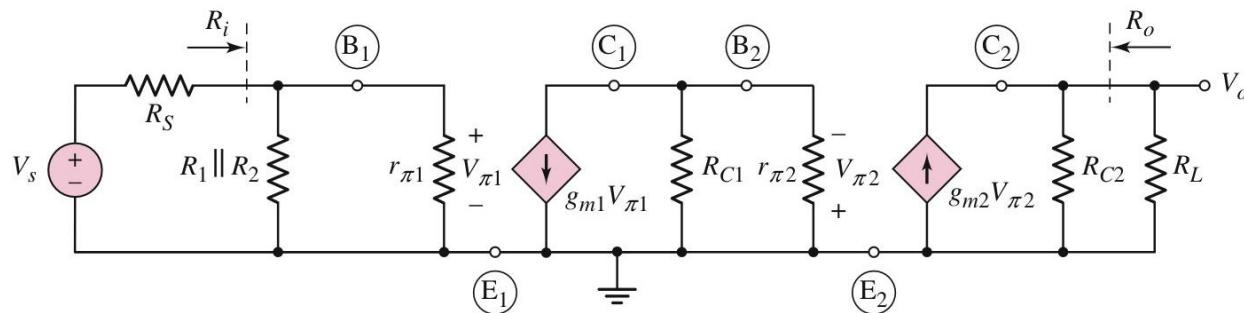


$$A_v = \frac{V_o}{V_s} = g_m 1 g_m 2 (R_{C1} \| r_{\pi 2}) (R_{C2} \| R_L) \left(\frac{R_i}{R_i + R_S} \right)$$

The input resistance of the amplifier is

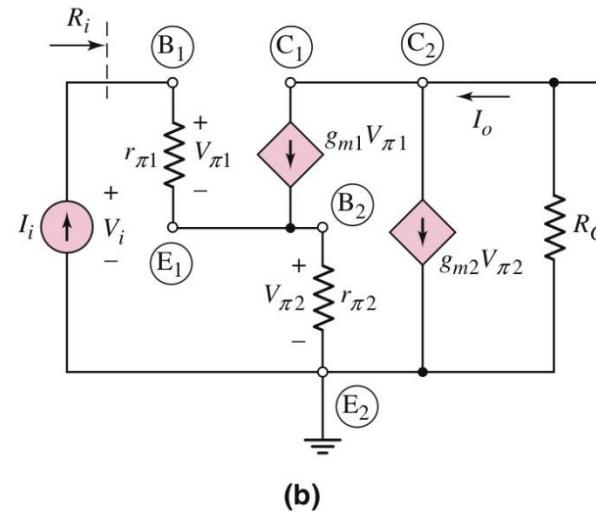
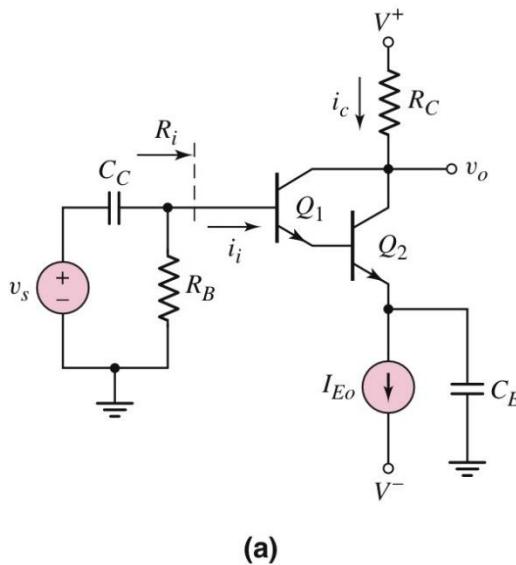
$$R_i = R_1 \| R_2 \| r_{\pi 1}$$

which is identical to that of a single-stage common-emitter amplifier. The output resistance looking back into the output terminals is $R_o = R_{C2}$.



Multi-stage Circuit: Darlington Pair Configuration

- to have a bipolar transistor with a much larger current gain

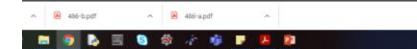


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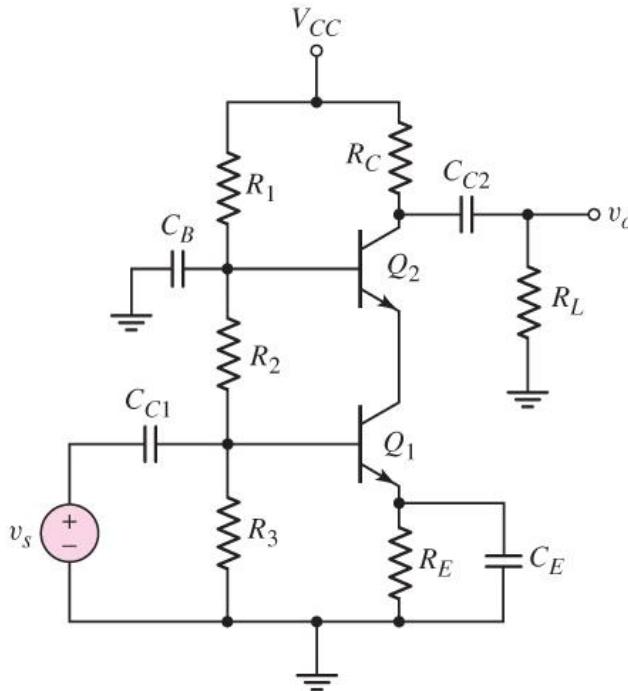
$$A_i \cong \beta_1 \beta_2$$

This is a two-transistor circuit that operates like a Darlington pair. It has similar characteristics: high current gain, voltage gain of near 1, high output impedance and high input impedance.
Note: it is **not the Darlington** configuration:

Darlington: 2 npn BJTs
Feedback Pair: pnp driving an npn BJT



Multistage Circuit: Cascode Configuration



- ❑ Wideband voltage amplifier
- ❑ CE stage operates at gain=-1, minimising miller loading of input.
- ❑ CB gives all the voltage gain, acting as transimpedance of value Z_L
- ❑ The cascode has a much higher output impedance (other than Z_L) than the CE amplifier (the common emitter Early resistance acts as series-series feedback to the common base with loop gain = gmR_{CE})

Discrete Op-Amp Circuit

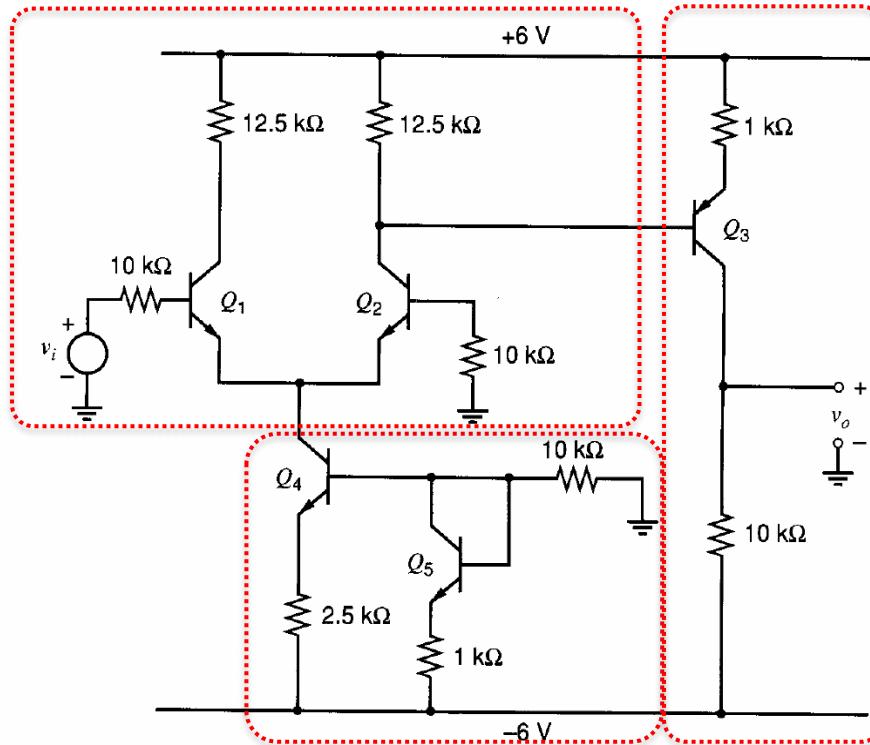


Figure 7.48 Two-stage amplifier with *pnp* second stage.

References

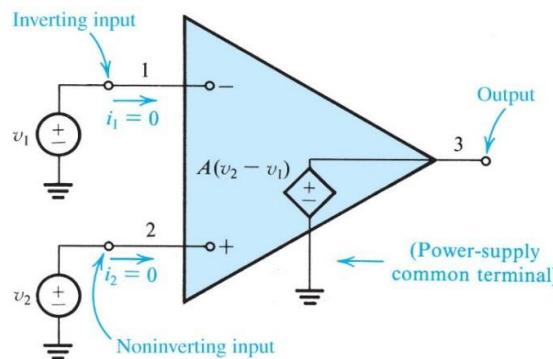
- ❑ D. Neamen, Microelectronics Circuit Analysis and Design, 4th ed., McGraw-Hill Education, 2009.
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8. BJT Operational Amplifiers

Introduction to Op-Amps

□ Characteristics:

- Infinite input impedance
- Zero output impedance
- Infinite open-loop gain (A_{OL})
- Infinite Bandwidth
- Zero common-mode gain
- Infinite CMRR



	ideal	LM741 ¹	LF411 ²
A _O (OL)	infinite	2×10^5	2×10^5
F _t	infinite	1.5MHz	4.0MHz
Slew Rate	infinite	0.5V/ μ s	15V/ μ s
Input Resistance	infinite	$2M\Omega$	$10^{12}\Omega$
Output Resistance	zero	50Ω	50Ω
V _{off}	Zero	1mV	0.8mV
I _B	Zero	80nA	50pA
I _{off}	zero	20nA	25pA
CMRR	High	90 dB	100 dB

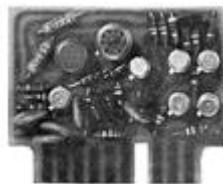
1. <https://www.ti.com/lit/ds/symlink/ua741.pdf>
2. https://www.ti.com/lit/ds/slos011c/slos011c.pdf?ts=1616049571753&ref_url=https%253A%252F%252Fwww.google.com%252F

Op-Amp History

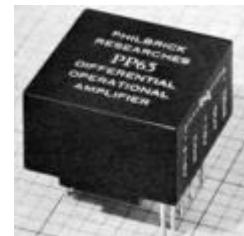
- 1930-1940: First op-Amp designed by Karl Swartzel for the Bell Labs M9 gun director
- Uses 3 vacuum tubes, only one input and +/- 350 v to attain a gain of 90 dB
- Loebe Julie then developed an Op-Amp with two inputs: inverting and non-inverting



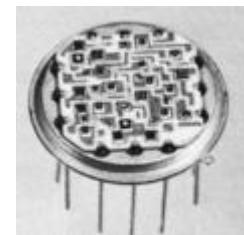
a vacuum-tube op-amp (1953)



a solid-state, discrete op-amp (1961).



a solid-state op-amp in a potted module (1962)



a high speed hybrid IC op-amp (1979)



An op-amp in a mini DIP package

Op-Amp Circuit: Vacuum Tube

A familiar shape to DC amplifier devotees



WIDELY
RECOGNIZED . . .
WIDELY ACCEPTED . . .
K2 OCTAL PLUG-INS
FROM PHILBRICK

FAST DC: K2-W is an efficient, foolproof high-gain operational unit for all feedback applications, fast and slow. The K2-W features balanced differential inputs for low drift, high input impedance, low output impedance, and economy of operation. Its range of operation is from d-c to above 100 kc depending on external circuitry.

\$24*

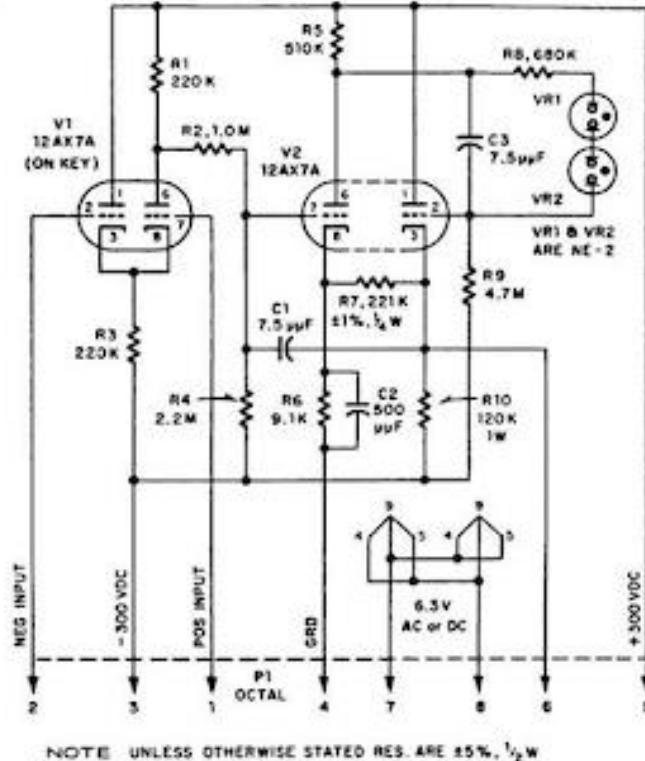


Figure 4. Schematic Diagram
<http://www.wisetech.co.jp/opampdou/story/04/>

Op-Amp Circuit: BJT

- One important application of differential amplifiers is at the input stage of operational amplifiers

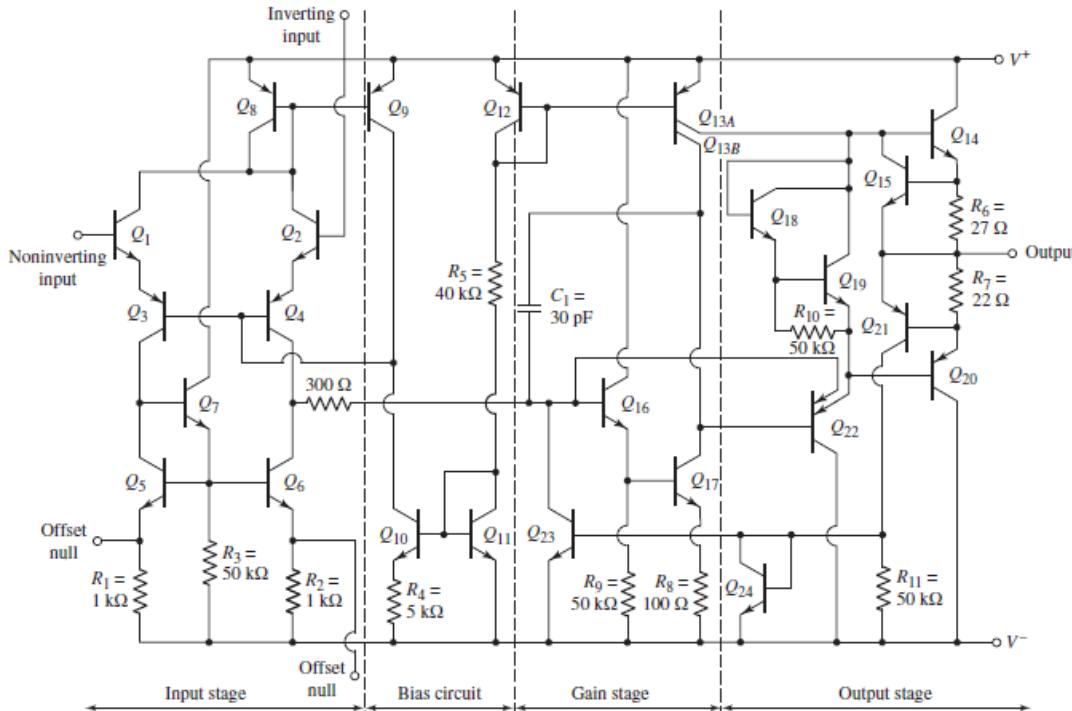
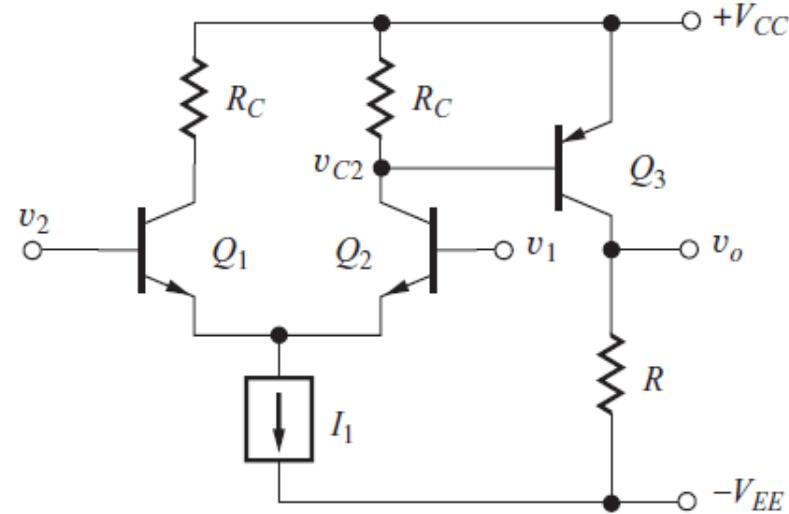
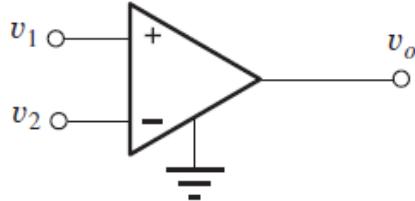


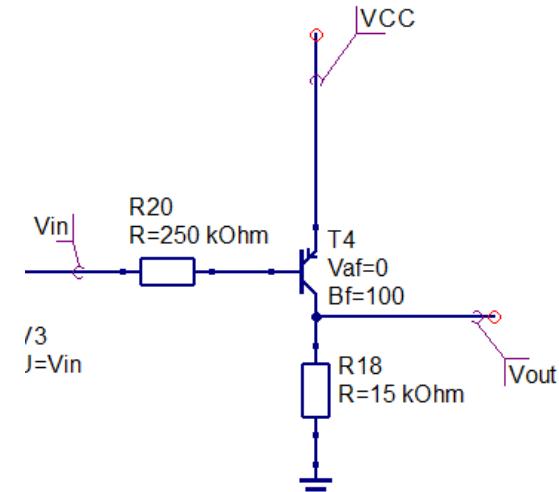
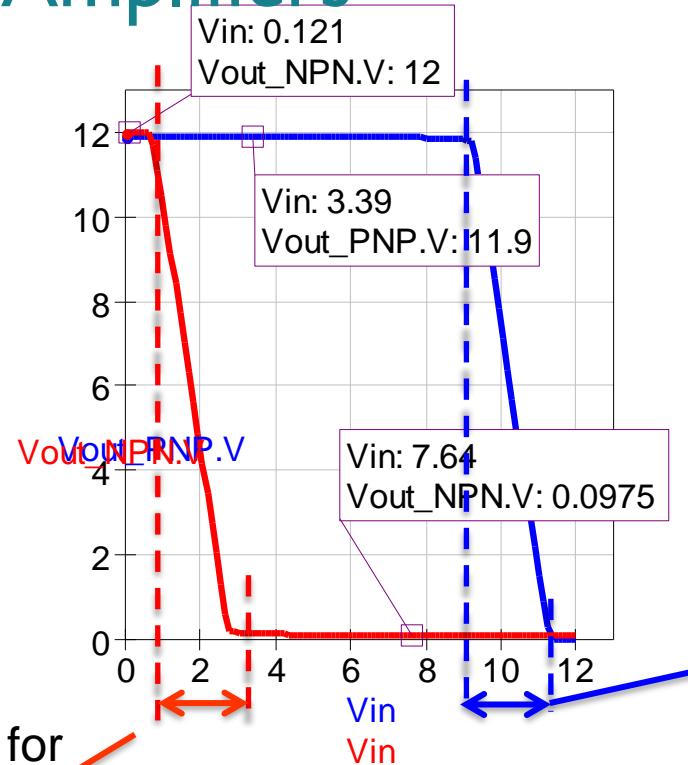
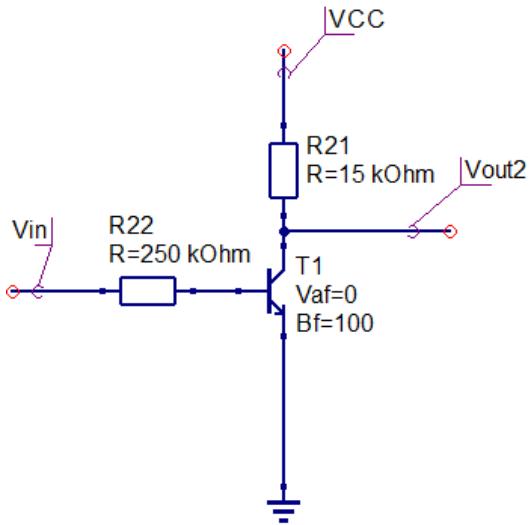
Figure 13.3 Equivalent circuit, 741 op-amp

Two-Stage Basic Operational Amplifier



- ❑ Two stages of gain – perhaps an additional output stage to provide lower output impedance and higher output current capability.
- ❑ Why do we use a PNP stage ?

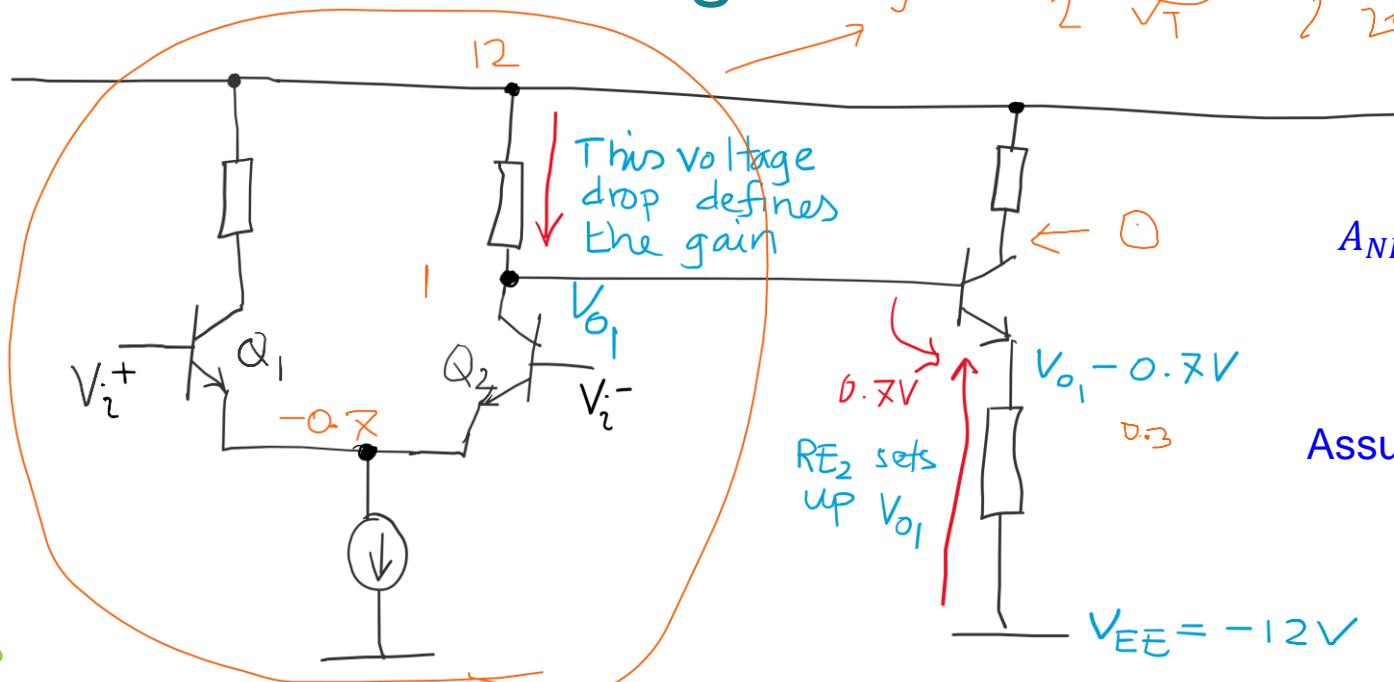
NPN and PNP Amplifiers



DC Op. region for
PNP Amplifier

DC Op. region for
NPN Amplifier

Can we use a NPN stage ?



$$\text{gain} = \frac{I_2 R_C}{\frac{1}{2} \sqrt{T}} = \frac{1}{2} \frac{11 \times 1000}{26} = 211$$

$$A_{NPNstage} = -\frac{R_{C2}}{R_{E2}}$$

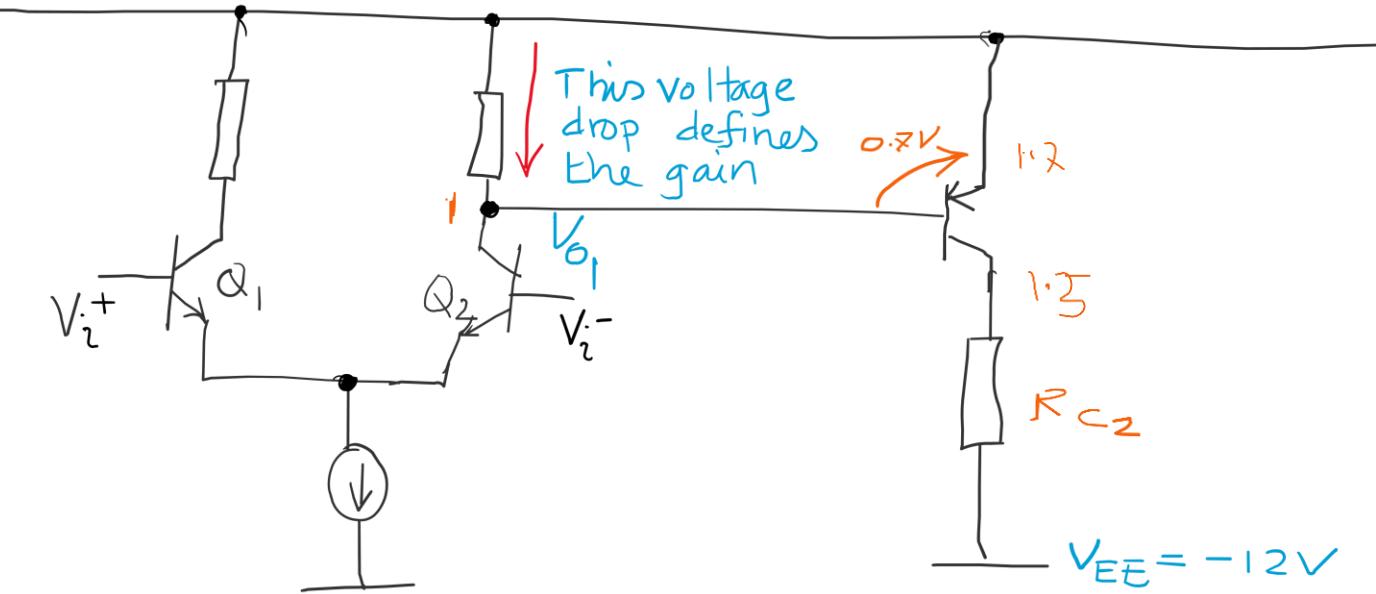
$$= -\frac{I_{C2}R_{C2}}{I_{C2}R_{E2}}$$

$$\text{Assuming } I_{C2} \approx I_{E2}$$

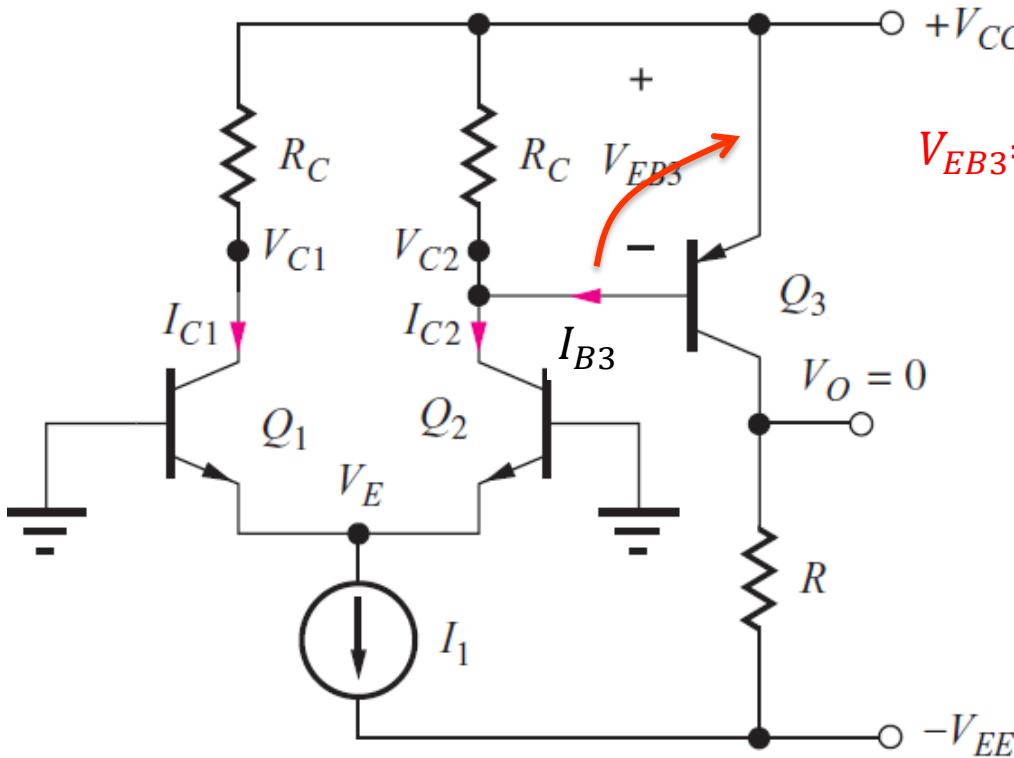
$$= -\frac{I_{C2}R_{C2}}{I_{E2}R_{E2}}$$

$$A_2 = \frac{12}{12.3} < 1$$

Can we use a NPN stage ?



Two-Stage Op-Amp: DC Analysis

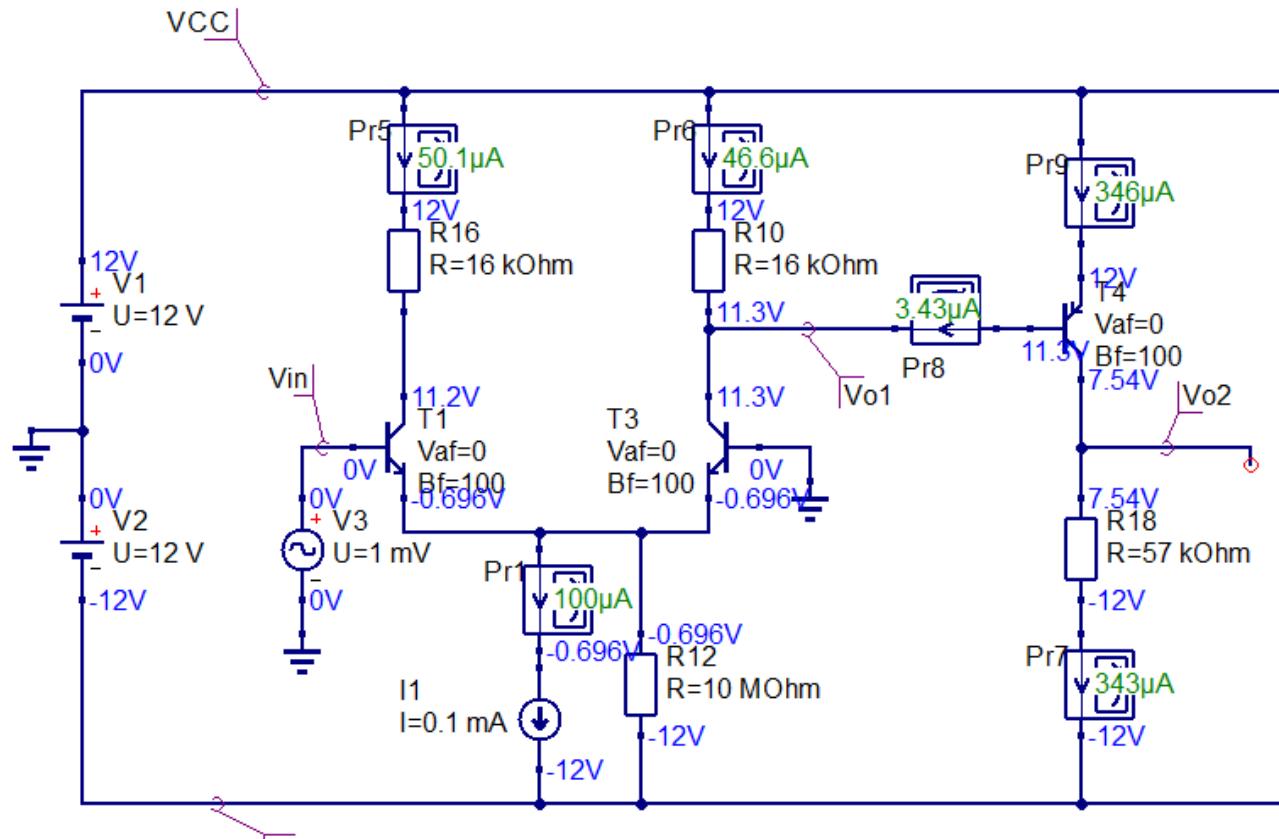


$V_{EB3}=0.7\text{V} \rightarrow \text{To keep } Q_3 \text{ in active mode}$

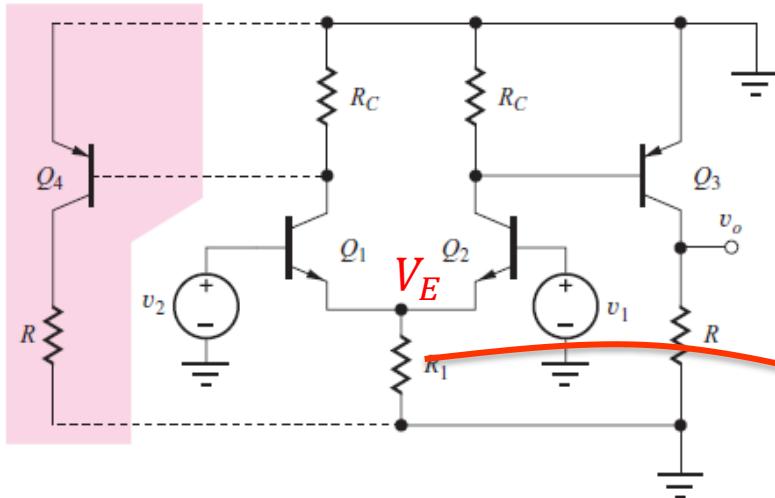
Drop across $R_c = 0.7\text{ V}$

$$R_{C2} (I_{C2} + I_{B3}) = 0.7\text{ V}$$
$$R_{C2} I_{C2} \approx 0.7\text{ V}$$

Two-Stage Op-Amp: DC Analysis

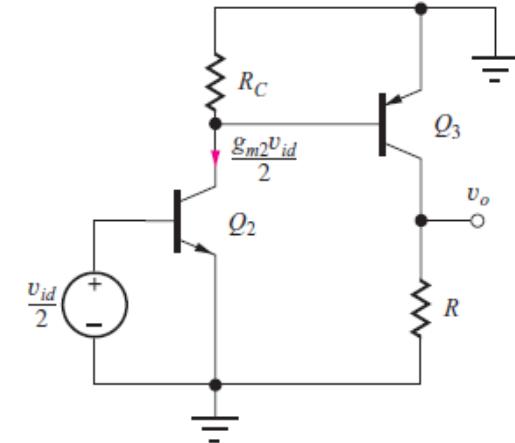


Two-Stage Op-Amp:AC Analysis



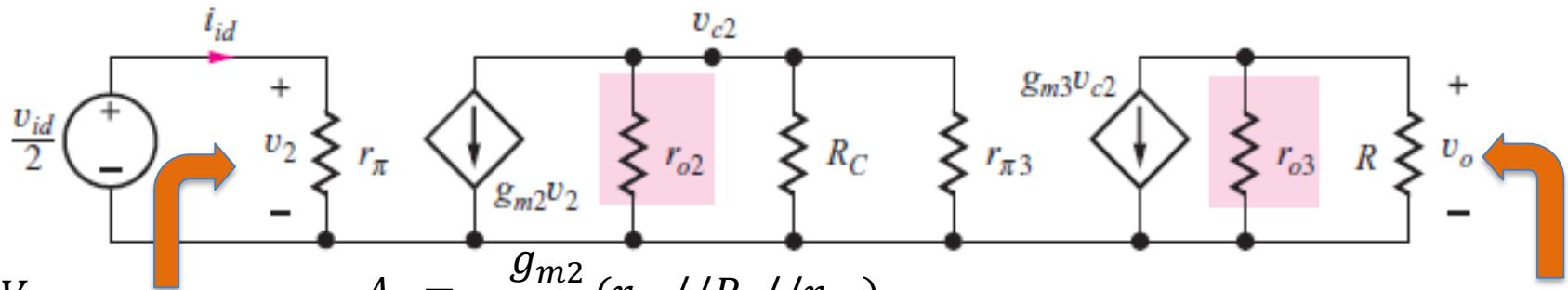
R1 is removed
because $V_E \approx 0$

voltage variations at the collector of Q2 do not substantially alter the current in the transistor when it is operating in the forward-active region



Half-circuit AC model

Two-Stage Op-Amp:AC Analysis



$$R_{id} = \frac{V_{id}}{i_{id}} = 2r_\pi$$

$$\begin{aligned}A_1 &= -\frac{g_{m2}}{2} (r_{o2}/R_c/r_{\pi3}) \\&= -\frac{g_{m2}}{2} \frac{R_C r_{\pi3}}{R_C + r_{\pi3}}\end{aligned}$$

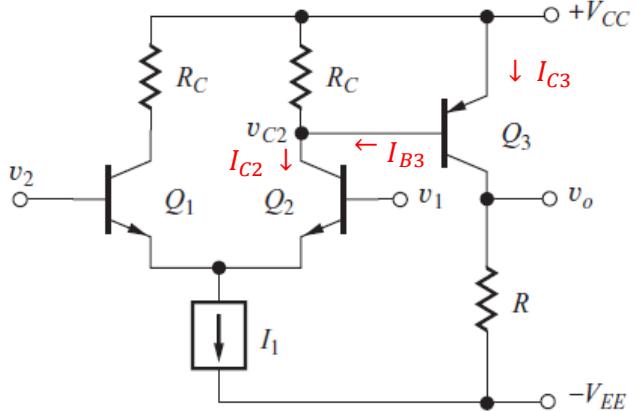
$$\begin{aligned}A_2 &= -g_{m3}(r_{o3}/R) \\&= -g_{m3}R\end{aligned}$$

$$R_o = R // r_{o3} \approx R$$

□ Overall gain of the Two Stage Amplifier:

$$A_{dm} = A_1 A_2 = \frac{g_{m2}}{2} \frac{R_C(r_{\pi3}g_{m3})R}{R_C + r_{\pi3}} = \frac{g_{m2}R_C}{2} \frac{\beta_3 R}{R_C + r_{\pi3}}$$

Two-Stage Op-Amp: AC Analysis



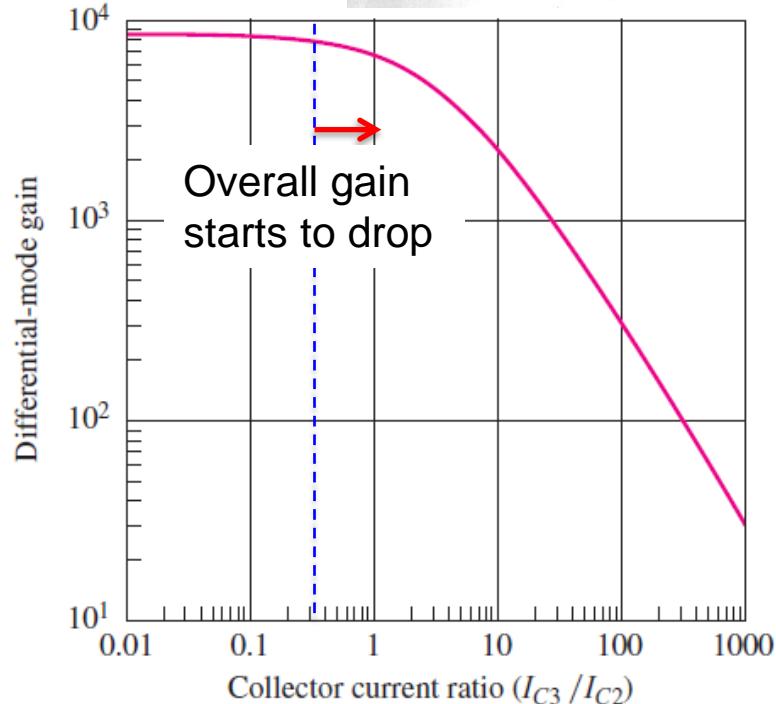
$$A_{dm} = \frac{g_{m2}R_c}{2} \frac{\beta_3 R}{R_c + r_{\pi3}}$$

$$= \frac{560 V_{EE}}{1 + \frac{28(I_{C3})}{\beta_3(I_{C2})}}$$

$$A_{dm} = \frac{g_{m2}R_c \beta_3 R}{2(R_c + \frac{\beta_3}{g_{m3}})}$$

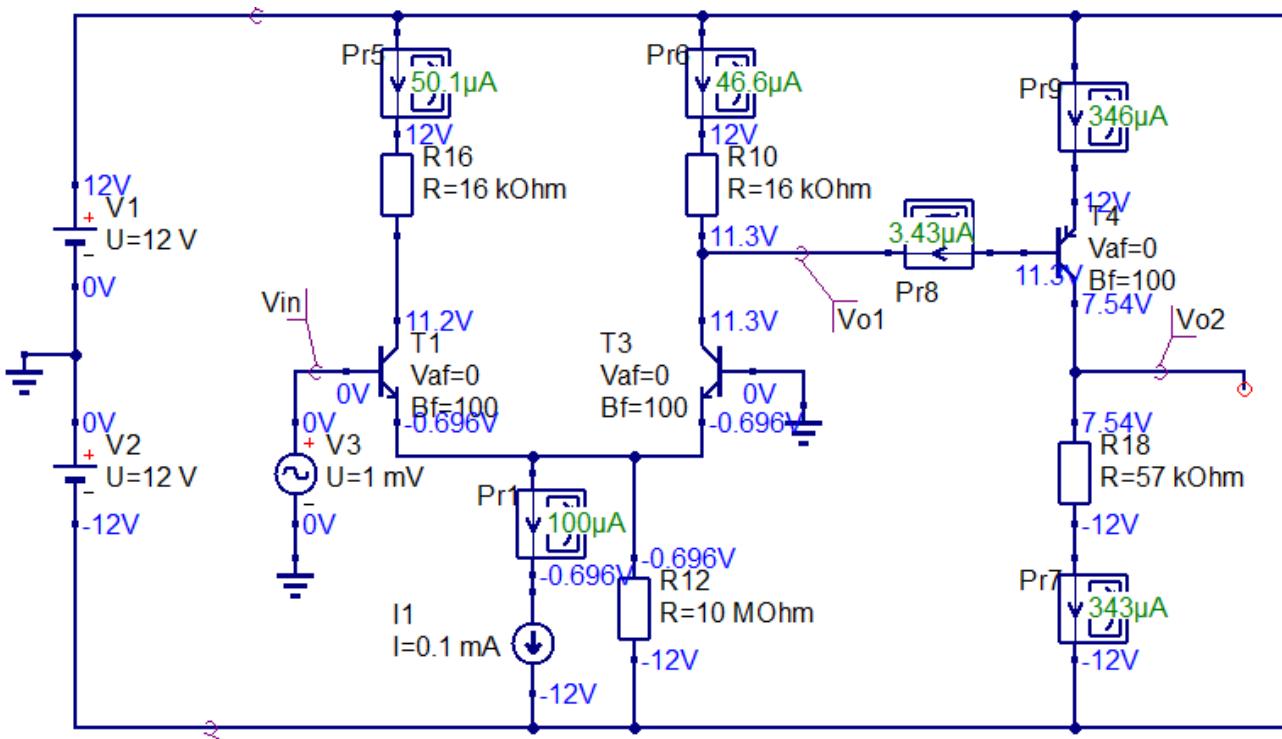
$$= \frac{40I_{c2}R_c \beta_3 g_{m3}}{2(g_{m3}R_c + \beta_3)}$$

$$= \frac{40(\frac{\beta_3}{0.7}I_{c2}R_c) \beta_3 \times 40I_{c3}R}{2(40\frac{I_{c3}}{I_{c2}}(\frac{I_{c2}R_c}{0.7} + \beta_3))} = \frac{V_{EE}}{V_{EE}}$$



- ❑ V_{EE} and β is fixed.
- ❑ Minimum value of I_{C3} is determined by the load. Generally, $I_{C3} > I_{C2}$
- ❑ An upper limit on I_{C2} is set by I_{B3}

Two-Stage Op-Amp: Gain Simulation



Estimated Gain

$$A_{dm} = \frac{560 V_{EE}}{1 + \frac{28}{\beta_3} \left(\frac{I_{C3}}{I_{C2}} \right)}$$
$$= \frac{560 * 12}{1 + \frac{28}{100} \left(\frac{346}{46.6 + 3.43} \right)}$$
$$= 2288$$

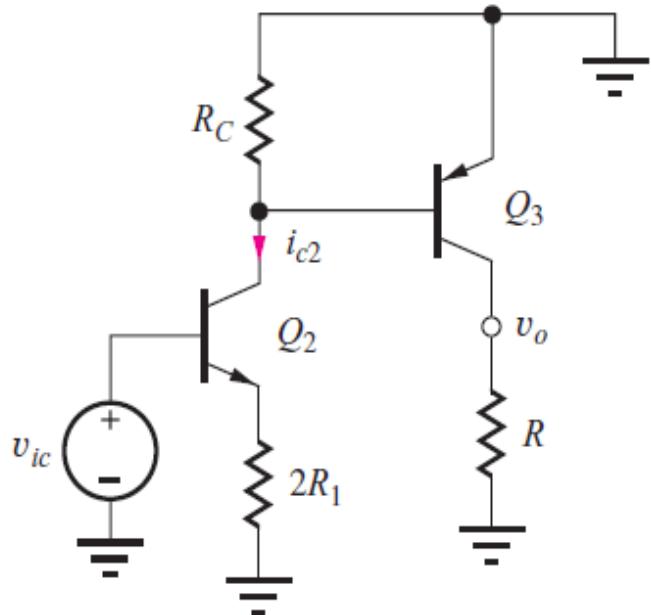
Simulated Gain

$$A1 = 4.98$$

$$A2 = 751$$

$$A_{dm} = A1 * A2 = 3740$$

Two-Stage Op-Amp: CMRR



$$i_{c2} = \frac{\beta_{o2} v_{ic}}{r_{\pi 2} + 2(\beta_{o2} + 1)R_1} \cong \frac{g_{m2} v_{ic}}{1 + 2g_{m2} R_1}$$

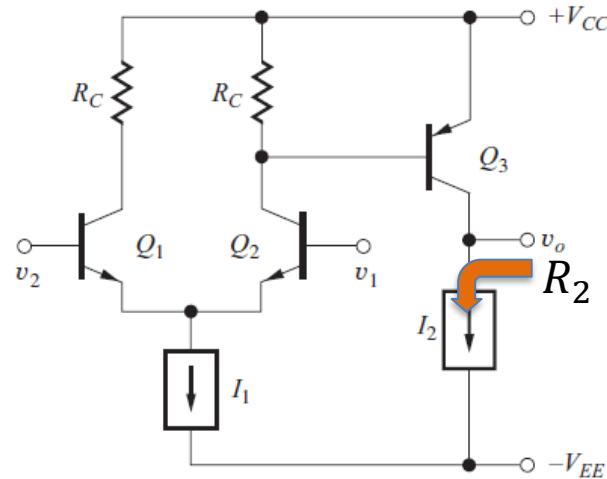
$$A_{cm} = \frac{g_{m2} R_C}{1 + 2g_{m2} R_1} \frac{\beta_{o3} R}{R_C + r_{\pi 3}} = \frac{2 A_{dm}}{1 + 2g_{m2} R_1}$$

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| = \frac{1 + 2g_{m2} R_1}{2} \cong g_{m2} R_1$$

- ❑ identical to the CMRR of the differential input stage alone.

Improving Op-Amp Voltage Gain

- We saw overall gain of the amplifier decreases rapidly as the quiescent current of second stage decreases
- How to improve Voltage gain? Replace the collector resistor with a current source



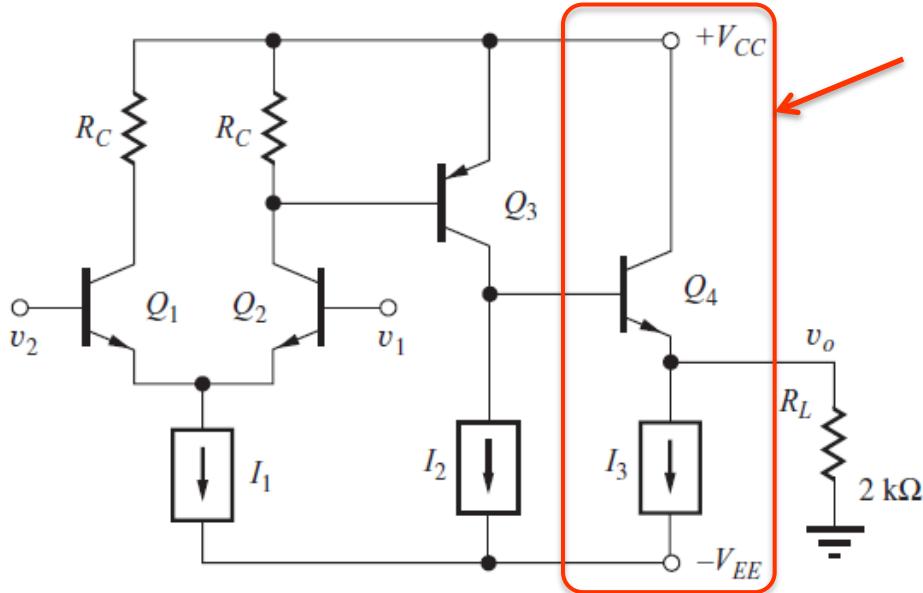
$$A_{dm} = A_{vt1} A_{vt2} = \left(-\frac{g_{m2}}{2} \frac{R_C r_{\pi 3}}{R_C + r_{\pi 3}} \right) (-g_{m3} r_{o3})$$

$$A_{dm} \cong \frac{560 V_{A3}}{1 + \frac{28}{\beta_{o3}} \left(\frac{I_{C3}}{I_{C2}} \right)}$$

For very low values of I_{C3} , $A_{dm} = 560 V_{A3} \rightarrow$ Very high

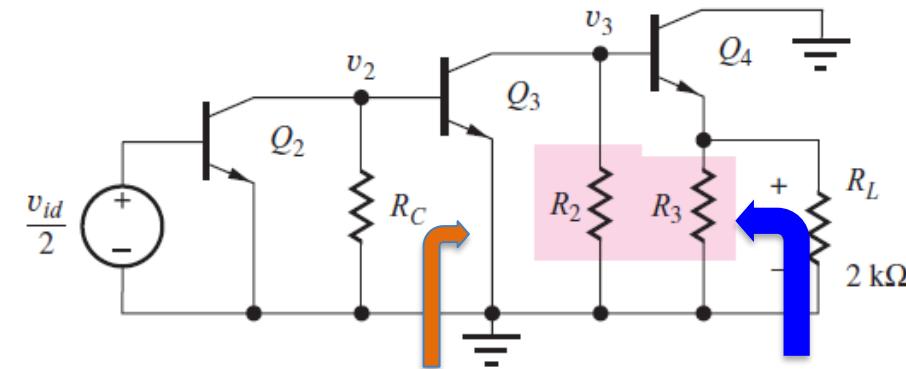
Now the output resistance is: $R_2 // r_{o3} \rightarrow$ high

Reducing Output Resistance



CC (Emitter Follower) stage

- *High input impedance*
- *Unity voltage gain*
- *Low output impedance*



$$A_{vt1} = -\frac{g_m 2}{2} (R_C \parallel r_{\pi 3})$$

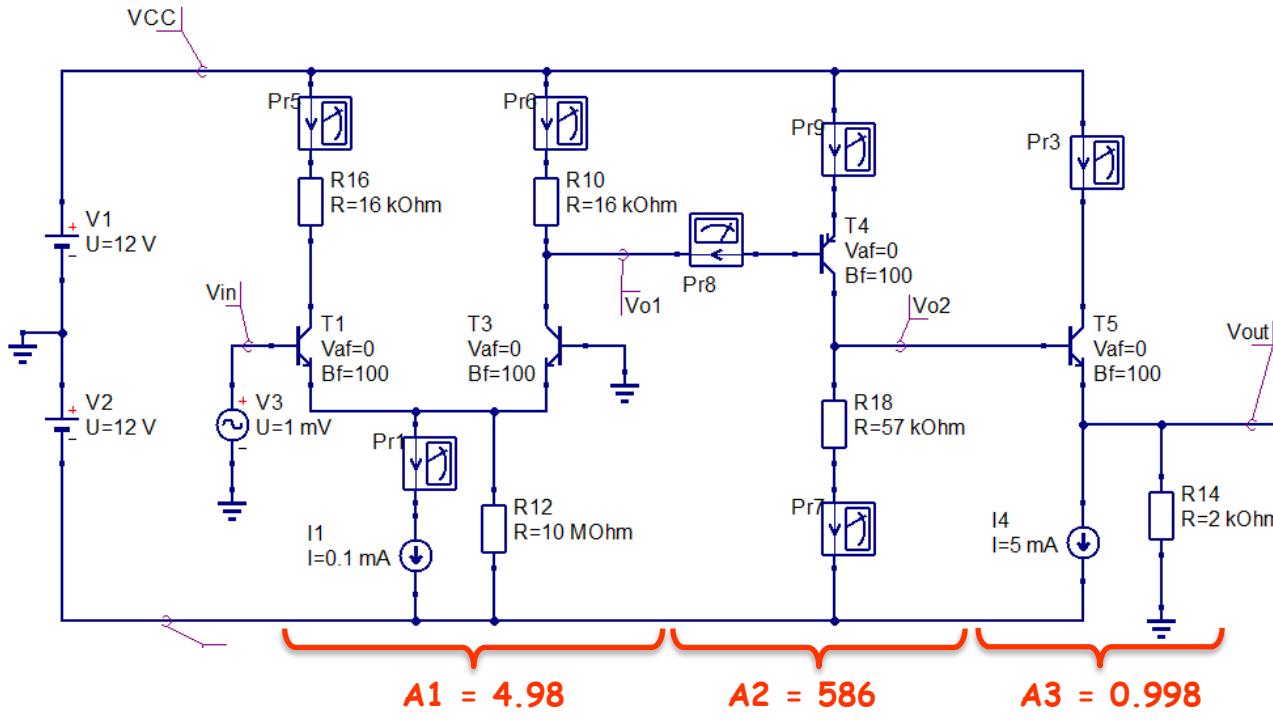
$$A_{dm} = \frac{V_2}{V_{id}} \frac{V_3}{V_2} \frac{V_o}{V_3} = A_{vt1} A_{vt2} A_{vt3}$$

$$A_{vt2} = -g_{m3} (r_{o3} \parallel R_{iB4}) \text{ where } R_{iB4} = r_{\pi 4} (1 + g_{m4} R_L)$$

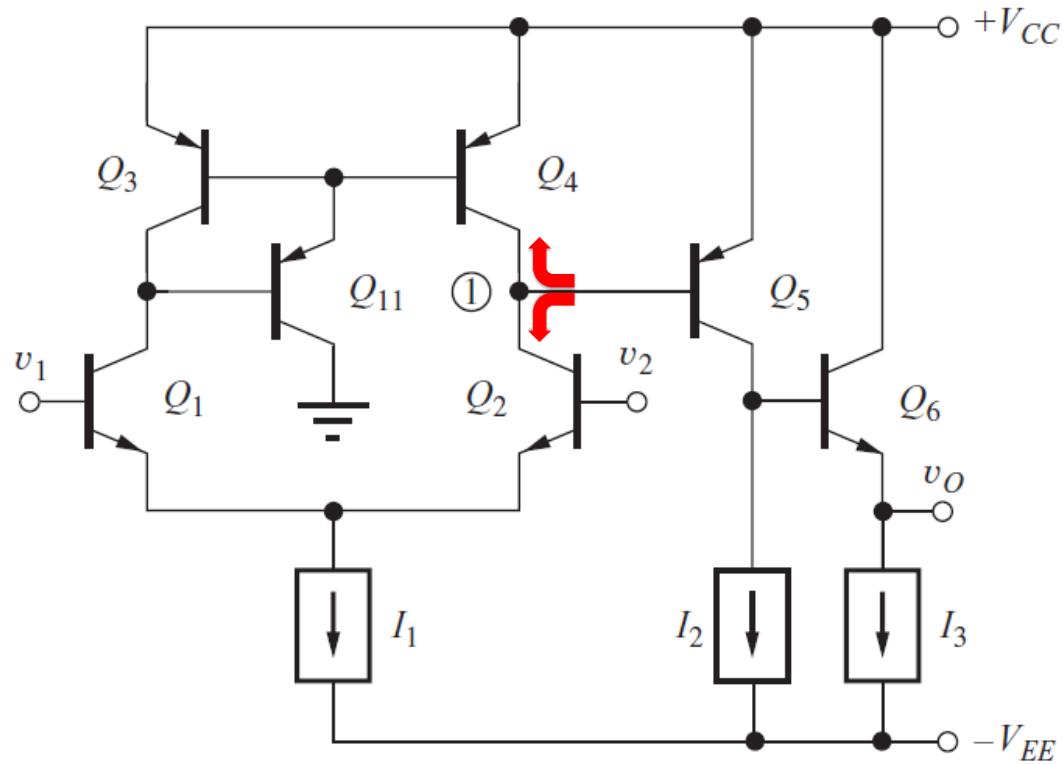
$$A_{vt3} = \frac{g_{m4} R_L}{1 + g_{m4} R_L} \cong 1$$

$$R_{out} \cong \frac{1}{g_{m4}} + \frac{r_{o3}}{\beta_{o4}}$$

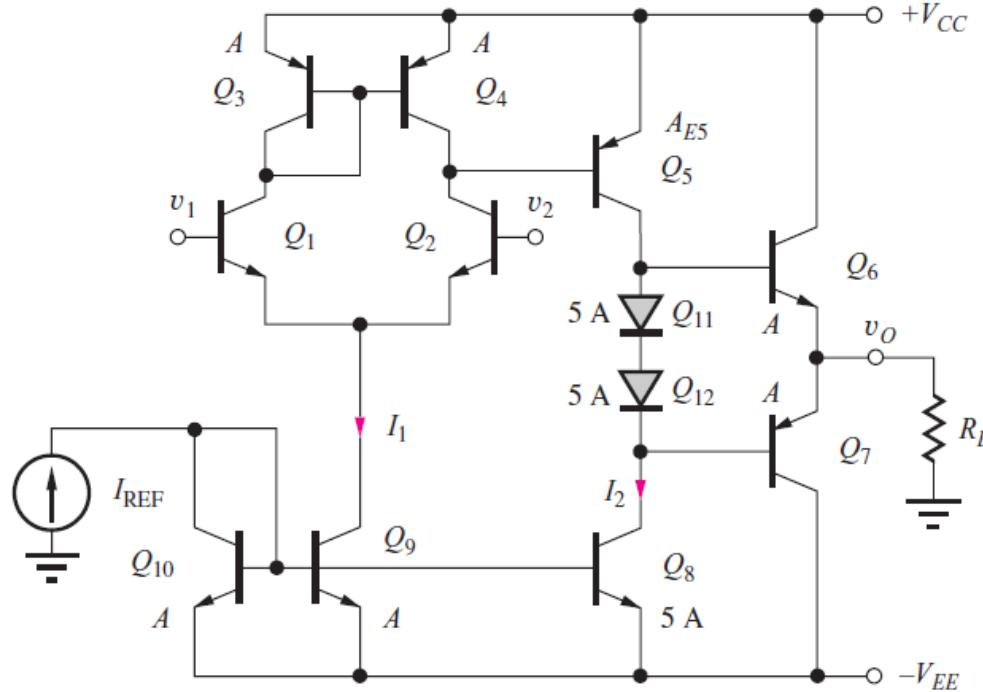
Three-Stage Op-Amp: Gain Simulation



Three-Stage OpAmp with Active Load



Three-Stage OpAmp with Active Load



$$A_{dm} \cong [g_{m2}r_{\pi5}][g_{m5}(r_{o5}\|r_{o8}\|(\beta_{o6} + 1)R_L)][1] \cong \frac{g_{m2}}{g_{m5}} g_{m5} r_{\pi5} g_{m5} \frac{r_{o5}}{2}$$

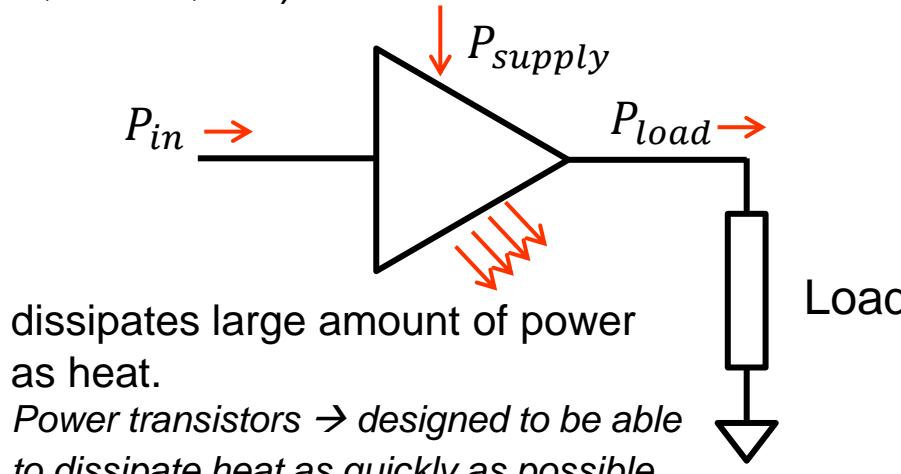
Examples for Three-Stage OpAmp Circuits

- http://www.kennethkuhn.com/students/ee351/lab_5.pdf
- <https://inst.eecs.berkeley.edu/~ee140/sp14/labs/Lab2.ee140.s14.v1.pdf>
- https://people.eecs.berkeley.edu/~pister/140sp20/labs/prob3_1.pdf
- https://people.eecs.berkeley.edu/~pister/140sp20/labs/prob3_2.pdf
- https://ocw.mit.edu/resources/res-6-010-electronic-feedback-systems-spring-2013/textbook/MITRES_6-010S13_chap08.pdf

9. Output Stages

Power Amplifiers and Output Stages

- Power amplifiers → designed to deliver a large amount of power to a passive load (eg. Speaker, motor, etc).

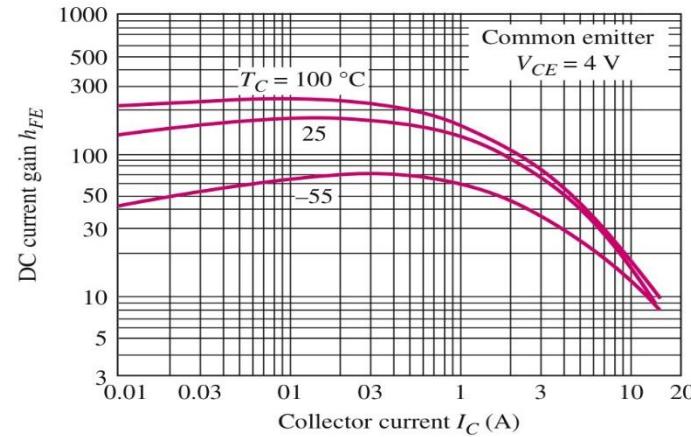


- PAs are often the last (or output) stage of a multi-stage amplifier. Preceding stages carry out amplification, buffering, etc.

Power BJTs

- Power BJTs have higher V and I rating; low range of β

Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE} (max) (V)	40	60	250
I_C (max) (A)	0.8	15	7
P_D (max) (W) (at $T = 25^\circ\text{C}$)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1



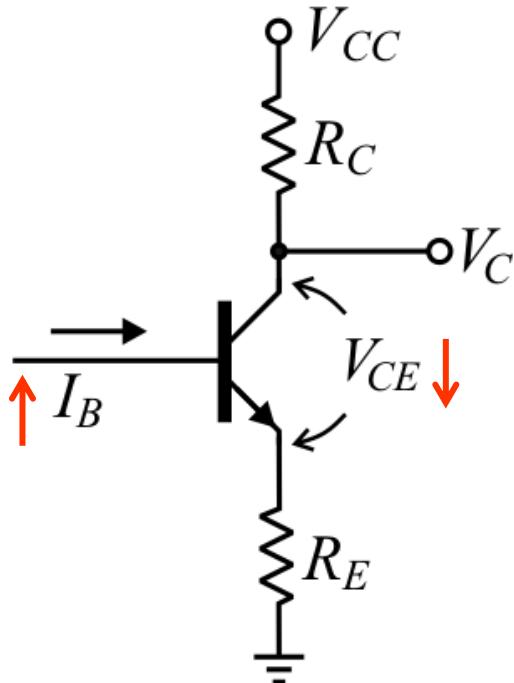
- PA design is constrained by:

- maximum rated current (on the order of amperes);
- maximum rated voltage (on the order of 100 V);
- Maximum rated power (on the order of watts or tens of watts).

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Power BJT Saturation Voltage

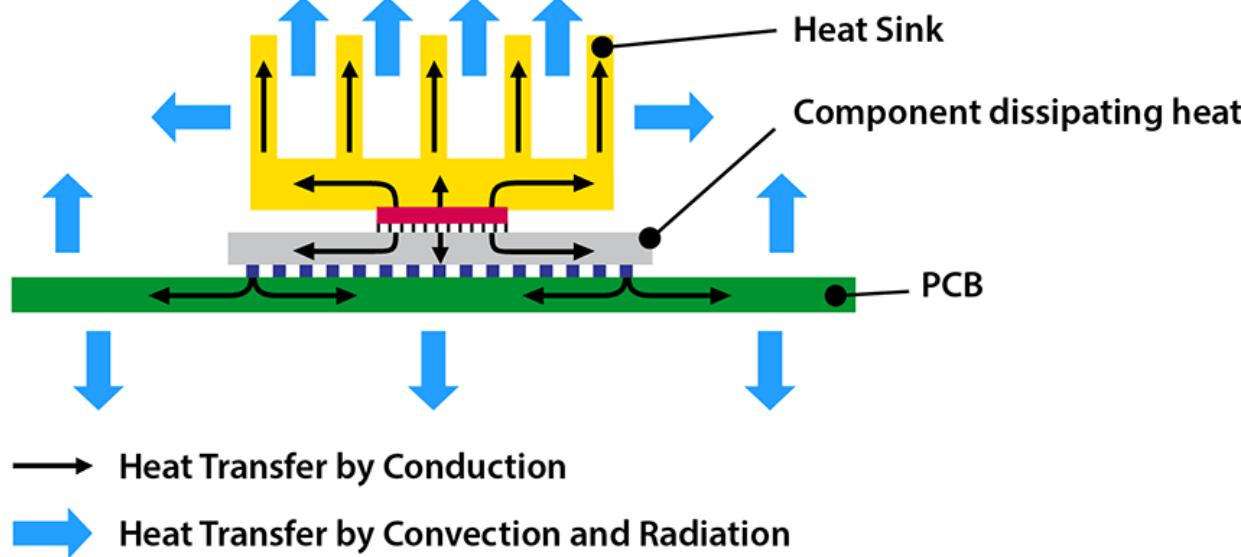
- As I_B increases, I_C increases and V_{CE} decreases. However, it reaches to a point where V_{CE} will not decrease further, regardless how much I_B is
→ saturation voltage $V_{CE(sat)}$



$V_{CE(sat)}$	<0.4 @ ($I_c=10\text{mA}$)	1.0V @ ($I_c=4\text{A}$)

Heat Transfer in Semiconductors

- Semiconductor devices are cooled by all three heat-transfer mechanisms.

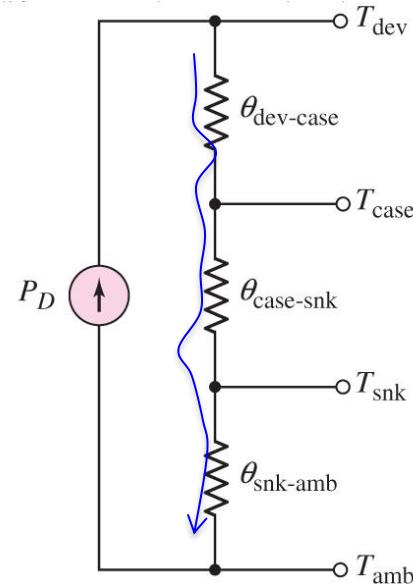


Thermal Resistance

- Heat flow by conduction is similar to conduction of electrical charge.
- Power dissipation (P) is the rate of flow of heat energy. It is proportional to the temperature difference of the region
- The flow of heat is impeded by “thermal resistance (θ)” of the medium.

$$P = \frac{\Delta T}{\theta} = \frac{T_2 - T_1}{\theta}$$

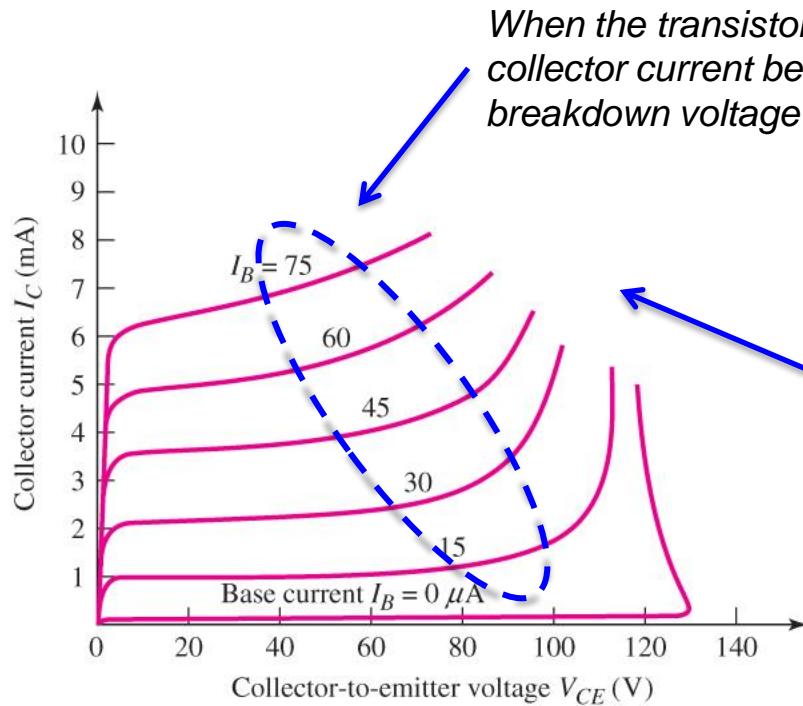
$$T_{dev} - T_{amb} = P_D(\theta_{dev-case} + \theta_{case-snk} + \theta_{snk-amb})$$



Ex 8.2: A power BJT is operating with an average collector current of $I_C = 2$ A and an average collector-emitter voltage of $V_{CE} = 8$ V. The device parameters are $\theta_{dev-case} = 3^\circ\text{C/W}$, $\theta_{case-snk} = 1^\circ\text{C/W}$, and $\theta_{snk-amb} = 4^\circ\text{C/W}$. The ambient temperature is 25°C . Determine the temperatures of the (a) device, (b) case, and (c) heat sink. (Ans. (a) 153°C , (b) 105°C , (c) 89°C)

BJT Maximum Voltage limit

- generally associated with avalanche breakdown in the reverse-biased base–collector junction

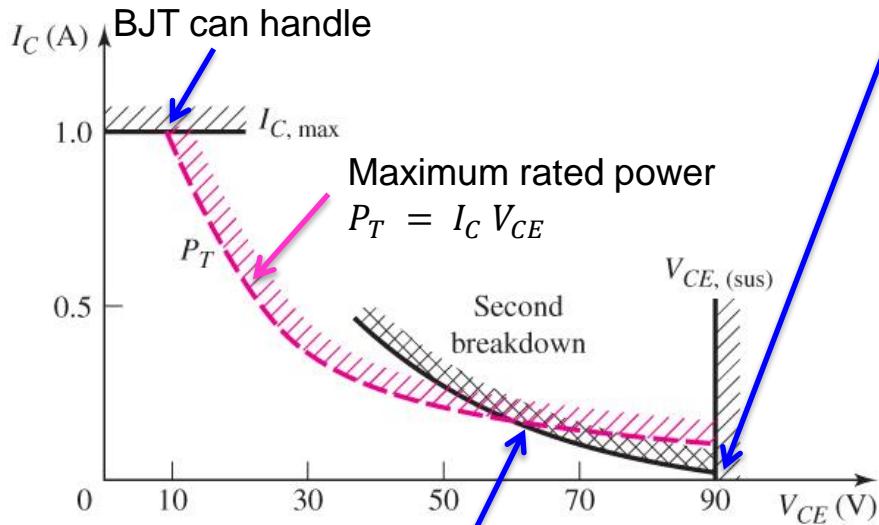


When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CEO} is reached

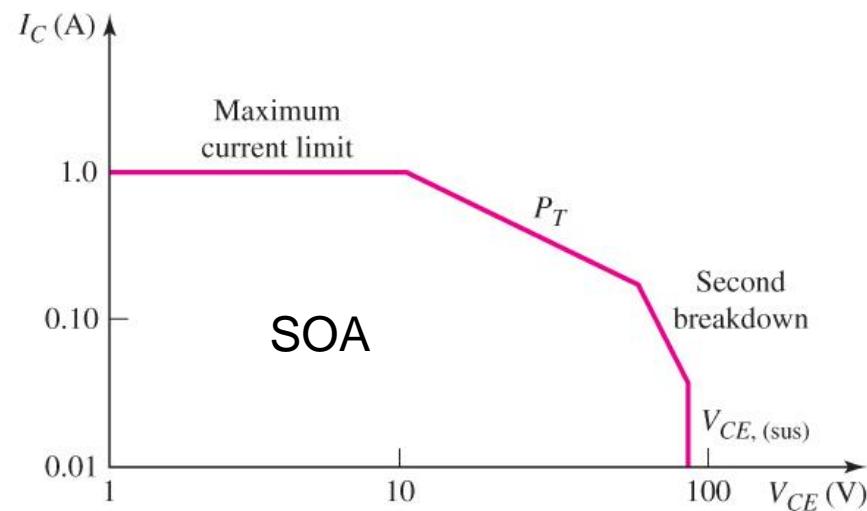
all the curves tend to merge to the same V_{CE} voltage once breakdown has occurred.
The voltage at which these curves merge is denoted $V_{CE}(\text{sus})$ and is the minimum voltage necessary to sustain the transistor in breakdown.

Safe operation Area (SOA) for BJT

I_{\max} is determined by how much current the wires in BJT can handle

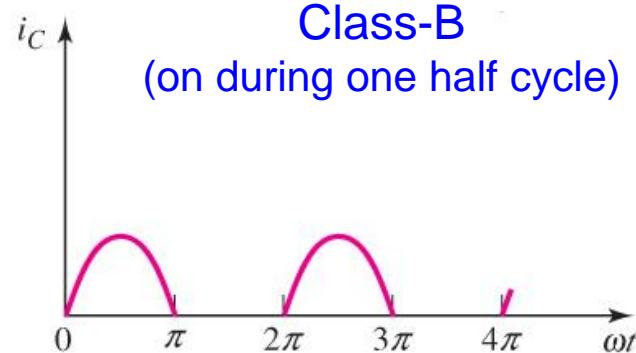
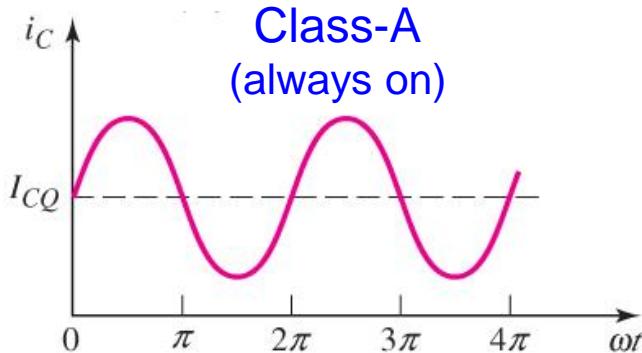


V_{\max} is determined by avalanche breakdown of reverse biased CB junction.

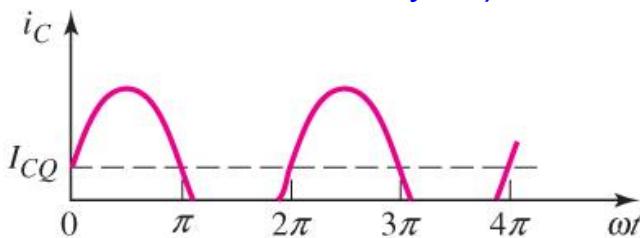


second breakdown → occurs in a BJT operating at high voltage and high current. Slight nonuniformities in the structure causes non-uniformities in current density. This produces local regions of increased heating, which increases current, which generates more heat. In a positive feedback cycle. This can cause material to melt.

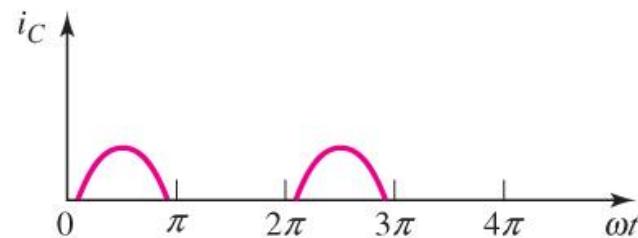
Classes of Amplifiers



Class-AB
(on more than one half-cycle
less than full-cycle)



Class-C
(on less than one half-cycle)



Performance Parameters of PAs

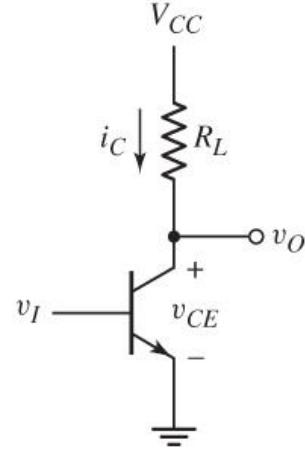
- ❑ **Amplifier Efficiency (η):** It is defined as a ratio of output ac power to the input dc power.

$$\eta = \frac{\text{Output Power}}{\text{Input Power}} \%$$

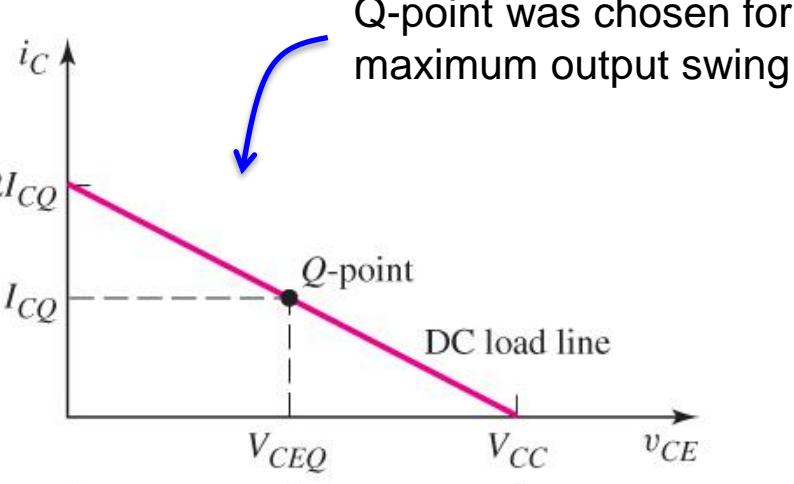
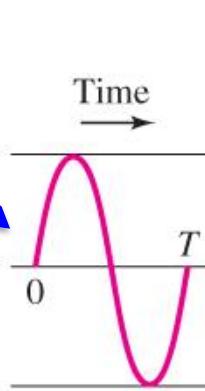
- ❑ **Distortion:** The change in output wave shape from the input wave shape of an amplifier is known as distortion. The distortion can be reduced using negative feedback in amplifier.
- ❑ **Power dissipation capability:** The ability of a power amplifier to dissipate heat is known as power dissipation capability. To achieve better heat dissipation heat sink (metal case) is attached with power transistor. The increase surface area allows heat to escape easily.

Class-A CE Amplifier

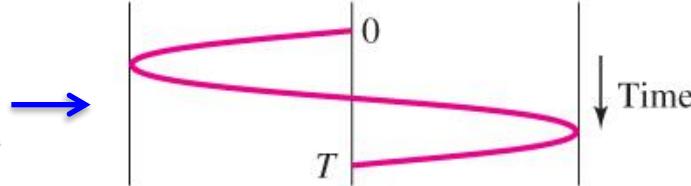
- The small-signal amplifiers considered previously were all biased for class-A operation → The bias circuitry has been omitted.



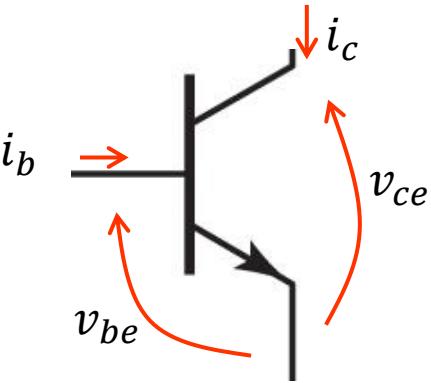
$$i_C = I_{CQ} + I_p \sin \omega t$$



$$v_{CE} = \frac{V_{CC}}{2} - V_p \sin \omega t$$



BJT Power Dissipation



- ❑ instantaneous power dissipation in a BJT

$$P_Q = i_b v_{be} + i_c v_{ce}$$

- ❑ Usually i_b and v_{be} are very small compared to i_c

$$P_Q = i_c v_{ce}$$

- ❑ Average power is:

$$\overline{P_Q} = \frac{1}{T} \int_0^T i_c v_{ce} dt$$

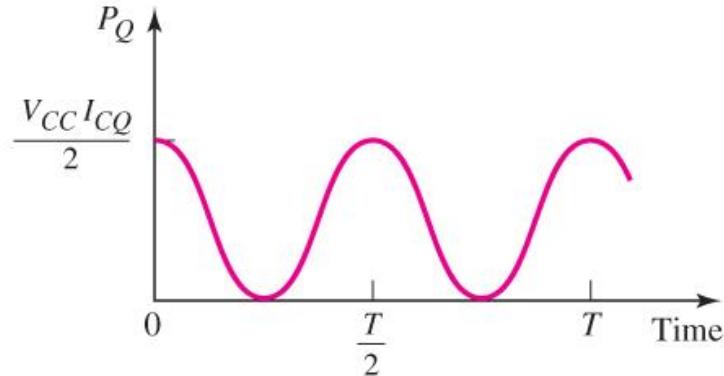
- ❑ Assuming a sinusoidal input signal, we can find that the maximum power dissipation of the BJT is:

$$P_Q = I_{CQ} V_{CEQ}$$

Class-A CE Amplifier: Power Efficiency

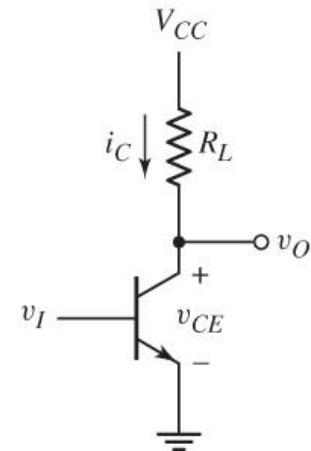
- Assuming maximum $I_p = I_{CQ}$ and $V_p = \frac{V_{CC}}{2}$

$$p_Q = i_c v_{ce} = \frac{V_{CC}I_{CQ}}{2} (1 - \sin^2 \omega t)$$

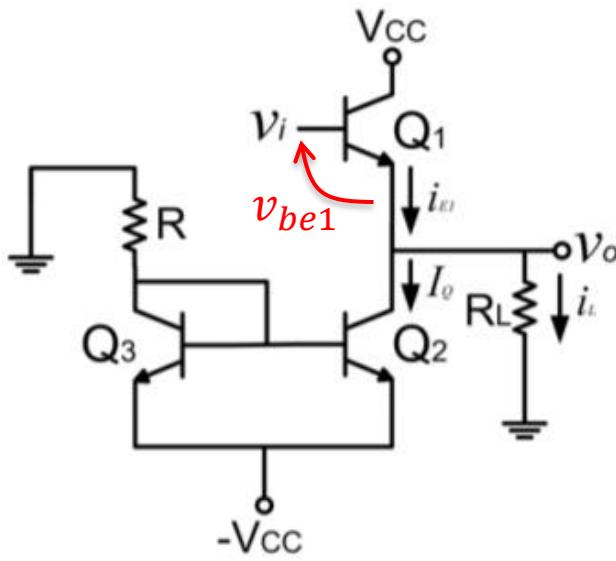


- Average ac power delivered to the load = $0.5V_pI_p = \frac{V_{CC}I_{CQ}}{4}$
- Average power supplied by the Vcc source = $V_{CC}I_{CQ}$
- Power Efficiency (η) = 25%

Consumes power even $v_I = 0$



Current Biased Class-A Emitter Follower

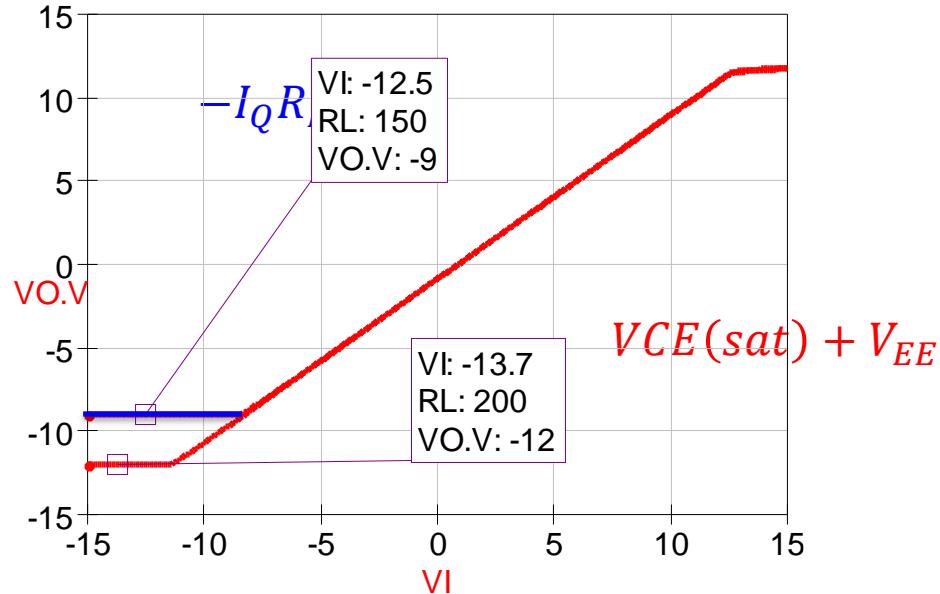
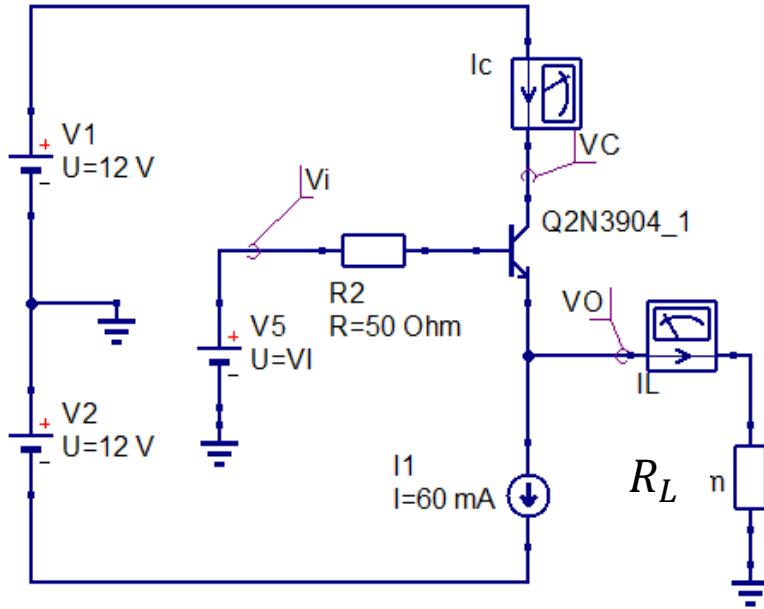


Current Mirror establishes the bias current.

$$i_{E1} = I_Q + i_L$$

- ❑ For reliable operation
 - Q₁ and Q₂ must be Forward active
 - Q₂ and Q₃ must be matched
- ❑ If $v_{be1} > 0.7 \text{ V}$, Q₁ is ON.
 - Q₁ is in forward active when $v_{ce1} > VCE(sat)$;
 $V_{cc} - v_o > VCE(sat)$
 $v_o < V_{cc} - VCE(sat) = v_{o-max}$
 $v_{I-max} = v_{o-max} + 0.7$
- ❑ If $v_{be1} < 0.7 \text{ V}$, Q₁ is OFF.
 - For Q₂ to be active: $v_{ce2} > VCE(sat)$
 $v_o > VCE(sat) + V_{EE} = v_{o-min}$
 - Also, since Q₁ is OFF, $i_{E1} = 0$

Current Biased Class-A Emitter Follower



- ❑ Lowest value of v_o depends on I_Q and R_L .
- ❑ For maximum output swing: $I \geq \frac{|VCE(sat)+V_{EE}|}{R_L}$

Class-A Amplifier

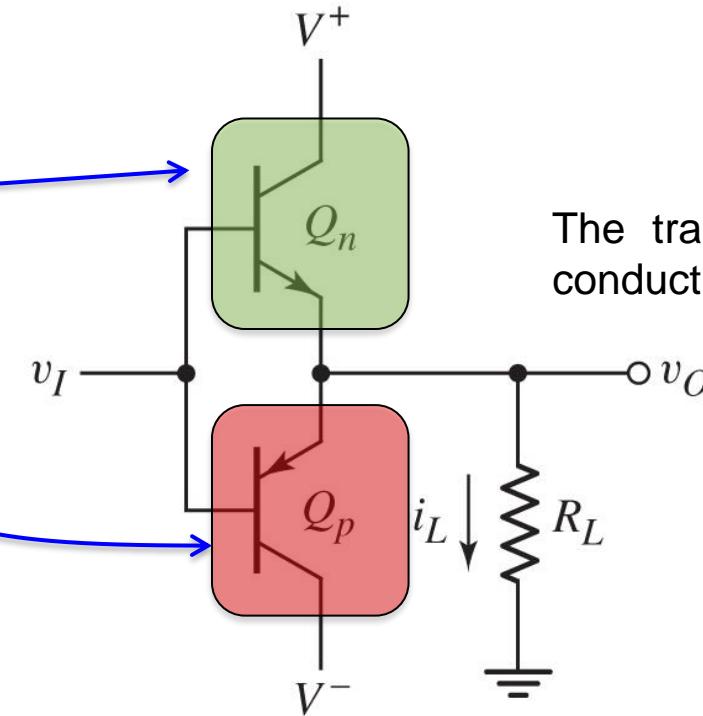
- ❑ Often used as op amp output stage and some audio output power amplifiers.
- ❑ Relatively high input impedance.
- ❑ The class A amplifier provides as a nearly linear amplification.
- ❑ No harmonic distortion.
- ❑ The maximum power conversion efficiency that can be obtained is 25%, which means 75% of the power supplied by the sources is dissipated in the transistors.
 - This is a waste of power, and could lead to a serious heating issue with the transistors.
 - When no signal is applied, it consumes power – zero percent efficiency!

Class-B

- Uses complimentary transistors and dual power supplies → **complementary push-pull output stage**

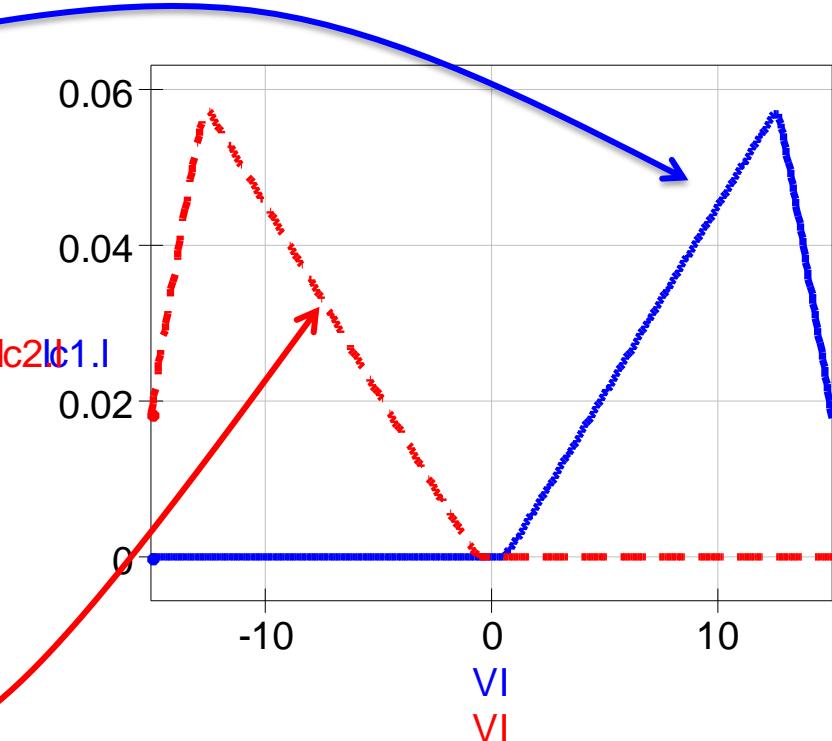
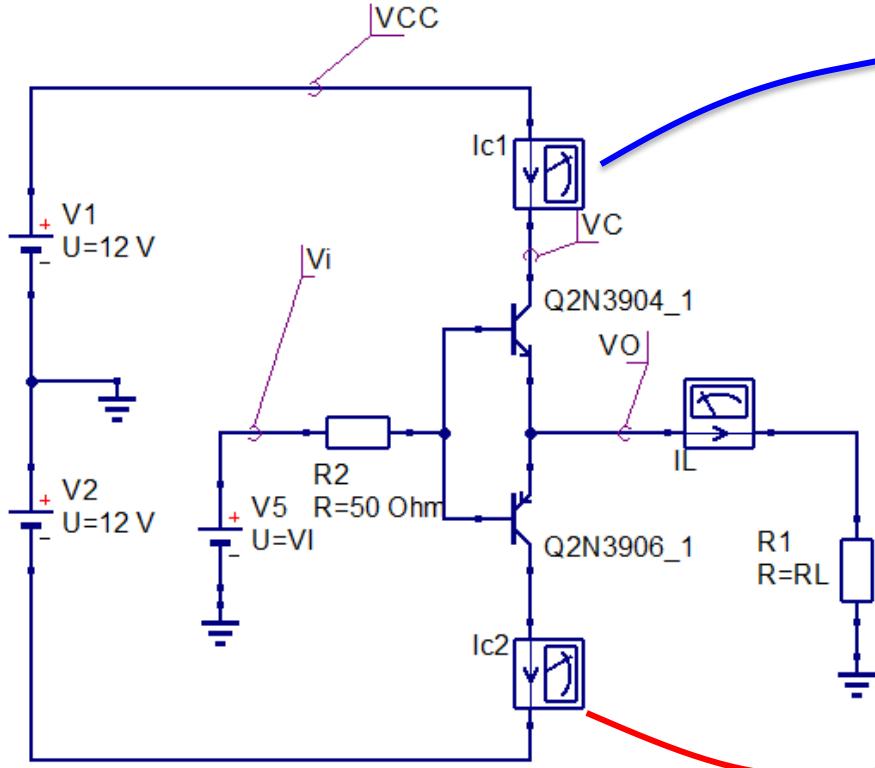
conducts during the positive half of the input cycle

conducts during the negative half-cycle.

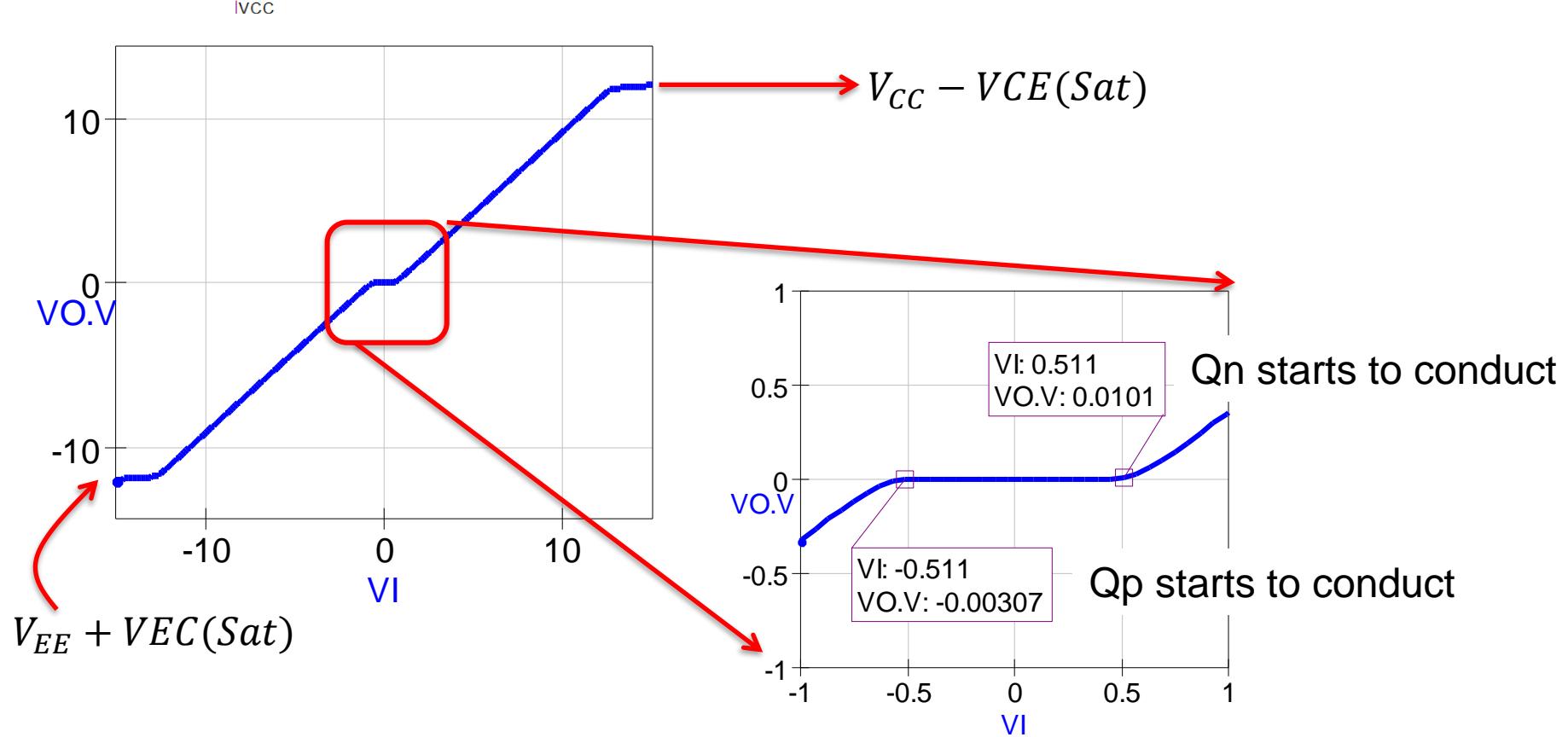


The transistors do not both conduct at the same time.

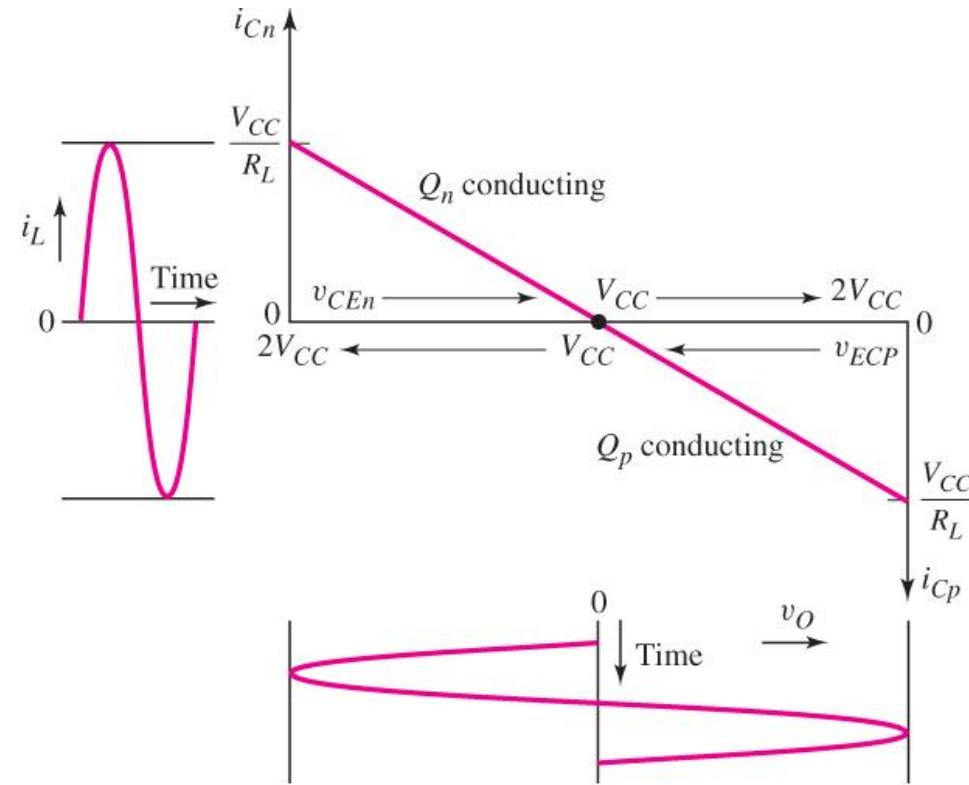
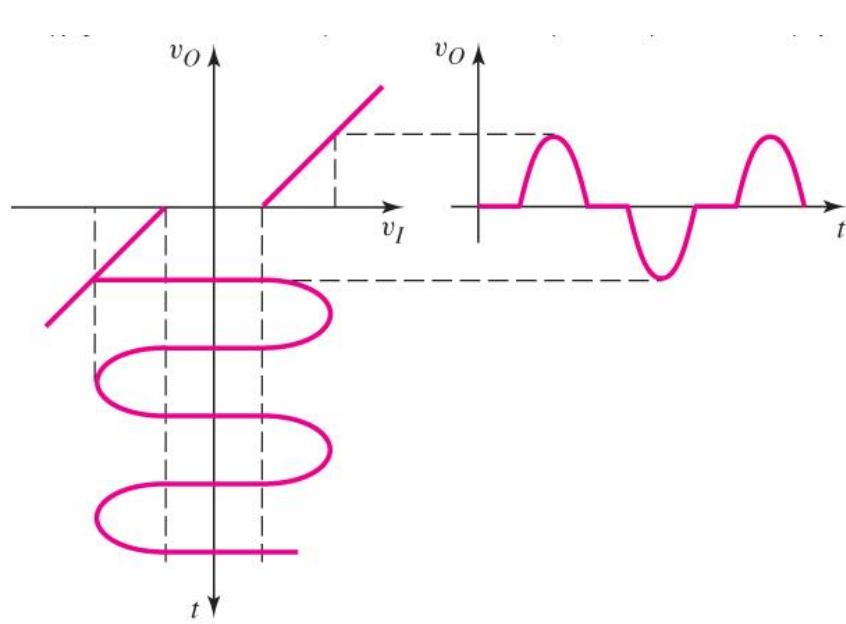
Class-B Operation



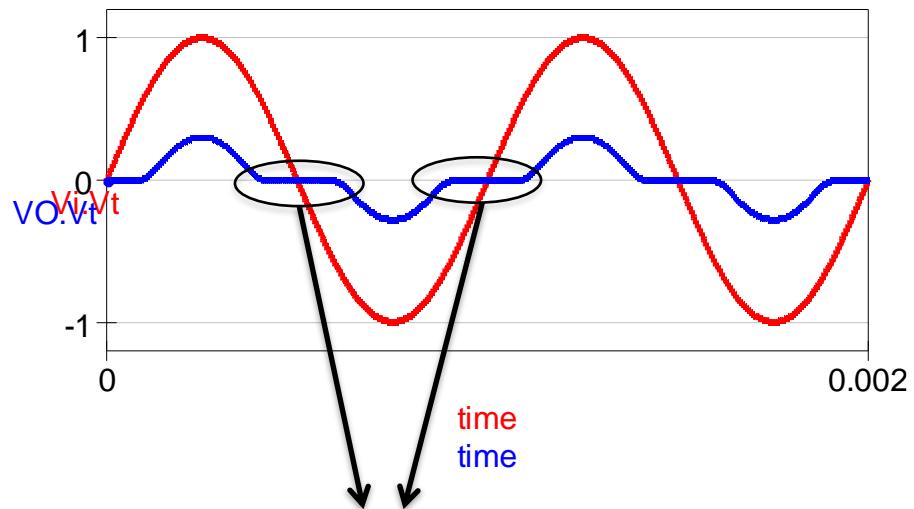
Class-B: Voltage Transfer Characteristics



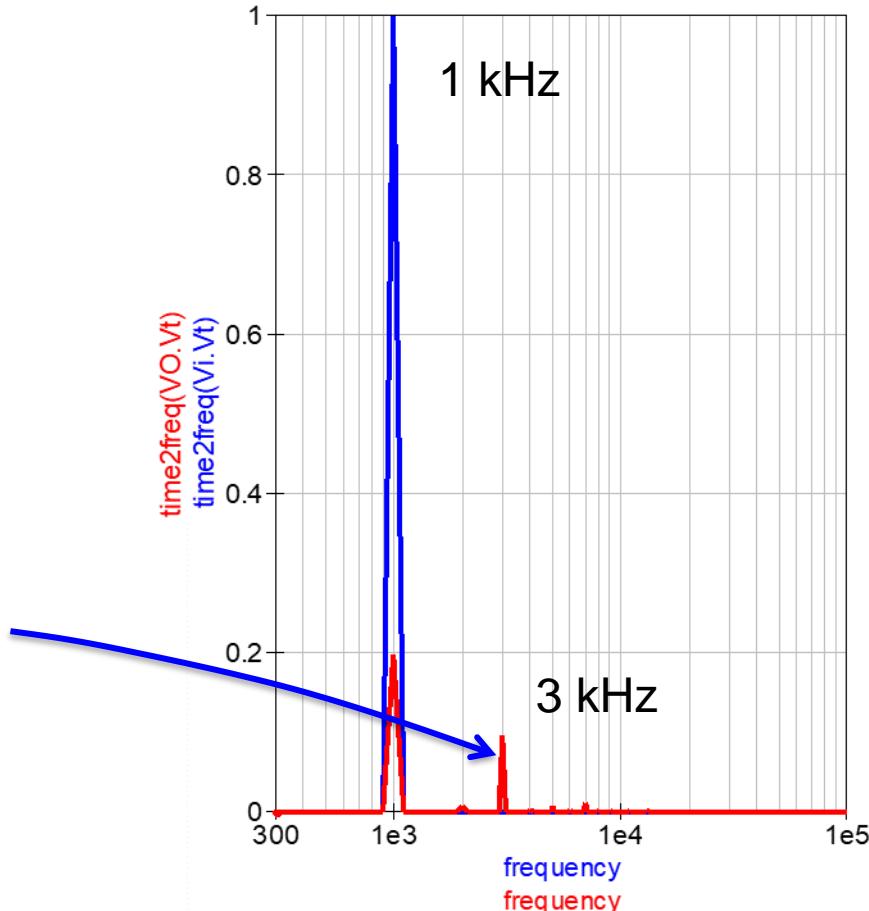
Class-B: Output Waveform Distortion



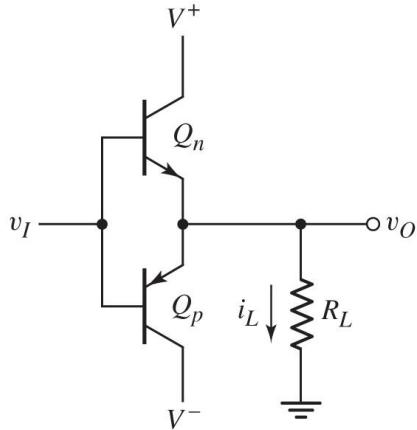
Class B: Output Waveform Distortion



Crossover distortion produces
unpleasant sounds in audio amplifiers



Class-B: Power Efficiency



- ❑ Assume $v_o = V_o \sin(\omega t)$; ignore the dead-zone at $V_i=0$ and $V_{CE}(\text{sat}) = 0$ (therefore $-V_{CC} \leq v_o \leq V_{CC}$)
- ❑ During positive half-cycle current draws from $V+$, and in negative half-cycle current draws from $V-$

Average power to the load: $P_{avL} = V_{o\text{rms}} I_{o\text{rms}} = \frac{V_o^2}{2R_L}$

Power supplied by $V+$ and $V-$: $P_{+V} = \frac{1}{\pi} \frac{V_o}{R_L} V_{CC}$ $P_{V-} = \frac{1}{\pi} \frac{V_o}{R_L} V_{CC}$

Total Power supplied: $P_{Dav} = \frac{2}{\pi} \frac{V_o}{R_L} V_{CC}$ Since $V_{o\text{max}} = V_{CC}$

Efficiency $\eta = \frac{P_{Lav}}{P_{Dav}} = \frac{\frac{V_o^2}{2R_L}}{\frac{2V_oV_{CC}}{\pi R_L}} = \frac{\pi}{4} \frac{V_o}{V_{CC}}$ $\eta_{\text{max}} = \frac{\pi}{4} = 0.785 \Rightarrow \eta_{\text{max}} = 78.5\%$

Class-B: Power Dissipation in Transistors

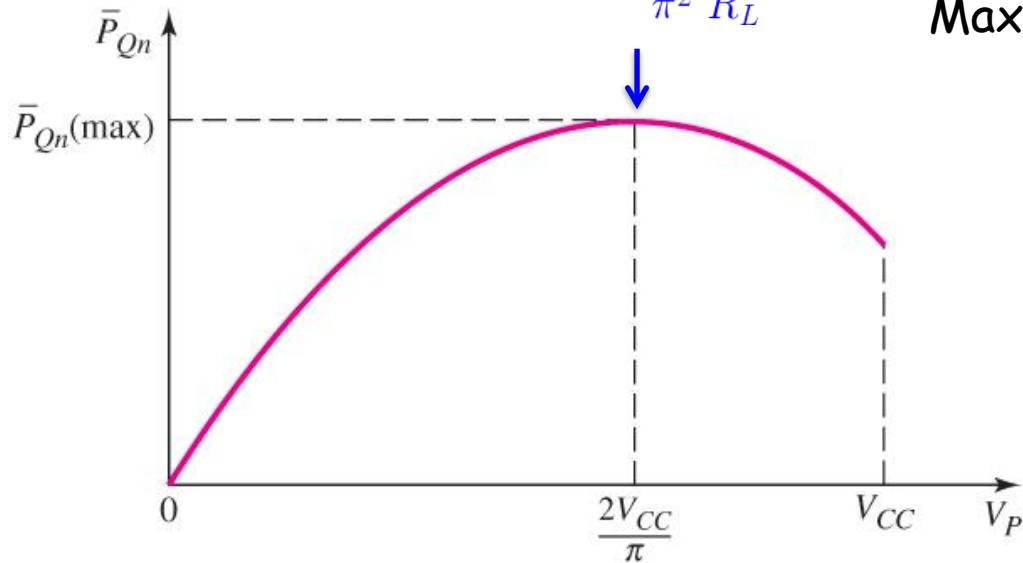
- Power dissipation in transistors: $P_{DQ} = P_{Dav} - P_{Lav} = \frac{2}{\pi} \frac{V_o V_{CC}}{R_L} - \frac{1}{2} \frac{V_o^2}{R_L}$
- When V_o is zero, $P_{DQ} = 0$

$$P_D^{max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R_L}$$

Maximum power dissipation:

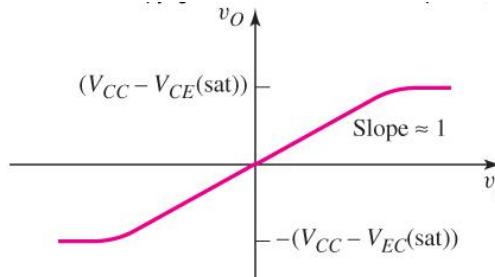
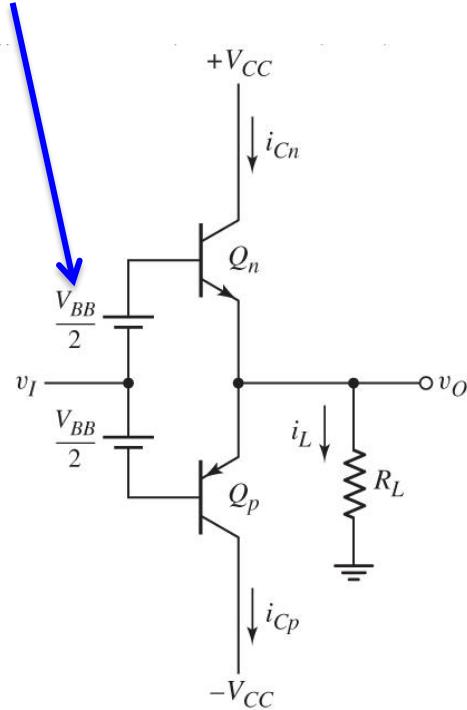
$$\frac{dP_D}{dV_o} = \frac{2}{\pi R_L} V_{CC} - \frac{V_o}{R_L} = 0$$

$$\Rightarrow V_o^{peak} = \frac{2}{\pi} V_{CC} < V_{CC}$$

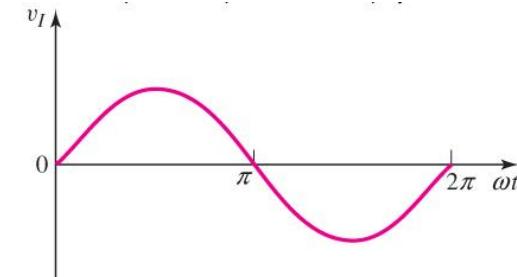


Class-AB

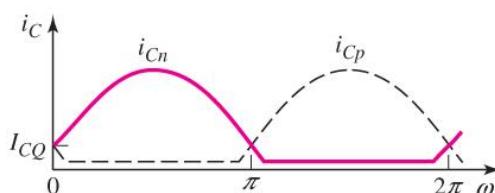
Supply bias voltages so that both transistors are turned on, with small quiescent current



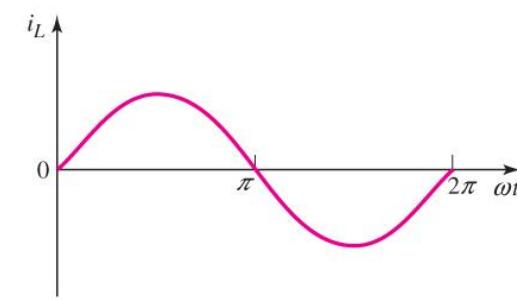
(a)



(b)

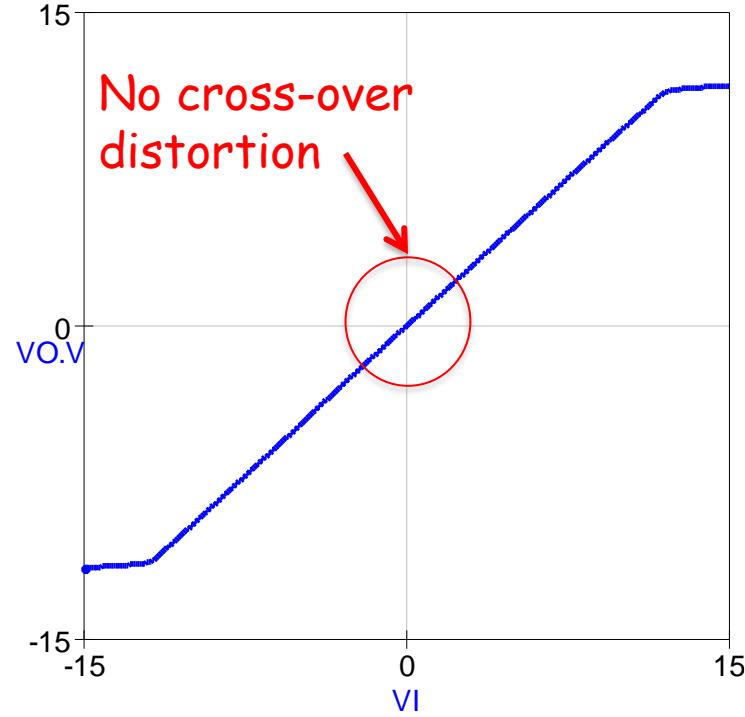
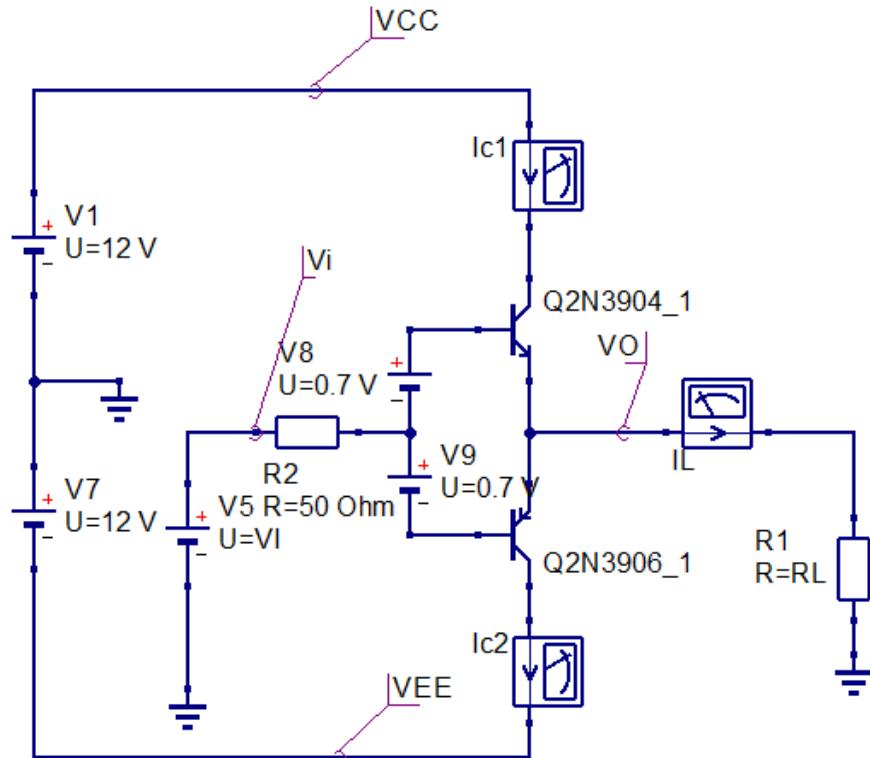


(c)

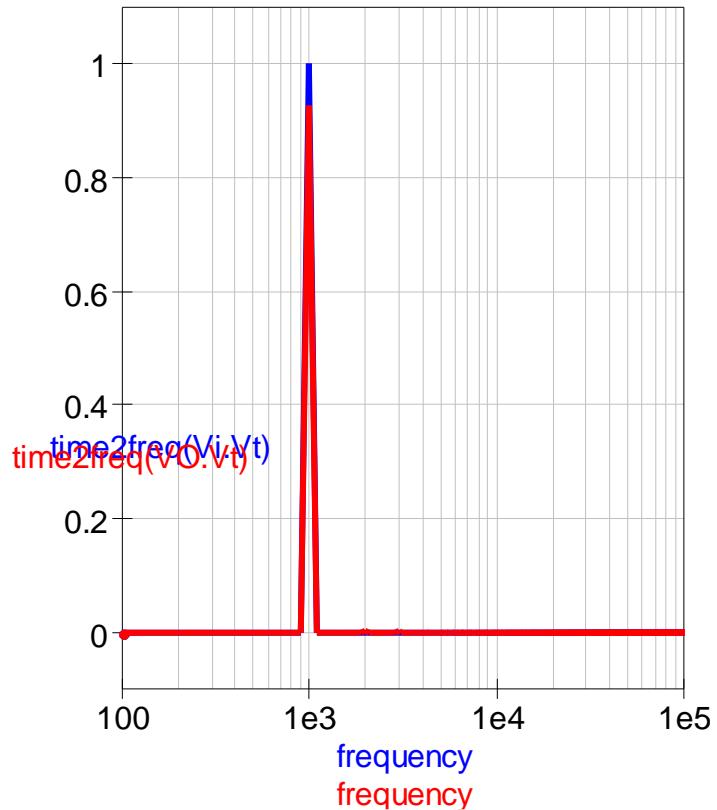
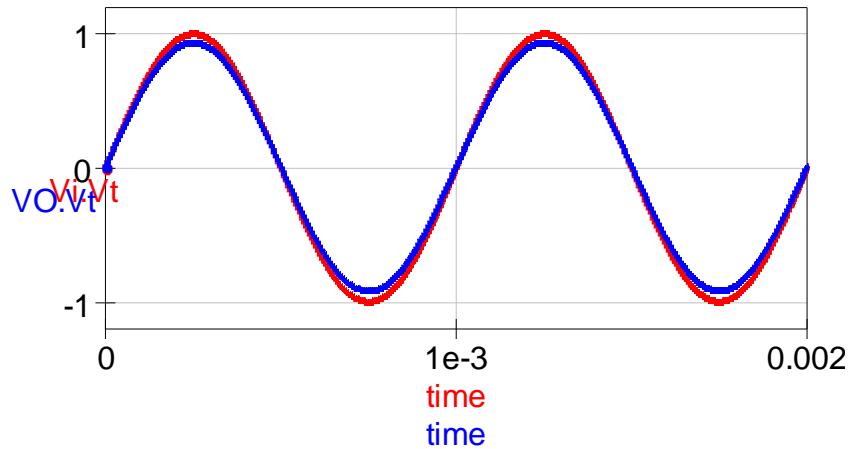


(d)

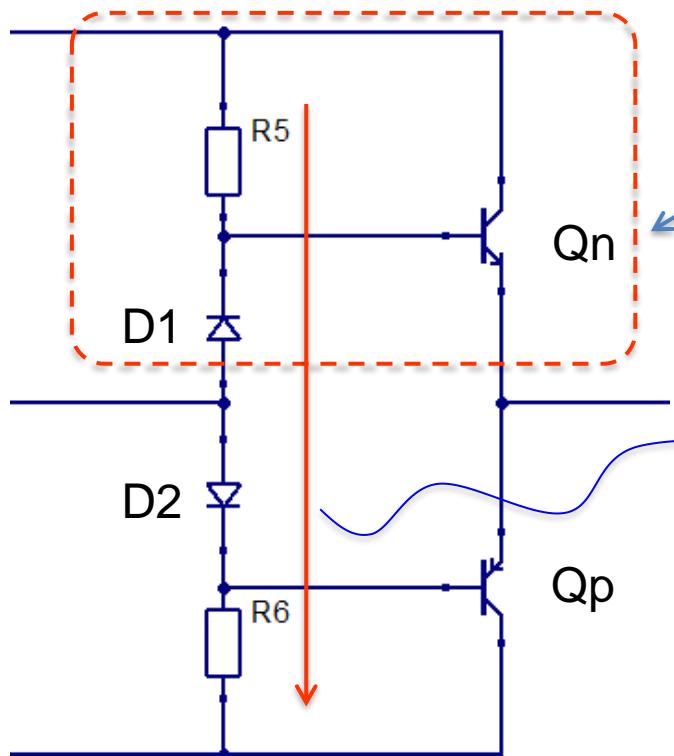
Class-AB: Voltage Transfer Curve



Class-AB: Signal Distortion



Class-AB: Current-Mirror Biasing



- D1 and D2 are diode-connected transistors identical to QN and QP, respectively.

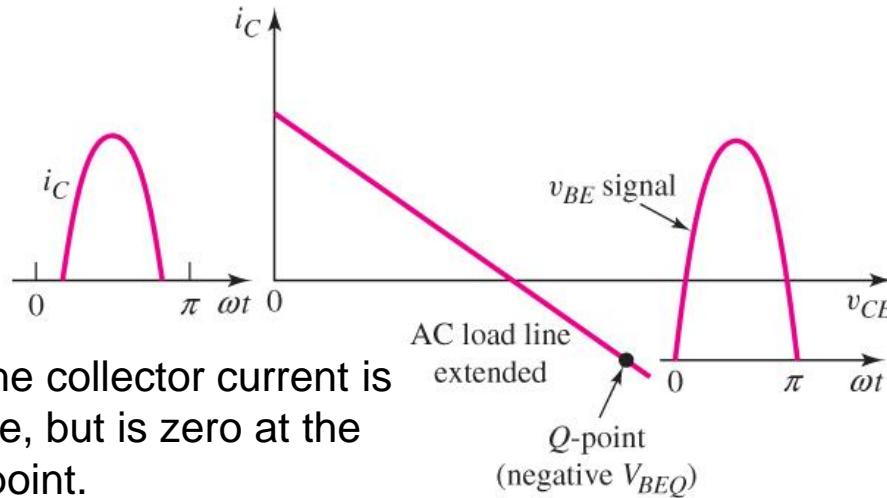
current mirror

- D1 and Qn (and D2 and Qp) should be matched.

$$I_Q = \frac{2V_{CC} - 2V_T}{2R} = \frac{V_{CC} - V_T}{R}$$

Class-C

- For class-C operation, the transistor has a reverse-biased B–E voltage at the Q-point.



Note that the collector current is not negative, but is zero at the quiescent point.

The transistor conducts only when the input signal becomes sufficiently positive during its positive half-cycle.

Class-C amplifiers are capable of providing large amounts of power, with conversion efficiencies larger than 78.5 percent.
These amplifiers are normally used for radio-frequency (RF) circuits

Summary

Class A	Class B	Class AB
Conducts over entire input cycle.	Conducts over 1/2 input cycle (each BJT).	Conducts over >1/2 input cycle (each BJT).
Low THD except when signal amplitude is large.	No power dissipated when $v_i = 0$. Higher efficiency than class A	Reduced THD over Class B. Power conversion efficiency similar to Class B
Conducts current and dissipates power when input is zero.	High THD even when signal amplitude is small.	Increased power dissipation over Class B.

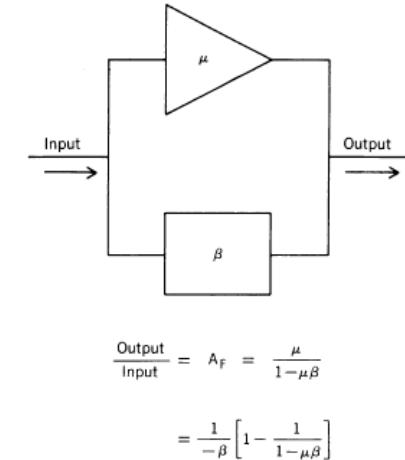
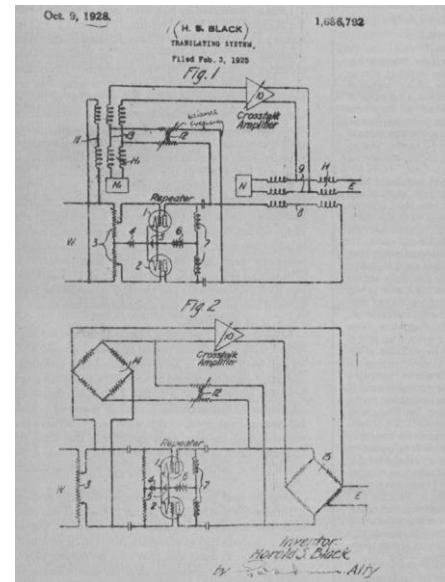
10. Feedback Amplifiers

Introduction

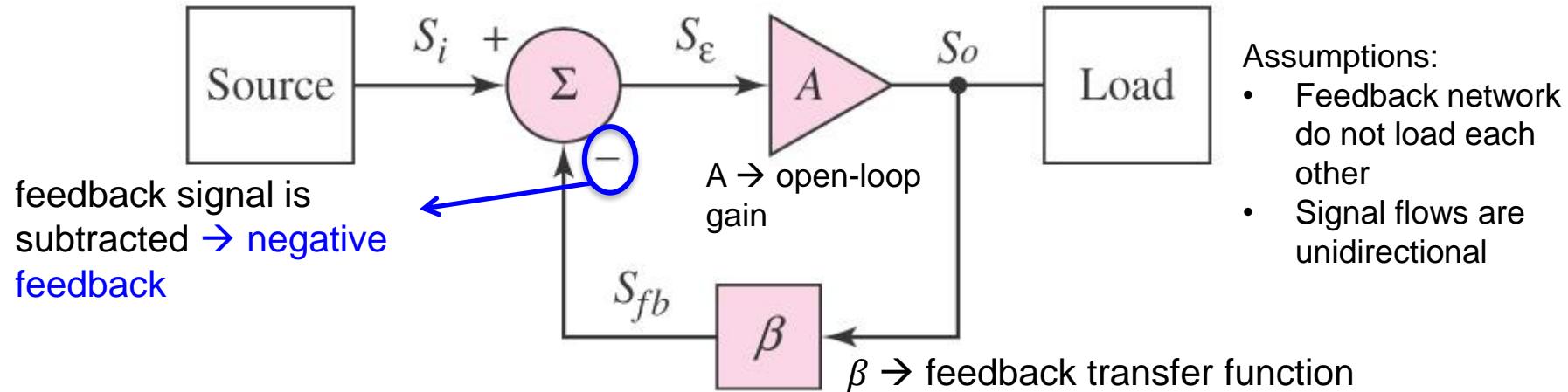
- ❑ Feedback is used virtually in all amplifier systems.
- ❑ Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier in 1928

- To manage the signal loss in long distance telephone lines, signal was amplified at several points – we call them repeaters.
- Every time the signal is amplified, noise is added and amplified.
- Black's amplifier compares the input and output signals and then negatively amplifies the distortion and combines the two signals, cancelling out some of the distortion

C. Desoer, "In memoriam: Harold Stephen Black (1898-1983)," in *IEEE Transactions on Automatic Control*, vol. 29, no. 8, pp. 673-674, August 1984
H. S. Black, "Inventing the negative feedback amplifier," *IEEE Spectrum*, pp. 55-60, Dec. 1977.



Basic Feedback Concepts

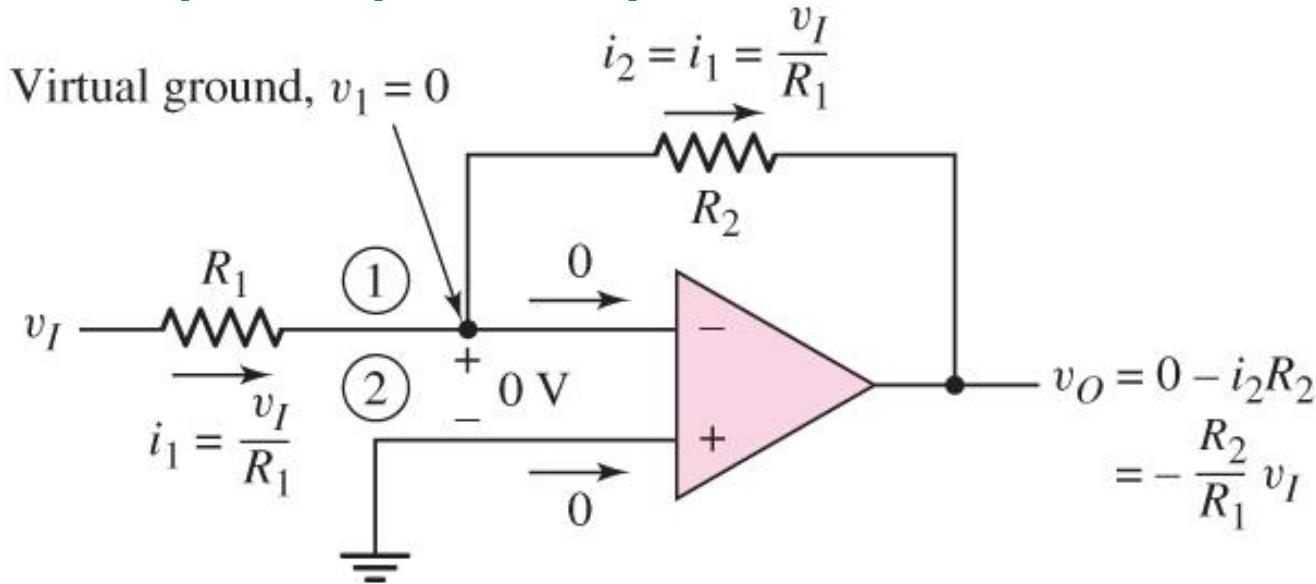


$$\text{closed-loop gain } (A_f) = \frac{S_o}{S_i} = \frac{A}{1 + \beta A} = \frac{A}{1 + T}$$

$T = \beta A \rightarrow$ loop-gain (T>0 for negative feedback; T<0 for positive feedback)

If $T = \beta A \gg 1$ then, we have $A_f \approx \frac{A}{\beta A} = \frac{1}{\beta}$

Common Op-Amp Example



Gain Sensitivity

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1 + \beta A)}$$

$$\frac{dA_f}{dA} = \frac{1}{(1 + \beta A)} - \frac{A}{(1 + \beta A)^2} \cdot \beta = \frac{1}{(1 + \beta A)^2}$$

or

$$dA_f = \frac{dA}{(1 + \beta A)^2}$$

Dividing both sides of Equation (12.11(b)) by the closed-loop gain yields

$$\frac{dA_f}{A_f} = \frac{\frac{dA}{(1 + \beta A)^2}}{\frac{A}{(1 + \beta A)}} = \frac{1}{(1 + \beta A)} \cdot \frac{dA}{A} = \left(\frac{A_f}{A}\right) \frac{dA}{A}$$

Using the same parameter values as in Example 12.1, we have $A = 10^5$, $A_f = 50$, and $\beta = 0.01999$. Assume that the change in the open-loop gain is $dA = 10^4$ (a 10 percent change).

$$dA_f = \frac{A_f}{(1 + \beta A)} \cdot \frac{dA}{A} = \frac{50}{[1 + (0.01999)(10^5)]} \cdot \frac{10^4}{10^5} = 2.5 \times 10^{-3}$$

The percent change is then

$$\frac{dA_f}{A_f} = \frac{2.5 \times 10^{-3}}{50} = 5 \times 10^{-5} \Rightarrow 0.005\%$$

compared to the 10 percent change assumed in the open-loop gain.

the % change in A_f is less than the corresponding % change in A by the factor $(1 + \beta A)$.

The change in open-loop gain may result from variations in individual transistor parameters in the basic amplifier.

Gain Versus Frequency

- Assume the frequency response of the basic amplifier can be characterized by a single pole

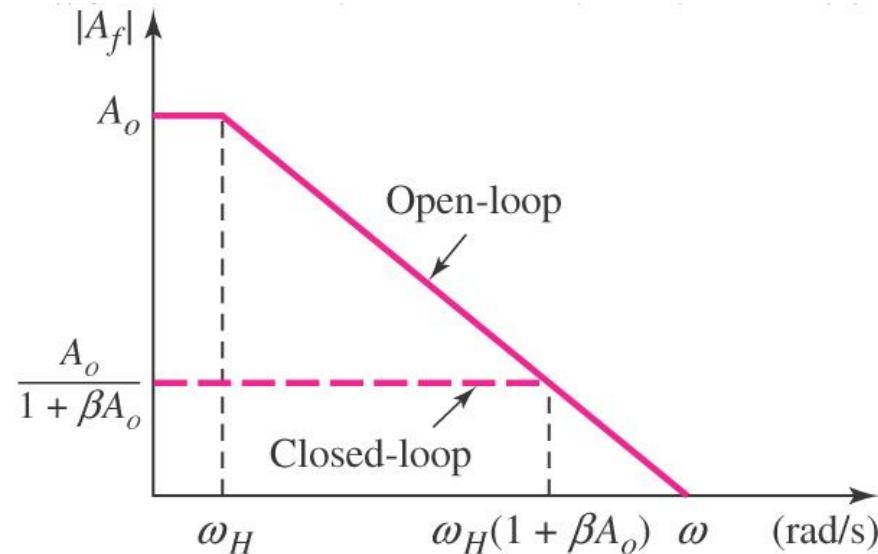
$$A(s) = \frac{A_o}{1 + \frac{s}{\omega_H}} \quad A_f(s) = \frac{A(s)}{(1 + \beta A(s))}$$

We assume that feedback gain (β) is frequency independent.

$$A_f(s) = \frac{\frac{A_o}{(1 + \beta A_o)}}{1 + \frac{1}{\omega_H(1 + \beta A_o)s}}$$

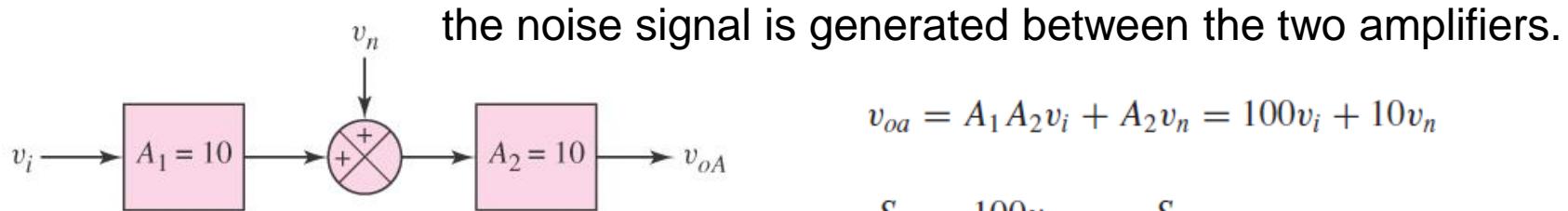
The closed-loop gain is smaller than the open-loop gain by a factor $(1+\beta A)$

The 3 dB bandwidth is larger by a factor $(1+\beta A)$



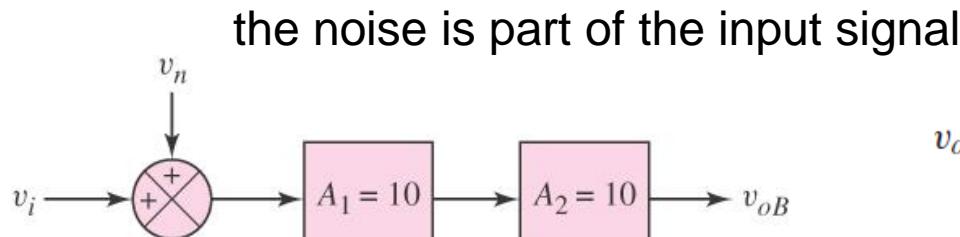
- Gain-Bandwidth product is constant
- Bandwidth increases at the expense of gain

Signal-to-Noise Ratio: Two Open Loop Amplifiers



$$v_{oa} = A_1 A_2 v_i + A_2 v_n = 100v_i + 10v_n$$

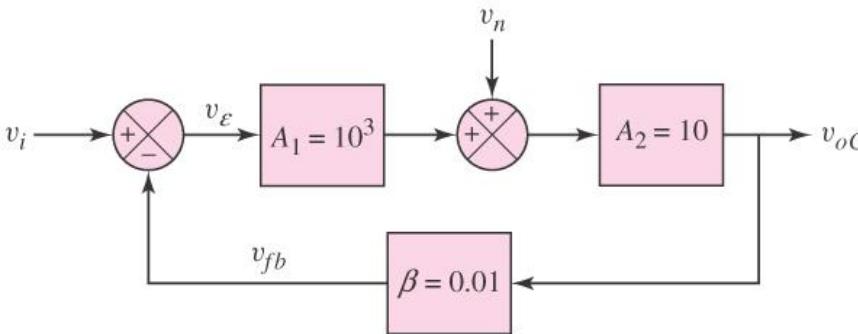
$$\frac{S_o}{N_o} = \frac{100v_i}{10v_n} = 10 \frac{S_i}{N_i}$$



$$v_{ob} = A_1 A_2 v_i + A_1 A_2 v_n = 100v_i + 100v_n$$

$$\frac{S_o}{N_o} = \frac{100v_i}{100v_n} = \frac{S_i}{N_i}$$

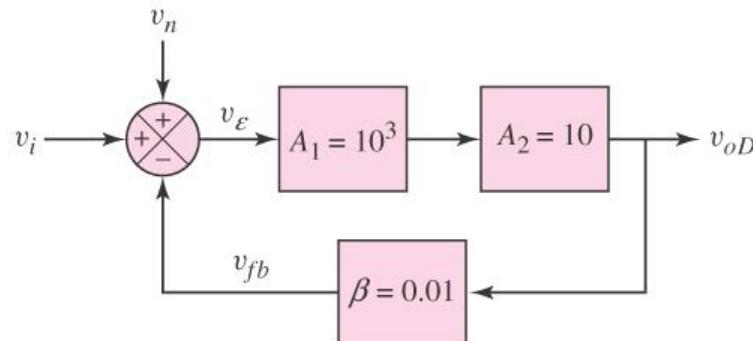
Signal-to-Noise Ratio: Feedback Configuration



$$v_{oc} = \frac{A_1 A_2}{(1 + \beta A_1 A_2)} \cdot v_i + \frac{A_2}{(1 + \beta A_1 A_2)} \cdot v_n \cong 100v_i + 0.1v_n$$

$$\frac{S_o}{N_o} = \frac{100v_i}{0.1v_n} = 1000 \frac{S_i}{N_i}$$

Negative feedback can reduce internally generated additive amplifier noise (improve SNR).



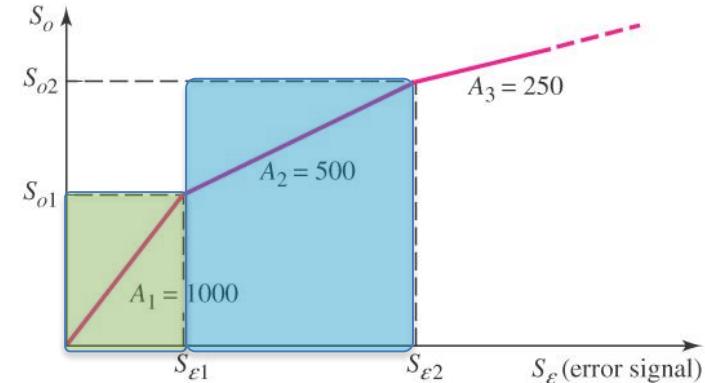
$$v_{od} = \frac{A_1 A_2}{(1 + \beta A_1 A_2)} (v_i + v_n) \cong 100v_i + 100v_n$$

$$\frac{S_o}{N_o} = \frac{100v_i}{100v_n} = \frac{S_i}{N_i}$$

Feedback mechanism does not improve SNR due to external noise

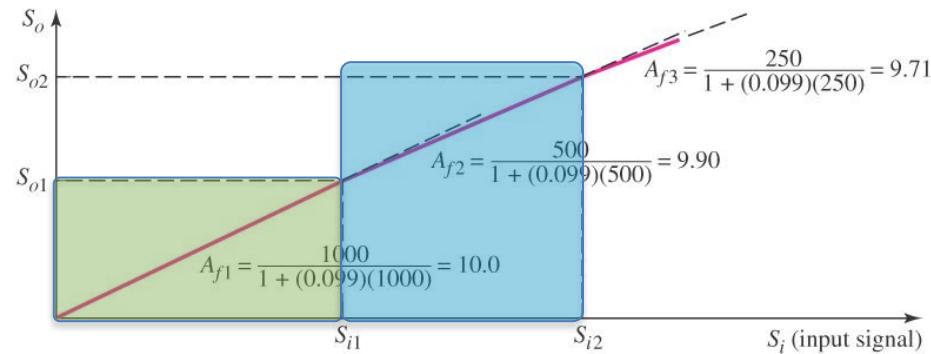
Reduction of Nonlinear Distortion

Basic amplifier (open-loop) transfer function is non-linear because the gain depends on the signal frequency. This is due to transistor non-linearities in high frequencies.



Amplifier is incorporated in a feedback circuit with a feedback transfer function of $\beta = 0.099$

Then $A_f \approx \frac{1}{\beta} \rightarrow$ which means closed-loop gain is independent of open-loop gain!



Negative Feedback: Pros and Cons

❑ Pros:

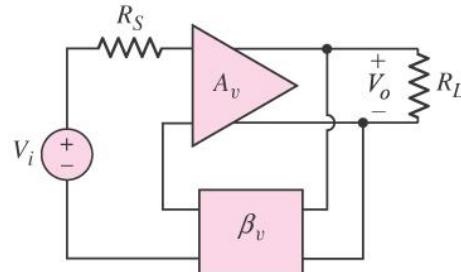
- **Gain sensitivity:** Variations in gain is reduced.
- **Bandwidth extension:** BW is larger than that of basic amplifier
- **Noise sensitivity:** May increase the SNR.
- **Reduction of nonlinear distortion.**
- **Control of impedance levels:** The input and output impedances can be increased or decreased

❑ Cons:

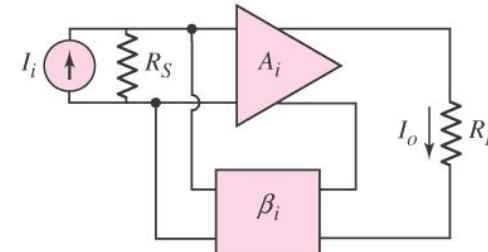
- **Reduced Circuit gain:** The overall amplifier gain is reduced.
- **Stability:** There is a possibility that the feedback circuit may become unstable (oscillate) at high frequencies.

Feedback Topologies

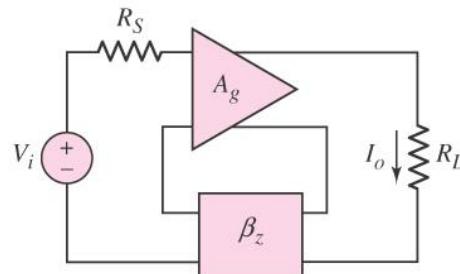
- four basic feedback topologies, based on the parameter to be amplified (voltage or current) and the output parameter (voltage or current).



(a) Series-shunt

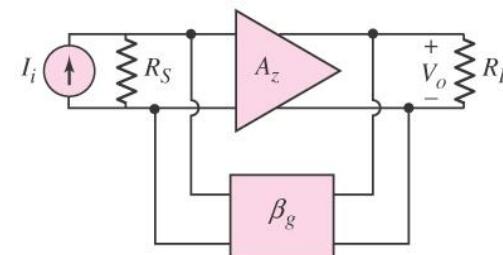


(b) Shunt-series



(c) Series-series

transconductance amplifier
(voltage in current out)



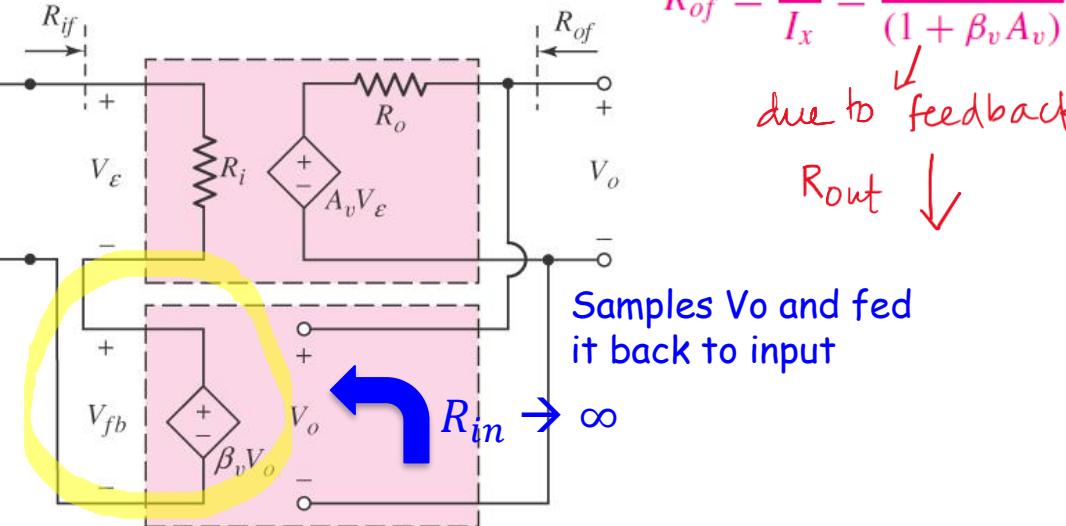
(d) Shunt-shunt

Trans-resistance amplifier
(current in voltage out)

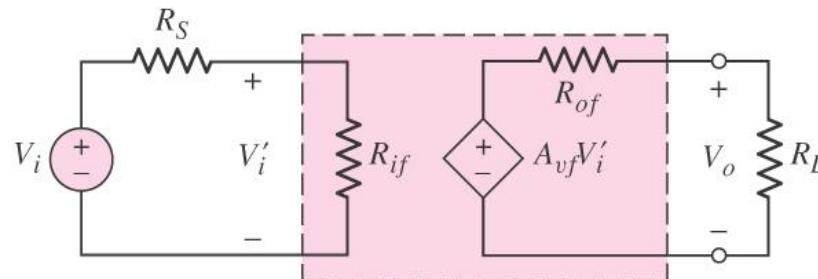
Ideal Series-Shunt Feedback

$$R_{if} = \frac{V_i}{I_i} = R_i(1 + \beta_v A_v)$$

Feedback voltage (V_{fb}) is subtracted from the input (V_i)



$$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{(1 + \beta_v A_v)}$$

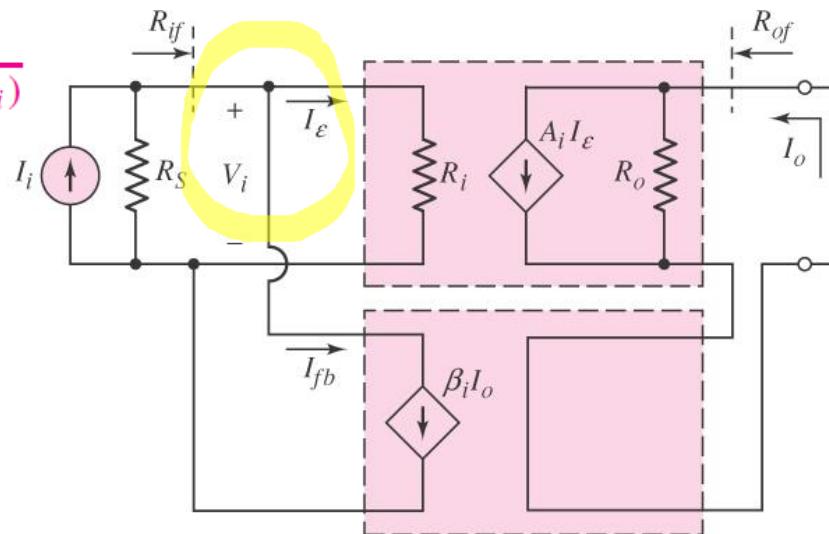


Ideal Shunt-Series Feedback

$$R_{if} = \frac{V_i}{I_i} = \frac{R_i}{(1 + \beta_i A_i)}$$

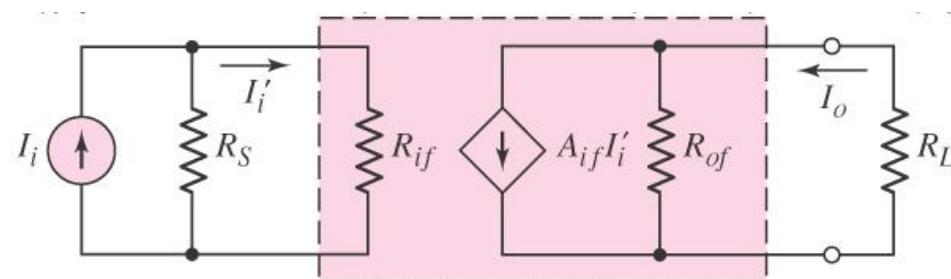
Feedback current (Ifb) is subtracted from the input (Ii)
 $I_e = I_i - I_{fb}$

$$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{(1 + \beta_i A_i)}$$



$$R_{of} = \frac{V_x}{I_x} = (1 + \beta_i A_i) R_o$$

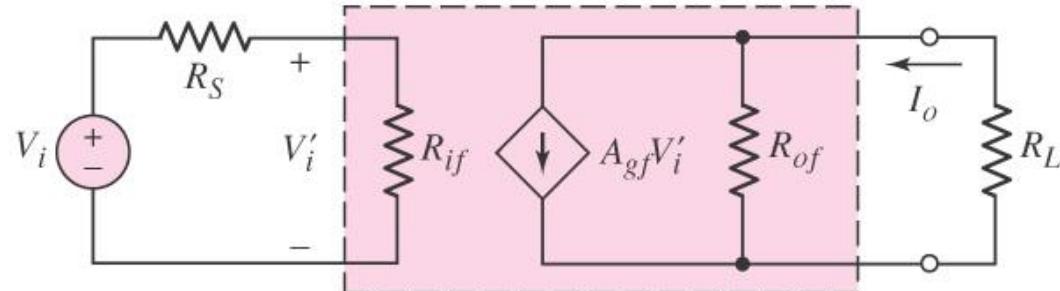
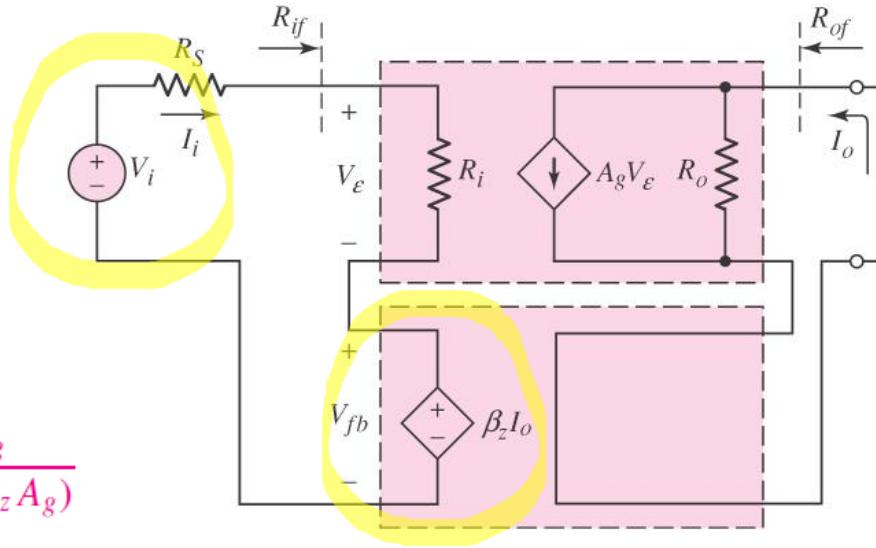
Sample output current fed to input



Ideal Series-Series Feedback

Feedback voltage (V_{fb}) is subtracted from the input (V_i)

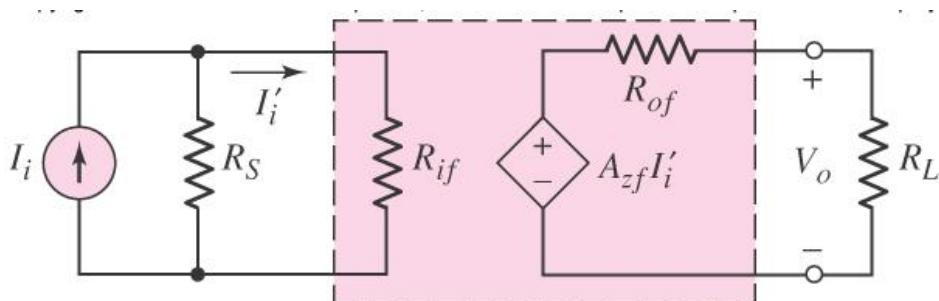
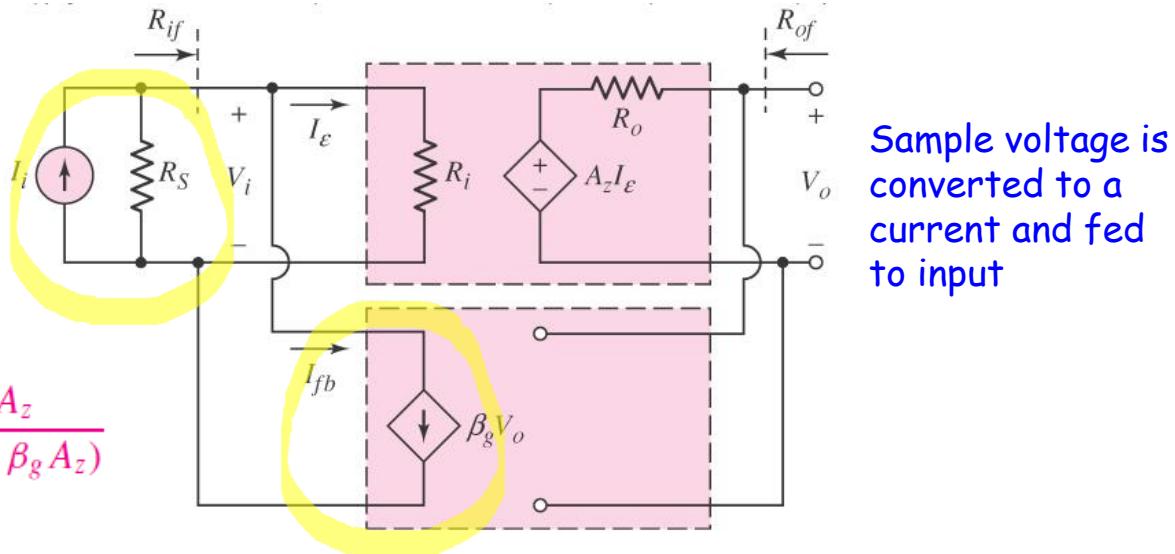
$$A_{gf} = \frac{I_o}{V_i} = \frac{A_g}{(1 + \beta_z A_g)}$$



Ideal Shunt-Shunt Feedback

Feedback current (Ifb) is subtracted from the input (Ii)
 $I_e = I_i - I_{fb}$

$$A_{zf} = \frac{V_o}{I_i} = \frac{A_z}{(1 + \beta_g A_z)}$$



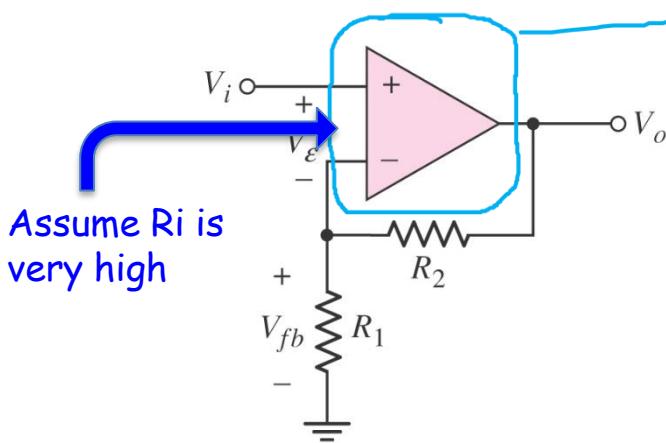
Summary Feedback Amplifier functions

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Table 12.1 Summary results of feedback amplifier functions for the ideal feedback circuit

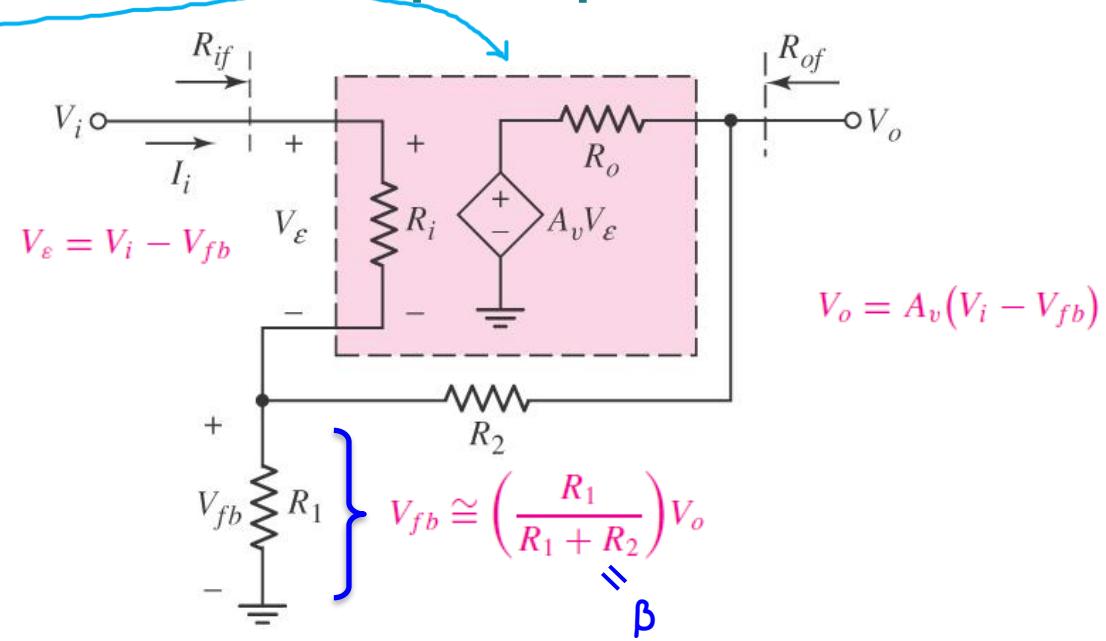
Feedback amplifier	Source signal	Output signal	Transfer function	Input resistance	Output resistance
Series-shunt (voltage amplifier)	Voltage	Voltage	$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{(1 + \beta_v A_v)}$	$R_i(1 + \beta_v A_v)$	$\frac{R_o}{(1 + \beta_v A_v)}$
Shunt-series (current amplifier)	Current	Current	$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{(1 + \beta_i A_i)}$	$\frac{R_i}{(1 + \beta_i A_i)}$	$R_o(1 + \beta_i A_i)$
Series-series (transconductance amplifier)	Voltage	Current	$A_{gf} = \frac{I_o}{V_i} = \frac{A_g}{(1 + \beta_z A_g)}$	$R_i(1 + \beta_z A_g)$	$R_o(1 + \beta_z A_g)$
Shunt-shunt (transresistance amplifier)	Current	Voltage	$A_{zf} = \frac{V_o}{I_i} = \frac{A_z}{(1 + \beta_g A_z)}$	$\frac{R_i}{(1 + \beta_g A_z)}$	$\frac{R_o}{(1 + \beta_g A_z)}$

Series-Shunt Feedback Circuit: OpAmp



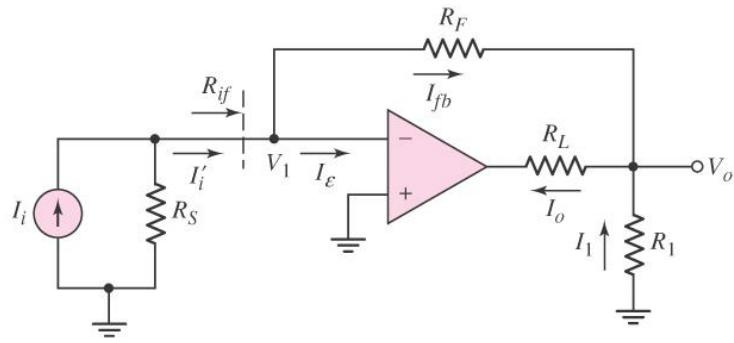
$$A_{vf} = \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right)$$

$$A_{vf} = \frac{A_v}{(1 + \beta_v A_v)}$$



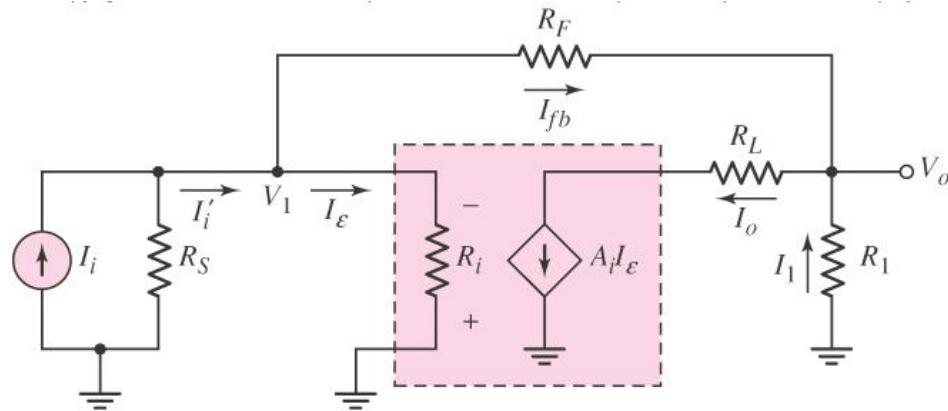
$$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{1 + \frac{A_v}{\left(1 + \frac{R_2}{R_1}\right)}}$$

Shunt-Series Feedback Circuit: OpAmp



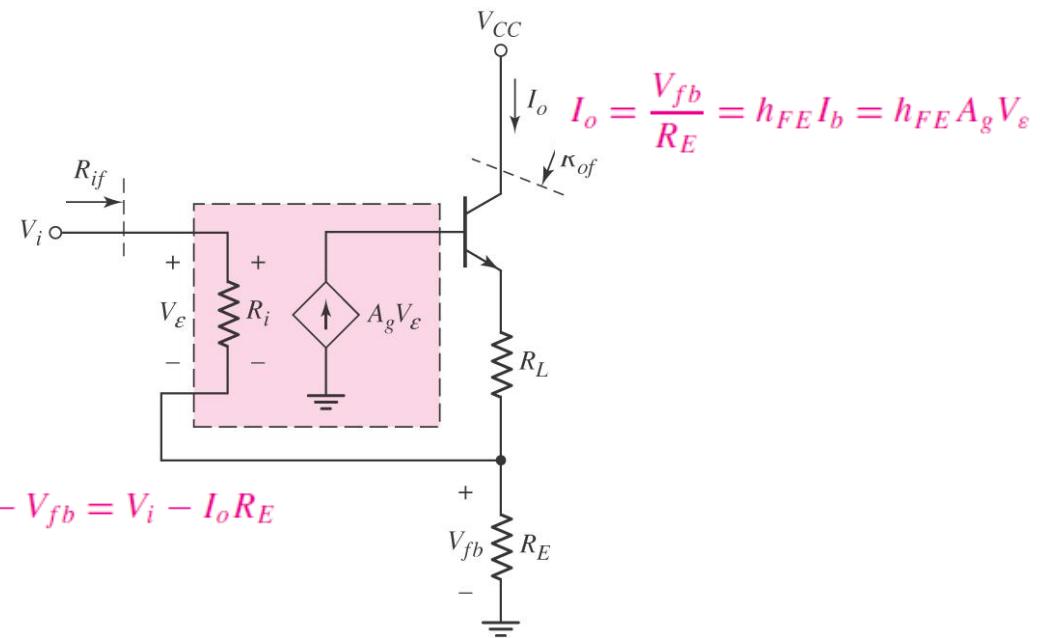
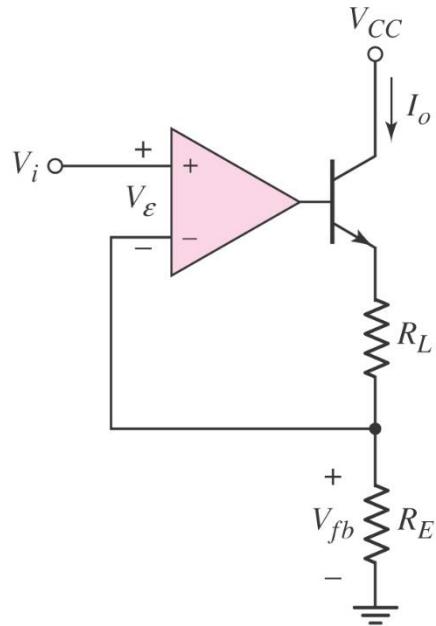
$$A_{if} = \frac{I_o}{I_i} \cong \frac{1}{\beta_i}$$

$$\beta_i = \frac{1}{\left(1 + \frac{R_F}{R_1}\right)}$$



$$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{1 + \frac{A_i}{\left(1 + \frac{R_F}{R_1}\right)}}$$

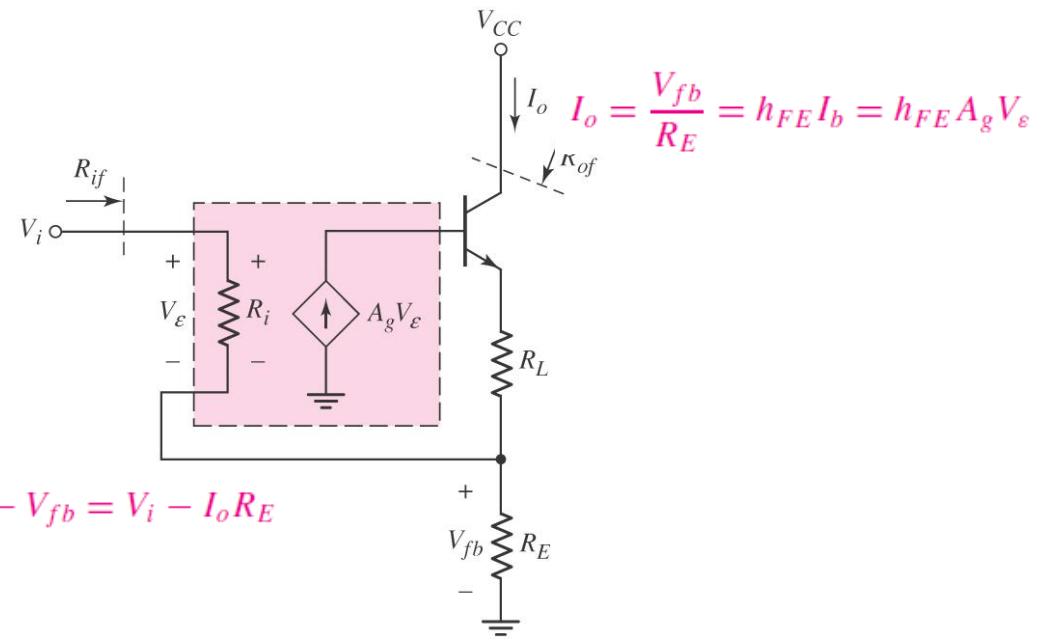
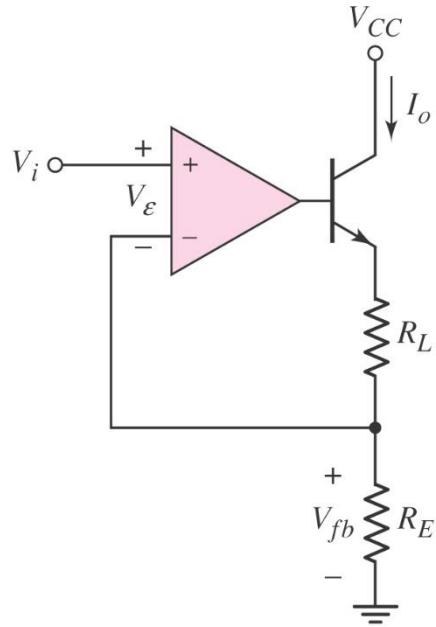
Series-Series Feedback Circuit: OpAmp



$$V_\varepsilon = V_i - V_{fb} = V_i - I_o R_E$$

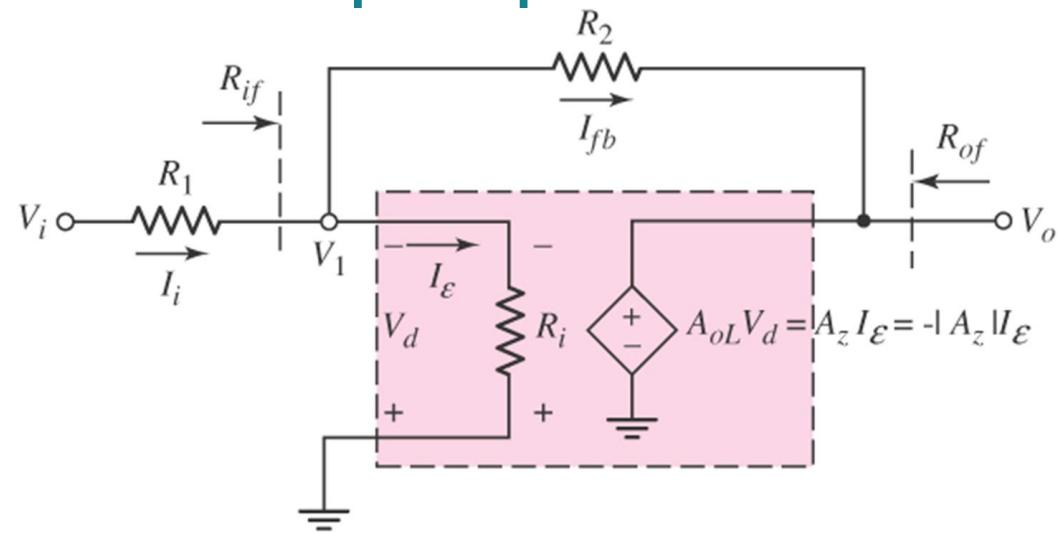
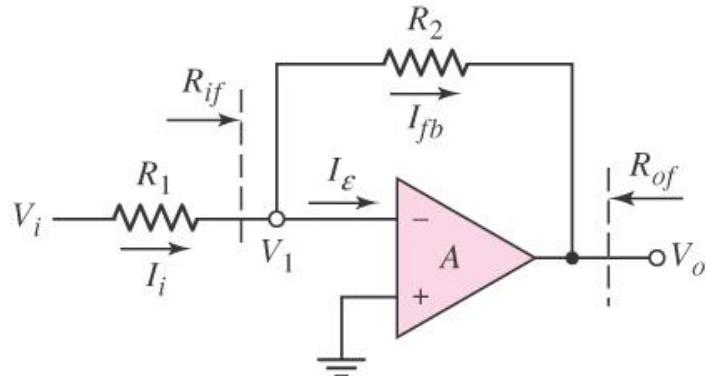
$$A_{gf} = \frac{I_o}{V_i} = \frac{(h_{FE} A_g)}{1 + (h_{FE} A_g) R_E}$$

Series-Series Feedback Circuit: Discrete



$$A_{gf} = \frac{I_o}{V_i} = \frac{(h_{FE} A_g)}{1 + (h_{FE} A_g) R_E}$$

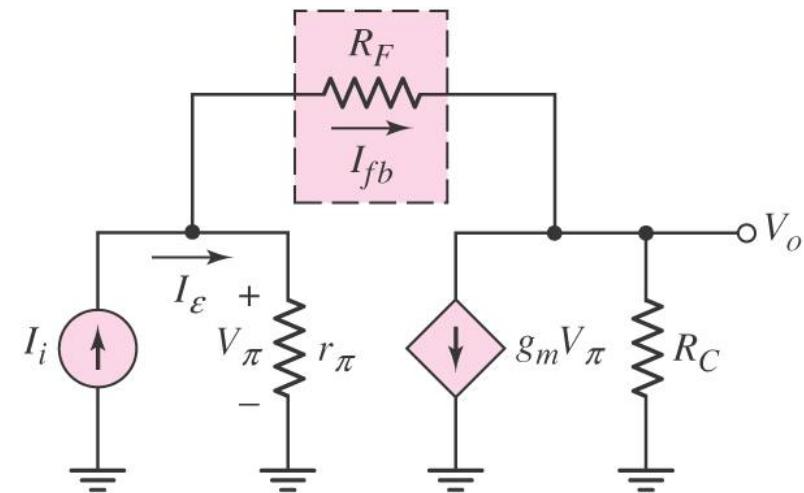
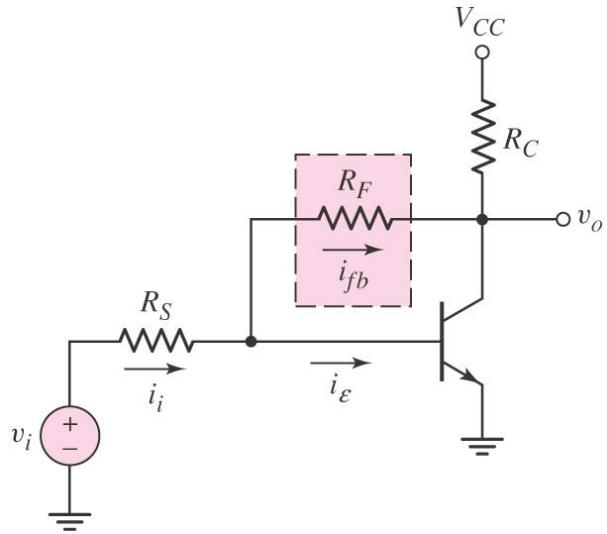
Shunt-Shunt Feedback Circuit: OpAmp



$$A_{zf} = \frac{V_o}{I_i} = \frac{-|A_z|}{1 + (-|A_z|)\beta_g} = \frac{A_z}{1 + A_z\beta_g}$$

$$\beta_g = -\frac{1}{R_2}$$

Shunt-Shunt Feedback Circuit: Discrete

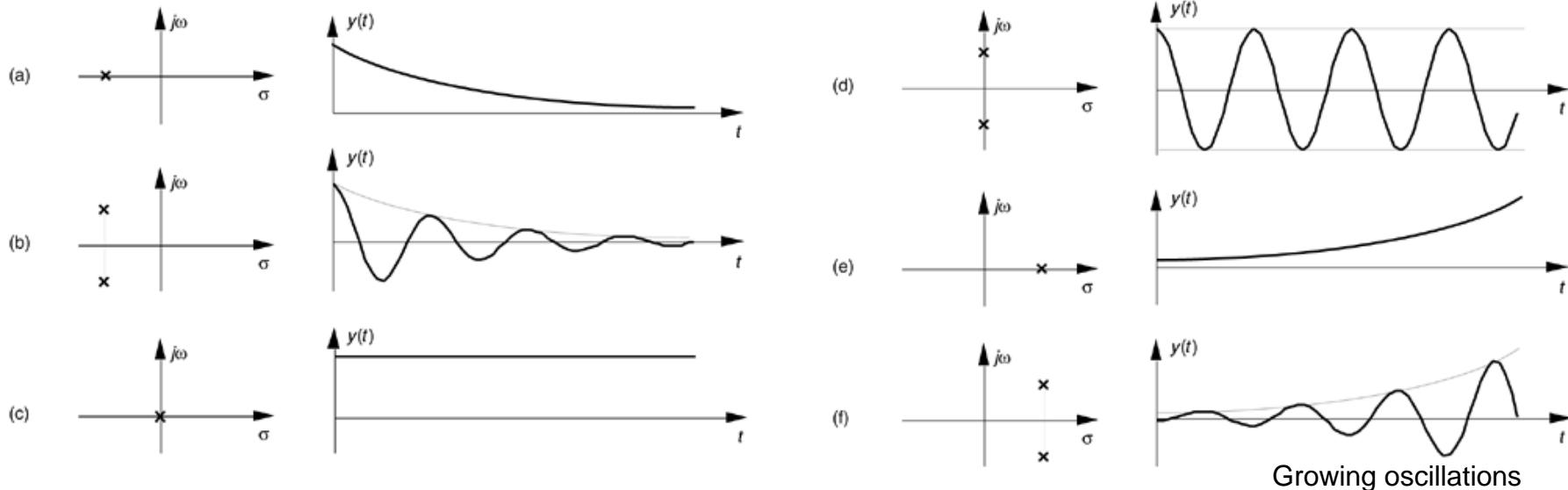


$$A_{zf} = \frac{V_o}{I_i} = \frac{+ \left(A_z + \frac{r_\pi R_C}{R_F} \right)}{\left(1 + \frac{R_C}{R_F} \right) \left(1 + \frac{r_\pi}{R_F} \right) - \frac{1}{R_F} \left(A_z + \frac{r_\pi R_C}{R_F} \right)}$$

11. Feedback Amplifier Stability

TF Pole Location and Stability

$$H(s) = \frac{1}{(s-p_1)(s-p_2)} \text{ where } p_i = \sigma_i \pm j \omega_i \text{ and } i \in (1,2)$$

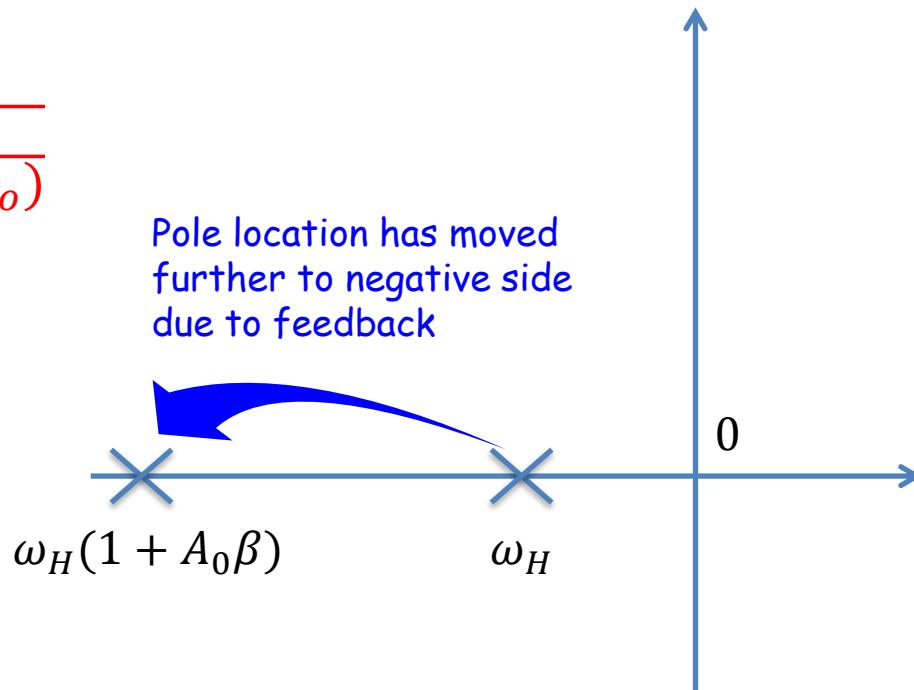


Root-Locus Analysis of Transfer Function

- the graphical representation in the s-plane of the possible locations of its closed-loop poles for varying values of a certain system parameter.

$$A_f(s) = \frac{A_o}{1 + \beta A_o} \frac{1}{1 + \frac{s}{\omega_H(1 + \beta A_o)}}$$

Pole location has moved further to negative side due to feedback



Stability problem

$$A_f = \frac{A}{1 + \beta A}$$

A is a function of frequency
β is frequency independent



$$A_f(j\omega) = \frac{A(j\omega)}{1 + T(j\omega)}$$

- $T(j\omega) = |T(j\omega)|e^{j\phi(\omega)}$ → changes with frequency. $T(j\omega) > 0$ for negative feedback.
- When $\phi(\omega) = \pi$, $e^{j\phi(\omega)} = -1$ and $T(j\omega)$ will be negative.

Case 1: $|T(j\omega)| = 1$, $A_f(j\omega) \rightarrow \infty$: System is unstable. an output will exist for a zero input

Case 2: $|T(j\omega)| > 1$, $A_f(j\omega) < 0$: ($A_f < A$ @ $\phi = 180^\circ$) Sustained oscillations (Oscillators).

Case 3: $|T(j\omega)| < 1$, $A_f(j\omega) > 0$: ($A_f > A$ @ $\phi = 180^\circ$) System is stable.

For stability: $|T(j\omega)| < 1$ when $\phi = 180^\circ$

Barkhausen's Criteria



Stability Criteria example (I)

Objective: Determine the stability of an amplifier, given the loop gain function.

Consider a three-pole feedback amplifier with a loop gain given by

$$T(f) = \frac{\beta(100)}{\left(1 + j\frac{f}{10^5}\right)^3}$$

In this case, the three poles all occur at the same frequency. Determine the stability of the amplifier for $\beta = 0.20$ and $\beta = 0.02$.

Solution: The loop gain can be written in terms of its magnitude and phase,

$$T(f) = \frac{\beta(100)}{\left[\sqrt{1 + \left(\frac{f}{10^5}\right)^2}\right]^3} e^{-j3\tan^{-1}\left(\frac{f}{10^5}\right)}$$

The frequency f_{180} at which the phase becomes -180 degrees is

$$-3 \tan^{-1}\left(\frac{f_{180}}{10^5}\right) = -180^\circ$$

which yields

$$f_{180} = 1.73 \times 10^5 \text{ Hz}$$

The magnitude of the loop gain at this frequency for, $\beta = 0.20$, is then

$$|T(f_{180})| = \frac{(0.20)(100)}{8} = 2.5$$

For $\beta = 0.02$, the magnitude is

$$|T(f_{180})| = \frac{(0.020)(100)}{8} = 0.25$$

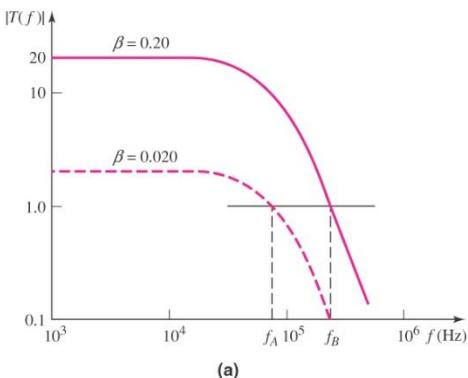
Comment: The loop gain magnitude at the frequency at which the phase is -180 degrees is 2.5 when $\beta = 0.20$ and 0.25 when $\beta = 0.02$. The system is therefore unstable for $\beta = 0.20$ and stable for $\beta = 0.02$.

Stability Criteria example (2)

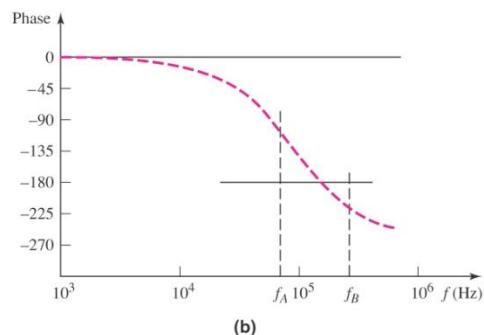
Ex 12.18: The loop gain function of a feedback amplifier is given by

$$T(f) = \frac{\beta(3000)}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{10^5}\right)^2}$$

Determine the value of β at which the amplifier becomes unstable. (Ans. $\beta = 0.0667$)



(a)



(b)

Find the loop-gain when phase is 180° :

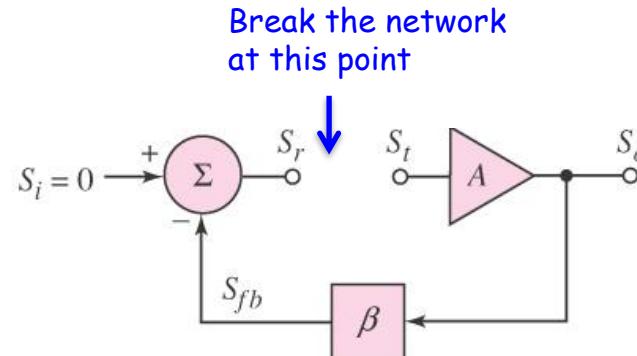
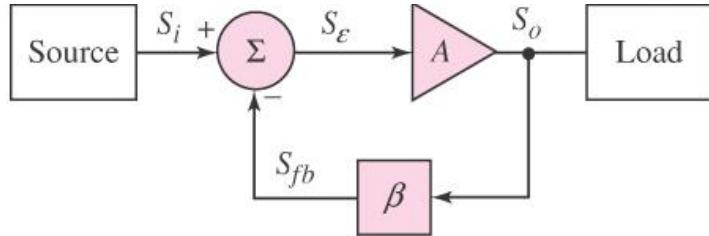
$$\phi = -\tan^{-1} \frac{f}{10^3} - 2 \tan^{-1} \frac{f}{10^5} = -180^\circ$$

If $\tan^{-1} x + \tan^{-1} y + \tan^{-1} z = \pi$, then

$$\begin{aligned}x + y + z &= xyz \\ \frac{f}{10^3} + \frac{2f}{10^5} &= \frac{2f^3}{10^{13}} \\ f &= 100995 \text{ Hz.}\end{aligned}$$

Loop Gain Measurement

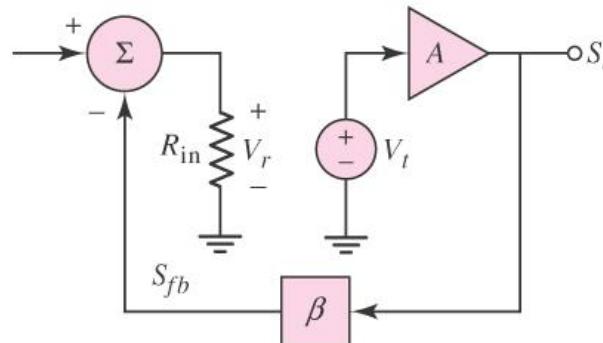
- For discrete transistor amplifiers it is difficult to obtain the loop-gain directly from the closed-loop transfer function



$$\frac{S_r}{S_t} = -A\beta$$

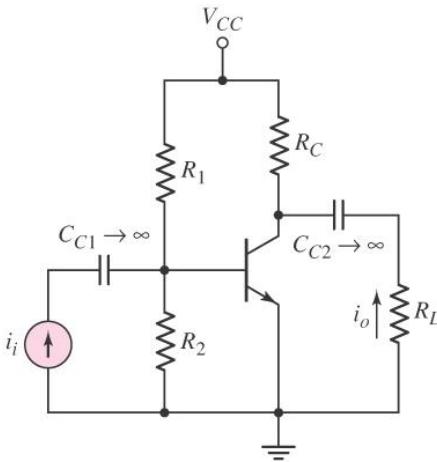
An equivalent impedance must therefore be inserted at the point where the loop is broken. This will maintain:

- same transistor biasing
- same impedance at the return point



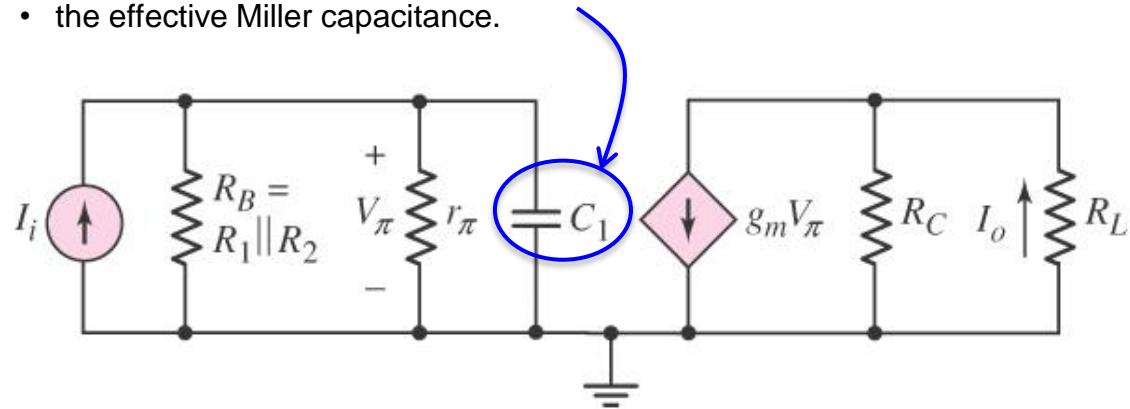
$$T = A\beta = -\frac{V_r}{V_t}$$

Bode Plots: One Stage (I-Pole) Amplifier



includes

- the forward-biased base-emitter junction capacitance
- the effective Miller capacitance.



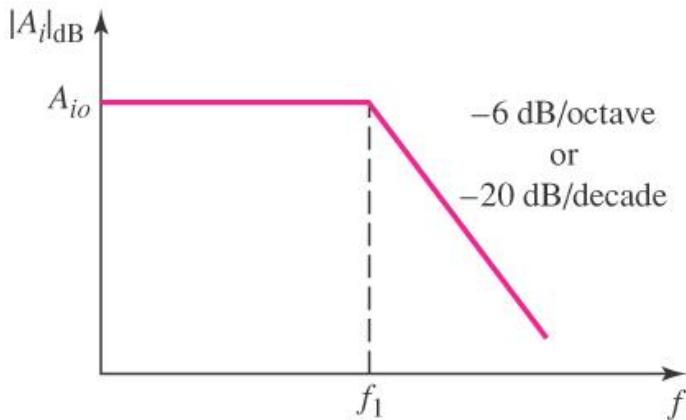
□ Current Gain:

$$A_i = g_m R_\pi \left(\frac{R_c}{R_c + R_L} \right) \left[\frac{1}{1 + sR_\pi C_1} \right] = \frac{A_{io}}{1 + j \left(\frac{f}{f_1} \right)}$$

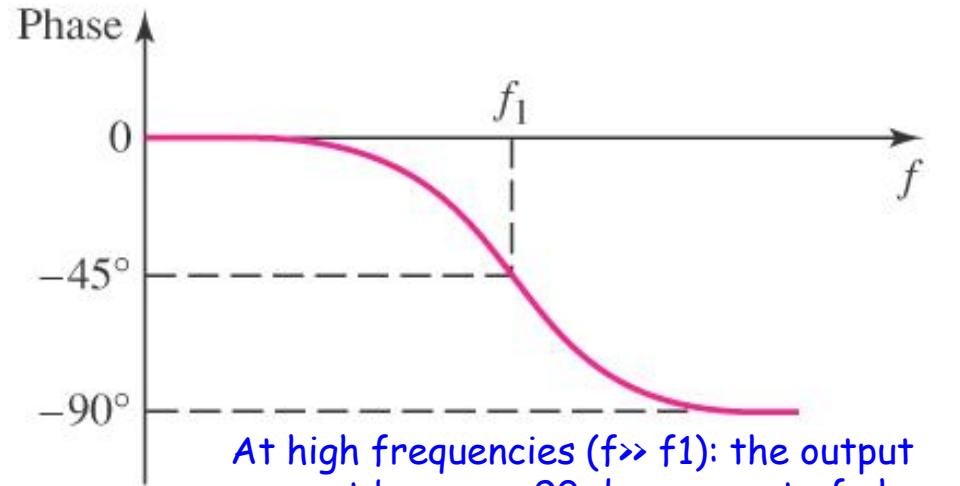
where A_{io} is the low-frequency or mid-band gain and f_1 is the upper 3 dB frequency.

Bode Plots: One Stage (1-Pole) Amplifier

$$A_i = \frac{A_{io}}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \angle -\tan^{-1}\left(\frac{f}{f_1}\right)$$



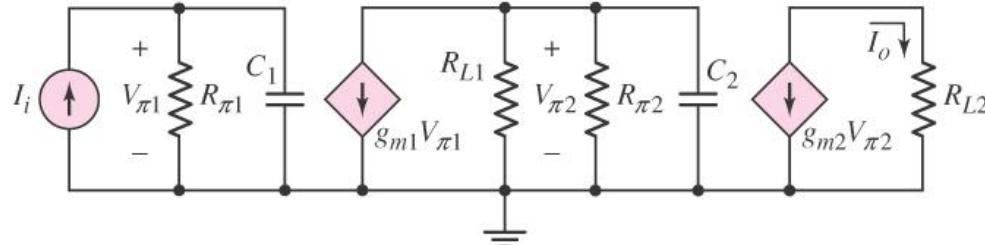
At low frequencies ($f \ll f_1$): the output current is in phase with the input current



At high frequencies ($f \gg f_1$): the output current becomes 90 degrees out of phase with respect to the input current.

1-pole amplifier is unconditionally stable

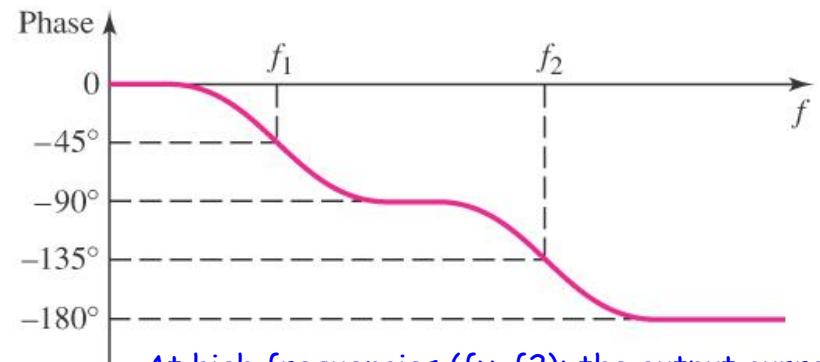
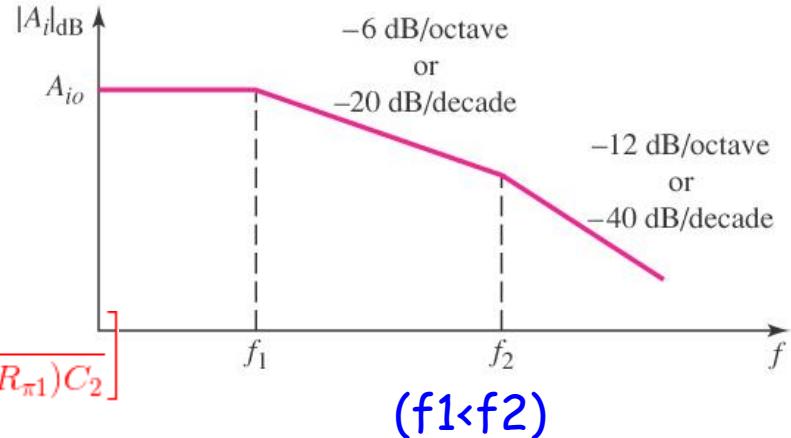
Bode Plots: Two Stage (2-pole) Amplifier



$$A_i = \frac{I_o}{I_i} = (g_{m1}g_{m2})(R_{\pi 1})(R_{L1} \parallel R_{\pi 2}) \left[\frac{1}{1 + sR_{\pi 1}C_1} \right] \left[\frac{1}{1 + s(R_{L1} \parallel R_{\pi 1})C_2} \right]$$

$$A_i = \frac{A_{io}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)}$$

$$A_i = \frac{A_{io}}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2} \sqrt{1 + \left(\frac{f}{f_2}\right)^2}} \angle -\left[\tan^{-1}\left(\frac{f}{f_1}\right) + \tan^{-1}\left(\frac{f}{f_2}\right)\right]$$

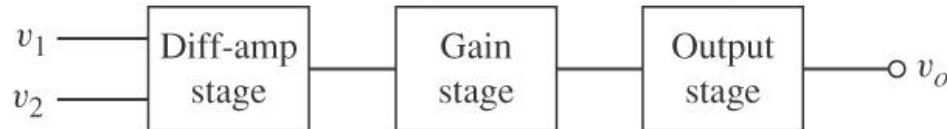


At high frequencies ($f \gg f_2$): the output current becomes 180° out of phase with respect to the input current.

Bode Plots: Three Stage (3-pole) Amplifier

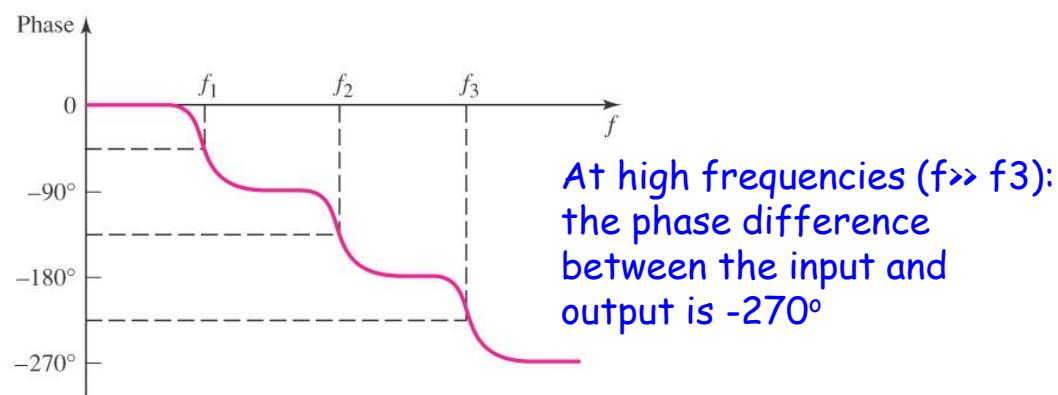
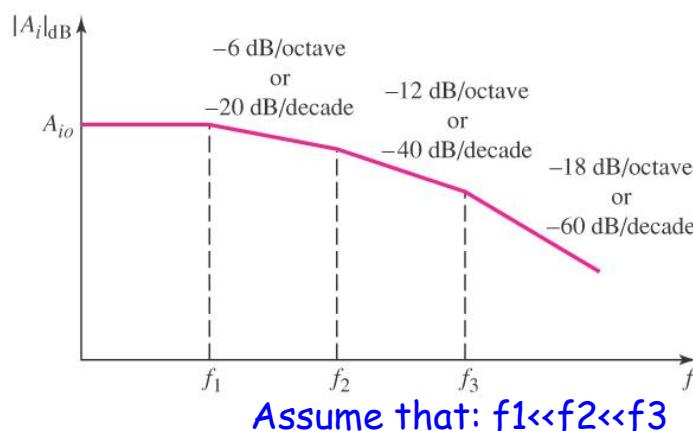
□ An op-amp is a three-stage amplifier

- each stage has an equivalent input resistance and capacitance, this circuit is an example of a three-pole amplifier.



low f gain factor

$$A = \frac{A_o}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$



Bode Plot: Phase and Gain Margins

Loop Gain $T(j\omega) = \beta A(j\omega)$

At the frequency when $|T|=1$, if the phase is less than 180 degrees the system is stable.

Phase Margin (PM or Φ_m) = $180^\circ - \phi(f_1)$

- the absolute value of the difference
- indicates how much the loop gain can increase and still maintain stability

Gain Margin (GM or A_m) = $0 - |T(f_{180})|_{dB}$

- usually expressed in dB
- an indication of how much the loop gain can increase and still maintain stability.

For a stable system:

GM > 0 dB and PM > 0°

For stable systems, $45^\circ < \phi_m < 75^\circ$

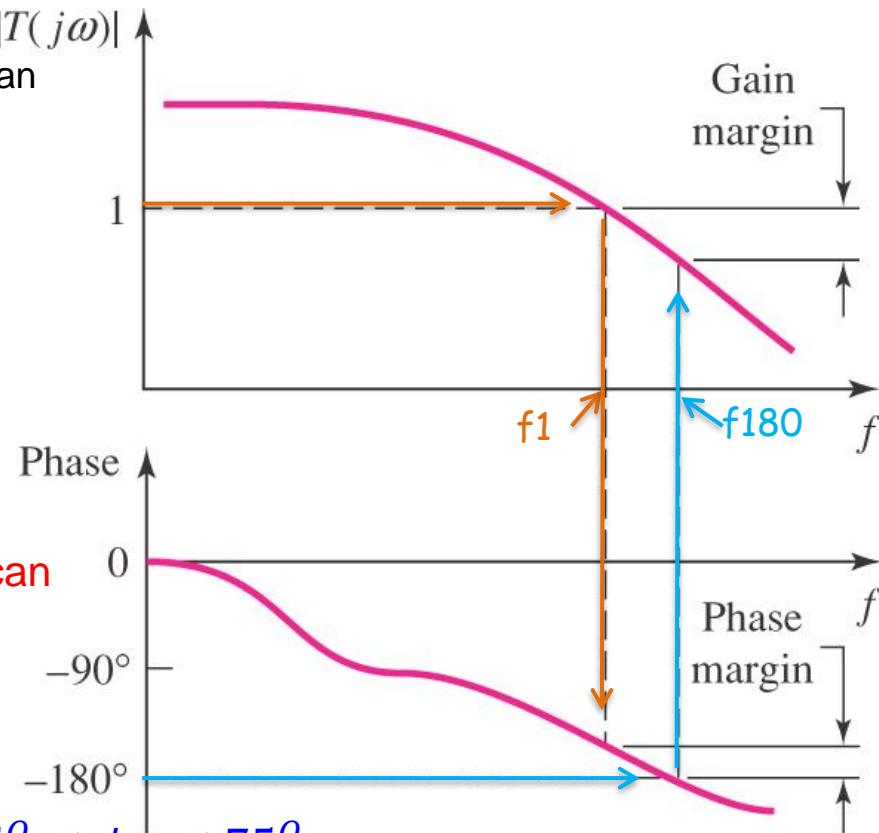
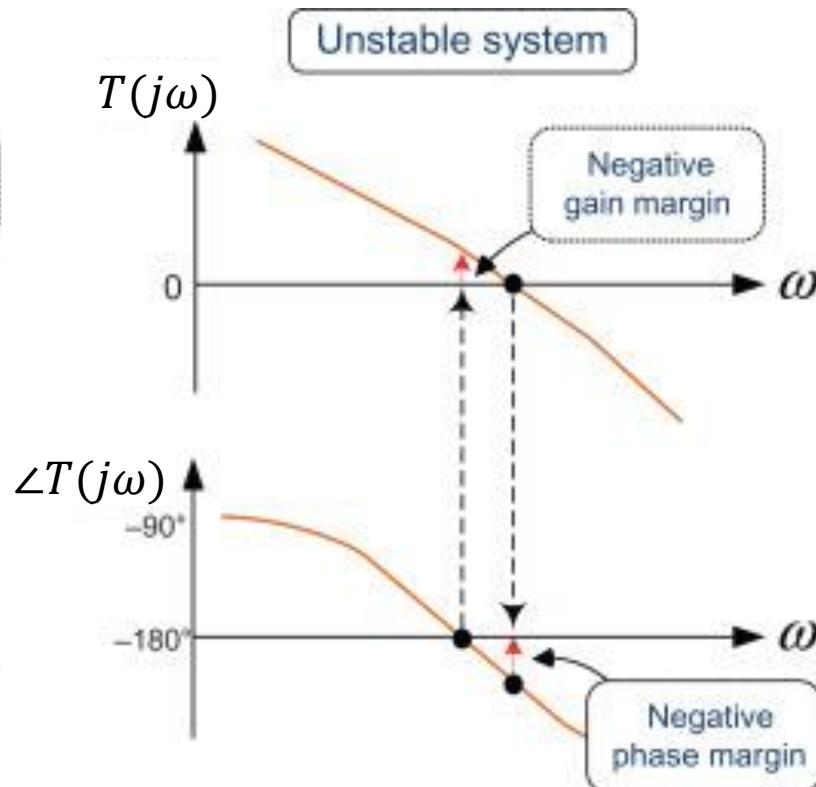
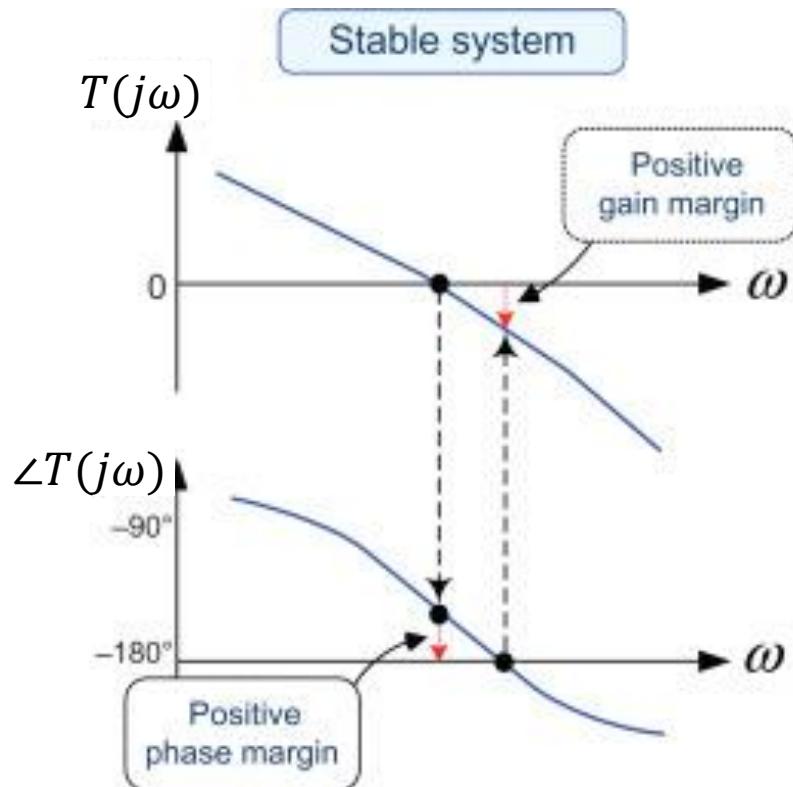
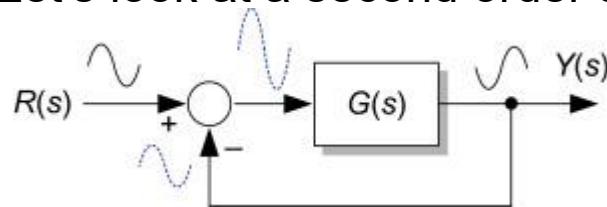


Illustration of Stable and Unstable Systems



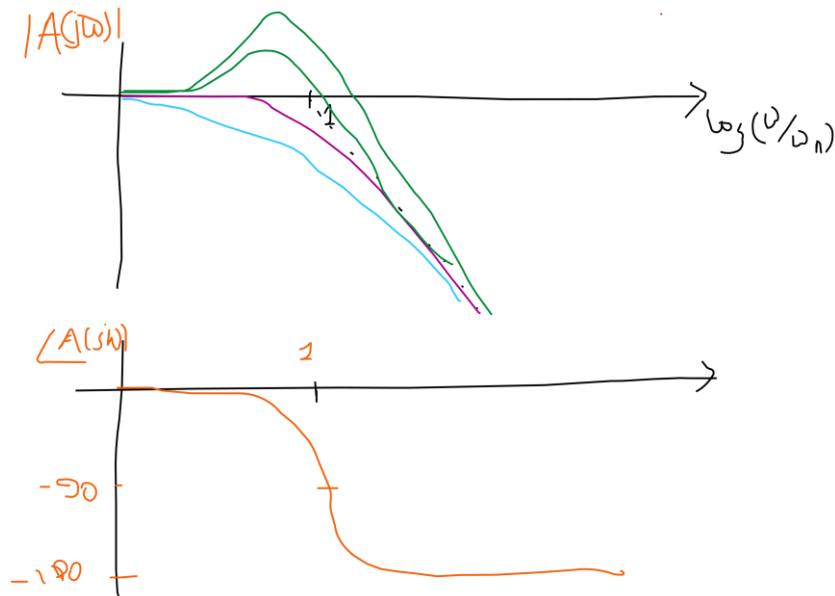
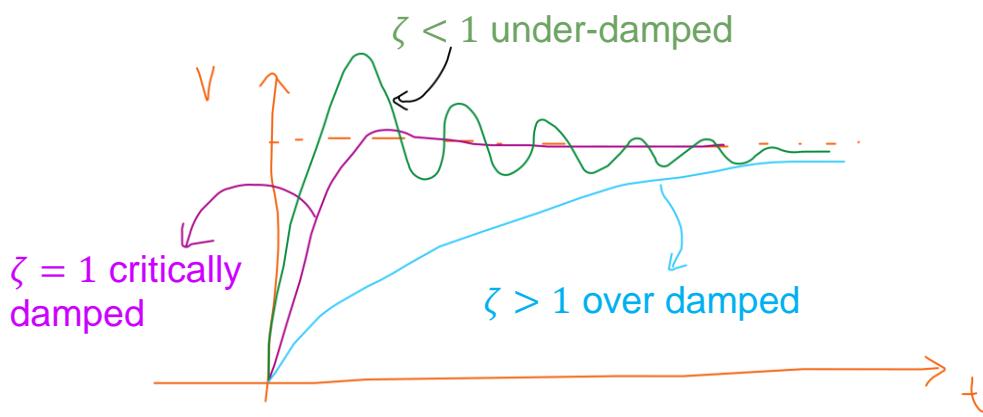
What does PM means in time-domain?

- Let's look at a second order system



$$G(s) = \frac{\omega_n^2}{s(s + 2\zeta\omega_n)}$$

$$A = \frac{Y(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$



What does PM means in time-domain?

- Loop Gain $T(s)$ for the second order system is:

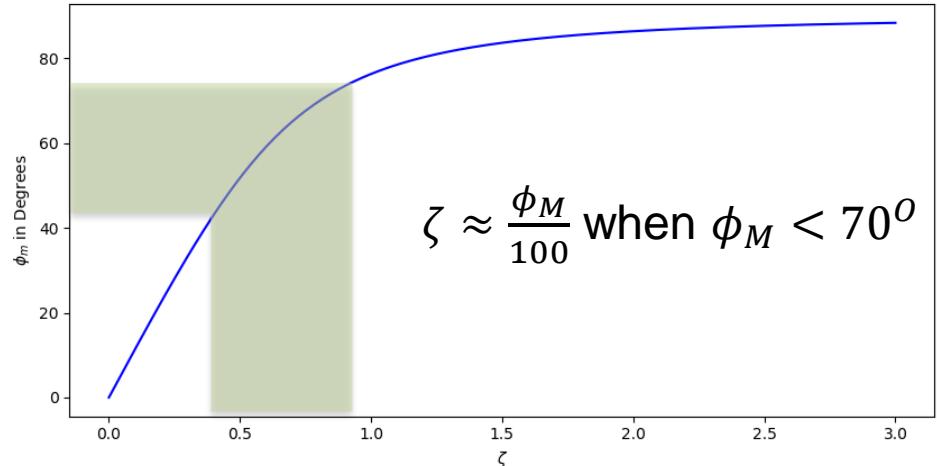
$$T(s) = \beta G(s) = \frac{\omega_n^2}{s(s + 2\zeta\omega_n)}$$

When $|T(s)| = 1 \rightarrow \frac{\omega_n^2}{\omega\sqrt{-\omega^2 + 4\zeta^2\omega_n^4}} = 1$ and $\omega_{g1} = \omega_n\sqrt{\sqrt{1 + 4\zeta^4} - 2\zeta^2}$

$$\angle T(s) = -\angle j\omega - \angle(j\omega + 2\zeta\omega_n^2) = -90^\circ - \tan^{-1} \frac{\omega_{g1}}{2\zeta\omega_n}$$

$$PM = \tan^{-1} \left(\frac{2\zeta}{\sqrt{\sqrt{1 + 4\zeta^4} - 2\zeta^2}} \right)$$

For stable systems, $45^\circ < \phi_M < 75^\circ$



Objective: Determine the required feedback transfer function β to yield a specific phase margin, and determine the resulting closed-loop low-frequency gain.

Consider a three-pole feedback amplifier with a loop gain function given by

$$T(f) = \frac{\beta(1000)}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{5 \times 10^4}\right)\left(1 + j\frac{f}{10^6}\right)}$$

Determine the value of β that yields a phase margin of 45 degrees.

Solution: A phase margin of 45 degrees implies that the phase of the loop gain is -135° at the frequency at which the magnitude of the loop gain is unity. The phase of the loop gain is

$$\phi = -\left[\tan^{-1}\left(\frac{f}{10^3}\right) + \tan^{-1}\left(\frac{f}{5 \times 10^4}\right) + \tan^{-1}\left(\frac{f}{10^6}\right)\right]$$

Since the three poles are far apart, the frequency at which the phase is -135° is approximately equal to the frequency of the second pole, as shown in Figure 12.53. In this example, $f_{135} \cong 5 \times 10^4$ Hz, so we have that

$$\phi = -\left[\tan^{-1}\left(\frac{5 \times 10^4}{10^3}\right) + \tan^{-1}\left(\frac{5 \times 10^4}{5 \times 10^4}\right) + \tan^{-1}\left(\frac{5 \times 10^4}{10^6}\right)\right]$$

or

$$\phi = -[88.9^\circ + 45^\circ + 2.86^\circ] \cong -135^\circ$$

Since we want the loop gain magnitude to be unity at this frequency, we have

$$|T(f)| = 1 = \frac{\beta(1000)}{\sqrt{1 + \left(\frac{5 \times 10^4}{10^3}\right)^2} \sqrt{1 + \left(\frac{5 \times 10^4}{5 \times 10^4}\right)^2} \sqrt{1 + \left(\frac{5 \times 10^4}{10^6}\right)^2}}$$

or

$$1 \cong \frac{\beta(1000)}{(50)(1.41)(1)}$$

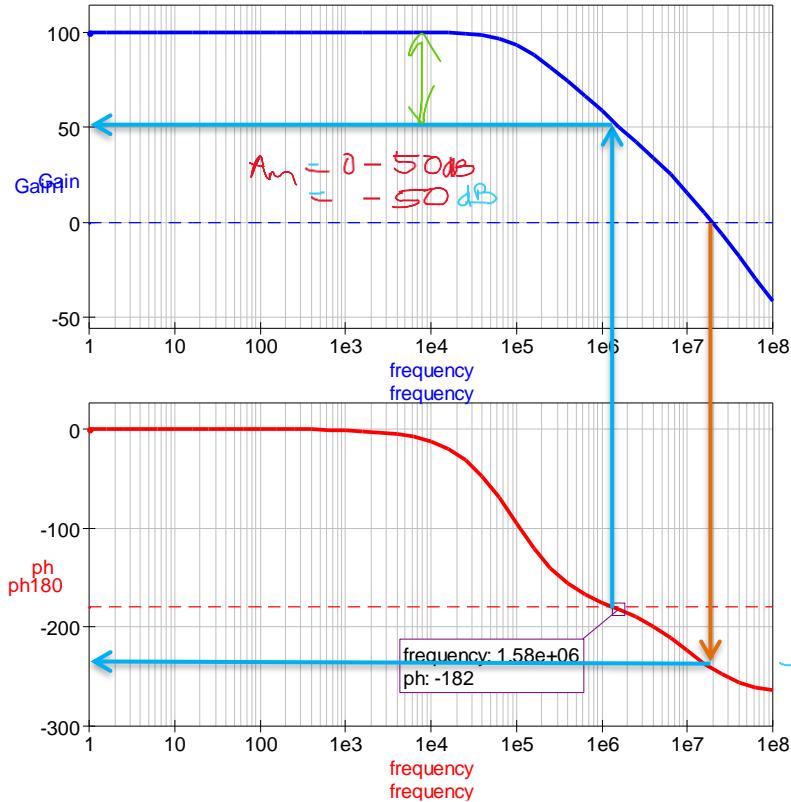
which yields $\beta = 0.0707$.

The closed-loop low-frequency gain for this case is

$$A_{fo} = \frac{A_o}{1 + \beta A_o} = \frac{1000}{1 + (0.0707)(1000)} = 13.9$$

Comment: For this value of β , if the frequency is greater than 5×10^4 Hz, the loop gain magnitude is less than unity. If the frequency is less than 5×10^4 Hz, the phase of the loop gain is $|\phi| < 135^\circ$ (phase margin of 45 degrees). These conditions imply that the system is stable.

Is this Amplifier Stable with $\beta=1$?



- ❑ $\beta=1$ means, $T(s)=A$;
- ❑ Unity gain amplifier configuration, will make this Amplifier unstable

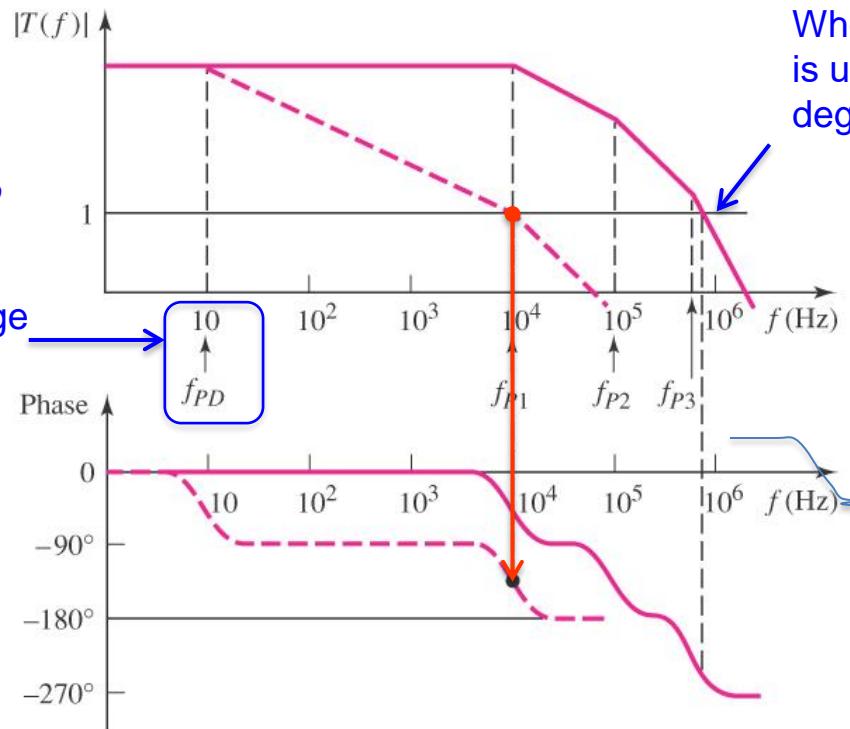
$$20 \log_{10} \left(\frac{1}{\beta} \right) = 50$$
$$\beta = 10^{-3} \rightarrow \text{for stability}$$

$$180 - (240) \\ = -60^\circ$$

Frequency Compensation

involves introducing a new pole in the loop gain function

introduce a new pole f_{PD}
at a very low frequency
assume that the original
three poles do not change



When the magnitude of the loop gain is unity, the phase is nearly -270 degrees and the system is unstable.

magnitude of the loop gain becomes unity well before $\Phi = -180$
→ system is stable.

This new pole (f_{PD}) is at a low freq. and it dominates the freq. response.

→ Dominant pole.

Frequency Compensation (Example)

Objective: Determine the dominant pole required to stabilize a feedback system.

Consider a three-pole feedback amplifier with a loop gain given by

$$T(f) = \frac{1000}{\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{10^6}\right)\left(1 + j\frac{f}{10^8}\right)}$$

Insert a dominant pole, assuming the original poles do not change, such that the phase margin is at least 45 degrees.

Solution: By inserting a dominant pole, we change the loop gain function to

$$T_{PD}(f) = \frac{1000}{\left(1 + j\frac{f}{f_{PD}}\right)\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{10^6}\right)\left(1 + j\frac{f}{10^8}\right)}$$

We assume that $f_{PD} \ll 10^4$ Hz. A phase of -135 degrees, giving a phase margin of 45 degrees, occurs approximately at $f_{135} = 10^4$ Hz.

Since we want the loop gain magnitude to be unity at this frequency, we have

$$|T_{PD}(f_{135})| = 1 = \frac{1000}{\sqrt{1 + \left(\frac{10^4}{f_{PD}}\right)^2} \sqrt{1 + \left(\frac{10^4}{10^4}\right)^2} \sqrt{1 + \left(\frac{10^4}{10^6}\right)^2} \sqrt{1 + \left(\frac{10^4}{10^8}\right)^2}}$$

or

$$1 = \frac{1000}{\sqrt{1 + \left(\frac{10^4}{f_{PD}}\right)^2} (1.414)(1)(1)}$$

Solving for the dominant pole frequency f_{PD} , we find

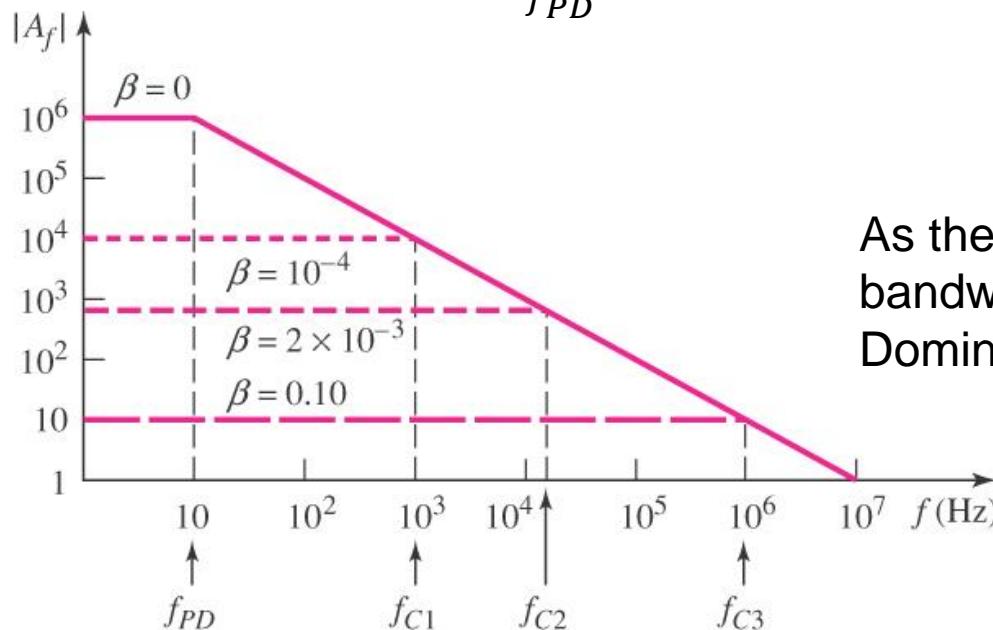
$$f_{PD} = 14.14 \text{ Hz}$$

Comment: With high-gain amplifiers, the dominant pole must be at a very low frequency to ensure stability of the feedback circuit.

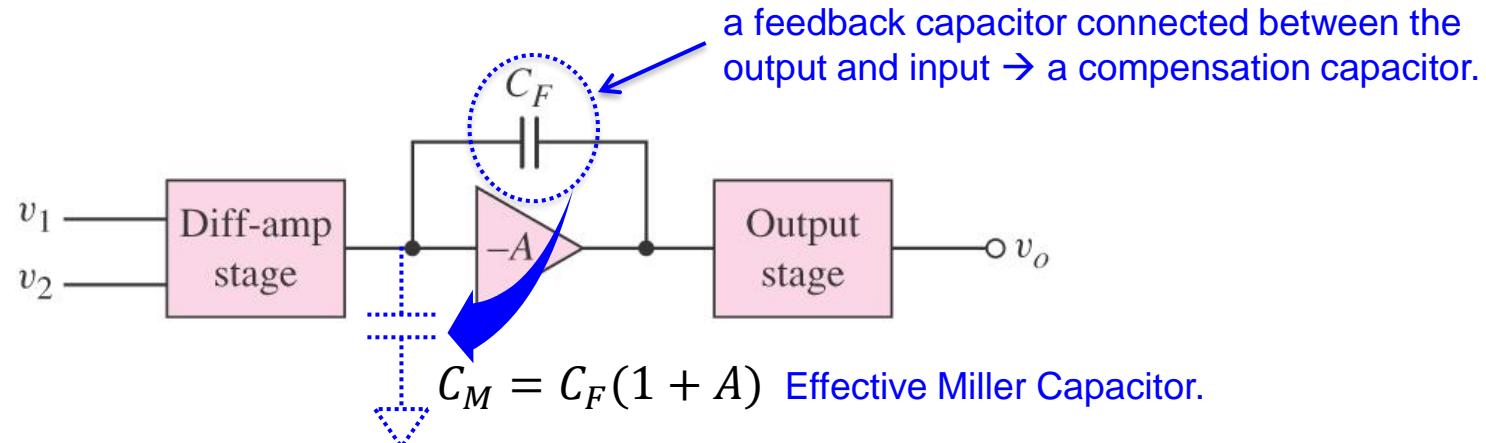
Frequency Compensation - BW

- When A_o is the low-frequency gain and f_{PD} is the dominant-pole frequency.

$$A(f) = \frac{A_o}{1+j\frac{f}{f_{PD}}} \text{ and then } A_f(f) = \frac{A_o}{1+j\frac{f}{f_{PD}}} \times \frac{1}{1+j\frac{f}{f_{PD}(1+\beta A_o)}} \\ \Leftrightarrow f_c \text{ is 3dB freq.}$$

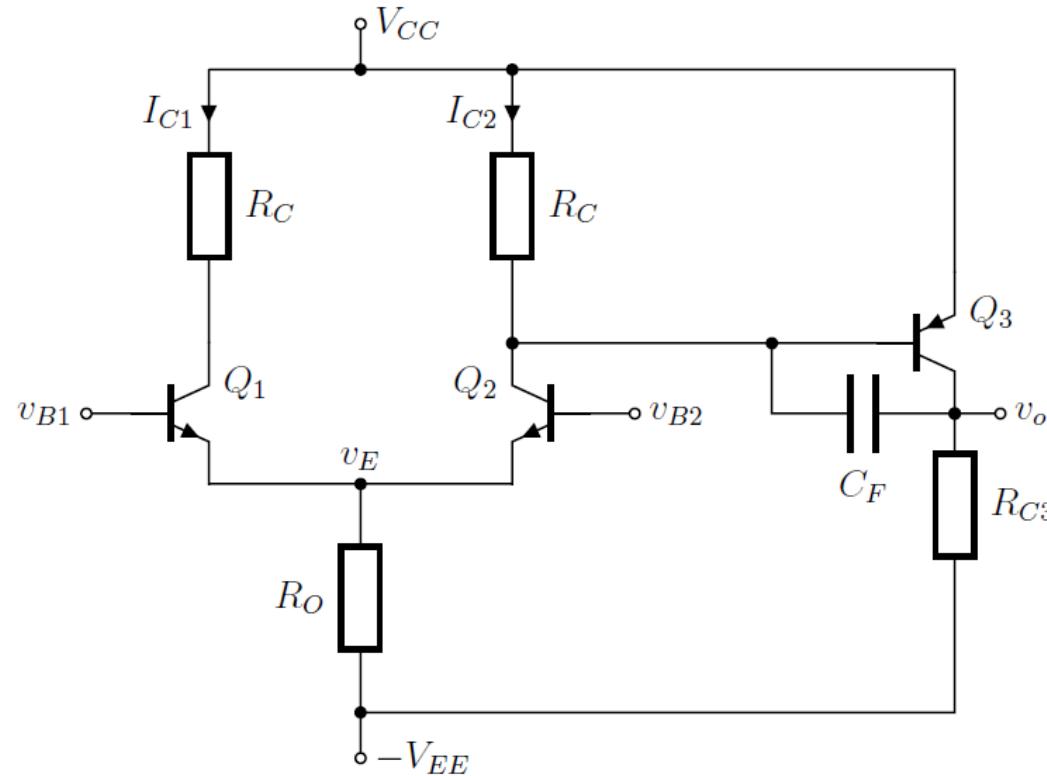


Frequency Compensation in Circuits

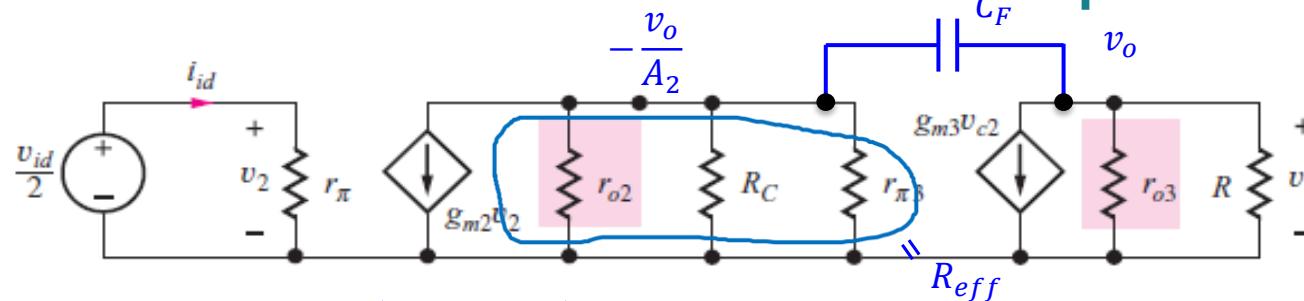


- ❑ The gain of stage 2 (A) is significantly large. Therefore, C_M is large.
- ❑ the pole $f_{p1} = \frac{1}{sR_2C_M}$ introduced by C_M is small → dominant pole.
- ❑ R_2 in this is the effective resistance at the input node of stage 2 amplifier. It is equivalent to the parallel combination of R_{in} of stage 2 and the R_o of stage 1.
- ❑ This method is called Miller Compensation.

Frequency Compensation in Op-Amps



AC Model with the Miller Compensation



Neglected the BJT junction capacitances

$$g_{m2}v_2 - \frac{v_o}{A_2} \times \frac{1}{R_{eff}} + \left(-\frac{v_o}{A_2} - v_o \right) sC_F = 0$$

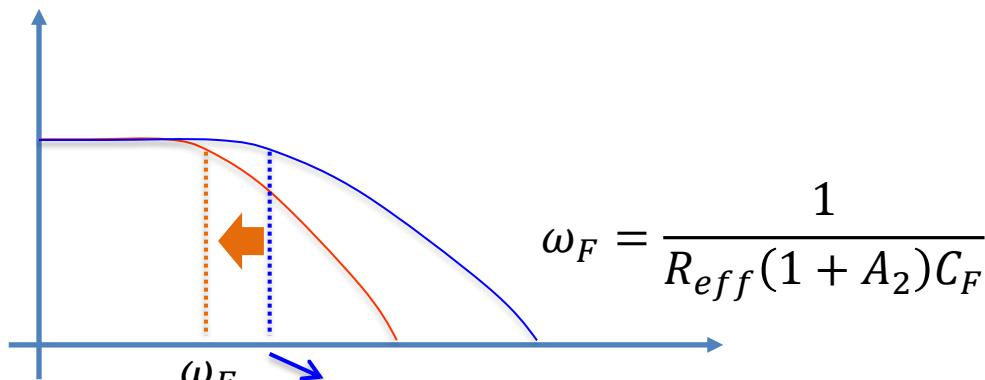
$$v_o = \frac{A_2 R_{eff} g_{m2} \left(\frac{v_{id}}{2} \right)}{1 + sR_{eff}C_F(1 + A_2)}$$

$$A_1 = \frac{A_2 R_{eff} g_{m2}}{2[1 + sR_{eff}C_F(1 + A_2)]}$$

$$A_1 = \frac{A_o}{1 + \frac{1}{\omega_F}}$$

Effective Miller Capacitor.

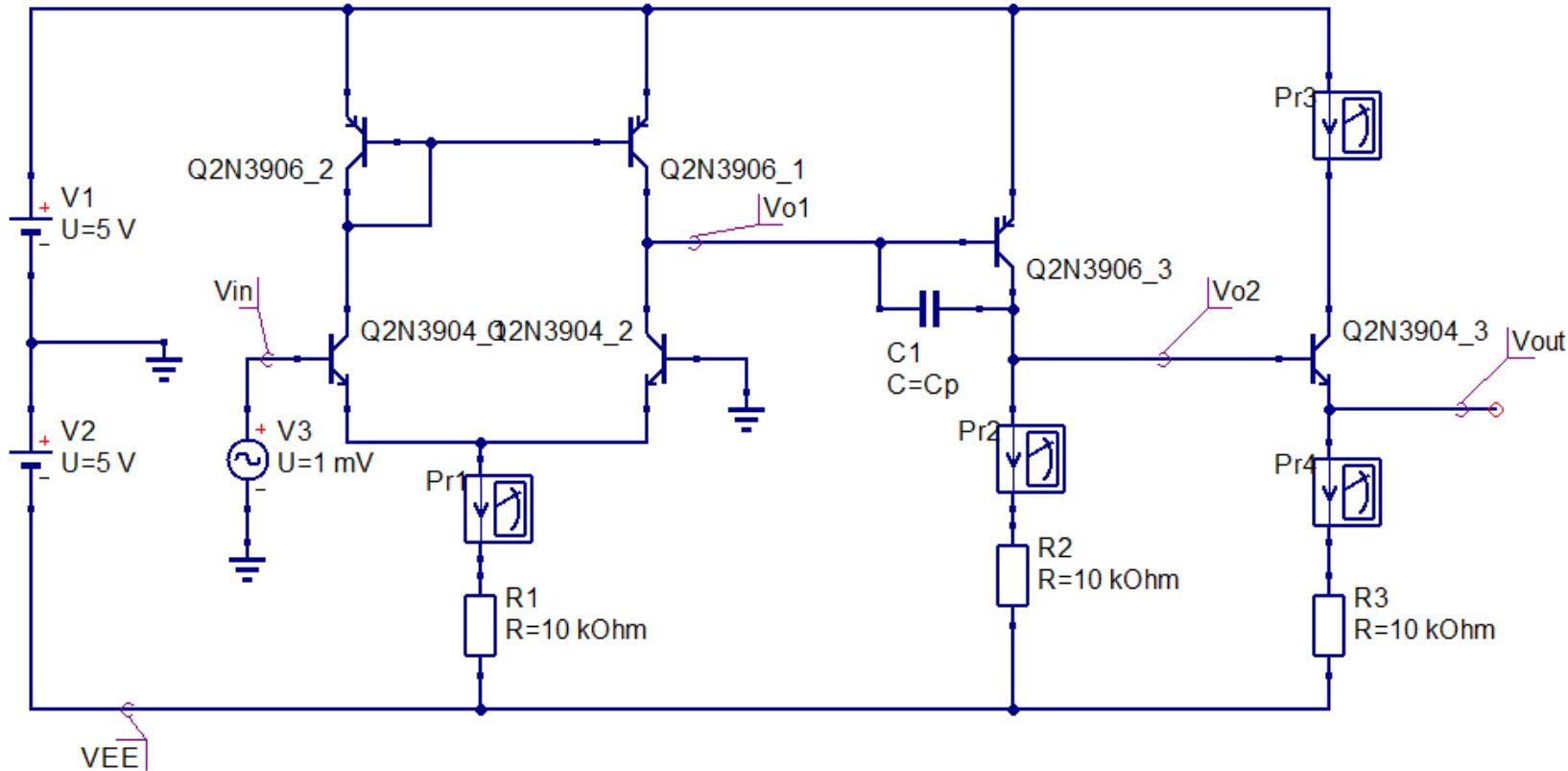
$$C_M = C_F(1 + A_2) + C_\mu$$



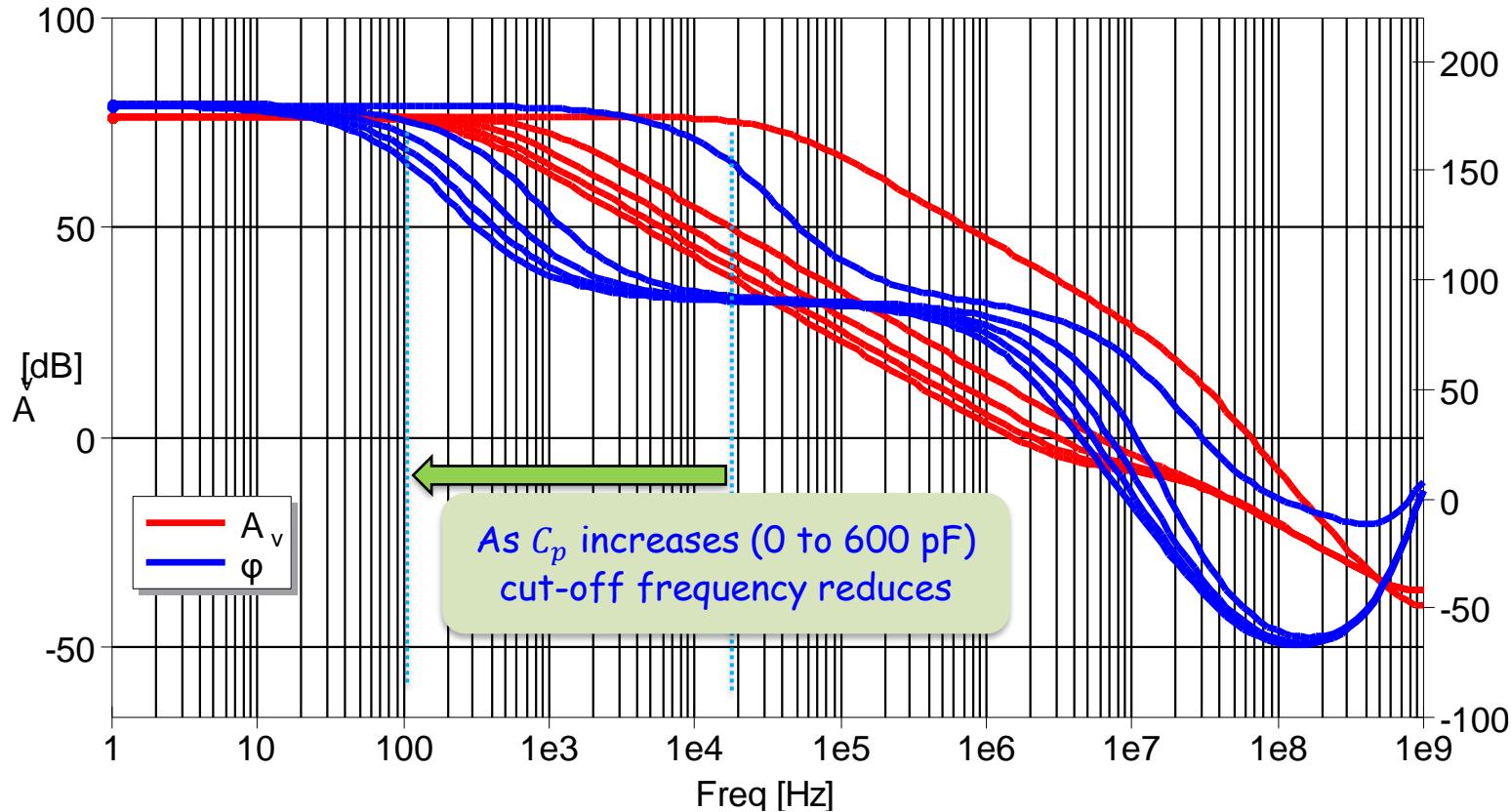
$$\omega_F = \frac{1}{R_{eff}(1 + A_2)C_F}$$

Defined by BJT junction capacitances

Three-Stage OpAmp Simulation



Three-Stage OpAmp Simulation



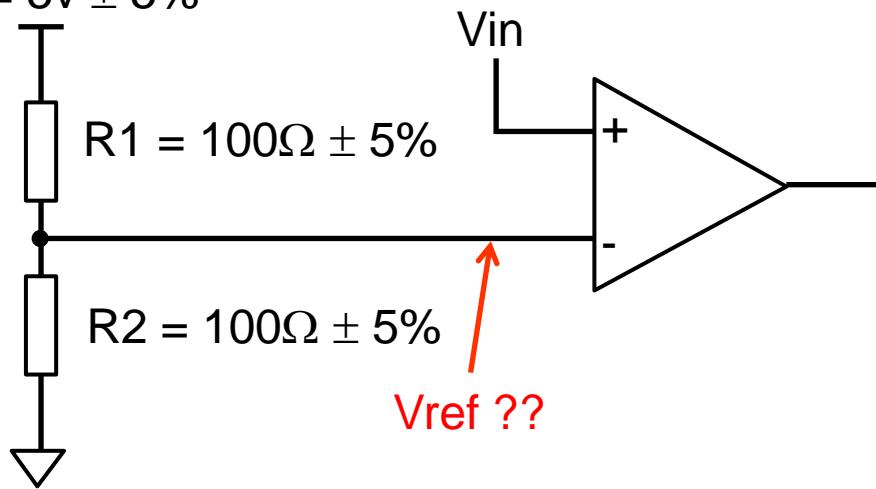
12. Circuit Sensitivity Analysis

Introduction

- ❑ All Circuits Have Performance That Varies As The Values Of The Components Change
 - Temperature
 - Time (Aging)
 - Phase Of The Moon
 - Component Tolerance In Manufacturing
- ❑ How would you determine most sensitive component and its parameter to a circuit metric.

Example Voltage Divider

V_{dc} = 5v ± 5%



❑ Worst-case Analysis:

$$\underline{V}_{ref} = \frac{\underline{R}_2}{\underline{R}_2 + \underline{R}_1} \underline{V}_{dc}$$

V	R1	R2	Vref
5	100	100	2.50
5	100	95	2.44
5	95	100	2.56
5	95	95	2.50
4.75	100	100	2.38
4.75	105	95	2.26
4.75	95	100	2.44
4.75	95	95	2.38
5.25	100	100	2.63
5.25	100	95	2.56
5.25	95	105	2.76
5.25	95	95	2.63

$$\overline{V}_{ref} = \frac{\overline{R}_2}{\overline{R}_2 + \overline{R}_1} \overline{V}_{dc}$$

Sensitivity

- ❑ How much a circuit's behavior changes as a component value changes is the sensitivity
- ❑ It is important to know the sensitivities for:
 - Proper component selection
 - i.e. A 1% Resistor vs. A 5% Resistor
 - Proper choice of topology
 - May Need To Upgrade To A Less Sensitive Topology
 - Proper Guard-band In the Mathematical Description
 - If The Variations Are Too Great, May Have To Modify The Mathematical Description For Greater Margin

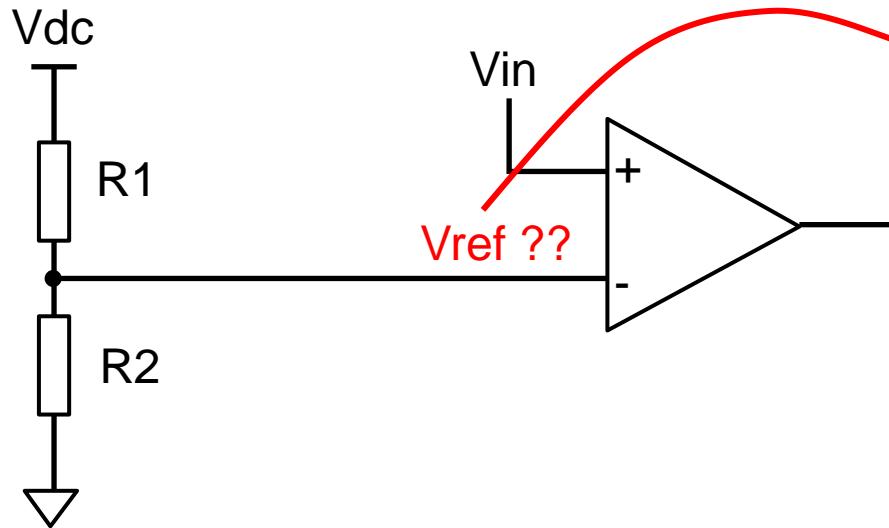
Sensitivity Definition

- Mathematical Definition Of Sensitivity:

$$S_y^x = \lim_{\Delta x \rightarrow 0} \left(\frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} \right) = \frac{x}{y} \frac{\partial y}{\partial x} = \frac{1}{y} x \frac{\partial y}{\partial x}$$

- Where X is the component that is varied and Y is the circuit characteristic that is to be evaluated as x changes.

Example Voltage Divider



$$V_{ref} = V_{dc} \frac{R_2}{R_1 + R_2}$$

$$S_y^x = \frac{1}{y} x \frac{\partial y}{\partial x}$$

$$S_{V_{ref}}^{R_1} = \frac{1}{V_{ref}} R_1 \frac{\partial V_{ref}}{\partial R_1} \quad \text{and} \quad S_{V_{ref}}^{R_2} = \frac{1}{V_{ref}} R_2 \frac{\partial V_{ref}}{\partial R_2}$$

Example Voltage Divider: Solution

$$S_{V_{ref}}^{R_1} = -\frac{R_1}{R_1 + R_2}$$

- Note the (-) sign. When R1 changes it affects negatively to Vref. R1 \uparrow Vref \downarrow

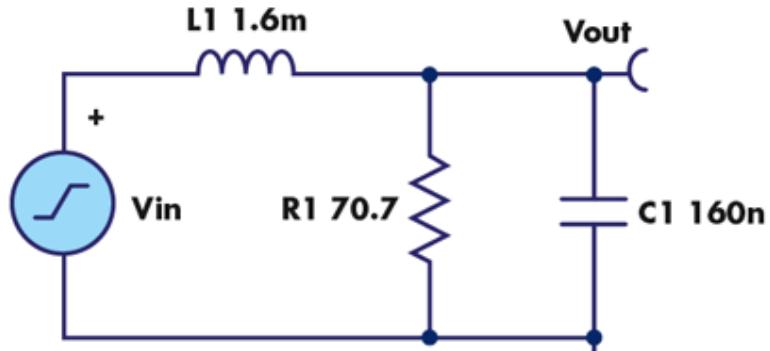
$$S_{V_{ref}}^{R_2} = \frac{R_2}{R_1 + R_2}$$

- R2 \uparrow Vref \uparrow

□ What does this mean for R1 = R2?

- Vref = 0.5 Vdc $S_{V_{ref}}^{R_1} = -0.5$ and $S_{V_{ref}}^{R_1} = 0.5$ Every 1% change in R1, there will be a -0.5% change in Vref.
- When R1 \rightarrow 1.05 R1 (5% increment) Vref changes by -2.5%. Correct?
- Originally Vref = 0.5 Vdc, when R1 \rightarrow 1.05R1, Vref = 0.4878 Vdc. i.e. -2.43% change!

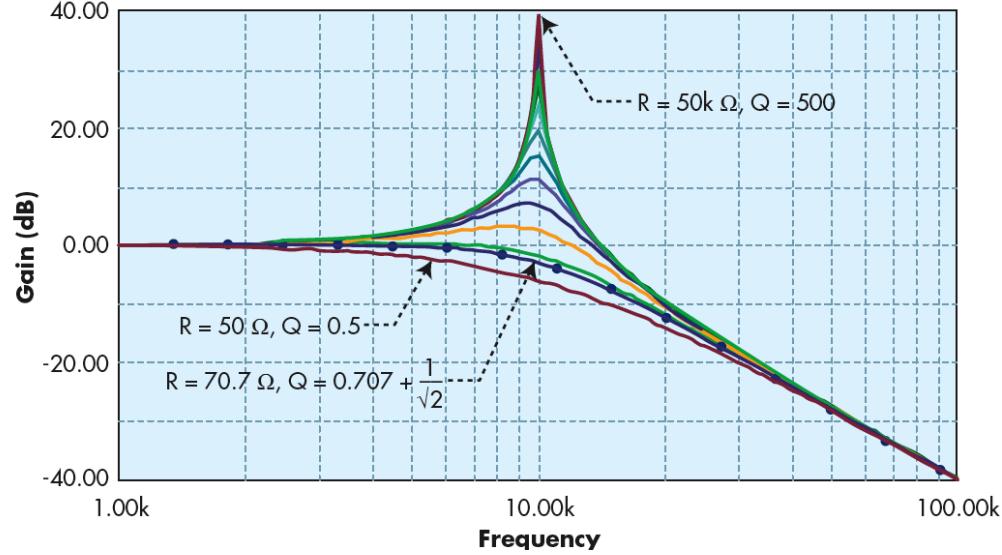
Example (2) RLC Filter



$$\frac{V_{out}}{V_{in}} = \frac{1}{S^2(C_1L_1) + S(C_1/L_1) + 1}$$

$$\omega_n = \frac{1}{\sqrt{L_1 C_1}}$$

$$Q = R_1 \sqrt{\frac{C_1}{L_1}}$$



RLC Filter sensitivity equations

$$\omega_n = \frac{1}{\sqrt{L_1 C_1}} \quad Q = R_1 \sqrt{\frac{C_1}{L_1}}$$

$$S_{C1}^Q = -S_{L1}^Q = \frac{1}{2} \quad S_{R1}^Q = 1 \quad S_{C1}^{\omega_n} = S_{L1}^{\omega_n} = -\frac{1}{2} \quad S_{R1}^{\omega_n} = 0$$

- If C_1 is increased by a factor of four $\rightarrow \omega_n$ decreases by a factor of 2.
- What if C_1 is increased by a factor of 10 \rightarrow

Sensitivity definition is valid only for small variations!

Transfer function sensitivity

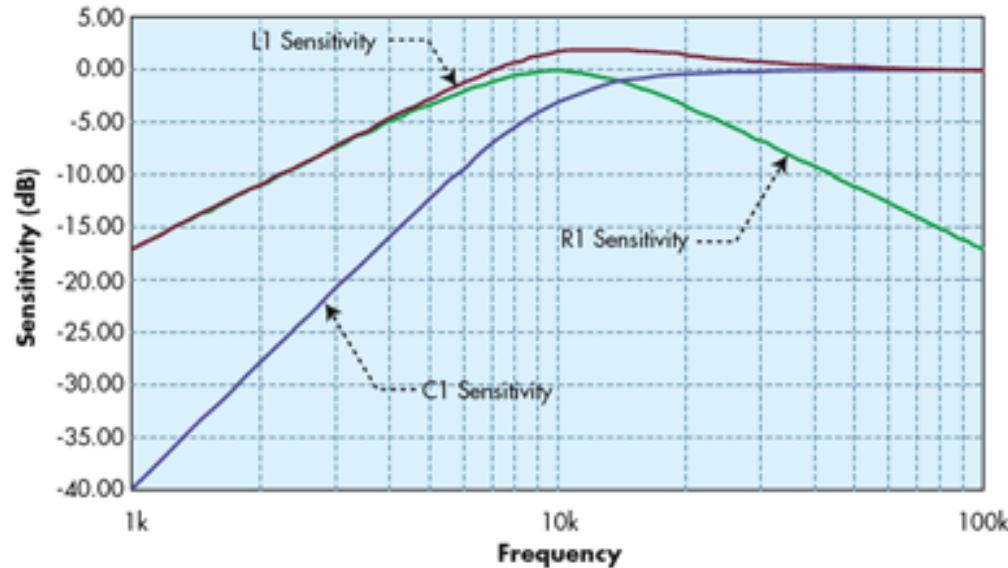
$$S_{C1}^{H(s)} = \frac{C1}{H(s)} \frac{\partial H(s)}{\partial C1}$$

$$S_{C1}^{H(s)} = -\frac{s^2 L1 C1}{S^2 L1 C1 + S L1 / R1 + 1}$$

$$S_{R1}^{H(s)} = \frac{s L1 / R1}{S^2 L1 C1 + S L1 / R1 + 1}$$

$$S_{L1}^{H(s)} = -\frac{s^2 L1 C1 + s L1 / R1}{S^2 L1 C1 + S L1 / R1 + 1}$$

They Are Functions Of The Components AND of Frequency



Sensitivity: Take home message

- ❑ We can determine how important each component is to each circuit parameter with the sensitivity equations
 - This allows us to intelligently specify the precision of the components we selected

is this all we can use sensitivity analysis for?

- ❑ We can also use the sensitivity equations to select component values to reduce sensitivity
 - Sensitivity equations that are functions of component values often reveal trade-offs that we can make

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