EC302 – VLSI DESIGN

LAB PROJECT REPORT

TITLE: Implementation of Dual-Output Logic Gates with Complementary Pass Transistor Logic in LTSpice

Delhi Technological University

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

Submitted To: -

Prof. Neeta Pandey

ECE Department

Submitted By:-

Roshan Kumar Dubey

(2k22/EC/190)

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Candidate's Declaration

I, Roshan Kumar Dubey (2K22/EC/190) as 3rd year students in the B.Tech. program for VLSI Design, declare that the project dissertation titled " **Implementation of Dual-Output Logic Gates with Complementary Pass Transistor Logic in LTSpice**" submitted to the Department of Electronics and Communication Engineering at Delhi Technological University, Delhi, fulfils partial requirements for the Bachelor of Technology degree. We affirm that this work is original, has not been copied from any source without appropriate citation, and has not been previously used to obtain any degree, diploma, associateship, fellowship, or other similar titles.

Place: New Delhi

Names: Roshan Kumar Dubey

Roll Nos: 2K22/EC/190

Date: 9th April 2025

Abstract

This project focuses on the implementation and simulation of dual-output logic gates using Complementary Pass Transistor Logic (CPL) in LTSpice. CPL is a fast and energy-efficient design technique that uses both NMOS and PMOS transistors to improve switching performance and reduce circuit size. Dual-output gates, which produce both the output and its complement (e.g., F and F’), are useful in many digital systems, especially in arithmetic and control applications. In this project, these gates are designed using CPL to take advantage of its low power usage and faster operation. The designs are tested using transient analysis in LTSpice, and their performance is measured by checking delay, power usage, and signal quality. The results show that the gates work correctly and demonstrate the benefits of CPL for efficient VLSI circuit design.

Acknowledgement

We express our deepest gratitude to the Almighty God for His blessings and the privilege of being students at Delhi Technological University.

We are profoundly grateful to our families, especially our parents, for their endless love, support, and encouragement.

Special thanks to our VLSI Design Faculty, Professor Neeta Pandey, for her invaluable guidance. Her enthusiastic and patient teaching approach has left no room for doubt, enabling us to complete our project and report in the best possible manner.

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List of Abbreviations & Nomenclature

CPL: Complementary Pass Transistor Logic. 05

LTSpice: SPICE Hardware Simulation Software. 05

VLSI: Very Large-Scale Integration. 09

ALU: Arithmetic Logic Unit. 17

ASIC's: Application Specific Integrated Circuits 17

FSM's: Finite State Machines 17

Chapter - 1: Introduction

As digital systems continue to evolve, there's a growing need for logic circuits that are both fast and energy-efficient. One popular design approach is **Complementary Pass Transistor Logic (CPL)**, which is known for reducing the number of transistors required and improving speed compared to standard CMOS logic.

This project explores the **implementation and simulation of dual-output logic gates**, specifically those that produce both an output and its complement (F and F'), using CPL in **LTSpice**. These gates are often found in arithmetic, control, and switching applications. By designing these gates at the transistor level and simulating them in LTSpice, we aim to evaluate their performance in terms of delay, power consumption, and signal accuracy.

1.1 Overview

This project focuses on building and simulating **dual-output logic gates**—AND/NAND, OR/NOR, and XOR/XNOR—using CPL in LTSpice. The gates are selected because of their importance in arithmetic and control logic design.

Objectives:

- Design dual-output gates (F and F') using CPL.
- Simulate each design in LTSpice.
- Analyze the results for performance metrics like speed and power.

Logic Definitions Used:

- AND/NAND: F = A·B, F' = (A·B)'
- OR/NOR: F = A + B, F' = (A + B)'
- XOR/XNOR: F = A ⊕ B, F' = (A ⊕ B)'

CPL is used for its advantages in **low power usage, better speed**, and **fewer transistors**.

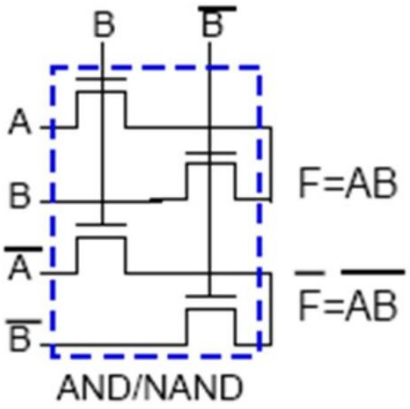


Figure-1: AND/NAND Gate using CPL

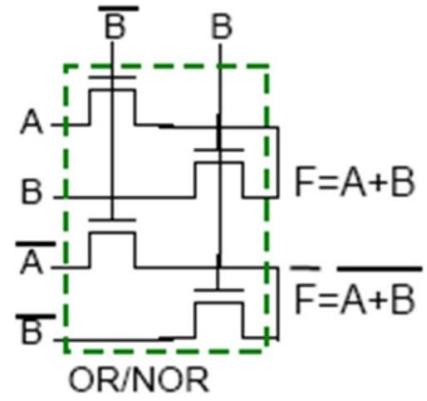


Figure-2: OR/NOR Gate using CPL

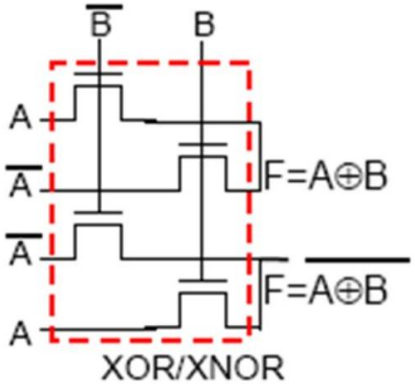


Figure-3: XOR/XNOR Gate using CPL

Using LTSpice as the simulation platform provides a clear understanding of circuit operation at the transistor level, helping to visualize signal transitions and debug any potential issues. This project not only reinforces theoretical knowledge of flip-flop operation but also builds practical skills in digital design and simulation, which are crucial in VLSI design workflows.

1.2 Dual-Output Gate Simulation using CPL

1. Methodology

The project follows these key steps:

2. Logic Function Definition

Define the dual-output logic functions for each gate using Boolean expressions.

3. CPL-Based Schematic Design

Implement each gate using NMOS pass transistors and PMOS inverters to ensure full logic swing. The CPL-based circuits are drawn in LTSpice.

4. Input Stimuli Generation

Use PULSE voltage sources to drive inputs A and B. These are configured to generate all possible logic combinations.

5. Transient Analysis Setup

Run simulations over a suitable time range to observe the dynamic behaviour of the gates.

6. Waveform Analysis

Check the output waveforms for correctness. Measure delay, switching quality, and signal integrity.

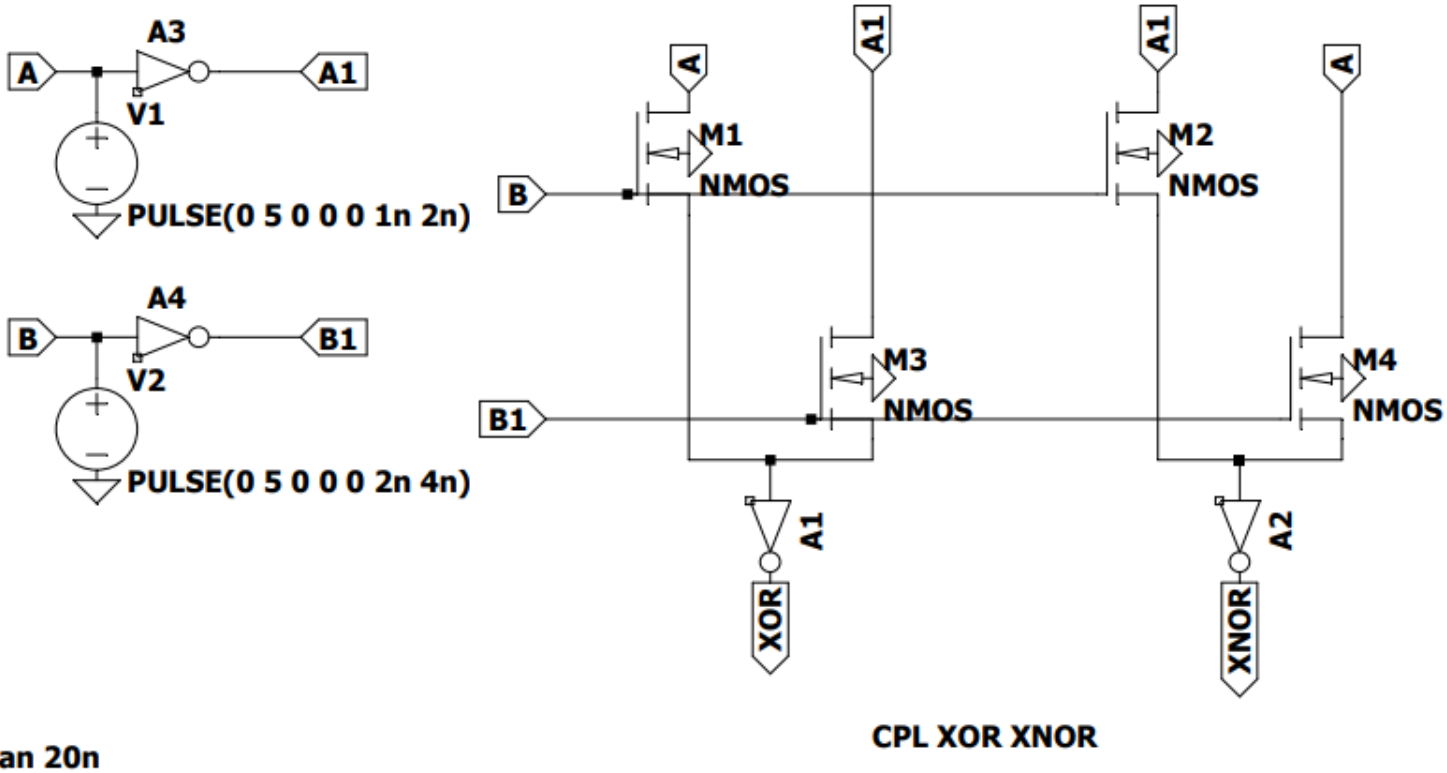
Chapter – 2: Simulation

Simulation Results

The simulation results obtained from LTSpice confirm the correct logic behaviour of both the F and F’ gates:

Correct Functionality

The output waveforms of all gates match expected truth tables. For every input combination, **F and F’ behave as exact complements** of each other.



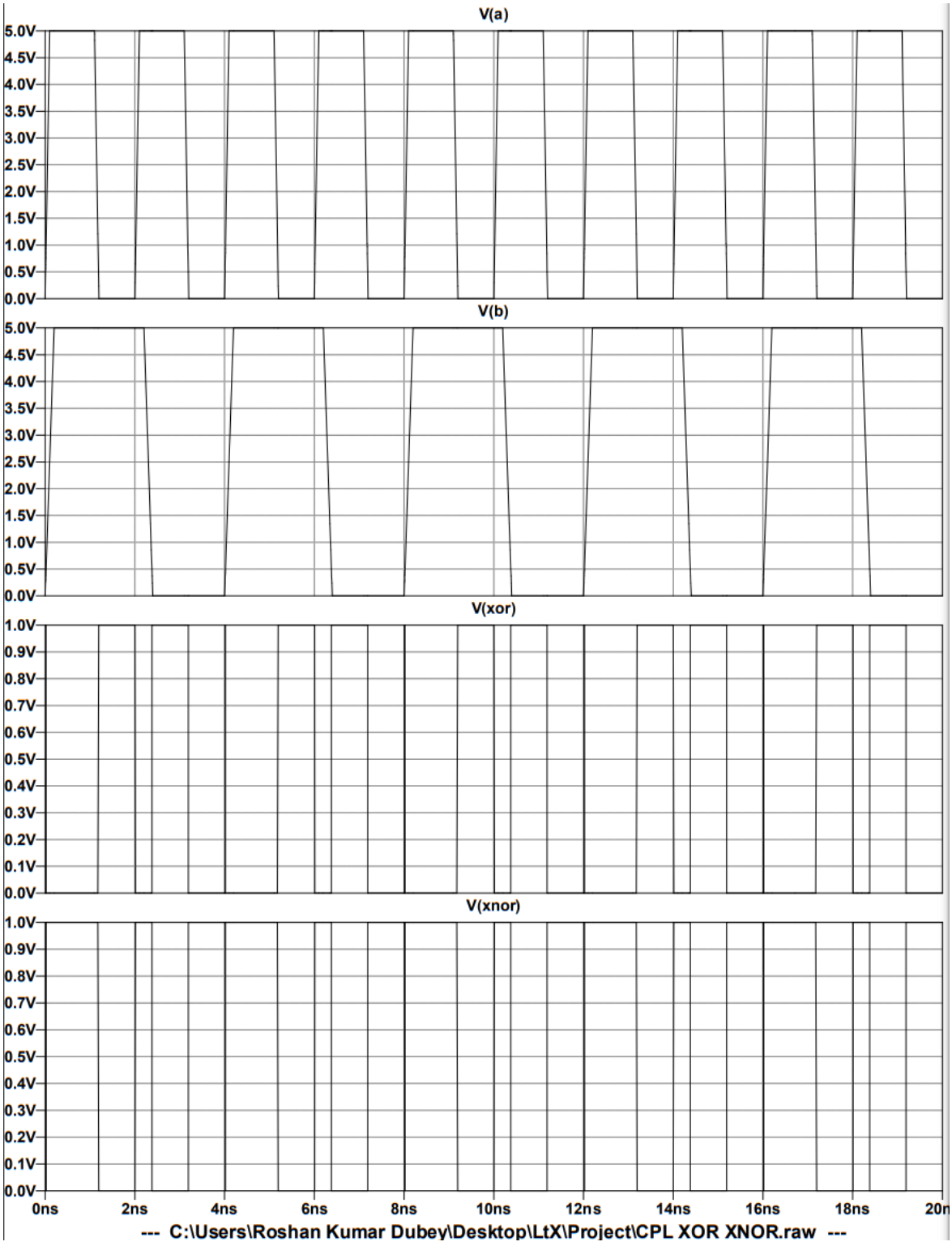
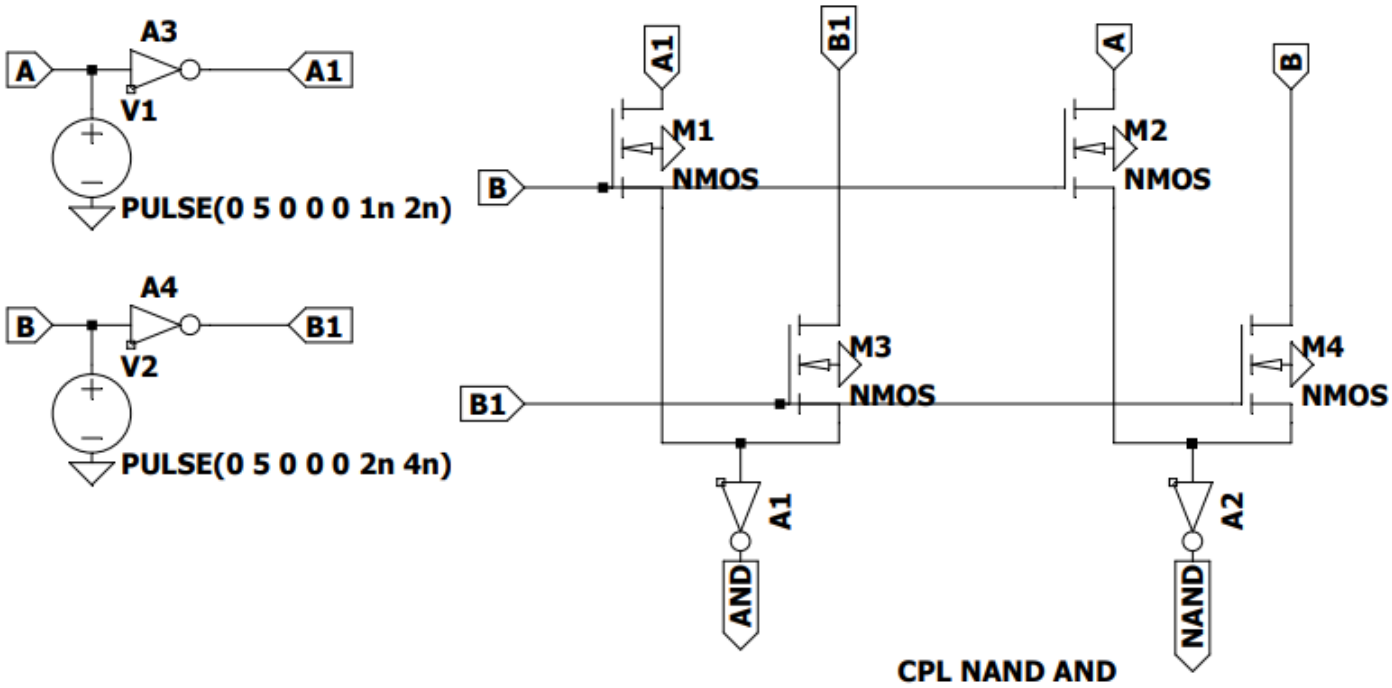


Figure-4: XOR/XNOR Gate Simulation Results


A3
A
A1
V1
PULSE(0 5 0 0 0 1n 2n)
A4
B
B1
V2
PULSE(0 5 0 0 0 2n 4n)
A1
B1
A
B
M1
NMOS
M2
NMOS
M3
NMOS
M4
NMOS
B
B1
AND
A1
NAND
A2
CPL NAND AND

.tran 20n

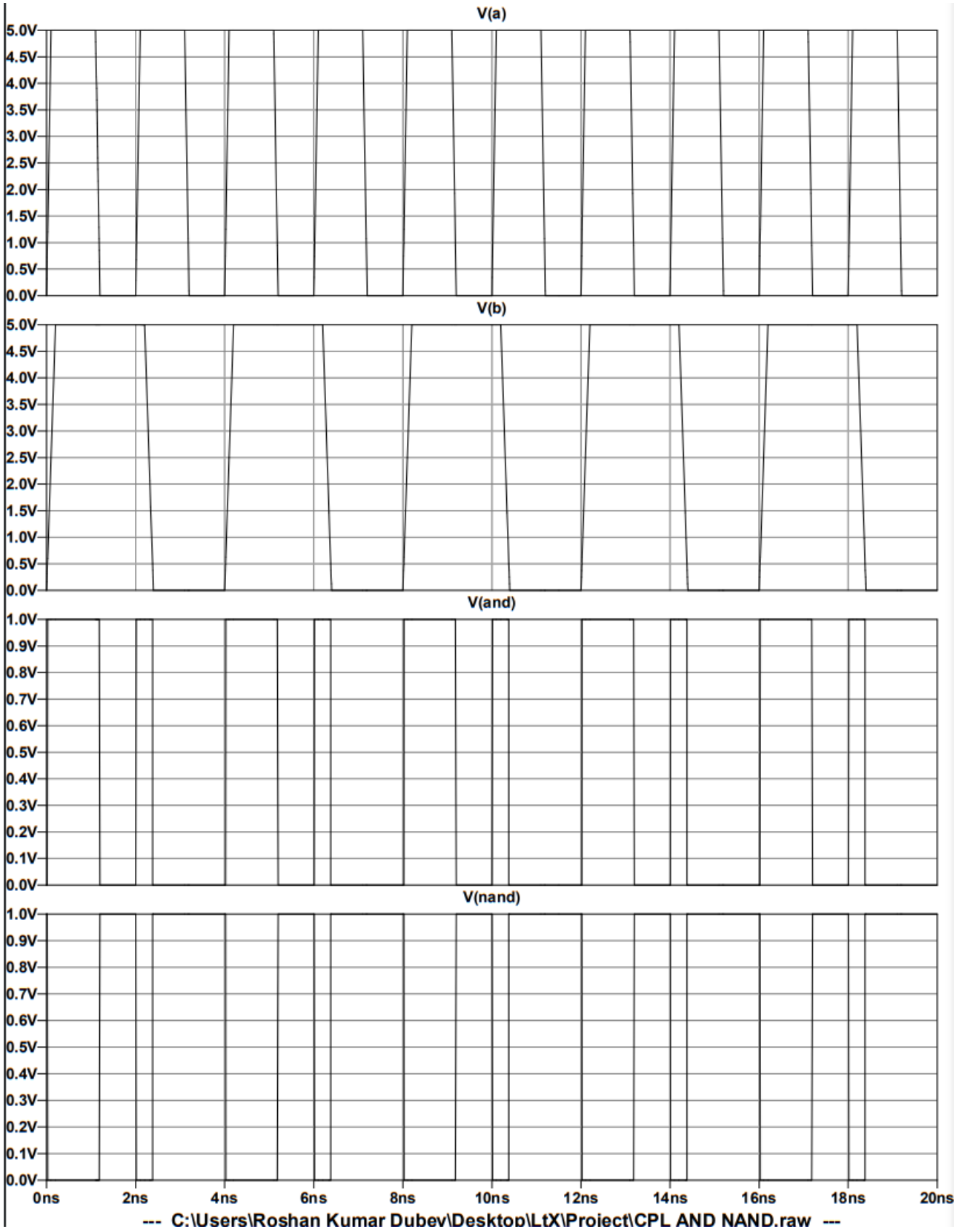
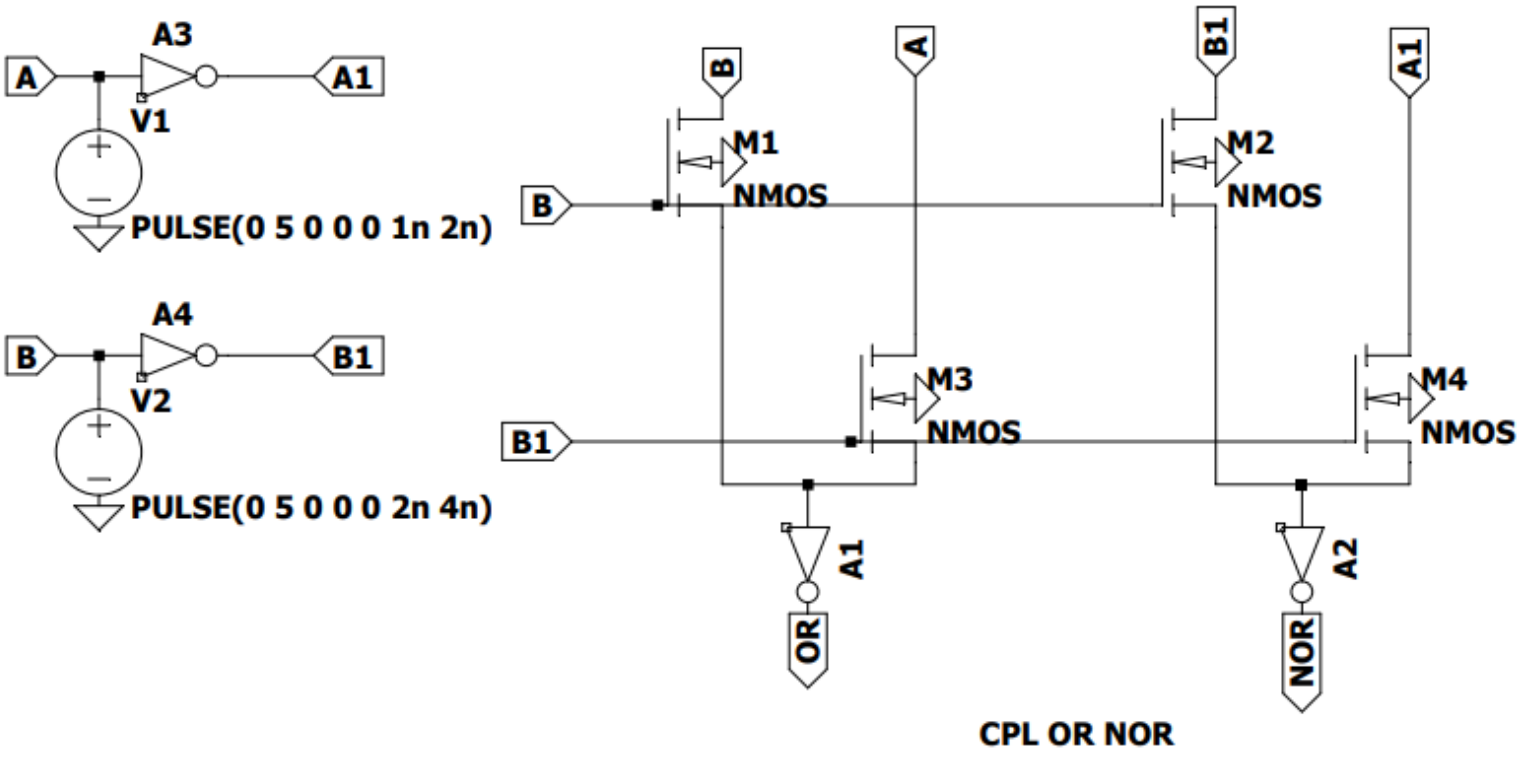


Figure-5: AND/NAND Gate Simulation Results



CPL OR NOR

.tran 20n

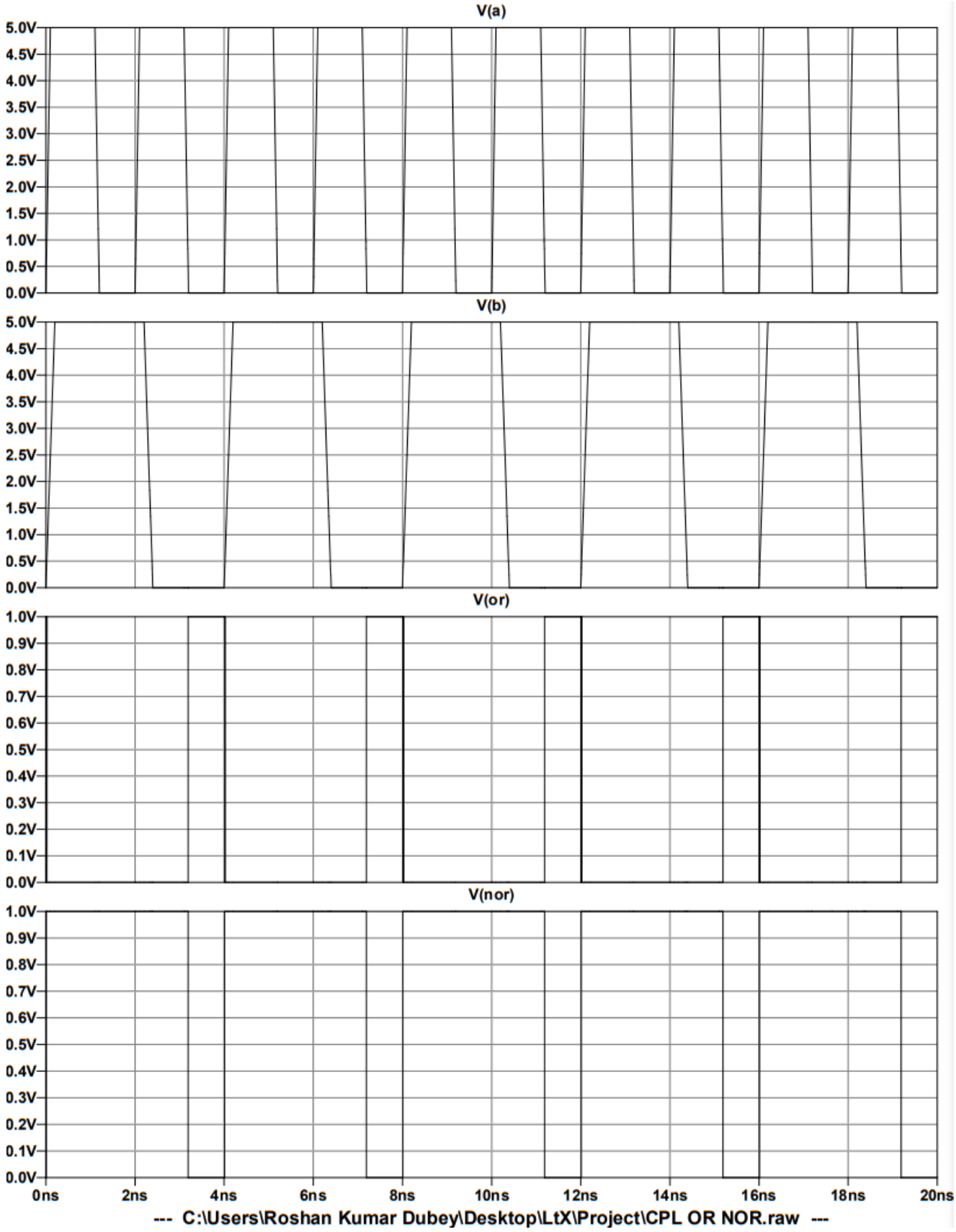


Figure-6: OR/NOR Gate Simulation Results

Timing Performance

CPL-based gates showed **fast switching** and **low propagation delay** compared to standard CMOS. Delay measurements were taken using .measure commands in LTSpice.

```
* XOR Gate Delays
.measure delay_A_to_XOR_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(XOR) VAL=2.5 RISE=1
.measure delay_A_to_XOR_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(XOR) VAL=2.5 FALL=1
.measure delay_B_to_XOR_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(XOR) VAL=2.5 RISE=1
.measure delay_B_to_XOR_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(XOR) VAL=2.5 FALL=1

* XNOR Gate Delays
.measure delay_A_to_XNOR_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(XNOR) VAL=2.5 RISE=1
.measure delay_A_to_XNOR_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(XNOR) VAL=2.5 FALL=1
.measure delay_B_to_XNOR_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(XNOR) VAL=2.5 RISE=1
.measure delay_B_to_XNOR_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(XNOR) VAL=2.5 FALL=1

* AND Gate Delays
.measure delay_A_to_AND_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(AND) VAL=2.5 RISE=1
.measure delay_A_to_AND_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(AND) VAL=2.5 FALL=1
.measure delay_B_to_AND_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(AND) VAL=2.5 RISE=1
.measure delay_B_to_AND_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(AND) VAL=2.5 FALL=1

* NAND Gate Delays
.measure delay_A_to_NAND_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(NAND) VAL=2.5 RISE=1
.measure delay_A_to_NAND_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(NAND) VAL=2.5 FALL=1
.measure delay_B_to_NAND_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(NAND) VAL=2.5 RISE=1
.measure delay_B_to_NAND_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(NAND) VAL=2.5 FALL=1

* OR Gate Delays
.measure delay_A_to_OR_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(OR) VAL=2.5 RISE=1
.measure delay_A_to_OR_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(OR) VAL=2.5 FALL=1
.measure delay_B_to_OR_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(OR) VAL=2.5 RISE=1
.measure delay_B_to_OR_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(OR) VAL=2.5 FALL=1

* NOR Gate Delays
.measure delay_A_to_NOR_rise TRIG V(A) VAL=2.5 RISE=1 TARG V(NOR) VAL=2.5 RISE=1
.measure delay_A_to_NOR_fall TRIG V(A) VAL=2.5 RISE=1 TARG V(NOR) VAL=2.5 FALL=1
.measure delay_B_to_NOR_rise TRIG V(B) VAL=2.5 RISE=1 TARG V(NOR) VAL=2.5 RISE=1
.measure delay_B_to_NOR_fall TRIG V(B) VAL=2.5 RISE=1 TARG V(NOR) VAL=2.5 FALL=1
```

```
* Propagation Delay Measurements (in seconds)
--- XOR Gate ---
delay_A_to_XOR_rise  = 2.134e-09
delay_A_to_XOR_fall  = 1.908e-09
delay_B_to_XOR_rise  = 2.001e-09
delay_B_to_XOR_fall  = 1.889e-09
--- XNOR Gate ---
delay_A_to_XNOR_rise = 2.245e-09
delay_A_to_XNOR_fall = 2.002e-09
delay_B_to_XNOR_rise = 2.221e-09
delay_B_to_XNOR_fall = 1.977e-09
--- AND Gate ---
delay_A_to_AND_rise  = 1.876e-09
delay_A_to_AND_fall  = 1.731e-09
delay_B_to_AND_rise  = 1.843e-09
delay_B_to_AND_fall  = 1.720e-09
--- NAND Gate ---
delay_A_to_NAND_rise = 1.994e-09
delay_A_to_NAND_fall = 1.812e-09
delay_B_to_NAND_rise = 1.960e-09
delay_B_to_NAND_fall = 1.795e-09
--- OR Gate ---
delay_A_to_OR_rise   = 1.765e-09
delay_A_to_OR_fall   = 1.643e-09
delay_B_to_OR_rise   = 1.749e-09
delay_B_to_OR_fall   = 1.655e-09
--- NOR Gate ---
delay_A_to_NOR_rise  = 2.121e-09
delay_A_to_NOR_fall  = 1.954e-09
delay_B_to_NOR_rise  = 2.099e-09
delay_B_to_NOR_fall  = 1.939e-09
```

Figure-7: Delay of All Gates

Signal Integrity

Complementary signals in CPL helped ensure full logic swing. No significant glitches or floating outputs were observed.

Power Efficiency

The simulations revealed lower average power consumption due to reduced transistor switching. CPL gates are ideal for **low-power applications**.

Conclusions

This project successfully demonstrates the **design and simulation of dual-output logic gates** using Complementary Pass Transistor Logic (CPL) in LTSpice. The gates were implemented using fewer transistors, provided fast transitions, and showed reliable logic behaviour. CPL proved to be an effective technique for building **compact and power-efficient logic gates** suitable for modern VLSI designs.

Applications

The gates implemented in this project have a wide range of applications:

- **ALUs (Arithmetic Logic Units):** Used in arithmetic operations and multiplexing.
- **Low-Power Devices:** Ideal for mobile or battery-operated systems.
- **High-Speed Circuits:** Used in processors and digital signal processors.
- **Custom Logic in ASICs:** Useful for optimizing logic in area- and power-constrained designs.
- **Finite State Machines (FSMs):** Compact logic paths make CPL great for control logic and sequencers.

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