DIGITAL SYSTEM DESIGN (EI63)

TWO MARK QUESTIONS AND ANSWERS

UNIT -1

1) What is logic family?

A group of compatible ICs with same logic levels and same supply voltages for performing various logical functions have been fabricated using specific circuit configuration is called as logic family.

2) What is propogation delay?

It is defined as time taken for the output of gate to change when the input have changed.In otherwords,it is defined as the time required by the output to change in accordance with the input.The propogation delay mostly depends on the load capacitance.

3) What is noise margin?

The immune or resistance of a device to noise is called noise immunity.It is an important property in the digital logic family.A quantitative measurement of noise immunity is called noise margin.

4) Mention the flexibilities available in the digital logic family?

- Breath of series.
- Popularity of series.
- Wired logic capability.
- Availability of complement output.
- Type of output.

5) Write the characteristics of TTL?

- The supply voltage is 5V.
- Logical 0 level output voltage is 0-0.4V.
- Logical 1 level output voltage is 2.4-5V.
- Logical 0 level input voltage is 0-0.8V.
- Logical 1 level input voltage is 2-5V.
- Noise immunity is 0.4V.

6) What are the uses of multi-emitter input in TTL?

- It increases the speed.
- Also increases the noise immunity.
- It decreases the propogation delay.

7) Write the advantages & disadvantages of ECL?

Advantages:

- The speed increases.
- Propogation delay is 1 (or) 2 nanoseconds.

Disadvantages:

- Noise immunity is very very low.

7) What is noise immunity?

The difference between the driver output voltage and required load input voltage is called noise immunity.It represents the built-in protection against noise.For TTL,the noise immunity is 0.4V.

8) Define figure of merit?

It is defined as the product of the speed and the power.In otherwords,it is defined as the product of the propagation delay and the power dissipation.

Figure of Merit = Propagation delay(ns) x Power(mW)

9) Write the differences between high speed TTL &low power TTL?

In high speed TTL,the power dissipation will be high(around 22mW) and the propagation delay will be low(approximately 6ns).Some examples are 74H00,74H01,74H02,etc.

In low power TTL,the pwer dissiapation will be low(around 1mW) and the propagation delay will be high(about 35ns).Some examples are 74L00,74L01,74L02,etc.

10) What happens when excess gate voltage is given to CMOS devices?

Because of the thinlayer of silicon dioxide between the gate and the substrate,CMOS devices have a very high input resistance(approximately infinite).The insulating layer is kept

as thin as possible to give the gate more control over the drain current.So,when excess gate voltage is given,the CMOS device will get easily destroyed.

11) Name the methods used for CMOS to TTL interface?

Some of the methods used for CMOS to TTL interface are

- By using a CMOS buffer.
- By giving supply voltage at 5V.
- By open drain interface
- By giving different supply voltages.

12) Explain in brief about IIL?

Integrated Injection Logic is the newest of the logic families and is used widely in large-scale integrated circuits.IIL logic gates are constructed using bipolar transistors.The absence of space-consuming resistors make it possible to integrate a large number of gates in a single package.IIL are easily fabricated and economical,Its speed-power product is quiet small.

13) What are the precautions to be taken while handling MOS devices?

- Individuals handling MOSFET devices and their workplaces should be grounded.
- When a chip is out of circuit,it should be inserted in a specila conductive foam that effectively shorts all pins together.
- In system design,all unused pins should be connected to ground or to the supply voltage.
- Circuits should have power applied before connecting or dis-connecting low impedance signal sources such as pulse generators.

14) Write the difference between Schottky TTL & Low power Schottky TTL?

Schottky TTL devices are very fast,capable of operating reliably at 100 megahertz.The power dissipation is around 20mW and the propagation delay time of Scottky TTL is approximately 3ns.Some examples are 74S00,74S01,etc.

In low power Schottky TTL,the speed is low.The power dissipation is around 2mW and the propagation delay time is approximately 10ns.Some examples of this devices are 74LS00,74LS01,74LS02,etc.

15) Define Fan in and Fan out?

Fan in is defined as the number of inputs connected to the gate without any supply variations.The minimum fan in should be 8.

Fan out is defined as the number of gates driven by the driving states,Simply,it is defined as the number of outputs.

17)What are the characteristics of ECL?

- It has an internal pull-down resistor connected between each input and the negative supply.
- The differential input circuitry in ECL gates provides common mode rejection.
- The output impedance is desirably small.
- ECL gates have very large fanouts and are relatively unaffected by capacitive loads.

18)What are the types of saturated bipolar logic family?

- Resistor Transistor Logic(RTL)
- Transistor Transistor Logic(TTL)
- Integrated Injection Logic(IIL)
- Diode Transistor Logic(DTL)
- Direct Couple Transistor Logic(DCTL)
- High Threshold Logic(HTL)

19) What are the characteristics of digital logic families?

- Speed of operation
- Fan in & Fan out.
- Power dissipation
- Figure of merit
- Noise immunity
- Current and voltage parameters
- Operating temperature range
- Power supply requirements
- Available flexibility.

20)Write about the interfacing circuit?Also explain its functions?

The word ‘interface’ refers to the way a driving device is connected to a loading device.An interfacing circuit is one which is connected in between the load and the driver.Its function is to take the drivers output signal and condition,so that it is compatible with the required merits of load.

UNIT 2

1.What is a PLD?

PLD stands for Programmable Logic Device which simplifies the design of sequential networks and generally leads to lower overall digital system cost.There are five basic types of PLDs.

2.What do you mean by volatile memory?Give example.

If the data cannot be hold in a memory when power is turned off,the memory is referred to as volatile memory.foreg.RAM is a volatile memory.

3.Give the truth table for 4x1 MUX.

INPUTS	S_0	S_1	OUTPUT
I_0	0	0	I_0
I_1	0	1	I_1
I_2	1	0	I_2
I_3	1	1	I_3

4.List some applications of multiplexers.

1. They are used as a data selector.

2.Used to implement combinational logic circuit.

3.Used in time and frequency multiplexing systems.

4.Used in A/D and D/A converter.

5.Used in data acquisition systems.

5.What makes PAL different from PLA?

In PLA both ANDand OR arrays are programmable while in PAL OR array is fixed and AND array is programmable.PLA is costlier and complex than PAL.

6.Compare ROM and PROM.

ROM	PROM
1.Read Only Memory	1.Programmable Read Only Memory.
2.Not programmable.	2.Programmable by the user.

7.List some applications of decoders.

- Used to implement combinational circuits.

- Used to convert BCD into 7-segment code.
- Used in memories to select a particular register.

8.List basic types of Programmale Logic Devices.

PROM,PLA,PAL,FPGA,CPLD.

9.What is PAL?

Programmable Array Logic is a programmable logic device with a fixed OR array and a programmable AND array.

10.What is a decoder?

A Decoder is a multiple-input,multiple-output logic circuit which converts coded inputs into coded outputs,where the input and output codes are different.n input produces 2^n outputs.

11.What is a multiplexer?

Multiplexer is a digital switch which allows digital information from several sources to be routed into a single output line.The basic MUX has several data-input lines and a single output line.

12.What is FPGA?

FPGA stands for Field Programmable Gate Array.It is one of the basic Programmable Logic Device.

13.What are the two ways of achieving memory expansion?

- By expanding word size
- By expanding memory capacity

14.List the classifications of memory.

- RAM
  - ✓ SRAM
  - ✓ DRAM
- ROM
  - ✓ PROM
  - ✓ EPROM
  - ✓ EEPROM

15.What is CPLD?

CPLD stands for CAOMPLEX Programmable Logic Device.It has 48AND gates and 36input pins.Interconnect array acts as select line.

16.Compare PROM,PLA&PAL.

SL.NO	PROM	PLA	PAL
1.	AND array fixed and OR array programmable.	Both AND and OR are programmable.	Only AND is programmable.
2.	Cheaper and simple to use.	Costlier and complex.	Cheaper and simpler.
3.	All minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.

17.Write short notes on memory expansion.

Memory can be expanded by expanding word size and memory capacity.word size can be expanded by connecting two or more ICs together.

18.Compare Static RAM and Dynamic RAM.

SL.NO	Static RAM	Dynamic RAM
1.	Contains less memory cells per unit area.	Contains more memory cells per unit area.
2.	Its access time is less hence faster memories	Access time is greater.

19.Draw the truth table for 2 to 4 decoder.

ENABLE	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

20.What is EEPROM?

Electrically Erasable PROM.A voltage as low as 20 to 25V can be used to move charges across the thin barrier in either direction for programming or erasing.

UNIT-3

1. What is ROM?

   Read Only Memory is a memory device in which permanent binary information is stored. The binary information must be specified by the designer and is then embedded in the unit to form the required inter-connection pattern. The pattern stays within the unit, even when power is turned off and on again.

2. What is a crosspoint in ROM?
   In ROM, the programmable intersection between two lines is called a crosspoint. It is logically equivalent to a switch that can be altered to either be close or open.

3. List out the different methods by which a ROM can be programmed?

   The four different methods are

   1. Mask programming

   2.PROM

   3.EPROM and
   4.EEPROM

4. Compare ROM and EPROM

PROM	EPROM
1. PROM once programmed, the fixed pattern is permanent and cannot be altered.	1. EPROM can be reconstructed to the initial state even though it has been programmed previously.

5. Define RAM.

   Random Access Memory has the basic unit called binary cell. The binary cell can store either 1 or 0 indefinitely, as the power is on. Data can be written into RAM as read out from RAM. The previously stored data can be erased and new data can be written into RAM. Hence it is called read write memory. When power supply is switched off, all the binary cell gets erased.

6. What are the different types of RAM?
    1. NMOS RAM (Nitride metal oxide semiconductor RAM)
    2. CMOS RAM(Complementary metal oxide semiconductor RAM)
    3. Schottky TTL RAM
    4. ECL RAM

7. Define SRAM

    Static RAM consists of internal latches that stores the binary information. The stored information remains valid as long as power is applied to the unit. SRAM is easier to use and has shorter read and write cycles. It is an operating mode.

8. Define DRAM.

    1.The dynamic RAM is an operating mode,which stores the binary information in the form of electric charges on capacitors.

    2.The capacitors are provided inside the chip by MOS transistors. 3.The stored charge on the capacitors tend to discharge with time and the capacitors must be periodically recharged by refreshing the dynamic memory.

    4. Refreshing is done by cycling through the words every few milliseconds to restore the decaying charge.

    5. DRAM offers reduced power consumption and larger storage capacity in a single memory chip.

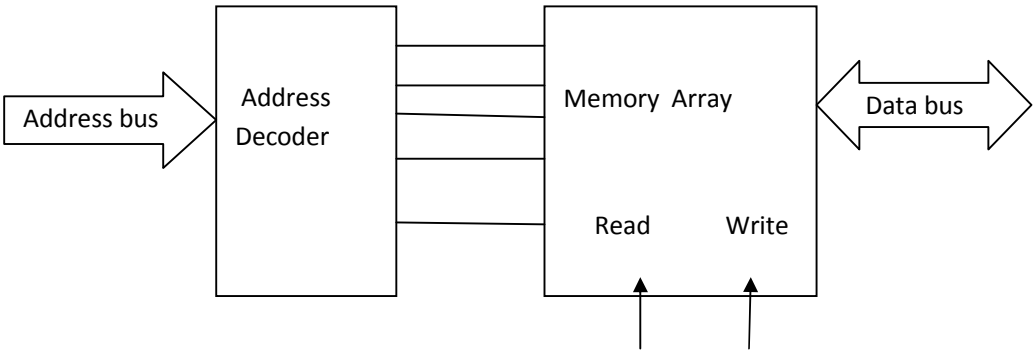
9. Differentiate volatile and non volatile memory.

Volatile memory	Non-volatile memory
They are memory units which lose stored information when power is turned off. Eg: SRAM and DRAM	It retains stored information when power is turned off. Eg: Magnetic disk and ROM

10. What are the types of memory?

    Types of Memories are
    1. ROM
    2. RAM
    3. PROM
    4. EPROM
    5. EEPROM

11. Draw the block diagram of a ROM.



12. Define ROM cell

The structure of a ROM is simple. A cell is located at each position where a row line crosses a column line. At cell locations where a 1 is stored, a voltage controlled switch is connected between the row line and the column line at that location. At cell locations where a 0 is stored there is no connection between the row line and the column line. To read a memory location, apply a voltage to that row line.

13. Describe features of main and peripheral memory.

Main memory:

Main memory is an integral part of the system hardware and is very fast in the sense information can be stored and retrieved from it quickly.

Peripheral memory:

Peripheral memory called auxillary memory, is typically add-on memory with very large storing capacity but slower than main memory. It often serves as data memory for storing very large quantities of data called mass storage. Users store program and data in the peripheral memory, the computer retrieves the program and its associated data stored in temporarily in main memory while it executes the program, and then stores the results back in peripheral memory.

14. Define word,wordsize,nibble

Word: A word is the fundamental group of bits used to represent one entity of information.Word size: Word size is the number of bits.

Nibble: A group of 4 bits is called nibble.

15.What is memory expansion?

. The two principle reasons for expanding memory are to increase the word size or increase the capacity. In bit- organised memory, each integrated

circuit stores 1 bit of each word. A memory in which every bit of a word is stored in a circuit is said to be word- organised

16. Define access time.
    Accesstime of a ROM is the time required to obtain
    valid output when reading it. It can be specified as the interval between the time that the input address bits arevalid and the time that the output data is\

17. List the advantage of RAM cell.

The advantage of RAM cell are

The type of cell is very simple thus allowing very large memory arrays to be constructed on a chip at a lowerbit than in static memories.

18. Write the uses of ROM

The uses of ROM are

1. Used as a look-up tables for code conversion and mathematical functions
2.High capacity ROMS have reduced power consumption

3. It is used as user-specified chip-select inputs.

19. Define EEPROMS

The Electrically Erasable PROM(EEPROM) can be erased and programmed with modest power requirements,so it is possible to integrate erasing and reprogramming circuit into the system utilising the memory.

20. Define ECL RAM

RAM constructed using ECL technology have the highest speeds .The access time for ECL RAM is on the order of 5-10ns.They consume considerable power and are not available in large sizes ,so they are used where speed is the most important consideration. ECL RAMs typically have open-emitter outputs to facilitate expansion and wire-ORing.They have separate pins for input and output data, a feature that can be used to reduce delays between read and write operations.

UNIT – 4

1. What is a multiplexer?

Multiplexer means many into one. A multiplexer is a digital circuit which contains many inputs and only one output. It contains ‘n’ input signals, ‘m’ output control or address signals and only one output (Y) signal

2. What is multiplexing displays?

Multiplexing is a technique used to reduce indicator power requirements. The decimal outputs of digital instruments such as digital voltmeters and frequency counters are often displayed using seven segment indicators. Hence it is called multiplexing displays.

3. Define Counter?

Counter is one of the most useful subsystems in a digital system. A counter is generally driven by a clock signal. It can be used to count the number of clock pulses. The counter can be used to measure time, period or frequency.

4. Write short note on Frequency Counter?

A frequency counter is a digital instrument that can be used to measure the frequency of any periodic waveform.

5. What are the major blocks that are present in frequency counter?
    1) Count gate
    2) Counter
    3) LED Display unit
    4) Clock generator
    5) Frequency divider

6. Draw the block diagram of frequency counter?

7. Define Time Measurement?

Time measurement can be used for the measurement of time period if the counted signal and gating signal are interchanged. It is also called as period measurement.

8. What are the instruments that are used for the measurement of time period?

The instruments used to measure time period are:-

1) Amplifier
2) JK Flip Flop
3) Clock generator
4) Count gate
5) Frequency divider
6) Counter
7) LED display unit

9. Define Digital Voltmeter?

Digital voltmeters are measuring instruments that convert analog voltage signals into a digital or numeric readout.

10. Explain about ADD3501 used indigital voltmeters?

The ADD3501 is widely used as a digital panel meter (DPM) as well as the basis for constructing a digital multimeter(DMM) capable of measuring voltage, current and resistance and it is readily available for around $9.

11. What is the need of control waveforms in multiplexing displays?

In multiplexing displays , by means of control wave forms we can infer which input is going as an output and which act as stand by.

12. What is Flash memory?

Flash memory or a flash RAM is a type of non volatile semiconductor memory device where stored data exists even when memory device is not electrically powered. It is an improved version of EEPROM.

13. Write down the types of flash memory?

There are two types of flash memory. They are:-

1) NOR flash
2) NAND flash

14. Discuss the difference between EEPROM and Flash memory?

EEPROM	Flash Memory
1. It erases and rewrite its content one byte at a time. 2. It can be erasable.	1. Flash memory erases or writes its data in entire blocks which make it a very fast memory compared to EEPROM. 2. Flash memory cant replace DRAM and SRAM.

15. What are the important pins that are used in interfacing with flash memory?
    1. OE (Output Enable)
    2. WE (Write Enable)
    3. CE (Chip Enable)
    4. Byte
    5. VPP (Program/Erase power supply)
    6. RP/PWD (Reset/DEEP power-Down)
    7. A0-A7 Address pins and DQ0-DQ15 Data pins

16. Draw the symbol of 3 input FGMOS transducers?

17. Draw the structure of flash memory cell?

18. Define NOR Flash?

NOR flash memory is a type of non-volatile storage technology that does not require power to retain data. NOR flash is faster, but it's also more expensive and takes longer to erase and write new data. NOR is most often used in mobile phones. NOR flash has an SRAM interface that includes enough address pins to map the entire chip, enabling for access to every byte stored within it.

19. Explain NAND Flash?

NAND flash memory is a type of non-volatile storage technology that does not require power to retain data. NAND has significantly higher storage capacity than NOR. An important goal of NAND flash development has been to reduce the cost per bit and increase maximum chip capacity so that flash memory can compete with magnetic storage devices like hard disks.

20. Write about PRBS Generator?

UNIT-5

1. Define testability.

   Testability of a circuit is an abstract concept that deals with a variety of costs associated with testing. By increasing testability of a circuit ,it is implied that some function of these cost being reduced, though not necessarily each individual cost.

2. What are the factors that determine the complexity of deriving the test of a circuit?

   There are 3 important factors that determine the complexity of deriving the test of a circuit. They are

   - Controllability
   - Observability
   - Predictability

3. What is Controllability?

   Controllability is the ability to establish a specific signal value at each node in a circuit by setting valves on the circuit,s input.

4. Define Observability.

   Observability is the ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs.

5. What are the impacts of accessibility on testing of circuits?

   The impacts of accessibility on testing leads to the following general observations

   - Sequential logic is much more difficult to test than combinational logic.
   - Control logic is more difficult to test than data-path logic.
   - Random logic is more difficult to test than structured bus-oriented logic.

6. Why Ad Hoc design for testability technique is more preferred than other DFT techniques?

Ad Hoc design for testability technique is more preferred than other DFT techniques because they do not deal with a total design methodology that ensures ease of test generation, and they can be used at the designer's option where applicable.

7. What are the major concepts used in Ad Hoc DFT technique?

Ad Hoc DFT technique uses the following concepts,

- Test points
- Initialization
- Monostable multivibrators
- Oscillators and clocks
- Counter/shift registers
- Partitioning large circuits
- Logical redundancy
- Breaking global feedback paths

8. Give some examples of good candidates for control points.

Some examples of good candidates for control points are,

- Control lines to tristate devices
- Data select lines to multiplexers and demultiplexers
- Enable and read/write inputs to memory devices
- Enable/hold inputs to microprocessors.

9. Give some examples of good candidates for observation points.

Some examples of good candidates for observation points are

- Global feedback paths.
- Redundant signal lines.
- Stem lines associated with signals having high fanouts.
- Address,control,and data buses.

10. Define Initialization.

Initialization is a process of bringing a sequential circuit into a known state at some known time, such as when it is powered on or after initialization sequence is applied.

11. List out the 3 generic forms of scan designs.

3 generic forms of scan designs are as follows,

- Full serial integrated scan
- Isolated serial scan
- Nonserial scan

12. What is a scan register ?

Scan register is used to enhance Controllability/Observability. A scan register is a register with both shift and parallel load capability. The storage cells in the register are used as observation points and/or control points.

13. List out the classical scan designs.

The classical scan designs are,

- Scan path
- Shift Register modification
- Scan/set
- Random-Access Scan
- Level-Sensitive Scan Design

14. Define level-sensitive network.

A network is said to be level sensitive if and only if the steady state response to any of the allowed input changes is independent of the transistor and wire delays in that network.

15. What are the attributes associated with use of scan designs?

Some of the attributes associated with use of scan designs are following,

- Flip-flops and latches are more complex.hence scan designs are expensive in terms of board or silicon area.
- One or more additional I/O are required.
- Test generation costs can be significantly reduced.this can also lead to higher fault coverage.

16. Why monostable multivibrators are use in Ad Hoc design for testability technique?

Monostable multivibrators are use in Ad Hoc design for testability technique inorder to disable internal one-shots during test.

17. What is the need for generic Boundary Scan?

In designing modules such as complex chips or PCBs,it is often useful for purposes of testing and fault isolation to be able to isolate one module from others. This can be done using the concept of Boundary Scan.

18. Explain Level-Sensitive Scan Design

IBm has developed several serial integrated scan architectures,referred to as Level-Sensitive Scan Design. This design uses a polarity-hold,hazard-free and level sensitive latch.

19. Explain System-level busses.

This DFT approach make use of a module's or system's functional bus to control and observe signals during functional level testing. A test and/or maintanence processor,such as the ATE,appears as another element attached to the system's busses.

20. List some advanced scan concepts used for testing.

Some advanced scan concepts used for testing are,

- Multiple test session
- Partial scan usin I-paths
- Structured Partial Scan design

PART B

16 MARK QUESTIONS

UNIT 1

1.With neat diagram explain TTL diagram?

Ans: Refer bogart text book and class notes

Derivation

Block diagram

Totempole

Tristate

Open collector

2.Explain ECL NAND operation?

Ans: Refer bogart text book and class notes

Derivation

Block diagram

Totempole

Tristate

Open collector

3.Explain IIL operation?

Derivation

Block diagram

Totempole

Tristate

Open collector

A ns: Refer bogart text book and class notes

4.Explain ANSI/IEEE operation?

Ans: Refer bogart text book and class notes

BLOCK DIAGRAM

Theory

5.Compare the various output configuration of TTL?

Ans: Refer bogart text book and class notes

BLOCK DIAGRAM

Theory

UNIT 2

1.Write notes on ROM and its types.

Ans: Refer bogart text book and class notes

Types

Theory

2.i)What is a decoder?With necessary diagrams explain the operation of 4 to 16 line decoder.

ii)Design a circuit F(A,B,C,D)=∑(1,3,4,11,12,13,15) BY USING 8:1MUX.

Ans: Refer bogart text book and class notes

3.Write short notes on i)FPGA

ii)EPROM

iii)CPLD

Ans: Refer bogart text book and class notes

Block diagram
Theory

4.i)Design a PLA circuit to implement the following function
Fo=ABC+AD;F_1=ABD+BD;F_2=ACD+D'.

ii)Implement a 16:1MUX using 8:1MUX ICs.

Ans: Refer bogart text book and class notes

Block diagram
Theory

5.Explain the steps involved in system design using PLA with an example..

Ans: Refer bogart text book and class notes

Block diagram
Theory

UNIT3

1.Explain ROM cell and its structure?

Ans: Refer Charles Roth text book and class notes

Block diagram
Theory

2.Explain memory types and terminology

Ans: Refer Charles Roth text book and class notes

Block diagram
Theory
Types

3.Explain various types of ROM

Ans: Refer Charles Roth text book and class notes

Block diagram

Theory
Types

4.Explain in detail about magnetic memory

Ans: Refer Charles Roth text book and class notes

Block diagram

Theory

5.Explain RAM and its types
Ans: Refer Charles Roth text book and class notes

Block diagram
Theory
Types

UNIT 4

1. Explain in detail about multiplexing displays?
   Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

2. What is flash memory? Explain the interfacing of flash memory with relevant diagrams?
   Ans: Refer Malvino leach text book and class notes

Block diagram

Theory
Types

3. Discuss the basic operation of digital voltmeters?
   Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

4. Define counter? Discuss about frequency counter and draw its control waveforms?
   Ans: Refer Malvino Leach text book and class notes

Block diagram
Theory
Types

5. Explain with suitable diagram the operation of PRBS Generator?
   Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

UNIT 5

1,Explain in detail about Ad hoc design?
   Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

2.What is testing? Explain the various steps?
   Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

3.Discuss the basic operation of scan register?

Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types

4.Define counter? Discuss about frequency counter and draw its control waveforms?

Ans: Refer Malvino Leach text book and class notes

Block diagram
Theory
Types

5.Explain with suitable diagram the operation of system level bus?

Ans: Refer Malvino leach text book and class notes

Block diagram
Theory
Types