SATISH B SUBRAMANYAM

#13/35, Annapoorneshwari Towers, Bangalore-560061, KA, India
Web: https://in.linkedin.com/pub/satish-b-subramanyam/58/6b9/46b

Ph.: +91-974-206-6170
Email: satishbsibm@gmail.com

EDUCATION

Visvesvaraya Technological University, Belgaum, KA, India — 85.44% [WES GPA: **4.00]**
BE, Electronics & Communication Engineering, Aug 2009 - June 2013 — **Academic Achiever** (Rank: 2/155)

RELEVANT WORK EXPERIENCE

IBM CORPORATION, Bangalore, India

Business Systems Analyst, *Systems Engineering & Architecture (SE&A)* — *Aug 2014 – Present*

- Performed Data Architecting, Business Process/UML Modeling and ETE Systems Engineering for a CMS BR.
- Involved in the entire project cycle – User story creation, high level BR->SR transformation, UAT, Production Go-live.

Interim Project Manager, *AT&T Solutions Group* — *Apr –Aug 2014*

- Managed an ETE project under the AT&T account of IBM -SDLC, OSS/BSS architecture, Agile methodology, Testing phases, Finance Management, Dependencies, Project Scheduling, Communication, SQA, Risk Management.

Systems Engineer, *ERP Group* — *Apr 2013 –Apr 2014*

- Implemented the middleware for integrating incompatible legacy and non-SAP systems with ECC systems. Developed Java mapping UDFs, configured adapters and performed runtime analysis.
- Worked on the System Z server Design for Testability (DFT) flow with IBM STG as part of a stretch assignment.

LSI CORPORATION, Bangalore, India

ASIC Verification GTE, *Networking Component Development (NCD)* — *Apr - Nov 2013*

- Responsible for FV of "PCI Express (PCIe) 3.0" in the AXI subsystem of LSI's standard Communication Processor.
- Developed robust reusable testbenches for 4GB MPage feature verification, automated register verification, scripts for running block level regressions and debugging errors by backtracking and simulation waveform interpretation.

ALCATEL LUCENT MANAGED SOLUTIONS, Bangalore, India

Wireless Communication Intern*, Wireless Networking Group* — *Jul – Aug 2011*

- Analyzed the frequency hop characteristics, MS and BTS output power levels, Antenna tilts, booster operation, area coverage, cell monitoring, Interference levels and power management.

BMS COLLEGE OF ENGINEERING, Bangalore, India

HCI Research Assistant*, Dept. of Medical Electronics & Computer Science* — *Dec 2013 – Apr 2014*

- Designed a mind wave controlled robot for assisting quadriplegics. The robot's direction and acceleration was controlled based on the attention & meditation levels of the acquired and processed EEG signals from brain.

STUDSAT (Student Satellite**) -2**, Indian Space Research Organization, Bangalore, India

Summer Intern*, Command & Data Handling(C&DH) Group* — *Jul 2012 – Aug 2012*

- Designed the redundant data handling module using ARM Cortex MP to implement inter-satellite communication.

INTERNATIONAL PUBLICATIONS

- "**Nanorelays - Power Driver of the next decade**", Regular Paper, *International Conference on Nanotechnology and Biosensors* (**ICNB 2012**), Dec 22-23,2012, Kuala Lampur, Malaysia; Published in the International Proceedings of Chemical, Biological & Environmental Engineering (IPCBEE), V48,p161. [http://ipcbee.com/list-73-1.html].

- "**High sensitivity Nanorelay based C-P sensors for biomedical implants**", Regular Paper, *8th IEEE, International Conference on Intelligent Sensors, Sensor Networks and Information Processing* **(IEEE ISSNIP 2013),** Apr 3-5, 2013, Melbourne, Australia. [http://ieeexplore.ieee.org/ielx7/6520926/6529738/06529743.pdf].

ACADEMIC PROJECTS

Physical design of parallel AES algorithm at 40nm technology node, *VLSI – System on Chip* *Aug – Dec 2012*

- Designed the PD flow=> Input: DCC generated netlist-> [Floor Planning -Placement –Routing -CTS (ICC) -Power analysis -STA (Primetime) –LVS –DRC -Parasitic Extraction (STARRC) -Physical Verification] -> Output: GDSII file.

H/W implementation of RC6 crypto-coprocessor using the fastest Multiplier-Adder, *VLSI -FPGA* *Jan – Jun 2013*

- Designed, verified and synthesized the RC6 crypto-algorithm using ALTERA Cyclone IV FPGA.
- Vedic theorems were used for optimization to obtain a 6% improvement in speed, area and power consumption.

Spectrum Harvesting using ARQ and probing for Cognitive radio application, *Wireless Comm.* *Aug – Dec 2013*

- A secondary pair listens to the primary ARQ feedback to glean information about the primary channel's state.
- Analyzed the system's performance to show that secondary throughput can be significantly improved without any primary outage.

TECHNICAL SKILLS

- **Business Tools:** MS Visio/Excel, Casewise Corporate Modeler, Rational Software Architect (RSA), ReqPro.
- **EDA Tools**: Cadence Virtuoso, Synopsys IC Compiler, VCS, Xilinx ISE, Questasim, Keil, Quartus II.
- **Programming Languages:** C/C++, VHDL/Verilog/System Verilog, ALP, PL/SQL, SAP-ABAP, Perl, MATLAB.

HONORS

- **MHRD Scholarship** from Ministry of Human Resource & Dev.**,** Govt. Of India, 2009-2013.
- **Meritorious Performance** award for securing second position during 2009-2010.
- **Academic Excellence** award for securing outstanding grades during 2010-2011.
- **IIT-JEE Achiever** award by BASE for securing EML rank in IIT-JEE exam during 2009.
- **Proficiency** awards in recognition for securing 100% in Computer Science and Mathematics.
- **IBM Deep Skill Adder Award, Q3 and Q4, 2015**, IBM, reward for demonstrating critical skills needed to support strategic solutions.

EXTRA-CURRICULAR

• **Student Mentee, Global Shapers, SAP Labs Inc.** *Feb - Jun 2012*

- Nominated for participation in the Youth Summit, 2012 headed by the world economic forum and Global Shapers.
- Underwent a six-month mentorship drill on Consulting & Corporate Leadership at SAP Labs.

• **CEO Shadowing Program, Global Shapers, Sonata Software Ltd.** *July 2012*

- Shadowed the CEO of Sonata software to understand the end-to-end operations of a business: management hierarchy, finance decisions, marketing strategies, services & delivery management.

• **Treasurer, IEEE Student Branch, RNSIT** *Jan-Dec 2012*

- Conducted workshops/events as part of the IEEE student chapter including an Inter-state IEEE technical fest -2012