ANY TIME ELECTRIC BILL PAYMENT MACHINE

TEAM: ERROR404

APPROACH

STEPS TAKEN:

1. Identified the inputs as **clk,rst,cashop,cheqop,stop,IA** which are clock signal, rest,cash option,cheque option, the stop switches and for storing the input amount from the user then, the outputs as **EXCSO** and **BAO** for storing the final exess amount and input amount.Also initialised the registers **BA** and **EXCS** for storing the values of the bill amount and excess amount of the user.
2. Then taken the states as **START, INFO_MODE, CASH, CHE_DD_PAYO,WAITING_CASH, INSUFF, WAITING_CHE_DD_PAYO, COMPLETED** which defines the various stages of the machine and thus enabling the trasition between various states.
3. Then drawn the state machine diagram of the given problem statement.
4. Considiring the state diagram along with the inputs and the outputs it became possible to start the initial stages of Verilog coding in Intel quartus.
5. At the **START** state the machine shows a welcome msg and request user for showing the bill at the scanner.
6. At the **INFO_MODE** state even if the input of scan is high it displays the details of the user including the bill information and mode of payment options.
7. At the scanning due to the lack of a particular database from any of the Electricity Boards, initialized BA and EXCS by giving some values and then moving on to the next state.
8. At the **CASH** state the machine displays the regarding the information of denominations and takes the user to the next state even if the IA is high.
9. During the **CHE_DD_PAYO** state similar to the **CASH** state it informs the user regarding some warnings of the input.
10. At the **WAITING_CASH** state the machine waits for the user to input the specified denominations and continues until the Bill amount **BA** is satisfied or else if the user doesn't have enough amount he can stop the process and thus resulting into move into the **INSUFF** state.
11. At the **WAITING_CHE_DD_PAYO** the similar case as of the **CASH** occurs and thus resulting into moving into the next state.
12. Even if the user inputs the insufficient amount then the next state is the **INSUFF** else the next state is the **COMPLETED** state.
13. After the Verilog coding obtained the output waveforms at the modelsim and the results.
14. Then done the area analysis as well as the power analysis and pasted it on the report.
15. After completing all the major steps files are uploaded in the GitHub.