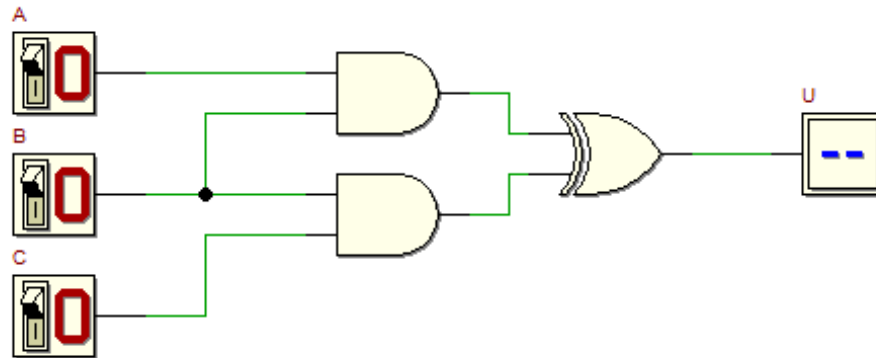


1. Analysis of combinational networks (Total 5 points)

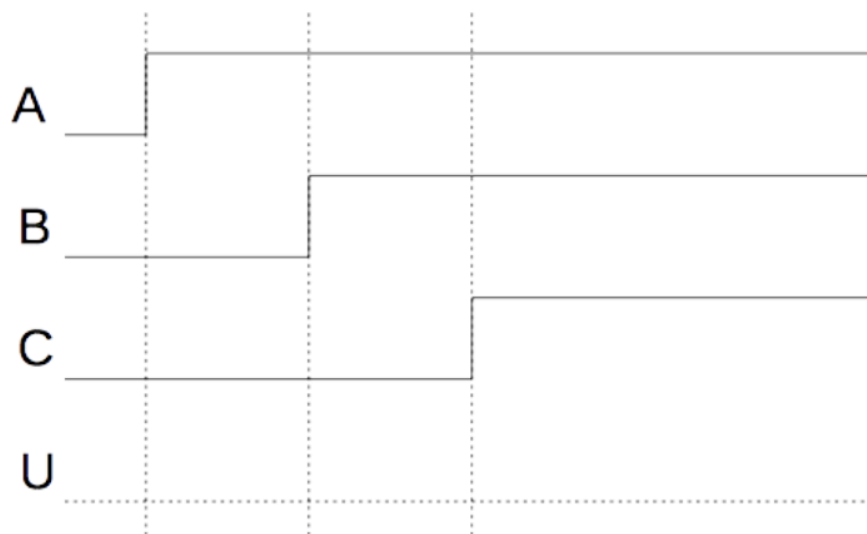
Consider the following combinational network:



1.1. Fill out the following truth table (2 points)

A	B	C	U
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

1.2. Fill out the following timing diagram (3 points)



2. Optimization of Boolean functions (Total 5 points)

2.1. Synthesize the following Boolean Function with AND/OR synthesis (2 points)

			W			
			0	0	0	0
X			0	0	1	1
			1	0	1	1
			1	1	0	1
			Y			
						Z

$F(X,Y,Z,W) =$ _____

2.2. Synthesize the following Boolean Function with OR/AND synthesis (2 points)

			W			
			0	0	1	1
X			1	0	1	1
			1	1	0	1
			0	0	0	0
			Y			
						Z

$F(X,Y,Z,W) =$ _____

3. Binary Arithmetic (Total 10 points)

3.1. Convert the following number from base 2 to base 10 (1 point)

$$1011001_2 = \underline{\hspace{2cm}}_{10}$$

3.2. Convert the following number from base 10 to base 2 (2 points)

$$117_{10} = \underline{\hspace{2cm}}_2$$

3.3. Represent in base 2 the following negative number using the 2 complement representation with 5 digits (2 points)

$$-13_{10} = \underline{\hspace{2cm}}_2$$

3.4. Execute the following sum of two positive base 2 numbers (2 points)

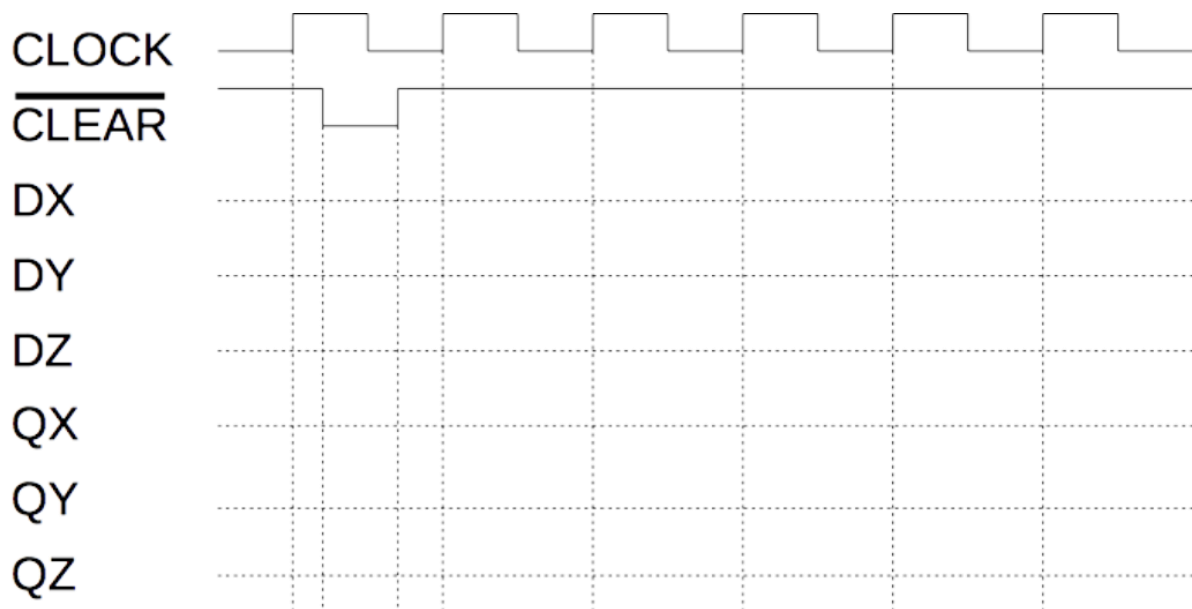
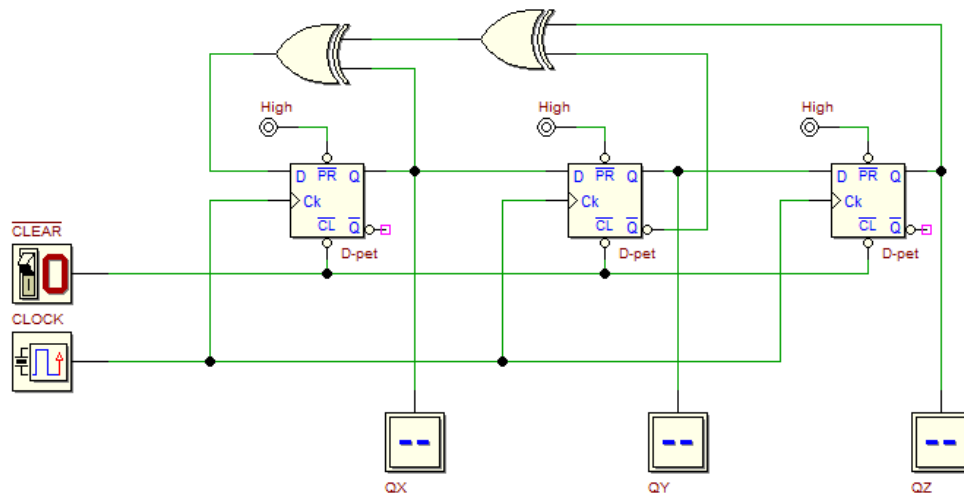
$$\begin{array}{r} 10110100 + \\ 00111101 = \\ \hline \end{array}$$

1.1. Execute the following subtraction of two positive base 2 numbers (3 points)

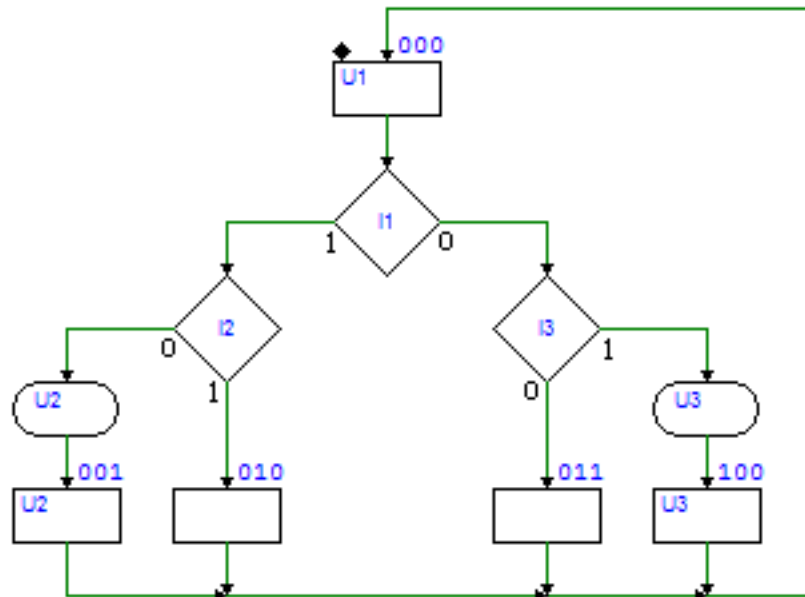
$$\begin{array}{r} 10110100 - \\ 00111101 = \\ \hline \end{array}$$

2. Analysis of sequential networks (Total 25 points)

2.1. Consider the following sequential network and fill out the corresponding timing diagram (15 points)



2.2. Consider the following Mealy FSM and fill out the corresponding timing diagram by indicating the states and the outputs of FSM (10 points)



STATE

CLOCK

RESET

11

12

13

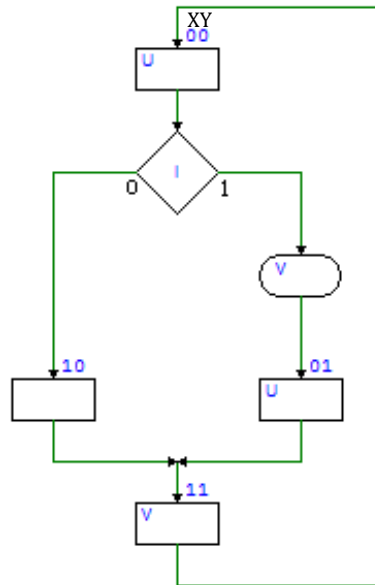
U1

U2

U3

3. Synthesis of sequential networks (Total 15 points)

Consider the following Mealy FSM



3.1. Synthesize the next state combinatorial network where the register is composed of two FF D (2 points)

$D_x =$ _____

$D_y =$ _____

1.1. Synthesize the next state combinatorial network where the register is composed of two FF D (10 points)

$J_x =$ _____

$K_x =$ _____

$J_y =$ _____

$K_y =$ _____

1.1. Synthesize the output combinatorial network (3 points)

$U =$ _____

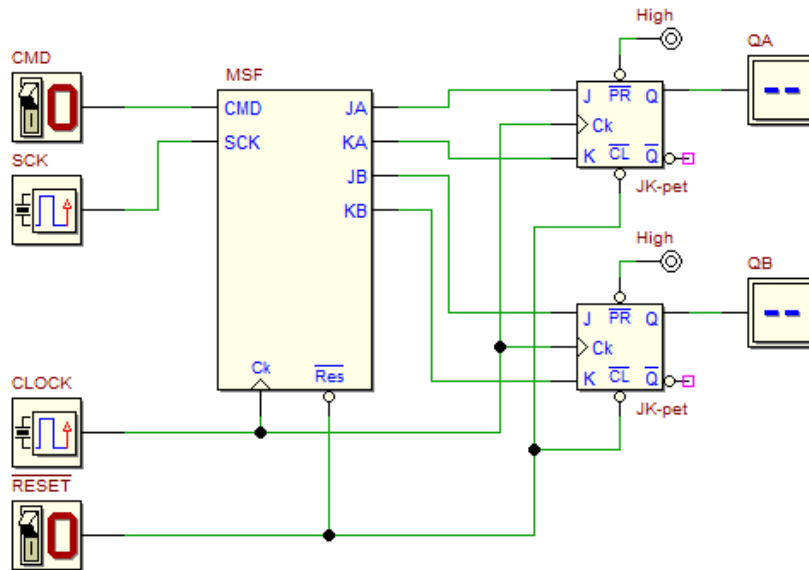
$V =$ _____

2. Project of a FSM (Total 40 points)

The system depicted in the next figure is the control of a blinker with two lights (light A and light B).

The system is composed by a clock synchronous FSM that receives a control command through the serial line CMD. The FSM controls two FF JK that themselves control the state of the lights of the blinker through the signals JA, KA and JB, KB. The light A (and analogously B) is on when the output of the FF QA is at logic level 1 and off otherwise. The FSM has another input SCK where it receives a slow clock of period 1 second.

The asynchronous RESET has the purpose of bringing the system in its initial conditions.



The input line CMD, usually at logic state 0, receives synchronous serial packets composed of four bits, each has a clock cycle period. The first bit, the start bit, is 1 and the last bit, the stop bit, is 0.

The two middle bits represents a code which identifies the blink type based on the following table.

Code	Blink type
"00"	Both lights off
"01"	Light A blinking (Light B off)
"10"	Light B blinking (Light A off)
"11"	Light A and B blinking (both on and off at the same time)

Every time the FSM receives a new packet on CMD the system sets the right blinking mode and stays in that mode until a new packet arrives. The blinking period is approximately 1 second.

Suppose that the input SCK is reset once a new packet arrives and do not consider the time needed for the transition between different modes.

2.1. Description of the FSM (25 points)

Draw the diagram of the FSM and indicate the RESET state.

[Hint: start the design from the blinking modes]

2.2. Timing Diagram (15 points)

Fill out the timing diagram according to the designed FSM

[Note that the second diagram is the continuation of the first one after half a second]

