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ECE 533: Computer Design and Architecture

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Optimum Superscalar Processor

Done by

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Abbreviations

Superscalar factor	(S)
Number of integer floating units	(FU)
Number of floating point functional units	(FFP)
Number of branch functional units	(FB)
Number of memory functional units	(FM)
Reservation stations multiplicity	(N_{RS})
Number of reorder buffer entries	(N_{RB})

I. Abstract :

This report aims in designing an optimum superscalar RISC processor by exploring its designs. A superscalar processor is one that is capable of sustaining an instruction execution rate of more than one instruction per clock cycle. Therefore different processor components have to be scheduled in an effective manner to maintain this execution and provide high utilization with the best performance. This report thus brings forth an optimum solution for better performance with lowest power consumption.

II. Introduction:

The performance of a superscalar processor depends upon the instruction per cycle throughput (IPC). To maximize the performance of the processors the parameters like number of reorder and renaming buffers, superscalar factor, floating point functional units, integer functional units, memory functional units, branch functional units, reservation stations, number of caches can be changed. In this report we assume a particular set of characteristics to be set throughout the simulations which is mentioned under section III of this report. The various designs of a superscalar RISC processor is done using the PSATSim architecture simulator from design of a superscalar RISC processor using the PSATSim[1]. A particular trace file is taken in this simulator and various designs are tested to obtain the optimum performance point. This is obtained by the method which in this report is called as the Break-point-constant test and is further explained in section IV . In this report, the parameters are selected in a way such that the chip area is less than equal to 60 mm^2.Sections V deals with the analysis and findings of the mentioned testing designs in which of the data obtained during this test suggests in choosing particular parameters for the processor to give the best performance. Section VI provides the limitations in such a proposed analysis. This report mainly provides three configurations. The first configuration provides the highest performance; second configuration provides the lowest energy consumption and third deals with the best balance between the performance and energy cost, thus providing an optimum superscalar processor. These configurations are mentioned in the section VI with trade-off's in of these estimated values.

III. Simulation background:

For the analysis in this report we use the compress trace file which gives a trace of the instructions completed during the execution of the Spec95 'compress' benchmark program.

The characteristics assumed before starting the simulation:

- Instruction fetches hit in the L1 cache is 97% of the time.
- Data fetches hit in the L1 cache 94% of the time.
- All L1 caches have a latency of 1 cycle.
- L2 cache hit is 99%
- L2 cache latency is 3 cycles.
- System memory latency is 5 cycles.
- Branch prediction accuracy is 93%.

The parameters that are varied are :

1. Superscalar factor (S)
2. Number of integer floating units (FU)
3. Number of floating point functional units (FFP)
4. Number of branch functional units (FB)
5. Number of memory functional units (FM)
6. Reservation stations multiplicity (N_{RS})
7. Number of reorder buffer entries (N_{RB})

For this report, it's assumed that the number of renaming buffers is made equal to the reorder buffers and also the chip area is not more than 60 mm^2.

IV. Methodology:

Each variable parameter (mentioned under section III) varies for 8 values respectively by maintaining the other such parameters at its highest possible value.
For example, the FU, FFP, FB and FM are maintained constant at their highest value that is 8 and also N_{RS} , N_{RB} are maintained constant at a randomly chosen value of 150.
Now, the superscalar factor is varied for 1 to 8 and each time its varied, its respective IPC, power and execution time (ns) is noted down. The energy is thus calculated from the equation,

$$\text{Energy (Joules)} = \text{Power (Watts)} \times \text{Time (secs)} \qquad \text{..... (1)}$$

Graphs are plotted for each Energy and IPC value obtained for their respective change in its superscalar factor. The optimum superscalar factor is noted from the breaking point of the graph.
This process is repeated for each of the above varying parameters.

After its completion, the obtained optimum values of each of these parameters and simulated together. A hit and trial method is used around these optimum values to obtain the best IPC value for a higher performance level. Similarly, the optimum values that provide the lowest energy consumption is noted. A best balances between performance and energy cost is estimated which provides an optimum superscalar processor. Also, in doing so the chip area is calculated and maintained to be not more than 60 mm^2. The chip area is calculated as :

CPU COMPONENT	Chip area Cost function (mm^2)
Reservation stations	$0.065\times(FI + FFP+FB+FM)\times N_{RS}$
Integer units	$2.0\times FI$
Floating point units	$3.5\times FFP$
Branch Units	$1.5\times FB$
Memory buffers	$3.0\times FM$
Reorder buffers	$0.04\times N_{RB}\times S + 0.035\times N_{RB}$

Table 1 : Calculation of the chip area

V. Analysis and Findings:

The following graphs are obtained by implementing the above methodology. The optimum values for S, FI,FFP,FB,FM,N_{RS},N_{RB} are located with the help of the break –point-constant test method.

Optimum values obtained from the below mentioned graphs for

a) Providing best performance :

S= 9 ; FI= 3; FPP= 3 ; FB= 2 ; FM= 4; N_{RS}= 3 ; N_{RB}= 50

b) Providing the lowest energy consumption:

S= 2 ; FI= 2 ; FPP=1 ; FB=2 ; FM=3; N_{RS}=2 ; N_{RB} = 20

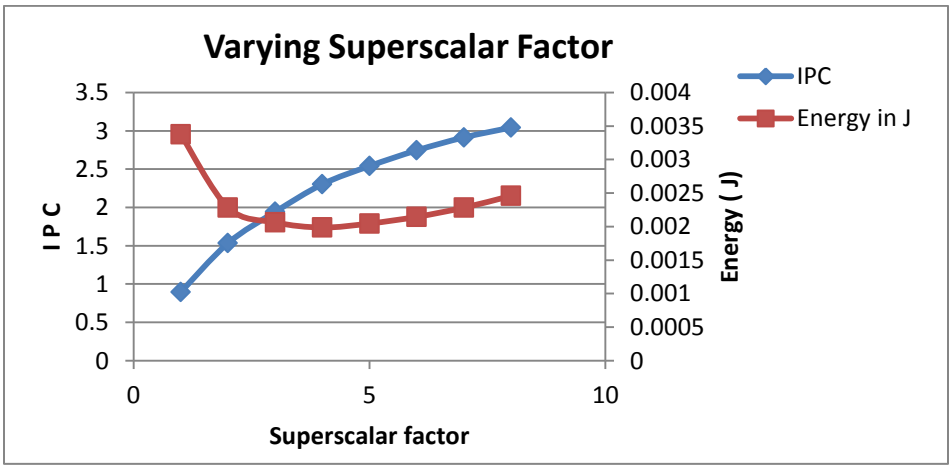

Fig 1: Different values of superscalar factors vs IPC and Energy (J)

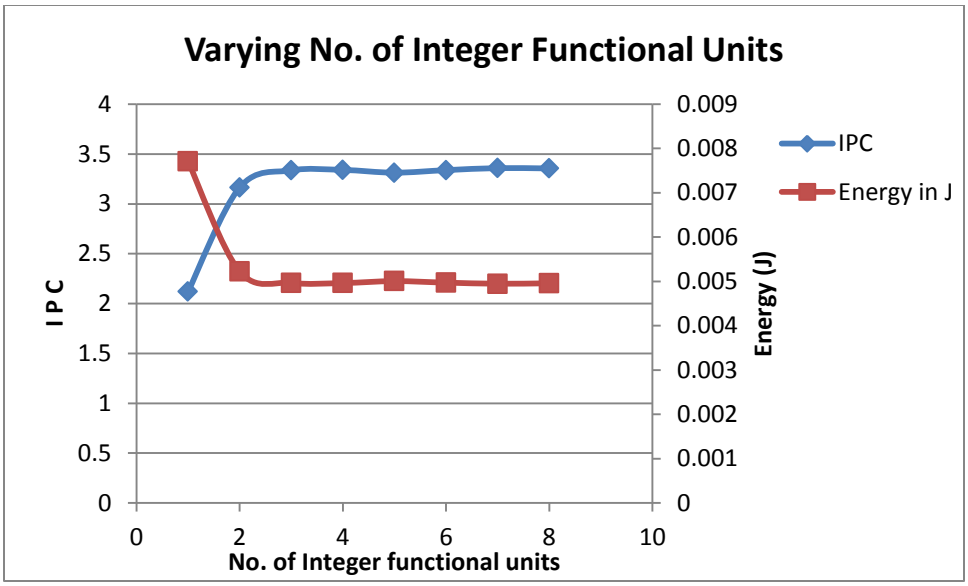

Fig 2:Various no. of the integer functional units vs IPC and Energy (J)

Its observed from fig 2 that as we try to obtain the lowest energy consumption we tend to

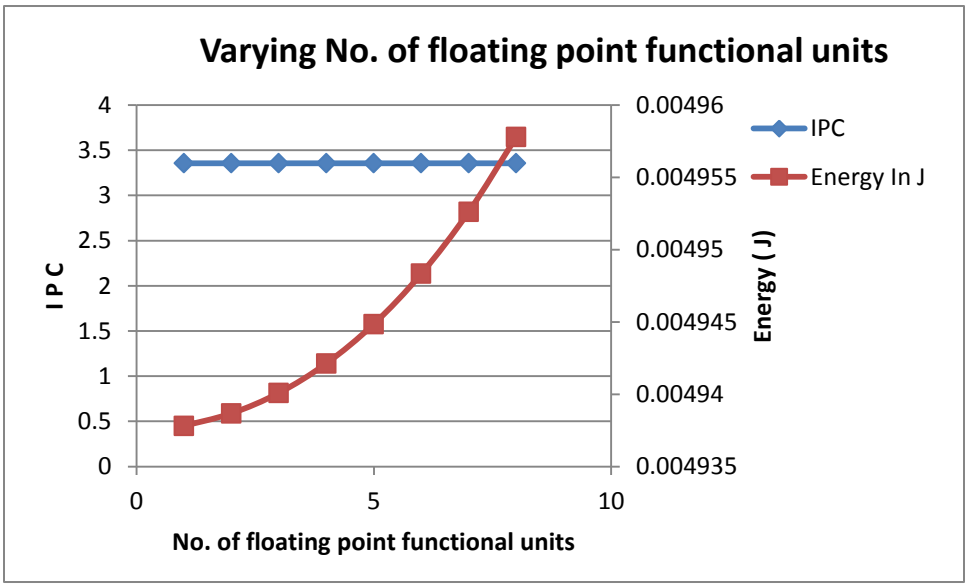

Fig 3: Various of no. of floating point functional units vs IPC and Energy (J)

Its also observed from fig 3 that by varying the number of functional units there is relatively no change in the IPC of the processor but the energy consumed increases exponentially.

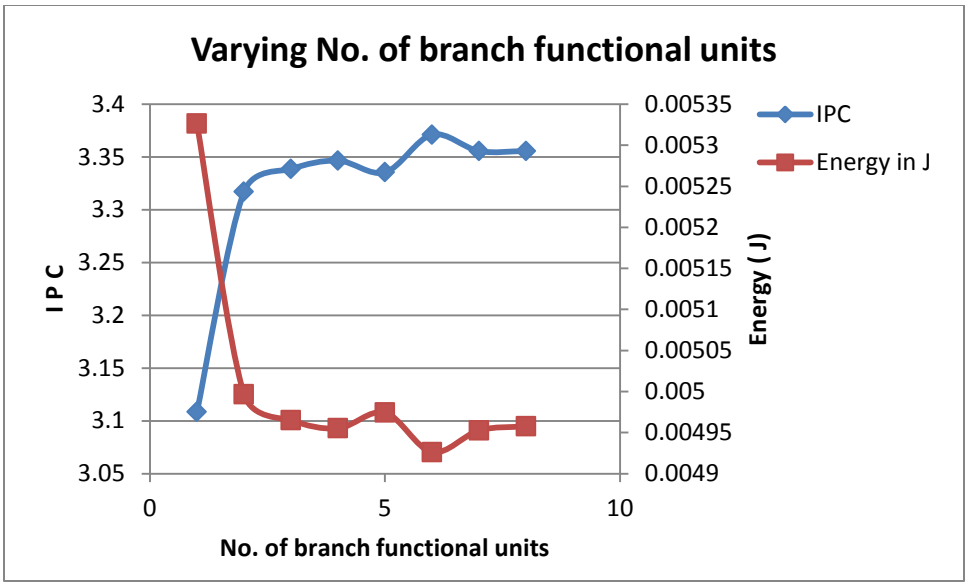

Fig 4: No. of branch functional units vs IPC and Energy (J)

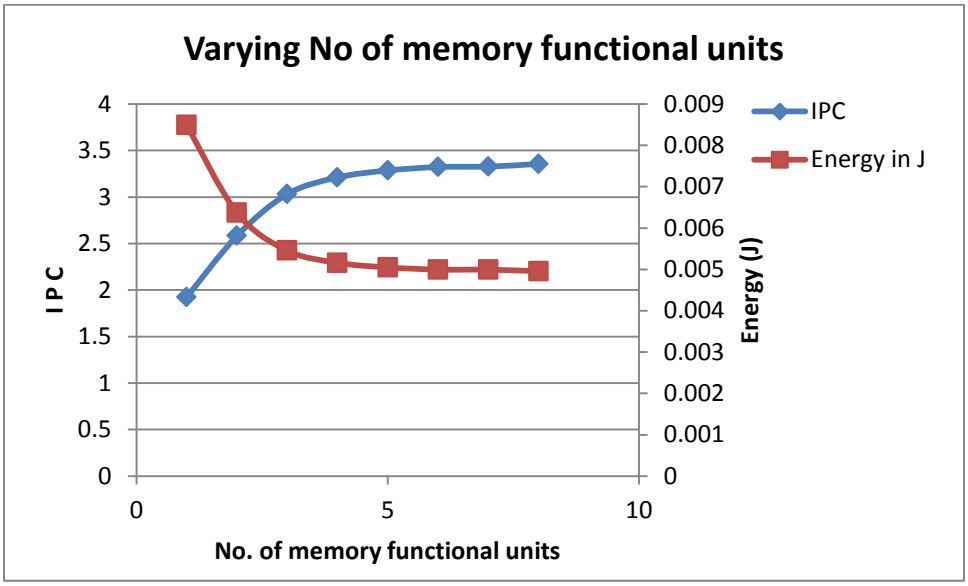

Fig 5: Number of memory functional units vs IPC and Energy (J)

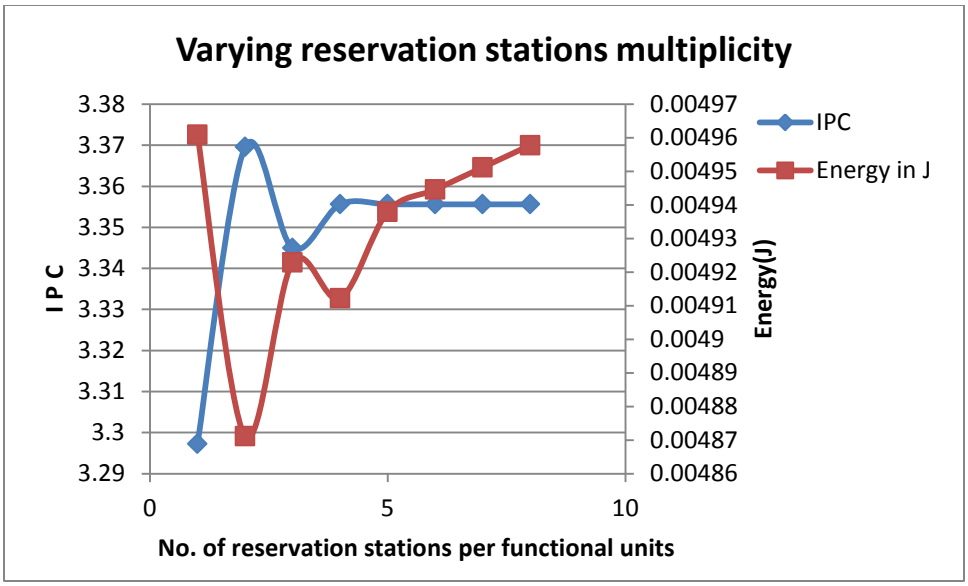

Fig 6: Different reservation stations multiplicity vs IPC and Energy (J)

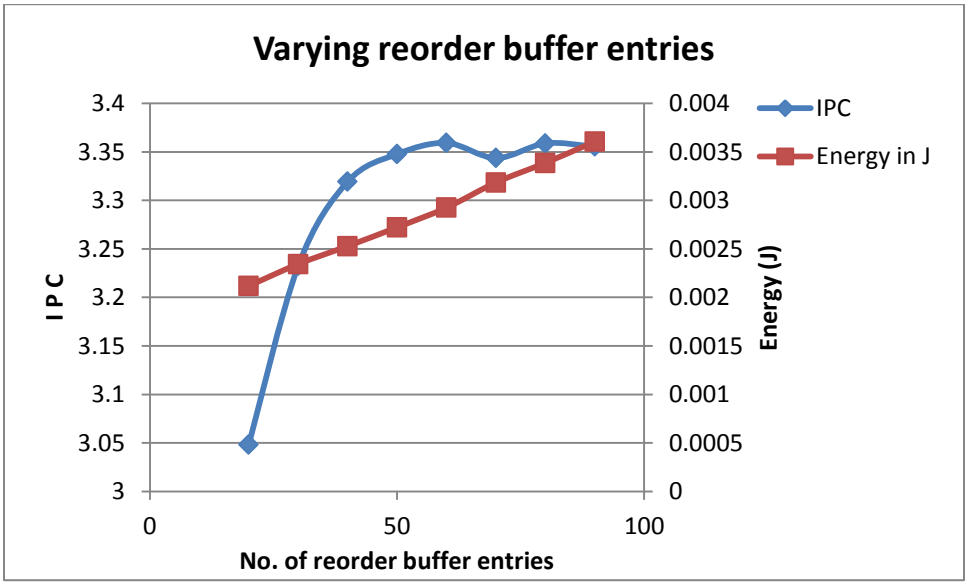

Fig 7: Various values of reorder buffer entries vs IPC and Energy (J)

From fig 7 its observed that by increasing the number of reorder buffer entries, the energy consumption increases almost linearly and the IPC value increases and reaches a constant value.

To achieve the best balance optimum solution between the performance and energy consumption of the processor, the simulations in table 3 are performed.

S	F1	FFP	FB	FM	N_{RS}	N_{RB}	IPC	Power (W)	Time (s)	Energy (m J)	Area (mm^2)
10	**4**	**3**	**2**	**4**	**4**	**50**	**3.006**	**29.9978**	**6.47**	**1.9416**	**58.63**
5	**2**	**1**	**2**	**4**	**2**	**20**	**2.4**	**17.177**	**8**	**1.405**	**23.2**
6	2	1	2	4	2	10	2.14	16.866	9.08	1.5322	21.3
6	3	1	2	4	2	10	2.33	16.95	8.6	1.4727	21.3
6	2	1	1	4	2	10	2.14	16.86	9.08	1.531	19.8
5	3	1	2	4	2	10	2.17	16.27	8.94	1.45	20.9
8	**2**	**1**	**2**	**4**	**2**	**20**	**2.604**	**20.23**	**7**	**1.5**	**25.7**
9	2	1	2	4	2	20	2.645	21.39	7	1.6	26.5

Table 2 : Different simulations for achieving the best balance optimum solution between the performance and energy consumption of the processor. Green- represents configuration 1; Blue – represents configuration 2; Red – represents configuration 3(explained in next section).

VI. Results and Limitations:

a) Configuration 1 : Provide the highest performance

Parameter	Value
Superscalar factor (S)	10
No. of integer functional units (FI)	4
No. of floating point functional units (FFP)	3
No. of branch functional units(FB)	2
No. of memory functional units (FM)	4
Reservation stations multiplicity (N_{RS})	4
No. of reorder buffer entries (N_{RB})	50

Table 3 : Parameter values that provide the highest performance

The IPC determines the performance of the system. The better the value of IPC , higher is the performance of the processor. Thus with the above set of values, the IPC obtained is 3.006 and the Energy consumption is 1.941 mJ with a total chip area of 58 mm^2 calculated using the equations in table no. 1.Thus its observed that to have an increase in performance of the processor, the energy consumption is pretty high.

b) Configuration 2: Provide the lowest energy consumption

Parameter	Value
Superscalar factor (S)	5
No. of integer functional units (FI)	2
No. of floating point functional units (FFP)	1
No. of branch functional units(FB)	2
No. of memory functional units (FM)	4
Reservation stations multiplicity (N_{RS})	2
No. of reorder buffer entries (N_{RB})	20

Table 4 : Parameter values that provide the lowest energy consumption

The energy is calculated as per equation (1) . From the above set of values in table (3) , the Energy consumption is obtained as 1.405 m J and IPC is 2.4. Thus its seen that to obtain a processor to have lowest energy consumption, the performance of the processor goes down.

c) Configuration 3: Best optimum solution for performance and energy cost

Parameter	Value
Superscalar factor (S)	8
No. of integer functional units (FI)	2
No. of floating point functional units (FFP)	1
No. of branch functional units(FB)	2
No. of memory functional units (FM)	4
Reservation stations multiplicity (N_{RS})	2
No. of reorder buffer entries (N_{RB})	20

Table 5 : Best optimum solution for performance and energy cost

The IPC obtained with this set of values is 2.60464 and the energy consumption is 1.511m J , consuming an area of 25.7 mm^2.

VII. Conclusions:

VIII. References:

1. http://homepages.udayton.edu/~ttaha1/psatsim/