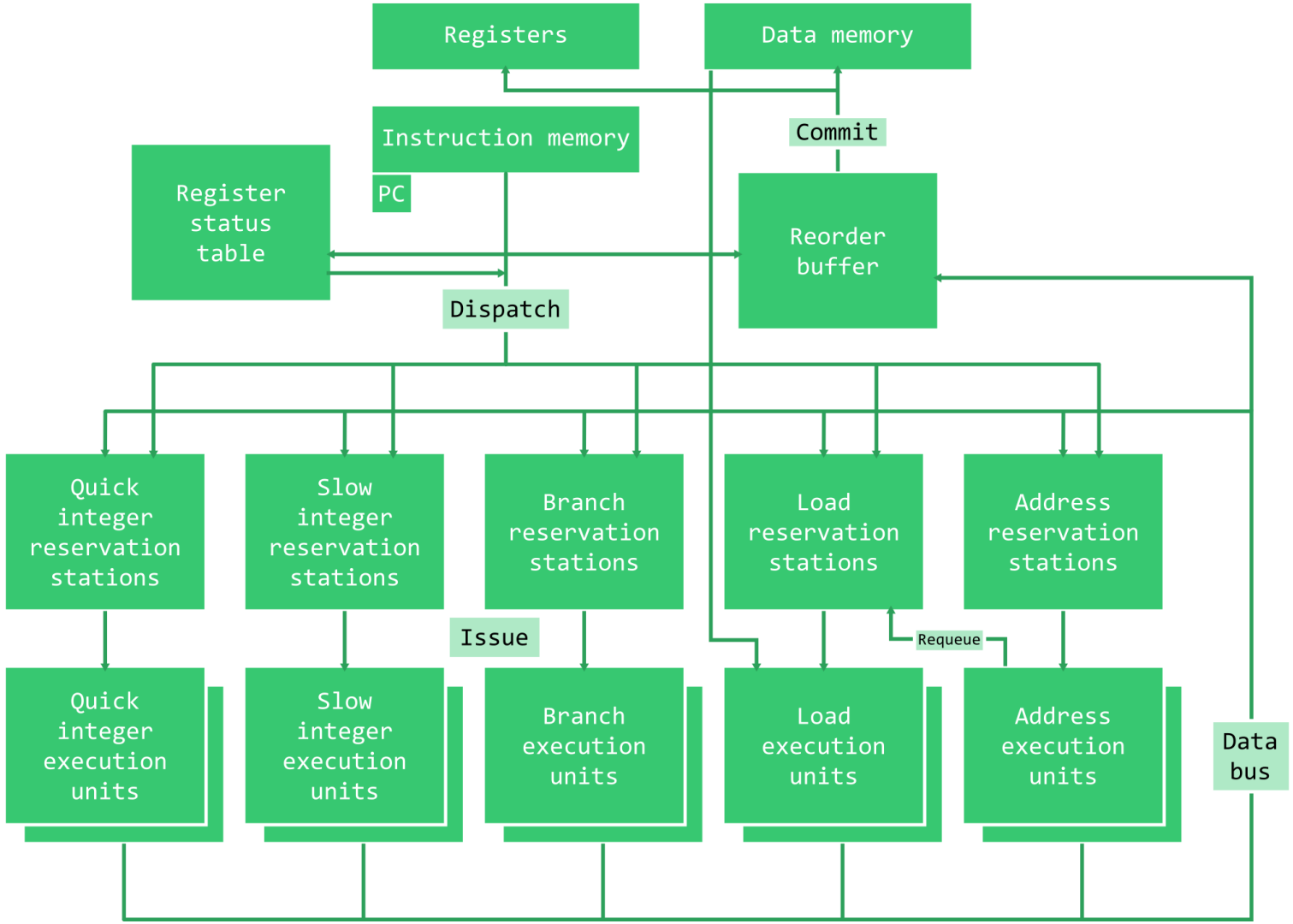
Aku

A superscalar, out-of-order CPU simulator

COMSM0109 Advanced Computer Architecture

Ross Gardiner (rg14820)

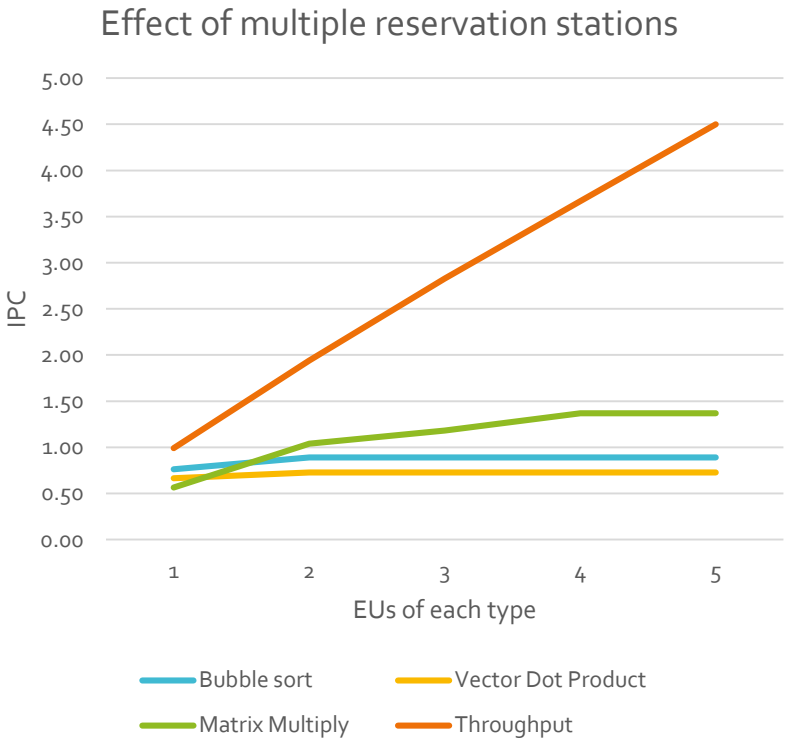
Architecture



Architectural Features

- Re-order buffer (controllable size)
  - Register renaming, in-order commit
- Multiple execution units (controllable size)
  - Quick integer (add, sub), slow integer (mul), address, load, branch
- Speculative execution
  - Static branch prediction – never taken
- Group reservation stations (controllable size per group)
  - Fixed (controllable) issue per group, per cycle

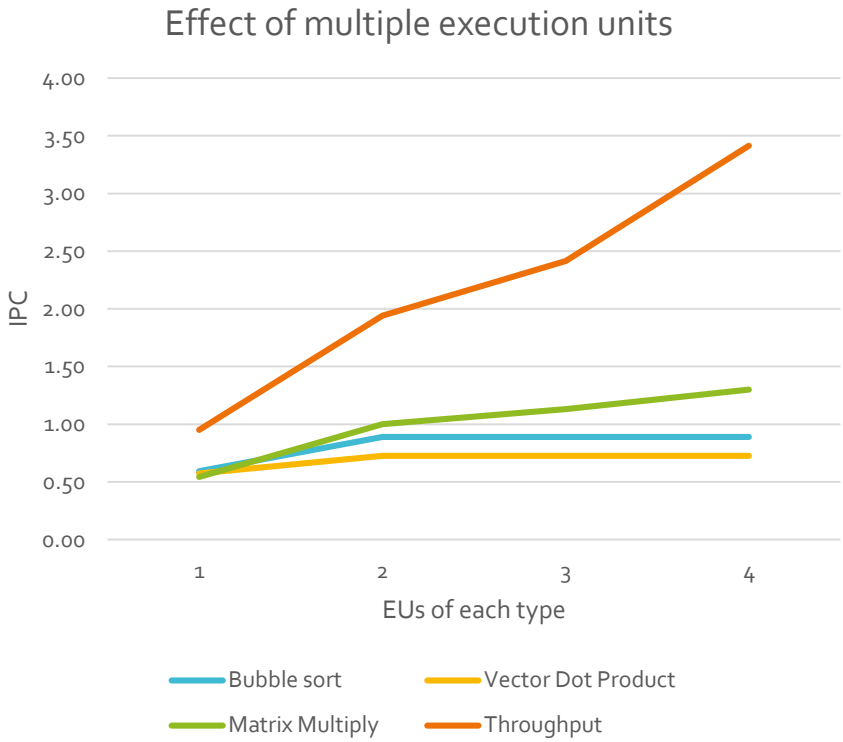
Experiments



EUs: 10 of each type

Memory latency: 3 cycles

Dispatch/issue/commit width: 10

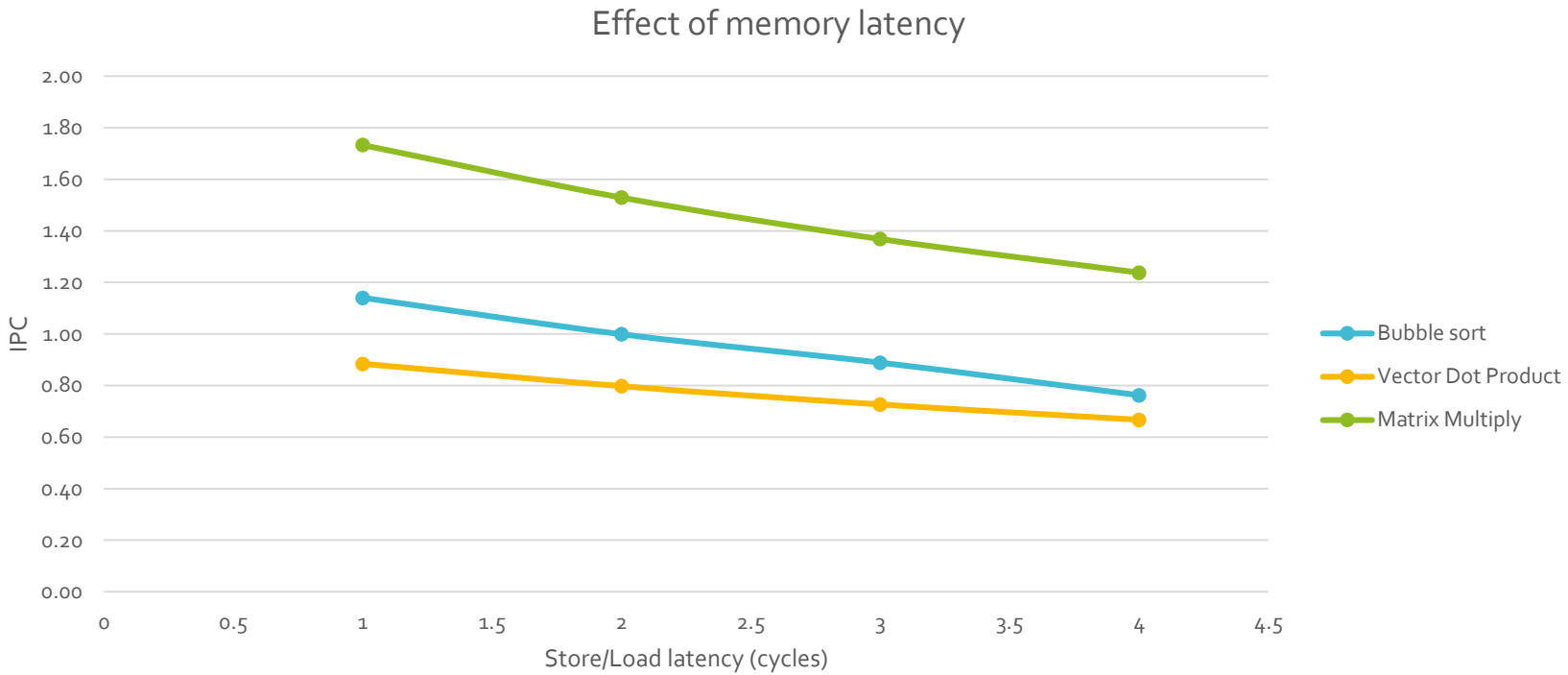


RSVs: 10 of each type

Memory latency: 3 cycles

Dispatch/issue/commit width: 10

Experiments



- The time required to perform stores and loads has a significant impact on performance of all algorithms (except throughput demo)
  - Memory caching would significantly improve performance compared to reading/writing main memory directly