# 02223 Fundamental models for modern embedded systems E10

[Scheduling deterministic] *

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## ABSTRACT

## 1. INTRODUCTION

## 2. THE WCET

The Worst Case Execution Time is the maximum time a given task can take up the cpu. It has a complimentary brother called Best Case Execution Time.

### 2.1 Obtaining WCET

To be able to obtain the exact WCET it is essential that the hardware is known, and all post an preconditions.

Modern processors tend to try and make things run faster by utilizing pipelines, instruction caches and branch prediction.

#### *2.1.1 Branch prediction*

When a branch in the program is reached (for example an if statement), the processor will try to predict which route the software will take. This saves cpu cycles, when guessed correctly, but costs extra cycles when an incorrect prediction is made, due to the fact that all the instructions that was lined up, now has to be replaced.

#### *2.1.2 Pipelining*

#### *2.1.3 Instruction cache*

#### *2.1.4 Virtual memory*

A few suppliers of real-time operating systems gives the programmer the option of using virtual memory, giving the benefit of being able to extend the application. QNX for example has this feature. The majority of suppliers does not implement virtual memory though, so in most cases this is not an issue.

*This report should also be available online at `www.retrospekt.dk/02223report`

## 3. VERY SIMPLE SIMULATOR

### 3.1 Rate monotonic scheduling

Rate monotonic scheduling (RMS) is used when you have a set of periodic tasks without the need for preemtion.

### 3.2 Schedulability analysis

The schedulability analysis is based on the following theory:

#### *3.2.1 Generation of the random numbers*

Uniform distribution.

> Returns a pseudorandom, uniformly distributed int value between 0 (inclusive) and the specified value (exclusive) ... All n possible int values are produced with (approximately) equal probability

Perhaps a seed could be used for recreating the random numbers

## 4. RESPONSE-TIME ANALYSIS

## 5. SOMETHING ADVANCED

## 6. CONCLUSION

## APPENDIX