Hadassah Academic College

Department of Computer Science

Computer Architecture **Exercise 10**

1. Consider two CPUs with the following cache characteristics:

	CPU 1	CPU 2
Bytes per block	64	64
Cache type	Unified (data + instruction)	Unified (data + instruction)
Cache size	16 KB	16 KB
Associativity	2-way	1-way
Storage policy	write-through no-write-allocate	write-back write-allocate

A. For CPU 1 and CPU 2 find the set into which a byte at memory address **0x2000** will be copied in cache. In each cache a block is already in the destination set before the transfer of byte **0x2000** to cache. How will each CPU handle the transfer?

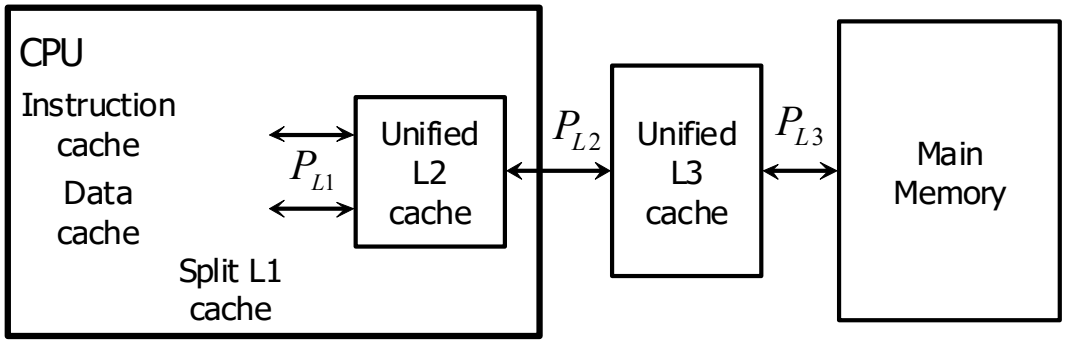
B. The following program runs on the CPUs:

PC		Instruction
0x4000	L1:	BEQZ R0, L2
		.
		.
		.
0x8000	L2:	BEQZ R0, L1

Explain the effect of the cache organization on the three types of cache miss: compulsory miss, capacity miss, conflict miss.

2. Consider a CPU with 3 levels of cache with the following characteristics:

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} , M^{D}_{L1}	P_{L1}
L2	Unified	M_{L2}	P_{L2}
L3	Unified	M_{L3}	P_{L3}



A. Generalize the expressions

$$CPI^{stall}_{1-level} = \left[M^{I}_{L1} + M^{D}_{L1} \times \frac{IC^{A}}{IC} \right] \times P_{L1}$$

$$CPI^{stall}_{2-level} = \left[M^{I}_{L1} + M^{D}_{L1} \times \frac{IC^{A}}{IC} \right] \times \left(P_{L1} + M_{L2} \times P_{L2} \right)$$

to find an expression for $CPI^{stall}_{3-level}$. (There is no need for a formal derivation or proof.) Explain briefly.

B. Find a numerical value for $CPI^{stall}_{3\text{-level}}$ using the expression from part A, using the following parameters.

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 10 %	P_{L1} = 2 cycles
L2	Unified	M_{L2} = 5 %	P_{L2} = 2 cycles
L3	Unified	M_{L3} = 1 %	P_{L3} = 50 cycles

$$\frac{IC^{A}}{IC} = 0.40$$

Compare this numerical result with $CPI^{stall}_{2-level}$ for the following characteristics:

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 10 %	P_{L1} = 2 cycles
L2	Unified	M_{L2} = 5 %	P_{L2} = 50 cycles