Hadassah Academic College

Department of Computer Science

Computer Architecture **Exercise 8**

Consider the following code fragment for the DLX CPU:

```
          LW R2, 1000(R0)
loop:     LW R4, 0(R2)
          SUBI R4, R4, #D0
          SW 0(R2), R4
          ADDI R2, R2, #4
          ADD R3, R2, R4
          BEQZ R3, loop
          AND R11, R8, R4
```

1. In its first iteration of the instruction **`BEQZ R3, loop`** the value in register **`R3`** is **`1234.`**
   Analyze the execution of the program for version 2 of the DLX, but completing the following tables:

   Format 1

	1	2	3	4	5	6	7
`LW R2, 1000(R0)`	IF	ID	EX	MEM	WB		
`LW R4, 0(R2)`		IF					

   Format 2

	IF	ID	EX	MEM	WB
1	`LW R2`				
2	`LW R4`	`LW R2`			
3	`SUBI`		`LW R2`		

2. Repeat the analysis in question 1 for version 6c of the DLX.
   In format 1, include arrows to indicate the forwarding of intermediate values between registers.