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Computer Architecture Exercise 10

1. Consider two CPUs with the following cache characteristics:

	CPU 1	CPU 2
Bytes per block	64	64
Cache type	Unified (data + instruction)	Unified (data + instruction)
Cache size	16 KB	16 KB
Associativity	2-way	1-way
Storage policy	write-through no-write-allocate	write-back write-allocate

A. For CPU 1 and CPU 2 find the set into which a byte at memory address **0x2000** will be copied in cache. In each cache a block is already in the destination set before the transfer of byte **0x2000** to cache. How will each CPU handle the transfer?

In a CPU where the bytes per block is 64 bit the number of bits in the block is 0x40

CPU 1: $\frac{16384}{64*2}$ = 0x80

CPU 2: $\frac{16384}{64}$ = 0X100

CPU 1: block = $\frac{0x2000}{0x40}$ = 0x80

Set = 0x80%0x100 = 0x80

The new block replaces the block in the first slot

B. The following program runs on the CPUs:

PC		Instruction
0x4000	L1:	BEQZ R0, L2
		.
		.
		.
0x8000	L2:	BEQZ R0, L1

Explain the effect of the cache organization on the three types of cache miss: compulsory miss, capacity miss, conflict miss.

CPU 1:

Block = $\frac{0x4000}{0x40}$ = 0x100 set = 0x100 % 0x80 = 0x20

Block = $\frac{0x8000}{0x40}$ = 0x200 set = 0x200 % 0x80 = 0x0

CPU 2:

Block = $\frac{0x4000}{0x40}$ = 0x100 set = 0x100 % 0x100 = 0x0

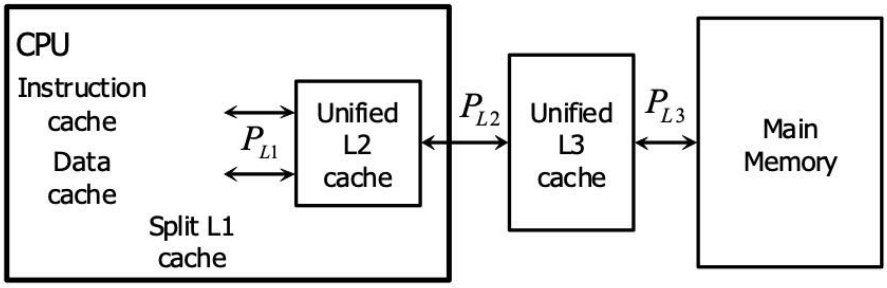
Block = $\frac{0x8000}{0x40}$ = 0x200 set = 0x200 % 0x100 = 0x0

In the first processor there is no problem of capacity - because each time the Set is different - and both commands are in the cache memory at the same time. There is a cache miss once while loading the commands.

In the second processor there is no problem of capacity, but there is only one command in the cache at any given time, so there will be memory errors when loading the data and at every round of the loop.

2. Consider a CPU with 3 levels of cache with the following characteristics:

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^I_{L1} , M^D_{L1}	P_{L1}
L2	Unified	M_{L2}	P_{L2}
L3	Unified	M_{L3}	P_{L3}



A. Generalize the expressions

$$CPI^{stall}_{1-level} = \left[M^I_{L1} + M^D_{L1} \times \frac{IC^A}{IC} \right] \times P_{L1}$$

$$CPI^{stall}_{2-level} = \left[M^I_{L1} + M^D_{L1} \times \frac{IC^A}{IC} \right] \times \left(P_{L1} + M_{L2} \times P_{L2} \right)$$

to find an expression for $CPI^{stall}_{3-level}$. (There is no need for a formal derivation or proof.)
Explain briefly.

$$CPI^{stall}_{3-level} = \left[M^I_{L1} + M^D_{L1} \times \frac{IC^A}{IC} \right] \times (P_{L1} + P_{L2} + M_{L2} + P_{L3} \times M_{L2} \times M_{L3})$$

ובצורה הסתברותית ניתן לכתוב את $CPI_{2-level}^{stall}$ כך:

$$CPI_{2-level}^{stall} = \left[M_{L1}^{1} + M_{L1}^{D} \times \frac{IC^{A}}{IC}\right] \times P_{L1} + \left[M_{L1}^{1} + M_{L1}^{D} \times \frac{IC^{A}}{IC}\right] \times M_{L2} \times P_{L2} =$$

$$P(L1\ miss) \times P_{L1} + P(L1\ miss) \times P(L2\ miss) \times P_{L2}$$

כעת, ניתן לכתוב את $CPI_{3-level}^{stall}$ בצורה הסתברותית כך:

$$CPI_{3-level}^{stall} = P(L1\ miss) \times P_{L1} + P(L1\ miss) \times P(L2\ miss) \times P_{L2} + P(L1\ miss) \times P(L2\ miss) \times P(L3\ miss) \times P_{L3}$$

B. Find a numerical value for $CPI^{stall}_{3\text{-level}}$ using the expression from part A, using the following parameters.

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 10 %	P_{L1} = 2 cycles
L2	Unified	M_{L2} = 5 %	P_{L2} = 2 cycles
L3	Unified	M_{L3} = 1 %	P_{L3} = 50 cycles

$$\frac{IC^{A}}{IC} = 0.40$$

$CPI_{L3}^{stall} = (0.01 + 0.1*0.4)*2 + (0.01 + 0.1*0.4)*0.05*2 + (0.01 + 0.1*0.4)*0.05*0.01*50 \approx 0.11$

Compare this numerical result with $CPI_{2-level}^{stall}$ for the following characteristics:

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 10 %	P_{L1} = 2 cycles
L2	Unified	M_{L2} = 5 %	P_{L2} = 50 cycles

$CPI_{L2}^{stall} = (0.01 + 0.1*0.4)*5 + (0.01 + 0.1*0.4)*0.05*50 \approx 0.38 > CPI_{L3}^{stall}$