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Computer Architecture **Exercise 5**

In the ISA of the 8086 CPU the distribution of assembly instruction in a certain program is:

Type i	IC_i/IC	CPI_i
ALU	50%	5
Branch	20%	12
Load	20%	10
Store	10%	10

Among the branch instructions, there are various operation types:

Jcc = {JL, JLE, LZ, JG, JGE, …}, JMP, CALL, LOOP

- In the table, 20% of instructions are branch, with an average CPI for all the branch types of $CPI_{branch} = 12$.
- We are also given that 10% of the instructions in the program are **LOOP** and that $CPI_{LOOP} = 14$.
- For this exercise we assume that the **JMP** and **CALL** instructions are not used.

A proposed improvement (called "instruction fusing") would work as follows:

- By adding hardware support, the LOOP instruction can be made to run with $CPI_{LOOP}' = 10$.
- A speedup is obtained by replacing code sections of the type

```
L1:   ...
      ...
      DEC CX          ; CX ← CX – 1       (ALU)
      CMP CX,0        ; compare CX == 0   (ALU)
      JG L1           ; loop if CX > 0    (Jcc – conditional branch)
```

with the code

```
L1:   ...
      ...
      LOOP L1
```

Assume that this replacement can be made for 50% of the cases that **Jcc** occurs in the code.

Find the total relative improvement in run time.