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Computer Architecture Exercise 9

Consider the following code fragment for the DLX CPU:

```
1            ADDI R2, R0, #8
2   loop:    LW R4, 0(R2)
3            ADDI R4, R4, #8
4            AND R4, R4, R3
5            SW 0(R2), R4
6            SUBI R2, R2, #4
7            BNEZ R2, loop
8            ADD R3, R3, R4
```

1. In each line, indicate if there is a stall in executing the instruction, the reason for the stall, and the number of clock cycles of the stall.

   Complete the analysis up to the second execution of the instruction in row 2.

1- No stall
2- No stall
3- There is a stall from LW to ALU. 1 clock cycle
4- No stall
5- No stall
6- No stall
7- There is a stall from ALU to BRANCH. 2 clock cycles
8- There is a stall from BRANCH. 1 clock cycle

2. Re-order the lines of the program to improve the run time. To make the code more efficient, you may change the values of literal (fixed) parameters in the instruction, if necessary. It is possible to remove all the stalls except for the control hazard for BNEZ.

   Explain the enhancement for each change.

1. ADDI R2, R0, #8
2. LW R4, 0(R2)
3. SUBI R2, R2, #4
4. ADDI R4, R4, #8
5. AND R4, R4, R3
6. SW 4(R2), R4
7. BNEZ R2, loop
8. ADD R3, R3, R4

Line 6 is under line 2. After the changes there are no stalls. Because of the changes the offset of the SW command had to be changed to 4.

3. A. Find CPI^{stall} for the execution in question 1.

$CPI^{stall} = 0.5 \times 14 \approx 7$

B. Find CPI^{stall} for the execution in question 2.

$CPI^{stall} = 0.07 \times 14 \approx 1$

C. Find the overall speedup for execution of the enhanced code relative to the original code.

$$1 + \text{CPI}^{\text{stall}} \times 1.5 = 1 + \text{CPI}'^{\text{stall}} = 1.07 \approx 1.4$$

4. Divide the original program into two threads by data decomposition.

Find the relative speedup relative to the original code.

	T0	T1
1	ADDI R2, R0, #4	ADDI R2, R0, #4
2	LOOP: LW R4, 4(RS)	LOOP: LW R4, 0(R2)
3	ADDI R4, R4, #8	ADDI R4, R4, #8
4	AND R4, R4, R3	AND R4, R4, R3
5	SW 4(R2), R4	SW 0(R2), R4
6	SUBI R2, R2, #4	SUBI R2, R2, #4
7	BNEZ R2, LOOP	BNEZ R2, LOOP
8	ADD R3, R3, R4	ADD R3, R3, R4

The loop has only one iteration.
There are 3 stalls clock cycles and 8 instructions.

$$\text{CC}_{\text{original}} = 7 \text{ stall cycles} + 4 \text{ init cycles} + 14 \text{ instructions} = 25 \text{ CC}$$

$$\text{CC}' = 3 \text{ stall cycles} + 4 \text{ init cycles} + 8 \text{ instructions} = 15 \text{ CC}$$

$$\text{S} = \frac{\text{CC}_{\text{original}}}{\text{CC}'} = \frac{25}{15} \approx 1.66$$