Joshua Andrew Rothe

Denver, CO

Active DoD Top Secret

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SUMMARY

Senior engineer at Lockheed Martin with a M.S. in Electrical Engineering from Johns Hopkins University. Specializes in FPGA firmware design with experience in electrical and mechanical hardware as well as software development. Proficient in Verilog, SystemVerilog, VHDL, and various simulation and software tools.

RECENT EXPERIENCE

Software Engineer Sr — **August 2023 – Present**
Lockheed Martin (Space/FBM) — *Denver, CO*

- Designed and simulated FPGA firmware using SystemVerilog and VHDL. Simulated using UVM and self-checking test benches. Wrote software test scripts and documentation as part of integration.
- Acted as lead for R&D efforts. Coordinated progress, schedule, and equipment cost with stakeholders and managers.
- Designed circuitry using Cadence OrCAD and simulated in PSPICE to verify functionality. Prototyped and tested circuits by both breadboarding and soldering components onto protoboards.
- Implemented a low-footprint Microk8s experiment (using Python) onto the LINUSS satellite to demonstrate functionality in a hardware-constrained environment. Automated deployment using YAML and bash scripts.
- Technical POC/Functional Owner of RTOS lab test environment, responsible for hardware and software configuration as well as cybersecurity (STIG) compliance. Acted as property coordinator for lab team.
- Lab hardware support, including wire harness design and hardware debugging/deployment.

Firmware Engineer 3 — **May 2022 – July 2023**
Kratos Space Federal (prev. Cosmic AES) — *Colorado Springs, CO*

- Developed FPGA firmware for Xilinx MPSoCs, tested with software (Python, C++) scripts on no-OS and PetaLinux builds. Debugged firmware using Vitis and JTAG connections as well as using software scripts on the board's processor (for MPSoCs).
- Implemented and tested C++/Python software and FPGA firmware on ICE FPGA cards using NeXT Midas.

Software Engineer — **November 2018 – Apr 2022**
Lockheed Martin (ADP/Skunkworks) — *Palmdale, CA*

- Wrote SystemVerilog FPGA code for Xilinx MPSoC FPGAs in avionics systems, and Tcl scripts for automation.
- Documented lab equipment assembly and generated drawings using Catia V5 and Solidworks.
- Managed lab hardware procurement and inventory, up to $1.2 mil annually. Dealt directly with vendors.
- Supported testbed operations (flight test, truck test) including building and troubleshooting test setups.

EDUCATION

Electrical Engineering, Master of Science — **Spring 2020 – Spring 2024**
Johns Hopkins University — *Baltimore, MD*
Degree focus – FPGAs/SoCs/Embedded Systems.

- MASTERS THESIS – Quantization and Pruning of Convolutional Neural Networks for Efficient FPGA Implementation of Digital Modulation Detection Firmware, doi: 10.13140/RG.2.2.12950.00324 . [link]

Electrical Engineering, Bachelor of Science — **Fall 2012 – Spring 2017**
California State University Northridge — *Northridge, CA*
Degree focus – Digital Electronics and Solid-State Devices.

PROJECTS

- **Embedded Systems Development Lab**: Designed a facial recognition lock system using OpenCV. [link]
- **FPGA SoC Lab**: Created software-defined radio on a Zynq-7000 SoC. [link]
- **Computer Architecture**: Added cache DDR2 memory to a pipelined MIPS processor on a Xilinx FPGA. [link]
- **Machine Learning for Signal Processing**: Developed algorithms to detect COVID-19 from x-ray images. [link]

PUBLICATIONS

- J. A. Rothe and H. Shajaiah, "Resource and Performance Improvements of Optimized Convolutional Neural Networks for FPGA Implementations of Automatic Modulation Recognition," 2025 59th Annual Conference on Information Sciences and Systems (CISS), Baltimore, MD, USA, 2025, pp. 1-6, doi: 10.1109/CISS64860.2025.10944746. [link] [IEEE Xplore]