Electronics SET 2

1. Which logic gate outputs 1 only when all inputs are 1?
   A) OR
   B) NAND
   C) AND
   D) XOR
   Answer: C) AND
   Explanation: AND outputs 1 only when every input is 1.

2. For a non-inverting op-amp with R1 = 10 kΩ between output and negative input and R2 = 2 kΩ between negative input and ground, the closed-loop gain is:
   A) 0.2
   B) 1.2
   C) 5
   D) 6
   Answer: D) 6
   Explanation: Gain = 1 + R1/R2 = 1 + 10k/2k = 1 + 5 = 6.

3. In a common-emitter amplifier, increasing emitter degeneration resistor improves:
   A) Voltage gain
   B) Thermal stability and linearity (reduces gain)
   C) Input capacitance
   D) Collector-emitter saturation voltage
   Answer: B) Thermal stability and linearity (reduces gain)
   Explanation: Emitter degeneration provides negative feedback, improving stability and linearity while lowering gain.

4. Which addressing mode uses the sum of a base register and offset to get the effective address?
   A) Immediate
   B) Direct
   C) Indexed (base+offset)
   D) Register
   Answer: C) Indexed (base+offset)

Explanation: Indexed/addressing with base + offset computes effective memory address dynamically.

5. When sampling a bandlimited signal of maximum frequency 20 kHz, the minimum sampling rate to avoid aliasing is:
   A) 10 kHz
   B) 20 kHz
   C) 40 kHz
   D) 80 kHz
   Answer: C) 40 kHz
   Explanation: Nyquist: sampling rate must be > 2 × f_max → >40 kHz.

6. Which component stores the conversion ratio in a digital potentiometer?
   A) Resistor ladder with switches
   B) Inductor bank
   C) Transformer
   D) Varactor diode
   Answer: A) Resistor ladder with switches
   Explanation: Digital pots use resistor ladders and electronic switches to provide discrete resistances.

7. In a buck converter operating in continuous conduction, if duty cycle D = 0.4 and input is 200 V, ideal output is:
   A) 80 V
   B) 200 V
   C) 120 V
   D) 50 V
   Answer: A) 80 V
   Explanation: Vo = D × Vin → 0.4 × 200 = 80 V.

8. Which flip-flop output can change asynchronously upon input change (without waiting clock edge)?
   A) Edge-triggered D flip-flop only
   B) Level-sensitive latch
   C) Master-slave flip-flop only
   D) Synchronous register only
   Answer: B) Level-sensitive latch
   Explanation: Latches are transparent when enable is active, allowing asynchronous changes relative to an external clock edge.

9. A low-pass RC filter with R = 1 kΩ and C = 0.1 µF has cutoff frequency approximately:
   A) 1.59 kHz
   B) 15.9 Hz
   C) 1592 Hz
   D) 159.2 Hz
   Answer: A) 1.59 kHz
   Explanation: fc = 1/(2πRC) = 1/(2π × 1000 × 0.1e-6) ≈ 1.59 kHz.

10. Which addressing method places I/O device registers in the same address space as memory?
   A) Isolated I/O
   B) Memory-mapped I/O
   C) DMA-only I/O
   D) Port-mapped with special opcodes
   Answer: B) Memory-mapped I/O
   Explanation: Memory-mapped assigns device registers into the CPU's memory address range.

11. In a PLL, the component that produces error voltage proportional to phase difference is:
   A) Voltage-controlled oscillator (VCO)
   B) Phase detector (or phase comparator)
   C) Frequency divider
   D) Low-pass capacitor
   Answer: B) Phase detector (or phase comparator)
   Explanation: Phase detector compares reference and feedback phases and outputs an error signal used to steer the VCO.

12. For a 4-bit DAC using binary-weighted resistors with MSB = 1, the output represents decimal 8 when:
   A) Only LSB = 1
   B) Only MSB = 1
   C) All bits = 1
   D) Bits 2 and 3 = 1
   Answer: B) Only MSB = 1
   Explanation: MSB of 4-bit binary equals decimal 8.

13. What is the primary reason to use hysteresis in comparator circuits?
   A) Increase gain

B) Reduce output drive capability
C) Prevent noise-induced oscillation at threshold
D) Lower power consumption
Answer: C) Prevent noise-induced oscillation at threshold
Explanation: Hysteresis gives two thresholds, preventing chatter on noisy signals.

14. A 16×2 character LCD's controller is typically driven over which interface in microcontroller applications?
A) SPI only
B) Parallel (4- or 8-bit) or I2C via backpack
C) PWM only
D) Ethernet
Answer: B) Parallel (4- or 8-bit) or I2C via backpack
Explanation: Character LCDs commonly use parallel data pins; I2C backpacks add serial convenience.

15. In a three-phase synchronous rectifier, using MOSFETs instead of diodes reduces:
A) Conduction loss (lower voltage drop)
B) Complexity without benefit
C) Switching loss to zero
D) Need for control signals
Answer: A) Conduction loss (lower voltage drop)
Explanation: MOSFETs in synchronous rectification exhibit much lower voltage drop when properly driven.

16. Which counter type requires feedback from multiple outputs to generate desired sequence (e.g., Johnson or LFSR)?
A) Binary ripple only
B) Linear feedback shift register (LFSR)
C) Up/down modulo counter only
D) Asynchronous decade counter only
Answer: B) Linear feedback shift register (LFSR)
Explanation: LFSRs use taps (feedback) to produce pseudo-random sequences.

17. For Ethernet using 1000BASE-T, what cabling type is required at minimum?
A) Cat-1 telephone cable
B) Cat-5e or better twisted pair

C) Coaxial RG-58
D) Fiber only
Answer: B) Cat-5e or better twisted pair
Explanation: Gigabit over copper requires Cat-5e or higher twisted-pair cabling.

18. In a BJT small-signal hybrid-π model, the input resistance at base is dominated by:
A) Collector-emitter resistance
B) r_π (base-emitter dynamic resistance)
C) r_o only
D) Inductance of wiring
Answer: B) r_π (base-emitter dynamic resistance)
Explanation: r_π models the small-signal base-emitter resistance affecting input.

19. A Reed-Solomon code is particularly effective for correcting:
A) Single-bit random errors
B) Burst errors (symbol-level errors)
C) Simple parity detection only
D) Thermal noise
Answer: B) Burst errors (symbol-level errors)
Explanation: RS codes operate on symbols (bytes), handling burst errors well.

20. Which ADC type uses a comparator and successive approximation register to converge on the digital value?
A) Flash ADC
B) Dual-slope ADC
C) Successive Approximation Register (SAR) ADC
D) Sigma-delta ADC
Answer: C) Successive Approximation Register (SAR) ADC
Explanation: SAR ADCs use binary search via comparator and DAC to approximate input.

21. In a three-phase induction motor, slip s = (synchronous speed − rotor speed)/synchronous speed. A slip near zero indicates:
A) Motor stalled
B) Rotor nearly synchronous speed (normal running)
C) Infinite torque
D) High rotor current always

Answer: B) Rotor nearly synchronous speed (normal running)
Explanation: Slip small under normal load; high slip implies heavy load or stall.

22. Which multiplexing method assigns fixed time slots to channels?
A) Frequency Division Multiplexing (FDM)
B) Time Division Multiplexing (TDM)
C) Code Division Multiplexing (CDM)
D) Space Division Multiplexing
Answer: B) Time Division Multiplexing (TDM)
Explanation: TDM divides time into slots allocated to channels.

23. In a CMOS inverter, static power dissipation ideally is:
A) High because both devices conduct DC always
B) Zero (neglecting leakage) because one device is off in steady states
C) Infinite at logic transitions
D) Dependent on input frequency only
Answer: B) Zero (neglecting leakage) because one device is off in steady states
Explanation: CMOS static current is negligible when input is stable; dynamic and leakage currents exist.

24. A 2-pole Butterworth low-pass filter has maximally flat response in the passband; its -3 dB cutoff occurs at:
A) $\omega = 0$
B) The designed cutoff frequency ω_c
C) Twice the designed cutoff frequency
D) Undefined
Answer: B) The designed cutoff frequency ω_c
Explanation: Butterworth -3 dB point defines cutoff; maximally flat inside passband.

25. In a UART, which framing element signals the start of a character?
A) Stop bit
B) Start bit (usually logic 0)
C) Parity bit
D) Baud rate only
Answer: B) Start bit (usually logic 0)
Explanation: Start bit alerts receiver to begin sampling bits at defined baud.

26. Which transmission medium is least affected by electromagnetic interference?
A) Twisted-pair copper
B) Coaxial cable
C) Optical fiber
D) Wireless RF
Answer: C) Optical fiber
Explanation: Optical fiber transmits light, immune to EMI and ground loops.

27. For a synchronous buck converter, the synchronous MOSFET replaces:
A) The inductor entirely
B) The diode (freewheeling) with actively controlled MOSFET for reduced loss
C) The input filter
D) The PWM controller
Answer: B) The diode (freewheeling) with actively controlled MOSFET for reduced loss
Explanation: Synchronous rectification reduces conduction losses by using MOSFET instead of diode.

28. A Karnaugh map grouping of 8 adjacent ones corresponds to simplifying expression by:
A) Reducing three variables
B) Reducing zero variables
C) Reducing four variables
D) Doubling terms
Answer: A) Reducing three variables
Explanation: Group of 8 eliminates three variables in a minimized product term (2^3 = 8).

29. Which phenomenon causes a MOSFET to turn on inadvertently when drain voltage changes rapidly?
A) Thermal runaway
B) Miller effect (gate-drain capacitance dV/dt coupling)
C) Avalanche breakdown only
D) Body diode conduction only
Answer: B) Miller effect (gate-drain capacitance dV/dt coupling)
Explanation: Rapid dV/dt couples through Cgd, potentially charging gate to threshold (false turn-on).

30. A two-tone test in RF amplifier characterization checks for:
A) DC load line only
B) Intermodulation distortion by injecting two close frequencies and observing spurs
C) Thermal stability only
D) Antenna impedance matching only
Answer: B) Intermodulation distortion by injecting two close frequencies and observing spurs
Explanation: Two-tone reveals nonlinear mixing products and amplifier linearity.

31. Which register in many microcontrollers stores the address used for stack operations?
A) Program Counter
B) Stack Pointer
C) Status Register
D) Instruction Register
Answer: B) Stack Pointer
Explanation: Stack pointer points to top of stack for push/pop operations.

32. In a PID controller, derivative action primarily:
A) Eliminates steady-state error
B) Predicts error trend and damps oscillations by responding to rate of change
C) Multiplies error by constant only
D) Has no effect on transient behavior
Answer: B) Predicts error trend and damps oscillations by responding to rate of change
Explanation: Derivative term responds to error slope mitigating overshoot.

33. A transmission line terminated in its characteristic impedance exhibits:
A) Full reflection of waves
B) No reflection (matched), maximum power transfer to load
C) Infinite standing waves
D) Reverse power only
Answer: B) No reflection (matched), maximum power transfer to load
Explanation: Proper termination absorbs incident wave, preventing reflection.

34. In a microcontroller, brown-out detection protects against:
A) Overtemperature only
B) Low supply voltage causing unpredictable operation by resetting MCU if Vcc

falls below threshold
C) Excessive clock rate
D) Watchdog timeouts
Answer: B) Low supply voltage causing unpredictable operation by resetting MCU if Vcc falls below threshold
Explanation: Brown-out detect resets MCU during undervoltage conditions to prevent corruption.

35. A power MOSFET's R_DS(on) largely affects:
A) Switching speed only
B) Conduction losses during on-state (I^2 × R_DS(on))
C) Gate threshold only
D) Maximum switching frequency only
Answer: B) Conduction losses during on-state (I^2 × R_DS(on))
Explanation: Lower R_DS(on) reduces conduction loss and heatsinking needs.

36. In a half-controlled converter with an R-L load, continuous conduction depends on:
A) Firing angle only
B) Load inductance and firing angle (sufficient inductance keeps current continuous)
C) Source frequency only
D) Number of diodes only
Answer: B) Load inductance and firing angle (sufficient inductance keeps current continuous)
Explanation: Inductance smooths current between conduction intervals to maintain continuous conduction.

37. Which addressing technique provides most flexibility for variable-length instructions?
A) Fixed-length only
B) Use of prefix or escape bytes and explicit length fields (variable-length instruction encoding)
C) Memory-mapped only
D) Direct only
Answer: B) Use of prefix or escape bytes and explicit length fields (variable-length instruction encoding)
Explanation: Variable-length encodings allow rich instruction sets and operand sizes.

38. A sigma-delta ADC achieves high resolution primarily by:
A) Very fast SAR conversion only
B) Oversampling and noise shaping followed by digital filtering and decimation
C) Using many comparators like flash ADC
D) Increasing reference voltage only
Answer: B) Oversampling and noise shaping followed by digital filtering and decimation
Explanation: Sigma-delta trades bandwidth for resolution using oversampling and shaping quantization noise.

39. Which transistor operation region is used in analog linear amplification?
A) Cutoff only
B) Saturation in MOSFET terms or forward-active in BJT (region of controlled conduction)
C) Breakdown only
D) Avalanche only
Answer: B) Saturation in MOSFET terms or forward-active in BJT (region of controlled conduction)
Explanation: MOSFET saturation (constant-current) and BJT forward-active used for linear amplification.

40. Which technique reduces EMI from a switching converter?
A) Slowing edges (controlled dv/dt) and adding snubbers, EMI filters, and good PCB layout
B) Increasing switching frequency only
C) Removing ground plane entirely
D) Using longer trace lengths
Answer: A) Slowing edges (controlled dv/dt) and adding snubbers, EMI filters, and good PCB layout
Explanation: Edge control, filters, and layout mitigations reduce radiated/emitted noise.

41. A load line analysis helps determine:
A) Time constant only
B) Q-point (operating point) of nonlinear device given supply and load constraints
C) Fourier coefficients
D) Bit error rate

Answer: B) Q-point (operating point) of nonlinear device given supply and load constraints
Explanation: Intersection of I–V device curve and circuit load line yields operating point.

42. Convolution in time domain corresponds to what operation in frequency domain?
A) Convolution also
B) Multiplication of spectra
C) Addition only
D) Differentiation only
Answer: B) Multiplication of spectra
Explanation: Time-domain convolution ↔ frequency-domain multiplication (and vice versa).

43. In a bootstrap gate driver for high-side MOSFET, the bootstrap capacitor provides:
A) Continuous DC supply for gate indefinitely without switching
B) A temporary charge to drive gate above source during each switching cycle, requires periodic refresh
C) Power to the load directly
D) Gate-to-drain capacitance reduction
Answer: B) A temporary charge to drive gate above source during each switching cycle, requires periodic refresh
Explanation: Bootstrap cap must be recharged when low-side conducts; not suitable for 100% duty high-side.

44. A Gray code sequence is useful because adjacent values differ by:
A) Many bits
B) Only one bit (minimizes glitching in transitions)
C) Exactly two bits always
D) No bits
Answer: B) Only one bit (minimizes glitching in transitions)
Explanation: Gray code ensures single-bit transitions aiding analog-to-digital position encoders.

45. For reliable high-speed serial links, pre-emphasis or equalization combats:
A) Thermal noise only
B) Channel loss and inter-symbol interference by boosting high-frequency components or recovering signal shape

C) DC offset only
D) Clock jitter only
Answer: B) Channel loss and inter-symbol interference by boosting high-frequency components or recovering signal shape
Explanation: Pre-emphasis compensates for channel attenuation at higher frequencies.

46. A comparator with open-drain output requires:
A) External pull-up resistor for proper logic high level
B) No additional components ever
C) A large bypass capacitor only
D) A current-limited diode only
Answer: A) External pull-up resistor for proper logic high level
Explanation: Open-drain can only pull low; pull-up required to present high state.

47. In an LC tank circuit used in oscillators, quality factor Q relates to:
A) Bandwidth and energy storage; higher Q => narrower bandwidth and lower damping
B) Only to DC current
C) Gate capacitance only
D) Bit error rate
Answer: A) Bandwidth and energy storage; higher Q => narrower bandwidth and lower damping
Explanation: Q=ω0L/R or 1/(ω0RC) indicates how underdamped/resonant the circuit is.

48. Which digital multiplier architecture uses partial product accumulation in an array with carry-save adders?
A) Serial shift-and-add only
B) Wallace tree or array multipliers (parallel partial-product addition)
C) Booth algorithm only
D) Direct memory mapping
Answer: B) Wallace tree or array multipliers (parallel partial-product addition)
Explanation: Wallace tree reduces addition stages via carry-save adders for fast multiplication.

49. For an op-amp integrator, output is proportional to:
A) Derivative of input
B) Integral of input over time (with -1/RC factor for inverting integrator)

C) Unchanged input
D) Square of input
Answer: B) Integral of input over time (with -1/RC factor for inverting integrator)
Explanation: Integrator accumulates input producing time integral at output.

50. A Hall-effect sensor primarily measures:
A) Electric field only
B) Magnetic field (or magnetic flux density) producing voltage proportional to current in conductor
C) Pressure only
D) Optical intensity only
Answer: B) Magnetic field (or magnetic flux density) producing voltage proportional to current in conductor
Explanation: Hall sensor outputs voltage proportional to perpendicular magnetic field.

51. In digital communication, bit stuffing is used to:
A) Scramble data only
B) Prevent occurrence of reserved bit patterns (e.g., frame delimiter) by inserting bits and enabling transparency
C) Encrypt bits
D) Convert serial to parallel
Answer: B) Prevent occurrence of reserved bit patterns (e.g., frame delimiter) by inserting bits and enabling transparency
Explanation: Bit stuffing ensures frame markers are unique by adding extra bits when needed.

52. A programmable logic device (PLD) differs from a microcontroller because:
A) PLD is purely analog always
B) PLD provides hardware-level parallel configurable logic, often lower-latency and application-specific, whereas microcontrollers run sequential software
C) Microcontrollers have reconfigurable logic only
D) Both are identical in function always
Answer: B) PLD provides hardware-level parallel configurable logic, often lower-latency and application-specific, whereas microcontrollers run sequential software
Explanation: PLDs (FPGAs, CPLDs) implement parallel hardware logic; MCUs run serial code on CPU.

53. In differential signaling, advantages compared to single-ended include:
A) Higher susceptibility to common-mode noise
B) Better noise immunity and lower EMI as differential receivers reject common-mode interference
C) No need for twisted pair cables
D) Higher DC power consumption always
Answer: B) Better noise immunity and lower EMI as differential receivers reject common-mode interference
Explanation: Differential pairs improve SNR and reduce radiated emissions.

54. For a first-order RC low-pass, step response reaches ~63% of final value at time:
A) t = 0
B) t = RC (time constant τ)
C) t = 10RC always
D) t = 1/RC
Answer: B) t = RC (time constant τ)
Explanation: First-order system reaches 1−e^−1 ≈ 0.632 of final at t=τ.

55. When designing PCB for high-speed signals, return path discontinuities cause:
A) Improved signal integrity
B) Increased EMI and signal integrity issues due to loop inductance and impedance discontinuities
C) No effect at all
D) Lower power consumption
Answer: B) Increased EMI and signal integrity issues due to loop inductance and impedance discontinuities
Explanation: Continuous return plane avoids large loop areas and maintains controlled impedance.

56. A phase margin of an amplifier is defined as:
A) The change in DC offset over time
B) The additional phase lag at unity loop gain before reaching −180°, indicating stability margin
C) Input capacitance only
D) Output resistance only
Answer: B) The additional phase lag at unity loop gain before reaching −180°, indicating stability margin

Explanation: Phase margin quantifies proximity to oscillation; larger is more stable.

57. In UART serial comms, parity bit provides:
A) Error correction for multiple bits
B) Simple error detection for odd/even number of bit flips (single-bit detection capability limited)
C) Increased baud rate
D) Framing synchronization always
Answer: B) Simple error detection for odd/even number of bit flips (single-bit detection capability limited)
Explanation: Parity detects single-bit errors (odd/even); cannot correct or detect many error types.

58. What is the main benefit of using a synchronous counter over an asynchronous counter?
A) Simpler logic always
B) No propagation delay accumulation; all flip-flops triggered simultaneously reducing timing issues
C) Requires no clock
D) Unlimited speed without constraints
Answer: B) No propagation delay accumulation; all flip-flops triggered simultaneously reducing timing issues
Explanation: Synchronous counters avoid ripple delays present in asynchronous designs.

59. For a given RF amplifier, noise figure represents:
A) Gain in dB only
B) Degradation of signal-to-noise ratio introduced by the amplifier; lower is better
C) Power supply rejection only
D) Bandwidth only
Answer: B) Degradation of signal-to-noise ratio introduced by the amplifier; lower is better
Explanation: Noise figure quantifies how much SNR is worsened by a device.

60. In a digital PLL for clock recovery, VCO jitter is reduced when:
A) Loop bandwidth is very wide without concern
B) Proper loop filter design balances tracking of low-frequency wander vs filtering high-frequency noise

C) No reference present
D) Phase detector disconnected
Answer: B) Proper loop filter design balances tracking of low-frequency wander vs filtering high-frequency noise
Explanation: Loop bandwidth selection trades jitter transfer from reference vs VCO noise.

61. A power supply with 12 V DC and a load drawing 2 A requires what minimum wattage rating for the supply?
A) 6 W
B) 12 W
C) 24 W
D) 120 W
Answer: C) 24 W
Explanation: Power = V × I = 12 × 2 = 24 watts.

62. In oversampled ADCs, decimation reduces sample rate and:
A) Increases quantization noise in passband
B) Reduces data rate and increases effective resolution after filtering
C) Removes need for anti-alias filter always
D) Increases analog front-end complexity only
Answer: B) Reduces data rate and increases effective resolution after filtering
Explanation: Oversample + digital filtering then decimation increases SNR/resolution.

63. In a full-bridge inverter feeding a purely resistive load with sinusoidal PWM, THD of output depends on:
A) Input DC voltage only
B) PWM modulation index and switching scheme (higher switching frequency and proper modulation reduce THD)
C) Only load impedance
D) None of the above
Answer: B) PWM modulation index and switching scheme (higher switching frequency and proper modulation reduce THD)
Explanation: THD influenced by PWM switching frequency and modulation depth.

64. Which error results from timing uncertainty in sampling instant relative to ideal sample time?
A) Quantization error

B) Aperture jitter (sampling clock jitter) causing sampling time error and resulting amplitude error, especially at high input frequency
C) Thermal error only
D) Aliasing only
Answer: B) Aperture jitter (sampling clock jitter) causing sampling time error and resulting amplitude error, especially at high input frequency
Explanation: Jitter in sampling causes voltage error proportional to slope of input.

65. In a differential amplifier, common-mode gain ideally should be:
A) Very high
B) Zero (or as low as possible) to reject common-mode signals
C) Equal to differential gain
D) Infinite
Answer: B) Zero (or as low as possible) to reject common-mode signals
Explanation: Small common-mode gain improves rejection of noise and interference present on both inputs.

66. For a toner pile-up (stack) in algorithmic CPU tasks, LIFO stands for:
A) Lost In First Out
B) Last In First Out (stack behavior)
C) Linear In First Out
D) Large In Fast Out
Answer: B) Last In First Out (stack behavior)
Explanation: Stack operations push/pop follow LIFO discipline.

67. In a current-mode controlled DC-DC converter, the control loop senses:
A) Output voltage only
B) Inductor current (or switch current) to regulate by controlling peak current or average current, improving dynamic response
C) Temperature only
D) MOSFET gate charge only
Answer: B) Inductor current (or switch current) to regulate by controlling peak current or average current, improving dynamic response
Explanation: Current-mode uses current feedback for inner loop control.

68. For error detection, CRC polynomial selection affects:
A) Processor speed only
B) Types of errors detectable (burst-length detection capacity based on polynomial degree)

C) Power factor only
D) Capacitor sizing only
Answer: B) Types of errors detectable (burst-length detection capacity based on polynomial degree)
Explanation: CRC generator polynomial degree determines max burst length detected reliably.

69. A breakout board for an embedded sensor often provides:
A) Only complex power management without pins
B) Convenient pins, level shifting, and decoupling to integrate sensor to breadboard or MCU more easily
C) Only software drivers; no hardware
D) High-voltage AC conversion only
Answer: B) Convenient pins, level shifting, and decoupling to integrate sensor to breadboard or MCU more easily
Explanation: Breakouts expose small SMD devices on user-friendly headers and often include necessary support components.

70. A phase-locked loop used as frequency synthesizer uses a frequency divider in the feedback to:
A) Increase noise only
B) Allow VCO frequency to be a multiple (N×) of reference, enabling programmable frequencies (divide-by-N)
C) Remove need for VCO
D) Convert analog signal to digital only
Answer: B) Allow VCO frequency to be a multiple (N×) of reference, enabling programmable frequencies (divide-by-N)
Explanation: Feedback division multiplies reference up to VCO frequency by N.

71. Which leakage mechanism grows dramatically as oxide thickness scales down in MOS devices?
A) Thermal conduction only
B) Gate oxide tunneling (direct tunneling / Fowler–Nordheim)
C) Inductance only
D) Mechanical wear
Answer: B) Gate oxide tunneling (direct tunneling / Fowler–Nordheim)
Explanation: Thinner oxides increase tunneling leakage currents across gate oxide.

72. A current transformer (CT) is used for:
A) Voltage measurement only
B) Isolated measurement of AC currents (especially high currents) scaling them down for meters/protection relays
C) Measuring DC currents accurately
D) Replacing power transformers always
Answer: B) Isolated measurement of AC currents (especially high currents) scaling them down for meters/protection relays
Explanation: CTs operate for AC and provide proportional isolated current.

73. In ladder logic programming, a rung that holds an output even after the actuating input drops is called:
A) A toggle only
B) Latching or seal-in circuit (self-hold using output contact in parallel with input)
C) Momentary circuit only
D) None of the above
Answer: B) Latching or seal-in circuit (self-hold using output contact in parallel with input)
Explanation: Seal-in uses a contact of the output to maintain coil energization.

74. A transient voltage suppressor (TVS) diode is typically used to:
A) Regulate battery voltage always
B) Clamp voltage spikes and protect sensitive circuits from transient overvoltage events
C) Provide long-term voltage smoothing like a regulator
D) Replace series resistors in filters
Answer: B) Clamp voltage spikes and protect sensitive circuits from transient overvoltage events
Explanation: TVS devices react fast to clamp transients like ESD or load-dump pulses.

75. The primary purpose of bit-interleaving in memory systems is to:
A) Increase single-bit error probability
B) Spread bits of a word across multiple memory banks to improve error tolerance or parallel access performance
C) Slow down access intentionally
D) Limit memory to single bank operation

Answer: B) Spread bits of a word across multiple memory banks to improve error tolerance or parallel access performance
Explanation: Interleaving benefits parallelism and can help error correction schemes.

76. In analog filter design, Chebyshev Type I filters trade:
A) Increased passband ripple for a steeper roll-off compared to Butterworth at same order
B) No benefits at all
C) Larger physical size always
D) Reduced selectivity only
Answer: A) Increased passband ripple for a steeper roll-off compared to Butterworth at same order
Explanation: Chebyshev offers steeper transition with passband ripple.

77. In servo motor control, back EMF is proportional to:
A) Motor winding resistance only
B) Rotor speed (and motor constant), used for sensorless speed estimation sometimes
C) Supply voltage only
D) Torque only
Answer: B) Rotor speed (and motor constant), used for sensorless speed estimation sometimes
Explanation: Back EMF is $k_e \times \omega$ and opposes applied voltage.

78. Which coding technique improves DC balance and provides transition density for clock recovery?
A) NRZ-L only
B) Manchester encoding (or 8b/10b) which ensures frequent transitions and DC balance
C) Unencoded TTL only
D) ASCII only
Answer: B) Manchester encoding (or 8b/10b) which ensures frequent transitions and DC balance
Explanation: These encodings embed clock transitions and balance ones/zeros.

79. A 10-bit ADC with full-scale range 0–5 V has LSB size of:
A) 5/1024 ≈ 4.8828 mV
B) 5/1000 = 5 mV exactly

C) 5/512 ≈ 9.77 mV
D) 5/2048 ≈ 2.44 mV
Answer: A) 5/1024 ≈ 4.8828 mV
Explanation: Resolution = Vfs / 2^N = 5 / 1024 ≈ 4.8828 mV per LSB.

80. A synchronous serial protocol where master provides clock and data lines and devices use chip-select is typically:
A) I²C
B) SPI
C) UART
D) USB
Answer: B) SPI
Explanation: SPI uses separate SS/CS lines, SCLK, MOSI, MISO; master-driven clock.

81. In an N-channel enhancement MOSFET, threshold voltage Vth is the gate voltage at which:
A) Device reaches endless conduction only
B) A conductive channel just forms between source and drain under specified test conditions
C) Device permanently damaged always
D) Gate oxide breaks down
Answer: B) A conductive channel just forms between source and drain under specified test conditions
Explanation: Vth defines minimal Vgs to start channel inversion under reference specs.

82. In a synchronous buck converter, inductor current ripple decreases if:
A) Switching frequency increases or inductance increases
B) Output voltage increases always
C) Input is AC only
D) MOSFET Rds(on) increases
Answer: A) Switching frequency increases or inductance increases
Explanation: $\Delta I_L \propto (V_L / L) \times D/f_s$; increasing L or f_s reduces ripple.

83. Which method helps prevent latch-up in CMOS ICs?
A) Using high supply voltage only
B) Guard rings, substrate ties, proper layout, limiting injection of parasitic currents
C) Removing ESD protection always

D) Thinning oxide always

Answer: B) Guard rings, substrate ties, proper layout, limiting injection of parasitic currents

Explanation: Layout and process techniques mitigate parasitic thyristor activation causing latch-up.

84. A three-state output buffer allows:

A) Only two logic states always

B) An additional high-impedance (Z) state to let multiple outputs share a bus without contention

C) Infinite voltage levels

D) Analog output only

Answer: B) An additional high-impedance (Z) state to let multiple outputs share a bus without contention

Explanation: Tri-state buffers can disconnect output driver leaving bus free.

85. In radio systems, diversity reception combats fading by:

A) Using a single antenna only

B) Using multiple antennas, frequencies, or time diversity and combining to reduce deep fades effect

C) Increasing modulation index only

D) Reducing bandwidth only

Answer: B) Using multiple antennas, frequencies, or time diversity and combining to reduce deep fades effect

Explanation: Diversity exploits independent fading paths to improve link reliability.

86. A CRC with polynomial degree k can detect all burst errors of length ≤ k:

A) True

B) False — it can detect burst errors of length ≤ k reliably (true)

C) Only random errors

D) None of the above

Answer: A) True

Explanation: A CRC of degree k detects any burst error of length ≤ k.

87. Which is true about thermal resistance θ_JA of a package?

A) Lower θ_JA means worse heat dissipation

B) Lower θ_JA means better thermal conduction to ambient (lower temperature rise for given power)

C) Thermal resistance irrelevant for power devices

D) Measured in volts

Answer: B) Lower θ_JA means better thermal conduction to ambient (lower temperature rise for given power)

Explanation: θ_JA = ΔT / P; smaller value yields less temperature rise per watt.

88. In PLL frequency acquisition, analog capture range depends on:

A) Only the VCO tuning range and loop filter dynamics affecting how far input frequency can be pulled into lock

B) Only ADC resolution

C) Only supply voltage

D) None of the above

Answer: A) Only the VCO tuning range and loop filter dynamics affecting how far input frequency can be pulled into lock

Explanation: Capture depends on VCO range and loop bandwidth/ damping.

89. A power stage uses snubbers mainly to control:

A) Switching transient voltages and dv/dt to protect semiconductor devices and reduce EMI

B) Increase switching speed without side effects

C) Voltage regulation precision only

D) Increase current indefinitely

Answer: A) Switching transient voltages and dv/dt to protect semiconductor devices and reduce EMI

Explanation: Snubbers absorb transient energy and limit overshoot.

90. In a multi-layer PCB, stitching vias in ground plane help:

A) Increase loop inductance

B) Provide low-impedance return paths, reduce EMI and improve grounding continuity

C) Block thermal conduction only

D) Act as resistors deliberately

Answer: B) Provide low-impedance return paths, reduce EMI and improve grounding continuity

Explanation: Stitching maintains ground integrity, especially around splits or near connectors.

91. Which modulation yields constant envelope, making it robust to nonlinear amplification?

A) QAM (higher-order)

B) FM or FSK (frequency/phase modulations) produce near-constant envelope
C) ASK only
D) PCM only
Answer: B) FM or FSK (frequency/phase modulations) produce near-constant envelope
Explanation: Constant-envelope schemes allow non-linear power-efficient amplification.

92. A wideband op-amp with gain-bandwidth product (GBW) of 10 MHz when used in closed-loop gain of 10 will have approximate bandwidth:
A) 100 MHz
B) 10 MHz
C) 1 MHz
D) 0.1 MHz
Answer: C) 1 MHz
Explanation: Closed-loop bandwidth ≈ GBW / closed-loop gain → 10 MHz / 10 = 1 MHz.

93. For fault isolation in large networks, which technique reduces broadcast domain size?
A) Using hubs only
B) Creating VLANs to logically separate broadcast domains within switches
C) Using longer cables only
D) Disabling STP always
Answer: B) Creating VLANs to logically separate broadcast domains within switches
Explanation: VLANs isolate broadcast traffic across logical segments.

94. A microcontroller ADC sampling a slowly changing signal benefits from:
A) Highest possible sampling rate always
B) Lower sampling rates and averaging to reduce noise; appropriate anti-alias filtering
C) No decoupling capacitors anywhere
D) Disabling reference
Answer: B) Lower sampling rates and averaging to reduce noise; appropriate anti-alias filtering
Explanation: Averaging and filtering improve effective resolution for low-dynamic signals.

95. A half-wave rectifier with capacitor input filter charges capacitor to peak minus diode drop and supplies load; ripple approximates:
A) ΔV ≈ I_load / (f_ripple × C) where f_ripple is pulse frequency (for half-wave equal to line freq)
B) No ripple at all always
C) Infinite ripple always
D) Not computable
Answer: A) ΔV ≈ I_load / (f_ripple × C) where f_ripple is pulse frequency (for half-wave equal to line freq)
Explanation: Approximate ripple formula from capacitor discharge between peaks.

96. In cache memory, write-back policy:
A) Writes data to main memory on every write hit
B) Updates main memory only on eviction, reducing write traffic but requires coherency mechanisms
C) Disables cache on writes
D) Increases write latency always
Answer: B) Updates main memory only on eviction, reducing write traffic but requires coherency mechanisms
Explanation: Write-back stores updates in cache and writes to memory later.

97. A variable-frequency drive (VFD) controlling AC motor typically uses:
A) Direct AC only with no conversion
B) Rectifier + DC link + inverter (PWM) to synthesize variable frequency/voltage to motor
C) Purely mechanical gearbox only
D) RF transmitter only
Answer: B) Rectifier + DC link + inverter (PWM) to synthesize variable frequency/voltage to motor
Explanation: VFD topology commonly uses AC→DC→PWM AC.

98. When designing mixed-signal PCBs, separating analog and digital ground with a single-point connection helps:
A) Increase ground loops always
B) Control return currents and minimize noise coupling if done correctly at star point or through low-impedance connection near power entry
C) Eliminate the need for decoupling caps
D) Ensure infinite isolation always

Answer: B) Control return currents and minimize noise coupling if done correctly at star point or through low-impedance connection near power entry
Explanation: Careful grounding minimizes digital noise injected into sensitive analog circuits.

99. A ring oscillator's frequency is primarily determined by:
A) Number of inverting stages and propagation delay per stage ($f \approx 1/(2N\tau)$)
B) Supply voltage only
C) Temperature only
D) Wire color only
Answer: A) Number of inverting stages and propagation delay per stage ($f \approx 1/(2N\tau)$)
Explanation: Odd number of inverters produce oscillation with period from stage delays.

100. How many usable host addresses exist in a /25 IPv4 subnet?
A) 128 usable hosts
B) 126 usable hosts
C) 254 usable hosts
D) 2 usable hosts
Answer: B) 126 usable hosts
Explanation: /25 has 2^(32-25) = 128 total addresses; usable hosts = 128 − 2 (network + broadcast) = 126.
