OLEKSII ZOLOTAREVSKYI

Analog Design Engineer

alexey.zolotarevskiy@gmail.com | +49 1522 107 40 27 | Gleiwitzer Str. 37, Erlangen, 91058, Germany
Erlangen, Germany | roundoutandabout.github.io | linkedin.com/in/oleksii-zolotarevskyi
github.com/roundoutandabout | facebook.com/iriderua

EXPERIENCE

Overall 6 years of experience in Analog Design.

Analog Design Engineer

eesy-ic GmbH

Feb 2019 – Jun 2023 | Erlangen, Germany

4 years of experience with main focus in analog design, layout support, design and simulation of analog top level, full chip simulation in Bulk and SOI technologies.

Designing of analog building blocks for RF Switches, LNAs, PAs:

- Charge pumps, LDOs, Analog DfT
- LNA Biasing
- Current references, Current DACs
- Power supply detectors/Power good detectors
- Level shifters, IO Pads
- Designing and verifying the analog building blocks for consumer LNA and Antenna Tuner products

Other activities:

- Fully differential amplifiers
- Feedback amplifiers
- Voltage buffers

Trainee With Specialization in Analog Design

Melexis Ukraine

June 2016 – June 2018 | Kyiv, Ukraine

- As a trainee, studied the fundamentals of the semiconductor devices operation, analog integrated circuit design and IC fabrication technology.
- Acquired practical experience with Cadence Virtuoso and knowledge of design and simulation of the common analog circuits.
- Completed a Master's Thesis on developing a methodology for modelling the faults and evaluating the reliability of the integrated circuits.

EDUCATION

Master's Degree in Micro- and Nanosystem Technology

National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute"

Sept 2016 – May 2018

Thesis title: Failures simulation of integrated circuits

Bachelor's Degree in Micro- and Nanoelectronics

National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute"

Sept 2012 – June 2016

Thesis title: Microclimate measurement system with wireless interface

Graduate

Kherson Physical-Technical Lyceum

Sept 2009 – May 2012

MY LIFE PHILOSOPHY

"If you can't explain it simply, you don't understand it well enough."

MOST PROUD OF

Contributing to the TO of the LNA Bank product as analog design owner
Improved the LNA performance by optimizing the analog biasing circuit. Solved non trivial issues with operation of the analog circuits in a full chip.
eesy-ic GmbH

Succeeding in a role of analog design owner for a chip with high reliability requirements
Developed several analog blocks and was responsible for the analog part of the chip used in the industrial base stations with the increased lifetime and the supply voltage not supported by the given technology.
eesy-ic GmbH

Developing a methodology of fault injection
Participated in the project aimed at estimation of the fault tolerance of the IP block, used in a commercial IC.
Melexis Ukraine

SKILLS

Cadence Virtuoso | Virtuoso Layout XL | Tanner EDA Tools | VerilogA | Bash | MATLAB

STRENGTHS

Eye for detail | Cheerful | Perfectionistic | Hard-working

LANGUAGES

German ●●○○○

English ●●●●○

Russian ●●●●●