![Texas Instruments]

TXS0104E 4-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

1 Features

- No Direction-Control Signal Needed
- Max Data Rates
  - 24 Mbps (Push Pull)
  - 2 Mbps (Open Drain)
- Available in the Texas Instruments NanoFree™ Package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ($V_{CCA} \leq V_{CCB}$)
- No Power-Supply Sequencing Required – V_{CCA} or V_{CCB} Can Be Ramped First
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2000-V Human-Body Model (A114-B)
    - 200-V Machine Model (A115-A)
    - 1000-V Charged-Device Model (C101)
  - B Port
    - 15-kV Human-Body Model (A114-B)
    - 200-V Machine Model (A115-A)
    - 1000-V Charged-Device Model (C101)
- IEC 61000-4-2 ESD (B Port)
  - ±8-kV Contact Discharge
  - ±10-kV Air-Gap Discharge

2 Applications

- Handset
- Smartphone
- Tablet
- Desktop PC

3 Description

This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V. V_{CCA} must be less than or equal to V_{CCB}. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V. This allows for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

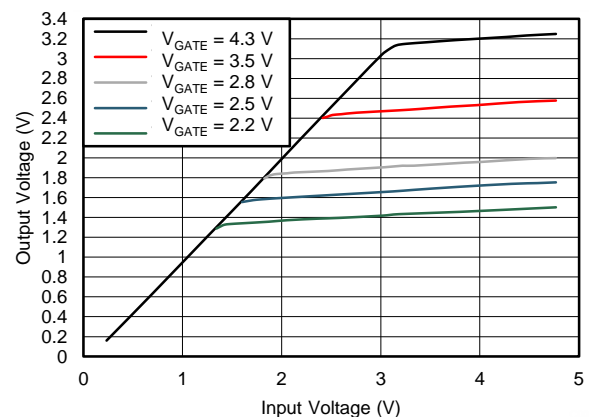The TXS0104E is designed so that the OE input circuit is supplied by V_{CCA}.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXS0104ED	SOIC (14)	8.65 mm × 3.91 mm
TXS0104EPW	TSSOP (14)	5.00 mm × 4.40 mm
TXS0104EZXU	BGA (12)	2.00 mm × 2.50 mm
TXS0104ERGY	VQFN (14)	3.50 mm × 3.50 mm
TXS0104EYZT	DSBGA (12)	1.87 mm × 1.37 mm

[1] For all available packages, see the orderable addendum at the end of the data sheet.

Transfer Characteristics of an N-Channel Transistor

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2008) to Revision E   **Page**

5 Pin Configuration and Functions

ZXU Package
12-Pin MICROSTAR JUNIOR
Top View
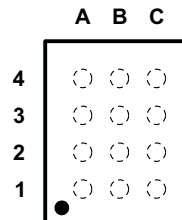
Pin Functions: BGA

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	A1	I/O	Input/output A1. Referenced to V_{CCA}.
A2	A2	I/O	Input/output A2. Referenced to V_{CCA}.
A3	A3	I/O	Input/output A3. Referenced to V_{CCA}.
A4	A4	I/O	Input/output A4. Referenced to V_{CCA}.
B1	C1	I/O	Input/output B1. Referenced to V_{CCB}.
B2	C2	I/O	Input/output B2. Referenced to V_{CCB}.
B3	C3	I/O	Input/output B3. Referenced to V_{CCB}.
B4	C4	I/O	Input/output B4. Referenced to V_{CCB}.
GND	B4	—	Ground
OE	B3	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	B2	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	B1	—	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V.

Product Folder Links: *TXS0104E*

YZT Package
12-Pin DSBGA
Top View
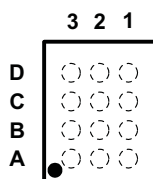
Pin Functions: DSBGA

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
A1	A3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	B3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	C3	I/O	Input/output A3. Referenced to V_{CCA}.
A4	D3	I/O	Input/output A4. Referenced to V_{CCA}.
B1	A1	I/O	Input/output B1. Referenced to V_{CCB}.
B2	B1	I/O	Input/output B2. Referenced to V_{CCB}.
B3	C1	I/O	Input/output B3. Referenced to V_{CCB}.
B4	D1	I/O	Input/output B4. Referenced to V_{CCB}.
GND	D2	—	Ground
OE	C2	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	B2	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	A2	—	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V.

**RGY Package
14-Pin VQFN
Top View**

NC - No internal connection

**D and PW Package
14-Pin SOIC and TSSOP
Top View**
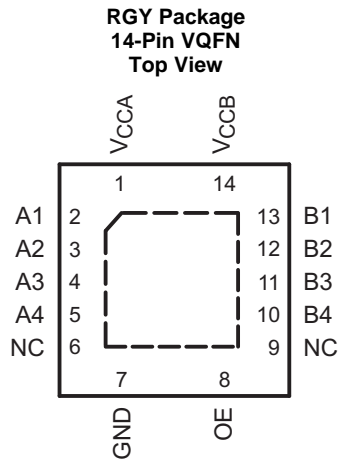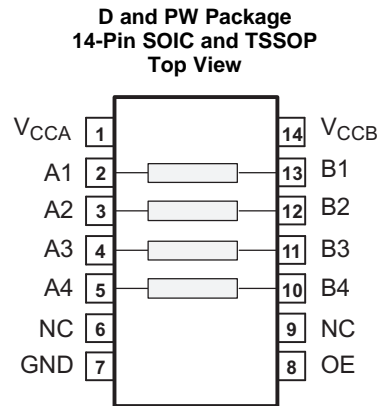
NC - No internal connection

Pin Functions: D, PW, or RGY

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	13	I/O	Input/output B1. Referenced to V_{CCB}.
B2	12	I/O	Input/output B2. Referenced to V_{CCB}.
B3	11	I/O	Input/output B3. Referenced to V_{CCB}.
B4	10	I/O	Input/output B4. Referenced to V_{CCB}.
GND	7	—	Ground
OE	8	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	—	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V.
Thermal Pad	—	—	For the RGY package, the exposed center thermal pad must be connected to ground

Product Folder Links: *TXS0104E*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		−0.5	4.6	V
Supply voltage, V_{CCB}		−0.5	6.5	V
Input voltage, V_I[2]	A port	−0.5	4.6	V
	B port	−0.5	6.5	
Voltage range applied to any output in the high-impedance or power-off state, V_O[2]	A port	−0.5	4.6	V
	B port	−0.5	6.5	
Voltage range applied to any output in the high or low state, V_O[2] [3]	A port	−0.5	V_{CCA} + 0.5	V
	B port	−0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK}	V_I < 0		−50	mA
Output clamp current, I_{OK}	V_O < 0		−50	mA
Continuous output current, I_O		−50	50	mA
Continuous current through each V_{CCA}, V_{CCB}, or GND		−100	100	mA
Operating junction temperature, T_J			150	°C
Storage temperature, T_{STG}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	A Port	±2000	V
			B Port	±15	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	A Port	±1000	V
			B Port	±1000	
		Machine model (MM)	A Port	±200	V
			B Port	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1] [2]

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage[3]				1.65	3.6	V
V_{CCB}	Supply voltage[3]				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	$V_{CCI} - 0.2$	V_{CCI}	V
			2.3 V to 3.6 V	2.3 V to 5.5 V	$V_{CCI} - 0.4$	V_{CCI}	
		B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	$V_{CCI} - 0.4$	V_{CCI}	
		OE input	1.65 V to 3.6 V	2.3 V to 5.5 V	$V_{CCA} \times 0.65$	5.5	
V_{IL}	Low-level input voltage	A-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	V
		B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	
		OE input	1.65 V to 3.6 V	2.3 V to 5.5 V	0	$V_{CCA} \times 0.35$	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port I/Os push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
		B-port I/Os push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	
		Control input	1.65 V to 3.6 V	2.3 V to 5.5 V		10	
T_A	Operating free-air temperature				−40	85	°C

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.4 Thermal Information: ZXU and YZT

		TXS0104E		
THERMAL METRIC[1]		ZXU (BGA MICROSTAR JUNIOR) [2]	YZT (DSBGA)	UNIT
		12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.0	89.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.4	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.7	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.2	14.4	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2)   The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Thermal Information: D, PW, and RGY

		TXS0104E			
THERMAL METRIC[1]		D (SOIC)[1]	PW (TSSOP)[2]	RGY (VQFN)[3]	UNIT
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.4	120.1	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.1	49.4	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.0	61.8	32.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.4	6.2	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.7	61.2	32.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	12.8	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2)   The package thermal impedance is calculated in accordance with JESD 51-7.
(3)   The package thermal impedance is calculated in accordance with JESD 51-5.

Product Folder Links: *TXS0104E*

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) [1] [2] [3]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}	Port A output high voltage	$I_{OH} = -20\ \mu A$, $V_{IB} \geq V_{CCB} - 0.4\ V$, $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	$V_{CCA} \times 0.8$			V
V_{OLA}	Port A output low voltage	$I_{OL} = 1\ mA$, $V_{IB} \leq 0.15\ V$, $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
V_{OHB}	Port B output high voltage	$I_{OH} = -20\ \mu A$, $V_{IA} \geq V_{CCA} - 0.2\ V$, $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	$V_{CCB} \times 0.8$			V
V_{OLB}	Port B output low voltage	$I_{OL} = 1\ mA$, $V_{IA} \leq 0.15\ V$, $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
I_I	Input leakage current	OE: $V_I = V_{CCI}$ or GND $T_A = 25°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	−1		1	μA
		$V_I = V_{CCI}$ or GND $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	−2		2	μA
I_{OZ}	High-impedance state output current	A or B port: $OE = V_{IL}$ $T_A = 25°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	−1		1	μA
		A or B port: $OE = V_{IL}$ $T_A = -40°C\ to\ 85°C$	1.65 V to 3.6 V	2.3 V to 5.5 V	−2		2	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_O = Open$, $I_O = 0$ $T_A = -40°C\ to\ 85°C$	1.65 V to V_{CCB}	2.3 V to 5.5 V			2.4	μA
			3.6 V	0			2.2	
			0	5.5 V			−1	
I_{CCB}	V_{CCB} supply current	$V_I = V_O = Open$, $I_O = 0$ $T_A = -40°C\ to\ 85°C$	1.65 V to V_{CCB}	2.3 V to 5.5 V			12	μA
			3.6 V	0			−1	
			0	5.5 V			1	
$I_{CCA} + I_{CCB}$	Combined supply current	$V_I = V_O = Open$, $I_O = 0$ $T_A = -40°C\ to\ 85°C$	1.65 V to V_{CCB}	2.3 V to 5.5 V			14.4	μA
C_I	Input capacitance	OE: $T_A = 25°C$	3.3 V	3.3 V		2.5		pF
		OE: $T_A = -40°C\ to\ 85°C$	3.3 V	3.3 V			3.5	
C_{io}	Input-to-output internal capacitance	A port: $T_A = 25°C$	3.3 V	3.3 V		5		pF
			3.3 V	3.3 V			6.5	
		B port: $T_A = -40°C\ to\ 85°C$	3.3 V	3.3 V		12		
			3.3 V	3.3 V			16.5	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

Product Folder Links: TXS0104E

6.7 Timing Requirements: V$_{CCA}$ = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V$_{CCA}$ = 1.8 V ± 0.15 V (unless otherwise noted)

				MIN	MAX	UNIT
Data rate	Push-pull driving		V$_{CCB}$ = 2.5 V ± 0.2 V V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V		24	Mbps
	Open-drain driving		V$_{CCB}$ = 2.5 V ± 0.2 V V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V		2	
t$_w$ Pulse duration	Push-pull driving	Data inputs	V$_{CCB}$ = 2.5 V ± 0.2 V V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V	41		ns
	Open-drain driving	Data inputs	V$_{CCB}$ = 2.5 V ± 0.2 V V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V	500		

6.8 Timing Requirements: V$_{CCA}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V$_{CCA}$ = 2.5 V ± 0.2 V (unless otherwise noted)

				MIN	MAX	UNIT
Data rate	Push-pull driving		V$_{CCB}$ = 2.5 V ± 0.2 V $_{CCB}$ = 3.3 V ± 0.3 V $_{CCB}$ = 5 V ± 0.5 V		24	Mbps
	Open-drain driving		V$_{CCB}$ = 2.5 V ± 0.2 V $_{CCB}$ = 3.3 V ± 0.3 V $_{CCB}$ = 5 V ± 0.5 V		2	
t$_w$ Pulse duration	Push-pull driving	Data inputs	V$_{CCB}$ = 2.5 V ± 0.2 V $_{CCB}$ = 3.3 V ± 0.3 V $_{CCB}$ = 5 V ± 0.5 V	41		ns
	Open-drain driving	Data inputs	V$_{CCB}$ = 2.5 V ± 0.2 V $_{CCB}$ = 3.3 V ± 0.3 V $_{CCB}$ = 5 V ± 0.5 V	500		

6.9 Timing Requirements: V$_{CCA}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V$_{CCA}$ = 3.3 V ± 0.3 V (unless otherwise noted)

				MIN	MAX	UNIT
Data rate	Push-pull driving		V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V		24	Mbps
	Open-drain driving		V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V		2	
t$_w$ Pulse duration	Push-pull driving	Data inputs	V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V	41		ns
	Open-drain driving	Data inputs	V$_{CCB}$ = 3.3 V ± 0.3 V V$_{CCB}$ = 5 V ± 0.5 V	500		

Product Folder Links: *TXS0104E*

6.10 Switching Characteristics: V$_{CCA}$ = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V$_{CCA}$ = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
t$_{PHL}$	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V		4.6	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V		4.7	
				V$_{CCB}$ = 5 V ± 0.5 V		5.8	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	2.9	8.8	
				V$_{CCB}$ = 3.3 V ± 0.3 V	2.9	9.6	
				V$_{CCB}$ = 5 V ± 0.5 V	3	10	
t$_{PLH}$	Propagation delay time (low-to-high output)		Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V		6.8	
				V$_{CCB}$ = 3.3 V ± 0.3 V		6.8	
				V$_{CCB}$ = 5 V ± 0.5 V		7	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	45	260	
				V$_{CCB}$ = 3.3 V ± 0.3 V	36	208	
				V$_{CCB}$ = 5 V ± 0.5 V	27	198	
t$_{PHL}$	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V		4.4	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V		4.5	
				V$_{CCB}$ = 5 V ± 0.5 V		4.7	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	1.9	5.3	
				V$_{CCB}$ = 3.3 V ± 0.3 V	1.1	4.4	
				V$_{CCB}$ = 5 V ± 0.5 V	1.2	4	
t$_{PLH}$	Propagation delay time (low-to-high output)		Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V		5.3	
				V$_{CCB}$ = 3.3 V ± 0.3 V		4.5	
				V$_{CCB}$ = 5 V ± 0.5 V		0.5	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	45	175	
				V$_{CCB}$ = 3.3 V ± 0.3 V	36	140	
				V$_{CCB}$ = 5 V ± 0.5 V	27	102	
t$_{en}$	Enable time	OE-to-A or B		V$_{CCB}$ = 2.5 V ± 0.2 V		200	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V		200	
				V$_{CCB}$ = 5 V ± 0.5 V		200	
t$_{dis}$	Disable time	OE-to-A or B		V$_{CCB}$ = 2.5 V ± 0.2 V		50	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V		40	
				V$_{CCB}$ = 5 V ± 0.5 V		35	
t$_{rA}$	Input rise time	A-port rise time	Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V	3.2	9.5	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V	2.3	9.3	
				V$_{CCB}$ = 5 V ± 0.5 V	2	7.6	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	38	165	
				V$_{CCB}$ = 3.3 V ± 0.3 V	30	132	
				V$_{CCB}$ = 5 V ± 0.5 V	22	95	
t$_{rB}$	Input rise time	B-port rise time	Push-pull driving	V$_{CCB}$ = 2.5 V ± 0.2 V	4	10.8	ns
				V$_{CCB}$ = 3.3 V ± 0.3 V	2.7	9.1	
				V$_{CCB}$ = 5 V ± 0.5 V	2.7	7.6	
			Open-drain driving	V$_{CCB}$ = 2.5 V ± 0.2 V	34	145	
				V$_{CCB}$ = 3.3 V ± 0.3 V	23	106	
				V$_{CCB}$ = 5 V ± 0.5 V	10	58	

Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{fA}	Input fall time	A-port fall time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	2	5.9	ns
				V_{CCB} = 3.3 V ± 0.3 V	1.9	6	
				V_{CCB} = 5 V ± 0.5 V	1.7	13.3	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	4.4	6.9	
				V_{CCB} = 3.3 V ± 0.3 V	4.3	6.4	
				V_{CCB} = 5 V ± 0.5 V	4.2	6.1	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	2.9	7.6	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.8	7.5	
				V_{CCB} = 5 V ± 0.5 V	2.8	8.8	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	6.9	13.8	
				V_{CCB} = 3.3 V ± 0.3 V	7.5	16.2	
				V_{CCB} = 5 V ± 0.5 V	7	16.2	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		V_{CCB} = 2.5 V ± 0.2 V		1	ns
				V_{CCB} = 3.3 V ± 0.3 V		1	
				V_{CCB} = 5 V ± 0.5 V		1	
	Maximum data rate		Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	24		Mbps
				V_{CCB} = 3.3 V ± 0.3 V	24		
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	2		
				V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

Product Folder Links: *TXS0104E*

6.11 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.2	ns
				V_{CCB} = 3.3 V ± 0.3 V		3.3	
				V_{CCB} = 5 V ± 0.5 V		3.4	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	1.7	6.3	
				V_{CCB} = 3.3 V ± 0.3 V	2	6	
				V_{CCB} = 5 V ± 0.5 V	2.1	5.8	
t_{PLH}	Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3.5	
				V_{CCB} = 3.3 V ± 0.3 V		4.1	
				V_{CCB} = 5 V ± 0.5 V		4.4	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	43	250	
				V_{CCB} = 3.3 V ± 0.3 V	36	206	
				V_{CCB} = 5 V ± 0.5 V	27	190	
t_{PHL}	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		3	ns
				V_{CCB} = 3.3 V ± 0.3 V		3.6	
				V_{CCB} = 5 V ± 0.5 V		4.3	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	1.8	4.7	
				V_{CCB} = 3.3 V ± 0.3 V	2.6	4.2	
				V_{CCB} = 5 V ± 0.5 V	1.2	4	
t_{PLH}	Propagation delay time (low-to-high output)	B-to-A	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V		2.5	
				V_{CCB} = 3.3 V ± 0.3 V		1.6	
				V_{CCB} = 5 V ± 0.5 V		0.7	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	44	170	
				V_{CCB} = 3.3 V ± 0.3 V	37	140	
				V_{CCB} = 5 V ± 0.5 V	27	103	
t_{en}	Enable time	OE-to-A or B		V_{CCB} = 2.5 V ± 0.2 V		200	ns
				V_{CCB} = 3.3 V ± 0.3 V		200	
				V_{CCB} = 5 V ± 0.5 V		200	
t_{dis}	Disable time	OE-to-A or B		V_{CCB} = 2.5 V ± 0.2 V		50	ns
				V_{CCB} = 3.3 V ± 0.3 V		40	
				V_{CCB} = 5 V ± 0.5 V		35	
t_{rA}	Input rise time	A-port rise time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	2.8	7.4	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.6	6.6	
				V_{CCB} = 5 V ± 0.5 V	1.8	5.6	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	34	149	
				V_{CCB} = 3.3 V ± 0.3 V	28	121	
				V_{CCB} = 5 V ± 0.5 V	24	89	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	3.2	8.3	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.9	7.2	
				V_{CCB} = 5 V ± 0.5 V	2.4	6.1	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	35	151	
				V_{CCB} = 3.3 V ± 0.3 V	24	112	
				V_{CCB} = 5 V ± 0.5 V	12	64	

Product Folder Links: TXS0104E

Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_{fA}	Input fall time	A-port fall time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	1.9	5.7	ns
				V_{CCB} = 3.3 V ± 0.3 V	1.9	5.5	
				V_{CCB} = 5 V ± 0.5 V	1.8	5.3	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	4.4	6.9	
				V_{CCB} = 3.3 V ± 0.3 V	4.3	6.2	
				V_{CCB} = 5 V ± 0.5 V	4.2	5.8	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	2.2	7.8	ns
				V_{CCB} = 3.3 V ± 0.3 V	2.4	6.7	
				V_{CCB} = 5 V ± 0.5 V	2.6	6.6	
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	5.1	8.8	
				V_{CCB} = 3.3 V ± 0.3 V	5.4	9.4	
				V_{CCB} = 5 V ± 0.5 V	5.4	10.4	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		V_{CCB} = 2.5 V ± 0.2 V		1	ns
				V_{CCB} = 3.3 V ± 0.3 V		1	
				V_{CCB} = 5 V ± 0.5 V		1	
	Maximum data rate		Push-pull driving	V_{CCB} = 2.5 V ± 0.2 V	24		Mbps
				V_{CCB} = 3.3 V ± 0.3 V	24		
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain driving	V_{CCB} = 2.5 V ± 0.2 V	2		
				V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

Product Folder Links: *TXS0104E*

6.12 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
t_{PHL}	Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.4	ns
				V_{CCB} = 5 V ± 0.5 V		3.1	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	1.3	4.2	
				V_{CCB} = 5 V ± 0.5 V	1.4	4.6	
t_{PLH}	Propagation delay time (low-to-high output)		Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		4.2	
				V_{CCB} = 5 V ± 0.5 V		4.4	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	36	204	
				V_{CCB} = 5 V ± 0.5 V	28	165	
t_{PHL}	Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	ns
				V_{CCB} = 5 V ± 0.5 V		3.3	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	1	124	
				V_{CCB} = 5 V ± 0.5 V	1	97	
t_{PLH}	Propagation delay time (low-to-high output)		Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V		2.5	
				V_{CCB} = 5 V ± 0.5 V		2.6	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	3	139	
				V_{CCB} = 5 V ± 0.5 V	3	105	
t_{en}	Enable time	OE-to-A or B		V_{CCB} = 3.3 V ± 0.3 V		200	ns
				V_{CCB} = 5 V ± 0.5 V		200	
t_{dis}	Disable time	OE-to-A or B		V_{CCB} = 3.3 V ± 0.3 V		40	ns
				V_{CCB} = 5 V ± 0.5 V		35	
t_{rA}	Input rise time	A-port rise time	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	2.3	5.6	ns
				V_{CCB} = 5 V ± 0.5 V	1.9	4.8	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	25	116	
				V_{CCB} = 5 V ± 0.5 V	19	85	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	2.5	6.4	ns
				V_{CCB} = 5 V ± 0.5 V	2.1	7.4	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	26	116	
				V_{CCB} = 5 V ± 0.5 V	26	116	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	2	5.4	ns
				V_{CCB} = 5 V ± 0.5 V	1.9	5	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	4.3	6.1	
				V_{CCB} = 5 V ± 0.5 V	4.2	5.7	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	2.3	7.4	ns
				V_{CCB} = 5 V ± 0.5 V	2.4	7.6	
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	5	7.6	
				V_{CCB} = 5 V ± 0.5 V	4.8	8.3	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		V_{CCB} = 3.3 V ± 0.3 V		1	ns
				V_{CCB} = 5 V ± 0.5 V		1	
	Maximum data rate		Push-pull driving	V_{CCB} = 3.3 V ± 0.3 V	24		Mbps
				V_{CCB} = 5 V ± 0.5 V	24		
			Open-drain driving	V_{CCB} = 3.3 V ± 0.3 V	2		
				V_{CCB} = 5 V ± 0.5 V	2		

Product Folder Links: TXS0104E

6.13 Typical Characteristics

$V_{CCA} = 1.8\ V \qquad V_{IL(A)} = 150\ mV$
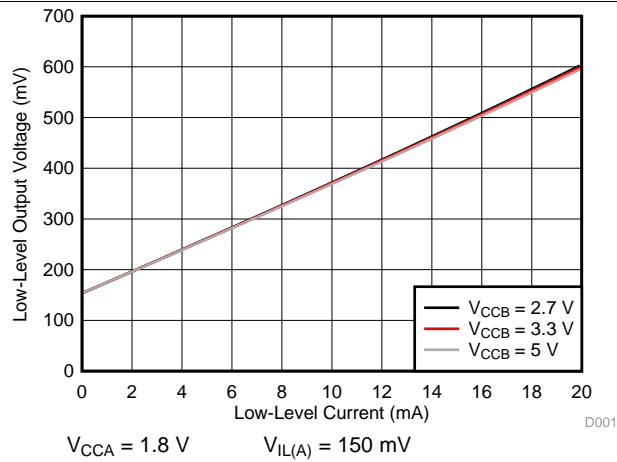
Figure 1. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

$V_{CCA} = 2.7\ V \qquad V_{IL(A)} = 150\ mV$
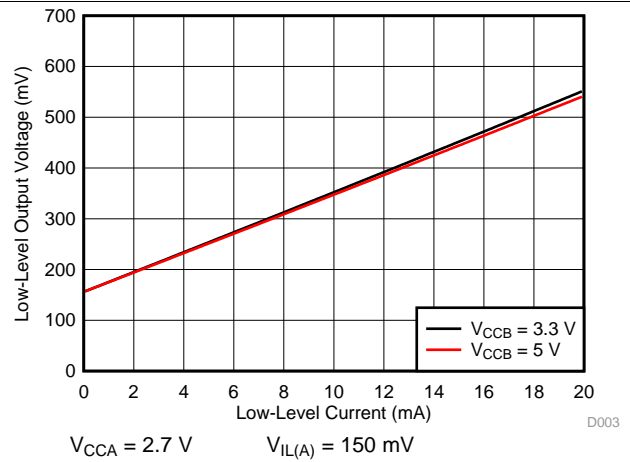
Figure 2. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

$V_{CCA} = 3.3\ V \qquad V_{IL(A)} = 150\ mV$
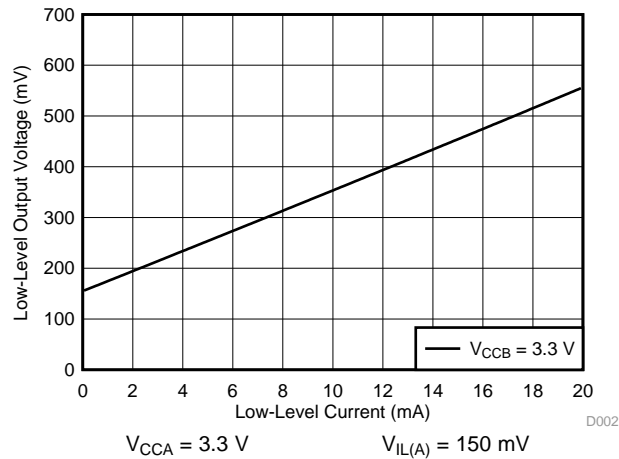
Figure 3. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

Product Folder Links: *TXS0104E*

7 Parameter Measurement Information

7.1 Load Circuits
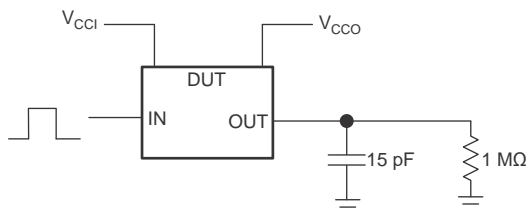
Figure 4. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver
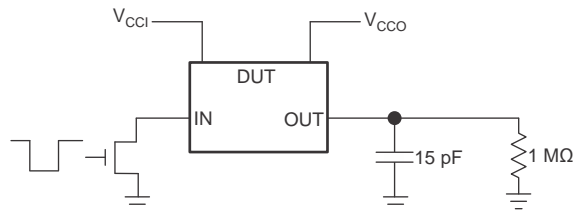
Figure 5. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver
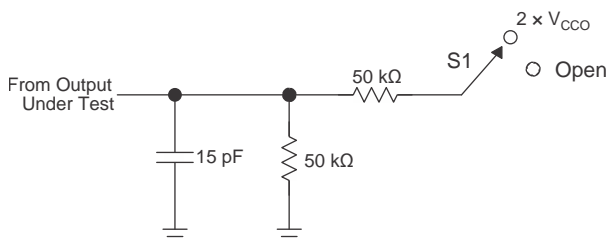
TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	$2 \times V_{CCO}$
t_{PHZ} / t_{PZH} (t_{en})	Open

Figure 6. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.
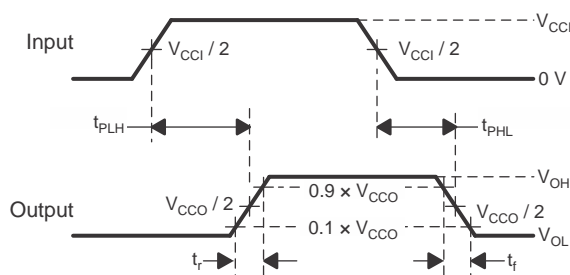
7.2 Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:
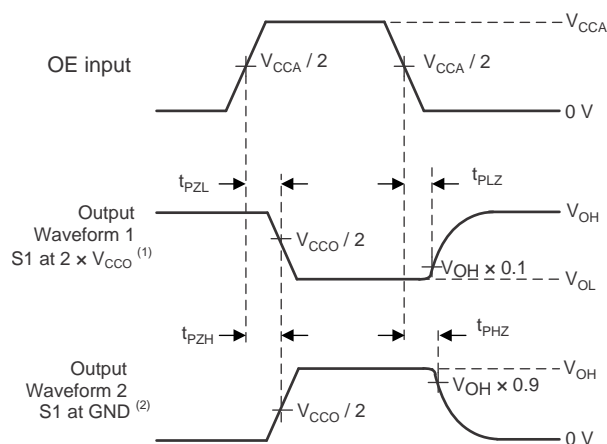
- PRR ≤ 10 MHz
- $Z_O = 50\ \Omega$
- dv/dt ≥ 1 V/ns
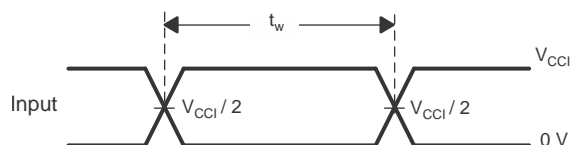
Figure 7. Pulse Duration

Figure 8. Propagation Delay Times

(1) Waveform 1 is for an output with internal such that the output is high, except when OE is high (see Figure 6).

(2) Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 9. Enable and Disable Times

Product Folder Links: *TXS0104E*

8 Detailed Description

8.1 Overview

The TXS0104E device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.
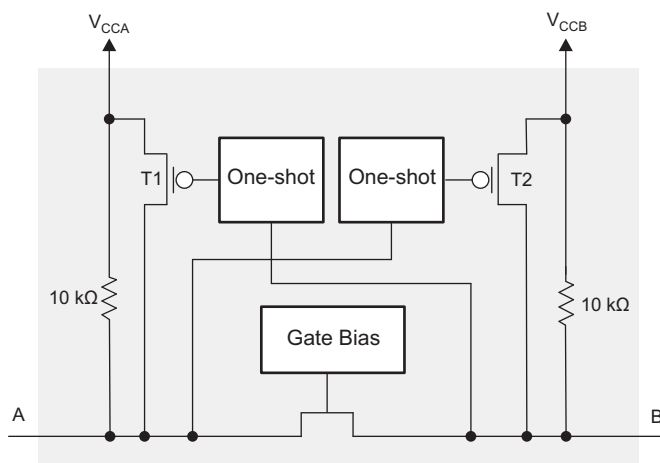
8.2 Functional Block Diagram
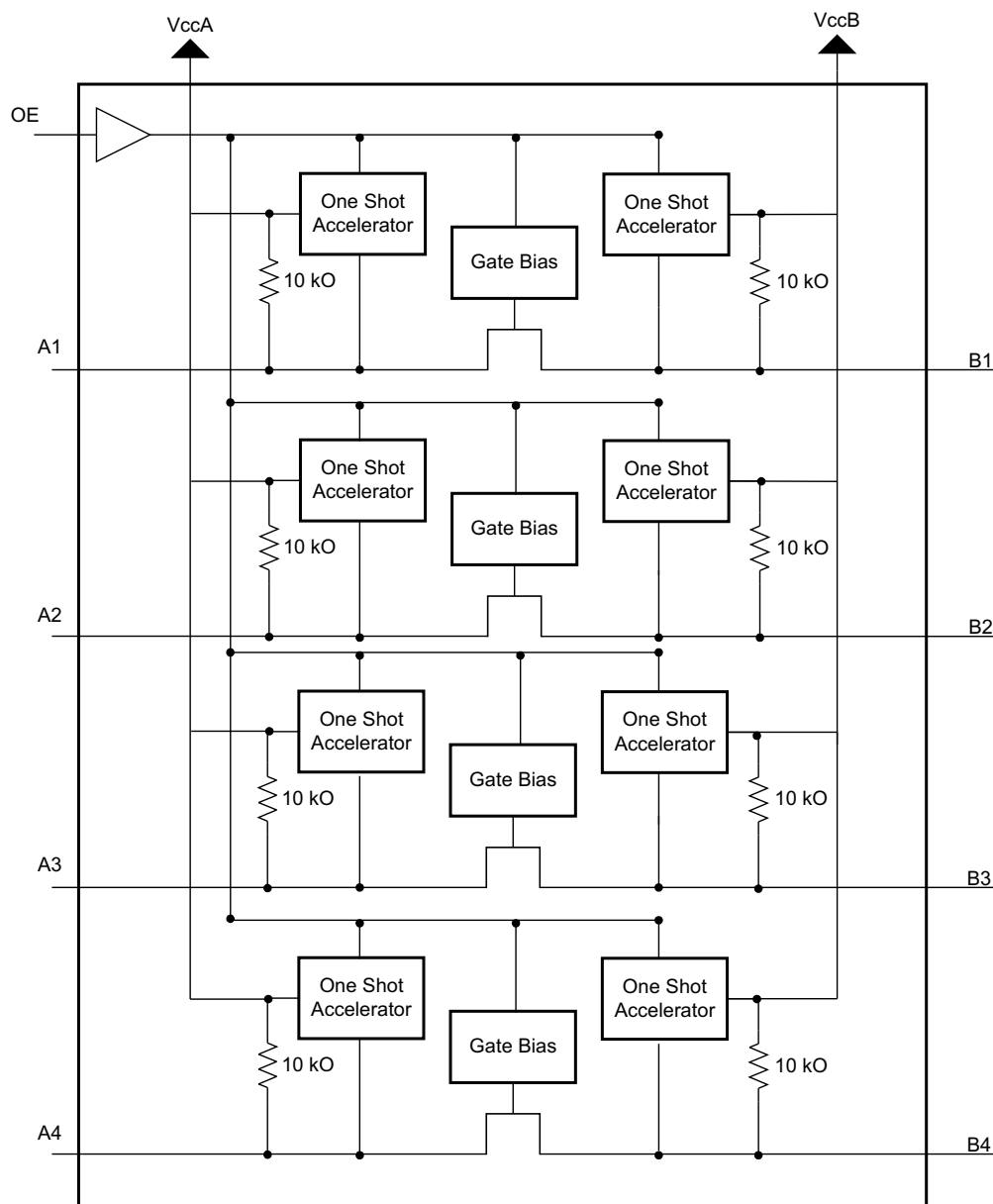
8.3 Feature Description

8.3.1 Architecture

The TXS0104E architecture (see Figure 10) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

Figure 10. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

8.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104E device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

8.3.3 Power Up

During operation, ensure that V_{CCA} ≤ V_{CCB} at all times. During power-up sequencing, V_{CCA} ≥ V_{CCB} does not damage the device, so any power supply can be ramped up first.

8.3.4 Enable and Disable

The TXS0104E device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

8.3.5 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors).

8.4 Device Functional Modes

The TXS0104E device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

Product Folder Links: *TXS0104E*

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXS0104E device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104E device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The TXS0104E device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device might be a better option for such push-pull applications.

9.2 Typical Application
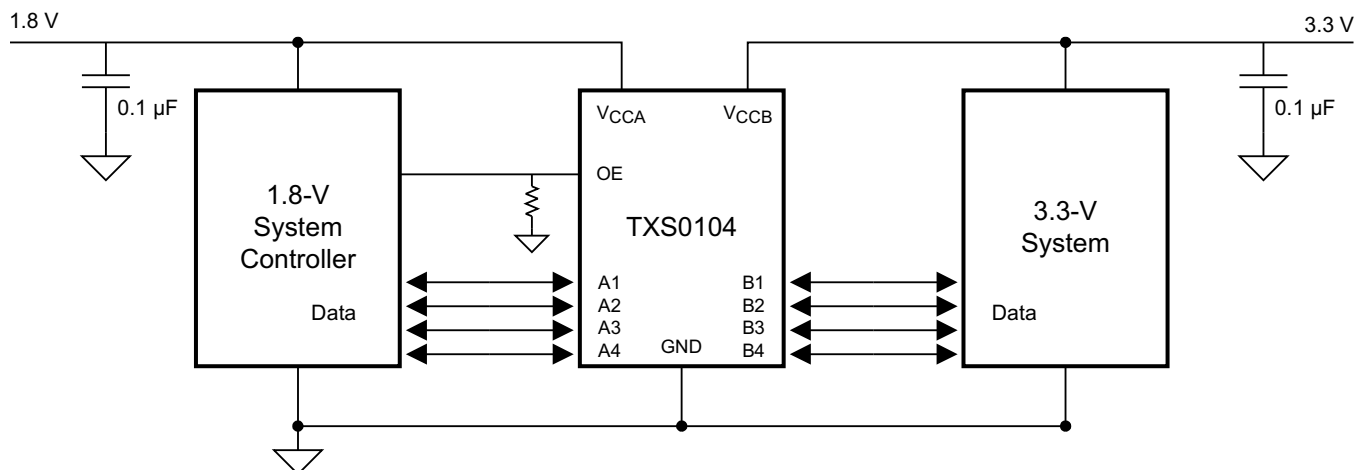
Figure 11. Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0104E device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0104E device is driving to determine the output voltage range.
  - The TXS0104E device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull down resistor.
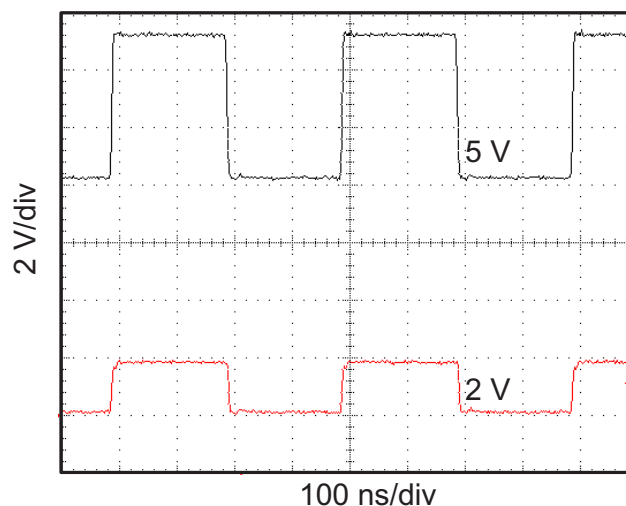
$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \tag{1}$$

where

V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}

R_{PD} is the value of the external pull down resistor

9.2.3 Application Curve

$V_{CCA} = 1.8\ V$ $\qquad$ $V_{CCB} = 5\ V$

Figure 12. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

The TXS0104E device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V and V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The TXS0104E device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.
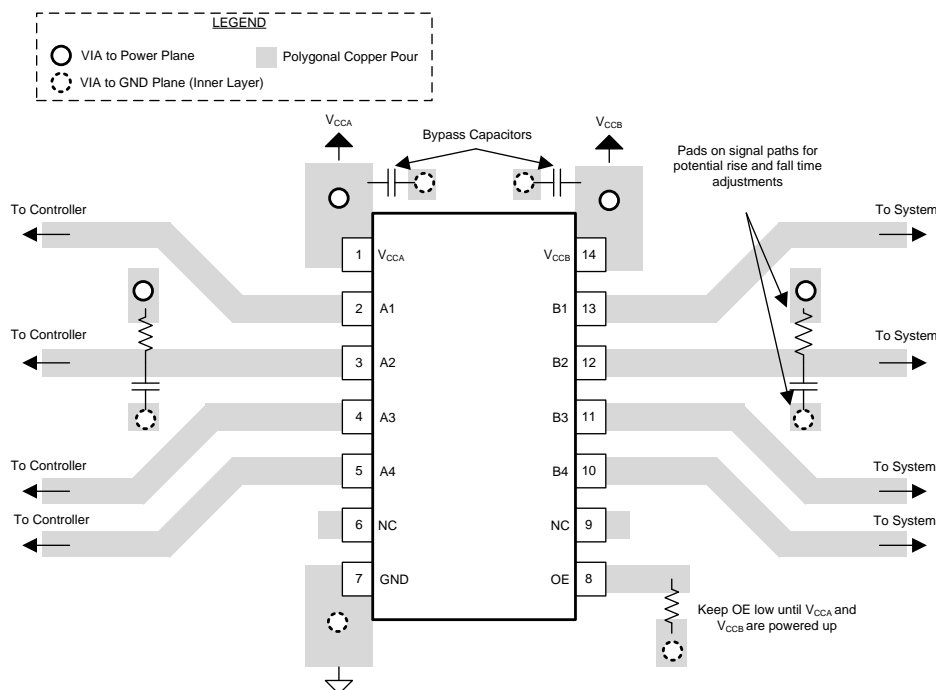
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.
- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

11.2 Layout Example

Figure 13. TXS0104E Layout Example

Product Folder Links: *TXS0104E*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* application report
- Texas Instruments, *Basics of Voltage Translation* application report
- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.
   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0104ED	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104E	Samples
TXS0104EDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104E	Samples
TXS0104EDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104E	Samples
TXS0104EPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04E	Samples
TXS0104EPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04E	Samples
TXS0104ERGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YF04E	Samples
TXS0104ERGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YF04E	Samples
TXS0104EYZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2HN, 2N, 2N7)	Samples
TXS0104EZXUR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YF04E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0104E :

• Automotive: TXS0104E-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104EDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TXS0104EPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXS0104ERGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104EYZTR	DSBGA	YZT	12	3000	180.0	8.4	1.49	1.99	0.75	4.0	8.0	Q2
TXS0104EZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104EDR	SOIC	D	14	2500	367.0	367.0	38.0
TXS0104EPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TXS0104ERGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TXS0104EYZTR	DSBGA	YZT	12	3000	182.0	182.0	20.0
TXS0104EZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	336.6	336.6	28.6

YZT (R-XBGA-N12)   (CUSTOM) DIE-SIZE BALL GRID ARRAY
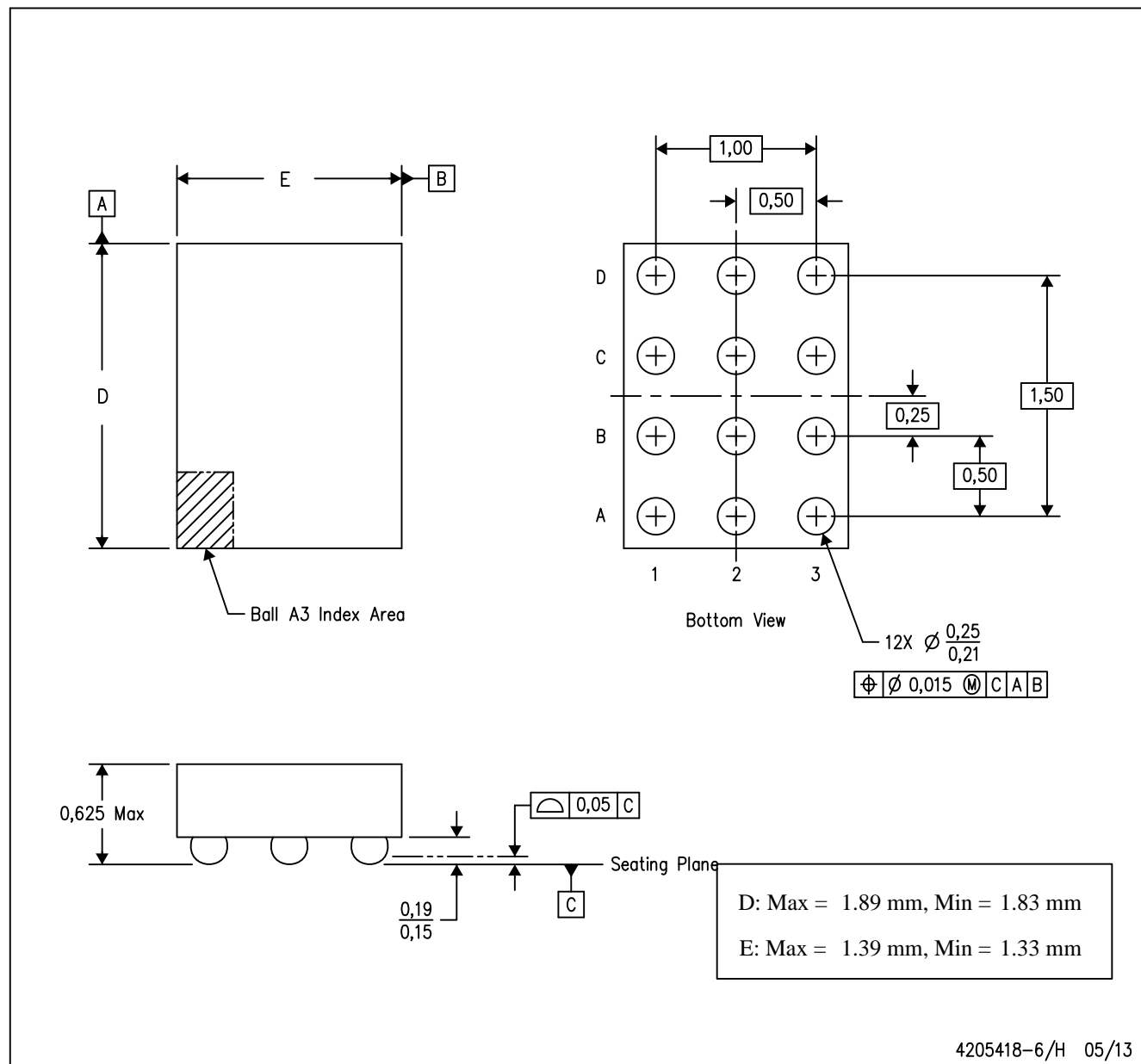
1,00

0,50

D
C
B
A

1   2   3

Bottom View

1,50

0,25

0,50

Ball A3 Index Area

12X Ø 0,25 / 0,21

⊕ Ø 0,015 Ⓜ C A B

E

A

B

D

0,625 Max

0,19 / 0,15

0,05 C

Seating Plane

C

D: Max = 1.89 mm, Min = 1.83 mm

E: Max = 1.39 mm, Min = 1.33 mm

4205418-6/H 05/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
         B. This drawing is subject to change without notice.
         C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

RGY (S−PVQFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

3,65 / 3,35   A

B

3,65 / 3,35

Pin 1 Index Area
Top and Bottom
F

0,20 Nominal
Lead Frame

1,00 / 0,80

Seating Plane

0,08 C

0,05 / 0,00
Seating Height

C

2,00

0,50

14X 0,50 / 0,30

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

1,50

14X 0,30 / 0,18

0,10 (M) C A B
0,05 (M) C

Bottom View
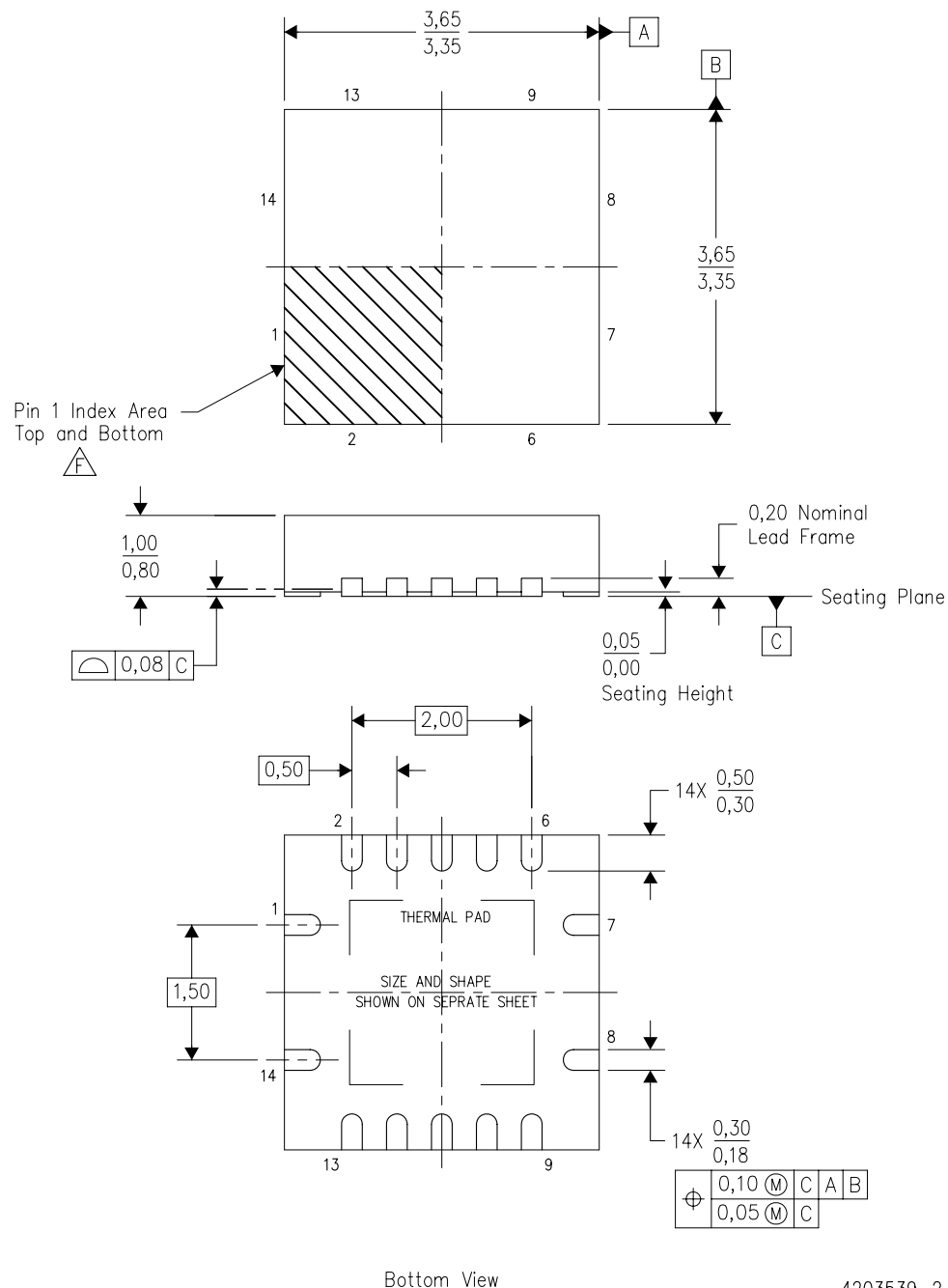
4203539−2/I   06/2011
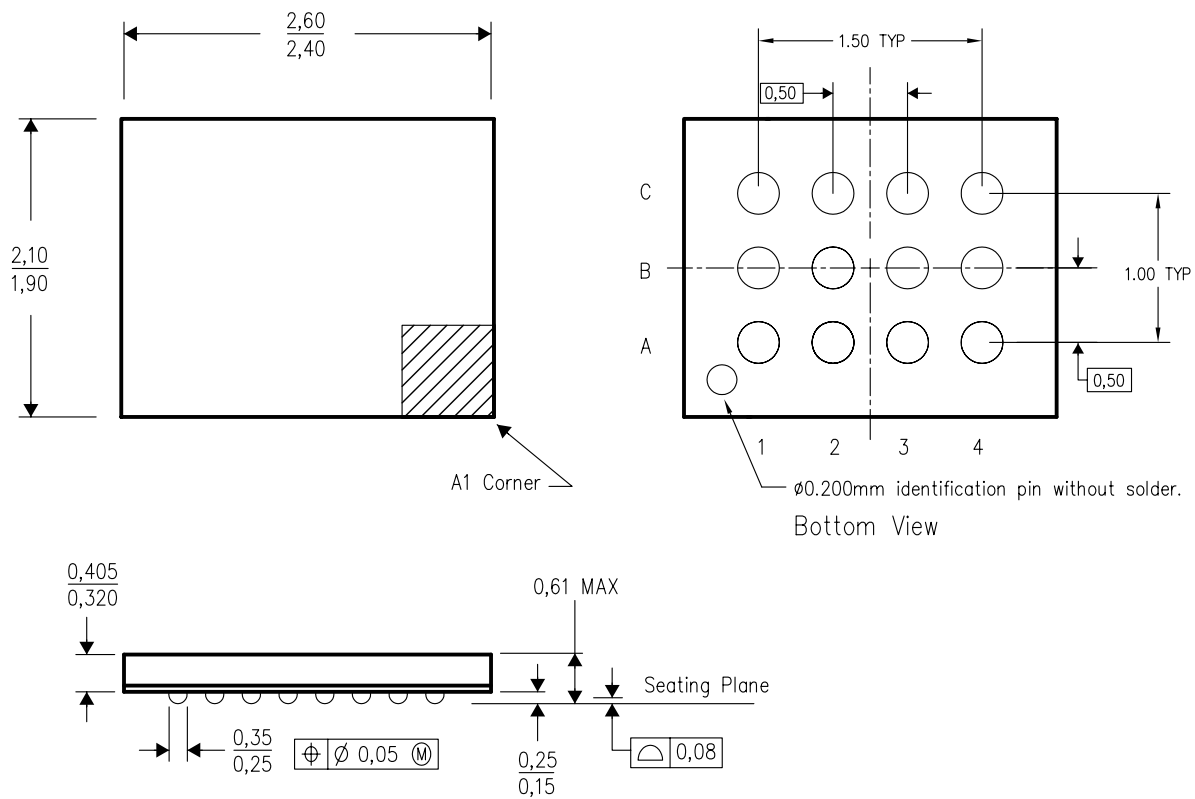
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
           The Pin 1 identifiers are either a molded, marked, or metal feature.
        G. Package complies to JEDEC MO−241 variation BA.

TEXAS INSTRUMENTS
www.ti.com

RGY (S−PVQFN−N14)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

2,05±0,10

2,05±0,10

Exposed Thermal Pad
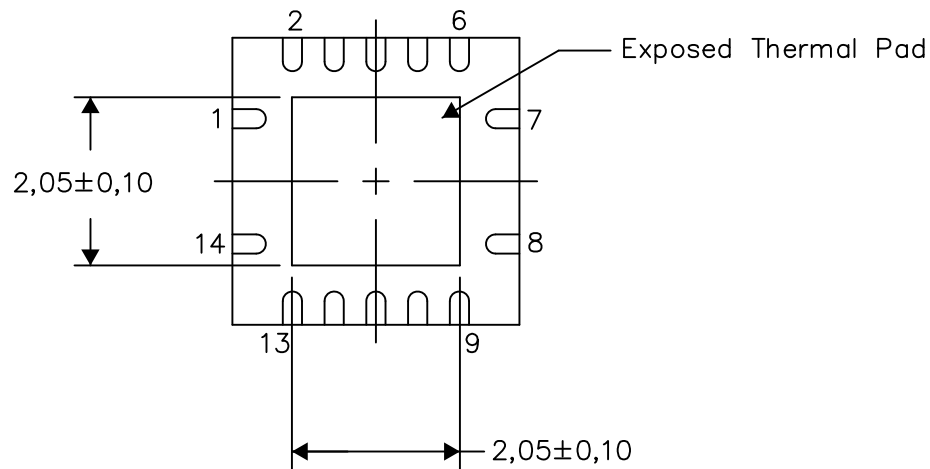
Bottom View

Exposed Thermal Pad Dimensions

4206353−2/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)   PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

4,30

4,30 2,60

2,05

2,05

1,50

Note D

8x0,50   0.28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25

4,25 2,65

1,50

0,82 SQ

0,50

0,80 x 14 PL.

8x0,50   0,23 x 14 PL.

64% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6xØ0,3

4208122-2/P 03/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   7

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AB.

TEXAS INSTRUMENTS
www.ti.com

D (R–PDSO–G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283–3/E 08/12

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC–7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

4,50
4,30

6,60
6,20

1   7

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌓ 0,10

4040064−3/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
          Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

TEXAS INSTRUMENTS
www.ti.com

ZXU (S–PBGA–N12)   PLASTIC BALL GRID ARRAY

$\frac{2,60}{2,40}$

$\frac{2,10}{1,90}$

A1 Corner

1.50 TYP

0,50

C

B

A

1.00 TYP

0,50

1   2   3   4

Ø0.200mm identification pin without solder.

Bottom View

$\frac{0,405}{0,320}$

0,61 MAX

Seating Plane

$\frac{0,35}{0,25}$ ⊕ Ø 0,05 Ⓜ

$\frac{0,25}{0,15}$ ⌓ 0,08

4207009/B 06/05

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   This package is a lead–free solder ball design.