THE HONG KONG POLYTECHNIC UNIVERSITY
香港理工大學

EIE4110 Introduction to VLSI and CAD

Laboratory 5 – High-Level Synthesis (HLS)

Student Name: _____

Student No.: _____

Date: _____

PART 1 – fir.c Synthesis

a.) Convert the fir SW description into synthesizable C code for HLS. Annotate here the changes required.

(2 marks)

b)Synthesize the fir.c design. Annotate from Resource constraint file (FCNT) the number and type of Functional Units (FUs) needed to fully parallelize the description

(2 marks)

b.) Report from the QoR file the size of the circuit in terms of number of LUTs and registers. Report also the latency of the synthesized circuit and the critical path and maximum frequency.

(2 marks)

c.) Perform Logic synthesis using Xilinx ISE and compare the area results in terms of LUTs. Discuss if they match or not and why they do/don't.

(4 marks)

PART 2 – for.c Verification

a.) Perform a cycle-accurate simulation using the untimed test vectors used for the software simulation and make sure that the simulation outputs match. Demonstrate it to the supervisor (signature required)

(2 marks)

PART 3 firc Design Space Exploration

a.) Reduce the number of FUs in the Resource Constraint file (FCNT) from the maximum number obtained in the initial design to half that number and to only 1 FU. Annotate the Area in terms if LUTs and the latency of each of the 3 designs in a table. Plot the graph of **area vs. latency** of the 3 designs. Discuss the results. Are they what you expected? (Yes/No)

(6 marks)

Design	Functional Units	LUTs	Latency	Critical path
1	Maximum number of FUs			
2	1 FU of each Type			
3	A single FU of each type of the largest bitwidth			