Fabrication and Characterisation

of a Graphene Field Effect Transistor

Nandini Nandini, Mainak Roy and Lukas Giehl

Faculty of Graphene-based Nanotechnology

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Contents

Introduction – Why Graphene?

- 2D structure with high number of benefits
- Super conductivity
- Hexagonal structure
- Both mechanical and Electrical property

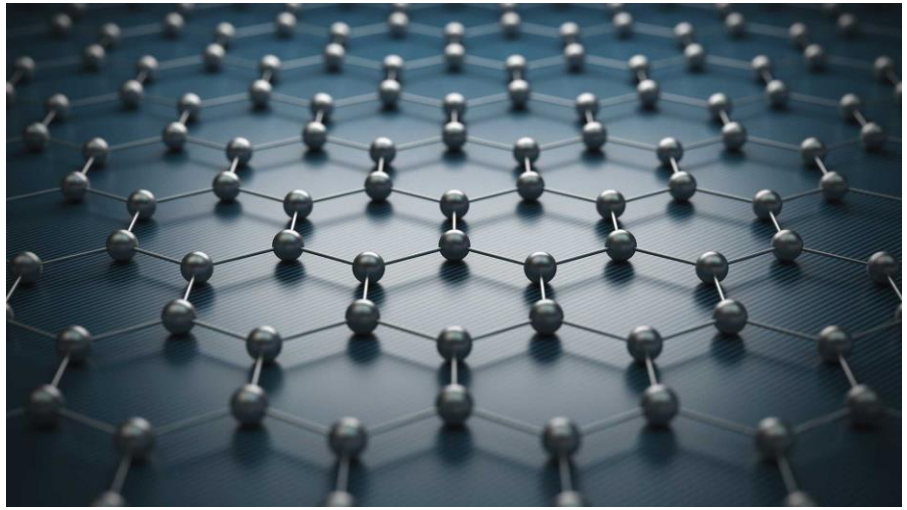

Figure 1: Hexagonal Structure of Graphene

https://singularityhub.com/uploads/2018/08/graphene-molecular-grid-atomic-structure_shutterstock_1052481413.jpg

Introduction – Types of GFET

types

- Back gated GFETs
- Top gated GFETs
- Dual – Gated GFETs

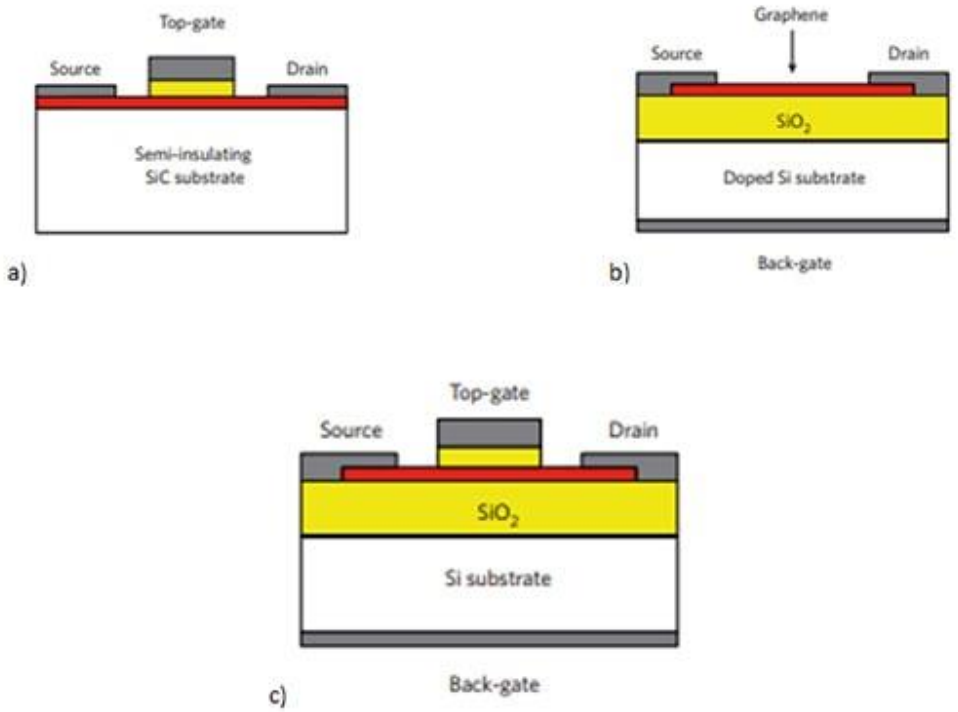

Figure 2: Different GFET Topologies

https://www.allaboutcircuits.com/uploads/articles/graphene-field-effect-transistors-gfets-construction-benefits-and-challenges-ak-aac-image3.jpg

Introduction – DIRAC Point

- The dirac point is observed where the conduction and valance bands intersect.
- At the dirac point, graphene exhibits excellent conductivity.

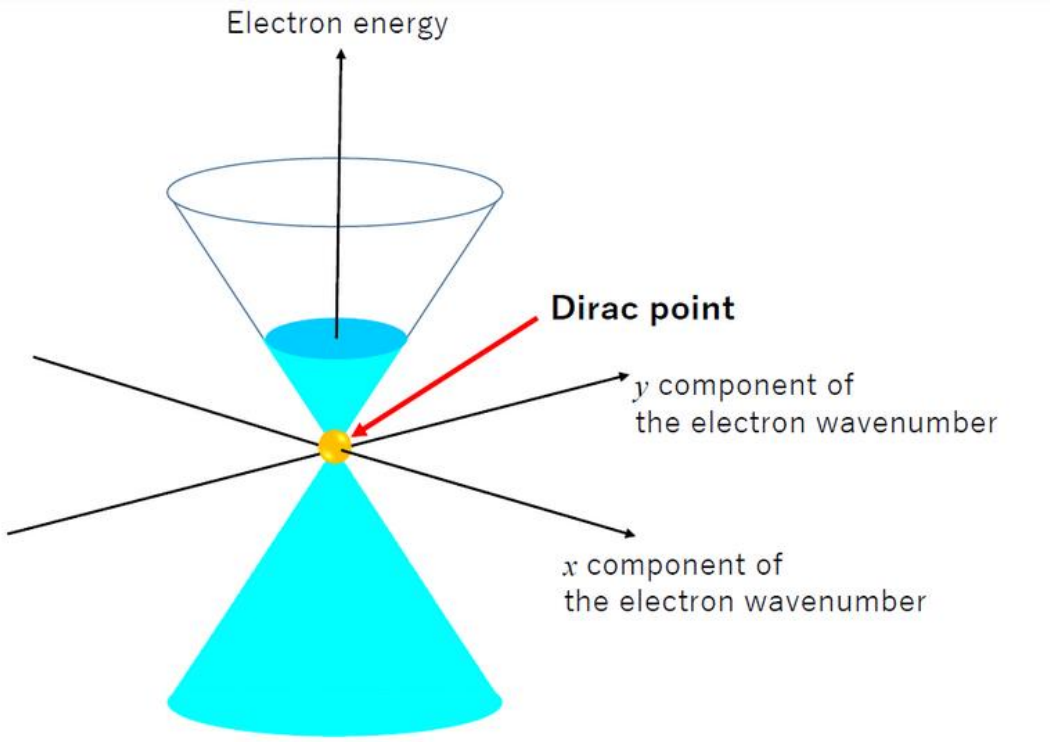

Figure 3: DIRAC Point Visualized

https://www.thegraphenecouncil.org/resource/resmgr/images/products/product/dec/product_1/product_2/Dispersion_relation2.PNG

Introduction – Photolithography

- Coating
- Exposure
- Development
- Etching
- Stripping

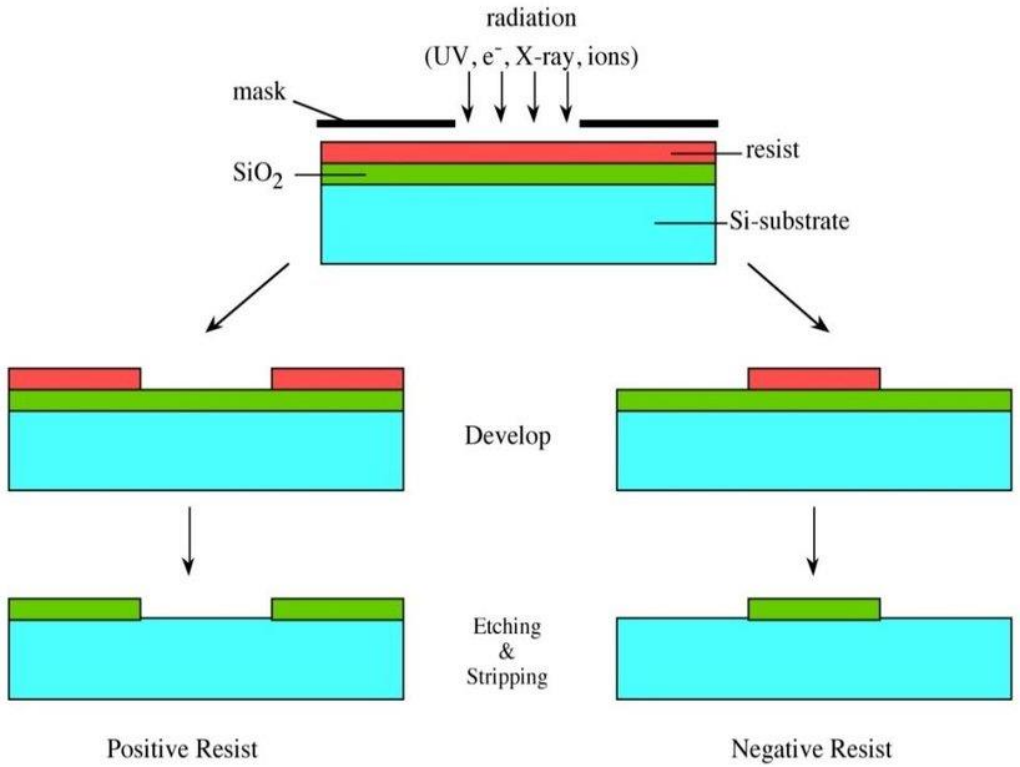

Figure 4: Photolithography Process Steps

https://www.researchgate.net/profile/Nur-Azura-Mohd-Said/publication/326287044/figure/fig22/AS:646643913355265@1531183331184/The-photolithography-process-with-negative-and-positive-photoresist.png

Methods

- Wafer Preparation
- Lithography
- Metal Finger Deposition
- Fabrication of the Graphene Channel

Methods – Wafer Preparation

- 6in Si-wafer
  - t = 675µm
  - Boron p-dopend
  - 85nm SiO_2
- Remove backside oxide
- Cut into 2x2cm dies
- Throughout cleaning
  - 5min Acetone
  - 3min Isopropanol
  - Dry with N_2

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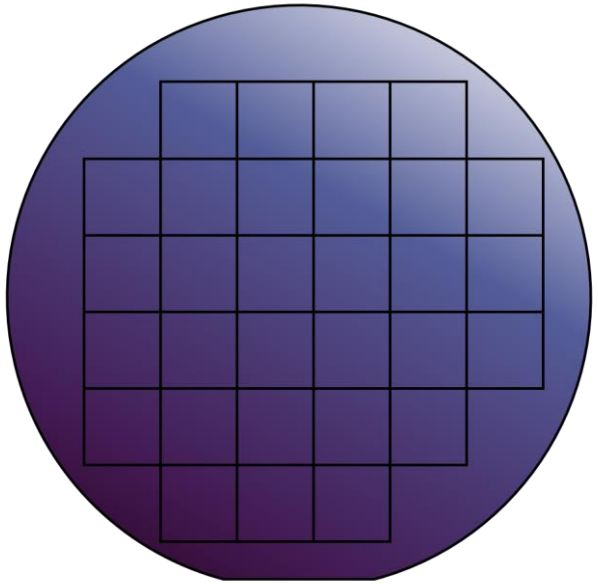

Figure 5: Wafer with Marked 2x2cm Dies

Methods - Lithography

- AZ nLOF2070
  - Spincoat 500rpm 5s + 3000rpm 50s
- Softbake
  - 100°C for 60s
- Mask Align & Exposure
  - 180mJ/cm^2
- Postbake
  - 110°C for 90s
- Develop in AZ 726 MIF
  - 70s
- Stop Process in Di water

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- AZ nLOF2070
  - Spincoat 500rpm 5s + 3000rpm 50s
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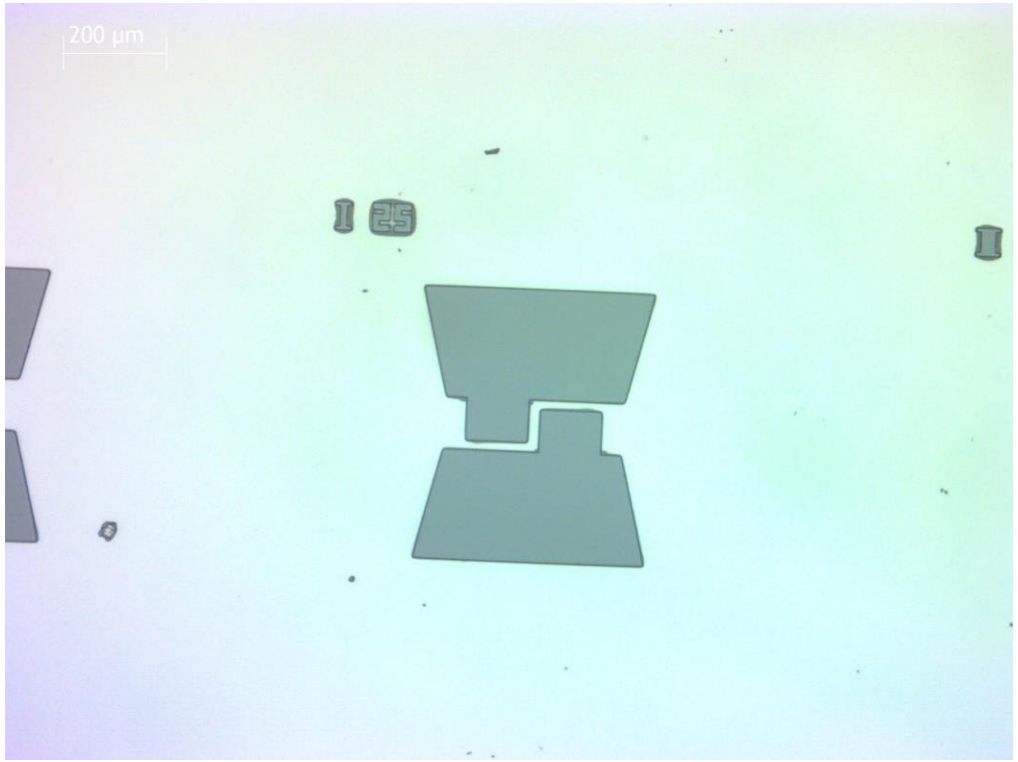

Figure 6: Negative Photomask of the Drain and Source Contacts of a Single Transistor After Development

Methods - Lithography

- AZ nLOF2070
  - Spincoat 500rpm 5s + 3000rpm 50s
- Softbake
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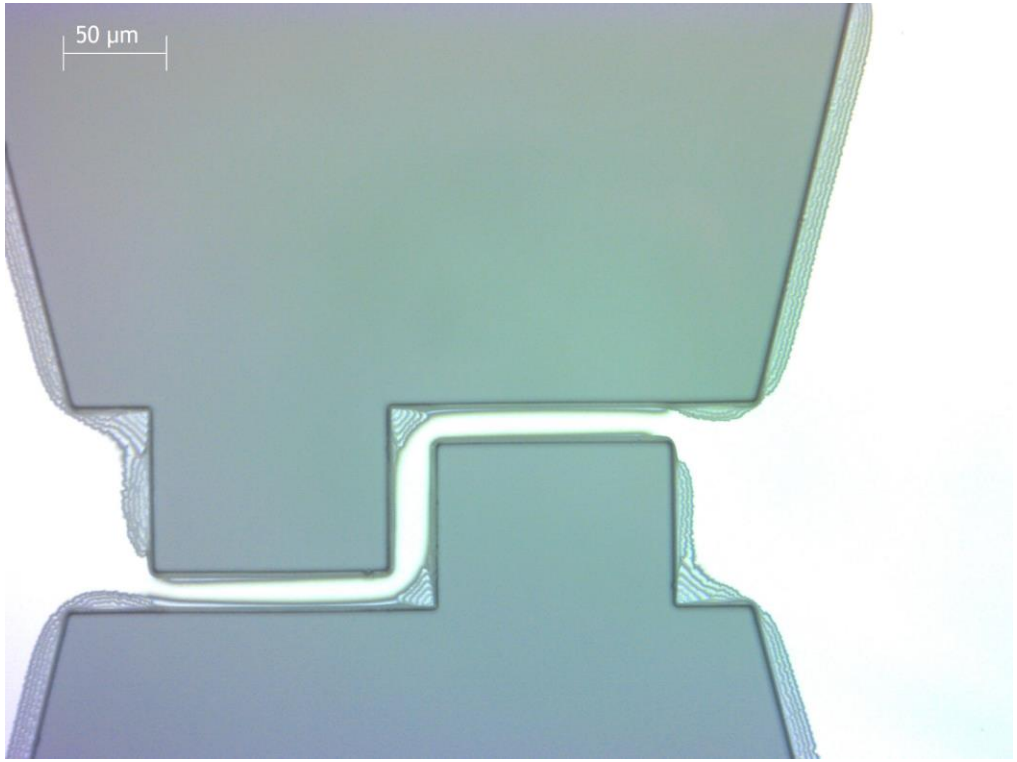

Figure 7: Undercut of the Photoresist on the Edges of the Drain and Source Structures

Methods – Drain and Source Channel Fabrication

- Base Material SiO_2
- Titanium 10nm
- Molybdenum 150nm

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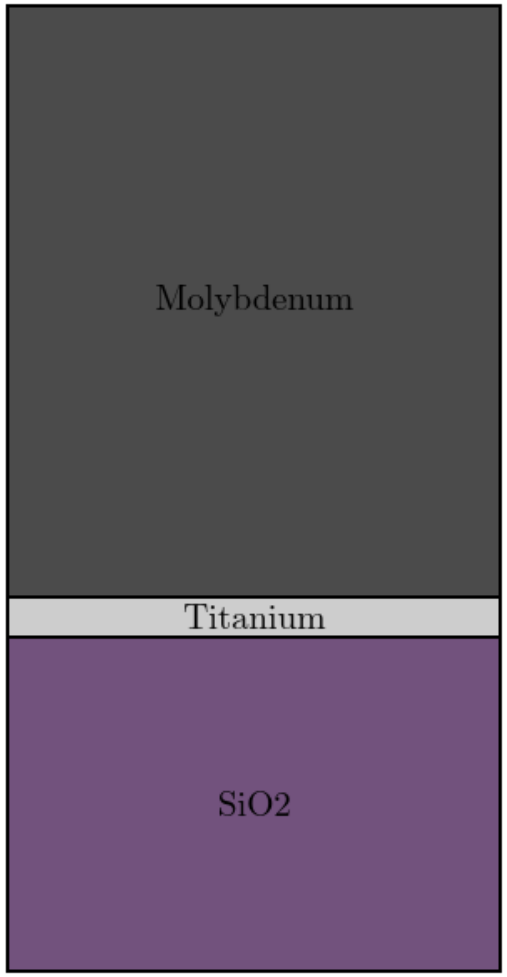

Figure 8: Stackup of Metals ontop of SiO_2

Methods – Drain and Source Channel Fabrication

- Electron Beam Evaporation
- Argon Plasma Cleaning
  - $7x10^{-6}$mbar
- Deposition of Ti at 0.2nm/s
- Deposition of Mo at 0.5nm/s
- Spinning Jig

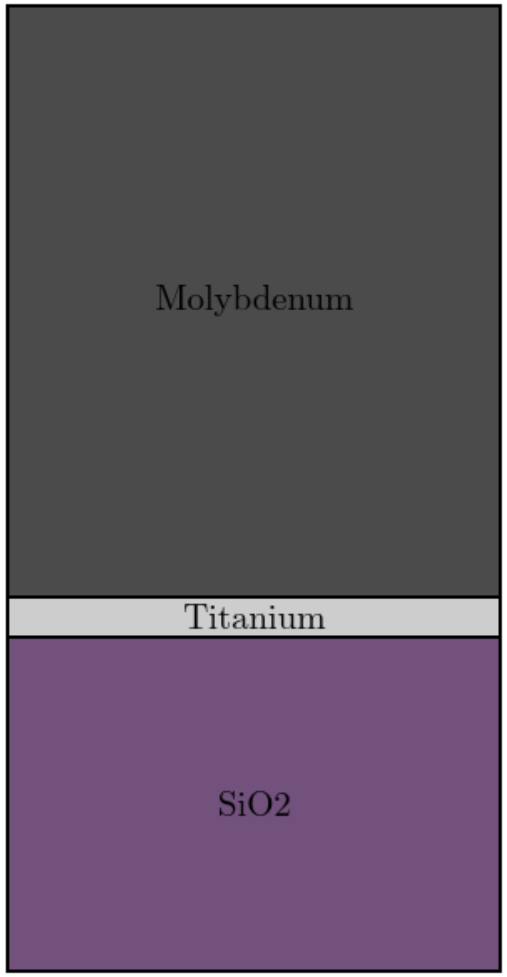

Figure 8: Stackup of Metals ontop of SiO_2

Methods – Drain and Source Channel Fabrication (Liftoff)

- Immerse into Acetone
  - Photoresist will detach from SiO_2
- Carry out cleaning step
  - 3min IPA
  - Dry with N_2

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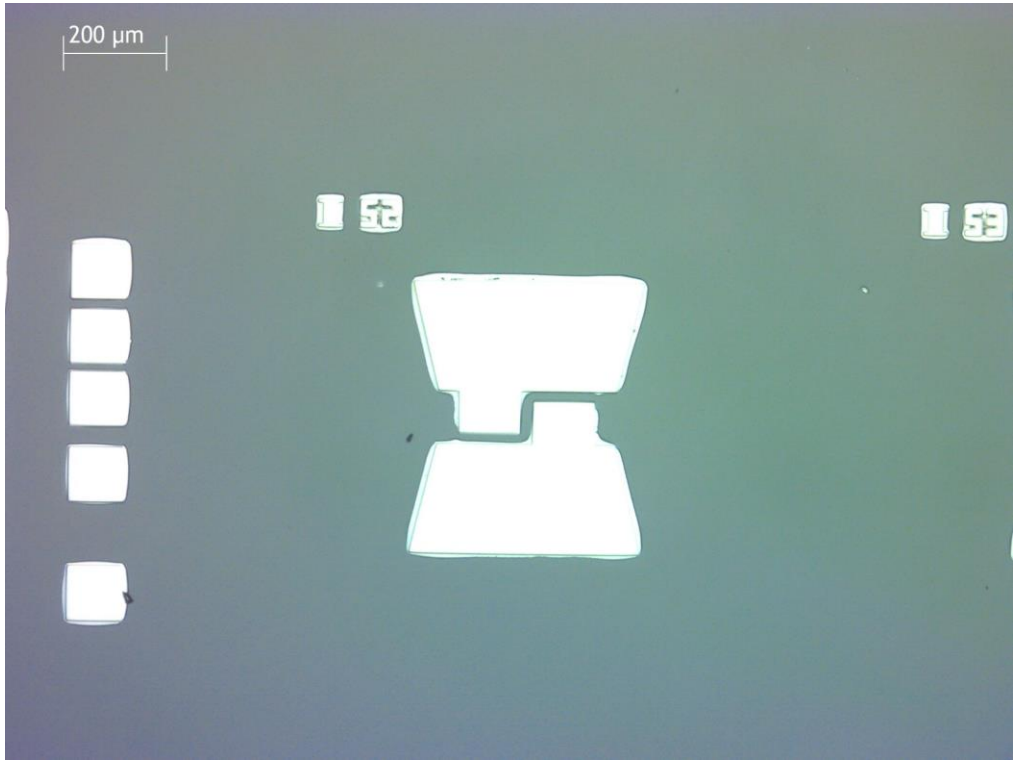

Figure 9: Source and Drain Structure after Liftoff

Methods – Drain and Source Channel Fabrication (Liftoff)

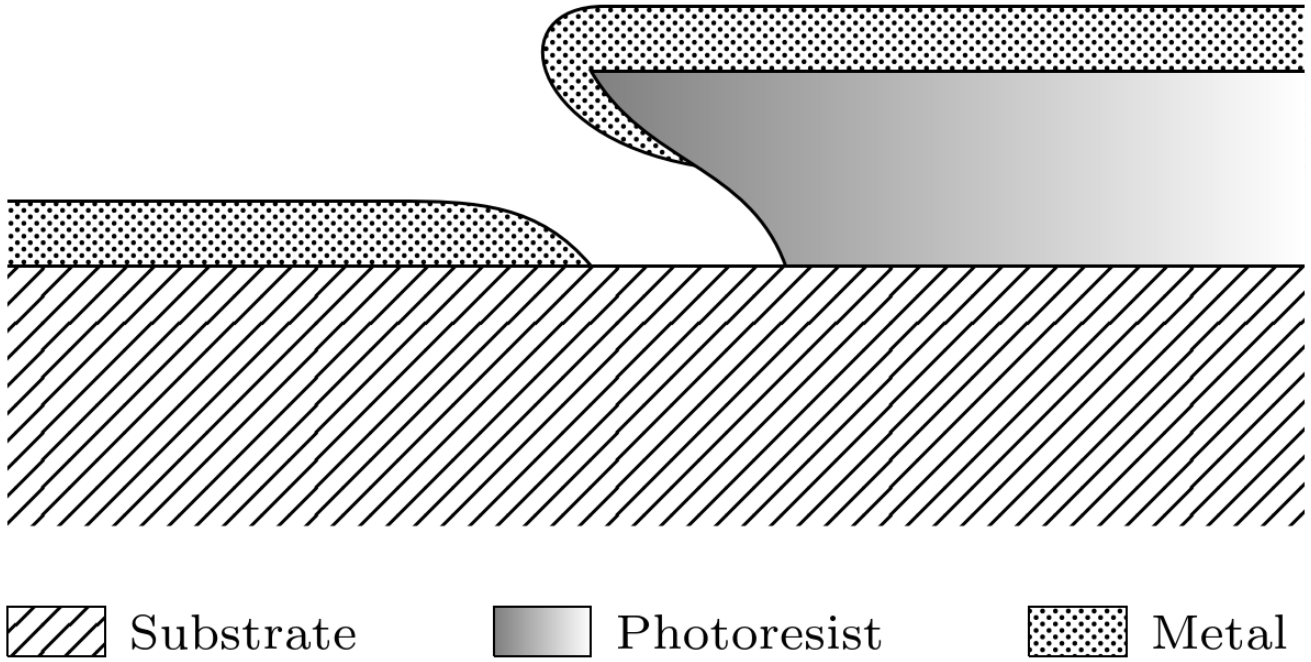

Figure 10: Cross Section after PVD Process before Liftoff

Methods – Graphene Preparation

- CVD Graphene
  - More uniform
  - Easier to work with
- Cut into 2x2 cm dies
  - Flatten

Methods – Graphene PMMA Application

- Stabilizes Graphene Sheet
- PMMA AR-P 649.04
  - Spincoat 2000rpm 50s
- Bake
  - 80°C for 3min
- Cut edges of die

Methods – Graphene Bubbling Transfer

- Chemical Reaction
  - Detaching Graphene from Copper Sheet
- Sodium Hydroxide Solution (NaOH)
  - 1g NaOH mixed with 100g DI water
- Setup
  - Electrode: Graphite Rod
  - Cathode: Sample held with tweezers
  - Supply: 3.5V CV

Methods – Graphene Bubbling Transfer

- Bubbling Transfer
  - Slowly lower copper sheet into solution
  - Turn 180° when nearly submerged
  - Continue and let go if sheet fully detached
- Cleaning
  - Two step process
  - Clean Graphene sheet in DI water
    - Two separate containers, 10min each
    - Transfer with spoon
- Transfer Graphene to sample

Methods – Graphene Bubbling Transfer

- Post Processing
  - Dry overnight
  - Bake in oven 150°C 30min
- Stripping PMMA
  - Immerse in Acetone
- Cleaning
  - 3min IPA
  - Dry with N_2

Methods – Graphene Channel Lithography

- AZ 5214E
  - Spincoat 500rpm 5s + 4000rpm 50s
- Soft bake
  - 110°C 2min
- Mask Align & Expose
  - 180mJ/cm^2
- Develop in AZ 326 MIF
  - 105s
- Stop Process in DI water

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- AZ 5214E
  - Spincoat 500rpm 5s + 4000rpm 50s
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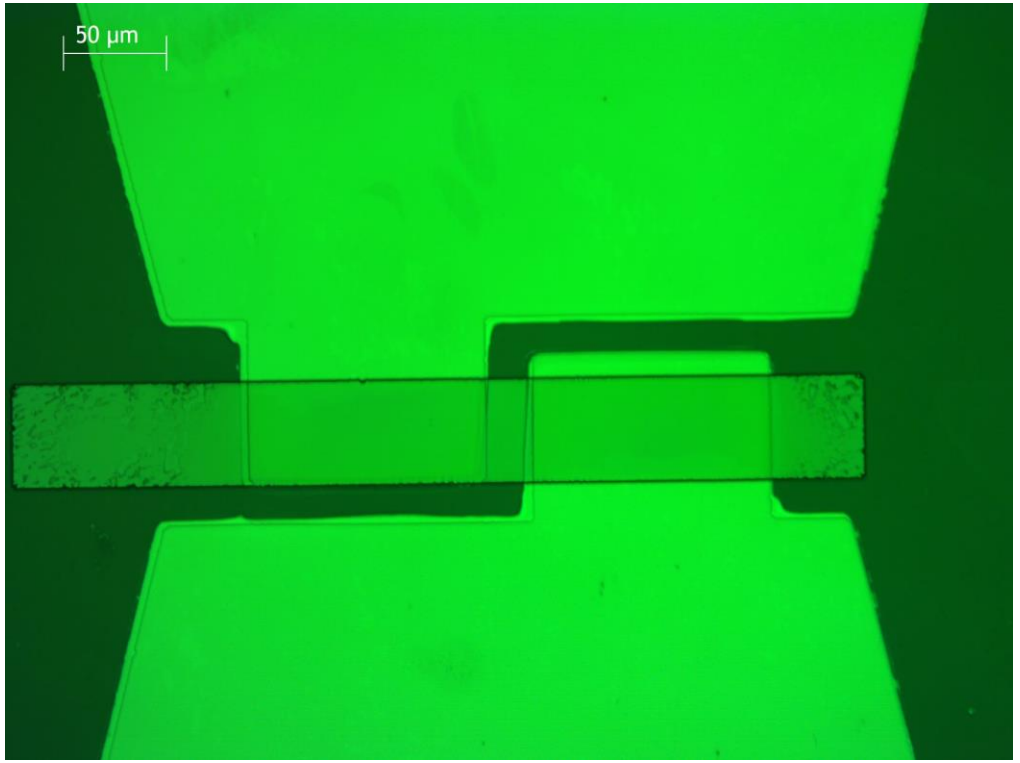

Figure 11: Positive Photomask after Development

Methods – Graphene Channel Etchback

- Reactive Ion Etching (RIE)
  - 80sccm oxygen
  - 57mtorr in chamber
  - 80W O_2 plasma (60s)
- Remove resist
  - 3min Acetone
- Cleaning
  - 3min IPA
  - Dry with N_2

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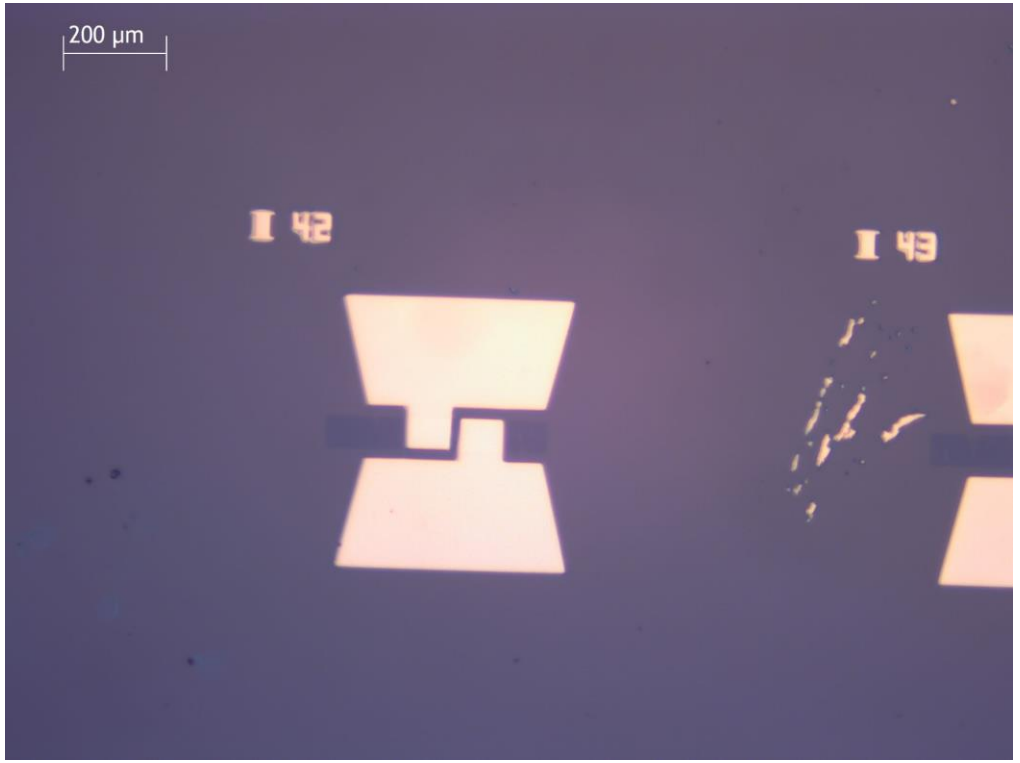

Figure 12: Graphene Channel after RIE on top of Molybdenum Drain and Source Contacts

Methods – Graphene Channel Etchback

- Reactive Ion Etching (RIE)
  - 80sccm oxygen
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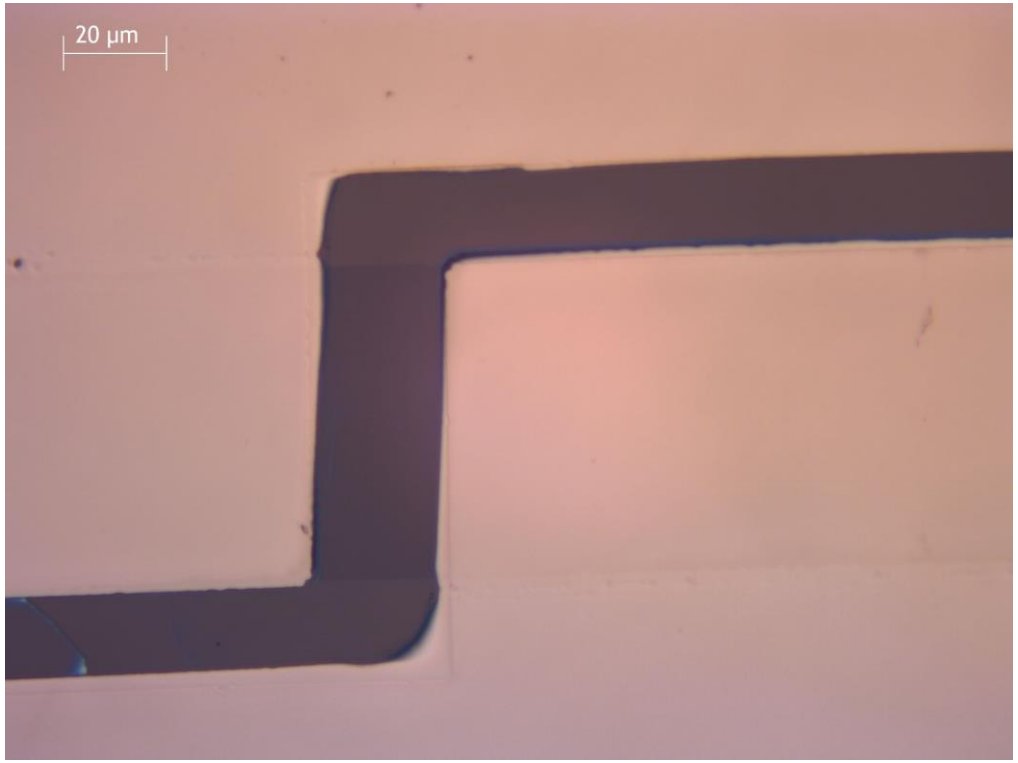

Figure 13: Graphene Channel after RIE on top of Molybdenum Drain and Source Contacts (zoomed)

Results

- Introduction
- IV-Curve Analysis
- Mobility Calculations
- Summary

Results – Introduction

This presentation evaluates the performance of a fabricated GFET using IV-Curve analysis.

Key Focus:

- Study the changes in slope of the IV-Curve under varying sweep voltages.
- Identify shifts in the Dirac point or the Neutrality point and their implications on GFET´s behavior.
- Understand the electron and hole mobilities.

Results – IV-Curve Analysis

1. The **Device III-25** was chosen for the IV-Curve measurement, and its drain, source, and gate terminals were connected using probes. A semiconductor parameter analyzer (KEITHLEY 4200-SCS) was employed for the measurements.
2. Gate-to-Source voltage $(\boldsymbol{V_{GS}})$ was swept from -30V to 70V, using a step size of 0.5V, which resulted in 201 measurement points. The drain current $(\boldsymbol{I_{DS}})$ was recorded throughout the sweep.

Results – IV-Curve Analysis

3. The IV-Curve also displays varying slopes under different sweep voltages. These slopes are critical for determining the charge carrier mobilities. Using the linear region method, the charge carrier mobilities for electrons $(\boldsymbol{\mu_e})$ and holes $(\boldsymbol{\mu_h})$ were extracted from the steepest points of the curve. The positive slope corresponds to electron mobility, while the negative slope represents hole mobility.

Results – IV-Curve Analysis

4. In an ideal GFET, the IV-Curve should exhibit a charge neutrality point, also known as the Dirac point, centered at $\boldsymbol{V_{GS}=0V}$. However, due to p-doping of the silicon substrate and the effects of impurities introduced during fabrication, the Dirac point in this experiment was shifted to $\boldsymbol{V_{GS}=4V}$. This shift is a common occurrence in GFETs fabricated on doped substrates, as the doping alters the Fermi level and influences the charge distribution in the graphene channel.

Results – IV-Curve Analysis

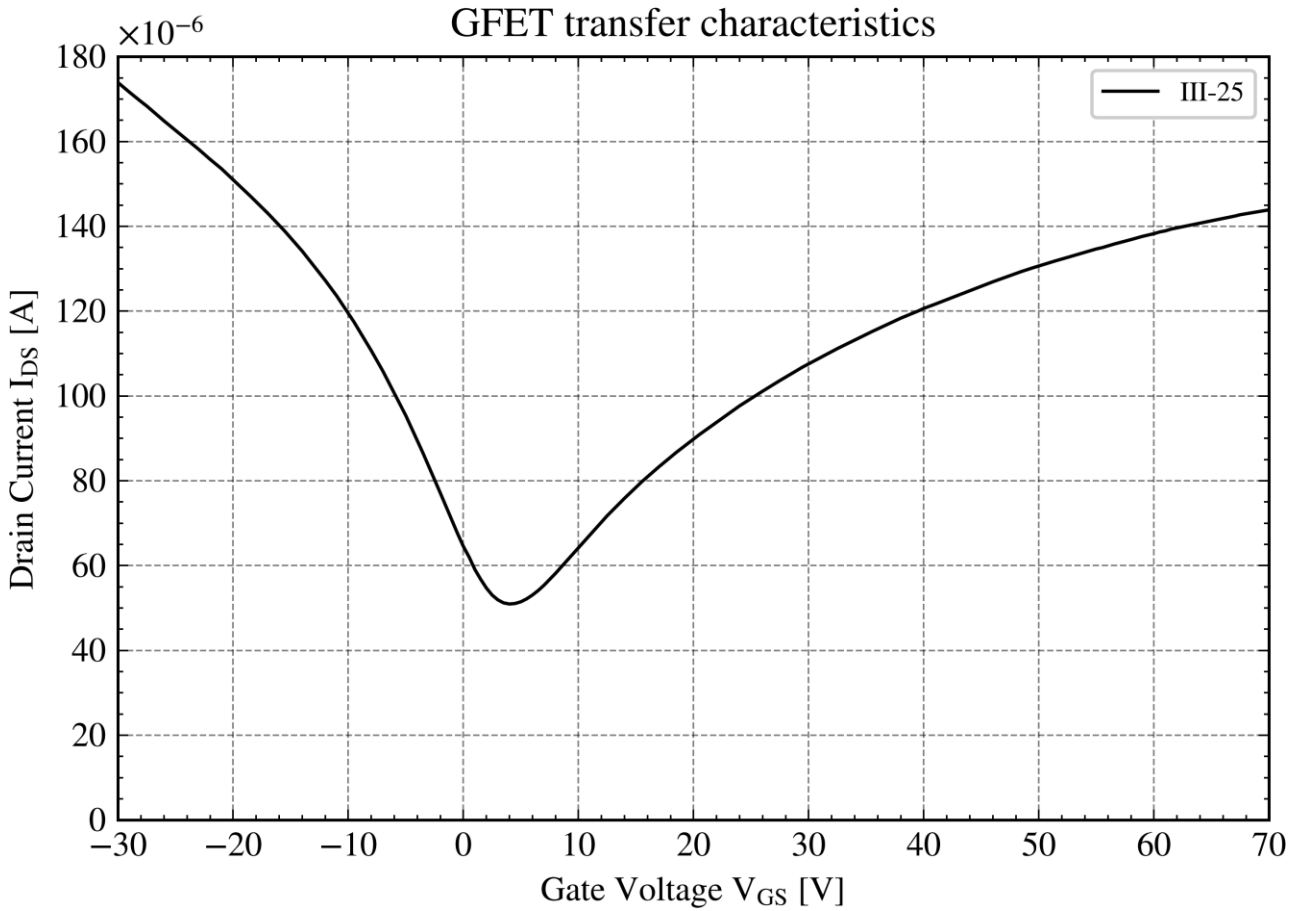

Figure 14: IV-Characteristics of GFET III-25

Results – IV-Curve Analysis

5. The IV-Curve also displays varying slopes under different sweep voltages. These slopes are critical for determining the charge carrier mobilities. Using the linear region method, the charge carrier mobilities for electrons (μ_e) and holes (μ_h) were extracted from the steepest points of the curve. The positive slope corresponds to electron mobility, while the negative slope represents hole mobility.

   Accurately capturing these values is essential for assessing the performance of the GFET, as mobility directly impacts the device's speed and overall efficiency. The higher the mobility, the better the device's ability to transport charge carriers, making it more efficient for high-frequency applications.

Results – Mobility Calculations

1. Charge carrier mobility ($\boldsymbol{\mu_e}$ for electrons and $\boldsymbol{\mu_h}$ for holes) was extracted from the IV-Curve using the linear region method.
2. Mobility: The steepest slopes were found by calculating the derivative of the IV-Curve. The largest positive slope represents electron conduction, while the largest negative slope represents hole conduction. This happens because, in GFETs, the conduction and valence bands are symmetrical, leading to positive slopes for electrons and negative slopes for holes.

Results – Mobility Calculations

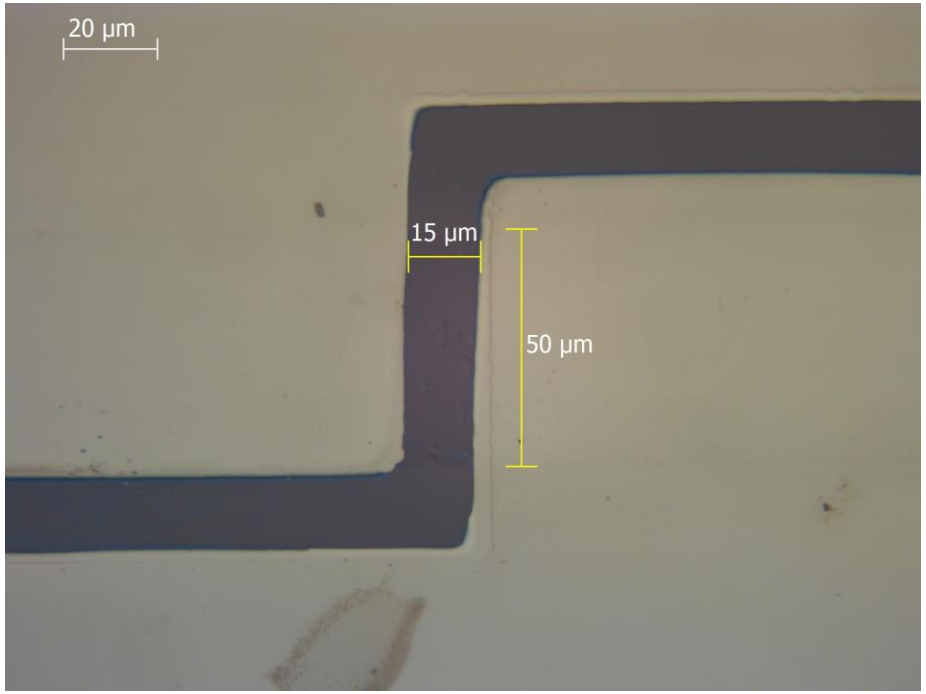

Figure 15: Channel Geometry of GFET III-25

Name	Variable	Value
Length	L	15µm
Width	W	50µm
SiO_2 thickness	t_{ox}	85nm
Resistivity	R	1-20Ω/cm
Dielectric constant of SiO_2	ε	3.9
Dielectric constant	ε_{ox}	$8.85x10^{12}$ As/(Vm)

Table 1: Properties of GFET III-25

Results – Mobility Calculations

3. Electron Mobility (μ_e) :

The positive slope is extracted from the IV- Curve at $V_{GS} = 9\ V$ to $8.5\ V$ with I_{DS} ranging from $59.65\ \mu A$ to $61.21\ \mu A$.

Slope = g_m (Transconductance) = $\frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{61.21\mu A - 59.65\mu A}{9V - 8.5V} = 3.12\ \mu A/V$

Results – Mobility Calculations

Furthermore, the geometrical oxide capacity C_{ox} can be calculated with the GFET's specifications taken from the properties table

$$C_{ox} = \frac{\varepsilon \cdot \varepsilon_0}{t_{ox}} = \frac{3.9 \cdot 8.8542 \times 10^{-12}\ As/Vm}{85 \times 10^{-9} m} = 4.0625 \times 10^{-8}\ F/cm^2$$

Finally, the electron mobility can be determined by substituting the values into the following equation

$$\mu_e = \frac{g_m \cdot L}{V_{DS} \cdot W \cdot C_{ox}} = \frac{3.12 \mu A/V \cdot 15 \mu m}{100 mV \cdot 50 \mu m \cdot 4.0625 \times 10^{-8} F/cm^2} = \boldsymbol{229.78\ cm^2/Vs}$$

Results – Mobility Calculations

4. Hole Mobility (μ_h) :

The negative slope is extracted from the IV- Curve at $V_{GS} = -1.5\ V$ to $-2\ V$ with I_{DS} ranging from $77.09\ \mu A$ to $73.86\ \mu A$.

Slope = g_m (Transconductance) = $\frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{77.09\mu A - 73.86\mu A}{-1.5V + 2V} = 6.46\ \mu A/V$

The hole mobility can be determined using the following formula

$$\mu_h = \frac{g_m \cdot L}{V_{DS} \cdot W \cdot C_{ox}} = \frac{6.46\mu A/V \cdot 15\mu m}{100mV \cdot 50\mu m \cdot 4.0625\times10^{-8} F/cm^2} = \boldsymbol{477.32\ cm^2/Vs}$$

Results – Key Points

1. Electron Mobility ($\boldsymbol{\mu_e}$): **229.78** $cm^2/(V \cdot s)$
2. Hole Mobility ($\boldsymbol{\mu_h}$): **477.32** $cm^2/(V \cdot s)$

Key Observations:

- Hole mobility is higher than electron mobility, likely due to contamination.
- Dirac point shifted to positive values due to substrate doping.

Results - Factors Influencing Performance

Several factors impact the performance of GFETs:

- **Substrate Doping**: p-doped Si substrate shifts the Dirac point.
- **Impurities**: Manufacturing contamination affects overall device characteristics.
- **Sweep Voltages**: Variations in voltage can alter the IV-Curve slopes.
- **Gate Current Threshold**: Excessive gate current can cause device breakdown.

Discussion and Improvements

The shift in the Dirac point and the difference in electron and hole mobility indicate areas for process improvement:

- Cleaner fabrication environments would reduce contamination and improve device performance.
- Better control of the doping process would help keep the Dirac point closer to 0V.
- Refinement in material quality and reduction in contamination would likely enhance the mobility characteristics.

Conclusion

- Molybdenum is an interesting metal
- Promising results
- Good position of Dirac-Point
- Possible improvements
  - Layer of Al_2O_3
  - Encapsulate in h-BN

Thank you for your attention!

Graphene and h-BN

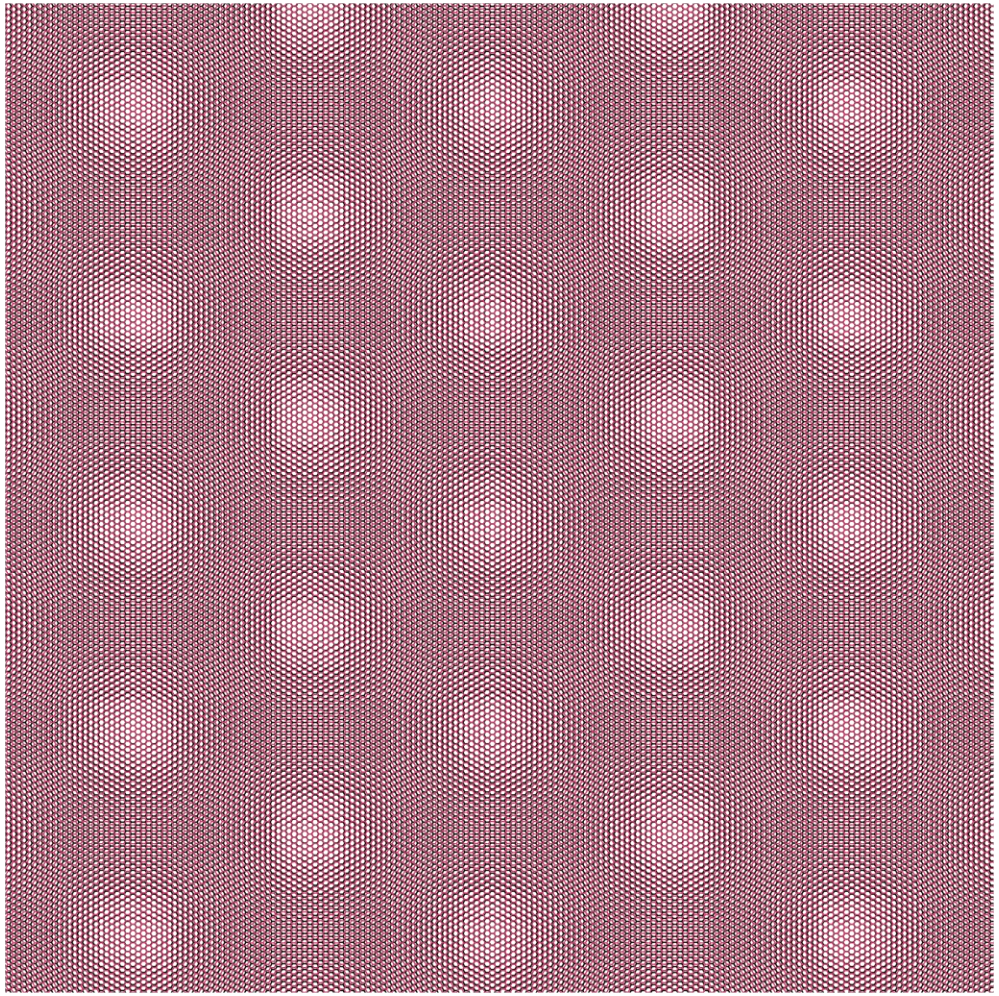

Figure 16: Graphene (black) and h-BN (purple) Chrystal Mismatch of 1.6% illustrated

Graphene and h-BN

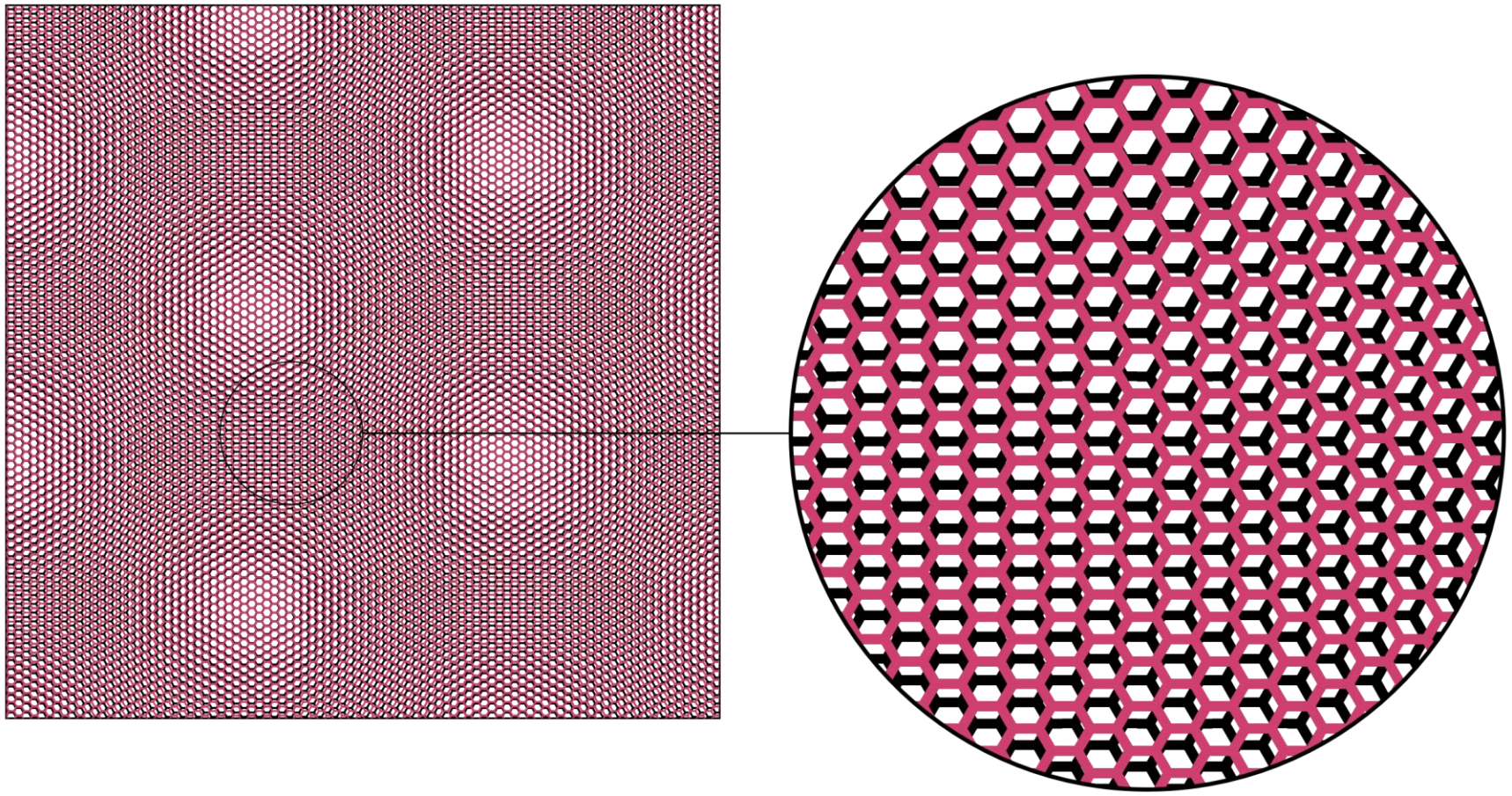

Figure 17: Graphene (black) and h-BN (purple) Christal Mismatch of 1.6% illustrated (zoomed)

GFET vs MOSFET

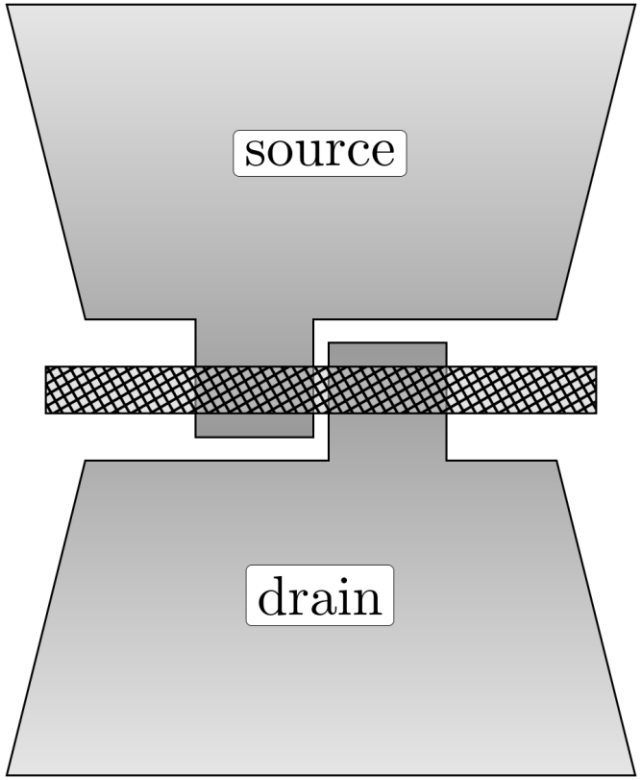

Figure 18: GFET Top View

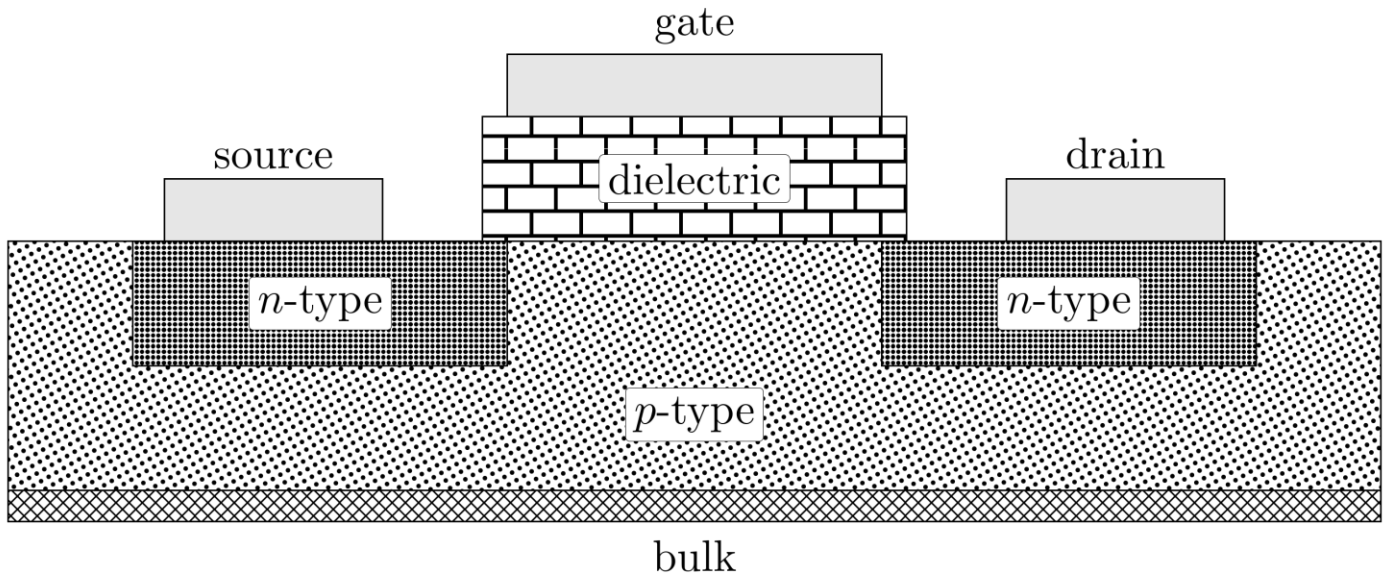

Figure 19: General MOSFET Side View