Fabrication and Characterisation of a Graphene Field Effect Transistor

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***Abstract*—In this paper, the process and included steps of fabricating a simple backgated Graphene Field Effect Transistor with Molybdenum source and drain contacts will be described in detail. At the end, the transistors will be characterised in order to determine the performance in relation to the charge carrier mobilities. (1425103)**

***Index Terms*—Graphene, GFET, Mobility, Characterization, Manufacturing Process, E-Beam PVD**

I. Introduction - 1793417

Graphene possesses several incredible abilities. Since graphene was shown to be a stable two-dimensional material in ambient conditions, there has been an increasing amount of interest in this single layer of carbon atoms with a hexagonal lattice structure exfoliated from graphite [1]. For high-speed electronics, especially field-effect transistors (FETs), graphene has been seen as a viable option because of GFET's high carrier mobility even at ambient temperature. Its remarkable mechanical, electrical, and thermal capabilities have attracted a lot of interest. The creation of graphene field effect transistors (GFETs) is notable for its promise in next- generation nano-electronics among its numerous use cases. Although graphene is used as the channel material instead of silicon or other semiconductors, GFETs function generally on the same principles as traditional field-effect transistors (FETs). With features including high electron and hole mobility, adjustable carrier concentrations and chemical sensitivity, GFETs are a good fit for flexible devices, high-speed electronics, and sensors. Industry has been implementing consecutive transistor down-scaling to create quicker and more affordable devices, while using fewer resources, thereby fulfilling Moores Law, for about fifty years. But in order to continue this progress once the physical constraints of downscaling are finally reached, a lot of research is being done on substitute materials. Many studies have been drawn to materials that have greater mobility and can be downscaled beyond silicon. The recently found two-dimensional graphene is a good option to replace the channel material in traditional field effect transistors due to its superior electrical characteristics [2]. The properties, manufacturing processes, and uses of graphene are briefly covered. Its three distinguishing features (properties, production methods, and applications of graphene) set it apart from other contenders for quicker and more compact electronics in the future. The ultra-high inherent mobility of graphene is its primary, and possibly most significant, priority. Graphene's maximum mobility limit at room temperature has been demonstrated to be currently higher than that of silicon material [3]. The second benefit is that graphene is a perfect material for the channel material in integrated circuit technology. Characterization and analysis of the findings to look at the efficiency of the manufacturing process and the transport properties of our products. We are fabricating the GFET in beforehand. In actuality, device research and monitoring of different fabrication stages depend heavily on characterization. For example, current-voltage measurements offer useful information for the extraction of electrical properties such as mobility. Here we characterize the transistor to know about how it works. The goal of this project is to serve as a success guide to ascertain the characterization of back-gate field effect transistors.

II. Methods - 1425103

In the following, the process of manufacturing a GFET is described in detail while important key points are pointed out.

A. Wafer Preparation

A $6\,\mathrm{in}$ Si wafer ($t = 675\,\mu\mathrm{m}$, Boron p-doped with $85\,\mathrm{nm}$ SiO_2, R $\approx$ $1\,\Omega$ to $20\,\Omega$) was used as a starting material. The oxide on the backside of the wafer got removed with hydrofluoric acid and a metal was deposited here. This forms the backgate of the devices and is used when contacted on a probe station. Then the wafer was cut into dies that fit the jigs in the machines used during the manufacturing processes, in this case $2\,\mathrm{cm} \times 2\,\mathrm{cm}$. After that, the dies got cleaned thoroughly in Acetone for $5\,\mathrm{min}$ and $3\,\mathrm{min}$ in Isopropanol (IPA) using an ultrasonic bath for both cleaning processes. Following that, the samples were dried with Nitrogen (N_2).

B. Fabrication of Drain and Source Structures

To manufacture the drain and source contacts of the GFET the lift-off technique was used. A layer of $150\,\mathrm{nm}$ Molybdenum (Mo) is used as the surface and contacting material. A $10\,\mathrm{nm}$ thin layer Titanium (Ti) served as a an adhesive between the SiO_2 and the Mo [4].

1) Lithography: To prepare the samples for masking, a negative photoresist (AZ® nLOF 2070) was applied in a spin-coating process to the surface of the samples. The process of applying the photoresist consisted of $500\,\mathrm{rpm}$ for $5\,\mathrm{s}$ and $3000\,\mathrm{rpm}$ for $50\,\mathrm{s}$, leading to a layer thickness of $7\,\mu\mathrm{m}$. Then a softbake was carried out, at $100\,^{\circ}\mathrm{C}$ for $60\,\mathrm{s}$, on the applied photoresist in order to decrease the residual solvent concentration [5]. This was done to improve resist adhesion to the substrate surface before the sample was exposed to UV-light through the mask with an energy of $180\,\mathrm{mJ/cm^2}$ [5]. The result was sufficient, so the photoresist was post baked at $110\,^{\circ}\mathrm{C}$ for $90\,\mathrm{s}$ to prepare it for development. Following that, the resist film was developed using AZ® 726 MIF for $70\,\mathrm{s}$ under gentle stirring. The process was stopped by immersing the sample in deionized (DI) water for at least $1\,\mathrm{min}$. The result is shown in Figure 1.

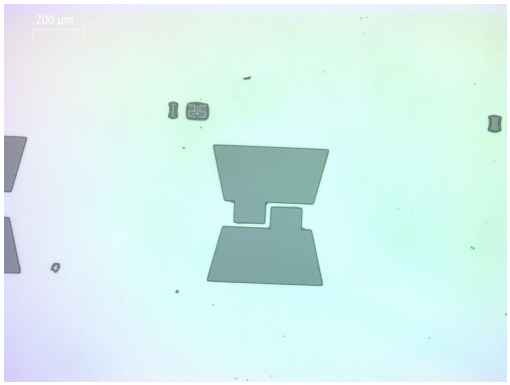

Figure 1. Negative Photomask of the Drain and Source Contacts of a Single Transistor After Development

By closer inspection in Figure 2 an undercut of the photoresist was developed during the process. This later on played an important roll during the liftoff process, because no metal deposition was possible under the protruding parts due to the undercut of the photoresist.

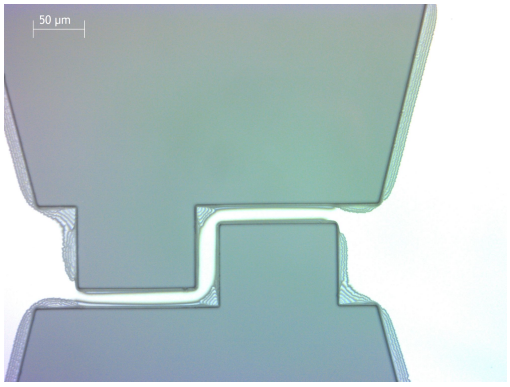

Figure 2. Undercut of the Photoresist on the Edges of the Drain and Source Structures

2) Metal Finger Deposition: In this step, electron beam (e-beam) physical vapor deposition was used in order to evaporate and deposit the metals on the sample. After placing the samples into the jig of the machine and lowering the pressure to $7 \times 10^{-6}\,\mathrm{mbar}$ they were cleaned with an argon (Ar) plasma. Following that using e-beam evaporation, Ti was deposited at a rate of $0.2\,\mathrm{nm/s}$ and Mo at a rate of $0.5\,\mathrm{nm/s}$, leading to a final thickness of $10\,\mathrm{nm}$ and $150\,\mathrm{nm}$ respectively.

3) Liftoff Process: In order to remove the excess metals from the sample, the photoresist had to be lift off the surface of the SiO_2 oxide. This was carried out by immersing the sample into Acetone. With the help of steady stirring, the remaining photoresist detached leaving just the metal fingers, as seen in Figure 3, which will later be used as the drain and source contacts of the device. Following that, the sample was then put into IPA for $3\,\mathrm{min}$ in order clean off the acetone and dried afterwards using N_2.

Figure 3. Source and Drain Structure after Liftoff

C. Graphene Channel Fabrication

Then, the graphene channels were formed. For the sake of uniformity, the use of self fabricated graphene was omitted and CVD grown graphene got used. In order to perform the forming of the channels, the graphene had to be prepared and coated with a polymethylmethacrylat (PMMA). It acted as a carrier to stabilize the graphene during the bubbling transfer.

1) Preparation of the Material: The manufactured graphene was grown on a copper foil. It was carefully cut into $2\,\mathrm{cm} \times 2\,\mathrm{cm}$ pieces and then carefully flattened so it was able stick to the vacuum chuck of the spincoater.

2) Carrier Application: In order to properly transfer the graphene to the wafer, a thin layer of PMMA was applied to the graphene on the copper sheet carrier. For this, AR-P 649.04 was applied using a spin coating process at $2000\,\mathrm{rpm}$ for $50\,\mathrm{s}$. A bake on a hotplate was carried out for $3\,\mathrm{min}$ at $80\,^{\circ}\mathrm{C}$. The edges of the coated coated copper sheet were cut. Through this, the graphene layer later can be detached from the copper during the bubbling transfer.

3) Bubbling Transfer: The process was carried out in a solution of $100\,\mathrm{g}$ DI water mixed with $1\,\mathrm{g}$ sodium hydroxide (NaOH). It became easier in the process to work with graphene in containers not made out of glass. This way the graphene will repel from the edges of the container and did not hard-stick to them. A graphite rod acted as an electrode that was immersed into the solution. The sheet of copper was

held with tweezers acting as a cathode. The electrodes were connected to a power supply set to $3.5\,\mathrm{V}$ CV. The entire process of the bubbling transfer in detail can be read in [6]. By lowering the sheet slowly into the solution, small bubbles were forming, indicating that the process was taking place. When the tweezers were closely above the surface the sheet is turned $180°$ with the help of a second pair and the process was continued until the graphene was fully detached from the copper foil. Subsequently the graphene sheet was transferred, with a surgical grade spoon, into two separate containers for cleaning, $10\,\mathrm{min}$ in each container. From there, the graphene sheet was transferred from the DI water to the sample. The graphene then was let dry overnight by itself and baked in an oven the next day at $150\,°\mathrm{C}$ for $30\,\mathrm{min}$ to smoothen the PMMA and respectively the graphene beneath it. After letting the sample cool down, the PMMA was stripped from the graphene by immersing it into acetone while gently stirring the beaker. The acetone then was cleaned off by putting the sample for $3\,\mathrm{min}$ into IPA and dried with N_2 afterwards. It is not advised to use an ultrasonic bath for these and further steps, as this will destroy the graphene layer.

4) Lithography: After cleaning with acetone and IPA, another photoresist was applied to the sample. This will pattern the graphene channels. As a resist, AZ® 5214E was used. It was applied using a spincoating process at $500\,\mathrm{rpm}$ for $5\,\mathrm{s}$ and $4000\,\mathrm{rpm}$ for $50\,\mathrm{s}$. These parameters resulted in a thickness of $1.4\,\mu\mathrm{m}$. A soft bake was performed for $2\,\mathrm{min}$ at $110\,°\mathrm{C}$. The sample was exposed through a mask, patterning the graphene channels, to UV-light with an Energy of $180\,\mathrm{mJ/cm^2}$. A post exposure bake was not necessary as it would have inverted the photomask [7]. Following exposure, the mask was developed using AZ® 326 MIF for $105\,\mathrm{s}$ under gentle stirring and afterwards stopped in DI water. Figure 4 shows the positive photoresist that covers the graphene channel structure after development.

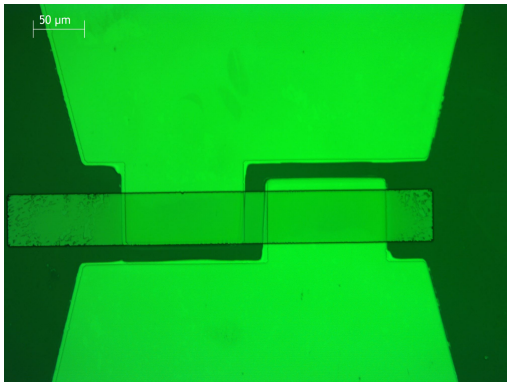

Figure 4. Positive Photomask after Development

5) Etchback: In order to remove the access graphene, reactive ion etching (RIE) was used. With an oxygen flow rate of $80\,\mathrm{sccm}$ the pressure in the chamber of the RIE tool was lowered to $57\,\mathrm{mtorr}$. The etchback process itself involved an O_2 plasma with an electric field power of $80\,\mathrm{W}$. The sample was exposed for $60\,\mathrm{s}$ to the plasma. Following the etchback, the resist had to be removed. This was carried out by immersing the sample for $3\,\mathrm{min}$ in acetone and afterwards washing the acetone of with IPA for another $3\,\mathrm{min}$. As a last step the sample was blown dry using N_2. The result is shown in Figure 5. There, the formed graphene channel is clearly visible, covering the fingers of the source and drain structure.

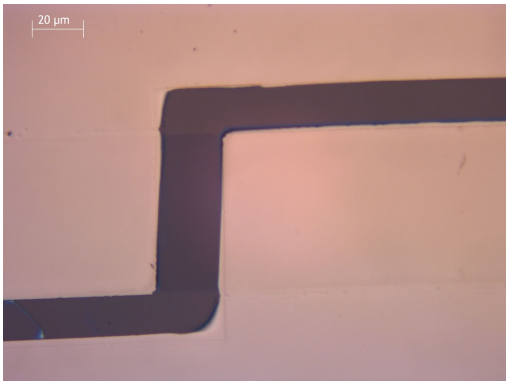

Figure 5. Graphene Channel after RIE on top of Molybdenum Drain and Source Contacts

III. Result - 1774012

This section covers the performance and characteristics of the fabricated GFETs. A probe station with four needles (SMU1, SMU3, and SMU4) and a semiconductor parameter analyzer (KEITHLEY 4200-SCS) were used to contact the drain and source structures.

A. IV-Curve

The IV-Curve is an important plot to determine the transfer characteristics of a GFET. It can be used to extract the electron and hole mobility, which is a measure of the device's performance rather than directly representing its conductivity. Ideally, the IV-Curve should have a charge neutrality point (Dirac point) centered at a gate voltage $V_{GS} = 0\,\mathrm{V}$, but in practice, it will be shifted due to doping of the substrate it was manufactured on and the oxide used [8]. Since a p-doped Si wafer was used, the Dirac point is expected to shift towards positive gate-to-source voltages due to the Fermi level shift. Impurities and auto doping of the material from manufacturing processes also affect the Dirac point, shifting it to more positive values, which worsens the overall device characteristics. It is important to note that the slope of the IV-Curve changes under varying sweep voltages. The gate voltage V_{GS} is swept here, and under the influence of magnetic fields, this could further impact the curve [9].

The charge carrier mobilities for electrons and holes (μ_e, μ_h) were extracted using the linear region method at the steepest points of the curve, as seen in Figure 6. These values, particularly in graphene, are highly dependent on the manufacturing quality. Therefore, avoiding contamination during the manufacturing process is crucial to ensure consistency [10]. In Table I the configuration of the parameter analyzer

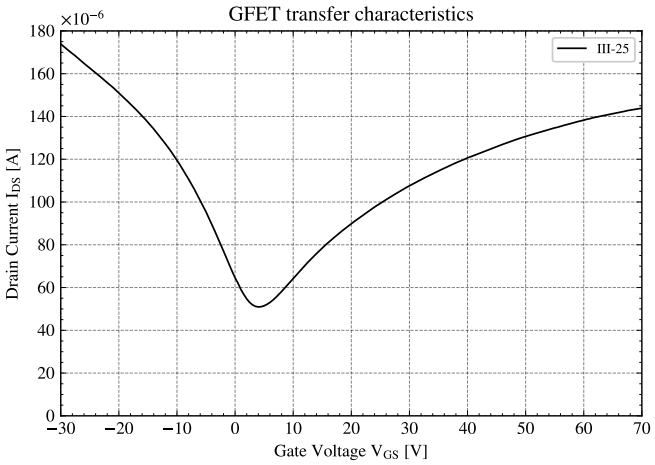

Figure 6. IV-Characteristics of a Manufactured GFET

Table I
CONFIGURATION OF SMU PROBES CONNECTED TO DUT

Signal	Voltage	Step Size	Current Limit
Gate	−30 V to 70 V	0.5 V	10 mA
Drain	0 V	Bias only	100 mA
Source	100 mV	Bias only	100 mA

is displayed, showing the parameters used to characterize the GFETs.

A step size of 0.5 V was chosen, resulting in 201 measurement points. A finer step size was possible but not feasible in this case since smaller voltage steps would significantly increase acquisition time. The current flowing through the drain and source contacts of the GFET was measured to ensure that the normal operating current was within a certain threshold and to verify if the device was functional. Typically, currents at the gate should not exceed a few µA for the GFET to be fully functional. If the gate current increases significantly, there is a high probability of breakdown due to excessive electric field strength. This results in a breakdown of the SiO_2 layer, causing a short circuit from the copper back gate to the channel through the doped Si substrate.

B. Mobility Calculation

As mentioned in the previous section, μ_e and μ_h were extracted using Figure 6. The Dirac point of the measured GFET is at $V_{GS} = 4\,\mathrm{V}$ and $I_{DS} = 50.93\,\mu\mathrm{A}$ (Note: The current is rounded to two decimal places for practical accuracy). Under ideal conditions, the electron and hole mobility of graphene on SiO_2, $\mu_{Gr\_on\_SiO_2}$ can reach values as high as $100\,000\,\mathrm{cm^2/(V\,s)}$ to $200\,000\,\mathrm{cm^2/(V\,s)}$ for electrons and holes [3].

In Figure 7 the channel of the measured GFET is depicted, and the data used to calculate the mobilities are shown in Table II.

In general, the electron mobility μ_e of a GFET can be calculated using the Drude model [8]:

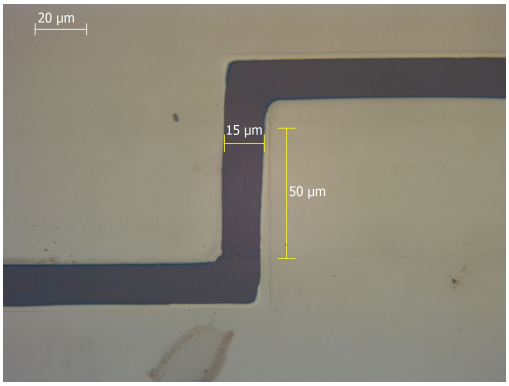

Figure 7. Channel Geometry of GFET III-25

Table II
PROPERTIES OF GFET III-25

Name	Variable	Value
Length	L	15 µm
Width	W	50 µm
SiO_2 thickness	t_{ox}	85 nm
Resistivity	R	1 - 20 Ω/cm
Dielectric constant of SiO_2	ε	3.9
Dielectric constant	ε_0	$8.8542 \times 10^{-12}\,\mathrm{A\,s/(V\,m)}$

$$\mu_e = \frac{I_{DS} \cdot L}{V_{DS} \cdot W \cdot C_{ox} \cdot (V_{GS} - V_D)} \tag{1}$$

with

$$g_m = \frac{I_{DS}}{(V_{GS} - V_D)} \tag{2}$$

follows

$$\mu_e = \frac{g_m \cdot L}{V_{DS} \cdot C_{ox} \cdot W} \tag{3}$$

for the mobility. Transconductance g_m can also be calculated as

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{I_{DS,a} - I_{DS,b}}{V_{GS,a} - V_{GS,b}} \tag{4}$$

when the slope of the IV-Curve is considered. Furthermore, the geometrical oxide capacity C_{ox} for the given parameters can be calculated as

$$\begin{aligned} C_{ox} = \frac{\varepsilon \cdot \varepsilon_0}{t_{ox}} &= \frac{3.9 \cdot 8.8542 \times 10^{-12}\,\frac{\mathrm{A\,s}}{\mathrm{V\,m}}}{85 \times 10^{-9}\,\mathrm{m}} \\ &= 4.0625 \times 10^{-8}\,\frac{\mathrm{F}}{\mathrm{cm^2}} \end{aligned} \tag{5}$$

The mobility of charge carriers depends on the slope of the IV-Curve of the GFET in Figure 6. The delta values for I_{DS} and V_{GS} were calculated based on the measurement points acquired from the sweep of V_{GS}. From the derivative of the IV-Curve, the steepest slopes were identified. The highest absolute slope corresponds to positive values for electrons and negative values for holes because, in GFETs the conduction band and

valence band are symmetric, leading to positive slopes for electron conduction and negative slopes for hole conduction. The positive slope was extracted at $V_{GS,e} = 8.5\,\mathrm{V}$ for electrons, and the negative slope was extracted at $V_{GS,h} = -2\,\mathrm{V}$ for holes. Thus μ_e and μ_h can be calculated as follows:

$$\begin{aligned}\mu_h &= \frac{(I_{DS,h,a} - I_{DS,h,b}) \cdot L}{V_{DS} \cdot W \cdot C_{ox} \cdot (V_{GS,h,a} - V_{GS,h,b})} \\ &= \frac{(77.0967\,\mu\mathrm{A} - 73.8648\,\mu\mathrm{A}) \cdot 15\,\mu\mathrm{m}}{100\,\mathrm{mV} \cdot 50\,\mu\mathrm{m} \cdot 4.0625 \times 10^{-8}\,\frac{\mathrm{F}}{\mathrm{cm}^2} \cdot (-1.5\,\mathrm{V} + 2\,\mathrm{V})} \\ &= 477.3256\,\frac{\mathrm{cm}^2}{\mathrm{V\,s}}\end{aligned} \tag{6}$$

$$\begin{aligned}\mu_e &= \frac{(I_{DS,e,a} - I_{DS,e,b}) \cdot L}{V_{DS} \cdot W \cdot C_{ox} \cdot (V_{GS,e,a} - V_{GS,e,b})} \\ &= \frac{(61.2130\,\mu\mathrm{A} - 59.6572\,\mu\mathrm{A}) \cdot 15\,\mu\mathrm{m}}{100\,\mathrm{mV} \cdot 50\,\mu\mathrm{m} \cdot 4.0625 \times 10^{-8}\,\frac{\mathrm{F}}{\mathrm{cm}^2} \cdot (9\,\mathrm{V} - 8.5\,\mathrm{V})} \\ &= 229.7791\,\frac{\mathrm{cm}^2}{\mathrm{V\,s}}\end{aligned} \tag{7}$$

IV. Discussion - 1774012

The results of this study highlight several critical observations about the performance of the fabricated GFETs. The discrepancy in electron and hole mobility was particularly notable. The measured electron mobility μ_e was found to be $229.78\,\mathrm{cm}^2/(\mathrm{V\,s})$, while the hole mobility μ_h was $477.32\,\mathrm{cm}^2/(\mathrm{V\,s})$. Although the lower electron mobility relative to hole mobility might seem unexpected, this can be attributed to the differences in the effective masses of the charge carriers. The smaller mass of electrons generally results in higher mobility, but in this case, the contamination introduced during the manufacturing process likely played a role in suppressing the expected electron mobility.

Further investigation into cleanroom techniques and material handling could mitigate such contamination and improve the consistency of results. In terms of overall device performance, the GFET exhibited a relatively good Dirac point at $V_{GS} = 0\,\mathrm{V}$, albeit with a slight shift as anticipated due to the p-doped Si substrate. This shift aligns with theoretical expectations and supports the assumption that the device is functioning as intended. However, the mobility values, while adequate for the theoretical purposes of this study, are lower than what might be expected for high-performance graphene devices. This suggests that although the fabrication process was largely successful, further refinement in material quality and reduction in contamination would likely enhance the mobility characteristics.

V. Conclusion - 1425103

The processes of fabricating a Molybdenum based GFET in a cleanroom environment was described and the characterization of the sample was provided in this paper. One advantage of Molybdenum for laboratory environments like universities is that it is much harder than for example Gold, which is usually used for contacting materials because of its anti-corrosive properties. It was observed that during testing procedures in the probe station no transistors were damaged through mechanical abrasion due to the hardness of the material as displayed in Figure 8.

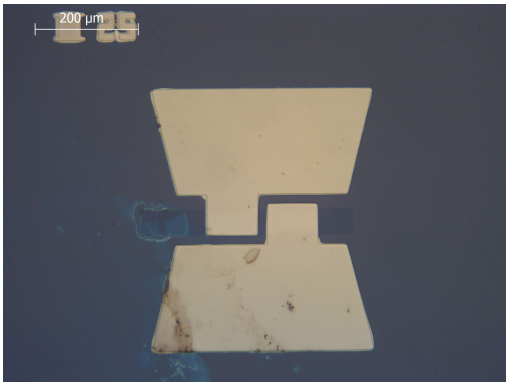

Figure 8. Measured GFET without Material Abrasion due to the Hardness of Molybdenum

This came at the cost of conductivity, Molybdenum is around $50\,\%$ less conductive than Gold ($2.06 \times 10^5\,\mathrm{S/cm}$ in contrast to $4.11 \times 10^5\,\mathrm{S/cm}$). To further improve the characteristics of the GFET devices on the sample die, the same mask that was used to pattern the graphene channels could be used to apply a layer of aluminium oxide (Al_2O_3). This way, a decrease of charge carrier mobilities in the graphene over time can be prevented.

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