High-Frequency Response of a JFET Amplifier

Mainak Roy
University of Siegen
Chair of Analogue Circuits and Image Sensors

May 19, 2025

Objective

To simulate and analyze the high-frequency behavior of a JFET amplifier using LTspice. The aim is to determine the voltage gain across a frequency sweep and identify the $-3\,\mathrm{dB}$ cutoff point.

Circuit Description

The circuit consists of a J310 N-channel JFET configured in a common-source amplifier topology. Key components include:

- **R1, R2**: Load and bias resistors
- **R3, R4**: Source and gate biasing
- **C1, C2, C3**: Coupling and bypass capacitors
- **V1**: DC supply ($15\,\mathrm{V}$)
- **V2**: AC signal source ($0.1\,\mathrm{V}$ peak)

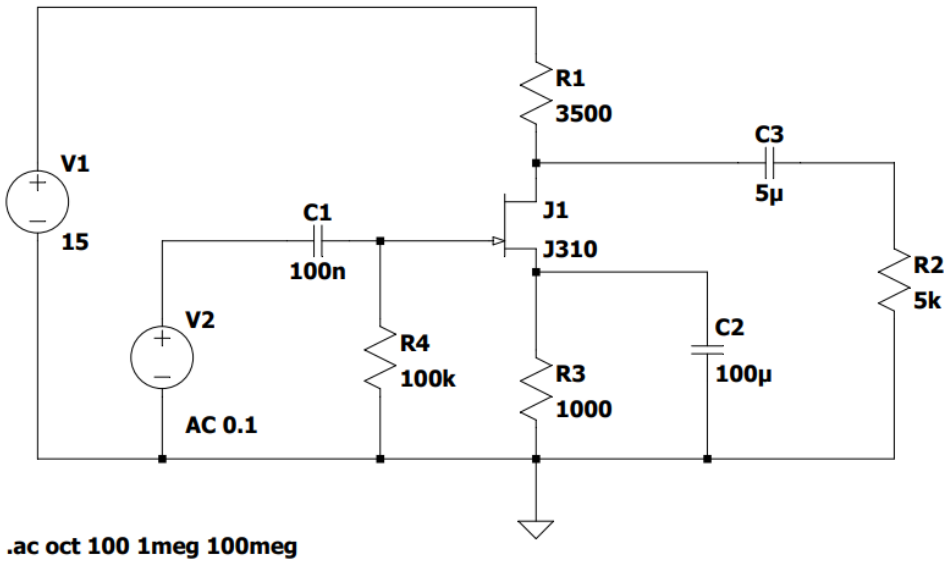

Figure 1: JFET Amplifier Circuit in LTspice

Simulation Setup

The AC analysis was conducted over a frequency range from 1 MHz to 100 MHz with 100 points per octave:

```
.ac oct 100 1meg 100meg
```

The gain was measured as the ratio $V_{\text{out}}/V_{\text{in}}$ and plotted in dB.

Results and Analysis

AC Gain Plot

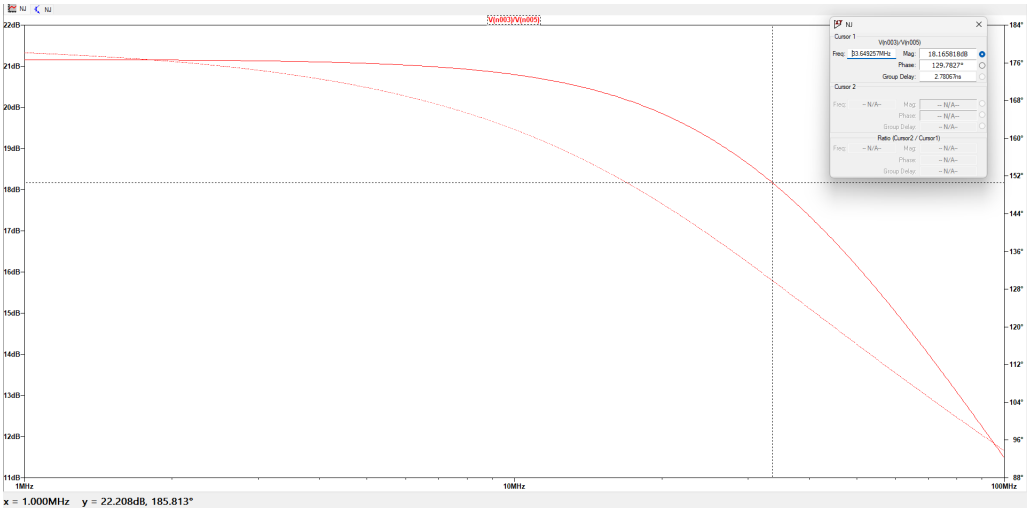

Figure 2: JFET Amplifier Gain vs Frequency

Voltage Gain and Cutoff Point

The amplifier shows a flat gain at lower frequencies, with roll-off starting due to parasitic capacitances.

- **Maximum Gain**: 21.16 dB $\Rightarrow$ Voltage Gain $\approx 11.4\times$
- **Cutoff Gain** (-3 dB): 18.16 dB
- **Cutoff Frequency**: 33.65 MHz
- **Gain at Cutoff**: 18.17 dB

Voltage Gain Calculation

The gain in **decibels (dB)** for voltage is defined as:

$$\text{Gain (dB)} = 20 \cdot \log_{10}\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right)$$

If Gain = 21.16 dB, we can solve for the voltage ratio:

$$21.16 = 20 \cdot \log_{10}\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) \Rightarrow \log_{10}\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) = 1.058 \Rightarrow \frac{V_{\text{out}}}{V_{\text{in}}} = 11.42$$

Example from LTspice simulation:

- Input voltage $V_{\text{in}} = 0.1$ V (i.e., 100 mV)
- Output voltage amplitude $V_{\text{out}} \approx 1.1$ V at low frequency

Interpretation

The -3 dB point marks the frequency where the gain falls to approximately 70.7 % of its maximum. This defines the bandwidth of the amplifier. The drop is attributed to the Miller effect caused by the JFET's gate-drain capacitance.

Conclusion

The simulated JFET amplifier exhibits a clear low-pass behavior with a high gain at low frequencies and a -3 dB cutoff near 33.65 MHz. The experiment verifies the expected response of a common-source amplifier operating at high frequencies.