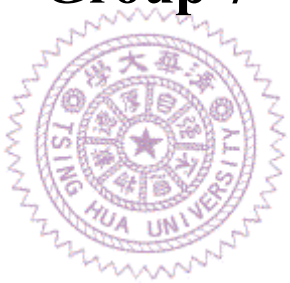
# 國立清華大學 電機工程系
# 112 學年度第二學期

# Advanced SOC Design Laboratory

## Lab #2-2

## Group 7

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中 華 民 國 一 一 三 年 四 月

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# 1. How you design your work (5 modifications)

## · Block diagram of our design:

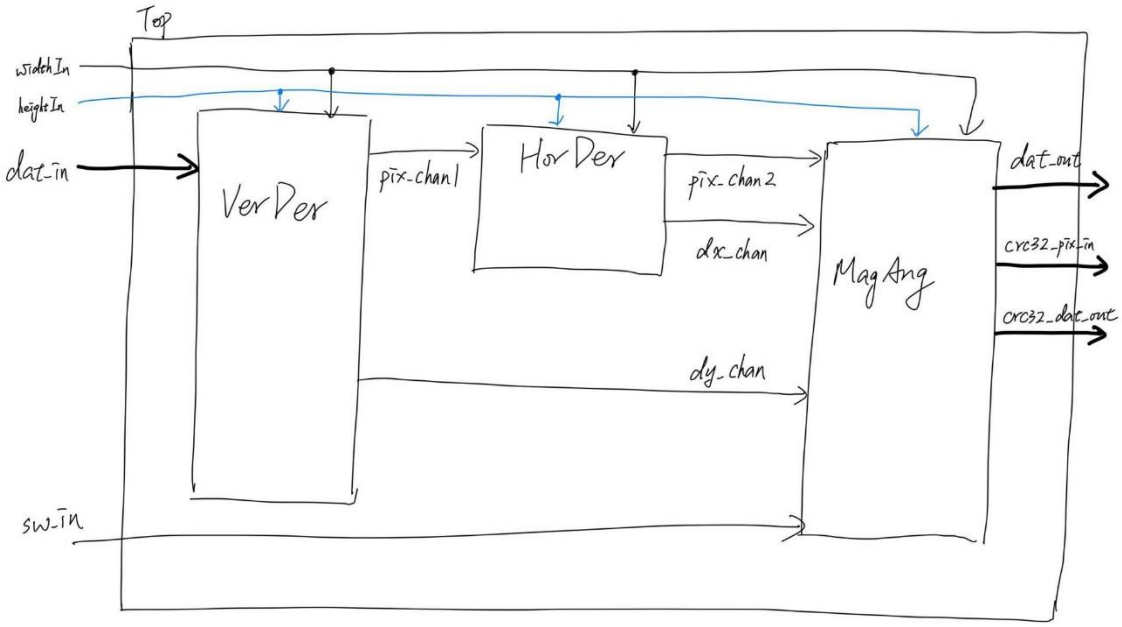



Fig. 1. Block Diagram of our design.

- **Process four pixels per clock cycle.**

Firstly, we defined several datatypes in EdgeDetect_defs.h for transferring pixels between functions, as shown in Fig. 2.

```
60  ////////////// My Part ////////////////////
61  //typedef uint64_t                  pixelType8
62  struct Stream_t{
63        bool sof;
64        bool eol;
65        pixelType4x pix;
66  };
67  /*
68  struct gradType4x{
69        gradType grad[4];
70  };
71  */
72  typedef int36                 gradType4x;
73  /*
74  struct magType4x{
75        magType mag[4];
76  };
77  */
78  typedef uint36                magType4x;  //
79  /*
80  struct pixelType8x{
81        pixelType data[8];
82  };
83  */
84
85  typedef ac_int<64,false>      pixelType8x;  /
86  ////////////////////////////////////////
```

Fig. 2. Definition of several datatypes.

Second, we changed the arguments of every function. This is illustrated from Fig. 3 to Fig. 6.

```
class EdgeDetect_Top
{
  //instances
  EdgeDetect_VerDer VerDer_inst;
  EdgeDetect_HorDer HorDer_inst;
  EdgeDetect_MagAng MagAng_inst;

  // Static interconnect channels (FIFOs) between blocks
  //ac_channel<gradType>       dy;
  //ac_channel<gradType>       dx;
  //ac_channel<pixelType>      dat; // channel for passing input pixels to horizontalDerivative
  ac_channel<gradType4x>       dy_chan;
  ac_channel<gradType4x>       dx_chan;
  ac_channel<pixelType4x>      pix_chan1, pix_chan2;


public:
  EdgeDetect_Top() {}

  //------------------------------------------------------------------------
  // Function: run
  //   Top interface for data in/out of class. Combines vertical and
  //   horizontal derivative and magnitude/angle computation.
  #pragma hls_design interface
  void CCS_BLOCK(run)(maxWType             widthIn,
                      maxHType             heightIn,
                      bool                 sw_in,
                      uint32               &crc32_pix_in,
                      uint32               &crc32_dat_out,
                      ac_channel<Stream_t>  &dat_in,
                      ac_channel<Stream_t>  &dat_out)
  {
    VerDer_inst.run(dat_in, widthIn, heightIn, pix_chan1, dy_chan);
    HorDer_inst.run(pix_chan1, widthIn, heightIn, pix_chan2, dx_chan);
    MagAng_inst.run(dx_chan, dy_chan, pix_chan2, widthIn, heightIn, sw_in, crc32_pix_in, crc32_dat_out, dat_out);
  }
```

Fig. 3. Top.

```
public:
  EdgeDetect_VerDer() {}

  #pragma hls_design interface
  void CCS_BLOCK(run)(ac_channel<Stream_t> &dat_in,
                      maxWType             &widthIn,
                      maxHType             &heightIn,
                      ac_channel<pixelType4x> &dat_out,
                      ac_channel<gradType4x>  &dy)
```

Fig. 4. VerDer.

```
public:
  EdgeDetect_HorDer() {}

  #pragma hls_design interface
  void CCS_BLOCK(run)(ac_channel<pixelType4x> &dat_in,
                      maxWType             &widthIn,
                      maxHType             &heightIn,
                      ac_channel<pixelType4x> &dat_out,
                      ac_channel<gradType4x>  &dx)
```

Fig. 5. HorDer.

```
public:
  EdgeDetect_MagAng() {}

  #pragma hls_design interface
  void CCS_BLOCK(run)(ac_channel<gradType4x> &dx_in,
                      ac_channel<gradType4x> &dy_in,
                      ac_channel<pixelType4x> &dat_in,
                      maxWType               &widthIn,
                      maxHType               &heightIn,
                      bool                   &sw_in,
                      uint32                 &crc32_pix_in,
                      uint32                 &crc32_dat_out,
                      ac_channel<Stream_t>   &dat_out)
```

Fig. 6. MagAng.

Third, we unfolded the multiply-add operation of one output pixel to 4 times, as illustrated in Fig. 7, Fig. 8, and Fig. 9.

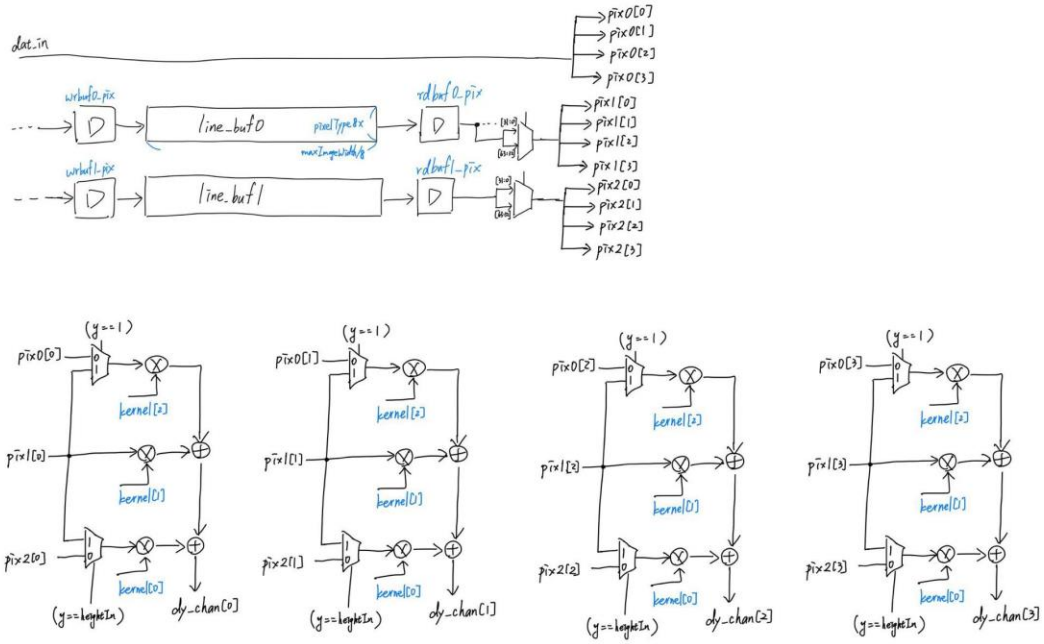



Fig. 7. Block diagram: VerDer.

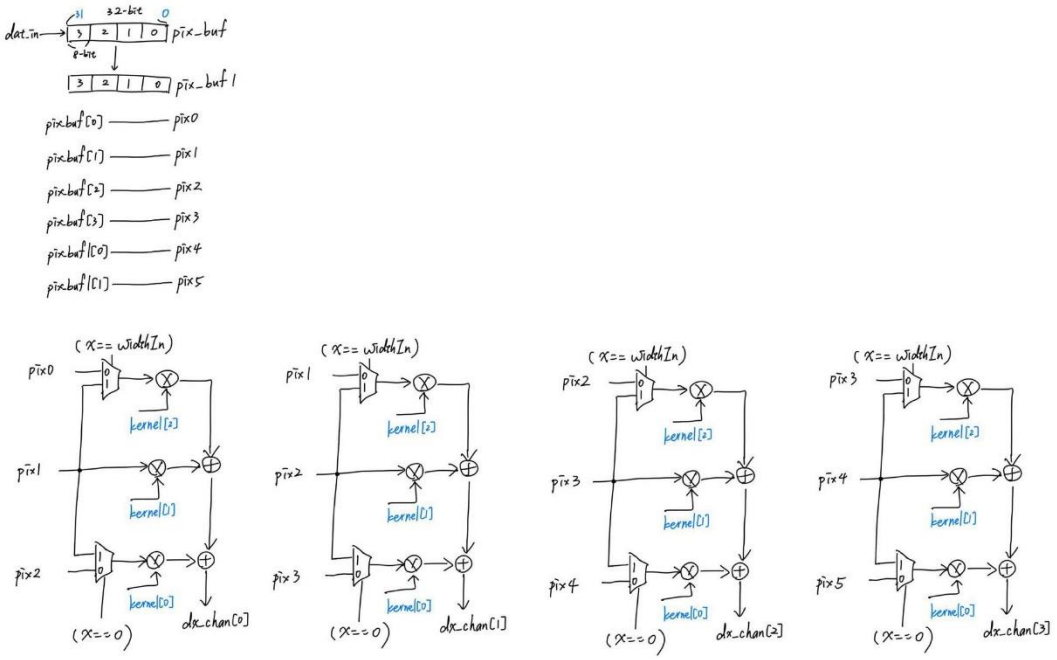



Fig. 8. Block diagram: HorDer.

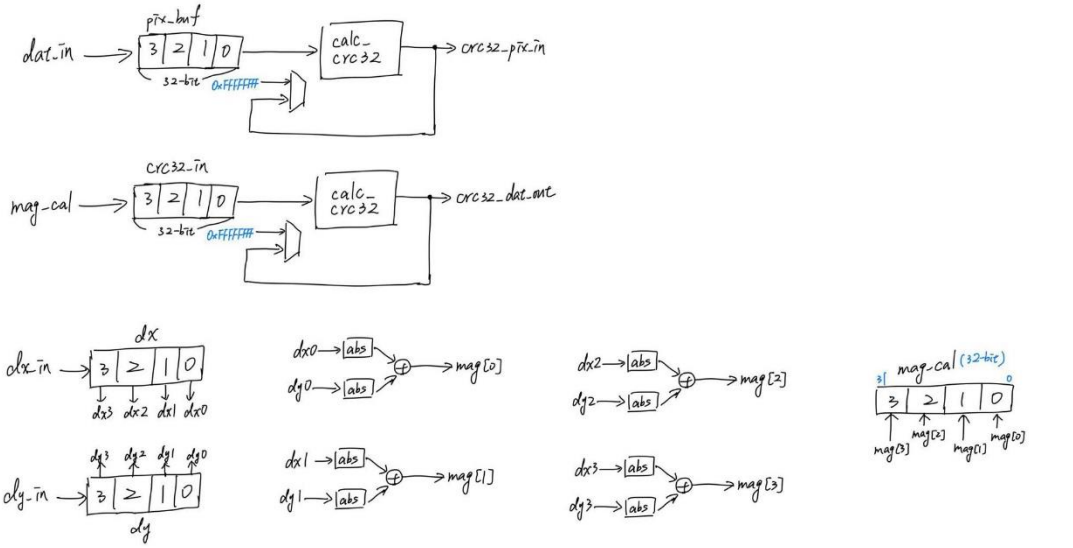



Fig. 9. Block diagram: MagAng.

- **Use sum of absolute difference (SAD) for edge magnitude calculation.**

The correction of the codes is shown in Fig. 10. Since the original dx.slc<9>(i*9) and dy.slc<9>(i*9) datatype are int9, and mag[i] datype is uint8, they should be clipped to 255 if the value is over 255.

```
112         // magn calculation
113         #pragma hls_unroll yes
114         ABSADD: for(int i = 0; i < 4; i++){
115             if((abs(dx.slc<9>(i * 9)) + abs(dy.slc<9>(i * 9)) ) > 255){
116                 mag[i] = 255;
117             }
118             else{
119                 mag[i] = abs(dx.slc<9>(i * 9)) + abs(dy.slc<9>(i * 9));
120             }
121         }
```

Fig. 10. The correction of the codes for SAD.

- **Add two crc32 calculation on image input / output.**

The crc32 calculation on image input and output are shown in Fig. 11 to Fig. 13, respectively. The local variables crc_32_pix_in_default and crc_32_dat_out_default are set to prevent the mapping of inout port for crc_32_pix_in and crc_32_dat_out during Architecture phase.

```
98          // crc32 for image input
99          crc32_in = pix_buf;
100         crc32_pix_in_default = calc_crc32<32>(crc32_pix_in_default, pix_buf);
```

Fig. 11. The crc32 calculation for image input.

```
139         // crc32 for image output
140         crc32_in = mag_cal;
141         crc32_dat_out_default = calc_crc32<32>(crc32_dat_out_default, mag_cal);
```

Fig. 12. The crc32 calculation for image output.

```
85        uint32 crc32_pix_in_default = 0XFFFFFFFF;
86        uint32 crc32_dat_out_default = 0XFFFFFFFF;
87
88        MROW: for (maxHType y = 0; ; y++) {
172       crc32_pix_in_default = ~crc32_pix_in_default;
173       crc32_pix_in = crc32_pix_in_default;
174       crc32_dat_out_default = ~crc32_dat_out_default;
175       crc32_dat_out = crc32_dat_out_default;
```

Fig. 13. The crc32 default values outside the loops.

- **Select the output source from input image or the calculated magnitude.**

The selection of the output source from image input of the calculated magnitude is depicted in Fig. 14.

```
123           // switch
124           if (sw_in==0){
125             mag_cal.set_slc(0, pix0);
126             mag_cal.set_slc(8, pix1);
127             mag_cal.set_slc(16, pix2);
128             mag_cal.set_slc(24, pix3);
129           }
130           else{
131             mag_cal.set_slc(0, mag[0]);
132             mag_cal.set_slc(8, mag[1]);
133             mag_cal.set_slc(16, mag[2]);
134             mag_cal.set_slc(24, mag[3]);
135           }
```

Fig. 14. The selection of the output source from image input of the calculated magnitude.

- **Remove the angle calculation.**

The removal of the angle calculation is illustrated in Fig. 15.

```
143           //ac_math::ac_atan2_cordic((ac_fixed<9,9>)dy, (ac_fixed<9,9>) dx, at);
144           //angle.write(at);
```

Fig. 15. The removal of the angle calculation.

## 2. What's the test result of catapult design (C design checker, testbench)

### · C design checker:

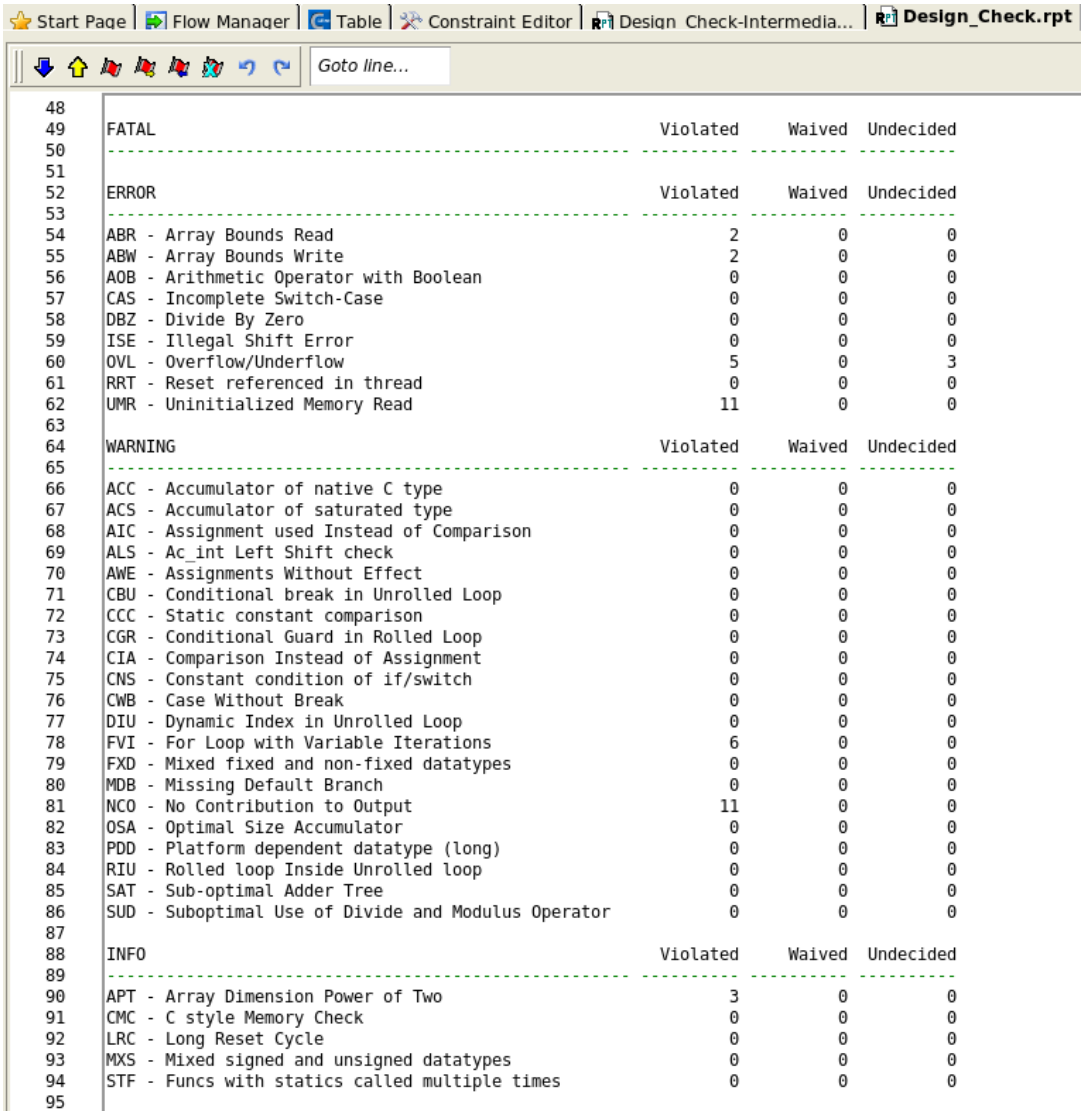
The C design checker result is shown in Fig. 16 to Fig. 19.

Start Page | Flow Manager | Table | Constraint Editor | Design Check-Intermedia... | Design_Check.rpt

Goto line...

```
1  -- Catapult System Level Synthesis: C Design Checker Formal Rules Report by Rule Status
2
3  Current Option Settings
4    Option                        Description                                          Value
5    ----------------------------  ---------------------------------------------------  -----
6    WAIVER_FILE                   C Design Checker Waiver file
7    MEMORY_LIMIT                  Memory Usage Limit in (GB)                           0
8    SYMBOLIC_MEMSIZE_THRESHOLD    Symbolic Memory Size Threshold                       256
9    VERIFICATION_EFFORT           Verification Effort                                  medium
10   VERIFICATION_MODE             Verification modes of CDesignChecker run             Custom
11   RPT_UNDECIDED_PROPS           Report undecided properties in report files          true
12   GLOBAL_OPTIONS                Global Options
13   ABR                           ABR - Array Bounds Read                              CHECKED
14   ABW                           ABW - Array Bounds Write                             CHECKED
15   ACC                           ACC - Accumulator of native C type                   CHECKED
16   ACS                           ACS - Accumulator of saturated type                  CHECKED
17   AIC                           AIC - Assignment used Instead of Comparison          CHECKED
18   ALS                           ALS - Ac_int Left Shift check                        CHECKED
19   AOB                           AOB - Arithmetic Operator with Boolean               CHECKED
20   APT                           APT - Array Dimension Power of Two                   CHECKED
21   AWE                           AWE - Assignments Without Effect                     CHECKED
22   CAS                           CAS - Incomplete Switch-Case                         CHECKED
23   CBU                           CBU - Conditional break in Unrolled Loop             CHECKED
24   CCC                           CCC - Static constant comparison                     CHECKED
25   CGR                           CGR - Conditional Guard in Rolled Loop               CHECKED
26   CIA                           CIA - Comparison Instead of Assignment               CHECKED
27   CMC                           CMC - C style Memory Check                           CHECKED
28   CNS                           CNS - Constant condition of if/switch                CHECKED
29   CWB                           CWB - Case Without Break                             CHECKED
30   DBZ                           DBZ - Divide By Zero                                 CHECKED
31   DIU                           DIU - Dynamic Index in Unrolled Loop                 CHECKED
32   FVI                           FVI - For Loop with Variable Iterations              CHECKED
33   FXD                           FXD - Mixed fixed and non-fixed datatypes            CHECKED
34   ISE                           ISE - Illegal Shift Error                            CHECKED
35   LRC                           LRC - Long Reset Cycle                               CHECKED
36   MDB                           MDB - Missing Default Branch                         CHECKED
37   MXS                           MXS - Mixed signed and unsigned datatypes            CHECKED
38   NCO                           NCO - No Contribution to Output                      CHECKED
39   OSA                           OSA - Optimal Size Accumulator                       CHECKED
40   OVL                           OVL - Overflow/Underflow                             CHECKED
41   PDD                           PDD - Platform dependent datatype (long)             CHECKED
42   RIU                           RIU - Rolled loop Inside Unrolled loop               CHECKED
43   RRT                           RRT - Reset referenced in thread                     CHECKED
44   SAT                           SAT - Sub-optimal Adder Tree                         CHECKED
45   STF                           STF - Funcs with statics called multiple times       CHECKED
46   SUD                           SUD - Suboptimal Use of Divide and Modulus Operator  CHECKED
47   UMR                           UMR - Uninitialized Memory Read                      CHECKED
```

Fig. 16. Design Checker Report (Part 1).

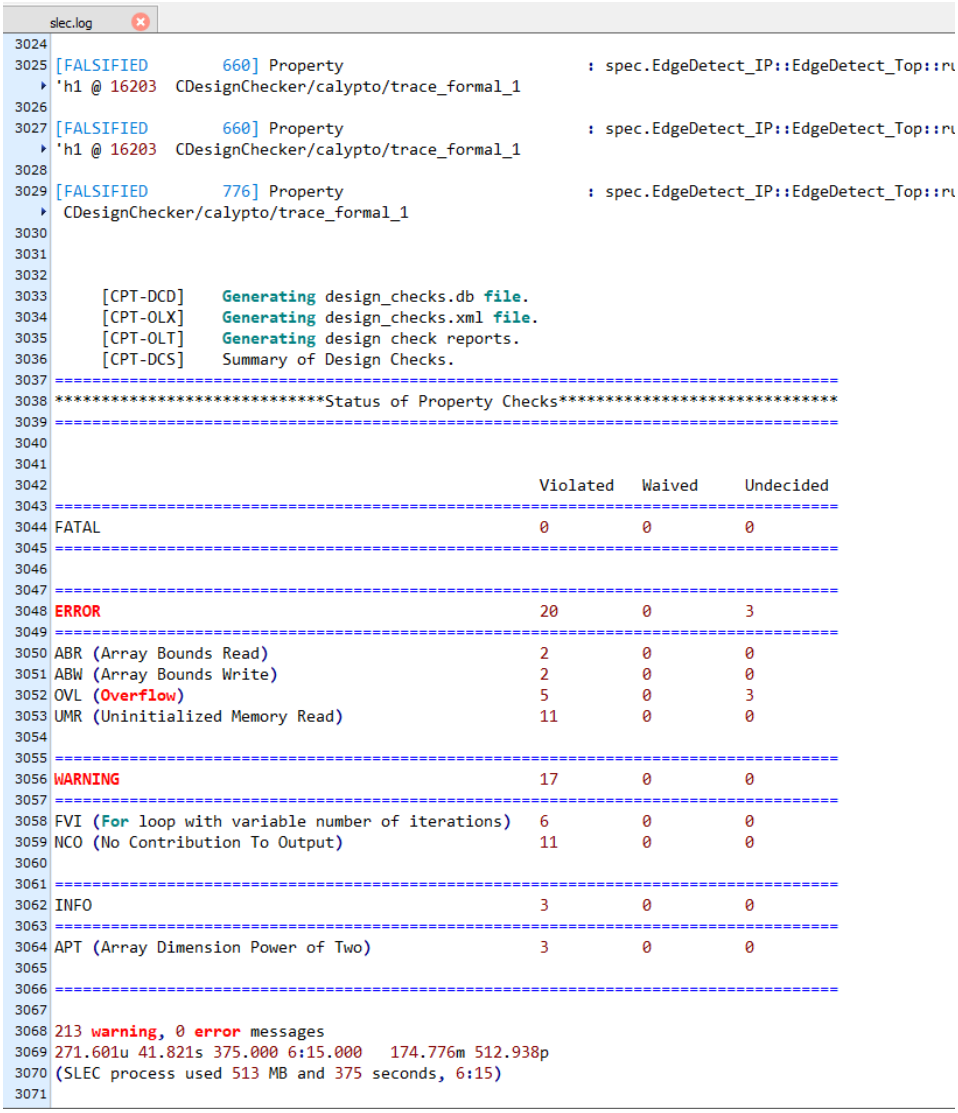



```
48
49  FATAL                                                Violated     Waived  Undecided
50  ---------------------------------------------------- ---------- ---------- ----------
51
52  ERROR                                                Violated     Waived  Undecided
53  ---------------------------------------------------- ---------- ---------- ----------
54  ABR - Array Bounds Read                                     2          0          0
55  ABW - Array Bounds Write                                    2          0          0
56  AOB - Arithmetic Operator with Boolean                      0          0          0
57  CAS - Incomplete Switch-Case                                0          0          0
58  DBZ - Divide By Zero                                        0          0          0
59  ISE - Illegal Shift Error                                   0          0          0
60  OVL - Overflow/Underflow                                    5          0          3
61  RRT - Reset referenced in thread                            0          0          0
62  UMR - Uninitialized Memory Read                            11          0          0
63
64  WARNING                                              Violated     Waived  Undecided
65  ---------------------------------------------------- ---------- ---------- ----------
66  ACC - Accumulator of native C type                          0          0          0
67  ACS - Accumulator of saturated type                         0          0          0
68  AIC - Assignment used Instead of Comparison                 0          0          0
69  ALS - Ac_int Left Shift check                               0          0          0
70  AWE - Assignments Without Effect                            0          0          0
71  CBU - Conditional break in Unrolled Loop                    0          0          0
72  CCC - Static constant comparison                            0          0          0
73  CGR - Conditional Guard in Rolled Loop                      0          0          0
74  CIA - Comparison Instead of Assignment                      0          0          0
75  CNS - Constant condition of if/switch                       0          0          0
76  CWB - Case Without Break                                    0          0          0
77  DIU - Dynamic Index in Unrolled Loop                        0          0          0
78  FVI - For Loop with Variable Iterations                     6          0          0
79  FXD - Mixed fixed and non-fixed datatypes                   0          0          0
80  MDB - Missing Default Branch                                0          0          0
81  NCO - No Contribution to Output                            11          0          0
82  OSA - Optimal Size Accumulator                              0          0          0
83  PDD - Platform dependent datatype (long)                    0          0          0
84  RIU - Rolled loop Inside Unrolled loop                      0          0          0
85  SAT - Sub-optimal Adder Tree                                0          0          0
86  SUD - Suboptimal Use of Divide and Modulus Operator         0          0          0
87
88  INFO                                                 Violated     Waived  Undecided
89  ---------------------------------------------------- ---------- ---------- ----------
90  APT - Array Dimension Power of Two                          3          0          0
91  CMC - C style Memory Check                                  0          0          0
92  LRC - Long Reset Cycle                                      0          0          0
93  MXS - Mixed signed and unsigned datatypes                   0          0          0
94  STF - Funcs with statics called multiple times              0          0          0
95
```

Fig. 17. Design Checker Report (Part 2).

```
STF - Funcs with statics called multiple times                0         0         0

DISABLED
-----------------------------------------------------

Violations - 40 (0 fatal, 20 error, 17 warning, 3 info)
FATAL
ERROR
  ABR - Array Bounds Read - 2
    EdgeDetect_VerDer.h:100:26
      | 98              if ( (x/4 &1) == 0 ) {
      | 99                // vertical window of pixels
      > 100               rdbuf1_pix = line_buf1[x/8];
      | 101               rdbuf0_pix = line_buf0[x/8];
      | 102             } else { // Write line buffer caches on odd iterations of COL loop

    EdgeDetect_VerDer.h:101:26
      | 99                // vertical window of pixels
      | 100               rdbuf1_pix = line_buf1[x/8];
      > 101               rdbuf0_pix = line_buf0[x/8];
      | 102             } else { // Write line buffer caches on odd iterations of COL loop
      | 103               line_buf1[x/8] = rdbuf0_pix; // copy previous line

  ABW - Array Bounds Write - 2
    EdgeDetect_VerDer.h:103:13
      | 101               rdbuf0_pix = line_buf0[x/8];
      | 102             } else { // Write line buffer caches on odd iterations of COL loop
      > 103               line_buf1[x/8] = rdbuf0_pix; // copy previous line
      | 104               line_buf0[x/8] = wrbuf0_pix; // store current line
      | 105             }
```

Fig. 18. Design Checker Report (Part 3).



```
slec.log
3024
3025 [FALSIFIED        660] Property                          : spec.EdgeDetect_IP::EdgeDetect_Top::ru
     'h1 @ 16203  CDesignChecker/calypto/trace_formal_1
3026
3027 [FALSIFIED        660] Property                          : spec.EdgeDetect_IP::EdgeDetect_Top::ru
     'h1 @ 16203  CDesignChecker/calypto/trace_formal_1
3028
3029 [FALSIFIED        776] Property                          : spec.EdgeDetect_IP::EdgeDetect_Top::ru
      CDesignChecker/calypto/trace_formal_1
3030
3031
3032
3033      [CPT-DCD]    Generating design_checks.db file.
3034      [CPT-OLX]    Generating design_checks.xml file.
3035      [CPT-OLT]    Generating design check reports.
3036      [CPT-DCS]    Summary of Design Checks.
3037 ================================================================================
3038 ***************************Status of Property Checks*****************************
3039 ================================================================================
3040
3041
3042                                                  Violated   Waived     Undecided
3043 ================================================================================
3044 FATAL                                            0          0          0
3045 ================================================================================
3046
3047 ================================================================================
3048 ERROR                                            20         0          3
3049 ================================================================================
3050 ABR (Array Bounds Read)                          2          0          0
3051 ABW (Array Bounds Write)                         2          0          0
3052 OVL (Overflow)                                   5          0          3
3053 UMR (Uninitialized Memory Read)                  11         0          0
3054
3055 ================================================================================
3056 WARNING                                          17         0          0
3057 ================================================================================
3058 FVI (For loop with variable number of iterations)  6          0          0
3059 NCO (No Contribution To Output)                  11         0          0
3060
3061 ================================================================================
3062 INFO                                             3          0          0
3063 ================================================================================
3064 APT (Array Dimension Power of Two)               3          0          0
3065
3066 ================================================================================
3067
3068 213 warning, 0 error messages
3069 271.601u 41.821s 375.000 6:15.000   174.776m 512.938p
3070 (SLEC process used 513 MB and 375 seconds, 6:15)
3071
```

Fig. 19. Design Checker Report (Part 4).

- **Testbench:**

The testbench result is shown in Fig. 20 to Fig. 23.

rtl_sim_vivado_lib.log - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
# (and any connected ports) is undebuggable as the tlm fifo size specified is '-1'. A tlm fifo with an infinite size is
# ** Warning: (vsim-4029) The fifo '/scverify_top/TLS_in_wait_ctrl_fifo_dat_in_sof'
# (and any connected ports) is undebuggable as the tlm fifo size specified is '-1'. A tlm fifo with an infinite size is
# ** Warning: (vsim-4029) The fifo '/scverify_top/TLS_in_fifo_dat_in_sof'
# (and any connected ports) is undebuggable as the tlm fifo size specified is '-1'. A tlm fifo with an infinite size is
# Disabling STALL_FLAG toggling
# do {./Catapult_8/EdgeDetect_IP_EdgeDetect_Top.v1/scverify/rtl_v_msim/scverify_msim_wave.tcl}
# Reading SCVerify waveform database './Catapult_8/EdgeDetect_IP_EdgeDetect_Top.v1/scverify/ccs_wave_signals.dat'
# Populating WAVE window...
#                 DONE
# 0
#
# stdin: <EOF>
run -all
# Loading Input File
# Input file:          ./image/people640x360_rgb.bmp
# Mode:                1
# Output file (alg):   1
# Output file (hw):    out_hw.bmp
# Image width: 640
# Image height: 360
########################################## FRAME NO.   0 ##########################################
# Running
# SCVerify intercepting C++ function 'EdgeDetect_IP::EdgeDetect_Top::run' for RTL block 'EdgeDetect_IP_EdgeDetect_Top'
#                      DUT instance '0x2aaabb1b0b90'
# Info: HW reset: TLS_rst active @ 0 s
# Info: HW reset: TLS_arst_n active @ 0 s
# Magnitude: Manhattan norm per pixel 10.470994
# Writing algorithmic bitmap output to: 1
# Writing bit-accurate bitmap output to: out_hw.bmp
# sofErr: 0 eolErr: 0
# crc32_alg_pix_in  = ebb44e76  crc32_hw_pix_in  = ebb44e76
# crc32_alg_dat_out = 398625ad  crc32_hw_dat_out = eab7d5b8
# Finished
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of widthIn
#    captured 1 values of heightIn
#    captured 1 values of sw_in
#    captured 1 values of crc32_pix_in
#    captured 1 values of crc32_dat_out
#    captured 57600 values of dat_in_sof
#    captured 57600 values of dat_in_eol
#    captured 57600 values of dat_in_pix
#    captured 57600 values of dat_out_sof
#    captured 57600 values of dat_out_eol
#    captured 57600 values of dat_out_pix
# Info: scverify_top/user_tb: Simulation completed
#
```

Fig. 20. Testbench result of rtl_sim (Part 1).

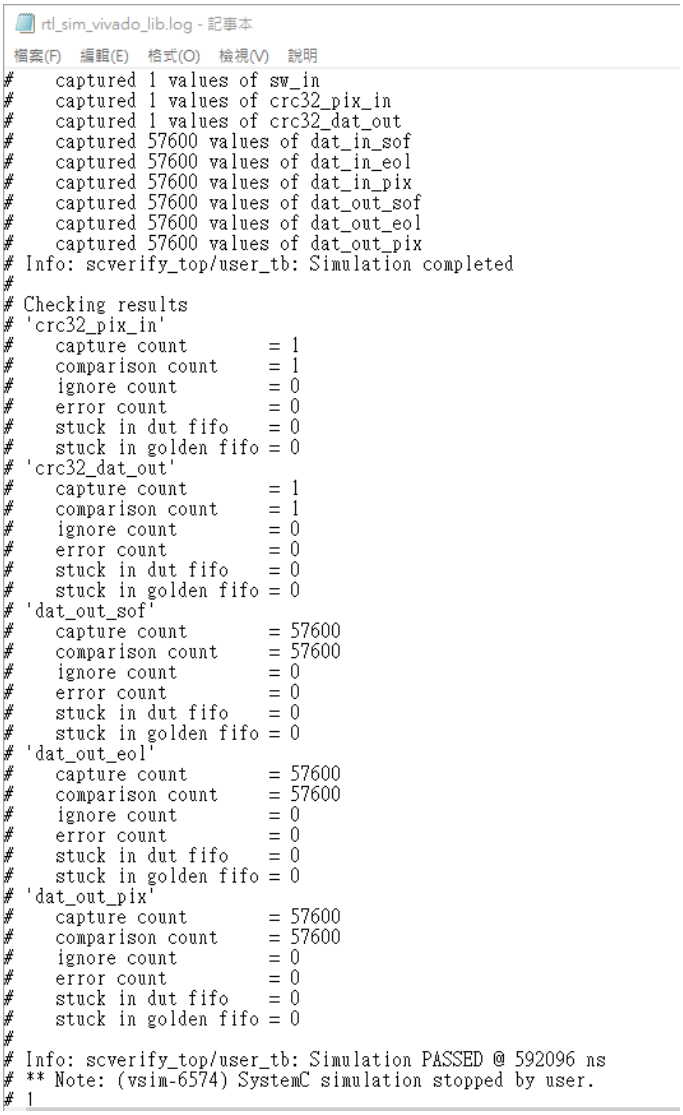


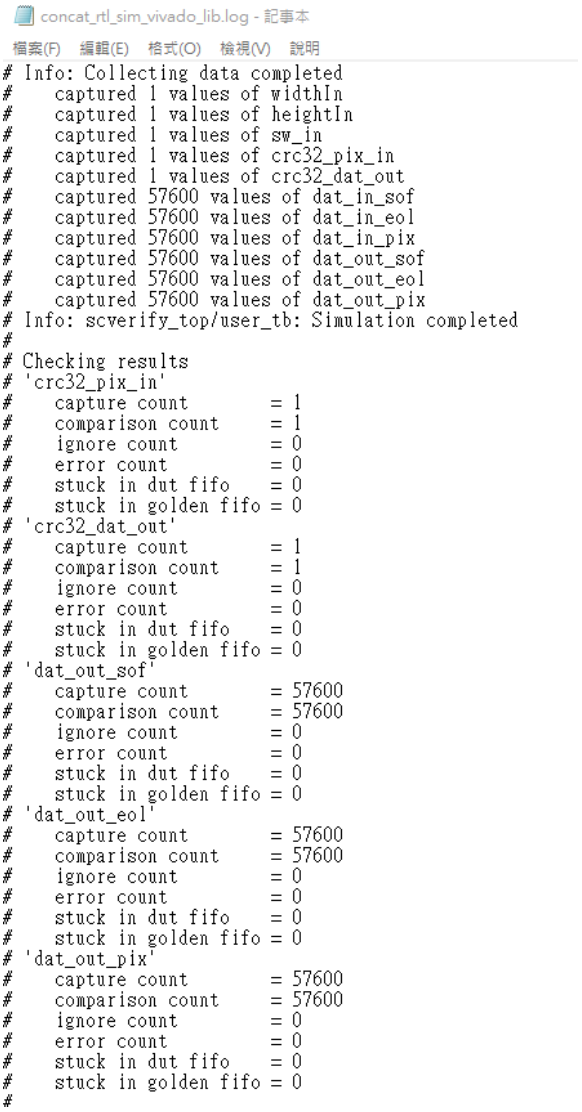

Fig. 21. Testbench result of rtl_sim (Part 2).


concat_rtl_sim_vivado_lib.log - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
# ** Warning: (vsim-4029) The fifo '/scverify_top/TLS_in_fifo_dat_in_sof'
# (and any connected ports) is undebuggable as the tlm fifo size specified is '-1'. A tlm fifo with an infinite size is
# Disabling STALL_FLAG toggling
# do {./Catapult_8/EdgeDetect_IP_EdgeDetect_Top.v1/scverify/concat_sim_rtl_v_msim/scverify_msim_wave.tcl}
# Reading SCVerify waveform database './Catapult_8/EdgeDetect_IP_EdgeDetect_Top.v1/scverify/ccs_wave_signals.dat'
# Populating WAVE window...
#                  DONE
# 0
#
# stdin: <EOF>
run -all
# Loading Input File
# Input file:          ./image/people640x360_rgb.bmp
# Mode:                1
# Output file (alg):   1
# Output file (hw):    out_hw.bmp
# Image width: 640
# Image height: 360
######################################### FRAME NO.   0 ##########################################
# Running
# SCVerify intercepting C++ function 'EdgeDetect_IP::EdgeDetect_Top::run' for RTL block 'EdgeDetect_IP_EdgeDetect_Top'
#                       DUT instance '0x2aaabb1b0b90'
# Info: HW reset: TLS_rst active @ 0 s
# Info: HW reset: TLS_arst_n active @ 0 s
# Magnitude: Manhattan norm per pixel 10.470994
# Writing algorithmic bitmap output to: 1
# Writing bit-accurate bitmap output to: out_hw.bmp
# sofErr: 0 eolErr: 0
# crc32_alg_pix_in  = ebb44e76  crc32_hw_pix_in  = ebb44e76
# crc32_alg_dat_out = 398625ad  crc32_hw_dat_out = eab7d5b8
# Finished
# Info: Execution of user-supplied C++ testbench 'main()' has completed with exit code = 0
#
# Info: Collecting data completed
#    captured 1 values of widthIn
#    captured 1 values of heightIn
#    captured 1 values of sw_in
#    captured 1 values of crc32_pix_in
#    captured 1 values of crc32_dat_out
#    captured 57600 values of dat_in_sof
#    captured 57600 values of dat_in_eol
#    captured 57600 values of dat_in_pix
#    captured 57600 values of dat_out_sof
#    captured 57600 values of dat_out_eol
#    captured 57600 values of dat_out_pix
# Info: scverify_top/user_tb: Simulation completed
```

Fig. 22. Testbench result of concat_rtl_sim (Part 1).


concat_rtl_sim_vivado_lib.log - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
# Info: Collecting data completed
#    captured 1 values of widthIn
#    captured 1 values of heightIn
#    captured 1 values of sw_in
#    captured 1 values of crc32_pix_in
#    captured 1 values of crc32_dat_out
#    captured 57600 values of dat_in_sof
#    captured 57600 values of dat_in_eol
#    captured 57600 values of dat_in_pix
#    captured 57600 values of dat_out_sof
#    captured 57600 values of dat_out_eol
#    captured 57600 values of dat_out_pix
# Info: scverify_top/user_tb: Simulation completed
#
# Checking results
# 'crc32_pix_in'
#    capture count        = 1
#    comparison count     = 1
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'crc32_dat_out'
#    capture count        = 1
#    comparison count     = 1
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'dat_out_sof'
#    capture count        = 57600
#    comparison count     = 57600
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'dat_out_eol'
#    capture count        = 57600
#    comparison count     = 57600
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
# 'dat_out_pix'
#    capture count        = 57600
#    comparison count     = 57600
#    ignore count         = 0
#    error count          = 0
#    stuck in dut fifo    = 0
#    stuck in golden fifo = 0
#
```

Fig. 23. Testbench result of concat_rtl_sim (Part 2).

# 3. How to integrate your design in FSIC

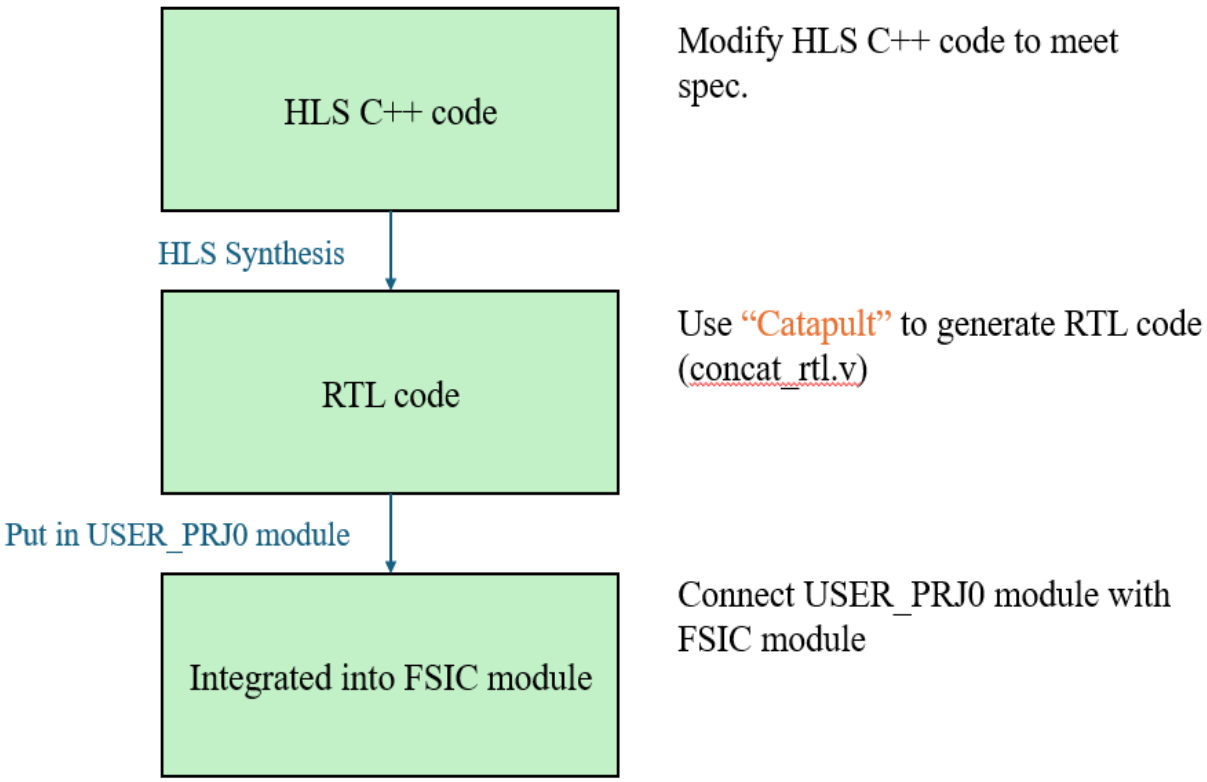



Fig. Work process

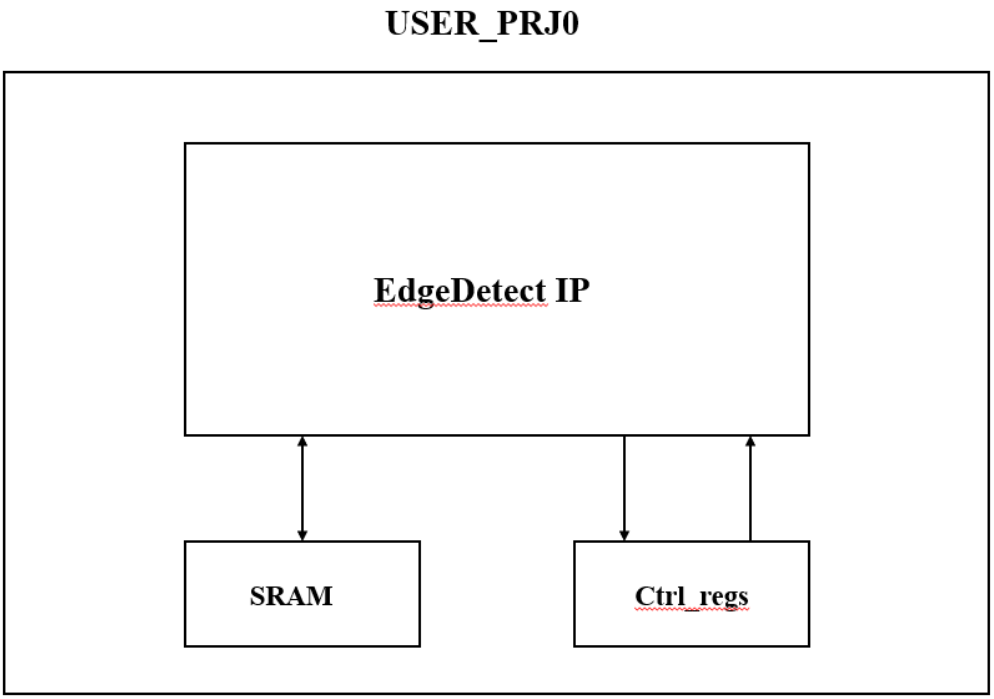
- First, put the RTL code (concat_rtl.v) into USER_PRJ0 module.
  - Copy concat_rtl.v file into the user_prj0/rtl folder.
- Second, replace concat_EdgeDetect_Top_fsic.v with concat_rtl.v

- Before executing the simulation, you need to fill in the filelist based on the design you are using.
  - Filelist in the user/testbench/tc folder.

```
../fpga.v
../fsic_clock.v
../../rtl/fsic.v
../../axilite_axis/rtl/axi_ctrl_logic.sv
../../axilite_axis/rtl/axil_axis.sv
../../axilite_axis/rtl/axilite_master.sv
../../axilite_axis/rtl/axilite_slave.sv
../../axilite_axis/rtl/axis_master.sv
../../axilite_axis/rtl/axis_slave.sv
../../axis_switch/rtl/sw_caravel.v
../../config_ctrl/rtl/config_ctrl.v
../../fsic_clkrst/rtl/fsic_clkrst.v
../../io_serdes/rtl/fsic_coreclk_phase_cnt.v
../../io_serdes/rtl/fsic_io_serdes_rx.v
../../io_serdes/rtl/io_serdes.v
../../logic_analyzer/rtl/LogicAnalyzer.v
../../logic_analyzer/rtl/Sram.v
../../mprj_io/rtl/fsic_mprj_io.v
../../user_subsys/rtl/user_subsys.v
../../user_subsys/axil_slav/rtl/axil_slav.v
../../user_subsys/axis_mstr/rtl/axis_mstr.v
../../user_subsys/axis_slav/rtl/axis_slav.v
../../user_subsys/irq_mux/rtl/irq_mux.v
../../user_subsys/la_mux/rtl/la_mux.v
../../user_subsys/user_prj/user_prj0/rtl/user_prj0.v
../../user_subsys/user_prj/user_prj0/rtl/concat_rtl.v
../../user_subsys/user_prj/user_prj0/rtl/spram.v
../../user_subsys/user_prj/user_prj1/rtl/user_prj1.v
../../user_subsys/user_prj/user_prj1/rtl/bram11.v
../../user_subsys/user_prj/user_prj1/rtl/fir.v
../../user_subsys/user_prj/user_prj1/rtl/multiplier_adder.v
../../user_subsys/user_prj/user_prj2/rtl/user_prj2.v
../../user_subsys/user_prj/user_prj3/rtl/user_prj3.v
```

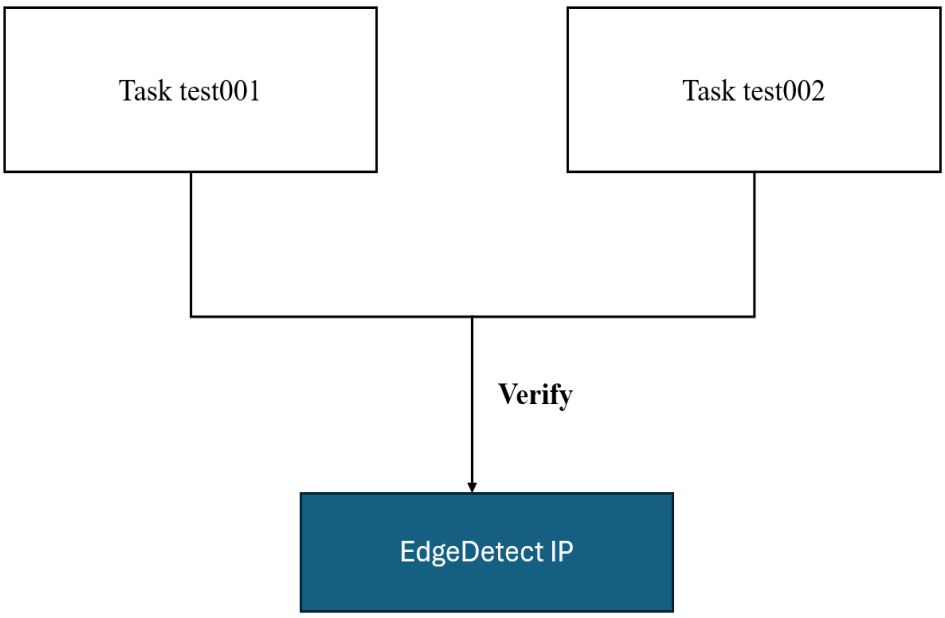
- Put the two SRAM(spram.v) and ctrl_regs rd/wr circuits into USER_PRJ0 module.

- USER_PRJ0 internal block diagram

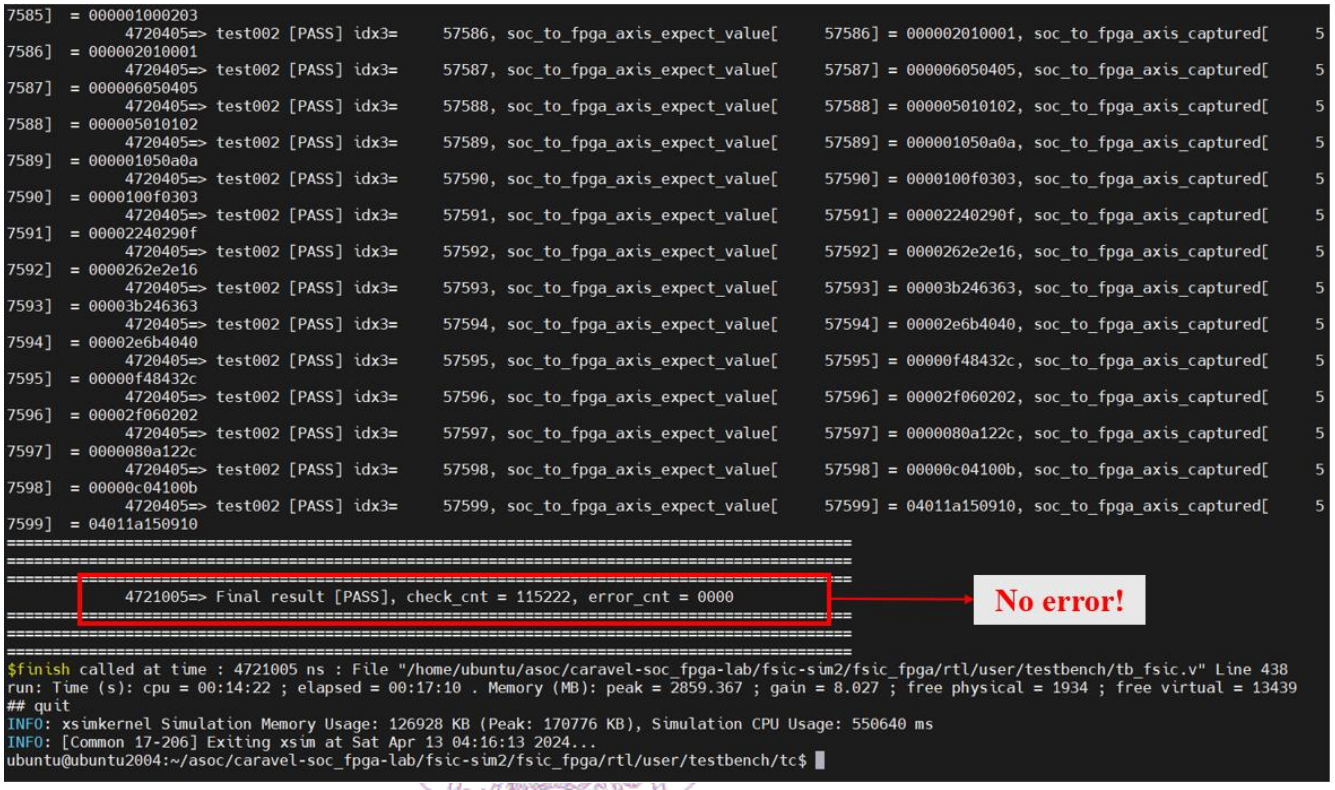


## 4. What's the simulation result of FSIC

- This is the simulation result verified using testbench. Use task "test001" ~ task "test007" function in testbench for verify the FSIC module, and then task "test001" and task "test002" mainly verify the EdgeDetect IP.
  - The mainly task is to test the EdgeDetect IP.



- Simulation results





# Distribution of work:

- 02_edgedetect_fsic: 蔡宗穎
- 03_fsic_prj: 張傑閔
- Discussion with each other when we were faced with some problems.