SystemC & Behavior Coding

Assignment 6, 2021-12-17

Abstract

Remodel the Assignment 5 timer module with `SC_CTHREAD`.

Please read carefully. All outputs required are described in the text. Five (5) points will be taken for each bug, missing required output and behavior.

The `SC_CTHREAD` timer module

Description

1. Remodel the Assignment 5 timer module with `SC_CTHREAD`, where `clock` pin is a positive-triggered clock port, and `start` pin is a synchronous active-high reset port.

sc_main

Description

1. Reuse the `main.cpp` implemented in Assignment 5.
2. Create a trace file named `RESULT.vcd`. And trace ports and the register `count` in following order:
   - `clock`
   - `count`
   - `start`
   - `timeout`

makefile

Description

1. A `makefile` must be provided, with proper modifications to your environment.

Please turn in the source codes only and `makefile`. Do not turn in the executable.

Due date

2PM, December 24th, 2021

Score weight (towards the final grade) 5%