SystemC & Behavior Coding

Assignment 5, 2021-12-03

Abstract

Install SystemC 2.3, and compile and test the timer module described on pages 36 and 37 of the Lecture Notes, Section 4.

Please read carefully. All outputs required are described in the text. Five (5) points will be taken for each bug, missing required output and behavior.

The 'timer' module

Description

1. Copy exactly the timer module on pages 36 and 37 of the Lecture Notes, Section 4.

SystemC 2.3.3

Description

1. You can download the SystemC 2.3.3 from http://www.accellera.org/downloads/standards/systemc and select systemc-2.3.3. Please fill up your basic data and register. Do not worry. Accellera will not try to sell you anything or release your information to anyone.
2. Follow the instruction and install SystemC 2.3.3 in your computer.

sc_main

Description

1. Create a test suite, i.e. `sc_main`, for the `timer` module, that
   - Instantiate a `timer` module
   - Provide a 100MHz clock to the `timer` module
   - Create a trace file named `RESULT.vcd`. And trace ports/variable in following order:
     - `clock`
     - `start`
     - `timeout`
     - `count`

- Feed in a `start` signal to create a trace which contains a waveform of exactly 30 cycles (300ns, that is.) This 30-cycle waveform should include following scenarios:
  - reset the `timer` for 3 cycles before it is released for counting,
  - during counting reset the `timer` before `count` reaches 0, and
  - during counting reset the `timer` after `count` reaches 0

- Note: to give a specific value to a signal, say, `start` in the

`sc_main()` that connects to the `timer->start` port, it can be written as `start.write(0)` or `start.write(1)`.

Please turn in the source codes only and `makefile`. Do not turn in the executable.

Due date
2PM, December 10th, 2021

Score weight (towards the final grade) 5%