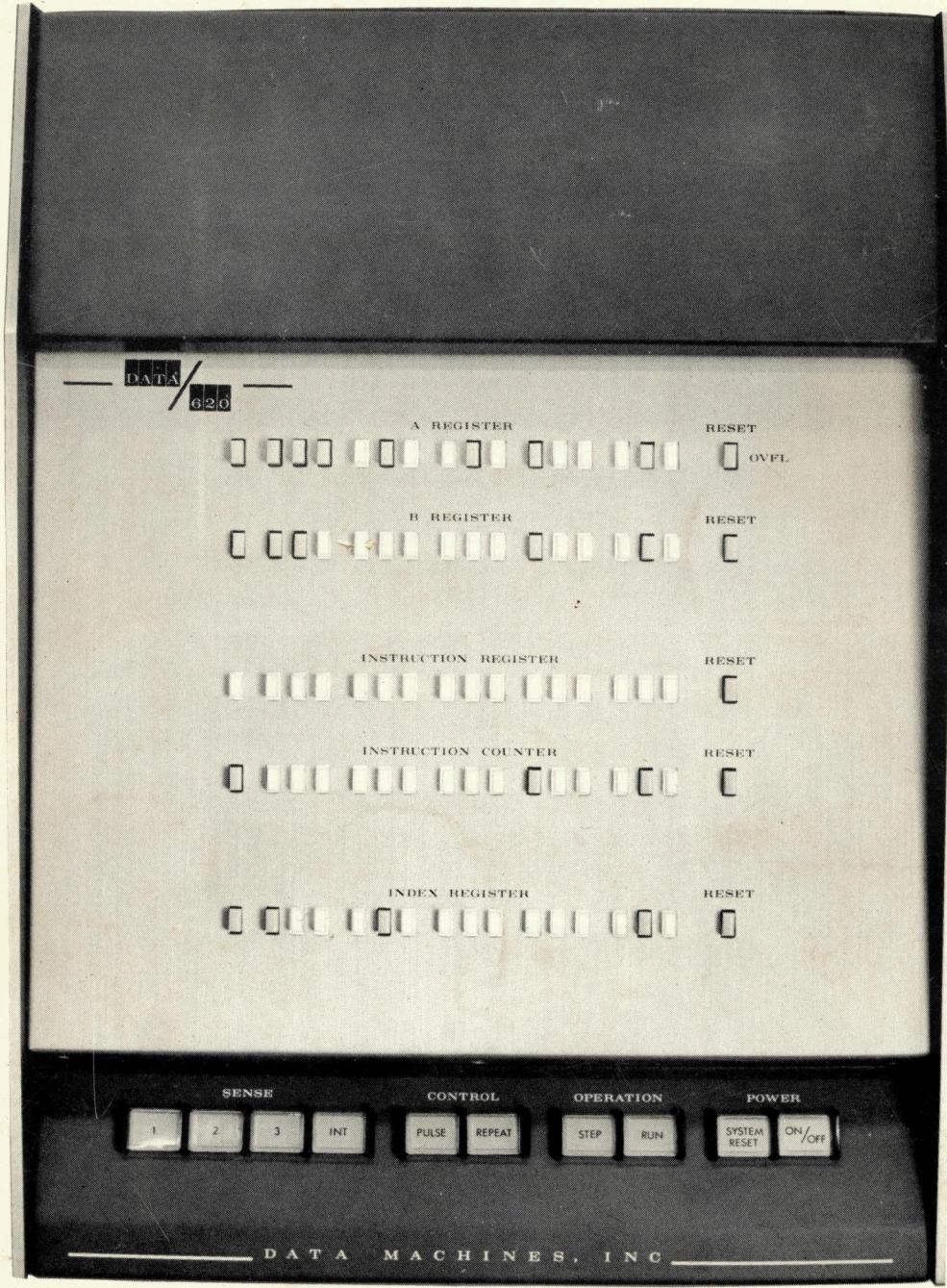
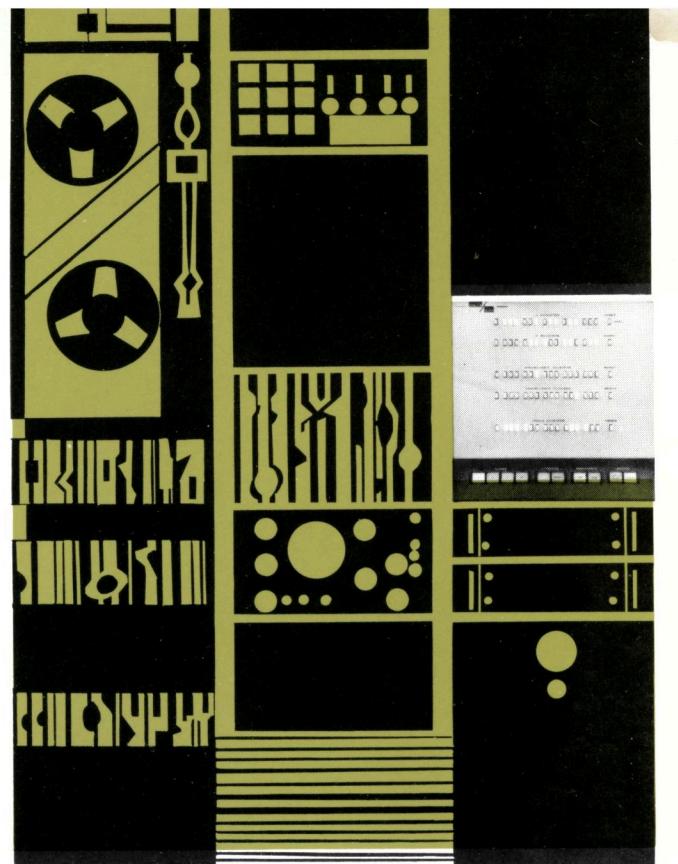


the
data machine
that wants
to be part
of a system



DATA 620

system oriented computer features...



- A package to blend in with YOUR system and environment.
- Six Addressing Modes for Memory efficiency and speeds.
- 107 Machine Commands plus Micro-commands at 1.8
- Simultaneous I/O Rates at over 500,000 word/sec.
- Party Line I/O for field plug-in expansion.
- Micro-Exec for Nanosecond Processing Rates.
- Gp Memory Modules for concurrent processing, buffering and I/O.

For use in systems that perform real-time data reduction, on-line control, remote site monitoring, automatic checkout, process control, inventory management, production line control, hybrid digital-analog computation, and other applications where the goal is to maximize system throughput.

CONTENTS

The Data Machine 5

- Data 620 Computer Organization (diagram) 6
- Data 620 Dimensional Drawings 6
- Data 620 Bit Slice (diagram) 10, 11
- Data 620 Specifications (insert) 15
- Data 620 Instruction List (insert) 16

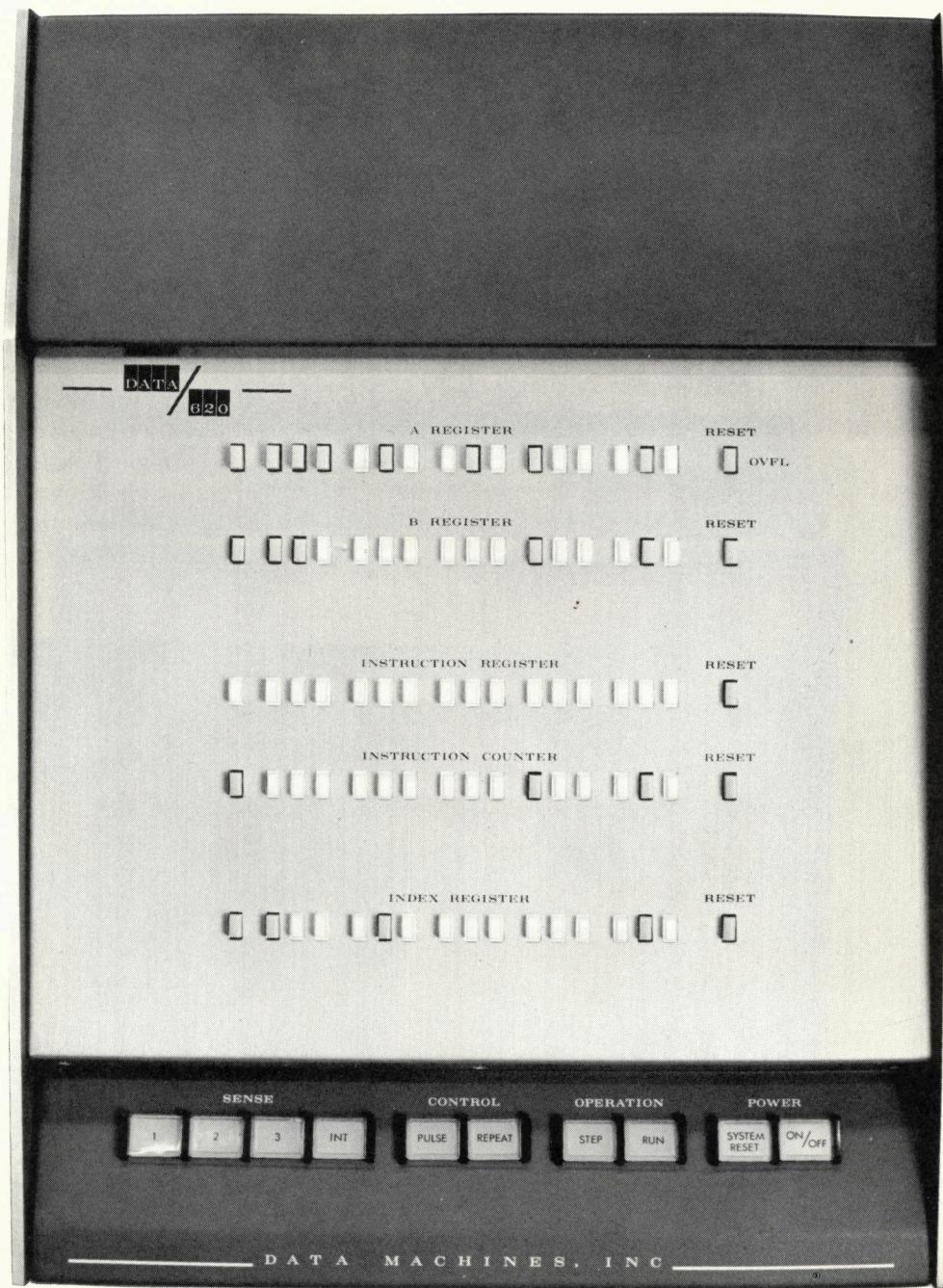
System Interface 21

- Data 620 System Organization (diagram) 23

User Interface 27

Accessories & Options 30

Manufacturing Facilities (inside back cover)



a true SYSTEM COMPUTER has got to be different!

There is much talk these days about the need for system computers. It's about time. There is really no excuse for making a system engineer, who already has a roomful of electronic gear to look after, have to negotiate with the computer in his system as though it were an independent foreign power. But the need is not met by taking a computer originally intended for use in an office or laboratory, slapping a coat of olive drab paint on it, fitting it into a bay of 19-inch racks, and calling it a system computer.

No. The need is for a different kind of computer—a data machine that is the product of a pervasive design philosophy oriented in every particular toward optimizing system performance. Only with such a machine will the prerogatives of system operation be put back where they belong: with the user system engineer. The DATA 620 is such a machine.



Some of the differences between a true system computer and one designed for conventional scientific/engineering use are obvious. Some are subtle. Close examination of details will identify the superior data machine. This booklet discusses, under the following headings, some of the more important of these details as they pertain to the DATA 620.

THE DATA MACHINE

As a physical system component, the DATA 620 is compact in size, occupying only 26 $\frac{1}{4}$ inches of rack space; it is accessible from the front like other system components; it is reliable and maintainable. Contents of all registers are continuously displayed on the front panel. Ninety-five percent of the computer can be checked out and debugged from the front panel without even having to use an oscilloscope. As the controlling element in a system, the DATA 620 has the "raw" data manipulating power of a much more costly computer—including 107 basic machine commands, microprogrammability, and canny special commands which are hardware-implemented and therefore exceedingly efficient. For example, MICRO-EXEC—a proprietary hardware technique for micro-step sequencing—permits subroutine processing at nanosecond speeds.

THE DATA MACHINE / SYSTEM INTERFACE

The DATA 620 was designed with the input-output requirements of other system functions in mind. A Party-Line I/O provides a single plug-in channel for as many as 18 peripheral devices of any kind. An interleave data channel runs independently of the program; a memory overlap control allows simultaneous operation of memory and I/O and the time-sharing of memories with other system devices; standard modules enable the system engineer to interface external digital, analog and control signals with the DATA 620. These interface features, together with priority interrupts, external sense lines and external control lines, give the DATA 620 virtually every I/O facility available.

THE DATA MACHINE / USER INTERFACE

As must be the case in any machine that is required to do—and do well—a large number of data manipulation tasks which are unspecifiable in advance, flexibility was the motif in designing the DATA 620 software package. The goal was to achieve flexibility without creating big programming problems on the one hand, or falling into the easy habit of accepting hardware/software tradeoffs, on the other hand. In the DATA 620, hardware and software features reinforce each other. For example, there are five modes of single-word addressing, one of which permits direct addressing of four times as many words in store as is normally possible with conventional designs. Instructions can be data-oriented, e.g. by bytes. Multiply/divide, scale and loop control instructions are available as options to meet more demanding computation speed requirements. The macro-assembler provided allows function-oriented pseudo-ops to be defined and used. The FORTRAN supplied with the system is a subset of FORTRAN IV, and also includes provisions whereby function-oriented statements can be added.

The DATA 620 is the kind of machine that looks better and better, the more its obvious and subtle features are explored. Start with this booklet and see for yourself.

— DATA / 620 —

A REGISTER



B REGISTER



INSTRUCTION REGISTER



INSTRUCTION COUNTER



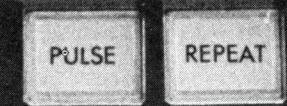
INDEX REGISTER



SENSE



CONTROL



OPERATION



ET

OVFL

ET

ET

ET

ET

POWER

SYSTEM
RESET

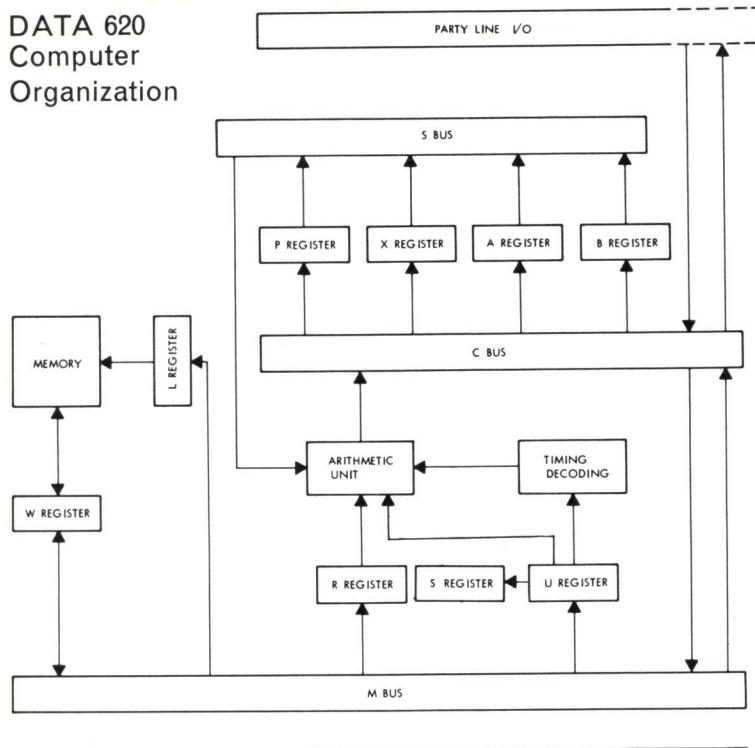
ON/OFF

The Data Machine

Organization

The DATA 620 is organized with a unique bus structure, selection logic, and nine registers. The organization provides universal internal information routing, buffered processing, micro-programming facility, information indexing without time penalty, and I/O trapping on a memory cycle basis. The organization optimizes the DATA 620 for maximum I/O throughput, minimum elapsed time between successive input or output transfers, and minimum programming.

This unique organization makes possible the facility by which complex algorithms can be implemented with external control hardware. This facility MICRO-EXEC produces an increase in processing speed in excess of 400 percent over conventional stored program techniques. This organization permits the system engineer to overcome traditional design barriers of processing speed, high rate/volume throughput, and data word length hardware.



M-Bus provides the parallel path and selection logic for routing data and instructions between memory, the I/O unit, the control unit, and the arithmetic unit. The M-Bus also provides a direct path to memory for the IN MEMORY and OUT MEMORY I/O instructions, and interlace I/O operations to occur simultaneous with extended arithmetic and shift commands.

C-Bus provides the parallel path and selection logic for routing data between the arithmetic unit, the I/O unit, the memory bus, and the operational registers. This bus permits data to be uniquely or commonly transferred to the operational registers. It performs the distribution function for micro-programming. The C-Bus provides a bidirectional parallel word path to the "Party Line" and the M-Bus. C-Bus is the central communication avenue and connects with all internal elements of the DATA 620. It is the key facility which permits MICRO-EXEC to be implemented.

S-Bus provides the parallel path and selection logic for routing data between the operational registers and the arithmetic unit. It implements the select, gather, and route function for micro-programming and MICRO-EXEC.

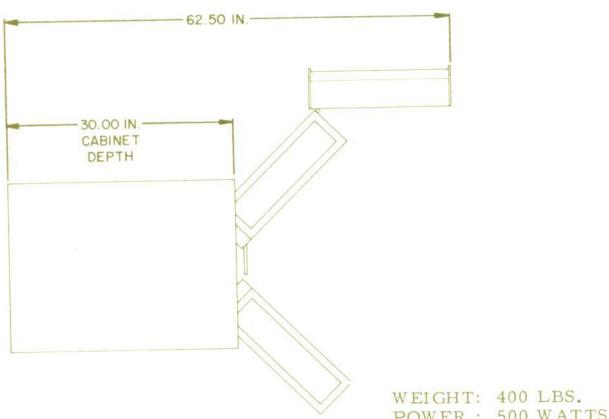
Party-Line Bus - provides a 16/18 bit parallel bidirectional I/O communication path. This bus includes the control lines for transfer ready, sense, control, interrupt address and acknowledge and information drop-ins. The "Party Line" is packaged as one-cable and each peripheral device has a party-line connector and a party-line extender connector. The device and the party-line form a daisy chain whereby additional subsystems can be added on site and on a plug-in basis.

Registers

Nine registers are provided with a basic DATA 620 and two more are added for each additional memory module. Four of the nine registers are incorporated to satisfy real-time system requirements. All the arithmetic and control unit registers are multi-purpose and can serve a unique micro-programming and MICRO-EXEC function. The memory register enables the memories to serve as multi-functional units for the total system.

R-register is an extra full word buffer which holds the multiplicand and divisor in arithmetic operations. R-register buffers the arithmetic unit from memory to permit interlace I/O operations to occur on a memory cycle by cycle basis. It is also a multipurpose register available to MICRO-EXEC.

U-register is an extra full word buffer which holds the instruction being executed. The U-register buffers the control unit from memory to permit interlace I/O operation to occur on a memory cycle by memory





cycle basis. It is also a multipurpose register available to MICRO-EXEC.

S-register is an extra 5 bit shift register which in combination with the U-register controls the length of shift instructions. This register buffers memory from the control unit also. S-register is available to MICRO-EXEC.

X-register is an extra full length register which permits indexing of memory addressing without adding time to accessing an indexed location. The X-register is addressable by the microprogramming instruction set where it serves logical, storage and counting functions. MICRO-EXEC can use the X-register for arithmetic and multiple other functions.

P-register is a full length register and is the program counter. P can serve multiple purposes under MICRO-EXEC, including select, set, shift and perform arithmetic and logical operations.

A-register is a full length register and is the high order half of the accumulator. A is a source and destination for programmed input/output and micro-programming. MICRO EXEC can select, set, shift, and perform arithmetic and logical operations on A.

B-register is a full length register and is the low order half of the accumulator. B is a source and destination for programmed input/output, micro-programmable, and can serve as the second hardware index register. MICRO-EXEC can select, set, shift, and perform arithmetic and logical operations on the B-register.

L-register is the memory location register and is 15 bits. The high order bits monitor the M-bus to recognize module selection. L can accept module addressing information from multiple sources enabling the memory module to serve as storage for more than one processor and/or device (with the DMA option). One L-register is supplied with each memory module.

W-register is the memory word register and is full length. W can accept information from multiple sources enabling the memory module to serve as storage for one or more additional processors and/or devices (with the DMA option). One "W" register is supplied with each module.

MICRO-EXEC (Optional) is a new and fresh technique with which the system designer has the option of externally combining and sequencing the DATA 620 micro-functions to perform a complex macro-function. Over 30 micro-function control lines are made available to the system user. These control functions are the micro-steps normally controlled by machine instructions. They control memory, arithmetic unit, control unit, all registers, I/O and communication networks. The memory can be operated in the Read/

Modify/Write, Read/Write, Clear/Write, and half-cycle read or write modes. The external control can operate the micro-steps as fast as five every 900 nanoseconds. The DATA 620 clock synchronizes the micro-step operations. MICRO-EXEC can be used to implement many types of algorithms. Typical functions are: convolutions, coordinate transformations, trigonometric, double precision arithmetic, floating point arithmetic, square root, limit checking, etc. MICRO-EXEC can produce a 10 to 1 speed advantage over stored programs and does not require DATA 620 memory for the program. The combination and sequence of micro-steps in MICRO-EXEC can be changed. MICRO-EXEC can command control over or be initiated by the DATA 620.

MICRO-EXEC opens new dimensions to the data system designer. It makes practical an extremely powerful and fast processor with small or large memories. It permits the mode of processing to be controlled externally. It permits the processing to be optimized for the system. To illustrate the possibilities for program innovation using MICRO-EXEC, in a training situation where it is desired to give students a "feel" for the computer's fundamental operations at the flip-flop level, such elementary functions could be implemented in MICRO-EXEC hardware and made accessible to the student for step-by-step manipulation.

The DATA 620 organization and hardware provides the system engineer with the most flexibility available in off-the-shelf equipment. The standard options of MICRO-EXEC, machine instructions, memory, and I/O facilities provide functional adaptability and system optimization without engineering risk or unpredictable costs.

Word Formats

SEE DIAGRAM (A) (B)

The word formats separate into two categories: data and instruction. Each category has been optimized for the system environment. The data format is extendable from 16 bit to 18 bit words in the high order positions. The BYTE class of instructions (optional) permits data bytes of any size to be processed and stored. The instructions have four formats, single word, double word, generic, and macro-command.

1. Single Word

DIAGRAM (C)

Twelve basic commands and two optional commands have single word memory reference formats. The 16 bit instruction word is divided into three fields as shown below. There are six addressing modes including direct addressing to 2048 words, relative to P with a delta range of 512, index by X or B, indirect from (a), immediate.

Single Word Instructions include:

LDA LDB LDX INR ADD SUB MUL*
STA STB STX ERA ORA ANA DIV*

All basic single word instructions are executed in two cycles, including relative and index addressing modes. Add 1 cycle for each level of indirect addressing.

The single word instruction format is designed to enable the system user to write his programs in the minimum number of memory locations and have his program executed in minimum time. The format is uncomplicated and the fields divide into convenient octal groupings so that programs can be written and checked rapidly.

2. Generic

DIAGRAM (D)

Twenty-six instructions are 16 bit single word generics and divide into the three fields of class code, operation code and definition.

*Optional

These instructions perform arithmetic unit, control unit and input/output functions. The operation are:

HLT, NOP, SHIFTS (12), OVERFLOW (2), SENSE, EXTERNAL FUNCTIONS, INPUT AND OUTPUT, A or B (11).

The shift instructions can shift up to 32 places. The sense and external function instructions can address up to 64 peripheral devices and define up to eight functions. The input and output commands can select A or B, A and B, clear and input to A or B, A and B. The input/output instructions can address up to 64 devices. (The in memory and out memory instructions and the interrupt priority control are two word instructions.)

The generics are octal grouped for user convenience. They provide flexibility to optimize input/output processing.

3. Two Word

DIAGRAM (E)

Two classes, six types, and one optional(*) type of instructions are two word instructions. The types include:

JUMP, JUMP and MARK, EXECUTE, IMMEDIATE, IN/OUT MEMORY, SENSE, INTERRUPT PRIORITY CONTROL, BYTE*.

The first word contains three fields, the C field contains the class code, the O field contains the operation code and the condition field specifies any combination of nine conditions. The nine conditions are: SS1, SS2, SS3, X=0, B=0, A=0, A-Neg., A-Pos., Overflow. The second word contains the jump address, jump mark address, or the address of the instruction to be executed. Indirect addressing is permitted. If the specified conditions are all met the instruction is executed. If the conditions are not met the

DIAGRAM (D)

DIAGRAM (A)

DATA WORD FORMAT

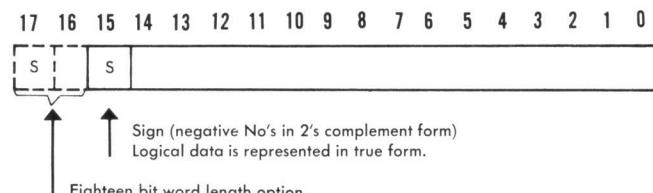


DIAGRAM (B)

INDIRECT ADDRESS FORMAT

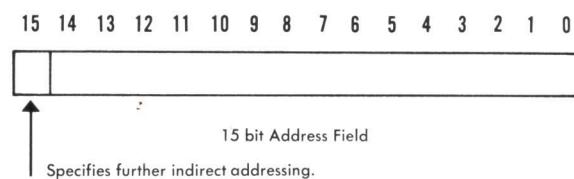
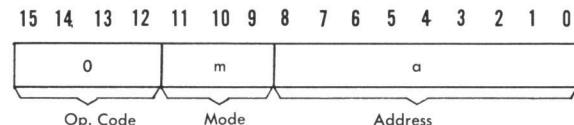


DIAGRAM (C)

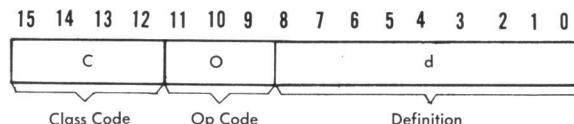
SINGLE WORD INSTRUCTION FORMAT



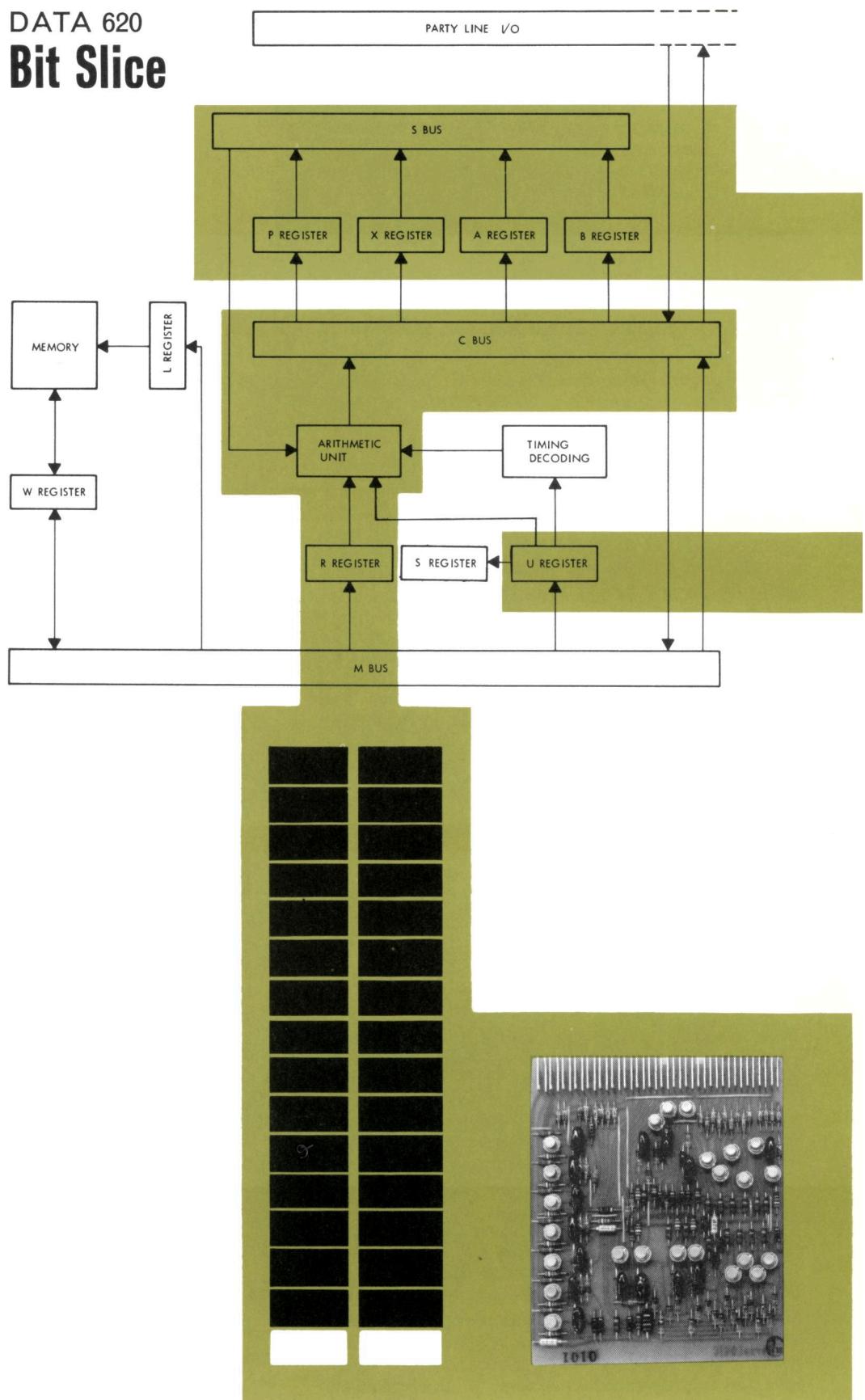
OXX	Direct addressing to 2048
100	Relative—add a field to P
101	Index (X)—add a field to X
110	Index (B)—add a field to B
111	Indirect—from a, multi-indirect.

DIAGRAM (D)

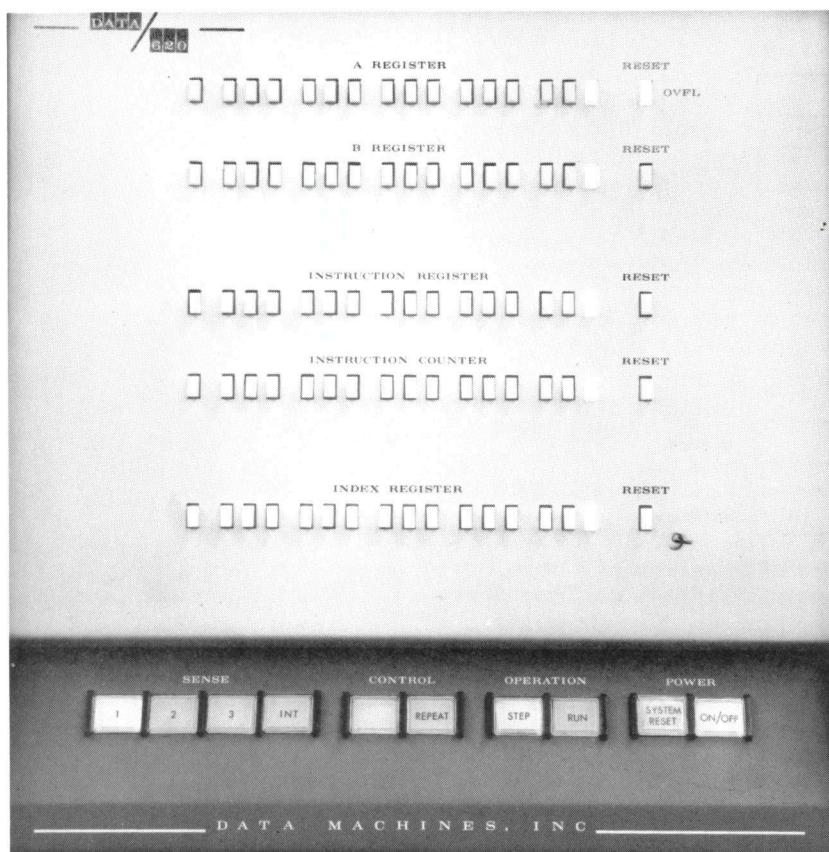
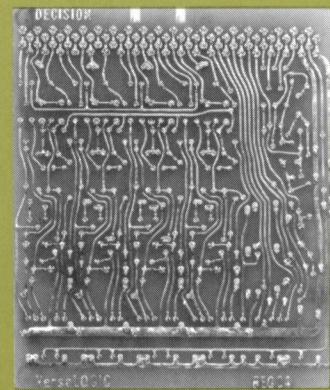
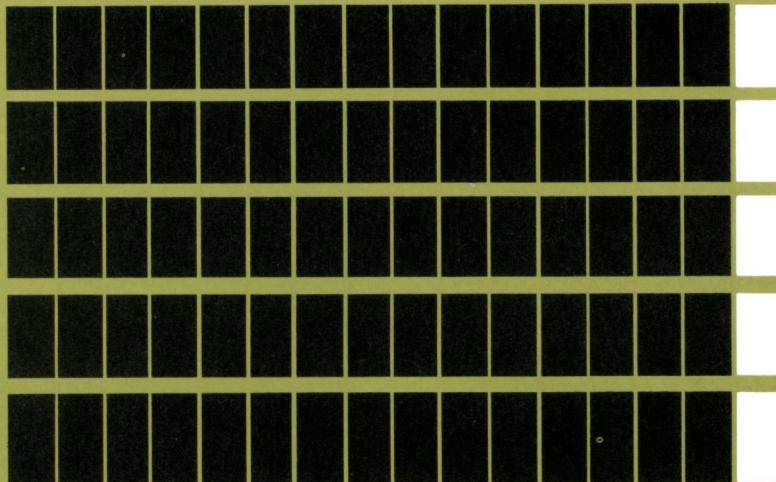
GENERIC INSTRUCTION FORMAT



DATA 620 Bit Slice



"Bit-Slice" is a technique whereby all the arithmetic unit and operational register circuits associated with one-bit are packaged on two cards which are mounted vertically and in a one-to-one correspondence with the bit positions on the control panel.



second word is skipped and the P-register incremented.

The IN/OUT MEMORY, INTERRUPT PRIORITY CONTROL, and BYTE* have a similar two word instruction format. The condition field of the INM/OTM instruction addresses the device selected, the second word contains the memory address for the data. Indirect addressing is permitted. The condition field of the interrupt priority control instruction contains the interrupt group address, the second word contains the interrupt priority arm/disarm mask. The second word of the BYTE* type instruction contains the 15 bit operand and jump address respectively. (Indirect addressing is permitted.)

IMMEDIATE is a special type instruction. The type includes twelve, plus two optional* two word instructions. The instructions include:

LDAI LDBI LDXI ADDI SUBI INRI MULI*
STAI STBI STXI ERAI ORAI ANAI DIVI*

SEE DIAGRAM (F)

Bits 3 through 6 define one of the instructions above. The IMMEDIATE type instructions provide literal addressing. Literal addressing, being the operand address field, contains the operand. This type automatically increments the P counter such that after the execution the next instruction is obtained from P + 2.

There are a total of 45 standard and over 16 optional two word instructions. The efficiency and power of the two word instructions becomes more and more apparent with use. They provide direct and random addressing and accessing to 32,768 words. They permit a two memory location sequence of instruction to replace the usual three memory location sequence in most cases. The amount of memory conserved and time saved by these instructions depends on the application, the range would be from 5 to 25%.

Macro-Commands

SEE DIAGRAM (G)

A number of micro-steps are programmable into a macro-instruction with the single word macro-command. This command has over 128 useful combinations in addition to those listed in the instruction repertoire. The macro-command format is:

The X, B, A register contents can be logical "ORed", cleared, transferred, set to a common value, complemented, "NORed", incremented, decremented, and if desired conditionally on an overflow. Sequences of micro-commands can be used to perform additional logical functions customary in a system environment.

The instruction repertoire is the most comprehensive available with a DATA 620 class com-

DIAGRAM (E)

JUMP, JUMP and MARK, EXECUTE FORMAT

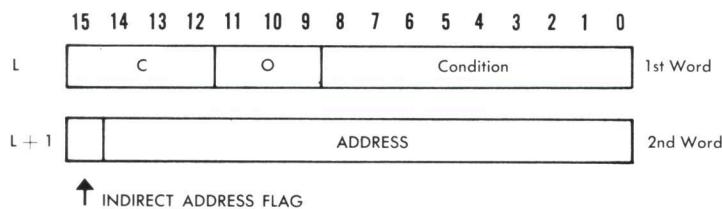
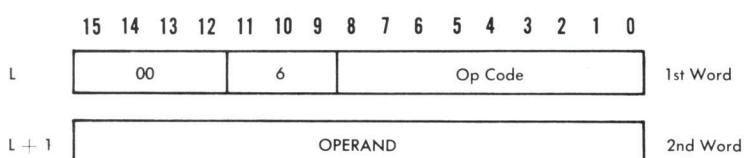


DIAGRAM (F)

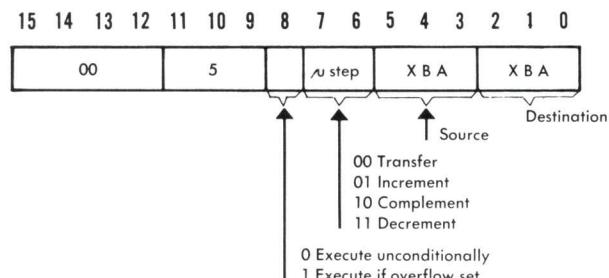
IMMEDIATE INSTRUCTION FORMAT



12

DIAGRAM (G)

MACRO-COMMAND FORMAT



DATA /
620

A REGISTER

RESET

OVFL

B REGISTER

RESET

INSTRUCTION REGISTER

RESET

INSTRUCTION COUNTER

RESET

INDEX REGISTER

RESET

SENSE

CONTROL

OPERATION

POWER

1 2 3 INT

PULSE

REPEAT

STEP

RUN

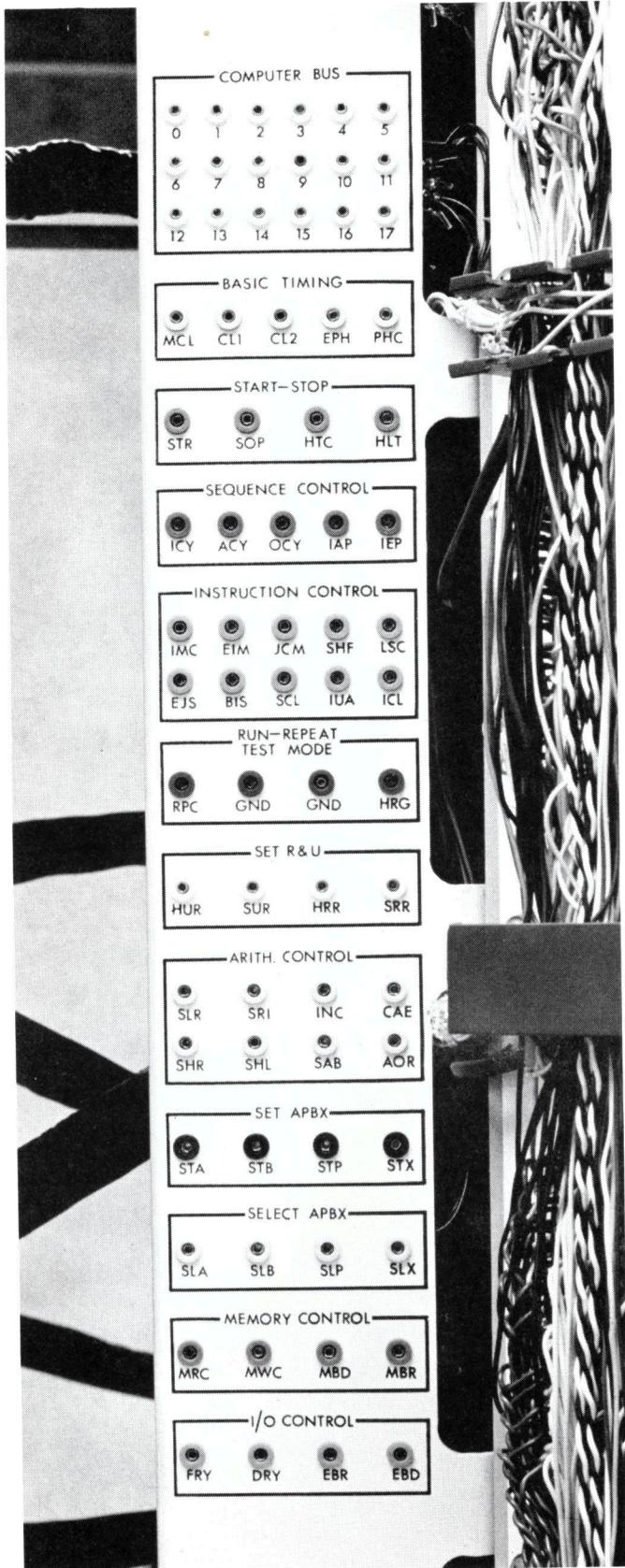
SYSTEM

RESET

ON/OFF

DATA MACHINES, INC

puter. They are job-oriented from first to last. The optional instruction sets have specific value to certain applications and are available to refine the DATA 620 to those applications. The repertoire, variety, simplicity, and power equates to economic optimization. The instruction list is presented in the following table.



Memory

DATA 620 memories are general purpose random access ferrite magnetic core memories. They contain a proprietary thermal compensation technique which preserves the operating margins over the temperature range (0° to 45°C) without adjustment. Each memory module contains a full word length data register and a fifteen bit location register. They are designed to service optional devices in addition to the DATA 620 processor. Under MICRO-EXEC or with the DMA option the memory can be operated in the following modes: Read/Write; Clear/Write; Read/Modify/Write and half-cycle Read or Write.

The memory communicates with the DATA 620 through a memory "Party-Line". Additional memory modules can be added simply by adding a "Party-Line" cable from the existing memory module to the new module. The memory "Party-Line" is accessible to the external system.

The memory can communicate with other system device through the optional direct memory access and overlap control unit. This option provides independence to the memory module. This independence changes the system analysis approach from considering the system computer an entity to a processing unit and a memory complex. The memory complex is then considered for serving the total system requirements.

The memories are available in 512, 1024, and 2048 and 4096 and 8192 word modules (16 or 18 bits per word). The memory cycle time is 1.8 microseconds; the access time is 700 nanoseconds.

Reliability and Maintainability

The circuits used throughout the DATA 620 are VersaLOGIC (T). These circuits are general purpose digital logic and are noted for low power consumption, packing density, high noise rejection, and reliability throughout the operating temperature range of 0° to 55°C . The low power equates to low heat generation and higher reliability.

The DATA 620 is produced under a quality control program designed and practiced to fully meet MIL Q 9858A and to the intent of NPC 200-3. The mean time between failures (MTBF) has been calculated for the basic DATA 620 to be over 7,500 hours. The mean-time-to-repair is estimated to be in minutes.

The DATA 620 is packaged to simplify maintenance. The circuit board layout is unique using a "bit-slice" layout. "Bit-Slice" is a technique whereby all the arithmetic unit and operational register circuits associated with one-bit are packaged on two cards which are mounted vertically and in a one-to-one correspondence with the bit positions on the control panel. This technique also simplifies the expansion of the DATA 620 from a 16 bit to an 18 bit configuration. The structure is designed for front access. All units of the computer are mounted on slides which makes all components and wiring easily acces-

DATA

620

Specifications

TYPE	A System Computer, general purpose digital, designed for on-line data system requirements, magnetic core memory, binary, parallel, single-address, with bus organization and micro-control.										
MEMORY	Magnetic Core, 16 bits (18 bits optional), 1.8 microseconds full cycle, 700 nanoseconds access time, 512 words minimum, 4096 words standard, expandable in 4096 or 8192 word modules to 32,768 words, power failure protection (voltage and frequency), non-volatile. Each module with data and address register. Memory operates for processor or direct memory access channel. Thermal overload protection.										
ARITHMETIC	Parallel, binary, fixed point, 2's complement.										
WORD LENGTH	16 bits standard; 18 bits optional.										
SPEED (FETCH & EXECUTE)	<table border="0"> <tbody> <tr> <td>Add or Subtract</td><td>3.6 microseconds</td></tr> <tr> <td>Multiply (optional 18 bits)</td><td>18.0 microseconds 19.8 microseconds</td></tr> <tr> <td>Divide (optional 18 bits)</td><td>18.0 to 25 microseconds 19.8 to 28.8 microseconds</td></tr> <tr> <td>Register change class</td><td>1.8 microseconds</td></tr> <tr> <td>Input/Output—from A or B from Memory</td><td>3.6 microseconds 5.4 microseconds</td></tr> </tbody> </table>	Add or Subtract	3.6 microseconds	Multiply (optional 18 bits)	18.0 microseconds 19.8 microseconds	Divide (optional 18 bits)	18.0 to 25 microseconds 19.8 to 28.8 microseconds	Register change class	1.8 microseconds	Input/Output—from A or B from Memory	3.6 microseconds 5.4 microseconds
Add or Subtract	3.6 microseconds										
Multiply (optional 18 bits)	18.0 microseconds 19.8 microseconds										
Divide (optional 18 bits)	18.0 to 25 microseconds 19.8 to 28.8 microseconds										
Register change class	1.8 microseconds										
Input/Output—from A or B from Memory	3.6 microseconds 5.4 microseconds										
OPERATIONAL REGISTERS	<p>A-register—accumulator, input/output, 16/18 bits. B-register—double length accumulator, input/output, index register, 16/18 bits. X-register—index register, 16/18 bits. P-register—program counter, 16/18 bits.</p>										
BUFFER REGISTERS	<p>R-register—operand register, 16/18 bits. U-register—instruction register, 16/18 bits. S-register—shift register, 5 bits, operates with the U-register for executing shift instructions. L-register—memory address register, 15 bits, one L-register per memory module. W-register—memory word register, 16/18 bits, one W-register per memory module.</p>										
CONTROL	<p>Addressing Modes—Six Direct addressing to 2048 Relative to P register 512 words Index with X-register, hardware, does not add to execution time Index with B-register, hardware, does not add to execution time Multi-level indirect addressing Immediate Instruction Types—Four Single Word Double Word Generic Micro-command</p> <p>Instructions: 107 standard, over 128 macro instructions, plus 28 optional, consisting of:</p> <ul style="list-style-type: none"> 3 Load 3 Store 5 Arithmetic (2 optional) 3 Logical 10 Jump 10 Jump and Mark 10 Execute 14 Immediate (2 optional) 										

Type	Mnemonic	Description	Time Cycles
Load	LDA	Load A Register	2
	LDB	Load B Register	2
	LDX	Load X Register	2
Store	STA	Store A Register	2
	STB	Store B Register	2
	STX	Store X Register	2
	ADD	Add to A Register	2
	SUB	Subtract from A Register	2
Arithmetic	INR	Increment and Replace	3
	MUL*	Multiply B Register, Double Length	10
	DIV*	Divide AB Register, Double Length	10-14
Logical	ERA	Exclusive OR to A Register	2
	ORA	Inclusive OR to A Register	2
	ANA	And to A Register	2
Jump	JMP	Jump UNCONDITIONALLY	2
	JOF	Jump if Overflow SET	2
	JAN	Jump if Register NEGATIVE	2
	JAZ	Jump if A Register ZERO	2
	JAP	Jump if Register POSITIVE	2
	JSSI	Jump if Sense Switch 1 SET	2
	JSS2	Jump if Sense Switch 2 is SET	2
	JSS3	Jump if Sense Switch 3 SET	2
	JXZ	Jump X Register ZERO	2
	JBZ	Jump B Register ZERO	2
Jump and Mark	JMPM	Jump UNCONDITIONALLY and Mark	2
	JOFM	Jump Overflow SET and Mark	2-3
	JANM	Jump A Register Negative and Mark	2-3
	JAZM	Jump A Register ZERO and Mark	2-3
	JAPM	Jump A Register Positive and Mark	2-3
	JS1M	Jump Sense Switch 1 SET and Mark	2-3
	JS2M	Jump Sense Switch 2 SET and Mark	2-3
	JS3M	Jump Sense Switch 3 SET and Mark	2-3
	JXZM	Jump X Register ZERO and Mark	2-3
	JBZM	Jump B Register Zero and Mark	2-3
Execute	XEC	UNCONDITIONAL Execute	2
	XOF	Execute Overflow SET	2
	XAN	Execute A Register NEGATIVE	2
	XAZ	Execute A Register ZERO	2
	XAP	Execute A Register POSITIVE	2
	XS1	Execute Sense Switch 1 SET	2
	XS2	Execute Sense Switch 2 SET	2
	XS3	Execute Sense Switch 3 SET	2
	XXZ	Execute X Register ZERO	2
	XBZ	Execute B Register ZERO	2
Immediate	LDAI	Load A Register Immediate	2
	LDBI	Load B Register Immediate	2
	LDXI	Load X Register Immediate	2
	STAII	Store A Register Immediate	2
	STBI	Store B Register Immediate	2
	STXI	Store X Register Immediate	2
	ADDI	Add to A Register Immediate	2
	SUBI	Subtract from A Register Immediate	2
	MULI*	Multiply B Register Immediate	10
	DIVI*	Divide AB Register immediate Double Length	10-14
INRI		Increment and Replace Immediate	3
	ERAI	Exclusive OR to A Register Immediate	2

DATA 620 Instruction List

Input/Output	EXC	External Control Function	1
	CIA	Clear and Input to A Register	2
	CIB	Clear and Input to B Register	2
	CIAB	Clear and Input to A and B Registers	2
	INA	Input to A Register	2
	INB	Input to B Register	2
	INAB	Input to A and B Registers	2
	INM	Input to Memory	3
	OAR	Output A Register	2
	OBR	Output B Register	2
	OAB	Output OR or A and B Registers	2
	OTM	Output from Memory	3
	SEN	Sense Input/Output Lines	2-3
Register Change	IAR	Increment A Register	1
	DAR	Decrement B Register	1
	IBR	Increment A Register	1
	DBR	Decrement B Register	1
	IXR	Increment X Register	1
	DXR	Decrement X Register	1
	CPA	Complement A Register	1
	CPB	Complement B Register	1
	CPX	Complement X Register	1
	TAB	Transfer AR to B Register	1
	TBA	Transfer BR to A Register	1
	TAX	Transfer AR to X Register	1
	TBX	Transfer BR to X Register	1
	TXA	Transfer XR to A Register	1
	TXB	Transfer XR to B Register	1
	TZA	Transfer Zero to A Register	1
	TZB	Transfer Zero to B Register	1
	TZX	Transfer Zero to X Register	1
	A0VA	Add OV to A Register	1
	A0VB	Add OV to B Register	1
	A0VX	Add OV to X Register	1
	SOVA	Subtract OV from A Register	1
	SOVB	Subtract OV from B Register	1
	SOVX	Subtract OV from X Register	1
	SOV	Set Overflow	1
	ROV	Reset Overflow	1
Logical Shift	LSRA	Logical Shift Right AR k places	1 + .25 k
	LRLA	Logical Rotate Left AR k places	1 + .25 k
	LSRB	Logical Shift Right BR k places	1 + .25 k
	LRLB	Logical Rotate Left BR k places	1 + .25 k
	LLSR	Logical Shift Right k places	1 + .25 k
	LLRL	Logical Rotate Left k places	1 + .25 k
Arithmetic Shift	ASRA	Arithmetic Shift Right AR k places	1 + .25 k
	ASRB	Arithmetic Shift Right BR k places	1 + .25 k
	ASLA	Arithmetic Shift Left AR k places	1 + .25 k
	ASLB	Arithmetic Shift Left BR k places	1 + .25 k
	LASR	Long Arithmetic Shift Right k places	1 + .25 k
	LASL	Long Arithmetic Shift Left k places	1 + .25 k
Control	HLT	Halt	1
	NOP	No Operation	1

*Denotes optional instruction. Times given are for 16-bit computer.
Add 1 cycle for each level of indirect addressing.

SPECIFICATIONS (Cont.)

- 13 Input/Output
- 26 Register Change
- 6 Logical Shift
- 6 Arithmetic Shift
- 2 Control
- 6 Byte (optional)
- 14 Extended addressing (optional)
- Over 128 micro-instructions

MICRO-EXEC (Optional)

Facility and hardware to construct a hardware program external to the DATA 620. Eliminates stored program memory accessing by use of hardware program.

Console

Display and data entry switches on all operational registers; 3 sense switches; manual interrupt; automatic load option; instruction repeat; single step; run; power on/off.

Maintenance Panel

Contains test points and jacks for: Computer Bus, Basic Timing, Start/Stop, Sequence Control, Instruction Control, Run-Repeat Test, Set R & U, Arithmetic Control, Set Registers, Select Registers, Memory & I/O Control.

INPUT/OUTPUT**Data Transfer**

Four modes: Single word to/from memory (program control); single word to/from arithmetic registers (program control); Buffer Interface Control (optional—up to 200,000 words/sec.) Direct Memory Access (optional—555,000 words/sec. max.)

I/O Party-Line Access (standard) over 200,000 word/sec.

Memory Party-Line Access (standard) to 555,000 words/sec.

External Control and Program Sense

Up to 512 external control lines, up to 512 external sense lines.

Interrupts

Power failure/thermal overload and console interrupts standard. Priority interrupts expandable in groups of eight (interrupt of interrupt), enable/disable and individual arm/disarm. Each interrupt line has unique memory destination address.

Dimensions

Main Processor (up to 8k and 18 bits)—26 $\frac{1}{4}$ inches high, 19 inches wide, 28 inches deep; memory power supply—5 $\frac{1}{4}$ inches high; logic power supply—5 $\frac{1}{4}$ inches high.

Access

Front: All chassis, drawer and/or page mounted for full front access.

Weight

400 lbs.

Power

500 watts, single phase, 115 \pm 10V, 60 \pm 2 cps. Power supplies are regulated. Additional regulation is not required under normal commercial power sources. A constant voltage ferroresonant transformer provides magnetic regulation of the —12V output. The +6V output is zener regulated.

Construction

Modular, logic pages unhinge and unplug. All drawers are connector coupled. Bit/slice packaging. Remote control panel (optional).

Expansion

Main processor contains provisions and space for all internal options and memory expansion to 8192 (16/18 bit) words. Peripheral controllers and special interfaces available in 7-inch drawers. Memory module book racks of 4096 and 8192 words available for expansion to 32,768 words (plug-in).

Installation

Mounts in standard 19 inch cabinet, no air conditioning, sub-flooring or special wiring and site preparation required.

Environments

0°C to 45°C; 0 to 90% relative humidity.

LOGIC AND SIGNALS

8 mc VersaLOGIC, 2.2 mc clock, logic levels 0V false, —12V true. Noise rejection 6V. Worst-case design.

SOFTWARE

Complete package, includes: Assembler, Library Subroutines, AID, Maintain, Diagnostics, and FORTRAN. Modular in construction, expandable for application orientation.

sible. A comprehensive maintenance panel is provided which contains jacks to all vital test monitor and control points. See photo on Page 14. The design, layout, documentation and maintenance provisions satisfy the criterion "The System Computer must be designed such that a system user can feel secure when maintaining the computer himself".

Failure Prevention: The source of faults in a solid state electronic computer with conservative circuit and timing designs is from external causes. The external causes are power failures, power frequency failures, environmental thermal overloads, radio frequency interference, and the failure of electro-mechanical peripheral devices. The DATA 620 has been designed to prevent each of these fault sources from destroying the integrity of the system computer function.

1. A power failure interrupt system is standard. This system monitors power line voltage and frequency. If voltage and/or frequency falls outside the safe range, the DATA 620 is automatically interrupted. The interrupt routine programs a save and shutdown condition before the power failure can degrade operation.
2. A thermal sensor is embedded in the DATA 620 to continually monitor internal temperature. If the temperature rises above the specified limit (45°C) the sensor initiates a fault interrupt. The interrupt routine programs a save and shutdown condition before the thermal overload can degrade operation.
3. The DATA 620 is designed to mount in standard 19 inch rack. If a severe radio frequency interface environment is predicted, the DATA 620 can easily be mounted in RFI cabinets. DATA 620 has the highest noise immunity circuits available. The noise rejection is 6V at -12 and over 2V at 0. Twisted pair wiring is used on high frequency signals. The clock frequency is 2.2 mc.
4. The DATA 620 guards against errors generated by peripheral equipment. Parity is generated for data transmissions to storage type peripheral equipment and is checked when data is received from such devices. DATA 620 programs can request retransmissions and/or signal that an error exists.
5. Real-Time clocks and watchdog timers are available as system safety options. The DATA 620 includes instructions which prevent computer hangup from non-responding input/output equipment.
6. The control panel is electrically disconnected during "run" mode. A key lock is available (Option) which disconnects all console controls in a "run" or "off" mode.

These facilities provide the level of assurance necessary for a system engineer to use the DATA 620 to tackle the most demanding process control applications where one failure can be dangerous and extremely costly.

Physical

Packaging:

The DATA 620 is packaged to offer the user maximum convenience, positioning flexibility, and space-saving economies. The memory, arithmetic and control unit, and operator console are packaged as separate units. The inter-connections between these units are connectors. The arithmetic and control unit forms one page in the book type mounting. The memory forms the other page. Each page is connected to the chassis with a piano type hinge. The DATA 620 assembles and disassembles easily into five light-weight portable units. The control console can be remote up to 25 feet. This packaging technique enables the DATA 620 to be positioned into tight quarters and users' cabinets, 19" relay racks, consoles, mobile vans, aircraft, ships, submarines, etc. The compactness and light-weight make it practical to mount the computer on a mobile cart and move it from test station to test station.

Control Panel:

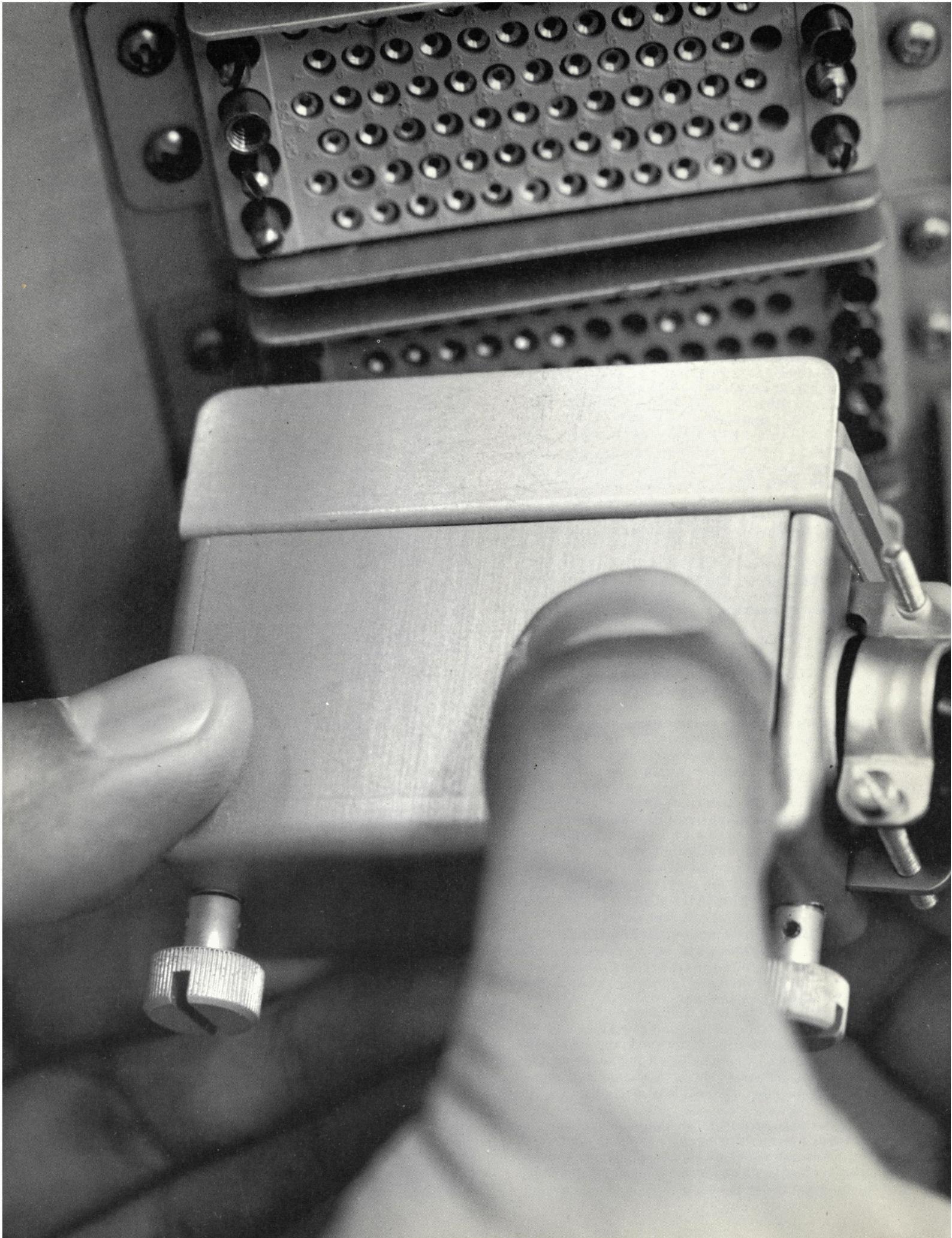
The DATA 620 Control Panel is illustrated in the following Figure. All operational registers are displayed. The display lights are also data entry buttons. The data entry facility is automatically disconnected during "RUN" mode to avoid accidental errors. A panel lock option is available which electrically disconnects the controls. The following controls and displays are provided.

Item	Data Entry	Display	Control
Overflow		X	
A-Register	X	X	
B-Register	X	X	
Instruction Register (U)	X	X	
Instruction Counter	X	X	
Index Register (X)	X	X	
Power On/Off		X	X
Operate Run	X		X
Operate Step	X		X
Load (Optional)	X		X
Repeat	X		X
Console Interrupt	X		X
Sense Switch 1	X		X
Sense Switch 2	X		X
Sense Switch 3	X		X

The control panel has been optimized for user convenience to prepare programs, inspect operation, and verify machine operations.

Environmental

The DATA 620 connects to standard commercial single phase 115 power. Power regulation is not required under normal commercial power conditions. Subflooring or conditioned air are not required. All the cooling required to operate over the temperature range of 0° to 45°C is supplied by the blowers contained in the DATA 620. The DATA 620 feels equally at home in the shop, field, instrumentation room, classroom, and laboratory.





The Data Machine System Interface

System Interface

The Data Machine adapts to the System Requirement. This adaptability is an excellent criterion for determining a true systems computer. The DATA 620 offers the widest range of interface facility. Eight types of input output facilities are available. These include: Party Line, multilevel priority interrupts, external sense lines, external control lines, buffer interlace control, direct memory access control I/O "Party-Line" access and Memory "Party-Line" access. The "Party-Line" can be coupled with the buffer interlace control to form a combination, automatic and/or program controlled I/O facility.

Party Line

The "Party-Line" is a bidirectional common communication channel containing the data and control lines required for system communication. It is designed to prevent conflicts or traffic jams under heavy communication loads. Each transmission contains the routing information as well as the data. It is transmitted as an entity which is not separable by interrupt or trap. Thus, numerous devices can time share the "Party-Line" on a window of 1.8 microseconds. The transmission has two phases. Each phase is 900 nanoseconds. The first phase is the route set-up, the second is the data transmission.

The following control and data lines are contained in the "Party-Line". Sixteen bidirectional data lines, function ready line (FRY), data ready line (DRY), sense response line, 1.1 mc clock line, the Buffer Interlace control lines, and the priority interrupt system control lines.

Information can be placed on or received from the "Party-Line" from the following sources: the Data Machine memory, the A and B register, the interrupt system and all peripheral devices. The Data Machine program and the Buffer Interlace Control unit can control "Party-Line" communication.

The "Party-Line" permits "plug-in" expansion of all peripheral devices. The party-line contains line drivers and line receivers to service up to eighteen peripheral devices. Each peripheral device contains a data buffer and party-line adapter. Thus no device can "tie-up" the party-line and modifications to the Data Machine are not required to add peripherals. Each device has a party-line connector and a party-line extender connector. The last device on the party-line has a termination shoe on the extender connector. When another device is added, a party-line cable is provided between the added and the last device. The termination shoe is moved to the added device. The following figure shows the party line connectors.

The party-line technique solves the troublesome problems usually encountered in time shared operation and on-site system expansion.

Interrupt System (Model 620-27)

The DATA 620 has a multi-level priority interrupt system incorporating single execute, on-off, and selective arm/disarm capability. Each interrupt line is assigned a unique memory destination address consisting of two locations. This address is transmitted to the DATA 620 when an interrupt is acknowledged. The system is modular and expandable in sets of eight. The interrupts form groups of 16. Each group of 16 has a unique party-line address. Up to 64 groups of 16 can be added to the DATA 620. Two interrupts are provided with the DATA 620. The first and highest priority is connected to the failure protection system. The other is connected to the console interrupt switch. An interrupt functional response to the external device can be accomplished in as little as 2 cycle times.

22

Each interrupt line has an enable/disable flip-flop which is addressable and set by the interrupt control instruction. The interrupt system is automatically scanned every 900 nanoseconds and the program interrupt occurs before the fetch cycle of the next instruction to be executed. If signals exist on one or more interrupt lines, the highest priority line is recognized. The interrupt system is automatically inhibited until the first instruction at the interrupt memory destination is executed. Termination of the inhibiting is under program control. The program can

maintain the existing order of priority levels or re-order to meet dynamic queing. The order is determined by a 16-bit mask transferred to the external interrupt system by the program. The external action initiated by the interrupt subroutine causes the interrupting device to remove the interrupt signal.

The interrupt subroutine can remove the inhibit and selectively enable or disable lines to permit interrupts of higher or lower levels to interrupt the level being processed.

An interrupt automatically causes the instruction located at the unique destination to be executed. The instruction can be any DATA 620 instruction. This technique permits the interrupts to be "single execute" whereby single instruction responses to external interrupts can be serviced in one instruction time. A real-time clock can be implemented with an interrupt line and an external pulse generator. An automatic data channel can be implemented with as little as two interrupt lines. The DATA 620 interrupt system provides the high speed reaction time, expansion capability, priority and queing versatility and functional flexibility required for real-time control.

Sense Lines (Model 620-25)

Discrete sense lines are available as options in sets of eight. Each sense line has a unique address. Up to 512 sense lines can be addressed. The sense instruction is a two word conditional jump command. If a signal exists on the sense line addressed the program jumps to the effective address, otherwise the program continues at location P + 2. The sense lines can be configured in combination with the interrupt lines to permit more than one device to share an interrupt line. All DATA 620 peripheral options include the sense lines required.

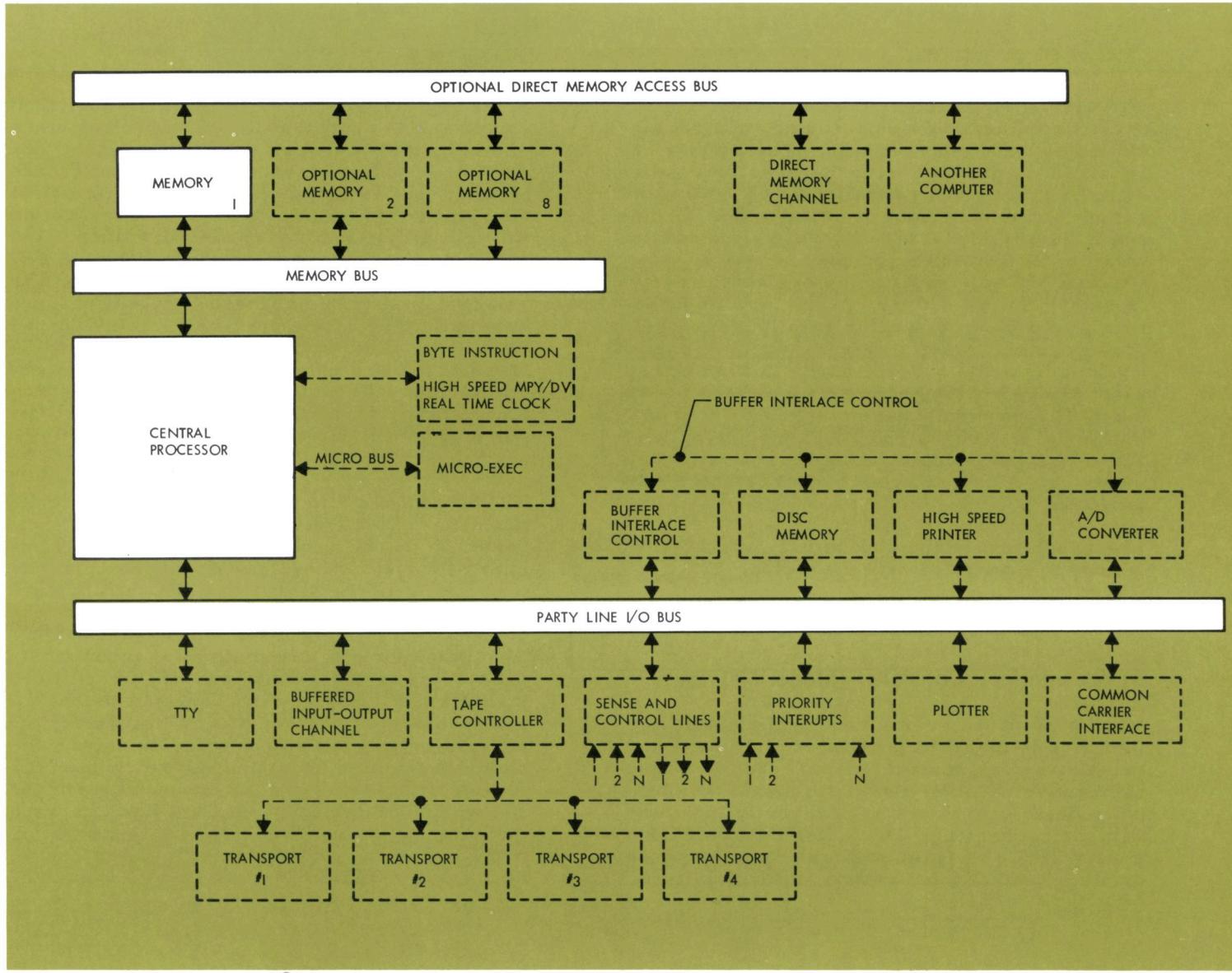
External Control Lines (Model 620-26)

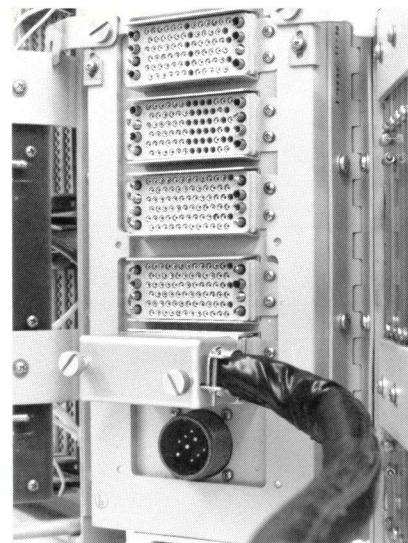
Discrete control lines are available as options in sets of eight. Each control line has a unique instruction address. Up to 512 control lines can be addressed. The external control instruction is a one word instruction which places a pulse on the addressed control line. These are general purpose control lines that can be used to perform external control functions throughout a system. The control pulse is at -12V and has a 450 nanosecond width. The control lines required by DATA 620 options are provided with the option.

Parallel I/O Channels (Models 620-20, 3)

The usual system application requires special devices to be connected to the computer. These devices can interface with the computer in many ways. The system designer can implement the interface with his own electronics, purchase and assemble the appropriate logic modules (VersaLOGIC); or select the assembled party-line adapter required by the device.

DATA 620 System Organization





The party-line adapters contain the device address decoding, function decoding, control signal inputs and response logic. The adapter can be supplied with a word parallel data gating structure, a word parallel data buffer and gating, for either input or output. The models available are Model 620-20, party-line adapter with 16/18 bit buffer for parallel data output. This services system devices which receive "levels." Model 620-21, party-line adapter with 16/18 bit buffer for parallel data input. This services system devices which transmit "pulses." Model 620-22, party-line adapter with 16/18 bit gating structure for parallel data input. This services system devices which contain buffers. Model 620-23 party-line adapter with 16/18 bit gating structure for parallel data input. This services system devices which contain buffers.

The party-line adapter required by DATA 620 options are provided with the option.

Buffer Interlace Controller (Model 620-15)

Many system devices require Data Machine facilities to transmit I/O data at high rates and volumes and at random periods. Such devices are best serviced by automatic means which do not require programming or directly interfere with the processing. The Buffer Interlace Controller (BIC) option services such requirements. The BIC contains two 15-bit registers,

party-line interfacing logic, priority logic and Data Machine control logic. The two registers maintain the current and final memory addresses of a data block. These registers are initially loaded by the program with the first and last addresses. These addresses define the sequential locations in memory to or from which the data is communicated. Once the BIC is initialized with the addresses, a device is selected and started. The I/O operations are automatic thereafter until the current address equals the final address. Data words can be transferred at a nominal rate of 200,000 words per second. The BIC automatically synchronizes the data transmission rate to that required by the device.

The BIC connects to the I/O Cable and controls the data transmission for those devices connected to the BIC. Interlaced input/output occurs on a memory cycle basis and has priority over the Data Machine. The BIC will capture the next memory cycle and stall the Data Machine for 2.7 μ s for each word transmitted. The Data Machine automatically resumes its processing at the completion of each word transferred. Any device connected to the BIC can be operated under control of the BIC or under program control. Any device may be adapted to function under the control of the BIC. An interrupt line may be connected with the BIC which will interrupt the Data Machine when the transfer of the data block has been terminated. The current address register can be read into the DATA 620 under program control.

Direct Memory Access and Overlap Control (Model 620-14)

Complex data systems frequently require data buffering and multiple simultaneous communications. The functional processing may be time phased, such that during one phase the system is in "data acquisition and quick look" and another phase "data analysis". During the "data acquisition" phase maximum throughput is required. During the "data analysis" maximum processing rates are desired. These objectives can be better realized if the memory complex is modular and can service multiple-purposes. The Direct Memory Access and Overlap Control option provides that capability.

The Direct Memory Access and Overlap Control (DMA) provides an additional memory hub, priority and control logic, and a memory bus. The additional memory hub makes available the W register, the L register, and the memory control signals on lines isolated from the Data Machine memory bus. The priority and control logic gives the DMA priority over the Data Machine when both units simultaneously access a memory module. The additional memory bus provides a communication facility for system devices to communicate with the memory module over an independent bus. A second Data Machine can be connected to this memory bus. An overlap control option must be added to each memory module which is to service multiple functions in the data system. One DMA's can be added to each memory module. The DMA enables the memory modules to operate simultaneously in the general purpose memory modes of: Read/Write, Read/Modify/Write, Clear/Write, and half-cycle Read or Write.

Peripheral Equipment

A full line of compatible peripheral equipment is available for the DATA 620. The model numbers and description of the peripherals are contained in the table: DATA 620 AND OPTIONS see Page 30. Each device has been selected for meeting the functional requirements of on-line and real-time data system.

The peripheral option is provided with a party-line adapter, buffering, control lines, and the utility software. The line printer, disc file, and magnetic tapes include word assembly/disassembly registers.

The peripherals will operate with the party-line under program control or automatically with an (optional) Buffer Interlace control unit.

The performance specification of data conversion equipment depends on the system application. The configuration conversion precision, high and low-level multiplexing, conversion rates, mode of operation, are normally contained in the user's performance specification. Therefore, the conversion equipments for meeting user performance specifications are offered on a custom basis.

6320

A REGISTER



B REGISTER



INSTRUCTION REGISTER



INSTRUCTION COUNTER



INDEX REGISTER



OPERATION



N C

RESET

OVFL

ESET

The Data Machine User Interface

System Software

The programming aids provided with the DATA 620 were designed and developed with the principle objectives of maximizing user productivity and efficiency. The programming languages and library subroutines conform to the most widely used standards and conventions. A program analysis package aids the user in timing and perfecting his real-time programs. The software is modular in design such that user-oriented macros, pseudo operations, compiler statements, special hardware test routines, and Input/Output drivers can be added. The documentation describes the construction and operation and contains a separate treatise describing how the user can add to or select a set of the standard software to enhance the effectiveness of the software for his particular application and system configuration.

Fortran

A one-pass modular FORTRAN is provided which is a subset of FORTRAN IV and operates on a 4k basic DATA 620. The full structure for FORTRAN IV as a language compilation is optional for expanded systems. Application-oriented statements such as TEST UNIT, SORT, MERGE, SYS, INTERRUPTS, as well as recursive subroutines and memory re-allocation procedures can be added. The FORTRAN has been developed to combine the conveniences of FORTRAN language programming with a modular open-ended construction to provide an efficient programming aid adapted to the particular real-time application and DATA 620 system configuration.

DAS Assembler

The DATA 620 ASSEMBLY SYSTEM (DAS) is a modular two-pass symbolic assembler which operates on a basic 4k DATA 620. The conventions and standards most widely used have been followed for user convenience. Increasing the effectiveness of an assembler for a specific application and system configuration is a function of the ease by which application-oriented Macros can be added and library subroutines called. The DAS executive program will CALL library subroutines and produce object code in absolute or relocatable form. Pseudo Ops include: BEGI, USE, ORG, BSS, BES, EQU, SET, MAX, MIN, DUP, DATA, PZE, MZE, CALL, ENTR, RETU, SPAC, LIST, NLIS, SMRY, DETL, END, MORE, COMN, EXT, NAME, IFT, IFF, GOTO, OPSY, REL, FORT, CONT, NULL, EJEC. DAS includes LITERALS, EXPRESSIONS, ARITHMETIC OPERATORS, and DECLARATIVES. DAS equally satisfied the one-time application programming and/or the user continually developing new programs.

AID

The program analysis package (AID) consists of routines to check out and correct application programs, calculate the execution time of real-time programs and an on-line executive program through which the user directs the program analysis. AID is compact and relocatable. The executive portion of AID can remain resident in memory to provide utility function such as loading absolute or relocatable, providing subroutine linkages, and a media through which the user can conveniently inspect the operation of his application programs. AID is modular and can be expanded readily. The subroutines in AID can fill many positions in a Real-Time Supervisory System. AID can clear user specified portions of memory, enter and obtain data and commands from the keyboard, dump memory in specified formats, search memory, establish breakpoints, trace conditionally or unconditionally, output in octal or loader format, list tapes in loader formats, initiate jumps to any location in memory, update source tapes, and calculate the execution time of application programs. Conventions and documentation is provided to enable the user to

add application-oriented checkout facilities to AID.

Maintain

Is a modular set of computer I/O and peripheral equipment verify and correct subroutines. These routines thoroughly test the arithmetic unit, all machine instructions, memory through worst-case patterns, I/O operations and peripheral equipment. MAINTAIN is designed such to exploit the full value of the maintenance and control panel facilities in the isolation and repair of faults. MAINTAIN operates in two modes, VERIFY and CORRECT. VERIFY is automatic and in minimum time establishes the operational readiness of the system. CORRECT assists the user in the diagnosis and isolation of suspect hardware. The test facilities and controls in combination with CORRECT reduce mean-time-to-repair to a few minutes. The MAINTAIN executive program can be resident and VERIFY cycled periodically. The modularity and open-endedness of MAINTAIN permits verify and correct programs for special system hardware to be written and easily incorporated.

Subroutine Library

The Subroutine Library includes: mathematical routines for logarithmic, exponential, trigonometric functions; arithmetic routines for single and double precision calculations; conversion routines for BCD to BINARY, BINARY to BCD, and BINARY to and from Special I/O codes; and service routines for communicating with peripheral equipment. Conventions and instructions are provided so the user can add application programs to the library and be called by DAS, FORTRAN and AID. New programs added to the library are available to users.

Documentation

The documentation is comprehensive and clear, containing the information required for the user to fully understand, program, operate and maintain the system. Interface and installation manuals are provided to the User prior to installation for system integration preparation. The program and service manuals are provided in advance of the user training attendance. The software manuals contain a special section covering software modularity and expansion techniques.

Programming Training

Programming training courses are provided on a scheduled basis at DMI facilities. User attendance is on a NO CHARGE BASIS. The one-week course covers instruction for programming in machine language, an introduction to the DATA 620 software, and machine operation. The course includes time at the console. Supplies required for the course are provided at no charge to the attendees. On-site courses are available on a contract basis.

Maintenance Training

A two week at the factory maintenance course is provided on a scheduled and no charge basis. The instruction covers: machine organization, operation, logic, design, timing, preventive maintenance, trouble-shooting, and repair. Extended training covering special systems hardware is available on an individual customer basis. The course is designed for personnel with existing digital logic design knowledge.

User Organization

DMI customer services (CS) provide continuing co-ordination, program exchange, library maintenance for DATA 620 users. Users are notified of new additions to the library, application data, program and hardware modifications and new equipment. CS maintains up-to-date master

prints on each system controlled. An inventory of programming forms, paper tapes and spare parts is maintained for expedited or emergency service. Statistical data on field operating experience based on user submitted reports is maintained and available to users. On-call and On-site maintenance services are available on a contract basis.

Application Programming

DMI's technical staff includes senior application programming specialists well qualified to assist the user in the preparation of application programs or to take full responsibility on a contract basis for the preparation of a total solution, including hardware and application programs. Their services are available on a daily rate or fixed price basis.



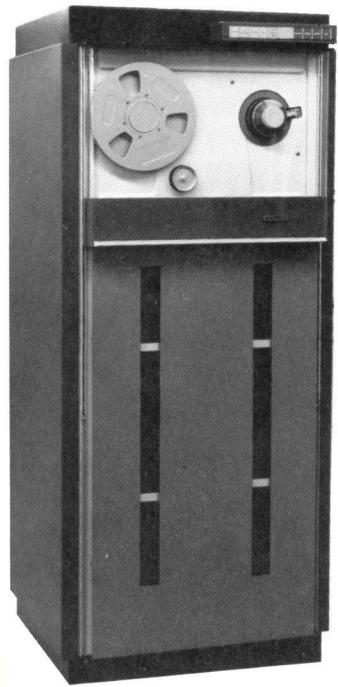
DATA 620

Accessories & Options

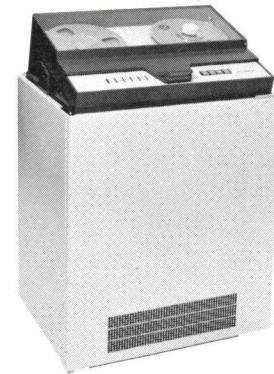


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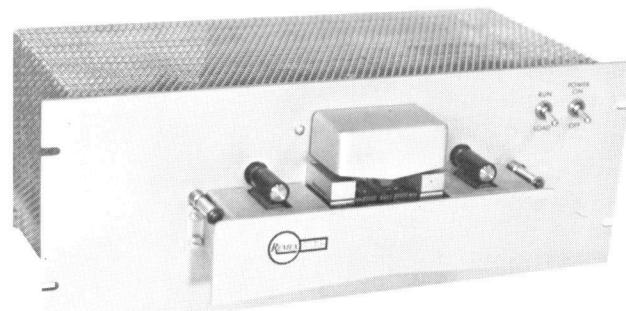
Model No.	Item
620-00	DATA 620 system computer, 16-bit word, 4096 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-01	DATA 620 system computer, 16-bit word, 8192 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-02	DATA 620 system computer, 16-bit word, 512 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-03	DATA 620 system computer, 16-bit word, 1024 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-04	DATA 620 system computer, 16-bit word, 2048 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
622-00	DATA 622 system computer, 18-bit word, 4096 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
622-01	DATA 622 system computer, 18-bit
	word, 8192 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-60	First TTY Unit added to computer, ASR 33 with adapter. Reads at 25 cps, punches and types at 10 cps. Operates on-line or off-line.
620-61	First TTY Unit added to computer, ASR 35 with adapter. Reads, punches and types at 10 cps. Operates on-line or off-line.
620-05	Additional 4096 word memory module, 16-bit.
620-06	Additional 8192 word memory module, 16-bit.
622-05	Additional 4096 word memory module, 18-bit.
622-06	Additional 8192 word memory module, 18-bit.
620-10	High speed multiply and divide.
620-11	Byte processing instruction set.
620-13	Real-time clock.
620-14	Direct Memory Access and Overlap for first memory module.
620-14-1	Overlap Control for each additional memory module



120 ips Magnetic Tape Unit



45 ips Magnetic Tape Unit



300 cps Paper Tape Reader

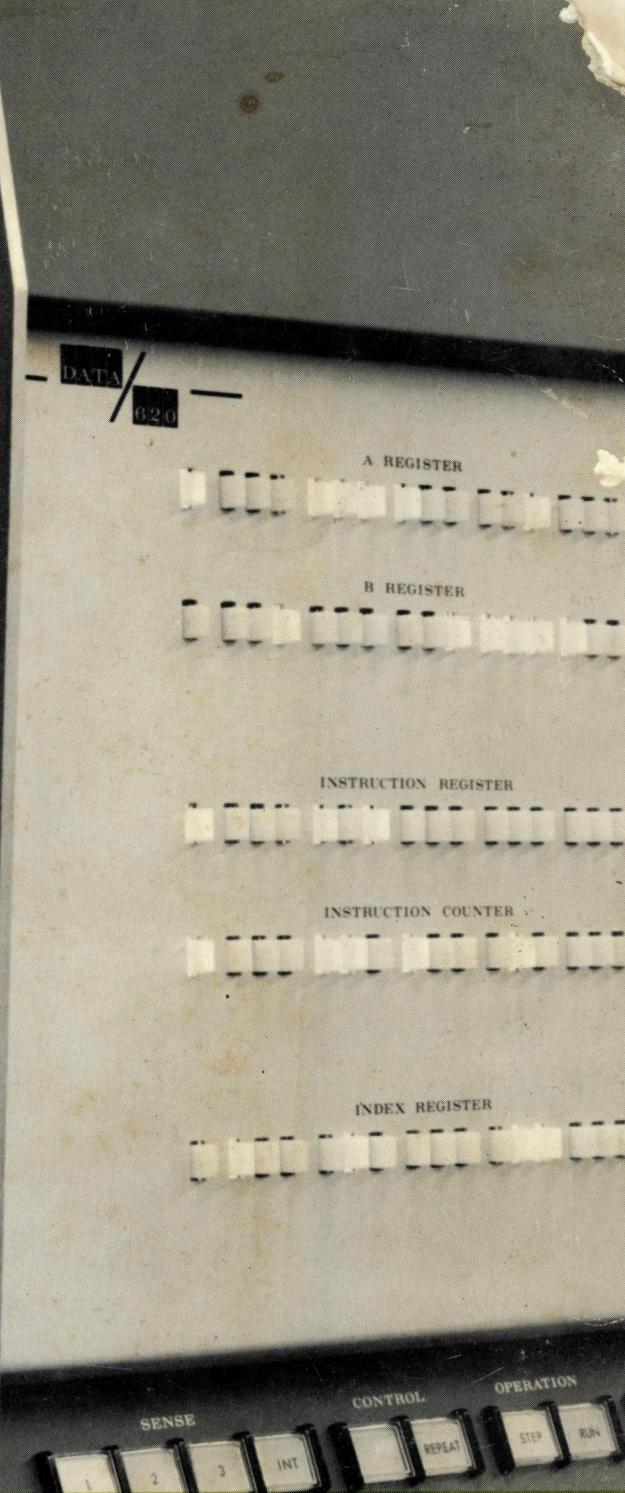
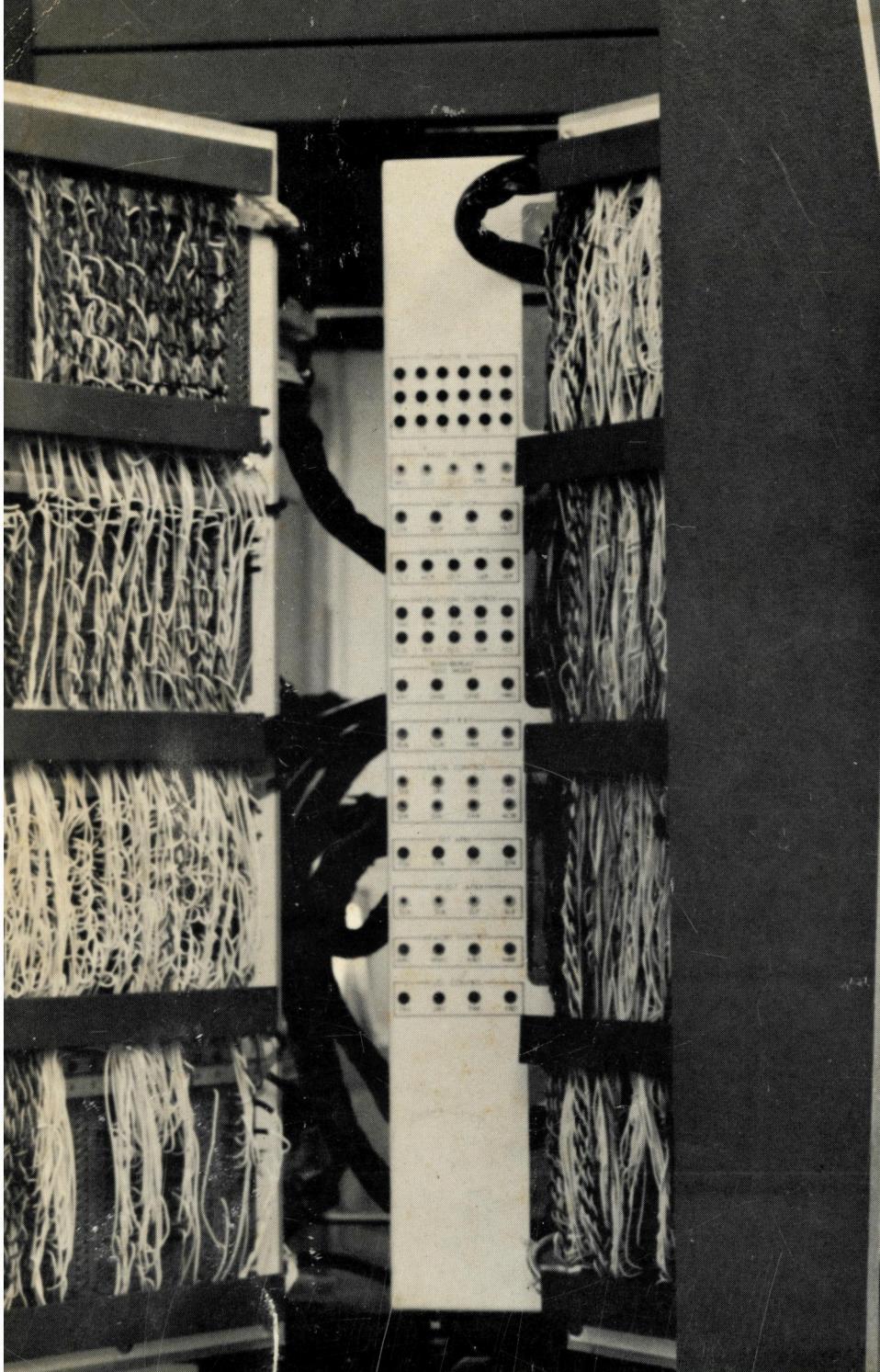


600 lpm Line Printer

620-15	Buffer Interlace control, and one device adapter.	620-41	Disc Memory Master Control Unit and One Disc file up to 225,000 16 bit words of storage. 66 kc word transfer rate.
620-15-1	Additional Buffer Interlace control - device adapter.	620-41-1	Additional Disc File for 620-41 provide up to 225,000 words of storage.
620-19	Micro-control adapter.	620-50	Card reader and adapter 100 CPM.
620-20	Buffered output channel, 16/18-bit parallel.	620-52	Card punch and adapter, 100 CPM.
620-21	Buffered input channel, 16/18-bit parallel.	620-55	High speed digital printer and adapter, 1200 LPM, 12 column, 15 characters per column.
620-22	Gated input channel, 16/18-bit parallel.	620-56	High Speed Line Printer, 120 columns, 600 LPM, Buffered.
620-23	Gated output channel, 16/18-bit parallel.	620-57	Medium Speed Line Printer, 120 columns, 300 LPM word buffer.
620-25	Eight external sense lines.	620-58	Paper Tape reader and adapter. Reads at 300 ips. Reads 5, 7 or 8 level tape.
620-26	Eight external control lines.	620-59	Paper tape punch and adapter. Punches at 60 cps. Punches 5, 7 or 8 level tape.
620-27	Eight priority interrupt lines with arm/disarm facility.	620-59-1	Paper tape system with common controller includes Models 620-58, 620-59.
620-30	Magnetic tape control unit and one transport. Includes assembly and disassembly register, IBM compatible, operates at 45 ips. Dual density, 556 and 800 bpi.	620-60-1	Second and each additional ASR 33 TTY unit with adapter. Reads at 25 cps, types and punches at 10 cps.
620-31	Magnetic tape control unit and master transport to control up to 3 slaves. Includes assembly/disassembly register, operates at 45 ips. Dual Density 556 and 800 bpi. IBM compatible.	620-61-1	Second and each additional ASR 35 TTY unit with adapter. Reads, types and punches at 10 cps.
620-31-1	Each slave transport for model 620-31.	620-62	Half Duplex Interface to Bell model 201 Modem. Transmits up to 2 KC.
620-32	Magnetic tape control unit and one transport. Includes assembly and disassembly register, IBM compatible, operates at 75 ips. Dual density 556 and 800 bpi.	620-70	Model 503 Oscilloscope adapter. 256 by 256 addressable points, without Oscilloscope.
620-33	Magnetic tape control unit and master tape transport to control up to 3 slaves. Includes assembly/disassembly register, operates at 75 ips. IBM compatible, dual density 556 and 800 bpi.	620-75	Digital plotter. Plots at 300 increments per second.
620-33-1	Each slave transport for model 620-33.	620-90	Additional enclosure and cooling unit.
620-34	Magnetic tape control unit and one transport. Includes assembly and disassembly register, IBM compatible, operates at 120 ips. Dual density 556 and 800 bpi.	620-91	75 taper pin connector drawer (Model SA75) for VersaLOGIC - 7".
620-35	Magnetic tape control unit and master tape transport to control up to 3 slaves. Includes assembly/disassembly register, operates at 120 ips. IBM compatible, dual density 556 and 800 bpi.	620-93	Auxiliary power supply 10A (Model PS611).
620-35-1	Slave transport for model 620-35.		(See catalog for description and price of complete line of compatible VersaLOGIC for Interface modules.)



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