

Technical Reference

Vaisala Sounding Processing Subsystem
SPS341AG

VAISALA

PUBLISHED BY

Vaisala Oyj
Vanha Nurmijärventie 21, FI-01670 Vantaa, Finland
P.O. Box 26, FI-00421 Helsinki, Finland
+358 9 8949 1

Visit our Internet pages at www.vaisala.com.

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1. About this Document

1.1 Version Information

This manual provides technical reference information for SPS341AG and its plug-in units. SPS341AG is used as part of Vaisala sounding systems.

Instructions for connecting SPS341AG to the sounding system are included in *Vaisala DigiCORA Sounding System MW41 Getting Started Guide* and *AUTOSONDE AS15 Installing and Configuring Software Technical Reference*. Instructions for updating SPS341AG software are included in *Vaisala DigiCORA Sounding System MW41 Technical Reference*.

Table 1 Document Versions

Document Code	Date	Description
M212199EN-A	January 2019	First version.

1.2 Related Manuals

Table 2 Related Manuals

Manual Code	Manual Name
M211429EN	<i>Vaisala DigiCORA Sounding System MW41 Getting Started Guide</i>
M211415EN	<i>Vaisala DigiCORA Sounding System MW41 Technical Reference</i>
M211730EN	<i>AUTOSONDE AS15 User Guide</i>
M211731EN	<i>AUTOSONDE AS15 Installing and Configuring Software Technical Reference</i>

1.3 Documentation Conventions



WARNING! **Warning** alerts you to a serious hazard. If you do not read and follow instructions carefully at this point, there is a risk of injury or even death.



CAUTION! **Caution** warns you of a potential hazard. If you do not read and follow instructions carefully at this point, the product could be damaged or important data could be lost.



Note highlights important information on using the product.



Tip gives information for using the product more efficiently.



Lists tools needed to perform the task.



Indicates that you need to take some notes during the task.

1.4 Trademarks

DigiCORA® is a registered trademark of Vaisala Oyj.

Microsoft® is either a registered trademark or trademark of Microsoft Corporation in the United States and other countries.

All other product or company names that may be mentioned in this publication are trade names, trademarks, or registered trademarks of their respective owners.

1.5 Safety

The product delivered to you has been tested for safety and approved as shipped from the factory. Note the following precautions:



WARNING! If the equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.



WARNING! Do not replace the detachable main supply cord with an inadequately rated cord.



WARNING! The equipment must be connected to an earthed mains socket outlet.

FI: VAROITUS: Laite on liitettävä suojakoskettimilla varustettuun pistorasiaan.

DA: ADVARSEL: Apparatet må tilkoples jordet stikkontakt.

SE: WARNING: Apparaten skall anslutas till jordat uttag.



CAUTION! Do not modify the unit. Improper modification can damage the product or lead to malfunction.

1.6 ESD Protection

Electrostatic Discharge (ESD) can cause immediate or latent damage to electronic circuits. Vaisala products are adequately protected against ESD for their intended use. It is possible to damage the product, however, by delivering electrostatic discharges when touching, removing, or inserting any objects inside the equipment housing.

To make sure you are not delivering high static voltages yourself:

- Handle ESD sensitive components on a properly grounded and protected ESD workbench.
- When an ESD workbench is not available, ground yourself to the equipment chassis with a wrist strap and a resistive connection cord.
- If you are unable to take either of the above precautions, touch a conductive part of the equipment chassis with your other hand before touching ESD sensitive components.
- Always hold component boards by the edges and avoid touching the component contacts.

2. Product Overview

2.1 Introduction to SPS341AG

Vaisala Sounding Processing Subsystem SPS341AG is a subsystem for Vaisala sounding systems. It consists of a front panel, a chassis, plug-in units and a connector panel.



Figure 1 Vaisala Sounding Processing Subsystem SPS341AG

2.2 Front Panel

The power control switch and the system indicator LEDs are located on the front panel. The power control dip switches are located on the backside of the front panel.

2.2.1 Power Control Switch

The power of the subsystem can be switched on and off from the power control switch located on lower left corner of the front panel.

2.2.2 Indicator LEDs

The standby and power/status indicator LEDs are located on lower left corner of the front panel beside the power control switch.

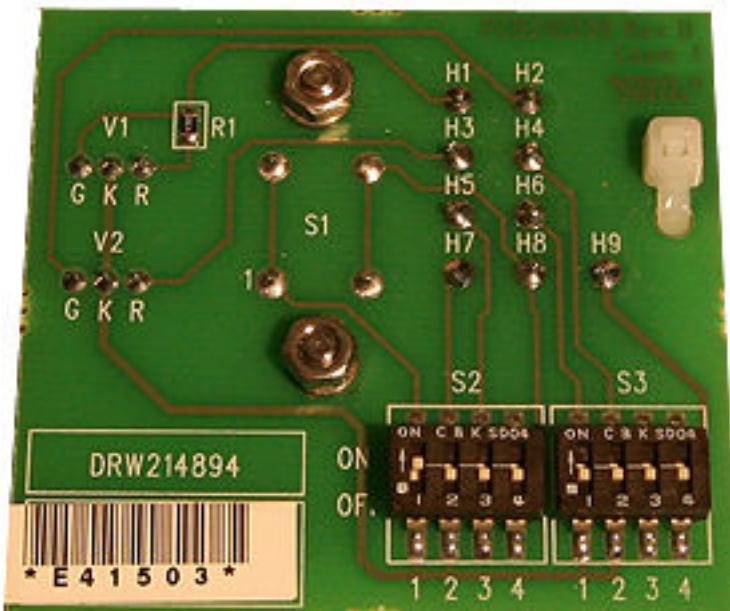
The status of the subsystem is indicated by the two LEDs as explained in [Table 3 \(page 12\)](#):

Table 3 Indicator LED Colors

Standby LED Color	Power/Status LED Color	System Status
Blank	Blank	Power is not applied
Yellow	Blank	Power is applied
Blank	Blinking green	Powering up
Blank	Green	Ready for operation
Blank	Red	Unit failure during power-up or operation, failure in network connection

2.2.3 Power Control Dip Switches

The functionality of the power switch can be configured using the eight DIP switches located behind the front panel, see [Figure 2 \(page 12\)](#).

**Figure 2 Power Control DIP Switches****Table 4 Power DIP Switches Default Setting**

Switch No.	Default Setting	Description
S2-1	ON	Signal PTOGGLE1#. When the front power switch is pushed, the PTOGGLE1# signal is set to Low. The unit is then switched ON by the power control logic. If the setting is OFF, the front power switch is disabled. This option is useful for AUTOSONDE and remote use.

Switch No.	Default Setting	Description
S2-2	OFF	Signal PON#. Remote PON# functions normally. Remote control capability is available with the Power CTRL connector. If the setting is ON, the unit is always on. This option is useful for AUTOSONDE use. The unit is switched on automatically after a blackout.
S2-3	OFF	Signal POFF#. Remote POFF# functions normally. Remote control capability is available with the Power CTRL connector. If the setting is ON, and S2-1 and S2-2 are ON, the unit is always on. Pushing the front power switch resets the unit.
S2-4	OFF	Not used.
S3-1	OFF	Signal RACK0#. S3-1 and S3-2 can be used to identify the units, if multiple units are used. See Table 5 (page 13) .
S3-2	OFF	Signal RACK1#. S3-1 and S3-2 can be used to identify the units, if multiple units are used. See Table 5 (page 13) .
S3-3	OFF	Not used.
S3-4	OFF	Not used.

Rack address is a binary number formed from signals RACK1# and RACK0#, where RACK1# is MSB (most significant bit) and RACK0# is LSB (least significant bit).

Table 5 Rack Identification

DIP Settings	Rack Address
S3-1 OFF, S3-2 OFF	00
S3-1 ON, S3-2 OFF	01
S3-1 OFF, S3-2 ON	10
S3-1 ON, S3-2 ON	11

2.3 Frame and Plug-in Units



WARNING! Make sure the SPS341AG power cable is grounded.

2.3.1 Unit Slots

The chassis contains a card frame with nine slots for the plug-in units, motherboard, and an I/O extension board. The slots are numbered from left to right (front view) with numbers 1 to 9. The figure below shows you the plug-in units inside the chassis.

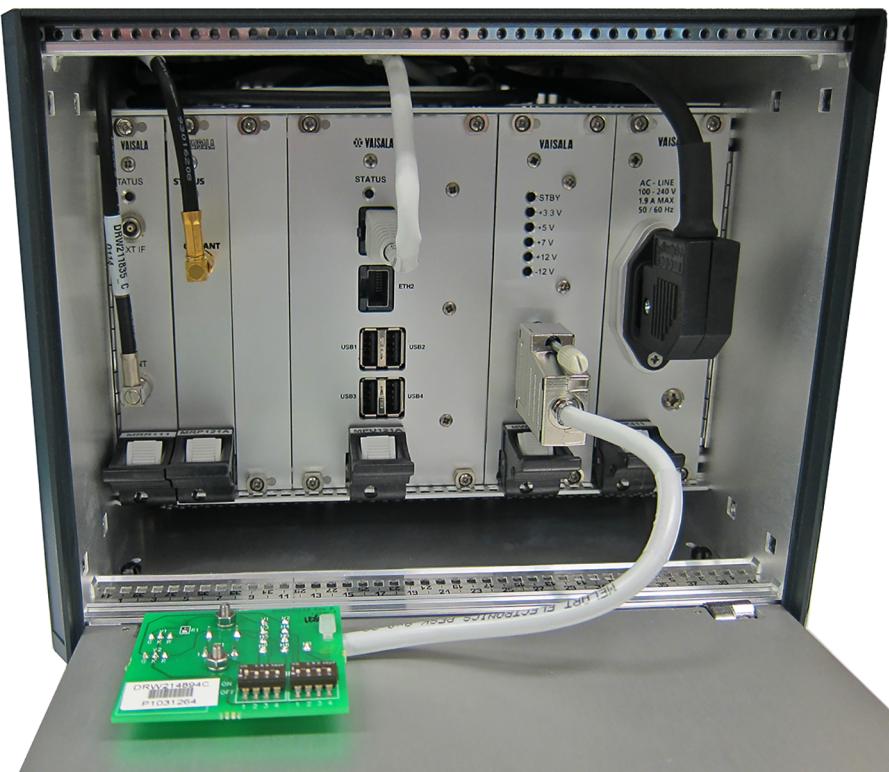


Figure 3 Plug-in Units inside the Chassis

2.3.2 Motherboard

The operating voltages as well as signal connections between different units are carried through the motherboard. The motherboard is fully passive. It does not contain any active electronic or electromechanical components.

2.3.3 I/O Extension Board

The I/O extension board is a printed circuit board which connects the I/O signals between the motherboard and the I/O connectors.

Signals to the connector panel are fed through an extension board connector on the back side of the motherboard.

2.3.4 Connector Panel

The connector panel at the back has connectors for antenna signals, LAN, I/O signals, and power.

The panel includes I/O connectors, a printed circuit board which connects the I/O signals between the connector board, and an I/O extension board.

Antenna signals and LAN are connected to the plug-in units via cables and the power inputs are wired from the connector to the motherboard. See [Table 6 \(page 15\)](#) for details.

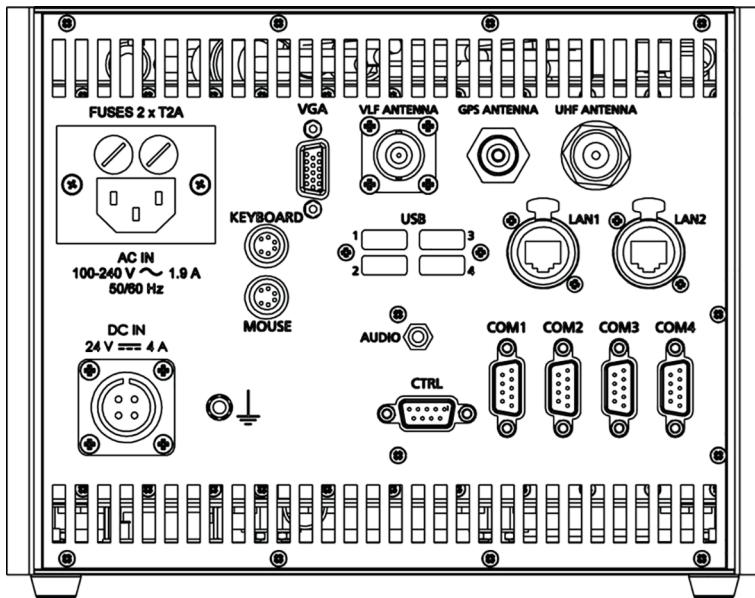


Figure 4 Power, Signal, and I/O Connectors in the Connector Panel

Table 6 Connector Panel Connectors

Connector	Description	Note
AC IN	Mains power connector	
DC IN	DC power connector	
UHF ANTENNA	UHF antenna connector	
GPS ANTENNA	GPS antenna connector	
VLF ANTENNA	VLF antenna connector	Not used
LAN1	LAN connector	
LAN2	LAN connector	For future use
CTRL	Control	
COM1	COM1	For future use
COM2	COM2	For future use
COM3	COM3	For future use
COM4	COM4	For future use
VGA	VGA display	For future use
KEYBOARD	Keyboard	Not used
MOUSE	Pointing device	Not used
USB1...4	Universal Serial Bus	For future use
AUDIO	Speakers	For future use

2.3.4.1 AC In

Connector type:

IEC power inlet with fuse holder (Shurter 0040.5001.2)

2.3.4.2 DC In

Connector type:

Glenair MIL-C-5015, 4-socket, shell size 14, IT3102A14S-2SF7

Table 7 DC In Connections

Pin	Signal	Note
A	+VDC input (+24 V)	
B	- VDC input	
C		
D		

2.3.4.3 UHF Antenna

Connector type:

Coaxial N female



+12 VDC power is supplied to the antenna.

2.3.4.4 GPS Antenna

Connector type:

Coaxial TNC female



+5 VDC power is supplied to the antenna.

2.3.4.5 LAN1

Connector type:

RJ-45 Connector (Neutrik NE8FAV)

Table 8 LAN Connections

Pin	Signal	Note
1	Transmit data +	

Pin	Signal	Note
2	Transmit data -	
3	Receive data +	
4		
5		
6	Receive data -	
7		
8		

2.3.4.6 CTRL

Connector type:

9 pin D female

Table 9 CTRL Connections

Pin	Signal	Note
1	+12V	Power out
2	StartIn	For future use
3	StartOut	For future use
4	POFF#	Power control
5	GND	Ground
6	RES#	System reset
7	PON#	Power Control
8	TEST#	For future use
9	PTOGGLE#	Power control

3. Maintenance

3.1 Sounding Processing Subsystem Maintenance

SPS341AG does not need any regular maintenance.

At higher operating temperatures, regular checking of the operation of the cooling fan is recommended.

In all maintenance work, remember to proceed in accordance with electrical safety regulations.



WARNING! Switch the subsystem POWER OFF before replacing any plug-in units. Unplug the mains connector before replacing the AC power supply MWP411. Switch External 24 VDC supply OFF before replacing the DC power supply MWP312.



CAUTION! To avoid damaging the front panel hinges, always open the front panel so that it is supported on a flat surface.

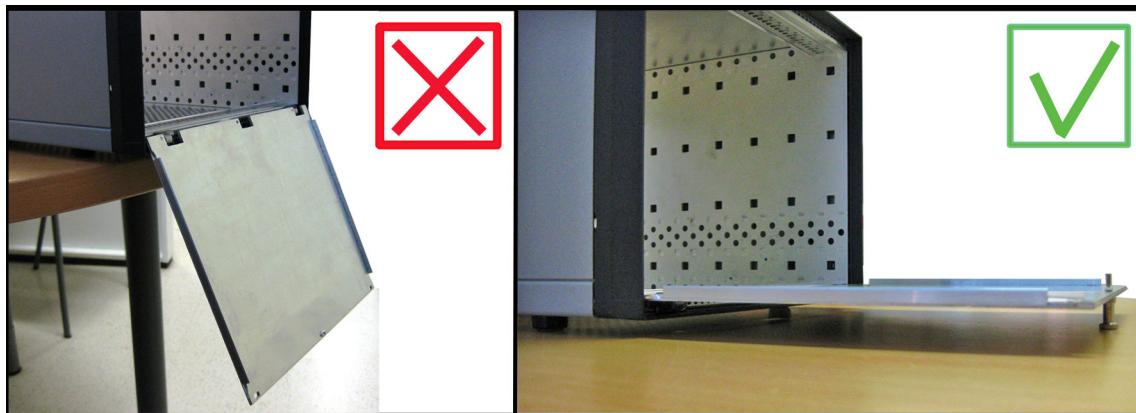


Figure 5 Opening the Front Panel

3.2 Replacing Fuses

Check the fuses in case power is connected to the subsystem, but the standby LED light on the front panel remains blank. There are three user-replaceable fuses in the system: two in connection with the AC power inlet and one in DC Power Supply MWP312.

The two fuses in connection with the AC power inlet are located in fuse holders in the connector panel. The fuse is a glass tube 5 × 20 mm, slow blow T2A/250VAC.

The MWP312 fuse is located in a hole in the middle of the cooling plate of the unit. The fuse is a glass tube 5 × 20 mm, slow blow T5A/250VAC.



You need a flat-head screwdriver to perform this maintenance procedure.

3.2.1 Replacing AC Power Inlet Fuses

- ▶ 1. Open the two adjacent fuse holders using a flat-head screwdriver or a coin.



Figure 6 Opening the AC Power Inlet Fuse Holder

- 2. Remove the fuse from the holder with your fingers.

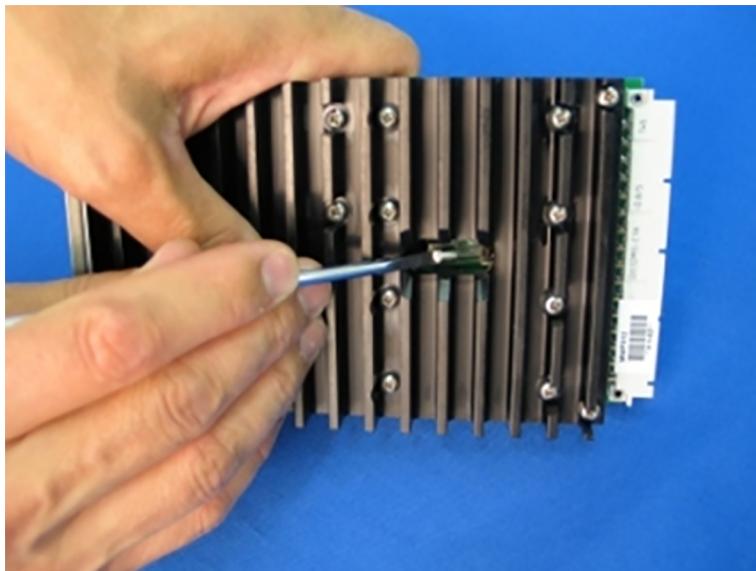


Figure 7 Removing the AC Power Inlet Fuses

- 3. Replace the fuses if needed.
- 4. Close the fuse holder with the screwdriver.

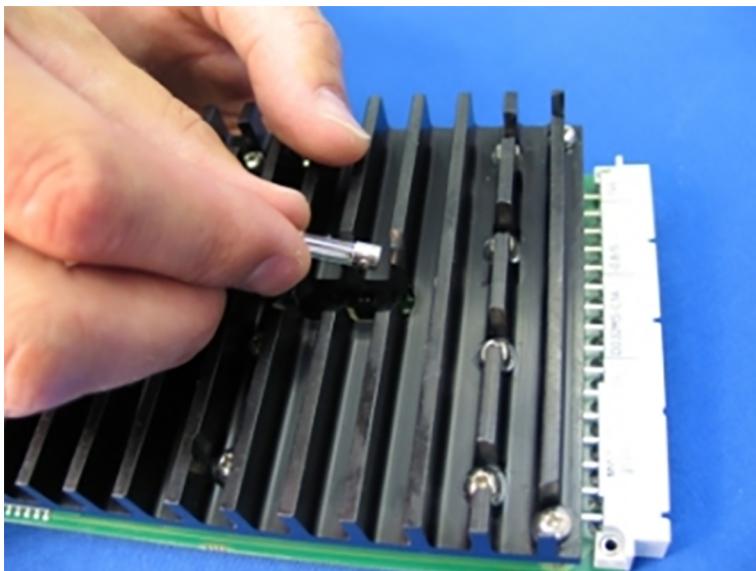
3.2.2 Replacing DC Power Unit Fuses

- ▶ 1. Remove the MWP312 unit as instructed in section [Replacing Plug-in Units \(page 22\)](#).
The fuse is located in a small hole in the middle of the cooling plate of the unit.
- 2. Lift the other end of the fuse carefully with the tip of the screwdriver and remove it with your fingers.



- 3. Replace the fuse if needed.

4. Install the fuse by dropping it carefully to the fuse holder and pressing it to its place.



5. Install the MWP312 unit as instructed in section [Replacing Plug-in Units \(page 22\)](#).

3.3 Replacing Plug-in Units

In the event of a fault, it is possible to replace the plug-in units in the field.



WARNING! Switch SPS341AG POWER OFF before replacing any plug-in units.
Unplug the mains connector before replacing the AC power supply MWP411.
Switch External 24 VDC supply OFF before replacing the DC power supply MWP312.

To remove a unit:

- Disconnect the unit cable in the front panel.
- Open the upper and lower attachment screws.
- Push first the handle lock button to release the latch and then push the whole handle down to unplug the unit.
- Pull out the unit.

To install a unit:

- Place the unit into lower and upper card slide rails in the correct card slot.
- Unlock the handle latch and push the unit almost completely into the slot.
- Finally, lift the handle up to complete the push until the card is fully in the slot and the handle latch is locked.
- Fasten the attachment screws.
- Connect the cable.



CAUTION! Do not damage the EMC strips in the front panel of the unit or in the adjacent front/blank panel when pulling out or pushing in a plug-in unit. Move the unit slowly in the card guides and avoid bending them.

3.4 Checking the Operation of Cooling Fans

There are three fans on the lower part of the chassis.

- ▶ 1. For a rough check:
 - a. Switch the subsystem power off and back on.
 - b. Check if you can hear the noise of the fans when power is on.
- 2. For a thorough check:
 - a. Remove all plug-in units except MWP312.
 - b. Connect the subsystem to 24 VDC power system using the 24 VDC input in the connector panel.
 - c. Check the air flow in the empty slots to see if the fans work.

4. Plug-in Unit Descriptions

4.1 400 MHz Receiver MRR111

400 MHz Receiver MRR111 is a Euro 1-sized (160 mm × 100 mm) unit. Together with Receiver Processor MRP111 and an external low-noise amplifier it builds up a digital radio receiver. The main emphasis on the design of this radio receiver has been on improving spurious free dynamic range and sensitivity over its predecessors.



Figure 8 Receiver MRR111

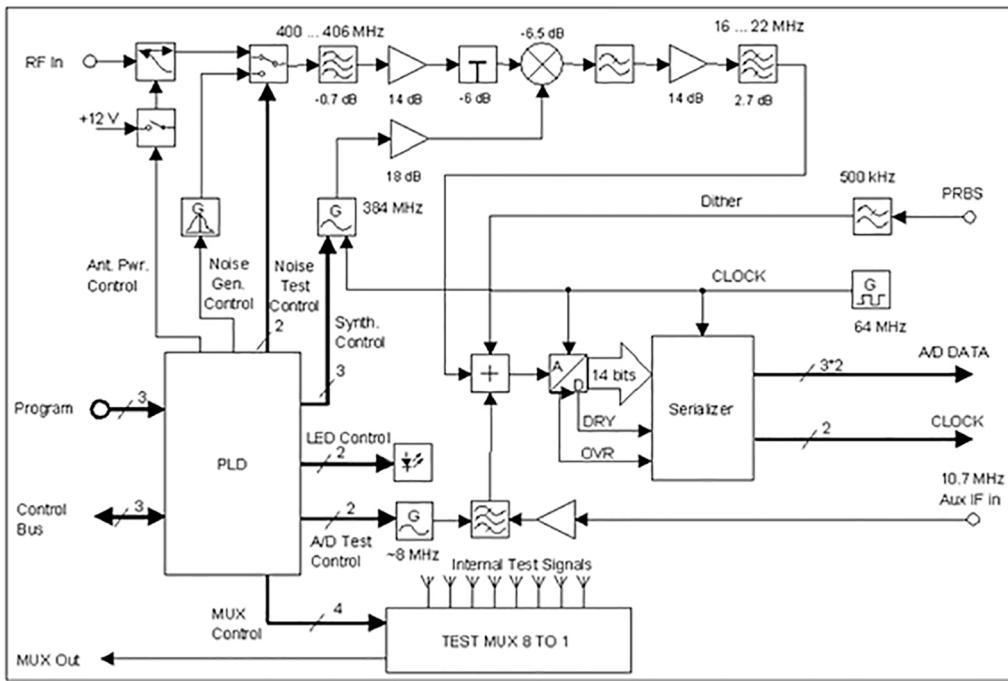


Figure 9 MRR111 Block Diagram

MRR111 performs a down conversion for the signal entering the RF input connector and translates the whole meteorological frequency band 400 ... 406 MHz to an intermediate frequency band 16 ... 22 MHz. The down conversion is carried out by a high-level diode mixer driven by a synthesized 384-MHz local oscillator. The IF signal is then sampled by a high-performance 14-bit analog to digital converter using a sampling rate of 64 Msamples / s. This “block down conversion” enables simultaneous multi-channel (multi-sonde) reception using multiple digital down converters and a common RF front end.

An external 10.7 MHz IF signal can also be fed to the A / D converter using connector “Ext IF In” on the front panel. It is possible to use this input simultaneously with normal 400 MHz reception.

The output signals from the A / D converter are transformed into serial format and fed via three 448 Mbit/s symmetric lines to MRP111 for further processing. The last down conversion, filtering, and signal demodulation are performed digitally in MRP111.

A crystal oscillator module with high spectral purity (low jitter) provides the 64-MHz sampling clock and also the reference signal for the 384-MHz local oscillator synthesizer.

For testing purposes, an onboard noise generator and test oscillator with associated electronic switches are provided.

All functions of the unit are controlled by Radio Processor MRP111 via a three-line serial control bus.

4.1.1 RF Section

The RF signal enters MRR111 through connector X8 (ANT) at the front panel. The signal is routed through a solid state RF switch A11 (UPG2009TB) to the RF filter. The purpose of the switch is to select either input signal or noise from the onboard noise source to the receiver (see section [Noise Test Circuitry \(page 33\)](#)). The antenna input signal is coupled to the RF section when logic 0 is applied to NTEST+ and logic 1 to NTEST-.

RF filter Z7 is a ceramic coaxial filter with three resonators and has a -3 dB pass band of 15 MHz centered at 403 MHz.

The filter is followed by an RF amplifier stage which consists of a monolithic wideband amplifier A7 (SGA-6289). It provides 14 dB of gain and a high dynamic range due to its low noise figure and high third order intercept point.

A simple LC-filter consisting of C74, C60, L14 and C55 at the output of the amplifier forms a band rejecting (notch) filter at 364 MHz. It increases the image rejection of the receiver and also prevents the image frequency noise of the amplifier to reach the down converter.

A resistive 6 dB attenuator formed by R48, R53, and R56 provides a good wideband impedance matching between the RF amplifier and mixer. It also increases the third order intercept point of the receiver without increasing the noise figure of the receiver too much.

The output signal of the RF amplifier is available for measurements at a test point with MMCX connector X6 (RF). When loaded with a 50-ohm impedance it provides 20.8 dB of attenuation.

A typical frequency response of the RF section measured from test point X6 is shown in the figure below.

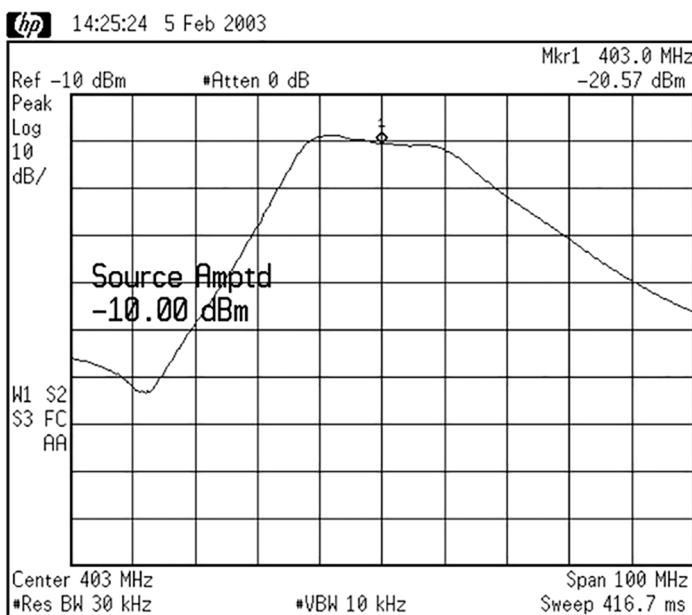


Figure 10 RF Response

4.1.2 Down Conversion

The RF signal at 400 ... 406 MHz is converted to an intermediate frequency (IF) at 16 ... 22 MHz. The down conversion is done using a fixed local oscillator frequency of 384 MHz. A double-balanced diode ring mixer A6 (SYM-18H) operates as a down converter. Due to its high local oscillator drive level (17 dBm), it has a high third order intercept point resulting in a good dynamic range with low intermodulation products.

The output signal from the mixer is fed to the IF amplifier through an LC low pass filter formed by L11, C37 and L10. Its -3 dB cut off frequency is 37 MHz and it prevents the unwanted high-frequency components from the mixer to reach the IF amplifier.

The LCR network consisting of C48, L9 and R42 compensates for the inductive input impedance of the low pass filter at high frequencies and provides a good wide-band impedance match for the IF port of the mixer.

The output signal of the down converter is available for measurements at a test point with MMCX connector X4 (IF AMP). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

4.1.3 IF Section

The IF signal from the down converter is fed to a monolithic wideband amplifier A2 (SGA-6289). It provides 14 dB of gain and a high dynamic range due to its low noise figure and high third order intercept point.

The amplifier is followed by an LC band pass filter with three sections. The pass band of the filter is flat within ± 0.5 dB between 15 ... 22 MHz. The -3dB points are at 13 and 24 MHz. The three resonant circuits of the filter are tunable by trimmer capacitors C26, C40, and C61. The coupling between resonators is capacitive and fixed. The termination impedances of the filter are different, input 50 ohms and output 100 ohms, which produces about 2 dB of voltage gain including filter losses.

The output signal of the IF section is available for measurements at a test point with MMCX connector X7 (IF). When loaded with a 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

Typical frequency responses of the combined RF and IF sections measured from RF input to test point X7 is shown in the two figures below.

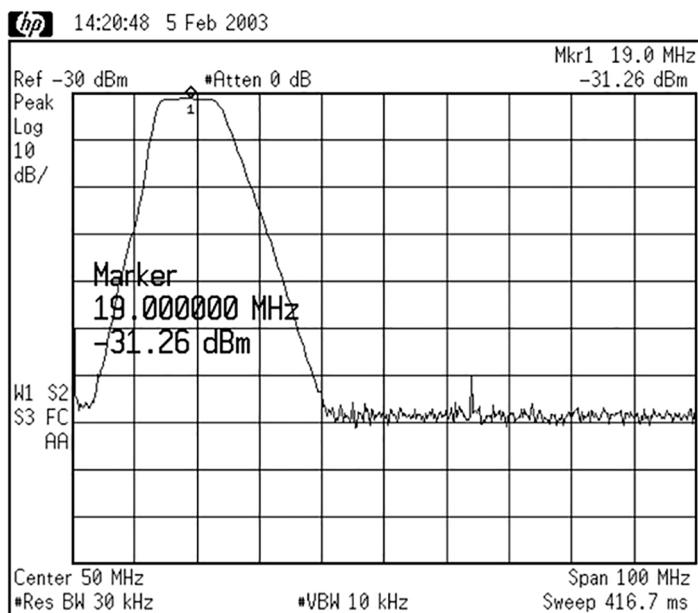


Figure 11 IF Response, Wide Span

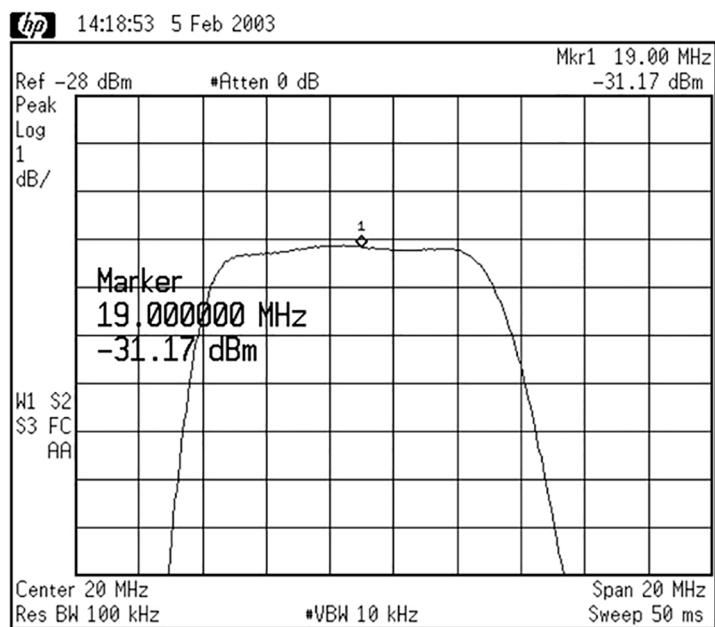


Figure 12 IF Response, Narrow Span

4.1.4 Analog to Digital Conversion

The analog to digital conversion is carried out by a high-performance 14-bit ADC A5 (AD6645). It has symmetrical (differential) inputs for both analog input and sampling clock signals to minimize cross talk. The analog input range is ± 1.1 V. The digital output is parallel, consisting of 14 bits (D0 ... D13), data ready (DRY) and over range (OVR). The output data is in two's complement format.

The signal coming from the IF section is first balanced by transformer T2 (ADTT4-1), which also steps up the voltage by two. The IF signal entering to the ADC can be measured from test connector X7 (IF). When loaded with a 50-ohm impedance it provides 23.9 dB of voltage attenuation compared to the actual voltage at the signal input of A5. Thus full scale voltage (2.2 Vp-p) equals to -13.1 dBm at X7.

The sampling frequency is 64 MHz and it originates from crystal oscillator Z2 (QEN60-AHR 64 MHz DT50). The sampling signal is at first balanced by transformer T1 (ADTT4-1) which also steps up the voltage by two. Then the sampling signal is clipped by two antiparallel coupled diodes V3 (BAV99) to limit the amplitude and retain the slew rate high at zero crossings.

The spurious signals generated by the small non-linearities and internal glitches of the ADC are attenuated by using a dither signal. It is a noise-like signal added to the analog input signal and located at a lower frequency than the signals of interest. It has a suitable (quite low) amplitude to linearize the ADC. The dither signal is a digital pseudo random signal generated in Receiver Processor MRP111 and fed to MRR111 via pin A4 of the card edge connector X1. The dither input signal is filtered with a two-section LC low pass filter (L1, C3, C4, L6 and C80) which has a cut off frequency of about 500 kHz to remove all spectral components from the IF signal range. The dither signal is attenuated to a suitable level by a series resistor (R59), which sums the dither signal to the output signal from the IF filter.

The 16 outputs of the ADC are fed to a parallel-to-serial converting device D1 (65LVDS95) through series resistors located at the close vicinity of the ADC to reduce noise generating capacitive load currents. The P-to-S converter has 21 inputs for parallel data and one for clock signal. The remaining five inputs are connected to either ground or +3.3 V supply for diagnostic purposes. It has three symmetrical (balanced) data outputs and one symmetrical clock output. The clock signal input frequency is multiplied by 7 using an internal phase locked loop frequency synthesizer. With the 64-MHz input clock frequency coming from crystal oscillator Z2, the P-to-S converter generates an internal clock frequency of 448 MHz, which is used as a clock for the three serial outputs. Thus the data rate at the serial outputs is 448 Mbit/s. These output signals and the clock signal are transmitted to Receiver Processor MRP111 via the card edge connector X1. The frequency of the output clock line is still 64 MHz.

To provide a noise-free supply voltage for the sensitive parts of the ADC and crystal oscillator, a special analog +5 V is provided by IC regulator A12 (MIC2920A-5.0BS) from the +7 V supply line.

4.1.5 Local Oscillator

The 384-MHz local oscillator signal for the down converter is generated by a phase-locked loop frequency synthesizer. Its core is an integrated circuit A10 (ADF4112BRU) which contains the phase detector, the prescaler, the programmable counters and the control logic for a dual modulus synthesizer. The loop filter and the voltage-controlled oscillator (VCO) are external.

ADF4112BRU is a very versatile circuit with many externally programmable parameters that are controlled via a three-line serial bus (LE, DATA and CLK). Among other parameters the division ratios of the internal counters are set as follows: R = 4 (reference counter), P = 8/9 (prescaler), B = 3 (N counter) and A = 0 (N counter swallow). With these settings the synthesizer multiplies the reference frequency (16 MHz) by 24 and produces 384 MHz. For diagnostic purposes, the ADF4112BRU contains a multiplexer through which several internal signals can be connected to one output (MUX) for monitoring. Normally the internal digital lock detector is chosen to this output. Details of the operation of ADF4112BRU can be found from its data sheet and MRR111 Control Functions Specification.

Reference frequency for the synthesizer is taken from the 64-MHz crystal oscillator Z2 and divided by four in the internal reference counter of A10 to obtain a reference frequency of 16 MHz for the phase detector. The output signal of the 64 MHz crystal oscillator is available for measurements at a test point with MMCX connector X2 (64 MHz). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

The loop filter is passive for the lowest possible phase noise and is comprised of R77, C91, R82, C118, R87, and input capacitance of A9. It sets for its part the loop band width to almost 300 kHz to efficiently reduce the phase noise at frequencies close to the center frequency.

VCO is a low-phase noise oscillator module A9 (VCO190-370T) which has a tuning range of 340 ... 400 MHz and a typical output level of +1 dBm. The output signal of the VCO is amplified by a monolithic wideband amplifier A8 (SGA-6489). It provides 20 dB of gain and enough power (18 dBm) to drive the local oscillator input of the high level mixer A6.

The output signal of the local oscillator is available for measurements at a test point with MMCX connector X5 (LO). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

To provide a noise-free supply voltage for the sensitive parts of the synthesizer (especially VCO and phase detector), a special analog +5 V is provided by IC regulator A12 (MIC2920A-5.0BS) from the +7 V supply line.

4.1.5.1 External IF

MRR111 is equipped with an input for external IF to facilitate using the receiver with an external front end having 10.7 MHz IF output.

The IF signal entering connector X3 (EXT IF 10.7 MHz) is first scaled down with an attenuator formed by resistors R3, R4, and R5. With original resistance values the attenuation is 18.5 dB and the maximum input level is 0 dBm. Attenuation can easily be modified according to the signal level to be applied.

The attenuated input signal is fed to a monolithic wideband amplifier A4 (MAR-6SM) through selection switch A3 (uPG2009TB). The amplifier provides 20 dB of gain. The signal from EXT IF input is connected to the amplifier when a logic 0 is present at ADTEST+ and logic 1 at ADTEST-.

The amplifier is followed by an LC band pass filter formed by C57, L13, and C43. Its passband is 4 ... 11 MHz between -3 dB points. The output signal of the filter is summed with the so-called dither signal coming from a low-pass filter through resistor R59. This sum signal is then combined to the main IF signal through LC tank circuit L15 and C67. Due to this arrangement, no selection switches are needed and, furthermore, it is possible to use the external IF input simultaneously with normal receiver operation.

The output signal of the IF section is available for measurements at a test point with MMCX connector X7 (IF). When loaded with 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

A typical frequency response measured from the EXT IF input to test point X7 is shown in the figure below.

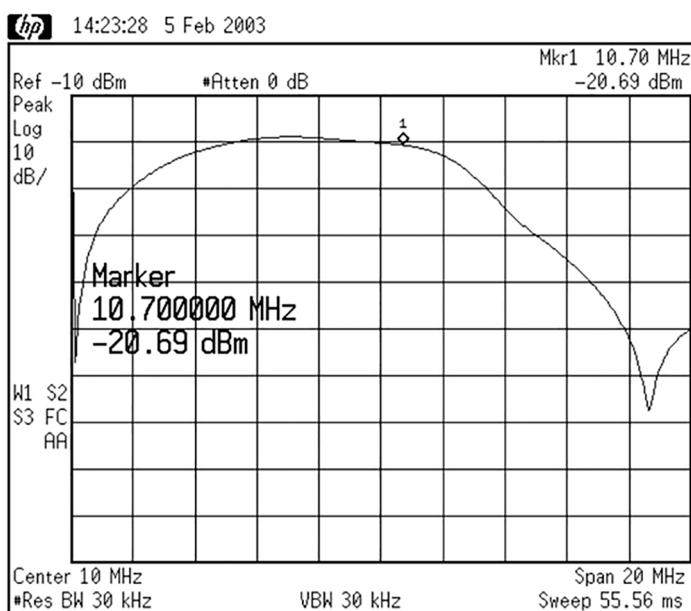


Figure 13 Ext If Response

4.1.6 ADC Test Circuitry

A test signal for verifying the operation of the analog to digital converter can be generated with an onboard oscillator. The EXT IF amplifier and filter are also utilized for this purpose by applying positive feedback to the input of amplifier A4 to get the circuit to oscillate.

Feedback is taken from the output of the filter via a loaded series resonant circuit (C35, R24, and L7) and connected to the amplifier input through selection switch A3. The test signal is set on by applying a logic 1 to ADTEST+ and logic 0 to ADTEST-.

This test oscillator generates a low distortion signal at about 6.5 MHz with an amplitude that is between half scale and full scale voltage of the ADC. Using this signal it is possible to check that all outputs of the ADC are active and also verify its linearity when a Fourier analysis is performed to the signal and levels of its harmonics are measured.

The output signal of the test oscillator is available for measurements at a test point with MMCX connector X7 (IF). When loaded with a 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

4.1.7 Noise Test Circuitry

An onboard noise source is provided for verifying that the receiver is functioning normally.

Noise diode V6 (ST-2) produces wideband noise when reverse biased over its breakdown voltage and current limited to a suitable value. The bias current is switched on and off by transistor V2 (SST3904). The noise generator is switched on when NGEN- is at logic 0.

RF switch A11 (uPG2009TB) selects signal either from the antenna input connector or from the noise generator to the receiver RF section. When a logic 1 is applied to NTEST+ and a logic 0 to NTEST- the noise source is coupled to the receiver input.

4.1.8 Power Feed to Antenna

Power and control signal to an external low noise amplifier (LNA) and antenna selection switch is applied through the antenna input connector.

To prevent extra noise from entering the receiver input, the power is fed to the antenna cable through an LC low-pass filter (C77, L17, and C88) followed by a tank circuit (L21 and C95) resonating at 403 MHz.

The power feed is controlled by an intelligent power switch IC A1 (L6377D) that also contains all necessary safety features such as an adjustable current limit with power saving pulsed operation and over temperature protection. A diagnostic output is available, indicating the operating status of the circuit. Power to the antenna line is switched on and off with control signal ANTPWR applied to IN+ of A1. Power is on when ANTPWR is at logic 1.

Control for the external antenna selection switch is generated by sequences of fast on and off pulses of feed voltage.

4.1.9 Test Multiplexer

An analog 8-to-1 multiplexer D2 (4051B) is provided for automatic testing of various voltages of MRR111. The address bits set by the serial control bus define which of the following test signals is routed to the MRRMUX output: +3.3 V supply, A+5 V supply, +7 V supply, +12 V supply, antenna feed voltage, SCLOCK, SWDATA and SYNMUX. The signals are scaled and shifted by resistor networks to comply with the 0 ... 5 V range of the multiplexer output. Details of the scaling and addresses can be found from MRR111 Control Functions Specification.

4.1.10 Control

All functions of MRR111 are controlled by Radio Processor MRP111 via a three line serial control bus (SCLOCK, SWDATA and SRDATA). The commands entering the unit via the bus are interpreted by a programmable logic device (PLD) D4 (EPM7064S). It has numerous outputs that control the operation of the receiver. Details of the controlling functions can be found from MRR111 Control Functions Specification.

Programming of PLD is done by using JTAG interface (TDI, TDO, TCLK, and TMS) via the card edge connector X1.

4.1.11 Introduction to Test Points

Typical signals and voltages at the test connectors and some essential points under normal operating conditions are described to help possible fault diagnosis.

The aluminum cover of the unit has to be removed to get access to the measurement points.

Measurement setup if not stated otherwise is:

- MRRR111 initialized for normal receiver operation and antenna power set off.
- A signal generator set at 403 MHz, no modulation, and level -20dBm is connected to ANT connector.
- Warm up time before measurements is at least ten minutes.
- A spectrum analyzer is connected to the test connectors using a test cable with a male MMCX connector.
- The DC voltages are measured with a digital voltmeter.

4.1.11.1 X6 RF

Typical spectrum measured from test connector X6 is shown in the figure below.

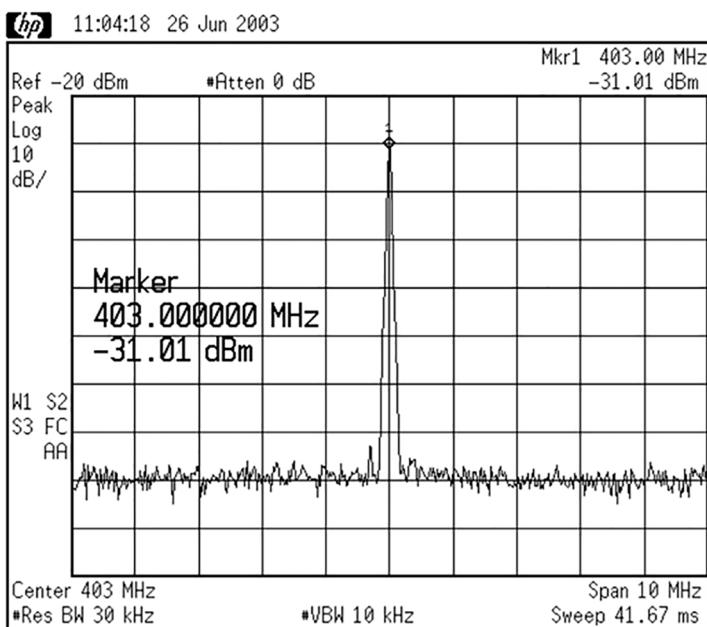


Figure 14 Spectrum from X6

4.1.11.2 X4 IF AMP

Typical spectrum measured from test connector X4 is shown in the figure below.

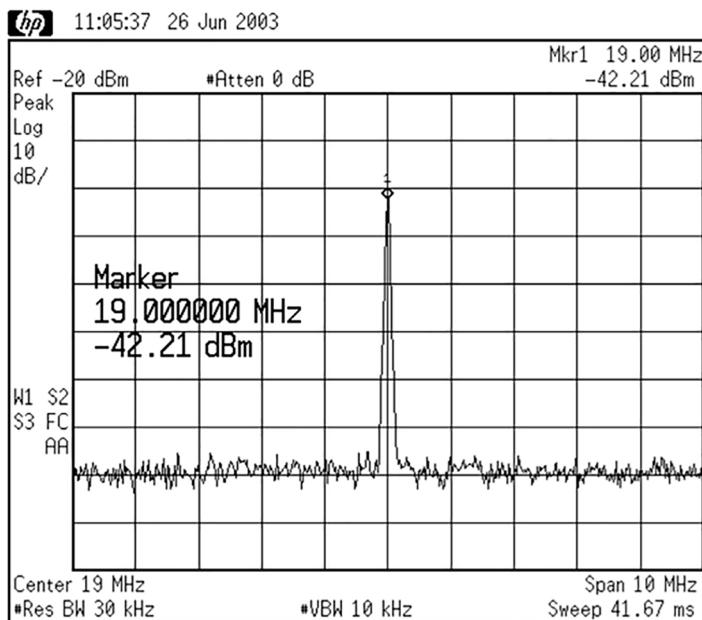


Figure 15 Spectrum from X4

4.1.11.3 X7 IF

Typical spectrum measured from test connector X7 is shown in the figure below.

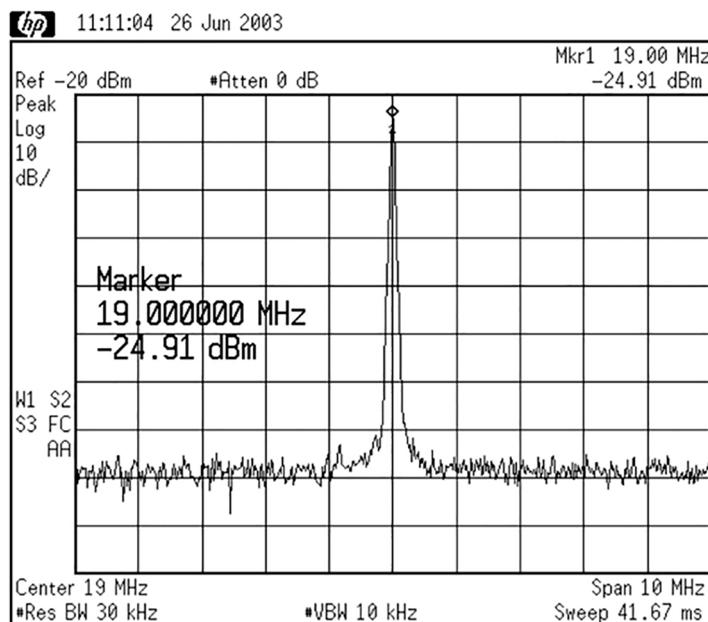


Figure 16 Spectrum from X7

4.1.11.4 X5 LO

Typical spectrum measured from test connector X5 is shown in the figure below.

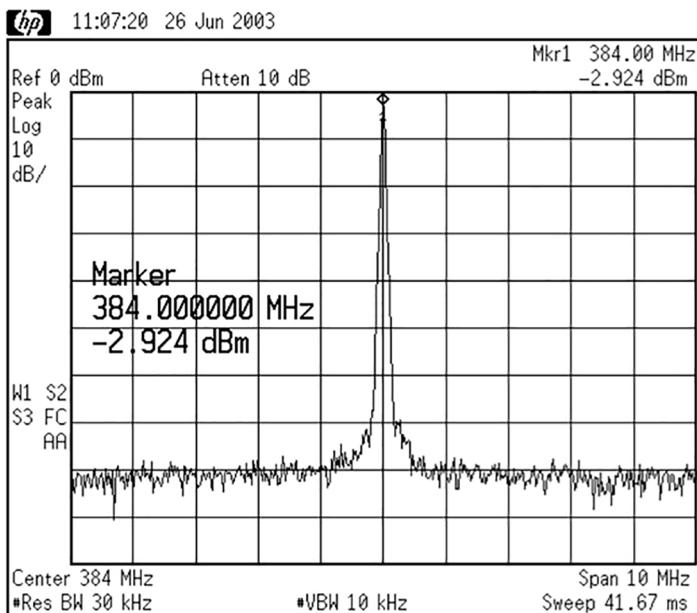


Figure 17 Spectrum from X5

4.1.11.5 X2 64 MHz

Typical spectrum measured from test connector X2 is shown in the figure below.

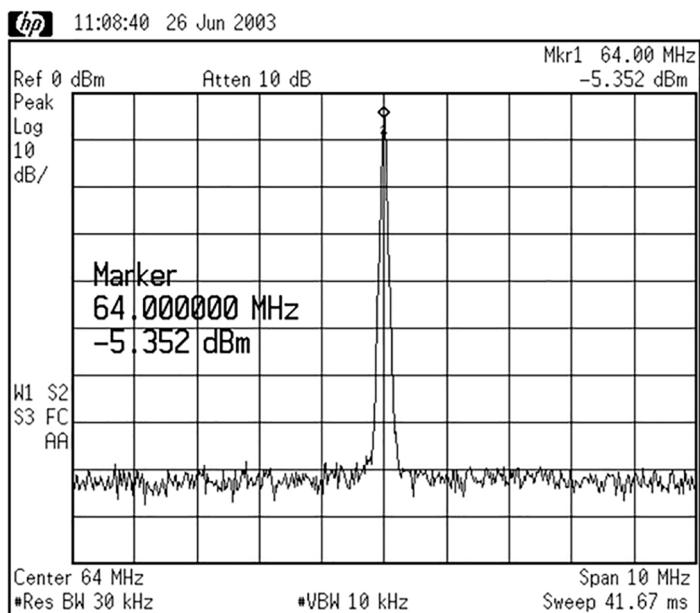


Figure 18 Spectrum from X2

4.1.11.6 EXT IF

Measurement setup is as described in 3.1 but the signal generator is connected to the EXT IF input (X3), frequency set at 10.7 MHz, modulation off and level -10 dBm.

Typical spectrum measured from test connector X7 is shown in the figure below.

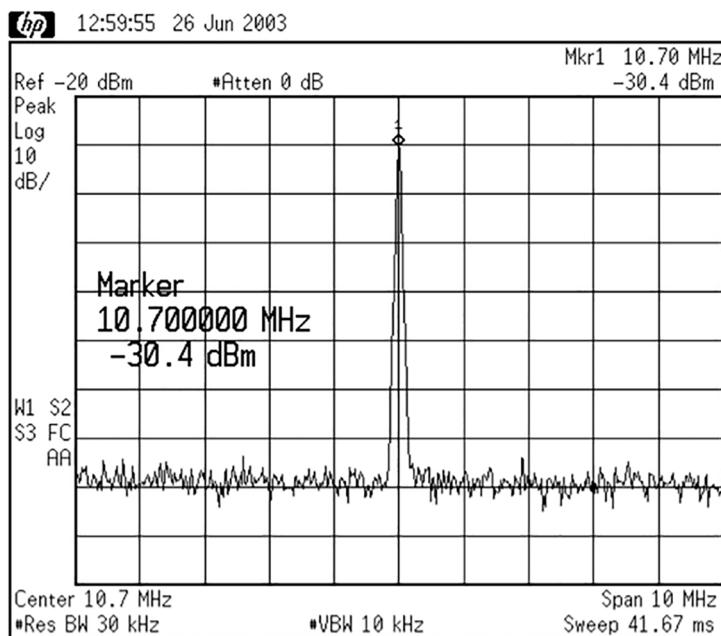


Figure 19 Spectrum from X7 (Input to EXT IF)

4.1.12 Typical Voltages

Typical DC voltages between some essential points and the ground are shown in the following table.

Table 10 Typical DC Voltages

Measurement Point	Description	Voltage [V]
A7 input pin 2	Amplifier input bias voltage	1.8
A7 output pin 1	Amplifier output bias voltage	3.9
A2 input pin 2	Amplifier input bias voltage	1.8
A2 output pin 1	Amplifier output bias voltage	3.9
A8 input pin 2	Amplifier input bias voltage	1.6
A8 output pin 1	Amplifier output bias voltage	4.5
A4 input pin	Amplifier input bias voltage	1.6
A4 output pin	Amplifier output bias voltage	3.4
T1 pin5 / C28	ADC clock input bias voltage	2.5
T2 pin5 / C78	ADC analog input bias voltage	2.5
C91 / R77	Phase detector voltage	3.2

4.1.13 Specifications

Table 11 MRR111 Technical Specifications

Property	Value/Description
Frequency Range	400 ... 406 MHz
Noise Figure	8 dB
Intermediate Frequency	16 ... 22 MHz
Image Rejection	45 dB
Spurious Free Dynamic Range	80 dB
Third Order Intercept Point (IIP3)	+16 dBm
Maximum Input Power Level	-9 dBm full scale +15 dBm absolute maximum
Antenna Power Feed	+12 V 150 mA
External IF input	10.2 ... 11.2 MHz +7 dBm full scale +15 dBm absolute maximum
Operating conditions	Temperature: -30 ... +55°C
Storage conditions	Temperature: -55 ... +80°C
Unit type	E1-size printed circuit board
Dimensions	210(L) x 130(W) x 21(H) mm
Weight	350 g

Table 12 MRR111 Power Requirements

V	mA
+3.3V	110 mA
+5.0 V	80 mA
+7.0 V	420 mA
+12.0 V	260 mA

Table 13 MRR111 Connectors

Connector	Description
System connector	220-pin female hard metric 2 mm
Antenna connector	LEMO EPS.00.250.NTN
External IF in connector	LEMO EPS.00.250.NTN

4.1.14 Signals and Connections

Table 14 Connector Pin Out for X1

Pin	Signal Name	I/O	Description
1A	GND		Ground, 0 V
1B	GND		Ground, 0 V
1C	GND		Ground, 0 V
1D	GND		Ground, 0 V
1E	GND		Ground, 0 V
2B	GND		Ground, 0 V
2C	MRRMUX	O	Output of analog test MUX (0 ... 5 V)
2D	GND		Ground, 0 V
4A	ADDITH	I	Dither signal input to A / D converter (0 / 5 VPRBS)
5C	GND		Ground, 0 V
6A	GND		Ground, 0 V
6B	GND		Ground, 0 V
6C	GND		Ground, 0 V
6D	GND		Ground, 0 V
6E	GND		Ground, 0 V
7A	SR1SD0	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7B	SR1SD0#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7C	GND		Ground, 0 V
7D	SR1SD1	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7E	SR1SD1#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
8A	GND		Ground, 0 V
8B	GND		Ground, 0 V
8C	GND		Ground, 0 V
8D	GND		Ground, 0 V
8E	GND		Ground, 0 V
9A	SR1SD2	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
9B	SR1SD2#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
9C	GND		Ground, 0 V
9D	SR1CLK	O	Data clock from ADC (64 MHz, 1.1 / 1.4 V)
9E	SR1CLK#	O	Data clock from ADC (64 MHz, 1.1 / 1.4 V)

Pin	Signal Name	I/O	Description
10A	GND		Ground, 0 V
10B	GND		Ground, 0 V
10C	GND		Ground, 0 V
10D	GND		Ground, 0 V
10E	GND		Ground, 0 V
21B	SCLOCK	I	Serial control bus clock input (-8 / 8 V)
21C	SWDATA	I	Serial control data input (-8 / 8 V)
22B	SRDATA	O	Serial data output from PLD (active high 10 V)
23A	GND		Ground, 0 V
23B	GND		Ground, 0 V
23C	GND		Ground, 0 V
23D	GND		Ground, 0 V
23E	GND		Ground, 0 V
37B	GND		Ground, 0 V
38A	JTDO	O	JTAG
38B	JTCK	I	JTAG
38D	JTDI	I	JTAG
38E	JTMS	I	JTAG
39E	GND		Ground, 0 V
40C	+7 V	I	Power supply voltage for synthesizer
42A	+3.3 V	I	Power supply voltage for logic circuits
42B	+3.3 V	I	Power supply voltage for logic circuits
42C	+3.3 V	I	Power supply voltage for logic circuits
42D	+3.3 V	I	Power supply voltage for logic circuits
42E	+3.3 V	I	Power supply voltage for logic circuits
44A	+5 V	I	Power supply voltage for logic circuits
44B	+5 V	I	Power supply voltage for logic circuits
44C	+5 V	I	Power supply voltage for logic circuits
44D	+5 V	I	Power supply voltage for logic circuits
44E	+5 V	I	Power supply voltage for logic circuits
46A	+12 V	I	Power supply voltage for analog circuits
46B	+12 V	I	Power supply voltage for analog circuits
46C	GND		Ground, 0 V

Pin	Signal Name	I/O	Description
46D	-12 V	I	Not used
46E	-12 V	I	Not used
47A	GND		Ground, 0 V
47B	GND		Ground, 0 V
47C	GND		Ground, 0 V
47D	GND		Ground, 0 V
47E	GND		Ground, 0 V

- Coaxial connector X8 (ANT): 400 MHz RF input
- Coaxial connector X3 (EXT IF 10.7 MHz): External 10.7 MHz IF input

4.1.15 Parts List MRR111

Table 15 Parts List

Reference	Part Number	Description
Assembly ref. 001	DRW213000	Front panel machining MRR111
Assembly ref. 001	DRW213001	Front panel assembly for MRR111
Included in the part above.	210849	Front panel, shielded, 3U,4HP,Schroff
	210853	Injector/ejector handle, 4HP, IEL, Schroff
	210854	EMC gasket, 3U, Schroff 21101-854
	210855	Sleeve, M2.5 x 3,Schroff 21100-660
	210856	Board holder, Schroff
	210857	Collar screw, M2.5 x 12.3, Schroff
	212048	Screw, crosshead, M2,5 x 8 DIN7985 PZ A4
	212049	Screw, crosshead, M2,5 x 8 DIN966 PZ A4
	5068	Screw-lock compound, Loctite 222
Assembly ref. 002	16166	Plastic label 1180
Assembly ref. 002	210854	EMC gasket 3U, Schroff 21101-854
Assembly ref. 003	210853	Injector/ejector handle 4HP, IEL, Schroff
Assembly ref. 003	15223	Sticker set type, barcode and serial number
Assembly ref. 004	DRW212909	Screening cover for MRR111
Assembly ref. 004	210856	Board holder Schroff
Assembly ref. 005	210855	Sleeve M2.5x3, Schroff 21100-660
Assembly ref. 006	210857	Collar screw M2.5 x 12.3, Schroff

Reference	Part Number	Description
	PCB210106	Printed circuit board MRR111
Integrated Circuits		
A1	211859	IC, power switch ST L6377D
A2, 7	210635	IC, RF amplifier SGA-6289 (SMD)
A3, 11	210634	IC, RF switch NEC uPG2009TB
A4	16889	IC, amplifier MAR-6SM (SMD)
A5	010113	IC, converter A/D AD6645ASQ-80
A6	210630	IC, mixer SYM-18H (SMD)
A8	210636	IC, RF amplifier SGA-6489 (SMD)
A9	210638	IC, VCO VCO190-370T
A10	210633	IC, freq. synth. ADF4112BRU
A12	19991	IC, voltage reg. MIC2920A-5.0BS
D1	010029	IC, LVDS Serdes transmit SN65LVDS95
D2	15525	IC, analog MUX 4051B (SMD)
D3	15964	IC, inverter Ex 74HC14 (SMD Reel)
D4	25771	IC,EPLD EPM7064STC44-10, TQFP44
Transistors and Diodes		
V1	010192	Diode, LED 591-3001, red and green
V2,5	15495	Transistor, NPN SST3904 SOT-23
V3	18135	Diode, silicon BAV99 (SMD)
V4	25184	Transistor, PNP BCP53-10
V6	210627	Diode, noise ST-2 (SOT-23)
Resistors		
R1, 4, 6	18601	Resistor, chip 221R 1% 100 ppm
R2, 7, 10, 11, 34, 35, 40, 41, 69, 75, 79-81	15304	Resistor, chip Ex 100R 1% 50 ppm
R3, 5	18151	Resistor, chip 68R 1% 100 ppm
R8, 12, 15, 24, 82-84	18409	Resistor, chip 100R 1% 100 ppm
R9, 14, 43, 46, 47, 64, 72	18600	Resistor, chip Ex 475R 1% 50 ppm
R13	18794	Resistor, chip 17k8 1% 50 ppm
R16-23, 25, 28-32, 36, 38	25264	Resistor, chip 464R 1.0% 100 ppm
R26, 44	18119	Resistor, chip 1k82 1% 50 ppm

Reference	Part Number	Description
R27, 39, 55, 58, 61, 63, 67, 68, 73	18123	Resistor, chip 10k 1% 50 ppm
R33	15830	Resistor, chip 1k2 5% 200 ppm
R37, 45	16384	Resistor, chip 56R 5% 200 ppm
R42, 76	18720	Resistor, chip Ex 56R2 1% 100 ppm
R48	18731	Resistor, chip 681R 1% 50 ppm
R49	16421	Resistor, chip 51R 5% 200 ppm
R50, 51	19240S	Resistor, chip 22R 5% 200 ppm
R52	18736	Resistor, chip Ex 2k15 1% 50 ppm
R53, 60	18153	Resistor, chip 39R 1% 100 ppm
R54, 57	16416	Resistor, chip 270R 1% 50 ppm
R56	18724	Resistor, chip 147R 1% 100 ppm
R59	18118	Resistor, chip 1k2 1% 50 ppm
R62, 70, 71	18117	Resistor, chip Ex 1k0 1% 50 ppm
R65	18723	Resistor, chip 121R 1% 50 ppm
R66	18716	Resistor, chip Ex 27R4 1% 100 ppm
R74	15889	Resistor, chip 1M0 1% 50 ppm
R77	18725	Resistor, chip 178R 1% 100 ppm
R78	18596	Resistor, chip 4k75 1% 50 ppm
R85, 86	15878	Resistor, chip 10R 5% 200 ppm
R87	18732	Resistor, chip 825R 1% 50 ppm
R89	26101	Resistor, chip 221R 1.0% 100 ppm
R90	25210	Resistor, chip 332R 1.0% 100 ppm
RA1-5	25800	Resistor network RA4C1632-203-F
Capacitors		
C1,10,16,46,58,59,64-66,75,76,79,83,85, 87,88,90,96-99,104,105,107,109,111,113- 115,118,119	18524	Cap., chip ceramic Ex 1n 5% NPO 50V
C2,5,7,12,18,28,31,41,42,71,73,78,82,84	15158	Cap., chip ceramic Ex 100 nF X7R
C3	25900	Cap., chip ceramic Ex 2222 580 16523
C4, 8, 11, 14, 17, 19, 23, 24, 27, 29, 30, 33, 34, 44, 45, 47, 51, 53, 54, 56, 62, 63, 68-70, 72, 77, 80, 89	15160	Cap., chip ceramic Ex 10n 10% X7R 63V
C6, 13, 25, 36, 81, 93, 108, 110, 116	15621	Cap., chip ceramic Ex 100n 10% X7R 50V
C9, 50	15804	Cap., chip ceramic 4p7 p25 NPO 50V

Reference	Part Number	Description
C15	17515	Cap., chip ceramic 2222 861 14279 RC12G
C20	15164	Cap., chip ceramic 22P 5 % NPO
C21, 86, 94, 101-103, 106, 112, 117, 120	26074	Cap., chip tantalum 22uF 16V 20% C LowESR
C22, 49	15803	Cap., chip ceramic Ex 3,3pF NPO
C26	16023	Cap., trimmer TZBX4Z250BA
C32	15166	Cap., chip ceramic
C35, 99, 100, 121	15163	Cap., chip ceramic Ex 100p 5% NPO 63V
C37 ,43	16391	Cap., chip ceramic Ex GRM40C0G181F50PT
C38, 39	26225	Cap., chip ceramic 6p8 p25 N750 50V
C40, 55, 61	18633S	Cap., chip trimmer 3p0-10p N150 TZBX4N100AB
C48	15933	Cap., chip ceramic 39pF NPO 5%
C52, 57	15608	Cap., chip ceramic 120pF N750
C60	15165	Cap., chip ceramic
C67	15488	Cap., chip ceramic 33pF NPO
C74	15376	Cap., chip ceramic 2222 861 15129
C91	15750	Cap., chip ceramic 330nF X7R
C92	19442	Cap., chip tantalum 220uF 10V 20% Case E
C95	15802	Cap., chip ceramic 1,5pF NPO
Connectors		
X1	210249	Connector, 2 mm Metric 5 x 44 socket, press-fit
X1	10948	Marking sticker OK46546, fixed on to the connector
X2, 4-7	210778	Connector, MMCX 90 MMCX-S50-0-51/119 OH
X3, 8	16799	Connector, coaxial EPS.00.250.NTN
Miscellaneous		
Z1, 3-6, 8, 9	25036	Filter, EMI (SMD) NFM61R30T472
Z2	210632	Crystal oscillator 64 MHz, (SMD)
Z7	210637	Filter, ceramic CF12S3-403
L1, 6, 7	17555S	Choke 18uH 10% SMD
L2, 16, 17, 19, 20, 22-24	18637S	Choke, chip 470n 5% coilcraft
L3	17506	Inductor, chip 1.0uH 10%
L4, 18	25312S	Choke 330uH 20% coilcraft
L5	25089S	Choke, chip 1 4700n 10% coilcraft
L8, 12, 13, 15	16398	Inductor, chip 2.2uH 10% 1210 250mA

Reference	Part Number	Description
L9-11	17559S	Choke 220n 5% SMD
L14, 21	17367S	Choke, RF 47 nH 10% SMD
T1, 2	210631	Transformer, RF, (SMD) ADTT4-1
	211738	Screw, crosshead M2,5 x 6 DIN7985 PZ A4
	211741	Therm. conductive liquid gap filler 1000, 50cc
	212048	Screw, crosshead M2,5x8 DIN7985 PZ A4
	212049	Screw, crosshead M2,5x8 DIN966 PZ A4
	5068	Screw-lock compound, Loctite

4.1.16 Diagrams and Board Layouts MRR111

Table 16 MRR111 Diagrams and Board Layouts

Code	Description
DRW230935	Circuit Diagram, 2 pages
DRW228506	Components Layout

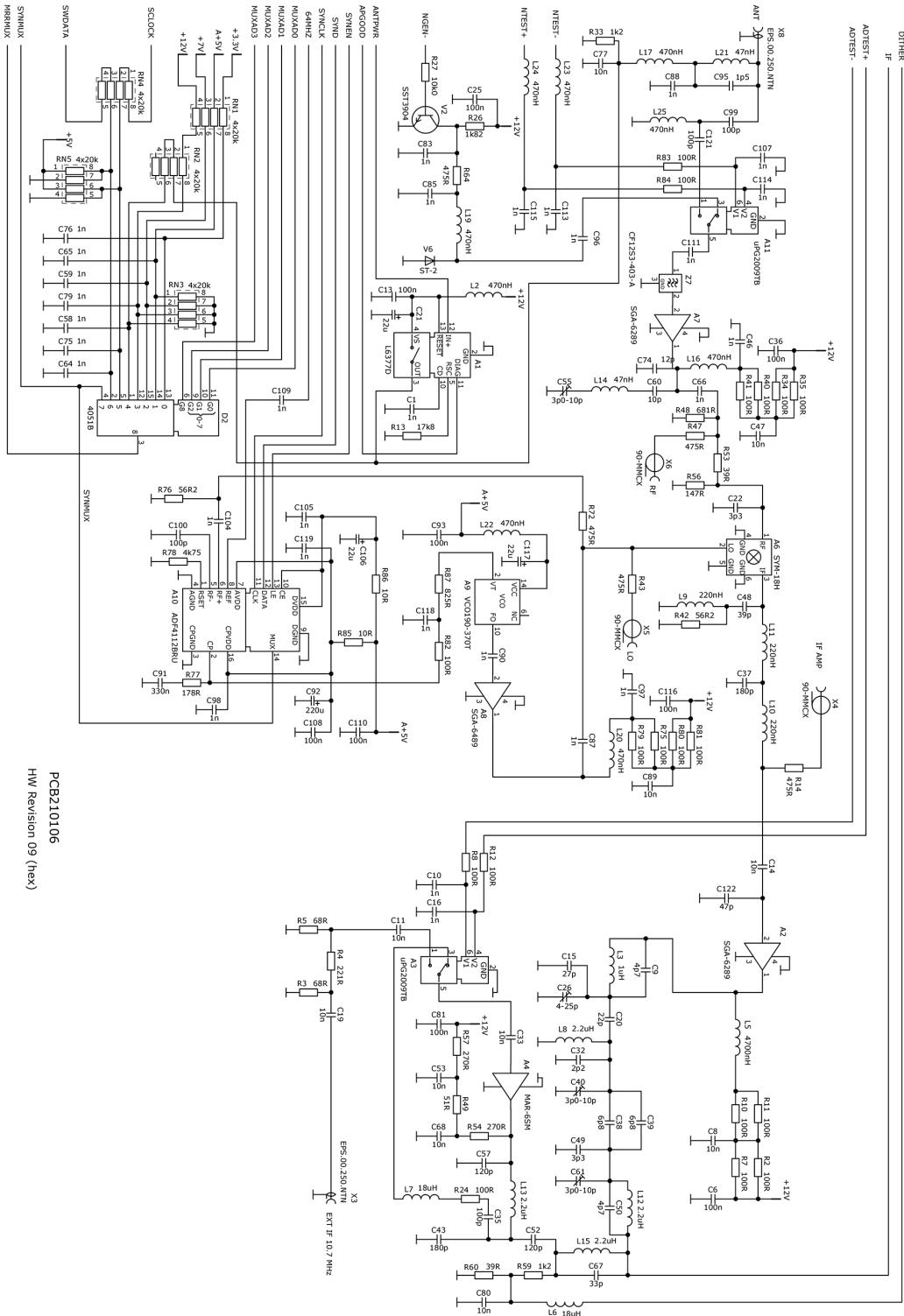


Figure 20 MRR11 and MWR321 Circuit Diagram, 1/2

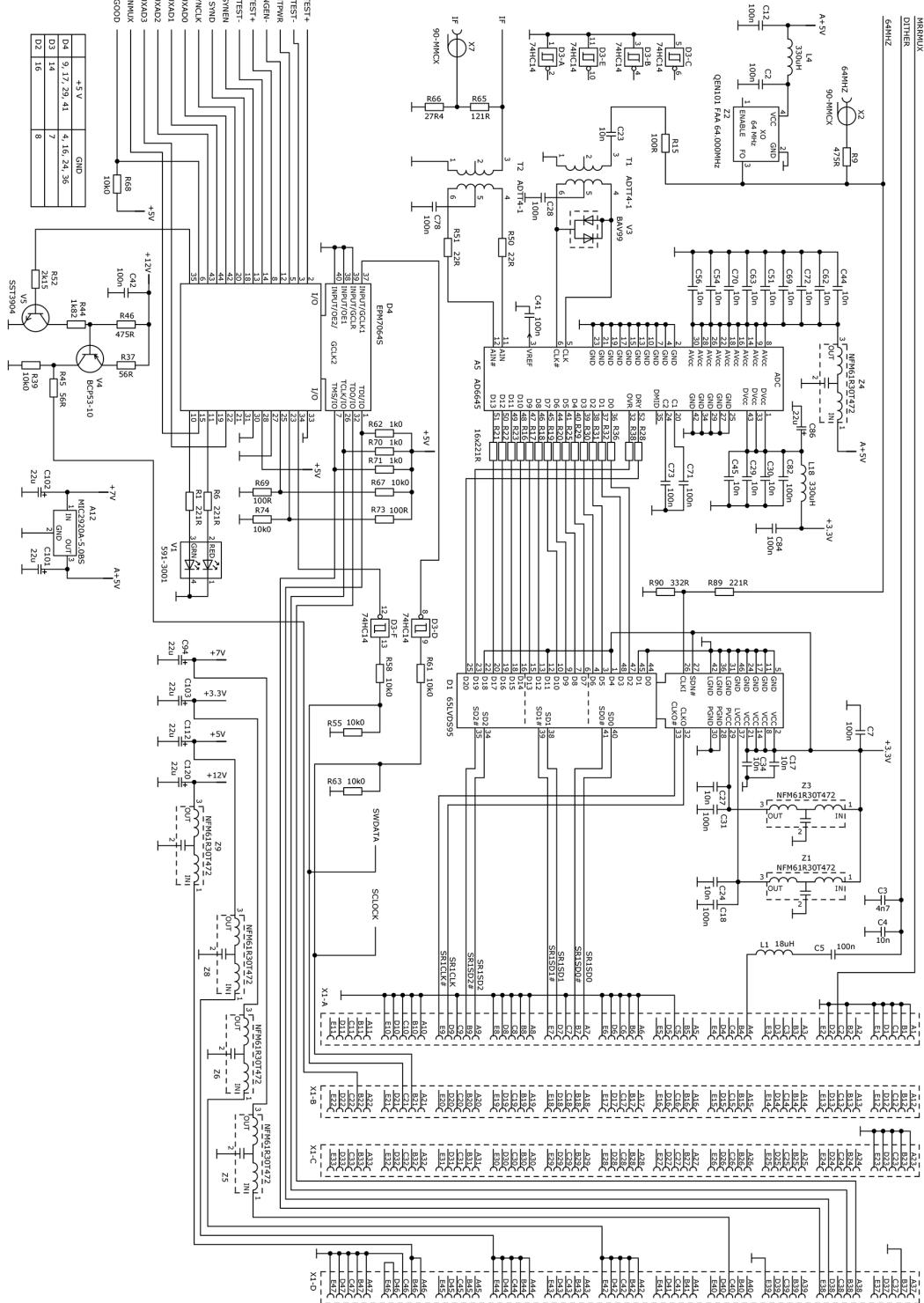


Figure 21 MRR111 and MWR321 Circuit Diagram, 2/2

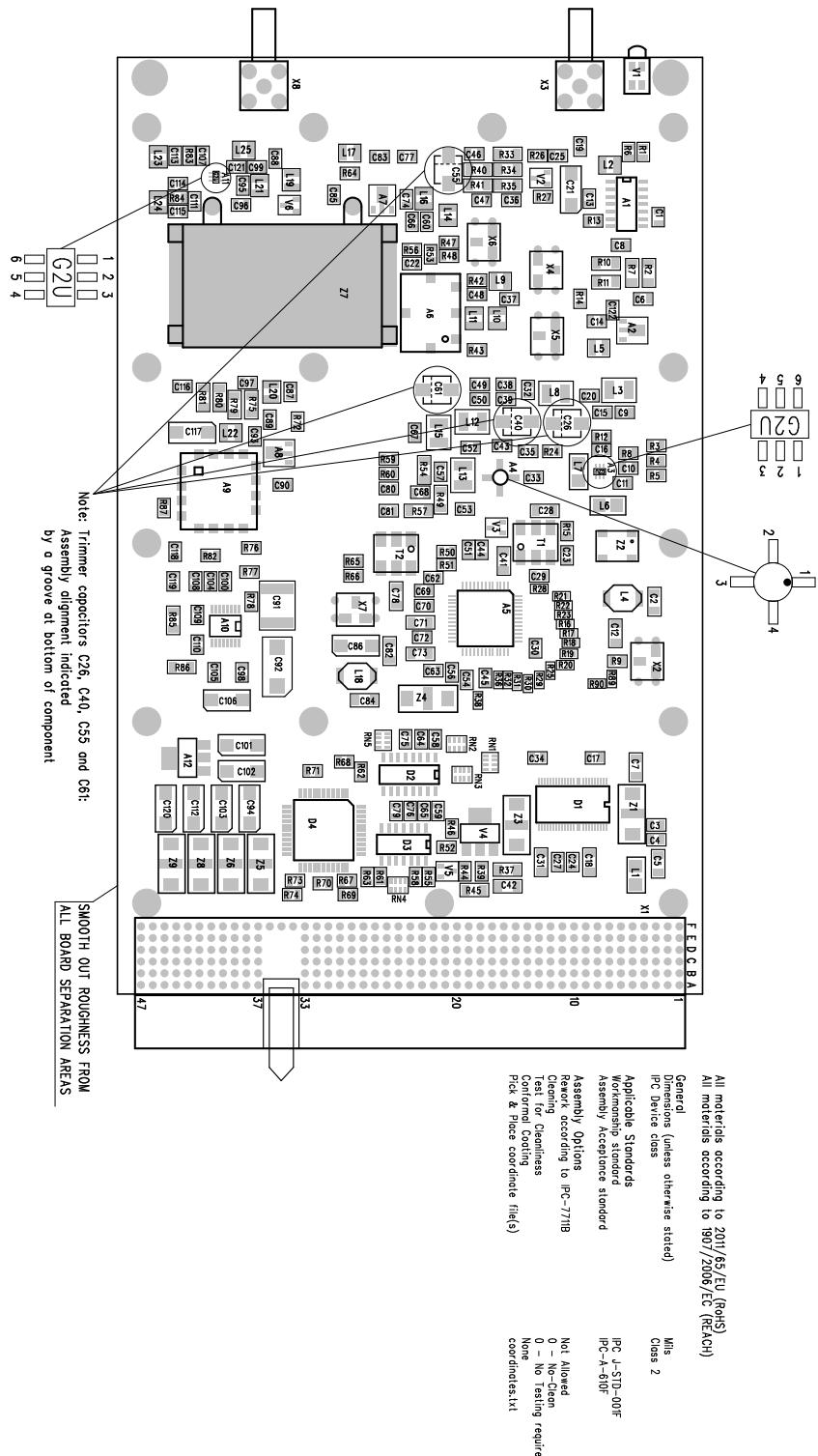


Figure 22 MRR111 and MWR321 Components Layout

4.2 Receiver Processor MRP121A

4.2.1 Introduction to MRP121A

Receiver Processor Unit MRP121A is a plug-in E1-size processor unit. It is used with the 400 MHz Receiver Unit to build up a digital radio receiver (Software Radio). Receiver Processor Unit MRP121A takes the digital IF data input from the receiver unit at the rate of 64 Msamples/s and all further receiver functions are performed digitally in the Receiver DSP Unit. In addition to radio receiver functions, the unit includes a local GPS receiver.



Figure 23 Receiver Processor Unit MRP121A

The Receiver DSP Unit contains three Digital Down Converter (DDC) chips, a Digital Signal Processor (DSP), a Field Programmable Gate Array (FPGA), a GPS receiver block, and input/output signals for receiver controls and for external communication.

Each DDC chip is a four-channel device containing digital mixers, a quadrature carrier Numerically Controlled Oscillator (NCO), digital filters, a resampling filter, an Automatic Gain Control (AGC) loop, and a cartesian-to-polar coordinate converter providing magnitude and phase output data at each channel.

The Digital Signal Processor is a complete 32-bit floating-point device integrating data processing elements, a large high-speed memory (SRAM), and I/O peripherals. In addition, fast external synchronous burst memory (SBSRAM) is provided.

Field Programmable Gate Array (FPGA) is an in-circuit-configurable logic chip, which is used to handle control and data connections between system blocks.

The GPS receiver is based on a commercial 16-channel receiver module, which provides precision timing and raw data outputs.

An RS232-compatible serial interface is provided for connection to an external GPS receiver.

A high-speed SERDES link is provided for connection to a required external main control processor.

The DSP Unit and FPGA circuit do not have operating codes at power-up. The external control processor takes the MRP121A into use by first loading the FPGA code via SERDES interface. In the second phase, the DSP code is loaded via SERDES/FPGA, and the operation starts when DSP responds via SERDES output channel.

Mechanically the MRP121 consists of three main parts: components board DRW226093, cooling plate and front panel. All electronics and connectors are located in the components board. The cooling plate has a component-by-component machined high profile at the inner side to effectively cool down component surfaces via a thin layer of soft heat transfer material. The front panel has handle and locking screws for fixing the unit in the card frame.

4.2.2 Functional Descriptions

4.2.2.1 Introduction to SERDES Interface

All system-level code loading, operation control, and data communication takes place via the SERDES interface. This interface has a 16-bit input channel from external control processor and a 16-bit output channel to the control processor. Both channels are connected serially via balanced differential lines to the corresponding SERDES interface at the external control processor.

In an operation with the standard 33.333 MHz word rate, the serial bit rates are 600 Mbits/s on both channels.

4.2.2.1.1 Initialization of SERDES Interface

At power-up, the 33.33 MHz reference clock is supplied to D12/4 from D4/21, and the SERDES interface is initialized as follows:

1. Control processor transmits a special sync-pattern.
2. D12 receiver gets synchronized to the pattern.
3. Received synchronized clock is supplied to the transmitter.
4. Transmitter starts sending the sync-pattern to the control processor.
5. Receiver at the control processor is synchronized.
6. Control processor drives ROUT15 (D12/73) high to indicate a synchronized loop.
7. Transmitter at MRP121A enters the normal operating mode.

4.2.2.1.2 FPGA Code Load

When operational, the interface is first used in a special mode to load the FPGA operating code. In this mode, it connects the 8-bit parallel data, chip select signal, and write strobe from external control processor to the code load inputs of the MRP121 FPGA. Code loading is started with low-to-high transition in Config# signal.

The following table lists the signals used in the FPGA code load:

Table 17 Signals Used in FPGA Code Load

Connection	Signal	Description
RSD00	CONFIG#	Configuration start
RSD01	D0	Data 0 in configuration (D9-A/D4)
RSD02	CS#	Chip select
RSD03	WS#	Write strobe
RSD04	RS#	Read strobe (not used)
RSD05	D1	Data 1
RSD06	D2	Data 2
RSD07	D3	Data 3
RSD08	D4	Data 4
RSD09	D5	Data 5
RSD10	D6	Data 6
RSD11	D7	Data 7
RSD12	Not used	
TSD00	CONF#	Configuration done
TSD01	STATUS#	Device status
TSD02...12	Not used	
TSD00	CONF#	Configuration done
TSD01	STATUS#	Device status
TSD02...12	Not used	

4.2.2.1.3 LPC Link

In normal operation, the SERDES interface is used to connect the 5-bit LPC bus between the external control processor and MRP121A. In addition to the LPC bus, some data and control signals are connected via the link.

[Table 18 \(page 52\)](#) lists the signals used in the operation mode:

Table 18 Signals Used in Operation Mode

Connection	Signal	Description
RSD00	Not used	Permanent high level
RSD01	Not used	Permanent high level
RSD02	LFRAME#	Indicates start of a new cycle from LPC bus.

Connection	Signal	Description
RSD03	LAD_IN0	LAD_IN0 ... 3 are multiplexed command, address and Data from LPC bus.
RSD04	LAD_IN1	
RSD05	LAD_IN2	
RSD06	LAD_IN3	
RSD07	TD_TO_GPS	Serial data to GPS receiver
RSD08..12	Not used	Permanent low level
TSD00	CONF_D	Not used. Permanent high level
TSD01	STATUS#	Not used. Permanent high level
TSD02	LAD0	LAD0 ... 3 are read data to the LPC bus. Two time multiplexed 4-bit nibbles are read in a cycle.
TSD03	LAD1	
TSD04	LAD2	
TSD05	LAD3	
TSD06	DSP_IRQ	Interrupt request from the DSP
TSD07	RD_FROM_GPS	Serial data from the GPS receiver
TSD08	STRTIN#	Start/event marker signal to MPU
TSD09 ..12	Not used	Permanent low level

4.2.3 Programmable Logic Device (FPGA)

4.2.3.1 Introduction to FPGA

The Field Programmable Gate Array (FPGA) is a digital, user-configurable Integrated Circuit (IC) that is used to implement custom logic functions. The D9 is a SRAM-based FPGA, which is in-circuit configurable. Its configuration (program) code is stored in the solid-state memory of the Main Processor Unit and the configuration takes place during the system power-up. The FPGA D9 is used to implement various timing, control, and interface logic functions in MRP121A.

In the circuit diagram, the FPGA D9 is divided into six parts:

- D9-A contains common control signals, special I/O signals, and five general purpose I/O signals
- D9-B contains 76 general purpose I/O signals
- D9-C contains 76 general purpose I/O signals
- D9-D contains 76 general purpose I/O signals
- D9-E contains 76 general purpose I/O signals
- D9-F contains power connections

The main functional blocks are described in more detail in the following paragraphs.

4.2.3.1.1 Clock Inputs

25 MHz input is the main clock signal for synchronous system logic.

The received clock from the SERDES interface (D12/49) is used for SERDES I/O functions.

4.2.3.1.2 Serdes Interface

The SERDES interface connects the FPGA to the data in and data out buses of the SERDES data link D13. Data is transmitted at the rising edge of the TCLK clock and received at the rising edge of the RCLK clock. In normal operation, the LPC bus of the computer module is linked to the Receiver DSP Unit, and in bus-read commands, adequate number of wait cycles are added to comply with the return delay time of the link.

4.2.3.1.3 LPC Bus Interface Connections with Bus Signals via SERDES

The LPC bus signals from the Main Processor Unit are connected via SERDES to the LPC bus interface of the FPGA. The LPC bus interface extracts the address and data bits from the nibble serial bus format in the write commands. In read commands, address bits are first extracted and data from the addressed read port is then driven to the bus.

4.2.3.1.4 PLL Programmer and Serial DAC Interface

PLL programmer sets the clock multiplier D27 for 40 MHz clock output by loading a 24 bit serial control word 330C02 (hex) into D2 with 1 MHz data clock. MSB is sent first and data load signal PLLLD is generated at the end. One programming cycle is automatically generated after FPGA configuration.

After the PLL programming, the same data, and clock signals are used for serial DAC A7 control. The 12-bit DAC code 800 (hex) is automatically sent after the PLL programming, and later on the interface runs under DSP control. The clock rate is 3.125 MHz, and signal DA4LD is used to load the data.

4.2.3.1.5 DSP Control and Data Interface

The DSP control interface connects reset, clock, and clock mode control signals to the DSP. The reset signal is released after the clock and clock mode control signals are active.

The operation of the DSP is controlled by the reset setting. After reset, the DSP starts reading boot code from link port 4.

Data flow from the LPC bus to DSP via link port 4:

Data to the DSP is written from the LPC bus as two 8-bit bytes in two or four byte packets. The FPGA logic writes the data in byte or nibble serial format to DSP link port 4. In the 16-bit mode, four nibbles are written after every two LPC bytes, and in the 32-bit mode, four bytes are written after every four LPC bytes. The nibbles are written in lower four bits of link port data. The FPGA logic and link port receiver are fast enough to keep the LPC port always ready for the next word write. For special use and diagnostics purposes, the port status can be checked by reading the status word.

The byte and nibble order at link port 4 are according to the following tables (B1 and B3 are high bytes at LPC bus, N3 is the highest nibble):

Byte order in the 32-bit mode:

Words written from the LPC	Bytes written to the link port
----------------------------	--------------------------------

1.	W1 (B1, B0)	1.	B3
2.	W2 (B3, B2)	2.	B2
		3.	B1
		4.	B0

Nibble order in the 16-bit mode:

Words written from the LPC		Nibbles written to the link port	
1.	W1 (B1, B0)	1.	N3
		2.	N2
		3.	N1
		4.	N0

Data flow from the DSP to the LPC via link port 5:

Data from the DSP is written in four-byte packets to four data registers in the FPGA, and further writes are inhibited until the registers are read as two 16-bit words (four LPC bytes) by the LPC interface. The link port is fast enough to provide data for continuous full speed read at the LPC bus. Data availability can also be checked by reading the status word. For diagnostics purposes, an empty read condition is indicated.

Byte order in the LPC read is according to the following table:

Bytes from the LPC		Words read by the LPC	
1.	B0		
2.	B1	1.	W1 (B2, B3)
3.	B2		
4.	B3	2.	W2 (B0, B1)

4.2.3.1.6 DSP Command Interface

The command interface connects to serial port 0 of the DSP. The rising edge of the transmit frame sync signal (DSTFSO) starts the operation and a serial 32-bit command is clocked in from transmit data line (DSDTO) and latched in parallel register at every 32 clocks (DSTCLK0) as long as the frame sync signal stays high. After reception, each command is executed and required actions are generated.

The 32-bit command word contains a direction bit, 7 device address bits, 8 register address bits, and 16 data bits.

In a read command (direction bit = 1) frame sync signal (DSRFSO) for input port is generated, followed by 16 data bits to the serial input data line (DSDRO).

The interface supplies a continuous 25 MHz external bit clock signals for output (DSTCLK0) and input port (DSRCLK0) data clocks.

4.2.3.1.7 DDC Control Interface

The DDC control interface generates control signals to the DDC chips, IF data receivers, and clock selectors. In addition, it transfers control data to and from the data bus of the DDC chips. For bus singals, see chapter Digital Down Converters (DDC), section [Control Bus \(page 61\)](#).

The control interface works under the control of the DSP command interface.

4.2.3.1.8 DDC Data Interface

The DDC data interface receives two serial data streams from the output ports of each DDC, converts both 224-bit serial data streams into byte format (28 bytes each), and writes the bytes in two separate FIFO memories. When complete data frames are received, the interface starts writing the data to the DSP link port and simultaneously the serial inputs are ready to receive next data frames. The frame sync signal starts the reception of a new data frame.

The frame rates depend on the DDC processing parameters.

Serial bit burst rates are 2×32 Mbits/s and link port byte burst rates are 16 Mbytes/s in each DDC connection.

DDC1, DDC2, and DDC3 are connected to link ports 1, 2, and 3, respectively.

4.2.3.1.9 Frequency Meter

The programmable frequency meter supports cycle time measurements of MUXFREQ and 1PPS input signals. The cycle times of all PLL frequencies can also be measured. The frequency meter is used by the DSP command interface.

4.2.3.1.10 A to D Control Interface

The A/D control interface is used to set the desired control outputs for the A/D converter according to the control commands via the DSP command interface.

Serial output data and sync signals from the A/D converter are passed via FPGA to the serial port 1 of the DSP unit.

4.2.3.1.11 Dual D to A Interface

The dual D/A interface connects the DSP link port 0 or DDC3 output data to the dual DAC A9. The converter has two operating modes:

- Normal mode: the DAC is connected to link port 0
- Direct DDC3 mode: the DAC is connected to the DDC3

In normal mode, the link port data is written to the DAC in four byte packets. Bytes 0/1 are the DAC1 LSB/MSB, and bytes 2/3 are the DAC2 LSB/MSB. Bits 4...7 in the MSB bytes are not used.

The port output rate is externally controlled by LPOACK according to the rate setting.

In the direct DDC3 mode, the 12 most significant bits of DDC3 serial data stream A are converted in parallel and directed to the DAC1. The output rate is the frame rate of the DDC3 output.

4.2.3.1.12 ADC Dither Generator

The ADC dither generator is a pseudorandom digital noise generator whose output can be used to add a dither signal to the input of an external A/D converter.

The generator is a 15-bit linear feedback shift register operating at the 3.125 MHz clock frequency. The generator can be enabled/disabled with a DSP command.

4.2.3.1.13 Receiver Control Interface

This interface is addressed by the command interface of DSP, and it writes control data to the serial synchronous control bus for the receiver modules. The bus comprises the following signals:

- Bus clock (GPOUT1)
- Serial control data (GPOUT2)
- Serial received data (GPIN1)

The following fixed length 21-bit format is used in bus commands:

Table 19 21-bit Format Used in Bus Commands

	Start	Dev. addr.	Reg. addr.	Stop	Stop
Bit	0	bits 1 ... 4	bits 5 ... 9	bits 10 ... 17	bits 18... 20
Signal	STA	DAO ... 3	RAO ... 4	D0 ... 7	STO 0 ... 2

A control command starts with a single start bit, followed by the device address, register address, control data, and stop bit fields.

The device address is used to select a unit in the bus, register addresses are used to select control functions inside a unit. Each unit has a unique fixed device address.

In read command, the 4-bit device address and an 8-bit data byte are received from the addressed unit.

The standard bit clock frequency is 100 kHz, but some special commands may use lower bit rates. The bus clock runs only during active commands.

MRP121A is a bus master and only it can drive the clock and control data lines. The received data line has pull-down resistors (R9, R13) in MRP121A, and each addressed unit can drive the line to a high level when transmitting serial data in a read command.

4.2.3.1.14 Antenna Switch Control

The antenna switch control provides reset and clock signals for an external antenna switch. The interface has two operating modes:

- In command mode, the control signals are used under direct DSP control.
- In automatic rotation mode, a repeated sequence of reset signals followed by 12 clock pulses are generated at programmable clock pulse interval and the current antenna positions (clock pulse counts after reset) are inserted in the data frame of the DDC2.

The reset signal is GPOUT3 (X1/D21) and the clock signal is GPOUT4 (X1/E21).

4.2.3.1.15 Data Output Registers

The control signals for LED lamp, status output, and general-purpose I/O lines are provided. The outputs are controlled by the LPC interface.

4.2.4 GPS Receiver

4.2.4.1 Introduction to GPS Receiver

The GPS receiver is based on the LEA-6T receiver module (A10). LEA-6T is a 50-channel receiver with precision timing and raw data output functions. Data communication takes place via serial data lines RD_FROM_INT_GPS and TD_TO_INT_GPS. In addition, precision GPS timing is available with the INT_GPS_1PPS signal.

GPS_RESET# control signal is for possible future use.

4.2.4.2 Antenna Connection

The GPS antenna signal is connected from the GPS ANT connector in front of the unit via short circuit board strip line to the RF input (A10/16) of the GPS module.

The power feed for the external antenna amplifier is provided from +5 VDC system voltage via RF input. The regulator A12 is used to limit the worst case short circuit current below 250 mA. The regulator output is fed via an open circuit detector and filter chokes (Z4, Z3) to the receiver module V_ANT input, from where it is internally connected to the RF input via a short circuit protection switch and bias-T coil.

Transistors V5 and V7 with shunt resistor R19 work as detectors for the open antenna circuit. If the antenna current is below 3...5 mA, the transistor V5 conducts the driving signal ANT_OPEN at high level for indication of an open antenna circuit.

Short circuit detector and protection switch are provided as internal functions of the GPS module.

4.2.4.3 Power Supply

The +3.3 VL operating voltage for the GPS receiver module is regulated linearly from the +5 V system voltage to get clean power for the sensitive GPS circuitry.

4.2.5 Digital Signal Processor DSP

4.2.5.1 Introduction to DSP

D13 (ADSP-21160) is a general purpose 32-bit Digital Signal Processor (DSP). It contains a processor core, 524kByte internal RAM, an I/O processor, and an external port. The I/O processor provides six 8-bit link ports and two serial ports for external communication. External port is used for 64-bit external memory connection.

The external clock frequency is 40 MHz and the core runs at 80 MHz. During power-up, a separate clock signal is supplied through a resistor. The final 40 MHz clock overrides this clock when the FPGA code is loaded.

In the circuit diagram, the processor D13 is divided into four parts:

- D13-A contains the common control signals

- D13-B contains the data bus interface
- D13-C contains the serial ports and link ports
- D13-D contains the power connections

4.2.5.2 Boot Loading

DSP has an internal ROM-based boot loader program. At power-up, the processor reset input signal (DSPRST#) is held active until the control processor is ready to communicate with the DSP. After the DSP reset is released, the internal boot loader program of the DSP is directed (by setting inputs LBOOT=1, EBOOT=0 and BMS#=1) to fetch an external program code from link port 4. The control processor writes the code to the port in a half-byte serial format, and after the whole start code block is transferred, it is executed by the DSP and a response is sent back to the control processor.

4.2.5.3 External SBSRAM

High speed SBSRAM (Synchronous Burst Static Random Access Memory) chips D38 and D14 are connected to the 64-bit external bus of the DSP. The chip size is 524288 x 32 bits (2MBytes) and the total memory size is 524288 x 64 bits (4MBytes). Standard system uses this memory as data storage. Address signals DSPA20 and DSPA21 are connected for possible future use with larger capacity memory chips.

4.2.5.4 Interrupts, Flags, and Timer

The DSP has three external interrupt pins (DSPIRQ0#, DSPIRQ1#, DSPIRQ2#), four flag pins (DSPFL0...3), and one timer pin (DSPTIMER).

Interrupts are used in external communication. Flags and timer are for special needs and for possible future use.

4.2.5.5 Link Ports

The DSP has six bi-directional link ports for external data transfer. Each port has internal FIFO (First-In-First-Out) buffer memories for input and output data. Each port has two control signals for data transfer, port direction is set by the DSP software. All port signals are connected to the FPGA, which includes the interface logic between the port and the destination connection.

The ports are used for the following data transfer channels:

- Port 0 is for dual DAC data output
- Port 1 is for DDC1 data input
- Port 2 is for DDC2 data input
- Port 3 is for DDC3 data input
- Port 4 is for data input from the control processor
- Port 5 is for data output to the control processor

4.2.5.6 Serial Ports

The DSP has two bi-directional high-speed serial ports for external data transfer. Each port has internal FIFO (First-In-First-Out) buffer memories for input and output data. Each port has three signals for both directions: clock, frame sync, and serial data.

Port 0 is used as the command interface between the FPGA and the DSP.

Port 1 is used for A/D converter data input. The bit clock frequency is 12.5 MHz.

4.2.5.7 JTAG Port

The serial JTAG test access port (TCK,TMS, TDI, TDO and TRST#) and EMU# control signal are for product development and are not used in the normal operation.

4.2.6 IF Data Receivers

IF (Intermediate Frequency) sample data from an external A/D converter are connected to MRP121A with a high-speed serial data link. Data from converter uses three serial data streams and a reference clock signal. At the transmitter end the parallel A/D converter data is clocked in the serializer circuit as three 7-bit groups, and the circuit transmits these groups serially with a bit rate of seven times the clock frequency.

In MRP121A, the deserializer circuit (D15, D23 or D27) multiplies the clock signal by seven and samples the incoming data streams by this multiplied clock rate to get the 7-bit groups back to the original parallel format. The resulting 21-bit data word is clocked out at the basic clock rate.

All data streams and clock signals use low-voltage differential signaling (LVDS).

The standard basic clock rate is 64 MHz, which results in a 448 Mbit/s rate at the data bit streams.

Data bits D0...3, D5...10, and D12...17 are used for A/D data (bits D0...1 are permanently low-level with the 14-bit converter).

Bits D4, D11, and D18 are permanently high-level (for diagnostics purposes) and bit D19 indicates overrange signal at the converter. Data bit D20 is not used.

4.2.7 Digital Down Converters (DDC)

4.2.7.1 Converter Circuits

Circuits D3, D6, and D10 are identical digital down converters (HSP50216). Each has four data input ports and four internal converter channels. Each channel includes digital mixers, a quadrature carrier NCO, digital filters, a resampling filter, an AGC loop, and a converter for phase and magnitude data output.

All converter channels have data selectors for connection to the desired data input port.

4.2.7.2 Data Inputs and Clock Selection

Data outputs from the IF data receiver 1 (D15) and 2 (D23) are connected to all DDC circuits, receiver 1 to A input ports and receiver 2 to B input ports. Data from receiver 3 (D27) is connected to C input port of converter D4.

In addition, data from receiver 1 is connected to the FPGA for diagnostics purposes. This connection can also be used to feed test data from the FPGA to all converter circuits.

The clock selectors are provided for all down converters to allow connection to the clock signal that corresponds to the selected data connection.

Buffer circuits D26 and D28 are used to select clock signal for converter 1: SERDES clock 1 is selected when D26 is active ($DC1SEL1 = 0$) and clock 2 is selected when D28 is active. The test clock signal from the FPGA is selected when both buffers are inactive.

Buffers D29, D31, D24 are used in the same way to select the clock for converter 2, and buffers D32, D34 select the clock for converter 3.

4.2.7.3 Control Bus

The DDC circuits are controlled via the control bus from the DSP via the FPGA. The chip select signals ($DC1CE\#$, $DC2CE\#$, $DC3CE\#$) select the active converter, address signals ($DCA0...2$) select internal registers, control strobes ($DCWR\#$, $DCRD\#$) select the write or read operation, and data lines ($DCD00...15$) carry the control data.

In addition, reset ($DC1RST\#$, $DC2RST\#$, $DC3RST\#$) and synchronize ($DC1SYNC$, $DC2SYNC$, $DC3SYNC$) inputs and interrupt outputs ($DC1INR\#$, $DC2INR\#$, $DC3INR\#$) are provided.

4.2.7.4 Data Output

The DDC circuit has four serial ports for data output. In MRP121A, ports A and B from all converters are in use. Each port comprises data and synchronize signals ($DC1SD1A$ and $DC1SYNA$ for converter 1 port A), and each converter chip uses a common data clock signal ($DC1SLK$ for DDC 1). Standard bit rate is 32 Mbits/s.

All serial data streams are converted as 8-bit byte streams in the FPGA and are further fed to the DSP via link ports.

4.2.8 A/D Converter

4.2.8.1 Input Selector and Buffer Amplifier

Input selector D21 is controlled by $ADSEL0...2$ signals. The following input channels are available:

Table 20 Input Channels

Channel	Signal	Description
0	ANTIN	Antenna input for possible future use
1	GND	Ground (0 V)
2	MRRMUX	MRR111 multiplexer output
3	+3.3VOSC	+3.3 V oscillator supply voltage
4	DA1T	D/A converter 1 test output
5	DA2T	D/A converter 2 test output
6	+2.5V	+2.5 V supply voltage
7	-12/+5V	-12/+5 V test voltage (+3.45 V nom.)

The active input voltage range for all inputs is 0.0 to 4.75 V (limited by the supply voltage of the selector).

Buffer op amp A8-B connects the selector output to the single-ended/differential amplifier A2, which further buffers the signal to the A/D converter. The gain of the circuit is 2/3.

The output of A8-B is also fed to the FPGA (signal MUXFREQ) for direct frequency measurements.

The converter active input voltage range is +0.5 ... +4.5V, which corresponds to a range of -0.5 ... +5.5V at the selector input.

4.2.8.2 Converter Circuit

The A5 (AD7723) is a 16-bit, sigma-delta analog-to-digital converter (ADC). The converter is used with the 12.5 MHz clock signal (ADCLK), resulting in the 390 kHz sample rate.

The converter data interface is serial and connects through the FPGA to the DSP. Signals' serial clock output (ADCSCO), serial data output (ADCSDO), and frame sync output (ADCFSO) are used in the serial data connection.

The output code is in two's complement binary format and the output equation is:

$$\text{Dout} = (\text{Vin} - 2.5) / 0.000091552$$

where

Dout = digital output code [two's complement binary]

Vin = analog voltage at selector input [V]

4.2.9 Support Logic

4.2.9.1 Clock Oscillator

The TCXO type clock oscillator Z1 provides the 10 MHz timing reference for MRP121A. The oscillator frequency is fine-tuned by the control voltage from the D/A converter A7 via amplifier A6-A to the VC input.

The oscillator output is amplified by the A6-B and buffered by the D22 to the main 10 MHz reference.

Linear regulator A4 supplies +3.3V operating voltage to the clock oscillator and PLL circuits.

4.2.9.2 MRP121A PLL Clock Multipliers

PLL (Phase Locked Loop) clock multipliers are used to generate all the required system clock signals from the 10 MHz reference clock source.

PLL circuits D4 and D1 are pin-programmed for the desired output frequency. Circuit D4 generates the 33.333 MHz clock for the SERDES data link and D1 generates 25 MHz for the FPGA logic.

PLL circuit D2 is serially programmable for the desired output frequency. In the standard MRP121A, the output frequency is programmed to 40 MHz for the DSP clock.

4.2.9.3 MRP121A Voltage Regulators

Linear voltage regulators are used to generate the required +2.5 V internal operating voltages from the +3.3 V system voltage.

Regulator A1 generates +2.5 V for the core voltages of the FPGA.

Regulator A15 generates the +2.5 V core voltage (+VDSP) for the 0020DSP.

4.2.9.4 MRP121A Reset Circuit

Circuit A16 controls the reset signal RES#, which is forced to the active low state if at least one of the following conditions apply:

- +5 V operating voltage falls below +4.5 V
- +3.3 V operating voltage falls below +3.0 V
- +2.5 V operating voltage falls below +2.2 V
- Internal reset line SELFRES# is in 0-state
- External reset line MRES# is in 0-state

The reset output signal is held active typically 200 ms after the reset condition disappears.

4.2.9.5 LED Lamps

Test lamp V1 is a red/green bi-color LED type lamp. The red and green lamps are controlled by signals REDLED# and GRNLED# from the FPGA D9. Yellow color is produced when both lamps are on.

During system reset, yellow color is shown. After the reset, the red lamp remains on during the boot sequence of the control processor. When booting is complete, the red lamp is switched off and the green lamp is switched on to indicate normal device operation.

4.2.9.6 Temperature Sensor and Voltage Monitor

Temperature sensor and voltage monitor circuit A17 measures the circuit board temperature, three system voltages (+3.3V, +5V, +12V) and internal voltage +VDSP.

The sensor is controlled serially via the clock (SBCLK) and data line (SBDATA). Control is performed by the control processor via the chip interface in the FPGA.

4.2.9.7 Remote Start

The signals STRTOUT (X1/A40) and STRTIN (X1/B40) are intended for the remote start or general purpose event marker input. In the external circuit, the STRTOUT is looped back to the STRTIN via a momentary switch, and a closing (or opening) switch contact is used to indicate sounding start or event mark. Minimum detectable pulse length is 0.1 s.

Alternatively, a ground referenced TTL or RS232 level pulse connected to the STRTIN input can be used.

The external switch or signal should be in the idle state during system power-up to allow the correct idle reference to be read.

4.2.9.8 MRP121A Rack Code

The rack code inputs R0IN# and R1IN# from system connector pins A45 and B45 are fed to control processor via the FPGA for information about the operating environment.

4.2.9.9 MRP121A Hardware Code

The 4-bit hardware code from the FPGA (D9-D) input pins H21, AA21, R21, and J22 is fed to control processor via the FPGA for information about operating the hardware environment of MRP121A.

4.2.9.10 Status Output

The STAT_OK control output from the FPGA controls the D18 buffer which drives the status signal output at system connector pin E37 to a low level when STAT_OK = 0.

The status signal output line is used at the system level to indicate the status of internal units.

4.2.9.11 MRP121A Test Input

The test input from system connector pin B39 is fed to the control processor via the FPGA for testing purposes. Leave the input unconnected in normal operation.

4.2.10 MRP121A Parts List

Table 21 MRP121A Parts List

Reference	Part Number	Description
Assembly ref. 001	DRW227303	Front Panel Machining for MRP121
Assembly ref. 002	210854	EMC Gasket 3U, Schroff 21101-854
Assembly ref. 003	210853	Injector/Ejector Handle4HP,IEL,Schroff 20817-613
Assembly ref. 004	210856	Board Holder Schroff
Assembly ref. 005	210855	Sleeve M2.5x3,Schroff 21100-660
Assembly ref. 006	210857	Collar Screw M2.5x12.3,Schroff
Assembly ref. 007	16097	ESD Warning Sticker
Integrated Circuits		
A1,15	27139	IC, Voltage Regulator2.5 V / 3 A, TO263-5
A2,3,6,8	210452	IC, Op. Amp. (Dual)AD8042AR (SMD)
A4,11,13,14	25757	IC, Voltage RegSOT-223, 3.3V/300mA
A5	010247	IC, Converter A/D16-BIT 1.2 MSPS
A7	25116	IC, Converter D/A Ex Serial low power 12-bit
A9	010032	IC, Converter D/AAD9765ASTZ
A12	17063	IC, Voltage Reg.SO-8, V.REG. 5V/50mA
A16	010148	IC, Supervisor MAX6355SYUT-T
A17	25815	IC, Converter A/DAD7417ARUZ

Reference	Part Number	Description
D1,4	27135	IC, Freq. Synthesizer ICS525R-02I
D2	210412	IC, Freq. Synthesizer ICS307M-02I
D3,6,10	27162	IC, Dig. Down Converter HSP50216
D5	19717	IC, Flip-Flop 74LV74
D7,8,11,18-20,22, 24-26,28,29,31, 32,34,36	26570	IC, Buffer Tiny NC7SZ125M5X_NL
D9	27133	IC, SRAM based PLD EP1K100F1484-2
D12	219689	IC, LVDS Serdes DS92LV16
D13	27170	IC, DSP ADSP-21160M
D14,38	27182	IC, SB SRAM 512k x 32 Synchronous SR
D15,23,27	010030	IC, LVDS Serdes Receiver SN65LVDS96
D16,17	19568	IC, Inverter TinyNC7S14, SOT23-5
D21	25495	IC, Analog MUX 8chMAX4051ACSE
D30,33,35	26108	IC, RS232C Transceiver MAX208EEAG
D37,39	26249	IC, Bus Transceiver 74LV245, TSSOP 20
Z1	210744	IC, Clock Oscillator VCTCXO 10MHz, SMD
Diodes		
V1	010192	Diode, LED 591-3001, Red and Green
V2-4	15976	Diode, Silicon Ex LL4148/ PMLL4148 (SMD)
V6	16059	Diode, Zener 3,9 V 5 % 500 mW
V8	17311	Transldiode 30V 600W/1mS +-5%
V9	17332	Diode, Transil 6.8V 57.A
V10,11	16004	Diode, Schottky Ex MBR0540T1G
Resistors		
R1,2,20,23-25,27, 28,30,36-39,49, 57,60,70 77,79, 82,83,85-89,93, 94,99,107,108, 110,111, 115-117, 119-121	26100	Resistor, Chip100R 1.0% 100ppm 0603
R3,6-8,10,15,21, 26,31-35,40-42, 45,47,52-54,58, 59,61,65-67, 69, 74-76,95-97, 100-106,112-114, 118,123,125-130, 132,138,141,143-145	25263	Resistor, Chip1K0 1.0% 100ppm 0603

Reference	Part Number	Description
R4,5,9,12-14, 16-18,43,48,55, 56,62,63,68,71-73,78 80,81,84, 90-92,98,131, 133-137,139,140, 142	25262	Resistor, Chip10K0 1.0% 100ppm 0603
R11,22,29,44,46, 50,51,64,109,122,124	010014	Resistor, Chip 21R5 1% 100ppm 0603
R19	15878	Resistor, Chip10R 5% 200ppm 1206
Transistors		
V5,7	11138	Transistor, PNP Ex MMBT3906, SOT-23
Capacitors		
C1,6,10,12,15,19,20,30-34,37,39, 40,43-47,50, 52-54,57-63, 65-80,82,83,85, 86, 88,89,92,93, 95-107	19941	Cap., Chip Ceramic100nF 10% X7R 16V 0603
C2,3,5,9,41,49,51,81,94	19959	Cap., Chip Tantalum10uF 10V 20% Case A
C4,7,16,17,21,23,25,28,29	217767	Cap., Chip Tantalum100uF 10% 16V Case D
C8,13,18,22,24	19462	Cap., Chip Ceramic2u2 16V X5R 1206
C11,14	18524	Cap., Chip Ceramic Ex 1n 5% NPO 50V 0805
C26,27	219924	Cap., Double Layer0.33F, 5.5V,-10...+85C
C35,38,90	25186	Cap., Chip Ceramic100p 5% NPO 50V 0603
C36,42,64,84,87, 91	19405	Cap., Chip Ceramic10n 10% X7R 50V 0603
C48	19915	Cap., Chip Ceramic470nF 10% X7R 16V 0805
C55,56	15621	Cap., Chip Ceramic Ex 100n 10% X7R 50V 0805
Connectors		
TP1,2	0172	Connector Pin Ex E03096L02
X1	210249	Connector, 2mm Metric 5 x 44 socket, press-fit
X2	220114	Connector, SMA Female,90 deg, PCB, B.H.
Miscellaneous		
A10	219022	GPS Receiver Module LEA-4T
L1-14	25097	Ferrite Bead Inductor Ex 2250ohm @100MHz, 0R8
Z2-4	25036	Filter, EMI (SMD)NFE61PT472C1H9L
	DRW227301	Heatsink

Reference	Part Number	Description
	220696	Screw, Crosshead, M2,5x10 DIN966 PZ A4
	211741	Therm. Conductive Liquid Gap Filler 1000, 50 cc
	5068	Screw-Lock Compound, Loctite 222
	212049	Screw, Crosshead M2,5x8 DIN966 PZ A4
	10948	Marking Sticker
	15223	Sticker Set, Matt White, Polyethylene
	16166	Plastic Label, 1180, 65+3mm
	PCB210491	Printed Circuit Board
	15223	Sticker Set Matt White, Polyethylene Assembly ref. 002, Serial number and barcode

4.2.11 MRP121A Technical Data

Table 22 MRP121A Digital Down Converters

Digital Down Converters	
Number of converters	3
Channels in a converter	4
Clock rate	64 MHz
Programmable Carrier NCO	32-Bit
FIR Out of Band Attenuation	110dB
Digital AGC	96dB Gain Range

Table 23 MRP121A Digital Signal Processor

Digital Signal Processor	
Processor type	ADSP-21160
Clock rate	80 MHz
Internal memory	524 kByte
External memory	4 MByte
Link ports	6
Serial ports	2

Table 24 MRP121A GPS Receiver

GPS Receiver	
Input connector	SMA, female
LNA power	+4.5 ... +5.0 V, 50 mA max.
Receiver type	LEA-6T
Channels	50
Time pulse	1 PPS

Table 25 MRP121A Communication Channels

Communication Channels	
SERDES link in	33.33 Mwords/s
SERDES link out	33.33 Mwords/s

Table 26 MRP121A Serial Line

Serial Line	
Serial line	RS232-C

Table 27 MRP121A Power Requirements

Power Requirements	
+3.3 V	3500 mA
+5 V	200 mA
+12 V	2 mA
-12 V	10 mA

Table 28 MRP121A General Technical Data

General	
Operating temperature	-30 ... +55 °C
Storage temperature	-55 ... +80 °C
Unit type	E1-size circuit board
Dimensions, length x width x height	190(L) x 128(W) x 20.5(H) mm
Weight	350 g
System connector	220-pin female
Status indicators	LED lamp

4.2.12 List of MRP121A Signals

Table 29 MRP121A Signal Names and Abbreviations

Signal	Description
+12V	+12 V operating voltage
+2.5V	+2.5 V operating voltage
+3.3V	+3.3 V operating voltage
+3.3VOSC	+3.3 V oscillator operating voltage
+5V	+5 V operating voltage
+VDSP	+ V DSP operating voltage
10MHZ	10 MHz clock signal
10MHZ+	10 MHz clock signal
10MHZ-	10 MHz clock signal
12M5HZ	12.5 MHz clock signal
1PPS#	1 pulse per second
25MHZ	25 MHz clock signal
ADAOR	Analog to digital converter A overrange
ADBOR	Analog to digital converter A overrange
ADCCFMT	Analog to digital converter serial clock format
ADCCLK	Analog to digital converter clock
ADCFSI	Analog to digital converter frame sync input
ADCFSO	Analog to digital converter frame sync output
ADCOR	Analog to digital converter A overrange
ADCSCO	Analog to digital converter serial clock output
ADCSCR	Analog to digital converter serial clock rate select
ADCSDO	Analog to digital converter serial data output
ADCSFMT	Analog to digital converter serial data format select
ADCSLDR	Analog to digital converter serial low data rate
ADCSLP	Analog to digital converter serial mode low pass filter
ADCUNI	Analog to digital converter unipolar input
ADDITH	Analog to digital converter dither
ADSELO ... 2	Analog to digital converter input select signals
AGND	Analog ground
ANTIN	Antenna input

Signal	Description
DA1OUT	Digital to analog converter 1 output
DA1T	Digital to analog converter 1 test signal
DA2OUT	Digital to analog converter 2 output
DA2T	Digital to analog converter 2 test signal
DA4LD#	Digital to analog converter data load
DAD00 ... 11	Digital to analog converter data 00 ... 11
DC1(2,3)CE#	Digital down converter 1 (2,3) chip enable
DC1(2,3)CLK	Digital down converter 1 (2,3) clock
DC1(2,3)CSEL1	Digital down converter 1 (2,3) clock select 1
DC1(2,3)CSEL2	Digital down converter 1 (2,3) clock select 2
DC1(2,3)ENI#	Digital down converter 1 (2,3) enable
DC1(2,3)INTR#	Digital down converter 1 (2,3) interrupt
DC1(2,3)RST#	Digital down converter 1 (2,3) reset
DC1(2,3)SCLK	Digital down converter 1 (2,3) serial data clock
DC1(2,3)SD1A	Digital down converter 1 (2,3) serial data 1 A
DC1(2,3)SD1B	Digital down converter 1 (2,3) serial data 1 B
DC1(2,3)SYNA	Digital down converter 1 (2,3) sync A
DC1(2,3)SYNB	Digital down converter 1 (2,3) sync B
DC1(2,3)SYNC	Digital down converter 1 (2,3) sync input
DC2CSEL3	Digital down converter 2 clock select 3
DCA0 ... 2	Digital down converter address 0 ... 2
DCD00 ... 15	Digital down converter data 00 ... 15
DCRD#	Digital down converter read
DCWR#	Digital down converter write
DSCDIS#	DSP start clock disable
DSDRO (1)	DSP serial port data 0 (1) receive
DSDTO (1)	DSP serial port data 0 (1) transmit
DSP	Digital signal processor
DSPA01 ... 21	DSP address 00 ... 21
DSPBRST	DSP burst
DSPCLK	DSP clock
DSPCLKM0	DSP clock mode
DSPD00 ... 63	DSP data 00 ... 63

Signal	Description
DSPEMU#	DSP emulator
DSPFLO ... 3	DSP flag 0 ... 3
DSPIRQ0# ... 2#	DSP interrupt request 0# ... 2#
DSPMS0#	DSP memory select 0
DSPRDH#	DSP read high end data
DSPRDL#	DSP read low end data
DSPRST#	DSP reset
DSPTIMER	DSP timer
DSPWRH#	DSP write high end data
DSPWRL#	DSP write low end data
DSRCLK0	DSP serial port receive clock 0
DSRCLK1	DSP serial port receive clock 1
DSRFS0	DSP serial port receive frame sync 0
DSRFS1	DSP serial port receive frame sync 1
DSTCLK0	DSP serial port transmit clock 0
DSTCLK1	DSP serial port transmit clock 0
DSTFS0	DSP serial port transmit frame sync 0
DSTFS1	DSP serial port transmit frame sync 1
GND	Ground
GPIN1(#)...6(#)	General purpose input 1 ... 6
GPIO5 ... 7	General purpose input/output 5 ... 7
GPOUT1(#)...7(#)	General purpose output 1 ... 7
GRNLED#	Green LED lamp control
I/O	Input / output
JTAG	Joint Test Action Group
JTCDIS	JTAG test clock disable
JTCK	JTAG Test clock
JTCKIN	JTAG bus test clock input
JTDI	JTAG test data input
JTDIN	JTAG bus test data input
JTDIFPGA	JTAG test data input FPGA
JTDO	JTAG test data output
JTMS	JTAG bus test mode select

Signal	Description
JTMSIN	JTAG test mode select
JTR#	JTAG test reset input
JTRIN#	JTAG bus test reset input
LPO(1,2,3,4,5)ACK	Link port O (1,2,3,4,5) acknowledge
LPO(1,2,3,4,5)CLK	Link port O (1,2,3,4,5) clock
LPO(1,2,3,4,5)DO ... 7	Link port O (1,2,3,4,5) data 0 ... 7
MRRMUX	Receiver board (MRR) multiplexer output signal
MUXFREQ	Multiplexer output signal frequency
FPGA	Field programmable gate array
PLLLD	Phase locked loop load
RO(1)IN#	Rack code 0 (1) input
RA0# ... 1#	Rack address 0 ... 1
RD3P	Received data 3 to FPGA
RD4P	Received data 4 to FPGA
RDA00 ... 15	Received data A 00 ... 15
RDB00 ... 15	Received data B 00 ... 15
RDC00 ... 15	Received data C 00 ... 15
REDLED#	Red LED control
RES#	Reset
RXD1 ... 4	Received data line 1 ... 4
SBCLK	Serial bus clock
SBDATA	Serial bus data
SELFRES#	Self reset
SERCCLK	Serial control clock
SERCD	Serial control data
SPCTRL	Spare control
SPOUT1	Spare output 1
SR1(2,3)CLK/CLK#	SERDES 1 (2, 3) clock signal pair
SR1(2,3)SD0/0#	SERDES 1 (2,3) data 0 signal pair
SR1SD1/1#	SERDES 1 (2,3) data 1 signal pair
SR1SD2/2#	SERDES 1 (2,3) data 2 signal pair
SR1(2,3)TDO ... 2	SERDES 1 (2,3) test data 0 ... 2
SRSDN#	SERDES shutdown

Signal	Description
STAT_OK	Status OK
STRTIN#	Start signal input
STRTOOUT#	Start signal output
SYSRES#	System reset
TEST#	Test signal
TS1 ... 5	Test signal 1 ... 5
TXD1 ... 4	Transmitted data line 1 ... 4

4.2.13 MRP121A Diagrams and Board Layouts

Table 30 MRP121A Diagrams and Board Layouts

Code	Description
DRW227377	MRP121A Block Diagram
DRW225649	MRP121A Circuit Diagram, 7 pages
DRW227371	MRP121A Assembly Drawing, 2 pages
DRW226093	MRP121A Components Layout, 2 pages

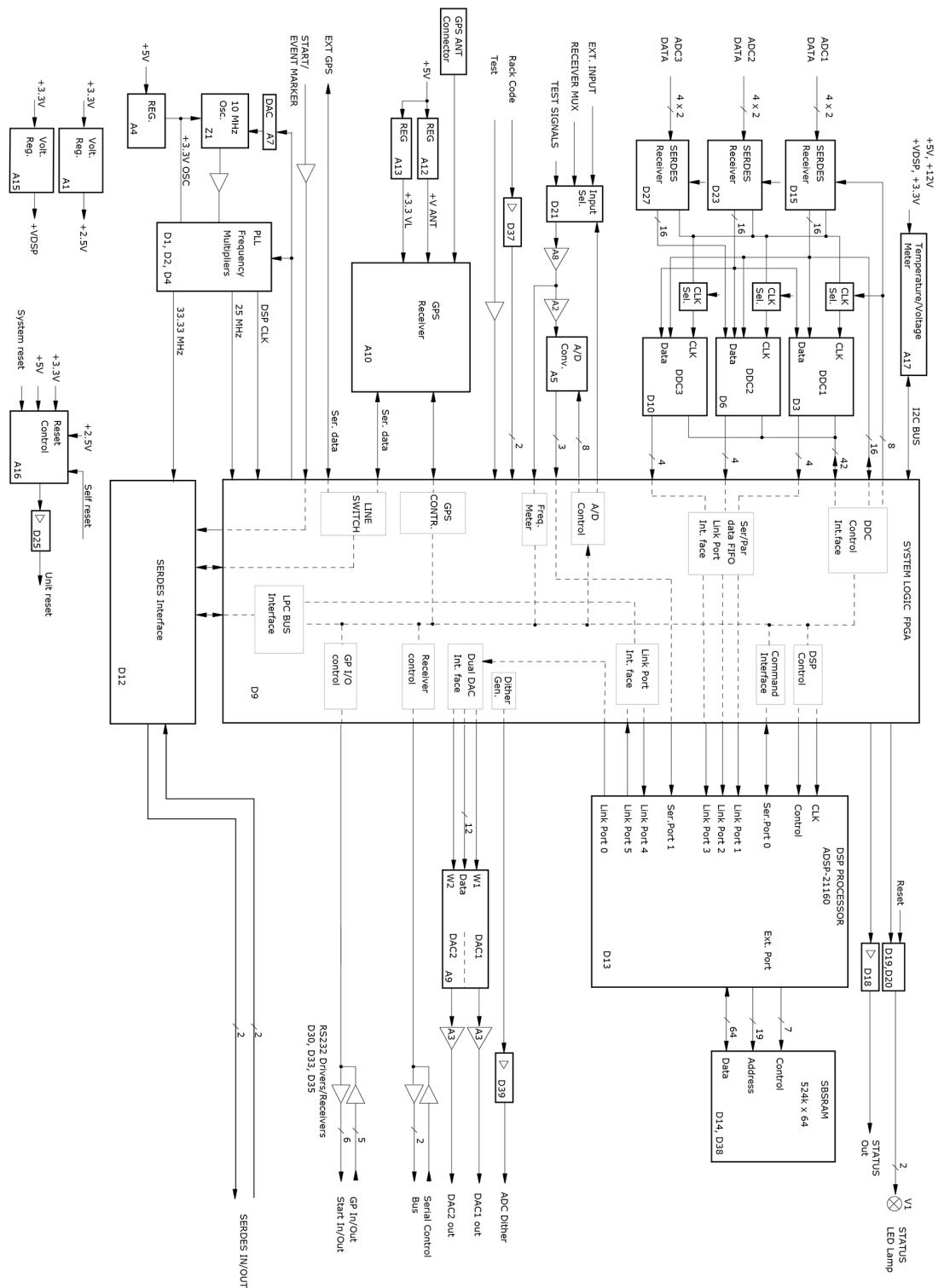


Figure 24 MRP121A Block Diagram

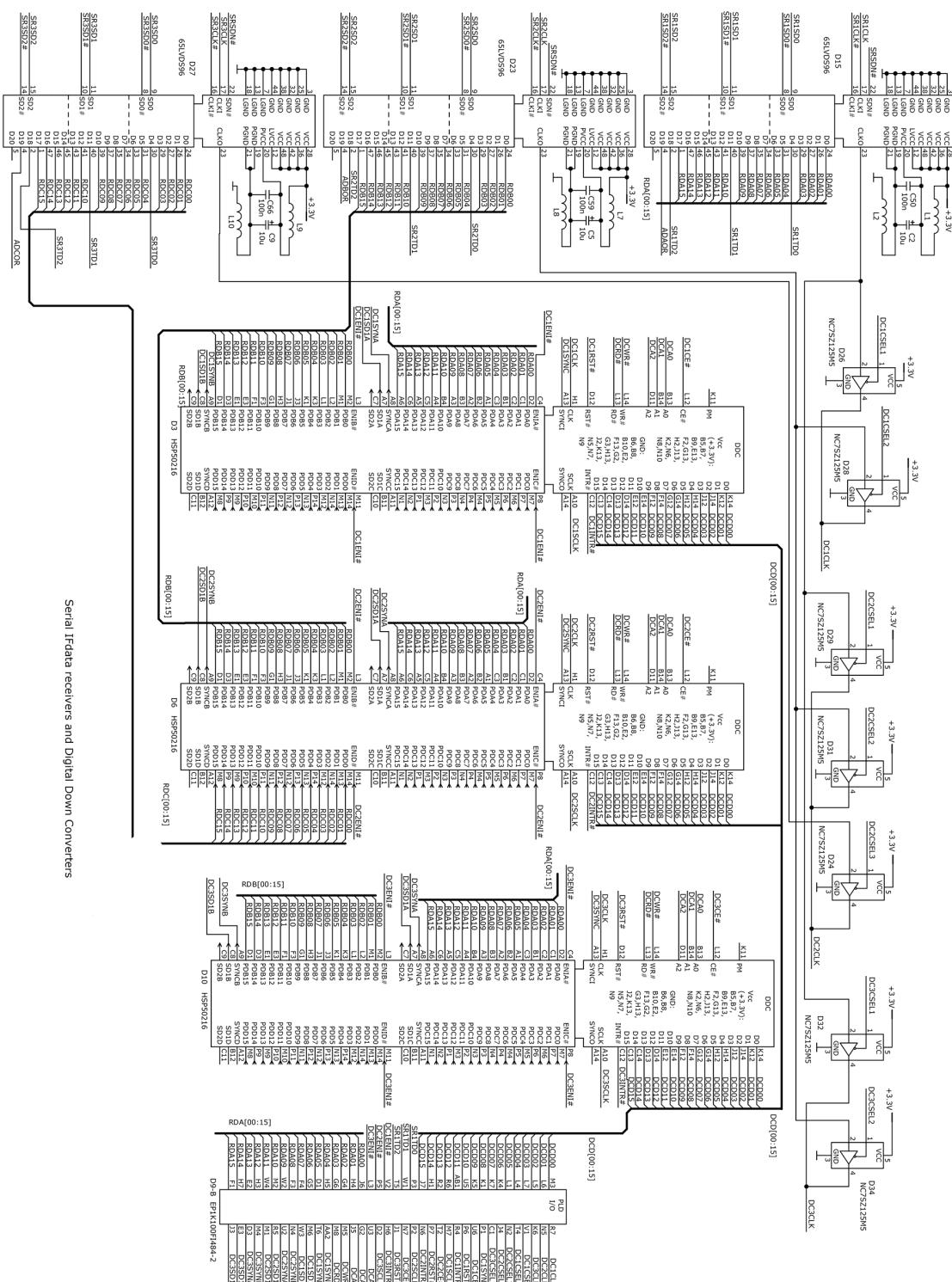


Figure 25 MRP121A Circuit Diagram, 1/7

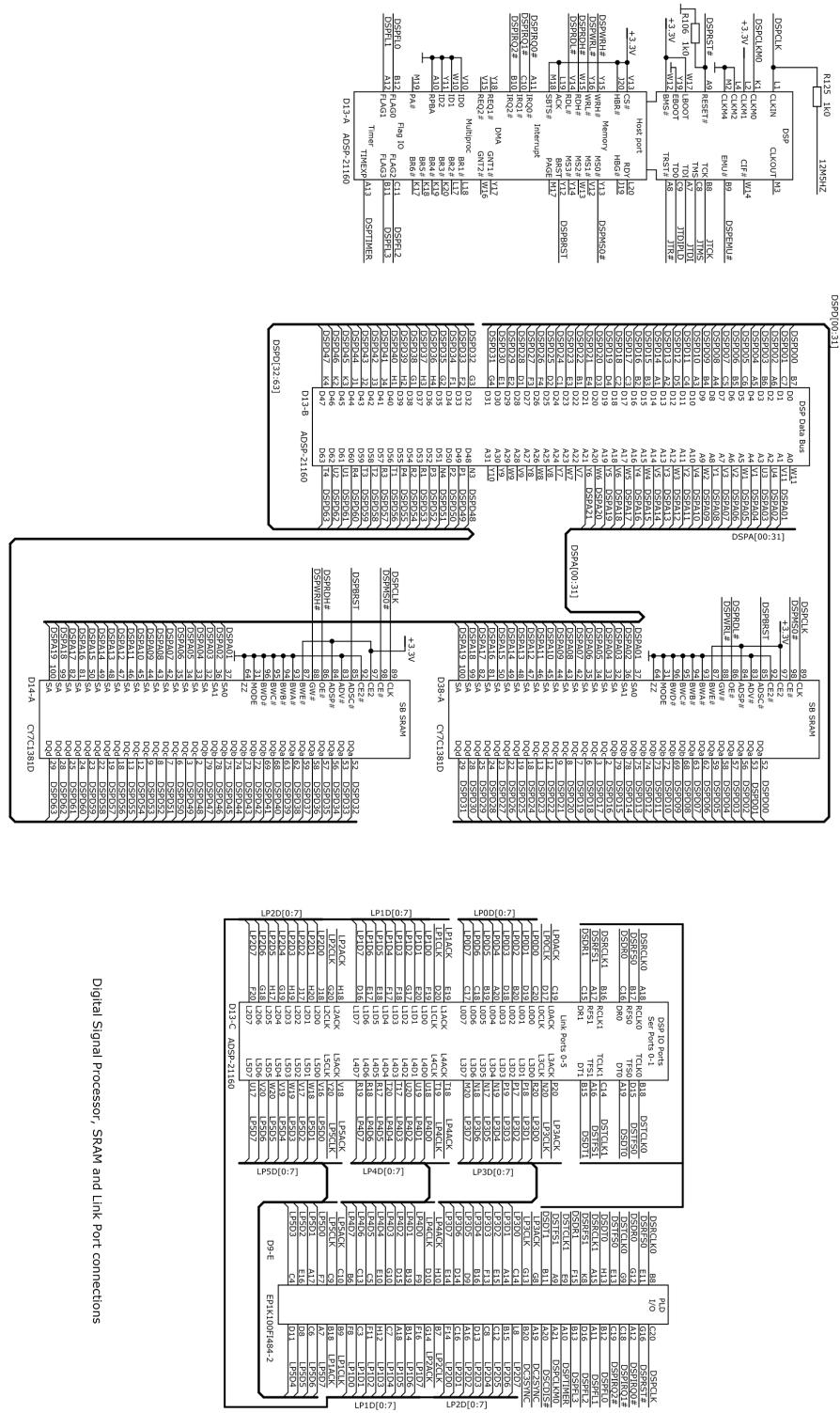


Figure 26 MRP121A Circuit Diagram, 2/7

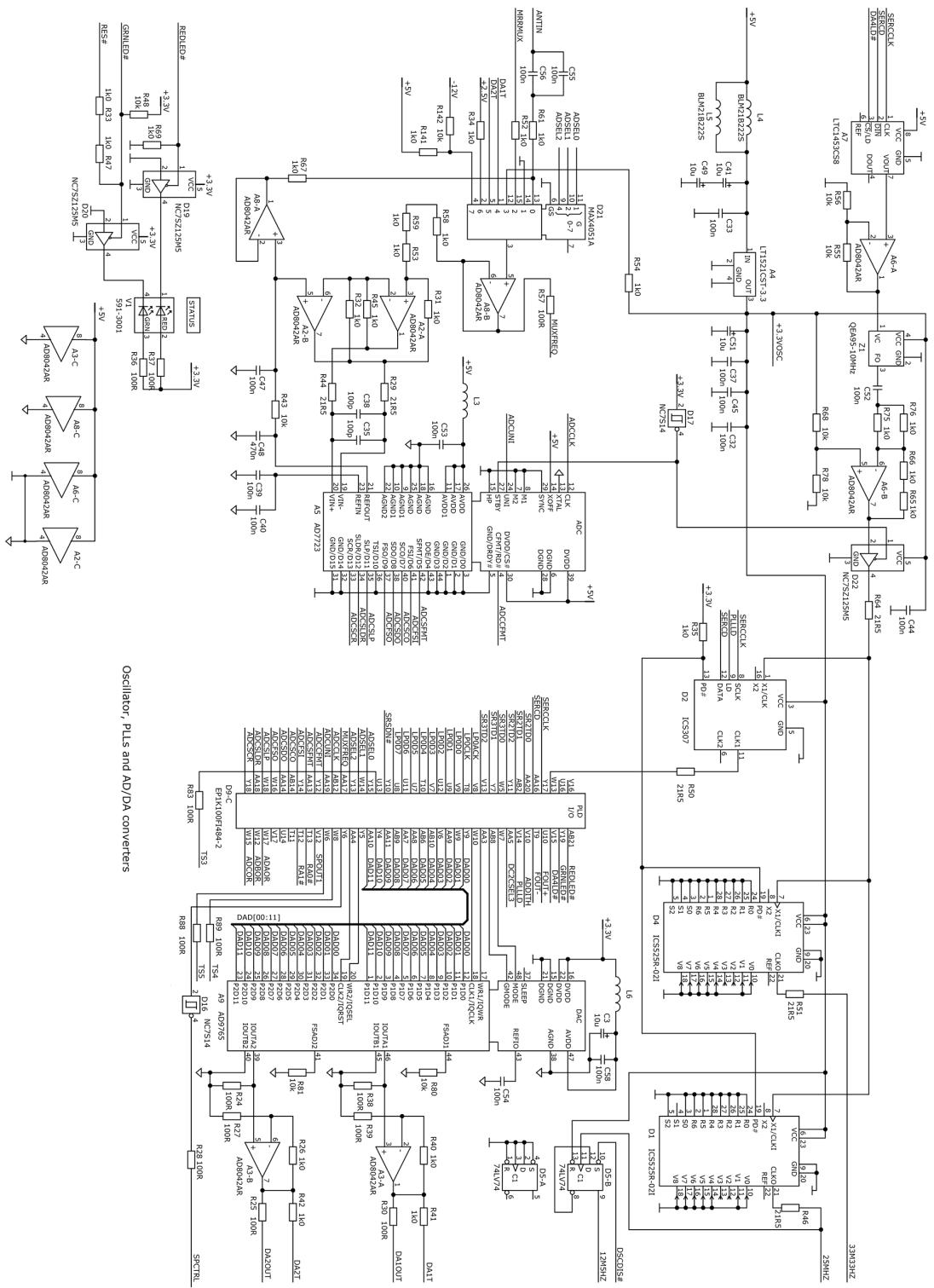


Figure 27 MRP121A Circuit Diagram, 3/7

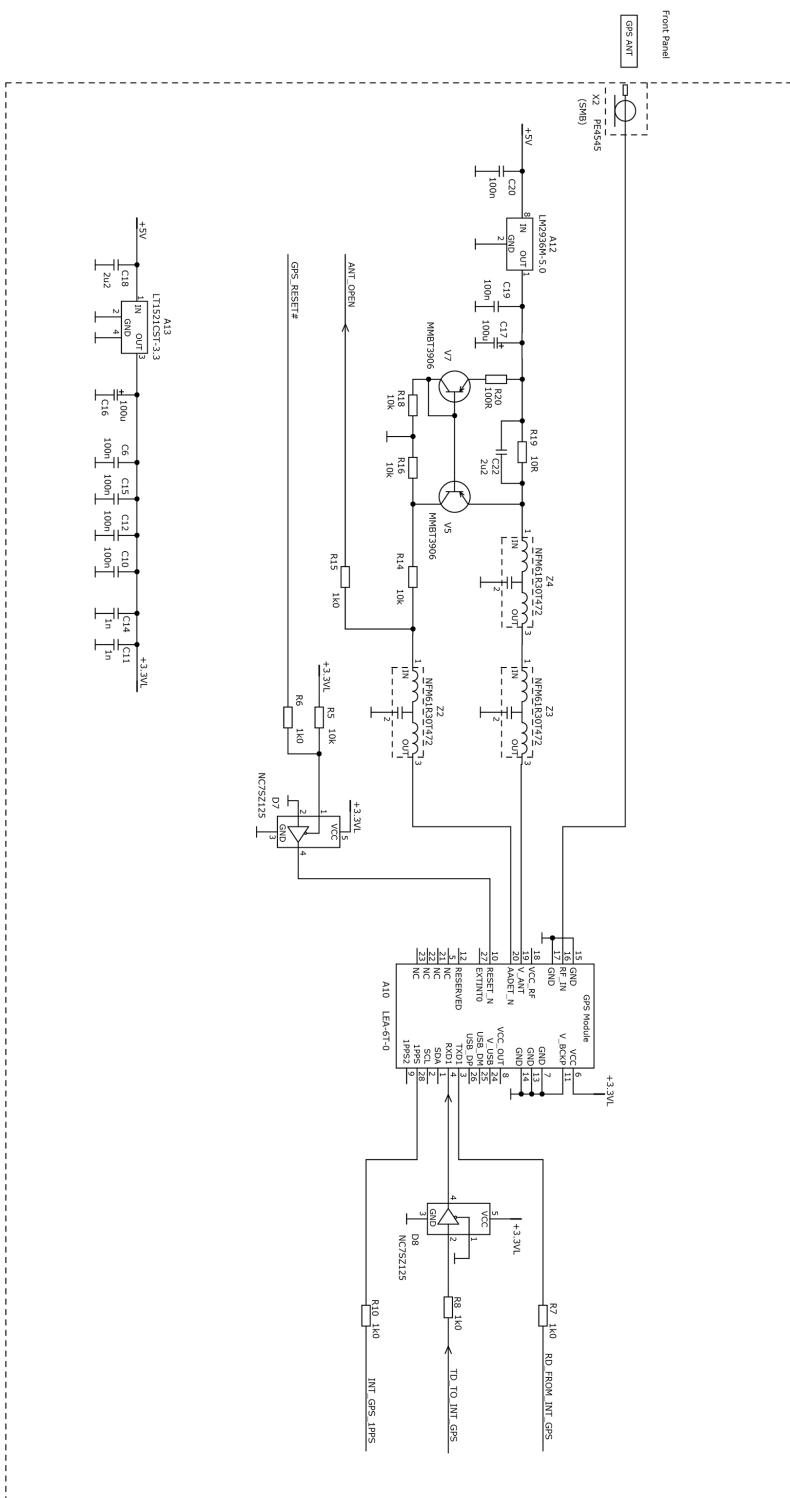


Figure 28 MRP121A Circuit Diagram, 4/7

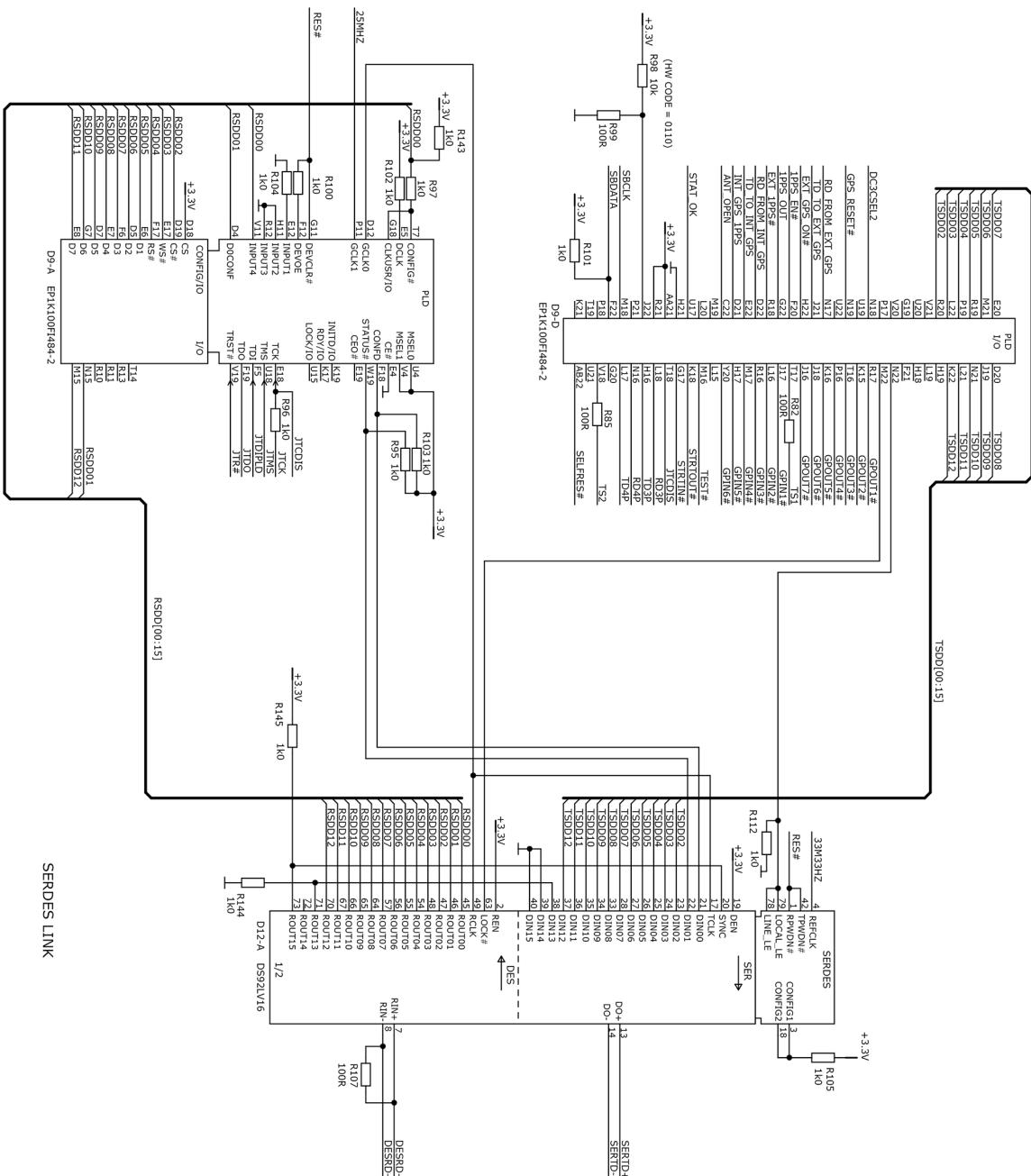
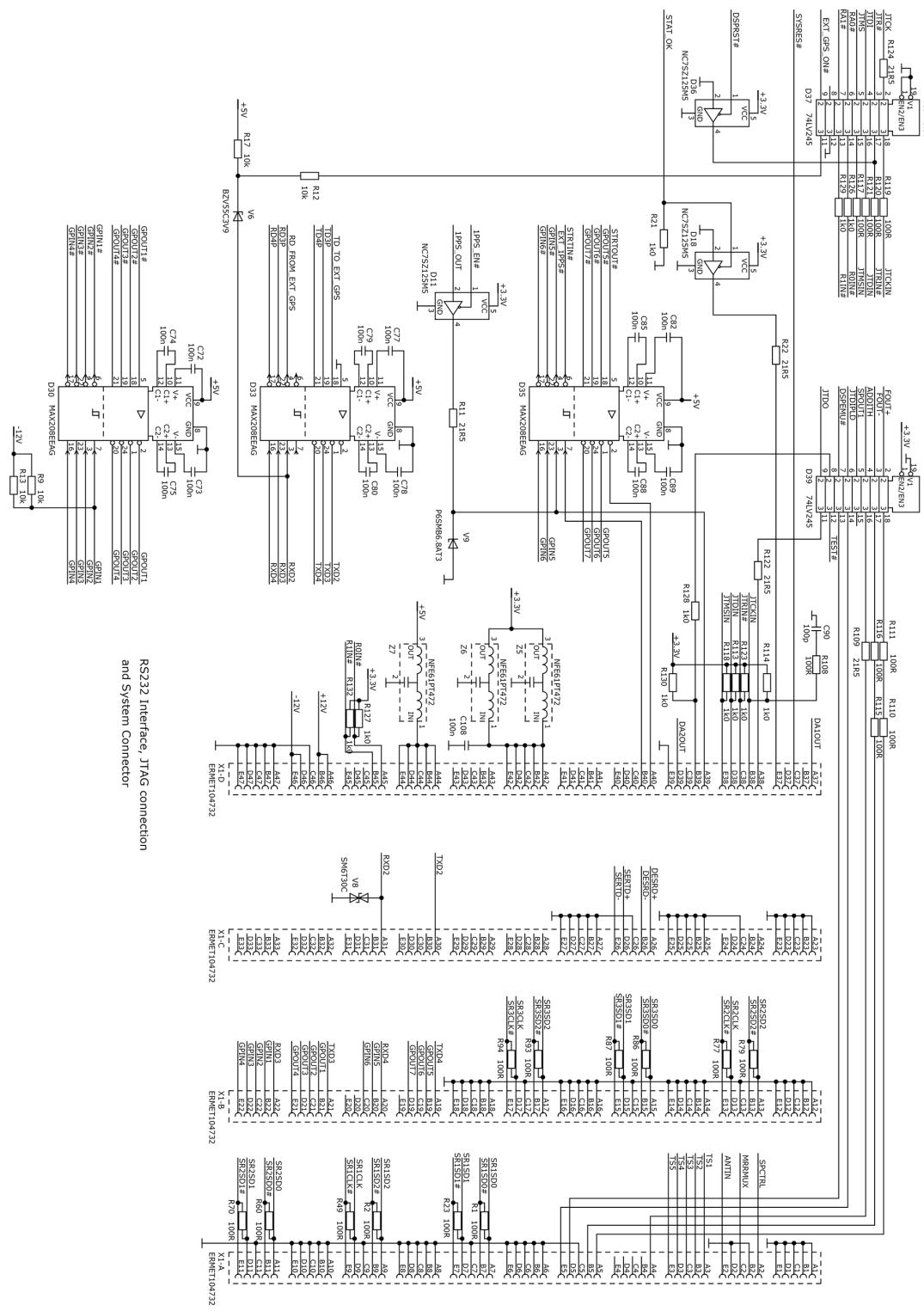


Figure 29 MRP121A Circuit Diagram, 5/7



RS232 Interface, JTAG connection
and System Connector

Figure 30 MRP121A Circuit Diagram, 6/7

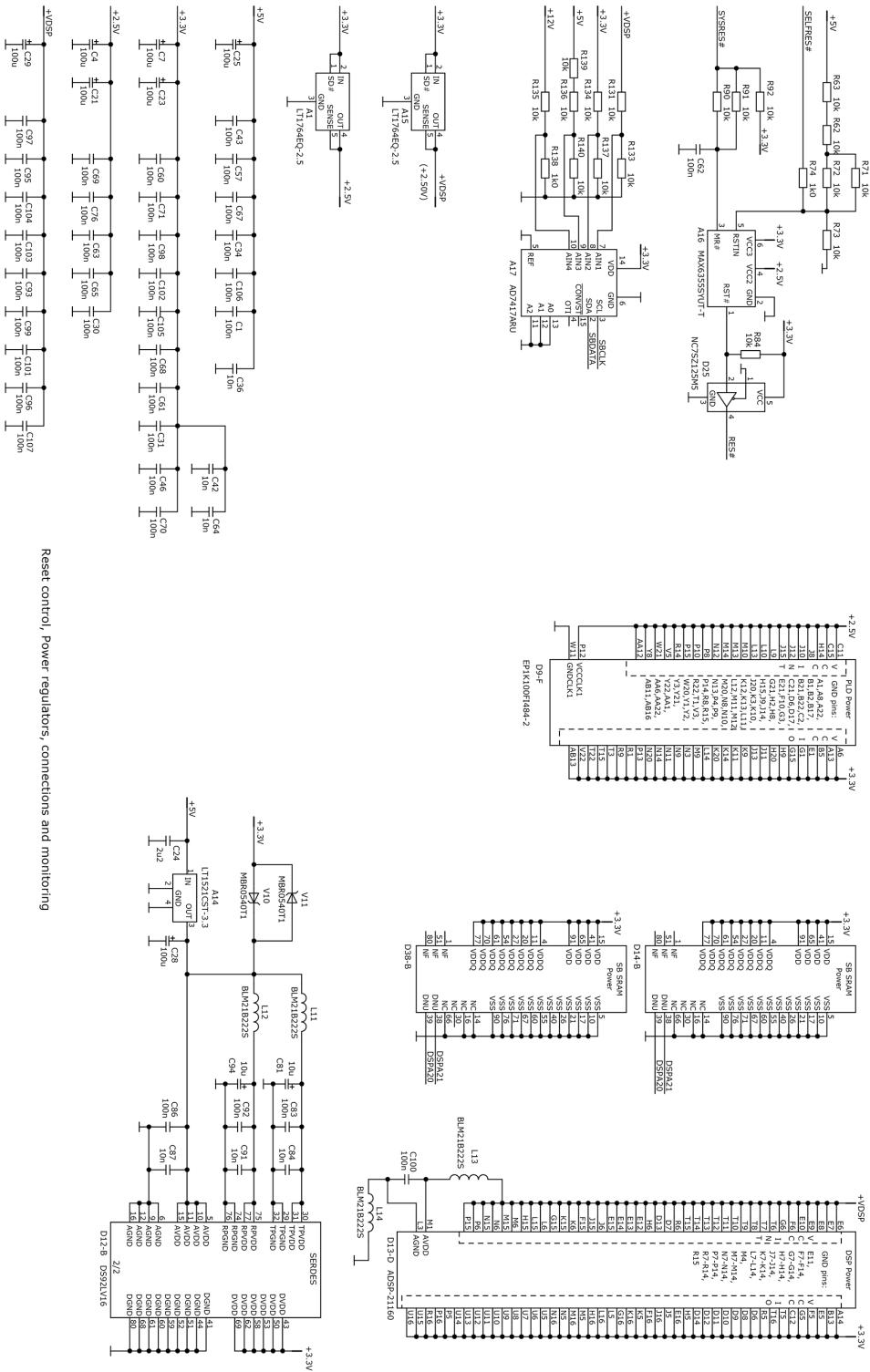


Figure 31 MRP121A Circuit Diagram, 7/7

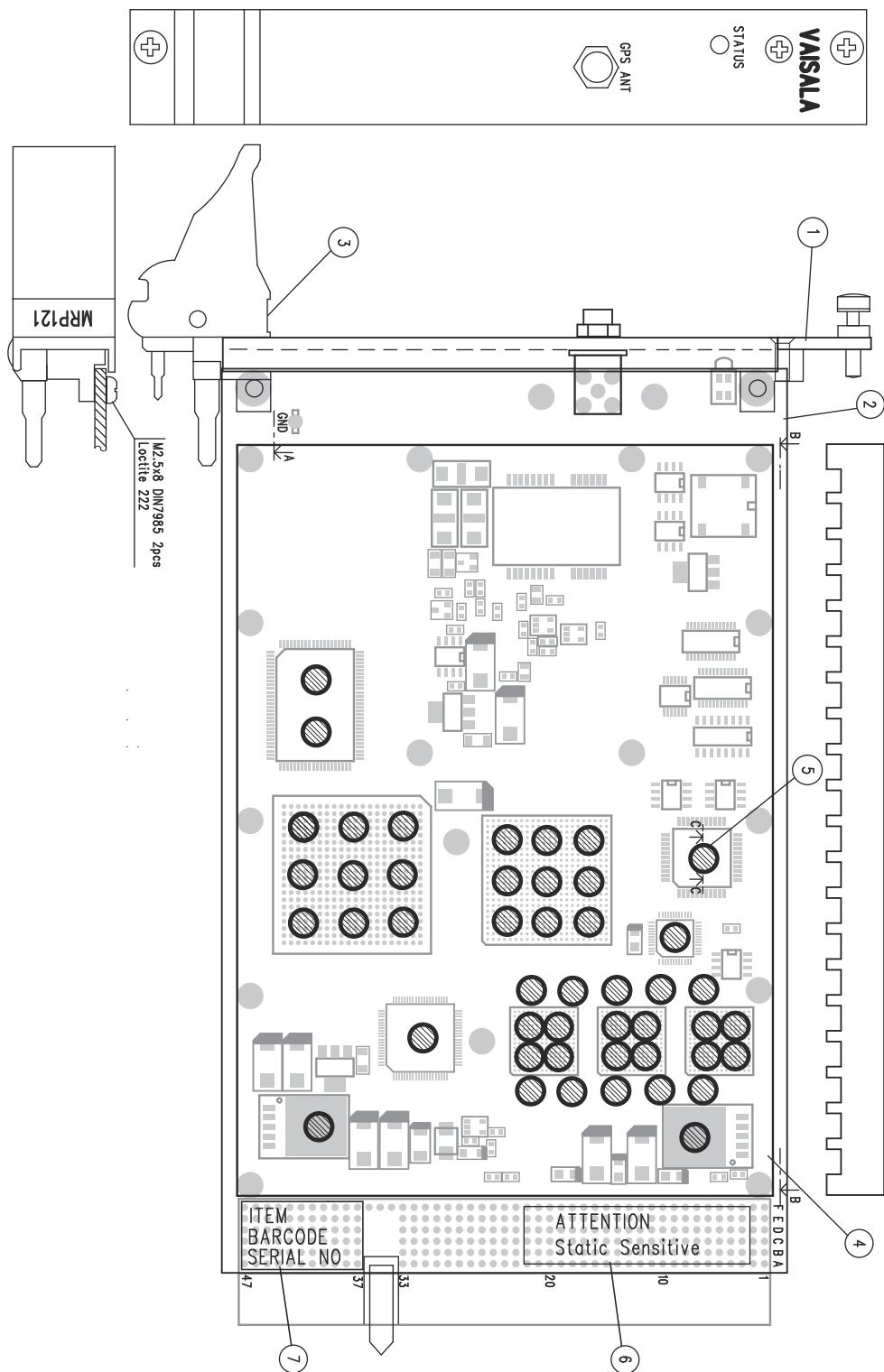


Figure 32 MRP121A Assembly Drawing, 1/2

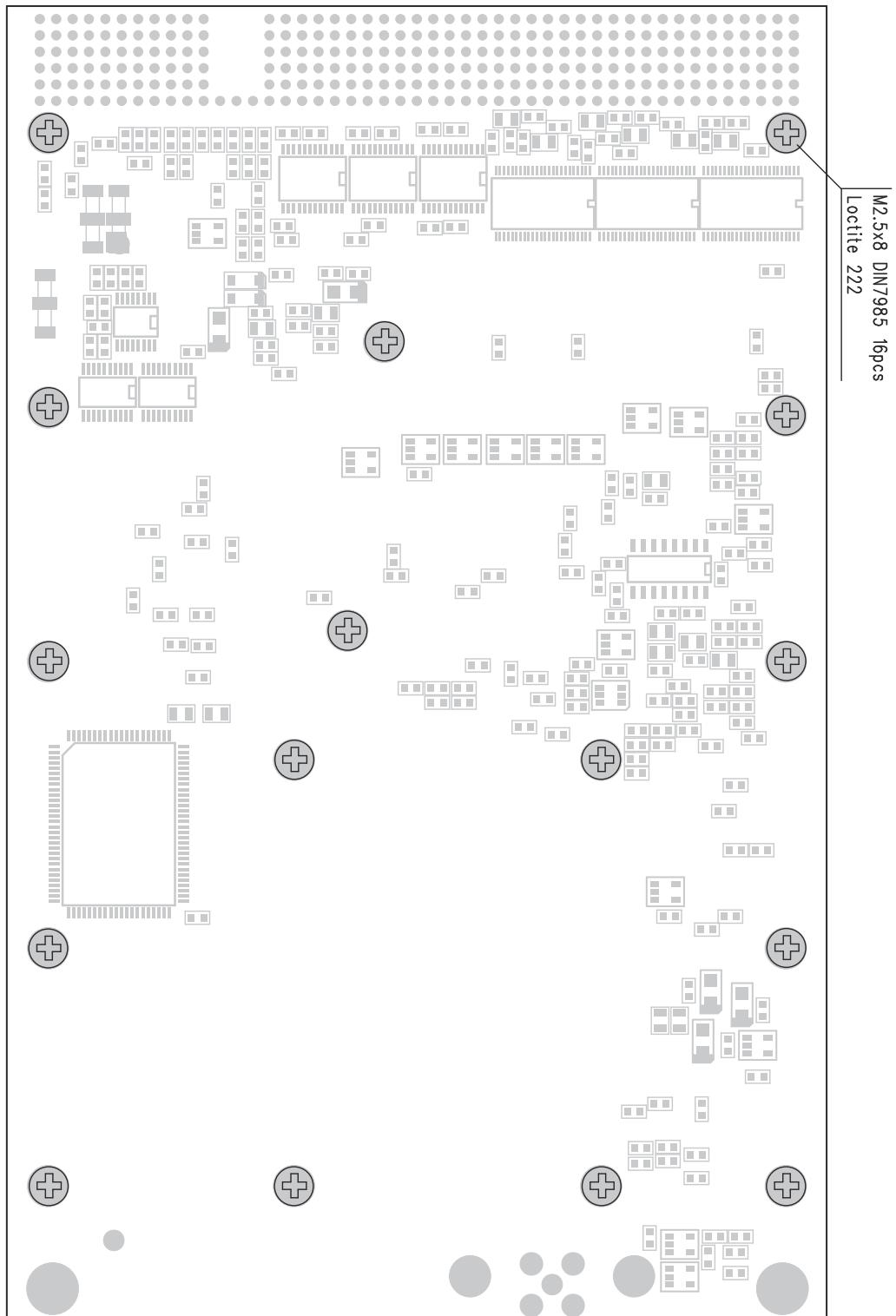


Figure 33 MRP121A Assembly Drawing, 2/2

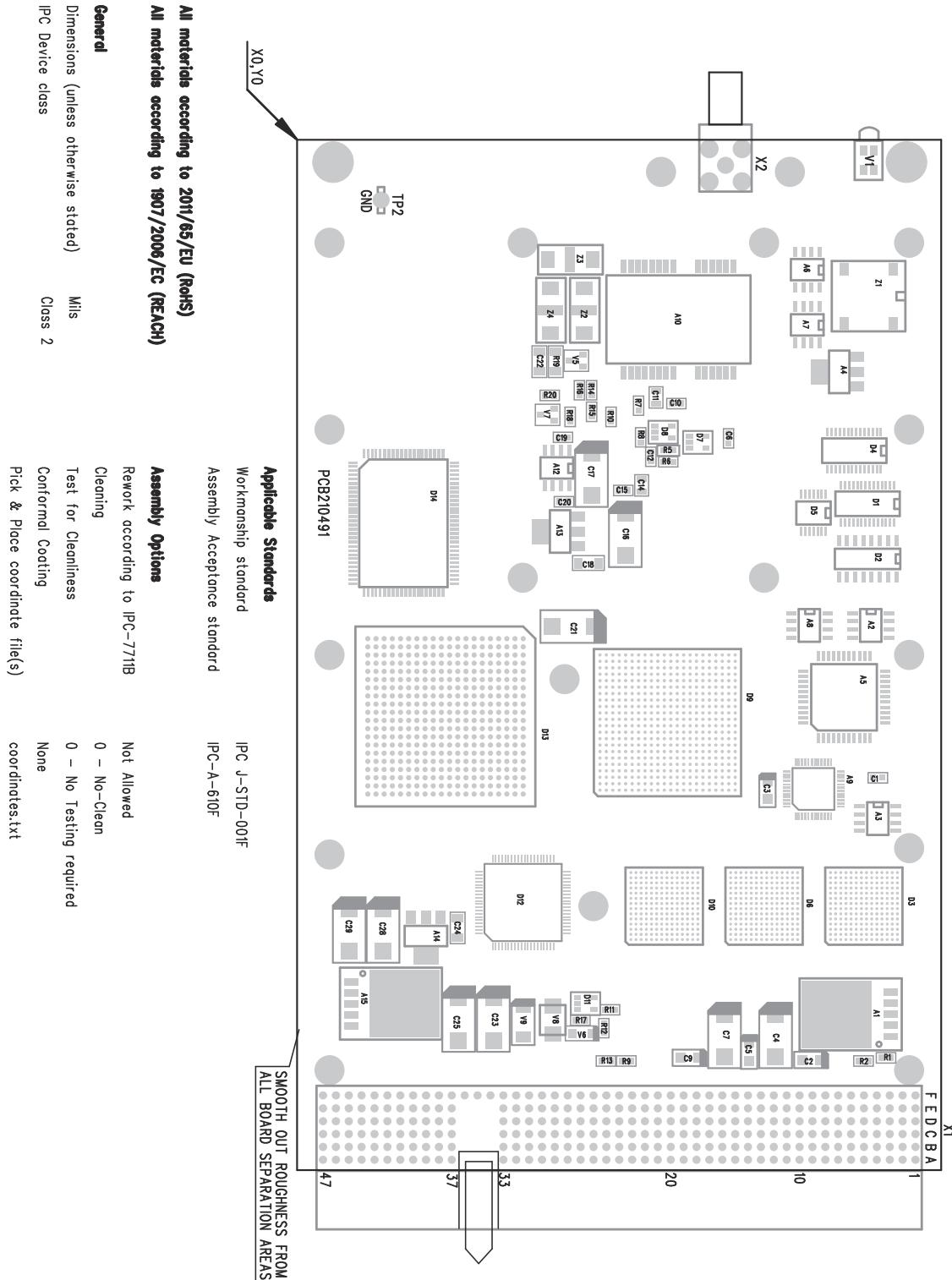


Figure 34 MRP121A Components Layout, 1/2

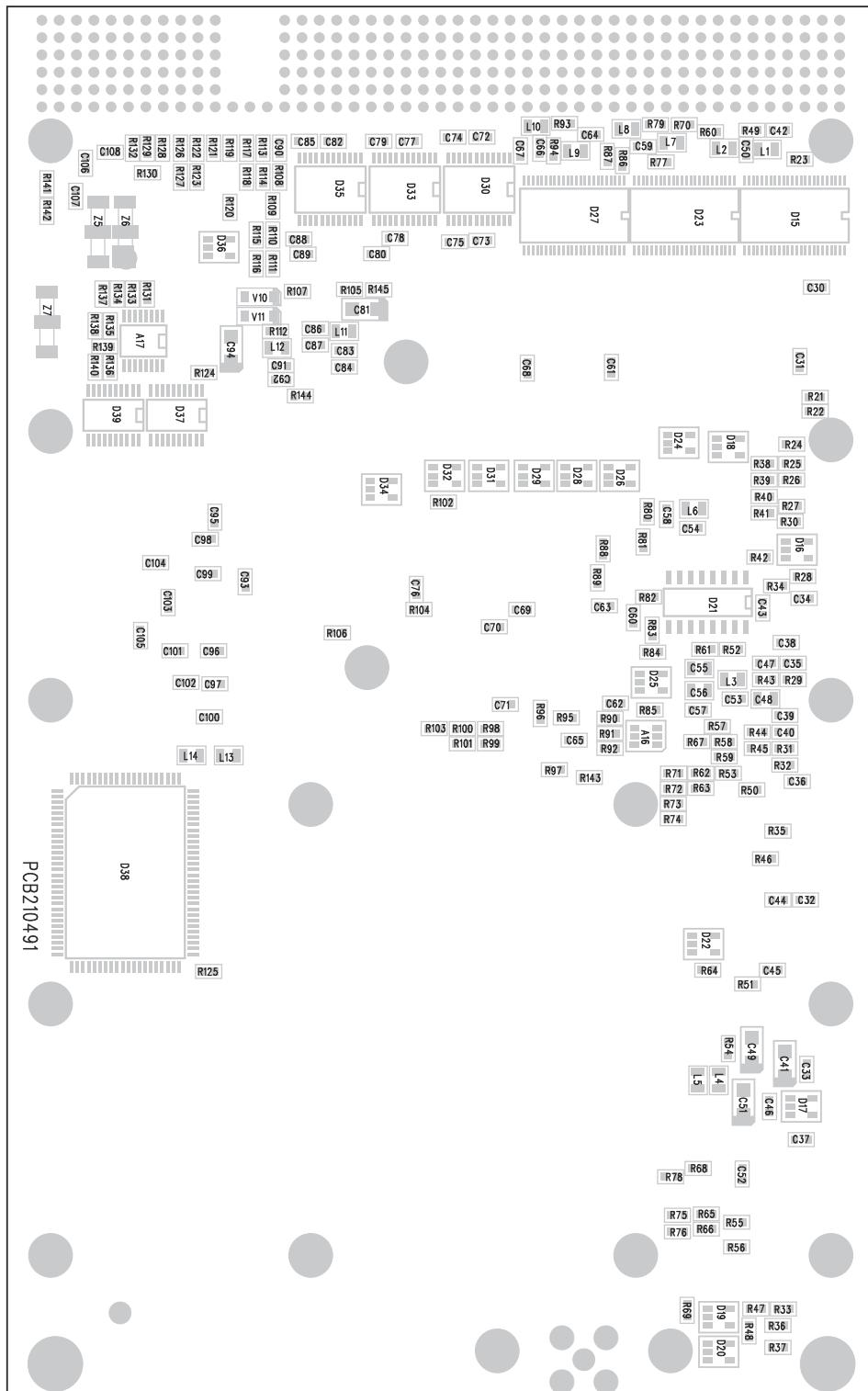


Figure 35 MRP121A Components Layout, 2/2

4.3 Main Processor Unit MPU121A

4.3.1 Introduction to MPU121A

MPU121A is a computer unit intended for system control functions and external communication in Vaisala sounding equipment. It comprises an E1-sized main circuit board and a computer module, which is installed on the main board.



Figure 36 Main Processor Unit MPU121A

The computer module is a COM Express type commercial unit. It contains a PC-compatible CPU with memory and basic PC interfaces. All external power and signal connections are carried out via main board connections.

The main board 254667 contains an Ethernet switch, a solid-state drive memory, a Field Programmable Gate Array (FPGA) with six serial communication channels, Serdes interface, ARCNET type local area network, audio CODEC, and a battery for the calendar clock.

Ethernet switch is an integrated five-channel device. One channel is connected to the computer module and four channels are available for external connections at 10 or 100 Mbits/s line speeds.

The solid-state drive memory is a 64-Gbyte serial ATA (SATA) compatible single chip device.

All timing and interface logic functions are implemented in FPGA. The configuration code of the FPGA is stored in the solid-state drive memory, and the configuration takes place during system startup.

Serdes interface connects LPC bus and a few special signals between MPU121A and an external DSP unit of the software radio system.

Five serial communication channels are available for external communication. One channel is used internally for GPS receiver connection.

Mechanically MPU121A consists of three main parts: components board 254667, computer module and cooling plate installation. The cooling plate has contact surfaces for main components of the computer module to effectively cool down components via thin layers of heat transfer material.

ARCNET type local area network is for connecting to other sounding system units.

4.3.2 MPU121A Functional Description

4.3.2.1 Computer Module

The computer module is a COM Express type complete PC-compatible commercial module, which contains the following main parts and interfaces:

- PC-compatible processor
- SO-DIMM type memory module
- Low Pin Count (LPC) bus interface
- Hard disk interface (SATA)
- USB channels
- AC'97 audio
- I2C bus
- VGA display output
- LVDS display output for flat panels
- PCI bus interface

LPC bus is used for system control functions, Serdes interface, serial channels, and ARCNET interface.

Hard disk interface (SATA) connects to the solid-state drive memory in the main board.

USB channels and I2C bus are connected for external use via main board.

AC'97 audio signals are connected to an audio CODEC chip in the main board for speaker and optional line audio connections.

LVDS outputs are used for external display.

PCI bus and ATA interfaces are not used in the main board.

At power-up, the processor starts operation by executing the BIOS code in its internal flash memory. The BIOS code first verifies the correct operation of the main system components and then transfers the further code execution to the SO-DIMM system memory.

After the BIOS phase is complete, the processor boots from SATA solid-state drive memory, loads code to FPGA, and starts the execution of the actual application program.

The main power supply for computer module is the +12 V system voltage. In addition, a +5 V_{stby} is supplied for power control circuits and a +3 V battery voltage is supplied for the real-time clock.

4.3.2.2 Solid-State Drive

The solid-state drive is a serial ATA (SATA) compatible single-chip flash type disk memory. It has a built-in intelligent SATA controller and a built-in embedded flash file system. It is connected in the main board via serial ATA connector and has a capacity of 64 Gbytes.

4.3.2.3 System Logic

The system logic consists of a Complex Programmable Logic Circuit (CPLD) D9 and Field Programmable Gate Array (FPGA) D16. Both devices are in-circuit configurable. The main device is D16, which is used to implement all required custom logic functions. The D9 is used only as a controller in the code-loading phases of the D16, which has volatile code memory.

At the first phase of power-up, the D9 logic forces the D16 to load automatically its initial code from code memory D2. Later, in system power-up, the final code is loaded from system solid-state drive memory by computer module via LPC interface in D9.

4.3.2.4 JTAG Chain

The JTAG chain and signaling is used only in the manufacturing phase to program configuration memory D2 and logic circuit D9. JTAG clock signal JTCK and test mode select signal JTMS are fed in parallel to both devices from an external programming controller.

Serial data signal is daisy-chained via both devices. The input data JTDI first comes to D2, before the chain continues with signal JTDICPLD to the D9 data in, and finally D9 data out JTDO is connected back to the programming controller.

4.3.2.5 Configuration Memory

The configuration memory D2 is for the initial code storing of the FPGA D16. It is programmed during the unit manufacturing phase via a JTAG serial interface. The FPGA code loading cycle takes place at system power-up under the control of CPLD D9.

4.3.2.6 Complex Programmable Logic Circuit (CPLD)

The CPLD is an instant-on, non-volatile programmable logic circuit. It is programmed during unit manufacturing phase via JTAG serial interface.

At power-up, the CPLD first connects the D2 data output (EDATA) to the D16 data input PDOCONF for serial configuration of the D16 to allow the automatic initial code loading from D2 to D16.

For further operation, the D9 contains an LPC interface, through which computer module controls its operation and external interfaces. In the phase that follows, it is used to convert the LPC bus to an 8-bit parallel bus for final code loading of D16. After code load is complete, the computer module starts using direct LPC bus interface in D16, and D9 is not used in further operation.

4.3.2.7 Field Programmable Gate Array (FPGA)

The FPGA D16 is an in-circuit configurable logic device for all main custom logic functions required in MPU121A.

Initial Code Load

The initial code allows the operating system of the computer module to recognize the logic devices in the FPGA.

At power-up, the operation starts with an automatic initial code loading as follows:

- The PMSEL0 and PMSEL1 to D16 are driven low by D9 for operation mode with serial configuration device.
- The EINITCONF from D2 drives PCONFIG to D16 high via D9.
- The EDATA from D2 is connected to PDOCONF via D9 for serial configuration data.
- The PCONF0 from D16 drives ECS low to D2 via D9.
- The D2 drives EOE low and goes through a 200 ms delay.
- The D9 releases EOE when D16 PSTATUS# goes high.
- The configuring operation starts when D9 and D2 are released the EOE to high level.
- The D16 output CONFD goes to high level to indicate properly completed configuration cycle.
- The D16 enters user mode and starts to operate according to the loaded code.

Final Code Load

The code load operation continues with the final code load when the boot sequence of the computer module is completed.

The final code is loaded as follows:

- The programming mode select signals FPGAMSEL0 and FPGAMSEL1 are set to high level to select parallel passive configuration mode in D16.
- The signal PCONFIG# is pulsed low to start configuration.
- The FPGA code is loaded in byte serial format using control signals PLDCS#, IOWR# and IORD#, along with data lines PDOCONF (data bit 0) and SD01 ... SD07 (data bit 7).
- The D16 output CONFD goes to high level to indicate properly completed configuration cycle.

Signal PDOCONF is used for data bit 0 only during configuration. Later in operation signal SD00 is used as data 0.

The main functional blocks of the FPGA D16 are described in the following sections.

LPC Bus Interface Information

The LPC bus is a serial implementation of the old ISA bus. The LPC bus interface handles all local bus references inside the D16 and directs the relevant external references via Serdes link to the DSP unit of the radio receiver.

The LPC bus signals are listed in the following table.

Table 31 **LPC Bus Signals**

Bus signal	Computer module	FPGA	Description
LPCCLK	O	I	Clock signal (33.333 MHz PCI clock)
LPCADO...3	I/O	I/O	Multiplexed command, address, and data
LPCFRAME#	O	I	Cycle start
LPCSERIRQ	I	O	Serialized interrupt (common with PCI bus)

Address Decoders

Address signals of the LPC bus are used to select the desired control functions in the FPGA. The address ranges of different functions are listed in the following table.

Table 32 Address Decoders

Addr. range [hex]	Function
0280-0287	FPGA code load
0288-28F	External FPGA code load
03F8-03FF	UART1 (COM1)
02F8-02FF	UART2 (COM2)
03E8-03EF	UART3 (COM3)
02E8-02EF	UART4 (COM4)
0290-02B7	Internal control operations
02B8-02BF	Reserved area for future use
02C0-02DF	External control operations
02E0-2E7	UART5 (COM5)
02F0-02F7	UART6

Serdes Interface Logic

The Serdes interface connects the FPGA to the data in and data out buses of the Serdes data link D13. Data is transmitted at the rising edge of the TCLK clock and received at the rising edge of the RCLK clock. In normal operation, the LPC bus of the computer module is linked to the Receiver DSP Unit, and in bus-read commands, adequate number of wait cycles are added to comply with the return delay time of the link.

Asynchronous Receivers/Transmitters

Serial asynchronous data receivers and transmitters (UARTS) with programmable baud rate generators are provided for communication channels COM1 ... COM6.

ARCNET Filter

Digital data filter for the incoming serial ARCNET data signal is provided.

Data Output Registers

Control signals for LED lamps and general purpose I/O lines are provided.

4.3.2.8 SERDES Interface

4.3.2.8.1 Introduction to SERDES Interface and DSP

Serdes interface is used in connection with the receiver DSP unit. All code loading, operation control, and data communication with software radio receiver takes place via Serdes interface. The interface has a 16-bit output channel to Receiver DSP Unit and a 16-bit input channel from the Receiver DSP Unit. Both channels are connected serially via balanced differential lines to the corresponding Serdes interface at the external Receiver DSP Unit. In addition to the 16 data bits, two framing bits are included in each serial bit frame.

In operation, the standard word rate is 33.333 MHz, driven by the PCI clock from computer module, and the serial bit rates are 600 Mbits/s in both channels.

4.3.2.8.2 Initialization of SERDES Interface with Receiver DSP

At power-up, the 33.333 MHz clock is supplied to reference clock (REFCLK) and transmit clock (TCLK) of the D13, and the Serdes interface with the Receiver DSP Unit is initialized as follows:

1. D13 transmits a special sync-pattern at FPGA control.
2. Serdes receiver at Receiver DSP Unit gets synchronized to the pattern.
3. Received synchronized clock is supplied to the transmitter at Receiver DSP Unit.
4. Serdes transmitter at Receiver DSP Unit starts sending the sync-pattern to MPU121A.
5. Serdes receiver at MPU121A gets synchronized.
6. FPGA drives DIN15 (D13/40) high to indicate a synchronized loop to the Receiver DSP Unit.
7. Transmitter at Receiver DSP Unit enters normal operating mode.

4.3.2.8.3 Code Load

When operational, the interface is first used in a special mode to load the operating code to the FPGA at the Receiver DSP Unit. In this mode, it connects a 8-bit parallel data, chip select signal, and write strobe from the FPGA in MPU121A to the code load inputs of the FPGA in the Receiver DSP Unit. Code loading is started with low to high transition in CONFIG# signal.

The following table lists signals used in the FPGA code load of the Receiver DSP Unit:

Table 33 Signals used in FPGA code load

Connection	Signal	Description
DIN00	CONFIG#	Configuration start
DIN01	D0	Data 0 in configuration (D9-A/D4)
DIN02	CS#	Chip select
DIN03	WS#	Write strobe
DIN04	RS#	Read strobe (not used)
DIN05	D1	Data 1
DIN06	D2	Data 2
DIN07	D3	Data 3
DIN08	D4	Data 4

Connection	Signal	Description
DIN09	D5	Data 5
DIN10	D6	Data 6
DIN11	D7	Data 7
DIN12	Not used	
ROUT00	CONF#D	Configuration done
ROUT01	STATUS#	Device status
ROUT02..12	Not used	

4.3.2.8.4 LPC Link

In normal operation, the SERDES interface is used to connect the 5-bit LPC bus between the external control processor and MRP121A. In addition to the LPC bus, some data and control signals are connected via the link.

Table 34 (page 92) lists the signals used in the operation mode:

Table 34 Signals Used in Operation Mode

Connection	Signal	Description
RSD00	Not used	Permanent high level
RSD01	Not used	Permanent high level
RSD02	LFRAME#	Indicates start of a new cycle from LPC bus.
RSD03	LAD_IN0	LAD_IN0 ... 3 are multiplexed command, address and Data from LPC bus.
RSD04	LAD_IN1	
RSD05	LAD_IN2	
RSD06	LAD_IN3	
RSD07	TD_TO_GPS	Serial data to GPS receiver
RSD08..12	Not used	Permanent low level
TSD00	CONF#D	Not used. Permanent high level
TSD01	STATUS#	Not used. Permanent high level
TSD02	LAD0	LAD0 ... 3 are read data to the LPC bus. Two time multiplexed 4-bit nibbles are read in a cycle.
TSD03	LAD1	
TSD04	LAD2	
TSD05	LAD3	

Connection	Signal	Description
TSD06	DSP_IRQ	Interrupt request from the DSP
TSD07	RD_FROM_GPS	Serial data from the GPS receiver
TSD08	STRTIN#	Start/event marker signal to MPU
TSD09 ..12	Not used	Permanent low level

4.3.2.9 Ethernet Switch

The Ethernet line from computer module is connected to Ethernet switch D10.

The D10 (KS8995) is a 5-port integrated Ethernet switch. It contains five 10/100 physical layer transceivers and five MAC (Media Access Control) units with an integrated layer 2 switch.

In the circuit diagram, the D10 is divided into three parts: D10-A is for common control and for port 5 connections; D10-B is for port 1 to 4 connections; and part D10-C is for power connections.

Ports 1, 2, 3, and 4 are for external connections. Ports 3 and 4 are connected through transformers T2 and T4 to the front panel connectors ETH1 and ETH2. Ports 1 and 2 are connected via transformers T3 and T5 to the system connector for external use. Port 5 is connected to the Ethernet controller in the computer module.

The operation of each port is identical and includes all standard functions required in Ethernet port connections.

The PLL clock synthesizer in D10 generates 125, 50, 25, and 10 MHz clocks for internal system timing. Internal clocks are generated from an external 25 MHz clock input.

The power connections to the D10 include extensive filtering for the analog supply voltages.

4.3.2.10 USB Ports

The computer module has 8 USB ports, out of which ports 1 ... 4 are connected via main board to the MPU121A system connector, and ports 5 ... 8 are connected to the USB connectors on the front panel.

All ports have +5 V power outputs via power switches in the main board. Power switches include 900 mA short-circuit current limit and thermal protection functions. Maximum continuous load current is 500 mA at each port. Recovery from possible thermal shutdown situation is automatic.

4.3.2.11 ARCNET Line Interface

The ARCNET controller D11 has 8-bit parallel connection and it is connected to computer LPC bus via dedicated interface logic in FPGA. Controller chip is selected with the PCS# line, and its registers are selected for processor access with address lines PA0, PA1, and PA2. The internal 2-Kbyte buffer memory is accessed indirectly through these registers. Read and write control signals PRD# and PWR# determine the data direction in the connection. Interrupt signal PINT# is connected via FPGA D16 to the serialized interrupt system of the LPC bus.

The controller performs all control operations necessary to carry out ARCNET token passing protocol, network configuration, and data transmission.

The computer transmits data by loading the data packed along with its destination node number into the buffer memory of the controller and by issuing a command to enable the transmission.

Timing signal (20 MHz) to D11 comes from oscillator Z6 through PLL clock multiplier D7 and level change buffer D1.

The controller serial data signals ARCTX and ARCRXIN are connected to the network through bidirectional differential Line Transceiver D12. The line is protected against voltage transients by bidirectional transient suppressors.

In the receive mode, the driver section of the transceiver is disabled by the 1-state of the ARCTXEN# output, which is inverted in D16 FPGA and connected to the transceiver pin 3. The receiver section of the transceiver is permanently enabled, and the received data ARCRXINP is connected through D16 to the controller RXIN input. The D16 contains a data filter, which is used to filter out short transient states from the incoming serial data. The filter length is approximately 320 ns.

During the transmit sequence, the controller enables the transmitter by driving pin 3 high, and the inverted transmit data from output pin P1 is driven to the line by the transmitter. The enable signal and the data signal (ARCTXEN# and ARCTX) are connected to the transmitter via FPGA D16.

4.3.2.12 Serial Channels

MPU121A has six serial channels for external serial communication. All channels have RS232-compatible line drivers and receivers. In addition, a differential RS422 type line interface is provided in channel 3.

All channels are using receiver/transmitter circuits in FPGA D16. All channels have their own programmable baud rate generators. For data widths, only two 8-bit modes are supported: 8-bit data with no parity or 7-bit data with even/odd parity. Receivers have 8-byte FIFOs, but FIFO control mode is not supported.

Transmit signals TD1 ... TD6 are driven via line interface circuits D14, D19, D20, and D21 to corresponding RS232 level signals TXD1 ... TXD6. The received line level signals RXD1 ... RXD6 are connected via same interface circuits to logic level input signals RD1 ... RD6.

Channel 3 output is driven parallel in three branches A, B, and C. Corresponding input lines are received as different signals, but are then combined as one signal by OR-ing logic in FPGA.

4.3.2.13 Audio System

The audio system consists of an AC'97-compatible audio codec circuit and an audio amplifier for speaker output.

4.3.2.13.1 Audio Codec

Audio Codec circuit D8 connects to serial AC'97 audio interface signals (ACRES#, ACBITCLK, ACSYNC, ACSDOOUT, ACS DIN) of computer module for PC-compatible audio functions.

Output connection (SNDL, SNDR) and auxiliary input (DA2OUT) connection are for optional external use.

4.3.2.13.2 Audio Amplifier

The amplifier circuit A2 is a fully differential device for speaker output. Input connection converts single-ended signal as differential format and summing resistors are used to add the right and left channel signals together for a single channel audio output to speaker.

Amplifier connection has a fixed voltage gain of 20 dB and the maximum output power to an 8 ohm speaker is 1.5 W.

4.3.2.14 Support Logic

4.3.2.14.1 MPU121A Reset Circuit

The circuit A6 controls the reset signal RES#, which is forced to the active low state if at least one of the following conditions appear:

- +12 V operating voltage falls below +4.5 V
- +3.3 V operating voltage falls below +10.2 V
- optional internal reset line SELFRES# is in 0-state
- external reset line MRES# is in 0-state

The reset output signal is held active typically 180 ms after the reset condition has disappeared.

4.3.2.14.2 MPU121A PLL Clock Multipliers

PLL (Phase Locked Loop) clock multipliers D4 and D7 have 25 MHz input clock from Z6 and are serially programmed at power-up for output frequencies 14.318 MHz and 20 MHz.

4.3.2.14.3 MPU121A Voltage Regulators

Five linear voltage regulators are provided to get all required operating voltages from +3.3 V and +5.0 V system voltages:

- Regulator A8 is for computer module +3.3 V stand-by voltage.
- Regulator A3 is for Ethernet switch D10 +1.8 V core voltage.
- Regulator A7 is for +2.5 V operating voltages.
- Regulator A1 is for clean +3.3 VCLK supply of clock generation circuits.
- Regulator A5 is for clean analog +3.3 VA supply of Serdes interface (D10).

4.3.2.14.4 Battery

The computer module contains real-time clock (RTC) circuitry for continuous time keeping. Battery G1 in the main board is provided to get the required no-break power supply for RTC (+3VRTC). In addition to the battery, the RTC power can also be supplied from two external +3.3 V sources: +3.3 Vstby and +3.3 Vbat. Battery power is not drawn if either one of these external +3.3 V sources is present.

The battery has enough capacity for typically more than 10 years of operation without external power sources.

4.3.2.14.5 MPU121A Hardware Code

The revision of the circuit board is a six-bit code, which is hard-wired at FPGA inputs Y14, Y15, Y17, W14, AB8, and W18 for processor read. The state of the last bit can be changed by resistors R38 and R39, and the upper part of the code is updated when a new revision of the board layout is required.

4.3.2.14.6 MPU121A Rack Code

The rack code signals (RACK0 ... 2) are connected from system connector to FPGA via buffer gates D3, D27, and D31. The code value can be read by processor and depends on connections at external connector. The code can optionally be used to identify the unit or its location.

4.3.2.14.7 MPU121A Test Input

Input signal TESTX# from X1/b39 is connected via D21 to the FPGA for possible future use.

4.3.2.14.8 Status LED Lamp

The status indicator lamp V1 is provided in the front plate. The V1 is a red/green bi-color LED type lamp. The red and green lamps are controlled by signals REDLED# and GRNLED# from the FPGA D16. Yellow color is produced when both lamps are on.

During active system reset (signal RES# = 0), both LEDs in the lamp are lit to show yellow color. After reset, the red lamp remains on during the boot sequence of the CPU module. When booting is complete, the lamp is used to indicate operational state of the unit.

4.3.2.15 Test Program Overview

After the reset, the red LED lamp is on and the processor starts operation by executing the BIOS code in LPC bus flash memory at the computer module. The BIOS code verifies the correct operation of the following system components:

- CPU
- LPC bus and BIOS code flash
- PCI bus and connection to Ethernet controller
- SDRAM system memory
- Solid-state drive

If a fault is detected, the operation is halted and the red LED remains on to indicate the faulty unit.

If correct operation is indicated, the further BIOS code execution is transferred to the SDRAM system memory. The processor boots from onboard SATA solid state drive, loads code to FPGA, changes LED color from red to green, and starts executing the actual application program.

4.3.3 MPU121A Parts List

Table 35 MPU121A Parts List

Code	Part No.	Description	Qty
Special Parts:			
Assembly ref. 001	DRW227305	Heatsink MPU121	1
Assembly ref. 002	220640	Computer Module Conga-B945/L7400	1
Assembly ref. 003	220685	Round Sleeve Spacer D5 d2.7 L8 PA, 5.82.080	5
Assembly ref. 004	254667	Components Board Main Processor Unit	1

Code	Part No.	Description	Qty
Assembly ref. 005	220669	Memory Module SODIMM DDR2, 1GB	1
Assembly ref. 006	10948	Marking Sticker OK46546	1
Assembly ref. 007	254273	License Sticker Win 10 IoT Ent LTSB MultiLang ESD OEI Entry	1
Assembly ref. 008	15223	Sticker Set Matt White, Polyethylene	1
Assembly ref. 009	220714	Therm. Conductive Liquid Gap Filler 3500S35, 50CC. Diameter 5 x 2 mm, bonds 3 pcs. Use bergquist applicator gun and 32 element mixing nozzle.	0.01
Assembly ref. 010	16166	Plastic Label 1180, 65+3mm. Text: MPU121A, printed with label printer. Document DRW214831.	0.005
Assembly ref. 011	DRW217261	Front Panel Assembly MPU121	1
Assembly ref. 001 (at 254667)	246411	SATA Flash Drive DESSF-64GD09BWADCF	1
Integrated Circuits:			
A1, 5, 8	25757	IC, Voltage Reg SOT-223, 3.3V/300mA	3
A2	217312	IC, Audio Amplifier TPA6211A1DRB	1
A3	218139	IC, Voltage Regulator 1.25-9V, 500mA, SOT-223	1
A4,9	212850	IC, Power Switch TPS2054AD	2
A6	010148	IC, Supervisor MAX6355SYUT-T	1
A7	27139	IC, Voltage Regulator 2.5 V / 3 A, TO263-5	1
D1, 5, 6, 22-25, 28-30	26570	IC, Buffer Tiny NC7SZ125M5X_NL	10
D2	26149	IC, Config. Memory EPC2TI32 (SMD)	1
D3, 26, 27, 31	19568	IC, Inverter Tiny NC7S14, SOT23-5	4
D4, 7	210412	IC, Freq. Synthesizer ICS307M-02I	2
D8	217320	IC, Ac'97 Audio Codec ALC850-LF	1
D9	217031	IC, CPLD EPM570F256I5N	1
D10	213990	IC, Ethernet Switch KSZ8995MAI	1
D11	16632	IC, Controller COM20020 ILJP (SMD)	1
D12	16732	IC, Bus Transceiver DIFF. BUS TRX SO-8 I	1
D13	219689	IC, Lvds Serdes DS92LV16	1
D14, 20, 21	26108	IC, Rs232c Transceiver MAX208EEAG	3
D16	27133	IC, Sram Based Pld EP1K100FI484-2	1
D17, 19	25703	IC, Rs485 MAX3085CSA, SO-8	2
Transistors and Diodes:			

Code	Part No.	Description	Qty
V1	010192	Diode, Led 591-3001, Red and Green	1
V2, 5, 30, 33	212869	Diode, Eds Suppressor PGB0040805NR	4
V3, 4, 7, 8, 16, 31, 32, 34, 35	17332	Diode, Transil 6.8V 57.A	9
V6, 9, 25-29	210575	Diode, TVS-Array SMDA03LCC-LF	7
V10-12	15976	Diode, Silicon Ex LL4148/ PMLL4148 (SMD)	3
V13, 21-24	18091	Diode, Transil 12V 600W/1ms +-5%	5
V14, 15, 17, 18	17341	Diode, Silicon Si 200V 2A 25ns	4
V19, 20	16004	Diode, Schottky Ex MBR0540T1G	2
Resistors:			
R1, 9, 51, 53, 62, 79, 80, 111, 114, 115	010014	Resistor, Chip 21R5 1% 100ppm 0603	10
R2, 3, 27, 29, 39, 49, 50, 52, 56, 57, 70-74, 100-102, 108, 109, 117, 118, 121-124	25262	Resistor, Chip 10KO 1.0% 100ppm 0603	26
R4, 21, 24-26, 31, 33-36, 40, 41, 46, 54, 55, 81, 82, 87, 90, 91, 95, 103, 104, 110, 112, 113, 116, 119, 120	25263	Resistor, Chip 1KO 1.0% 100ppm 0603	29
R5, 6, 68, 69	26132	Resistor, Chip 3k65 1.0% 100ppm 0603	4
R7	26097	Resistor, Chip 0R0 (jumper) 0603	1
R8, 14-20, 22, 23, 28, 30, 38, 42-45, 64, 66, 67, 76-78, 83-86, 88, 89, 93, 94, 96-99, 105, 106	26100	Resistor, Chip 100R 1.0% 100ppm 0603	37
R12, 13, 47	25217	Resistor, Chip 68KO 1.0% 100ppm 0603	3
R32, 48, 63, 65, 92, 107	25452	Resistor, Chip 2k74 1.0% 100ppm 0603	6
R59-61	18024S	Resistor, Chip 150R 5% 200ppm 0805	3
R75	25214	Resistor, Chip 4K64 1.0% 100ppm 0603	1
Capacitors:			
C1, 2, 92-95, 109, 111	25969	Cap., Chip Ceramic 12p 5% NPO 50V 0603	8
C3, 5, 6, 8, 10, 11, 23, 27, 28, 31-35, 37, 40, 41, 43-45, 47, 48, 50, 53, 54, 57, 60, 62, 66, 67, 69-71, 73-85, 101, 103, 105, 113, 115, 117, 119, 121, 124, 128, 134-136, 138, 139, 142, 143, 146, 147	217765	Cap., Chip Ceramic 100nF 10% X7R 25V 0603	65
C4, 9, 12, 97, 98, 116	213390	Cap., Chip Ceramic 1u 15% X7R 1206 50V	6
C7, 17-19, 87-91, 131	217767	Cap., Chip Tantalum 100uF 10% 16V Case D	10
C13, 21, 22, 30, 39, 42, 46, 49, 55, 56, 59, 72, 107, 118, 120, 123, 125, 126, 132, 133	19405	Cap., Chip Ceramic 10n 10% X7R 50V 0603	20

Code	Part No.	Description	Qty
C15, 16, 24, 25, 127, 130, 137, 140, 141, 144, 148-151, 153, 154	217766	Cap., Chip Tantalum 47uF 10% 25V Case D	16
C14, 26, 29, 36, 51, 52, 58, 96, 104, 106, 129, 145, 152	19959	Cap., Chip Tantalum 10uF 10V 20% Case A	13
C38, 61, 114, 122	27410	Cap., Chip Ceramic 1nF 10% X7R 2kV 1808	4
C99, 100, 102, 108, 110, 112	27098	Cap., Chip Ceramic 470p 5% NPO 50V 0603	6
Connectors:			
T1-5	27130	Transformer, Pulse LAN Transf.10/100Mbps	5
TP1	0172	Connector Pin Ex E03096L02	1
X1	210249	Connector, 2mm Metric	1
X2, 3	27134	Connector, Modular, RJ45 8S, PCB, SMD	2
X4, 5	211651	Connector, USB A Dual	2
X8	224581	Connector, Serial ATA, 7Circuits,1R,1.27Pitch	1
X6, 7	217293	Connector, PCB, SMD X6,7	2
Other Components:			
G1	251417	Battery, Lithium 3V 950mAh, Encapsulated	1
L1, 12, 14	18936	Ferrite Bead Inductor 120ohm @100MHz 0R15	3
L2-8, 13	25097	Ferrite Bead Inductor Ex 2250ohm @100MHz, 0R8	8
L9-11	18758	Ferrite Bead Inductor 200ohm @100MHz, 0R35	3
Z1-5, 7	25036	Filter, Emi (Smd) NFE61PT472C1H9L	6
Z6	210863	Oscillator, Crystal 25.000 MHz, SMD	1
Miscellaneous:			
	PCB210858	Printed Circuit Board 254667	1
	211284	SYMANTEC Ghost License VAR Corporate. Will be needed in application software loading.	1
Assembly ref. 002 (at 254667)	254681	Spacer, Hex Tapped M3 x 13, SW5.5, 5.03.123	1
	211738	Screw, Crosshead M2,5x6 DIN7985 PZ A4	6
	220696	Screw, Crosshead M2,5x10 DIN966 PZ A4	3
	25682	Screw, Crosshead M2,5x16 DIN7985 PZ A4	5
	6779	Nut, Hex M2,5 DIN934 A4	3
	7067	Washer, Spring Lock B2,5 DIN127 A4	14
	213988	Front Panel, Shielded 3U,14HP,Scroff 20848-013	1
	210854	Emc Gasket 3U, Schröff 21101-854	1
	210853	Injector/Ejector Handle 4HP,IEL,Schroff20817-613	1

Code	Part No.	Description	Qty
	210856	Board Holder Schroff	1
	210855	Sleeve M2.5x3,Schroff 21100-660	4
	210857	Collar Screw M2.5x12.3,Schroff	5
	212049	Screw, Crosshead M2,5x8 DIN966 PZ A4	1
	212048	Screw, Crosshead M2,5x8 DIN7985 PZ A4	1
	18832	Screw, Crosshead M3x6 DIN7985 PZ A4	2
	3939	Washer, Spring Lock B3 DIN127 A4	2
	5068	Screw-Lock Compound Loctite 222	0.001

4.3.4 MPU121A Technical Data

Table 36 MPU121A Computer Module

Computer Module	
Module type	COM Express
Processor type	Core 2 Duo
Clock speed	1.5 GHz
Dynamic RAM	DDR2 SO-DIMM

Table 37 MPU121A Solid-State Drive

Solid-State Drive	
Type	Solid-state drive
Interface	SATA
Capacity	64 Gbyte

Table 38 MPU121A Ethernet

Ethernet	
Type	10/ 100 Fast Ethernet
Number of controllers	1
Number of external channels	4

Table 39 MPU121A USB

USB	
Type	USB 1.0/ 2.0

USB	
Number of channels	8
Power output	+5V, 500mA (each channel)

Table 40 MPU121A Serial Lines

Serial Lines	
Line types	5 lines RS232-C 1 line RS422 / RS232-C
Baud rates	50 - 19200
Data types	8 bit, no parity 7 bit, even/odd parity

Table 41 MPU121A Serdes Link

Serdes Link	
Channels	Input/ Output
Word length	16-bit
Word rate	33.333 Mwords/s
Serial bit rate	600 Mbits/s

Table 42 MPU121A Power Requirements

Power Requirements (Typical)	
+3.3 V	500 mA
+5.0 V	500 mA
+12 V	2 A
+5 Vstby	150 mA

Table 43 MPU121A General Technical Data

General	
Operating temperature	-20+70 °C (frame temperature) ¹⁾
Storage temperature	-55 ... +75 °C
Unit type	E1-size module
Dimensions	125(H), 40(D), 180(L) mm
Weight	630 g
System connector	220-pin female
Status indicators	LED lamp

1) Frame temperature is a surface temperature at the contact area of an external cooling frame.

4.3.5 MPU121A Signals

Table 44 MPU121A Signal Names and Abbreviations

+1.8V	+1.8 V operating voltage
+12V	+12 V operating voltage
+2.5V	+2.5 V operating voltage
+2.5VA	+2.5 V analog operating voltage
+3.3V	+3.3 V operating voltage
+3.3VA	+3.3 V analog operating voltage
+3.3VBAT	+3.3 V from battery
+3.3VCLK	+3.3 V for clock oscillator
+3.3VSTBY	+3.3 V standby voltage
+3VRTC	+3 V for real-time clock
+5V	+5.0 V operating voltage
+5VSTBY	+5 V standby voltage
+5VUSB1...8	+5 V USB for port 1...8
+VE5CT	Center tab voltage for channel 5 Ethernet transformer
100LNK	100 Mbit link
10LNK	10 Mbit link
14.318MHZ	14.318 MHz clock signal
20MHZ	20 MHz clock signal
25MHZ	25 MHz clock signal
ACBITCLK	Audio codec bit clock
ACRES#	Audio codec reset
ACSDIN	Audio codec serial data in
ACSDOUT	Audio codec serial data out
ACSYNC	Audio codec sample sync
AGND	Analog ground
ARC+	Non-inverted ARCNET line
ARC-	Inverted ARCNET line
ARCRXIN	Received ARCNET data
ARCRXINP	Received ARCNET data
ARCTX	Transmitted ARCNET data
ARCTXEN#	ARCNET transmitter enable

ARCTXENP	ARCNET transmitter enable
ARCTXP	Transmitted ARCNET data
CBRES#	Carrier board reset
CPLD	Complex programmable logic circuit
CPUPON	CPU power on
CPUPON#	CPU power on inverted
CPURES#	CPU reset
CTS2	Clear to send 2
CTS2#	Clear to send 2 inverted
DA2OUT	Digital to analog converter 2 output
DEN	Data enable
DIN00...15	Data in 00...15
DMA	Direct memory access
DO+	Data out +
DO-	Data out -
DSR2	Data set ready
DSR2#	Data set ready inverted
DTR2	Data terminal ready
DTR2#	Data terminal ready inverted
E1...5RD+	Ethernet channel 1...5 received data+
E1...5RD-	Ethernet channel 1...5 received data-
E1...5RX+	Ethernet channel 1...5 receive signal+
E1...5RX-	Ethernet channel 1...5 receive signal-
E1...5TD+	Ethernet channel 1...5 transmitted data+
E1...5TD-	Ethernet channel 1...5 transmitted data-
E1...5TX+	Ethernet channel 1...5 transmit signal+
E1...5TX-	Ethernet channel 1...5 transmit signal-
ECS	Configuration memory chip select
EDATA	Configuration memory data
EDCLK	Configuration memory data clock
EINITCONF	Configuration memory initiate configuration
EOE	Configuration memory output enable
ESRES#	Ethernet switch reset
FPGA	Field programmable gate array

FULLDPX	Full duplex
GIO1...8	General-purpose I/O line 1...8
GND	Ground
GRNLED#	Green LED control
GRNLEDT	Green LED test
I2C	I2C (Inter-IC) bus
I2CSCL	I2C serial clock
I2CSDA	I2C serial data
INA3C	Input A channel 3 C
IORD#	I/O bus read
IOWR#	I/O bus write
IP1...2	Input 1...2
IPX1...2	Received input 1...2
JTAG	Joint test action group
JTCK	JTAG test clock in
JTCKIN	JTAG test clock input
JTDI	JTAG test data in
JTDICPLD	JTAG test data input
JTDIN	JTAG test data out
JTDO	JTAG test data output
JTDOUT	JTAG test data output from resistor
JTMS	JTAG test mode select
JTMSIN	JTAG test mode input
LINELE	Line loopback enable
LOCALLE	Local loopback enable
LOCK#	Locked
LPC	Low pin count bus
LPCADO...3	LPC address/data 0...3
LPCCLK	LPC clock
LPCDRQ0#	LPC DMA request 0...1
LPCFRAME#	LPC frame
LPCSERIRQ	LPC serialized interrupt request
LVDS	Low voltage digital signal
LVDSA0...3+	LVDS channel A output 0...3 non-inverted

LVDSA0...3-	LVDS channel A output 0...3 inverted
LVDSACLK+	LVDS channel A clock non-inverted
LVDSACLK-	LVDS channel A clock inverted
MDIXDIS	Disable auto cross-over
MRES#	Module reset input
OC1...8#	Over current 1...8
OC12#	Over current 1 or 2
OC34#	Over current 3 or 4
OC56#	Over current 5 or 6
OC78#	Over current 7 or 8
OP1...2	Output 1...2
OPX1...2	Transmitted output 1...2
OUTA...E3C	Output A...E channel 3 C
PA0...2	Peripheral address 0...2
PAD0...7	Peripheral address/data 0...7
PLD	Programmable logic device
PCONF D	PLD configuring done
PCONFIG#	PLD configuring start
PCS#	Peripheral chip select
PDOCONF	PLD data 0 in configuring
PDCLK	PLD data clock
PINT#	Peripheral interrupt
PLDCS#	PLD chip select
PLL	Phase locked loop
PLL DATA	PLL data
PLL D1...2	PLL load 1...2
PLL SCLK	PLL serial clock
PMSEL 0...1	PLD mode select
PRD#	Peripheral read
PRES#	Peripheral reset
PSTATUS#	PLD status
PTOGGLE#	Power toggle
PTOGGLE 1...2#	Power toggle 1...2
PWR#	Peripheral write

RACK0...2	Rack code 0...2
RACK0...2#	Rack code 0...2 inverted
RCLK	Receiver clock
RD1...2	Received data 1...2
RD3A...C	Received data 3 A...C
RD4...6	Received data 4...6
REDLED#	Red LED control
REDLEDT	Red LED test
REFCLK	Reference clock
REN	Receiver enable
RES#	Reset
RIN+	Receiver input non-inverted
RIN-	Receiver input inverted
ROUT00..15	Receiver data out 0...15
RPWDN#	Receiver power down
RTS2	Request to send
RTS2#	Request to send inverted
RXD1	Received serial data 1...6
RXD2 2	Received serial data
RXD3A	Received serial data 3 A
RXD3B	Received serial data 3 B
RXD3C+	Received serial data 3 C non-inverted
RXD3C-	Received serial data 3 C inverted
SATA	Serial Advanced Technology Attachment
SATA1RX+	SATA 1 received data non-inverted
SATA1RX-	SATA 1 received data inverted
SATA1TX+	SATA 1 transmitted data non-inverted
SATA2TX-	SATA 2 transmitted data inverted
SATA2RX+	SATA 2 received data non-inverted
SATA2RX-	SATA 2 received data inverted
SATA2TX+	SATA 2 transmitted data non-inverted
SATA1TX-	SATA 1 transmitted data inverted
SD00..07	Data 0...7
SELFRES#	Self reset

SNDL	Sound left channel
SNDR	Sound right channel
SPR+	Speaker output non-inverted
SPR-	Speaker output inverted
SPRSD#	Speaker shutdown
STATUS#	Status output
SYNC	Synchronizing pattern send control
TCLK	Transmitter clock
TD1...2	Transmitted data 1...2
TD3A...C	Transmitted data 3 A...C
TD4...6	Transmitted data 4...6
TEST	Test input
TESTX#	Received test signal
THRMTRP#	Thermal trip
TPWDN#	Transmitter power down
TS1...5	Test signal 1...5
TXD1...2	Transmitted serial data 1...2
TXD3A...B	Transmitted serial data 3 A...B
TXD3C+	Transmitted serial data 3 C non-inverted
TXD3C-	Transmitted serial data 3 C inverted
TXD4...6	Transmitted serial data 4...6
USB	Universal serial bus
USB1...8+	USB data 1...8 non-inverted
USB1...8-	USB data 1...8 inverted
VGA	Video graphics array
VGAB	VGA blue output
VGABL	VGA blue
VGAG	VGA green output
VGAGR	VGA green
VGAH	VGA horizontal sync output
VGAHSYNC	VGA horizontal sync
VGAI2CSCL	VGA I2C bus clock
VGAI2CSDA	VGA I2C bus data
VGAR	VGA red output

VGARED	VGA red
VGASCL	VGA I2C bus clock output
VGASDA	VGA I2C bus data output
VGAV	VGA vertical sync output
VGAVSYNC	VGA vertical sync

4.3.6 MPU121A Connectors

4.3.6.1 System Connector

System connector is a 220-pin, 5-row female connector for system connections via motherboard.

Signals at system connector are listed in the following table:

Table 45 System Connector Signal Layout

Pin/Ro w	a	I/O	b	I/O	c	I/O	d	I/O	e	I/O
1	GND		GND		GND		GND		GND	
2	SNDR	O	SNDL	O			VGASDA	I/O	VGASCL	O
3	TS1	I/O	TS2	I/O	TS3	I/O	TS4	I/O	TS5	I/O
4	VGAR	O	VGAG	O	VGAB	O	GND		VGAH	O
5	VGAV	O	GND		GND		GND		GND	
6	USB1+	I/O	USB1-	I/O	GND		USB2+	I/O	USB2-	I/O
7	+5VUSB1	O	GND		GND		+5VUSB2	O	GND	
8	USB3+	I/O	USB3	I/O	GND		USB4	I/O	USB4	I/O
9	+5VUSB3	O	GND		GND		+5VUSB4	O	GND	
10	SATA1RX+		SATA1RX-		GND		SATA1TX+		SATA1TX-	
11	GND		GND		GND		GND		GND	
12	LVDSA0+	O	LVDSA0-	O	GND		LVDSA1+	O	LVDSA1-	O
13	SPR-	O	SPR+	O	GND		LVDSA3+	O	LVDSA3-	O
14	LVDSA2+	O	LVDSA2-	O	GND		LVDSACLK +	O	LVDSACLK -	O
15	GND		GND		GND		GND		GND	
16	E1RX+	I	E1RX-	I	GND		E1TX+	O	E1TX-	O
17	GND		GND		GND		GND		GND	
18	ARC+	I/O	ARC-	I/O						
19	TXD6	O								

20	RXD6	I							
21	TXD5	O							
22	RXD5	I							
23	GND		GND		GND		GND		GND
24	E2RX+	I	E2RX-	I	GND		E2TX+	O	E2TX-
25	GND		GND		GND		GND		GND
26	RIN+	I	RIN-	I	DO+	O	DO-	O	
27	GND		GND		GND		GND		GND
28	TXD3A	O	TXD3B	O	TXD3C-	O	TXD3C+	O	
29	RXD3A	I	RXD3B	I	RXD3C-	I	RXD3C+	I	
30	TXD2	O	DTR2	O	RTS2	O	ARC+	I/O	
31	RXD2	I	DSR2	I	CTS2	I	ARC-	I/O	
32	TXD1	O	TXD4	O	OPX1	O	OPX2	O	
33	RXD1	I	RXD4	I	IPX1	I	IPX2	I	
37			+3.3VBAT	I	MRES#	I	+12V	I	STATUS#
38	JTDOUT	O	JTCKIN	I			JTDIN	I	JTMSIN
39			TESTX#	I			DA2OUT	I	
40									
41	PTOGGLE #	I	CPUON#	O	+5VSTBY	I	I2CSDA	I/O	I2CSCL
42	+3.3 V	I	+3.3 V	I	+3.3 V	I	+3.3 V	I	+3.3 V
43									
44	+5 V	I	+5 V	I	+5 V	I	+5 V	I	+5 V
45	RACK0#		RACK1	I	RACK2	I			
46	+12 V	I	+12 V		GND				
47	GND		GND		GND		GND		GND

4.3.6.2 Front Panel Connectors

4.3.6.2.1 Ethernet Connectors

Two Ethernet connectors for channels 1 and 2 are provided at the front panel of the unit.

Type of connector:	RJ45 female
Corresponding cable connector:	RJ45 male

Signals at both Ethernet connectors are according to following table:

Table 46 ETH1 and ETH2 Connectors Signal Layout

Signal	Pin	Description	Level
ETX+	1	Data output for Ethernet, differential line	Ethernet
ETX-	2	Data output for Ethernet, differential line	Ethernet
ERX+	3	Data input for Ethernet, differential line	Ethernet
ERX-	6	Data input for Ethernet, differential line	Ethernet

4.3.6.2.2 USB Connectors

Four USB connectors for channels 5 to 8 are provided at the front panel of the unit.

Type of connector:	KUSB-AS2NBLK30
--------------------	----------------

Table 47 ETH1 and ETH2 Connectors Signal Layout

Signal	Pin	Description	Level
+5V	1	+5 V power for external use	
USB+	2	USB data+, differential line	
USB-	3	USB data-, differential line	
GND	4	Ground reference	

4.3.7 MPU121A Diagrams and Board Layouts

Table 48 MPU121A Diagrams and Board Layouts

Code	Description
SCH210127	MPU121A Block Diagram
SCH210128	MPU121A Circuit Diagram, 7 pages
ASM213053	MPU121A Assembly Drawing, 2 pages
LAY210047	MPU121A Components Layout, 2 pages

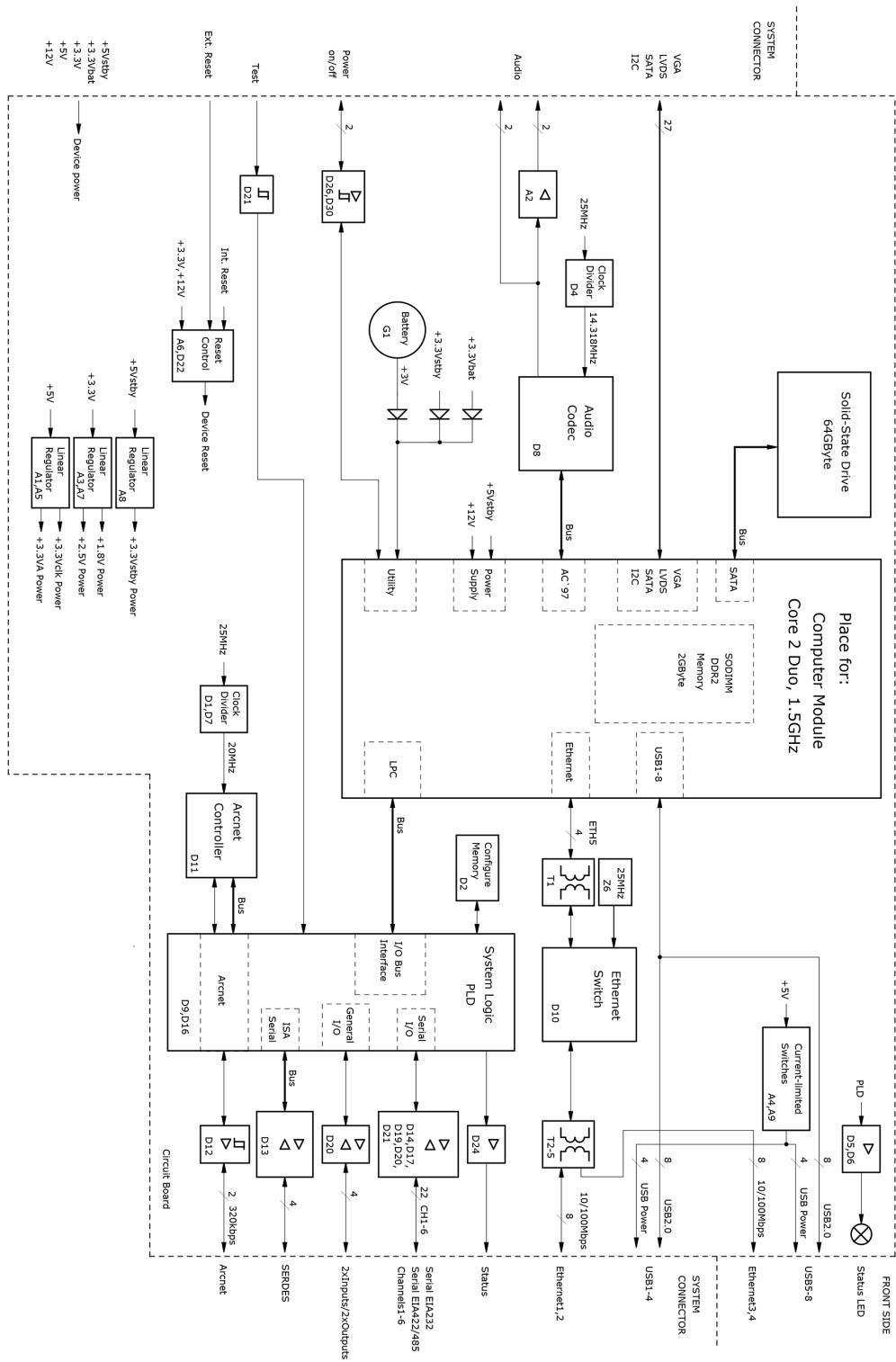


Figure 37 MPU121A Block Diagram

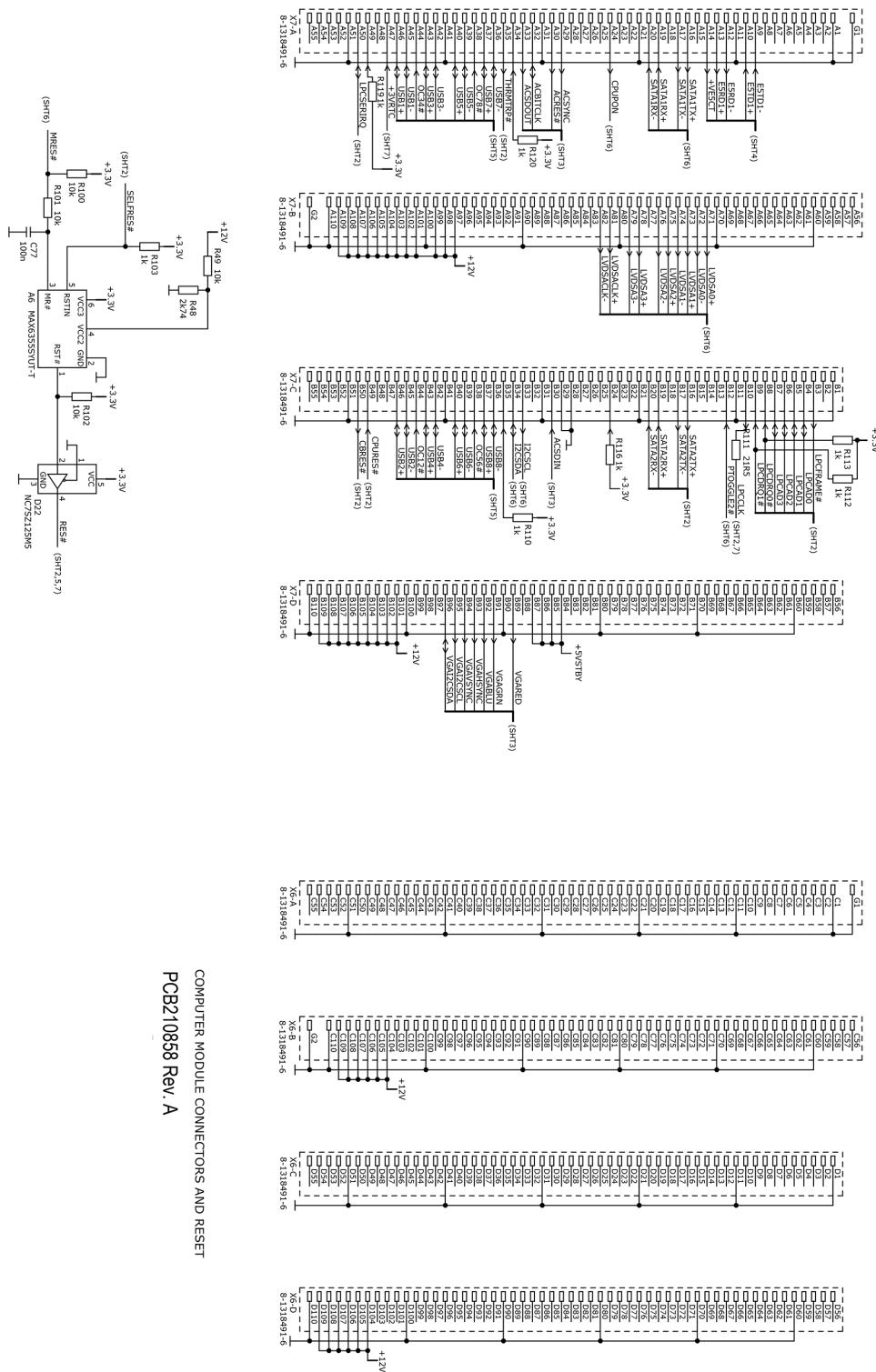


Figure 38 MPU121A Circuit Diagram, 1/7

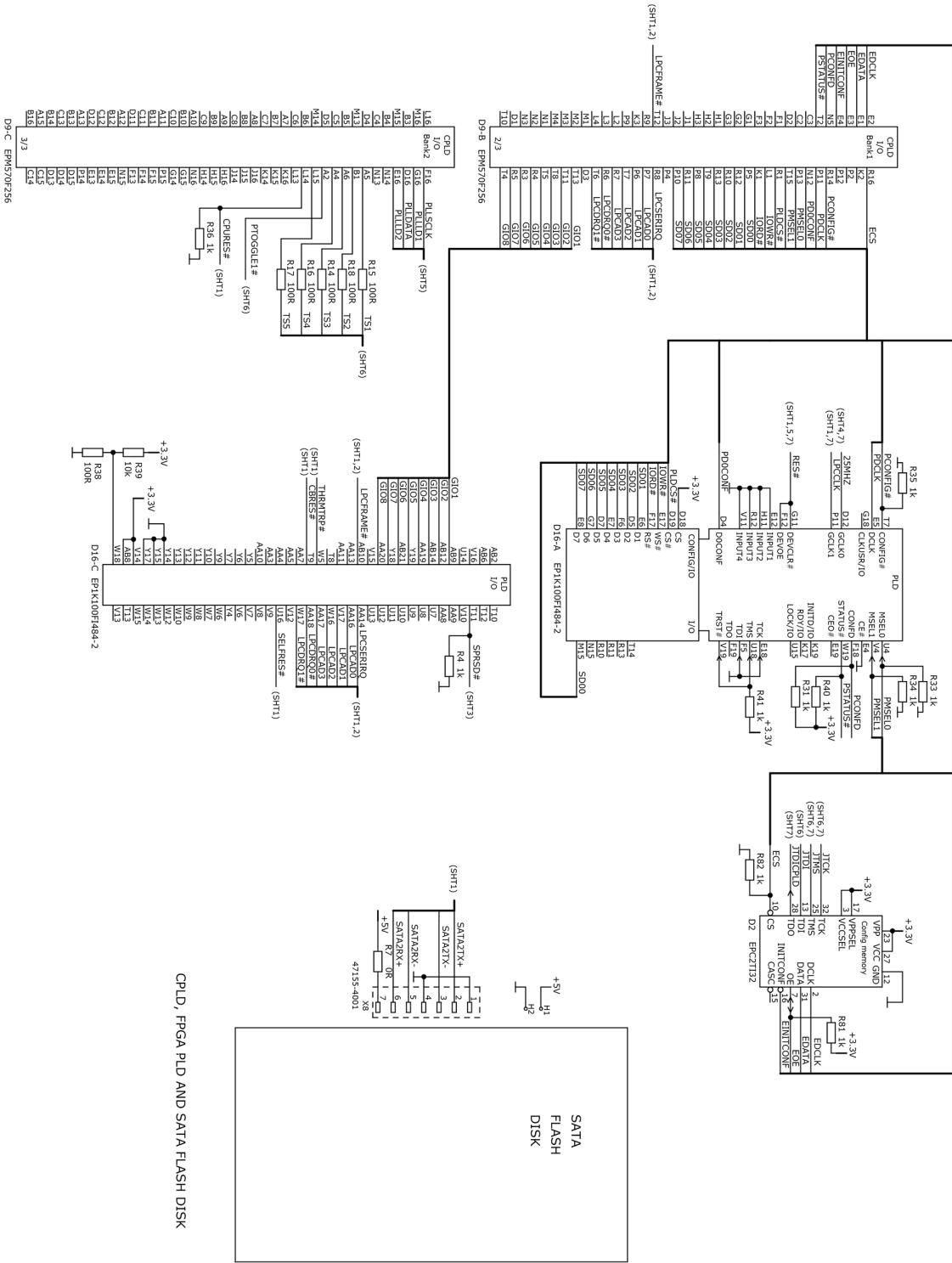


Figure 39 MPU121A Circuit Diagram, 2/7

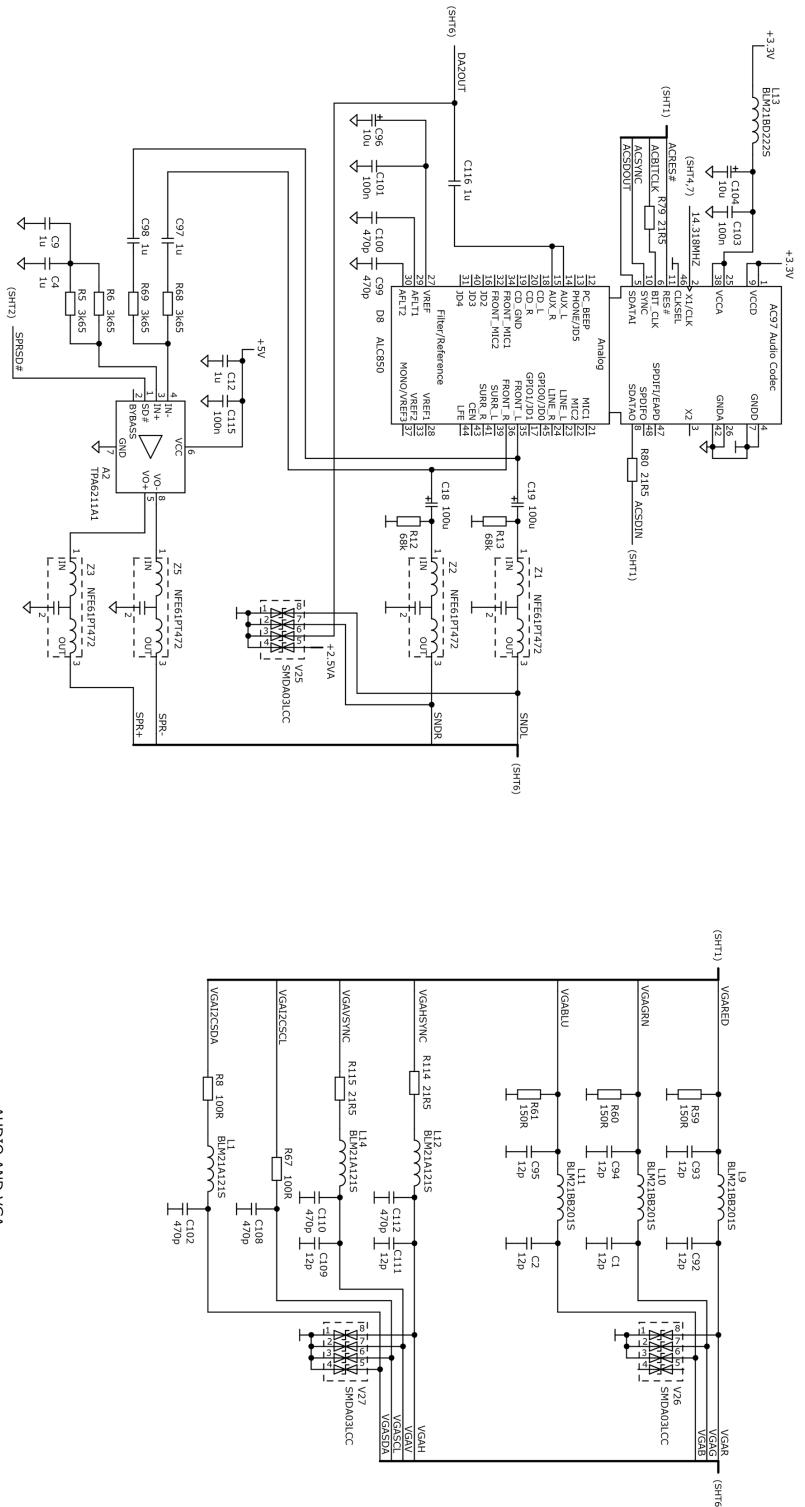


Figure 40 MPU121A Circuit Diagram, 3/7

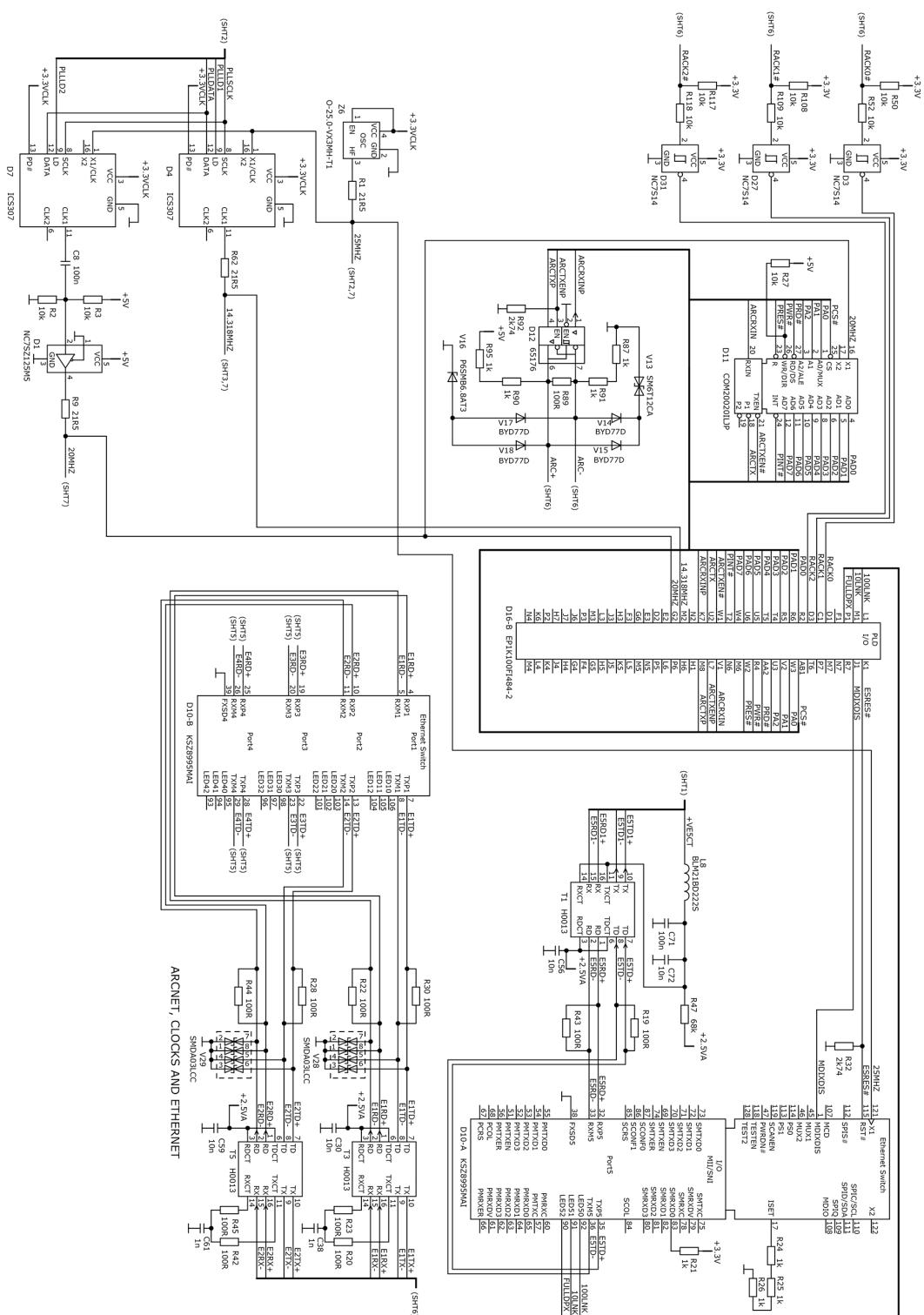


Figure 41 MPU121A Circuit Diagram, 4/7

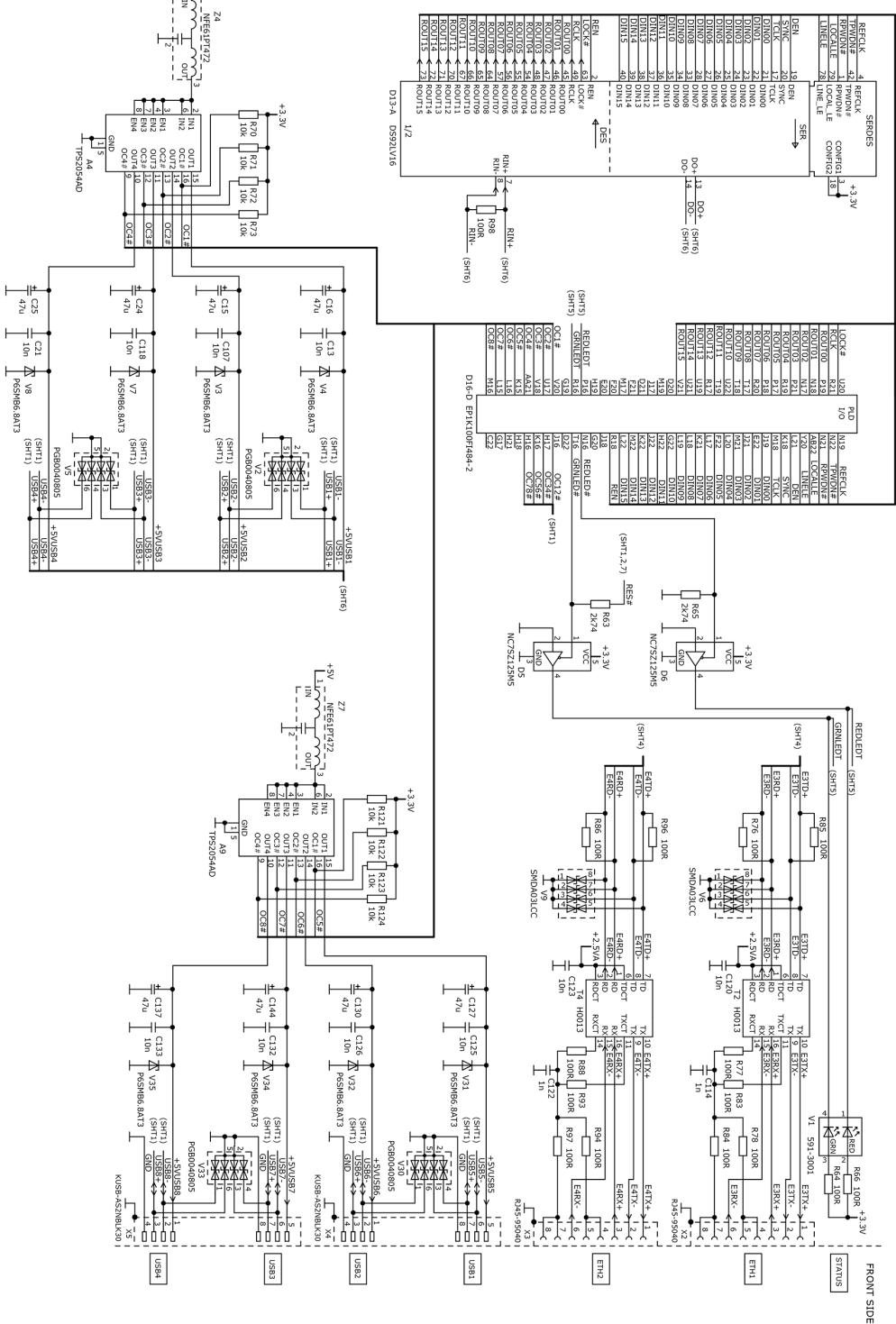


Figure 42 MPU121A Circuit Diagram, 5/7

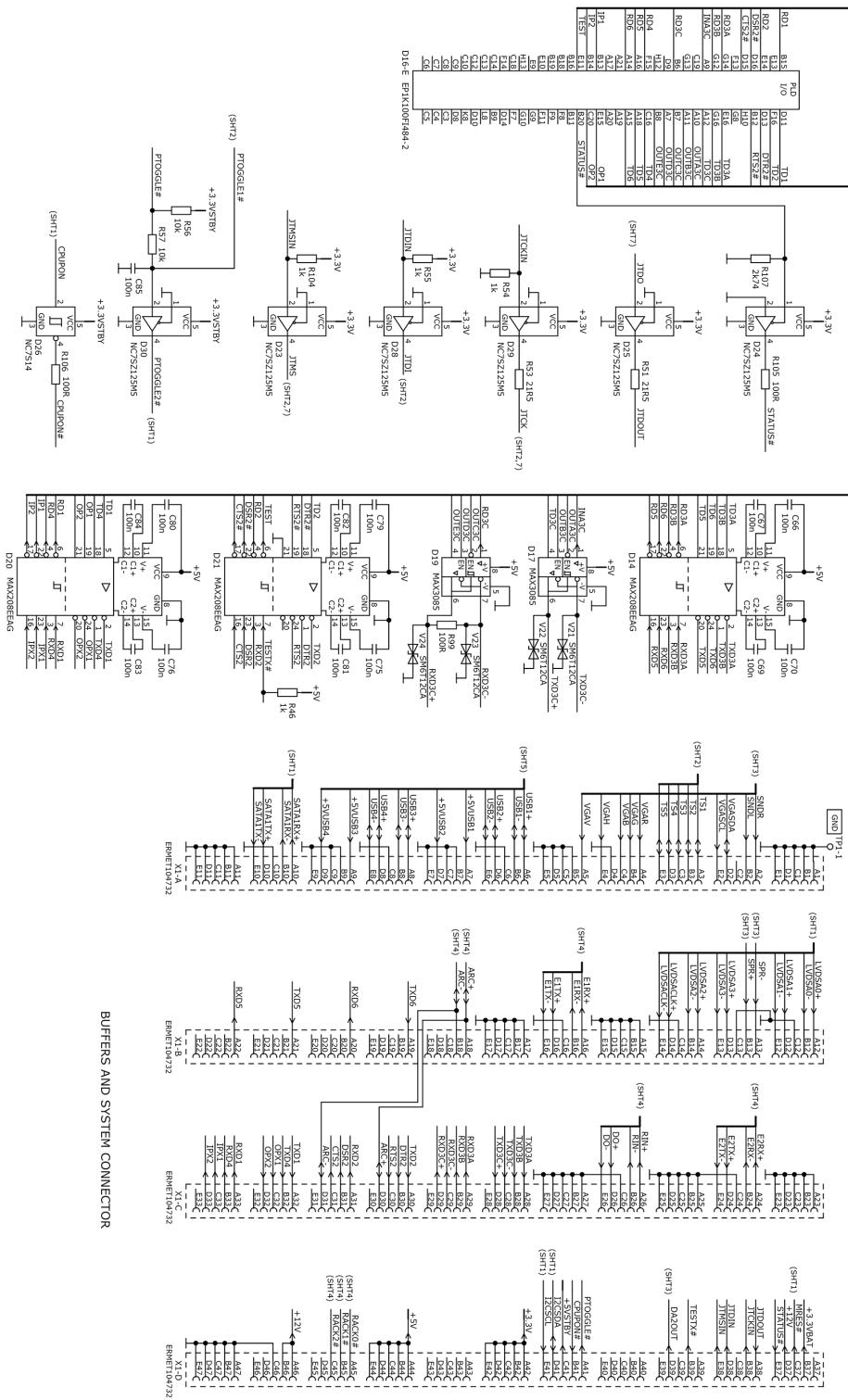


Figure 43 MPU121A Circuit Diagram, 6/7

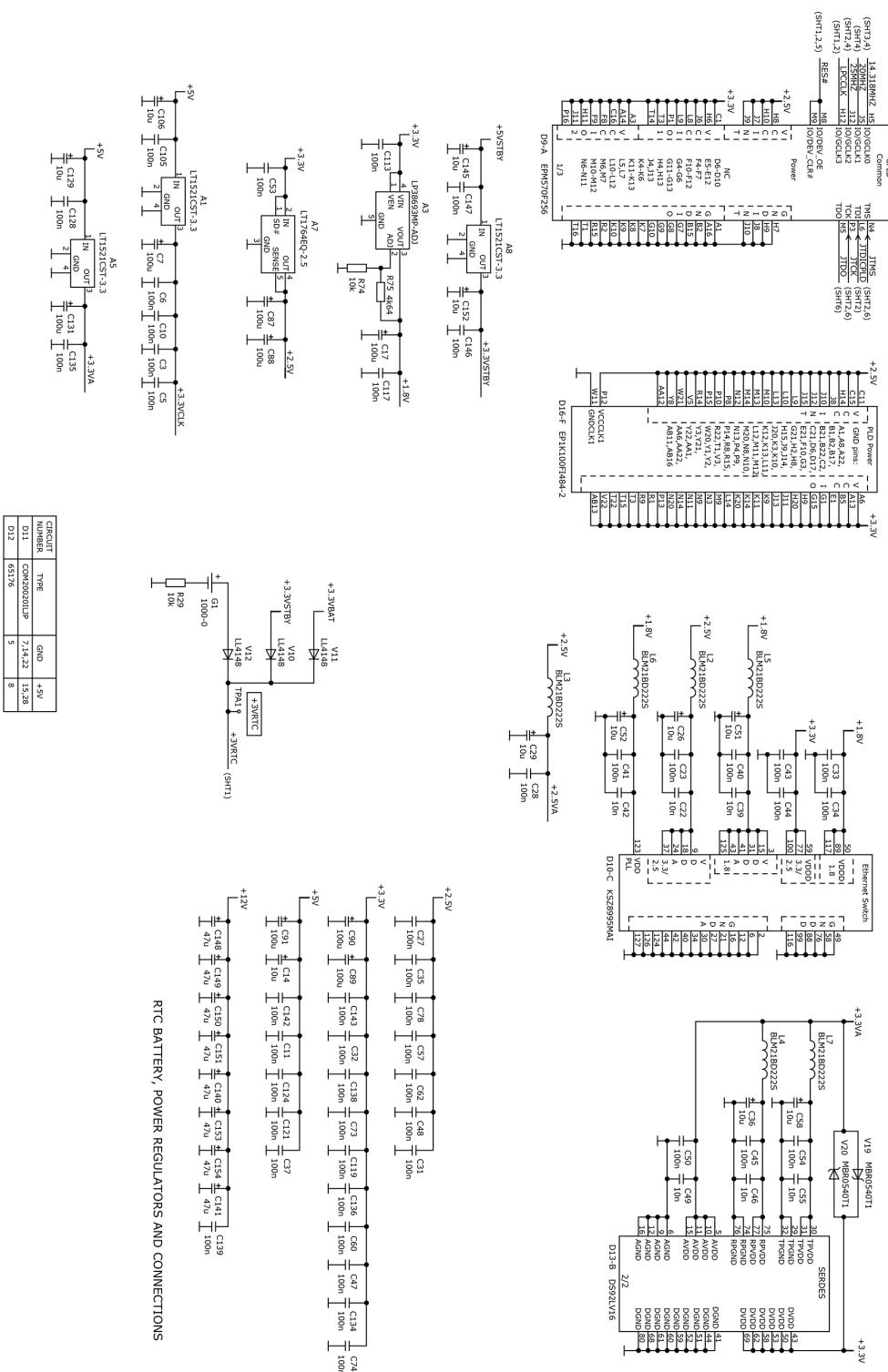


Figure 44 MPU121A Circuit Diagram, 7/7

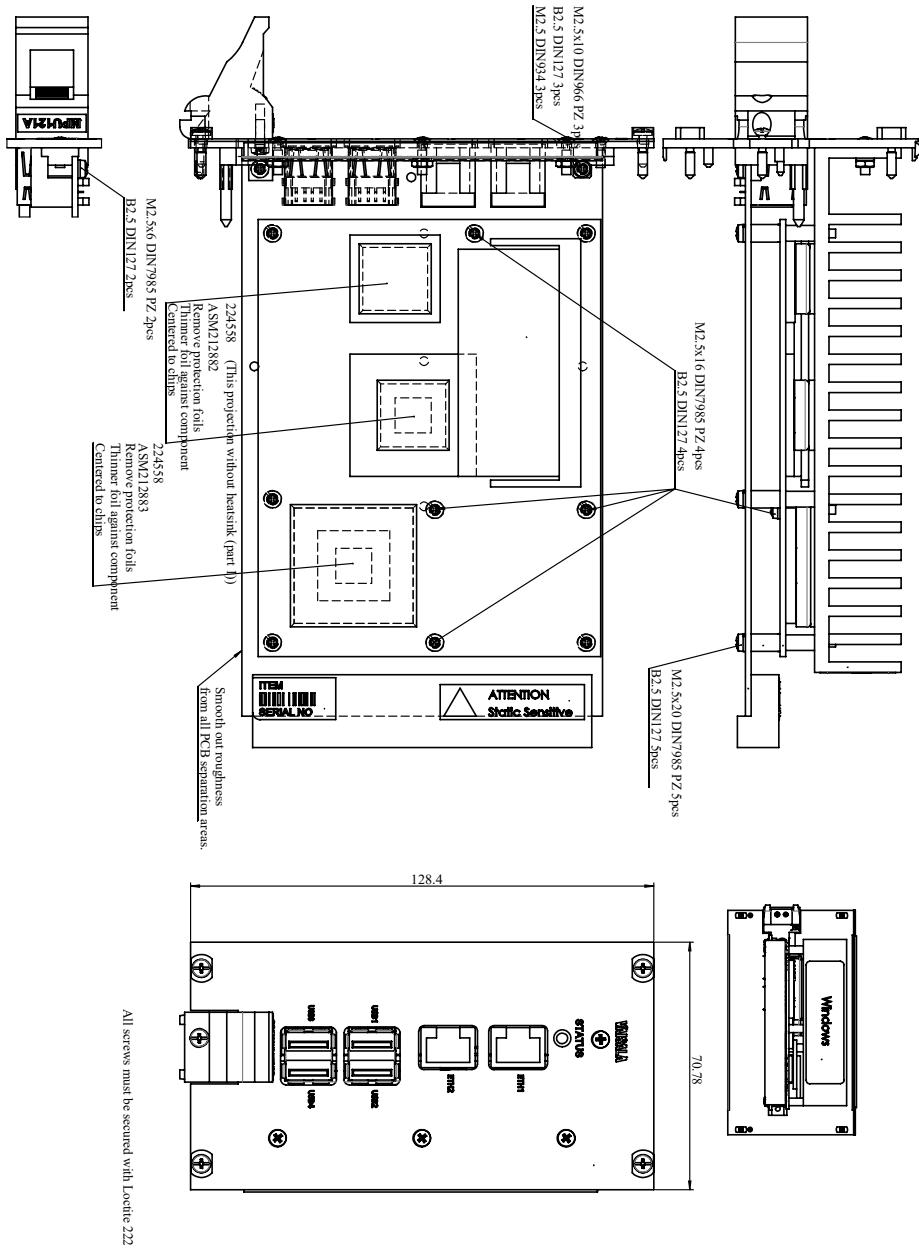


Figure 45 MPU121A Assembly Drawing 1/2

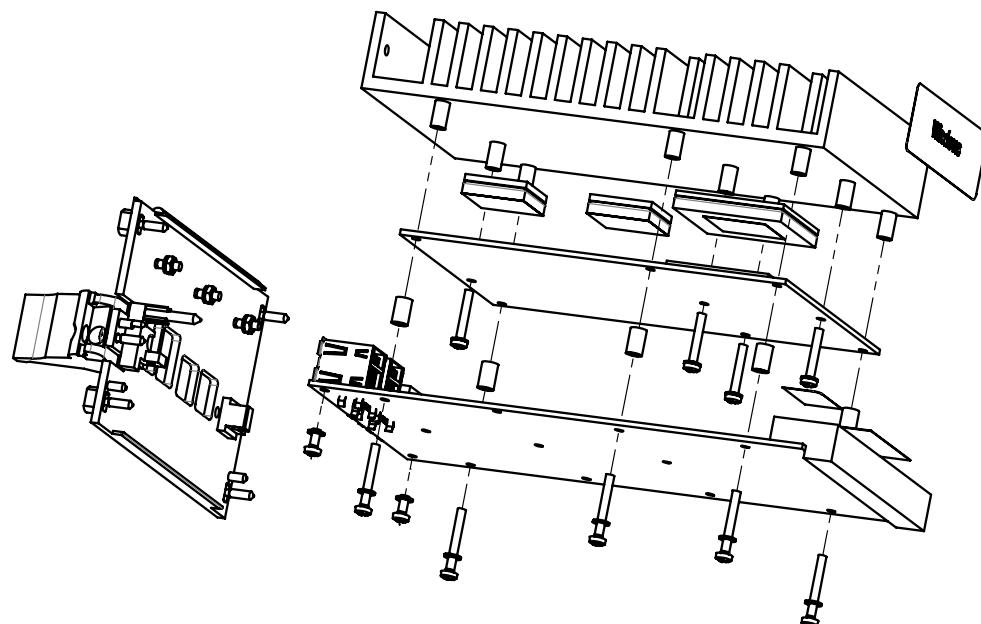


Figure 46 MPU121A Assembly Drawing 2/2

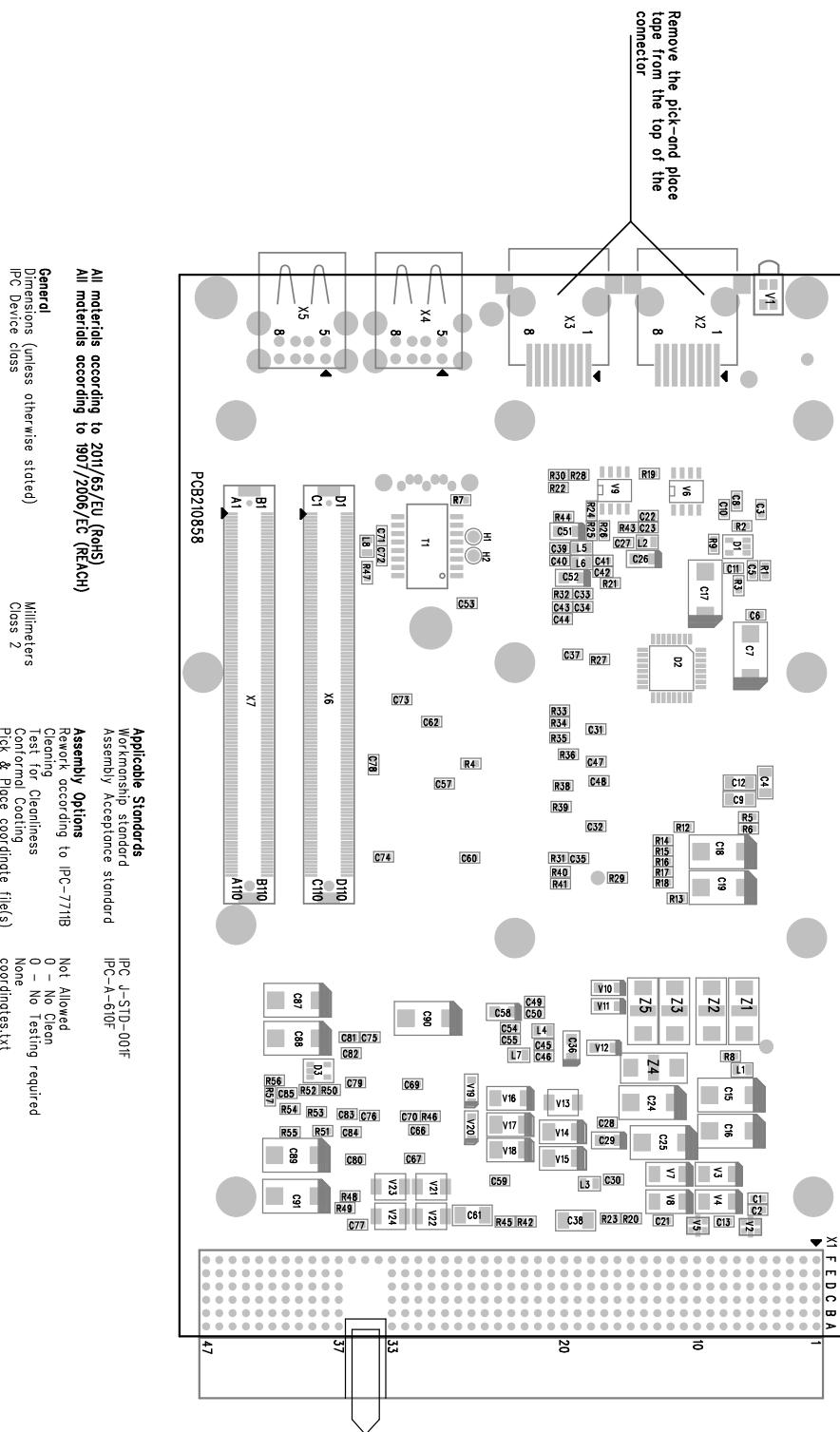


Figure 47 MPU121A Components Layout 1/2

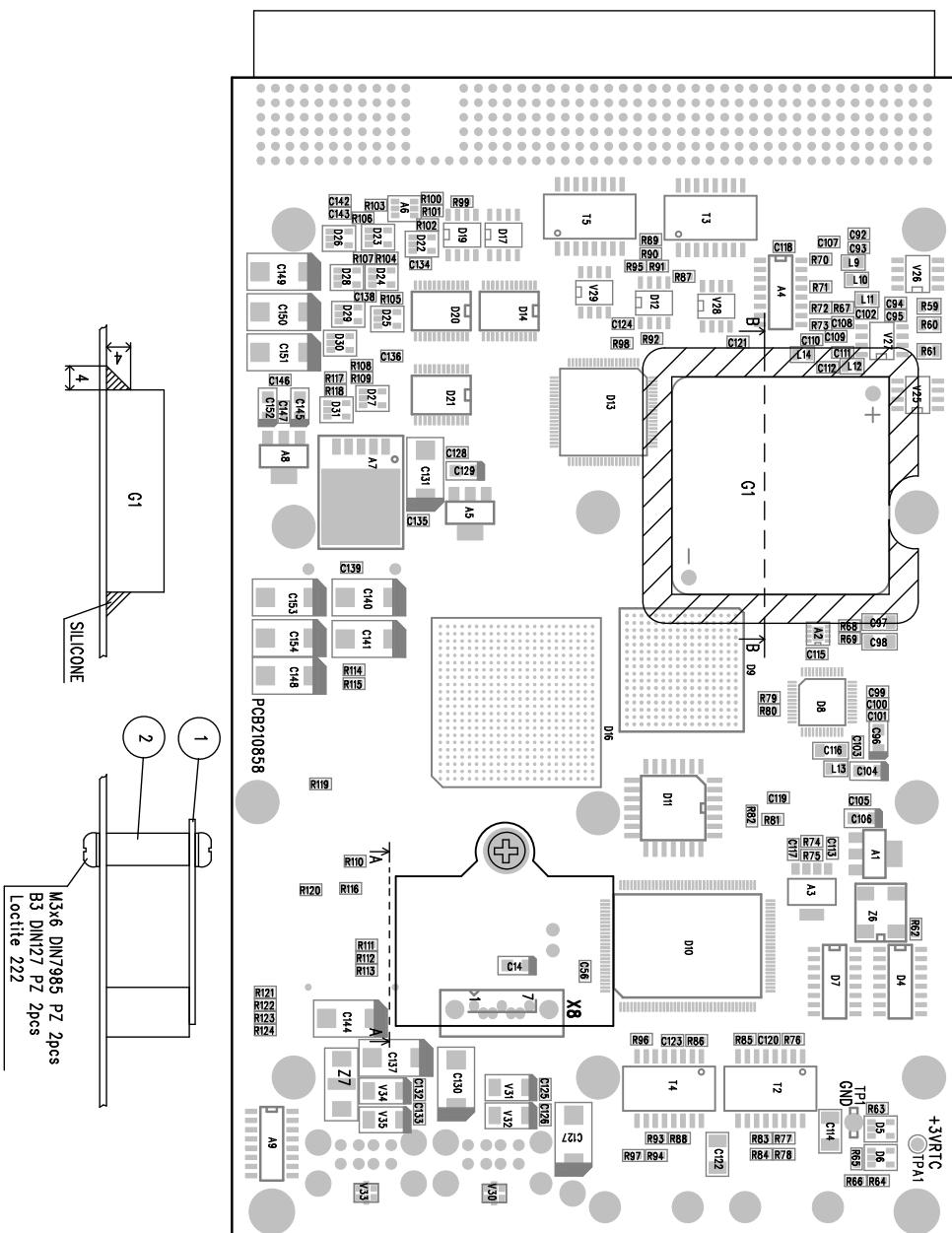


Figure 48 MPU121A Components Layout 2/2

4.4 Power Supply MWP312

Power Supply MWP312 is an E1-sized plug-in system power unit. MWP312 connects to the motherboard through a 32-pin Euro connector and provides DC operating voltages for the system.

The input power is a 24 V DC voltage. The regulated output voltages +3.3 V, +5 V, +7 V, +12 V and -12 V DC are fed to the Euro connector. The input power connection is floating and the output voltages are short-circuit protected.

MWP312 automatically enters standby state when the input power is connected. In this state, only +5 V internal DC voltage is on and a +5 V standby voltage for low power external use is available. All other DC/DC converters are disabled and the +5 V power switch is off.

The system power on/off is controlled by logic signals. Two alternative control methods are provided: direct on/off control with separate on and off control signals; or alternating control with a single on/off (toggle) control line. The control signals are available in the Euro connector and in the front panel power control connector. LED lights for all DC output voltages are provided for monitoring purposes.



Figure 49 Power Supply MWP312

4.4.1 Control Logic

The PLD circuit D1 controls the state of the power unit. During power-up, the reset controller A8 keeps the reset signal input (D1/31) active and the D1 enters power-off (standby) state where only internal +5V voltage and +5VSTBY output voltage are on.

The control inputs PON#, POFF#, PTOGGLE#, and MPUPON# are used to set the supply in power-on or in standby state. The signal PON# switches the power on. The signal POFF# switches the power off. The signal PTOGGLE# is used to change the state of the supply. The MPUPON# signal is optionally used for delayed power off (see section [Controlled Shut Down \(page 125\)](#)).

The output signal at pins 34 and 35 of D1 is used to control the A2, A3 and A4 DC/DC converters. The high-level output signal switches the converters on by feeding current to the optocoupler V21 which turns V21 collector voltage at low level. This further turns off the transistor V22 and enables the DC/DC converters A2 and A3 and turns on the FET V23 which feeds the input voltage to the -12 V DC/DC converter. Converter A3 output +12 V is further used to control the +5V power switch and as power input for +7V DC/DC converter A6.

4.4.2 Standby Regulator

The linear voltage regulator A5 is used as 400 mA current limiter in the +5 VSTBY output.

4.4.3 Output Switch

N-channel FET transistors V7 and V8 are used to connect +5 V output voltage on/off. Two 13.5 milliohm devices in parallel are used to keep the worst case on-state voltage loss below 40 mV.

+12 V output voltage is used to control the +5 V output switch V7 and V8. The +12 V switches the +5 V power on by turning the gate voltage of FET transistors at high level via operational amplifier A7. Gate voltage is not switched high if the +12 V voltage is below +8 V.

4.4.4 Power Indicators

The output voltages are monitored by comparator circuits A9, A10 and A11. When a voltage falls below 80 % of its nominal value, the output of the comparator changes state to indicate low voltage condition. The comparator outputs are connected to the PLD circuit D1 which turns the corresponding indicator LED light to red by switching off the green LED in a bi-color lamp. At the same time, blinking control is activated at control signal RED (power control connector X2 pin 6) for external indication of the power fault condition.

4.4.5 Power-up

At power-up, D1 sets the GRN control output (X2/1) blinking until the low drive of STATUS# input signal (X1/c12) is released by all external system units. A unit typically releases the common STATUS# line when its power-up test routines are completed successfully.

If STATUS# remains active for more than 6 minutes, the D1 turns the RED control on to indicate that at least one system unit has failed in the power-up procedure.

4.4.6 Controlled Shut Down

The signal MPUON# (X1/a4) is used for a controlled shut down if the system includes optional embedded PC computer. In that case when the PTOGGLE# control is activated the active MPUPON# signal delays power off until the computer is completed its shutdown operations and releases the MPUPON# control. The delayed power-off period is indicated by blinking GRN control for external status indicator.

4.4.7 Temperature Monitor

The unit includes a temperature monitor circuit for an over temperature warning and shut down features. The circuit consists of temperature sensing NTC resistor R57, fixed resistor R24, capacitor C29, inverter gate D3-F, and 3-state buffers D4,D5. In operation the PLD D1 alternatively connects NTC resistor and fixed resistor R24 as a feedback resistor for the RC oscillator and calculates the unit temperature by comparing the oscillator frequencies.

When temperature rises over +70 °C, a temperature warning is given by blinking the RED control for the external indicator.

At temperatures over +90 °C, a temperature shut-down to the standby state is performed and the RED control for external indicator is set.

4.4.8 Technical Specifications MWP312

Table 49 MWP312 Technical Specifications

Property	Value / Description
Nominal Input Voltage	24 V
Input Voltage Range	18 36 V
Typical Input Current	2.7 A, Vin 24 V (50 W load) 3.6 A, Vin 18 V (50 W load)
Outputs	+3.3 V (3.1... 3.4 V) / 7 A +5 V (4.75 ... 5.25 V) / 5 A +7 V (6.7 ... 7.2V) / 1 A +12 V (11.0 ... 13.0) / 1 A -12 V (-11.0 ... -13.0) / 0.1 A +5 V stby (4.25 ... 5.25) / 0.4 A
Operating Temperature	-30+55°C
Storage Temperature	-55+70°C
Humidity	Non-condensing
Dimensions (height, depth, width)	100 mm × 160 mm × 20 mm
Weight	0.4 kg

4.4.9 Power Control Connector

- Connector: 9-pin female D
- Mating cable connector: 9-pin male D

Table 50 Power Control Connectors

Pin	Signal	Description
1	GRN	Power on indicator output
2	RACK0	Rack code LSB
3	RACK1	Rack code MSB
4	POFF#	Power off control input
5	GND	Ground
6	RED	Error indicator output
7	PON#	Power on control input
8	YEL	Standby power indicator output
9	PTOGGLE#	Power toggle control input

4.4.10 System Connector MWP312

- Connector: 32-pin, 2-row male power Euro connector
- Mating connector: 32-pin, 2-row female power Euro connector

Table 51 System Connectors

Pin	Row A		Row C	
	Signal	Description	Signal	Description
2	GND	Ground	GND	Ground
4	MPUPON#	Power control input from MPU-unit	POFF#	Power off control input
6	PON#	Power on control input	PTOGGLE#	Power toggle control input
8	RACK0	Rack code LSB	RACK1	Rack code MSB
10	+V	Input Power +	+V	Input Power +
12			STATUS#	Status indicator input
14	-V	Input Power -	-V	Input Power -
16	+5VSTBY	+5 V standby voltage	+5VSTBY	+5 V standby voltage
18	+3.3V	+3.3 V DC power	+3.3V	+3.3 V DC power
20	+3.3V	+3.3 V DC power	+5V	+5 V DC power
22	+5V	+5 V DC power	+5V	+5 V DC power

24	+7V	+7 V DC power	+7V	+7 V DC power
26	+12V	+12 V DC power	+12V	+12 V DC power
28	-12V	-12 V DC power	-12V	-12 V DC power
30	GND	Ground	GND	Ground
32	GND	Ground	GND	Ground

4.4.11 Parts List MWP312

Table 52 MWP312 Parts List

Part No.	Code	Description	Qty
Chassis			
	DRW212800	Front panel assembly for MWP312	1
	DRW212802	Front panel, machined, for MWP312	-
	PCB210230(B)	Printed circuitboard for MWP312	1
	DRW212802	Heat sink for MWP311	1
Integrated Circuits			
A1	210846	Converter, DC/DC, QS075YG-A	1
A2	210845	Converter, DC/DC, QS050YE-A	1
A3	210847	Converter, DC/DC, QS100YH-A	1
A4	210300	Converter, DC/DC, TEP-2412	1
A4	16730	IC, op. amp., TL082ID (SMD)	1
A5	19991	IC, voltage regulator, MIC2920A-5.0BS	1
A6	25073	IC, voltage regulator LM2672-ADJ	1
A8	25330	IC, supervisor, MAX810EUR-T (SMD)	1
A9, A10, A11	19784	IC, comparator, LTC1442IS8(SMD)	3
D1	25771	IC, EPM7064STC44-10 (SMD)	1
D2,D3	15964	IC, inverter, Ex, 74HC14 (SMD)	2
D4, D5	26570	IC, buffer, NC7SZ125M5 (SMD)	2
Transistors and Diodes			
V1, V2, V3, V4,V5, V6	010192	Diode, LED, 591-3001	6
V7, V8, V23	25302	Transistor, FET, PHN1013 (SMD)	3
V9, V11, V14, V19, V26, V27, V28, V31	17332	Diode, Transil, P6SMB6.8AT3 (SMD)	8
V10	17448	Diode, Transil, SMCJ43A, (SMD)	1

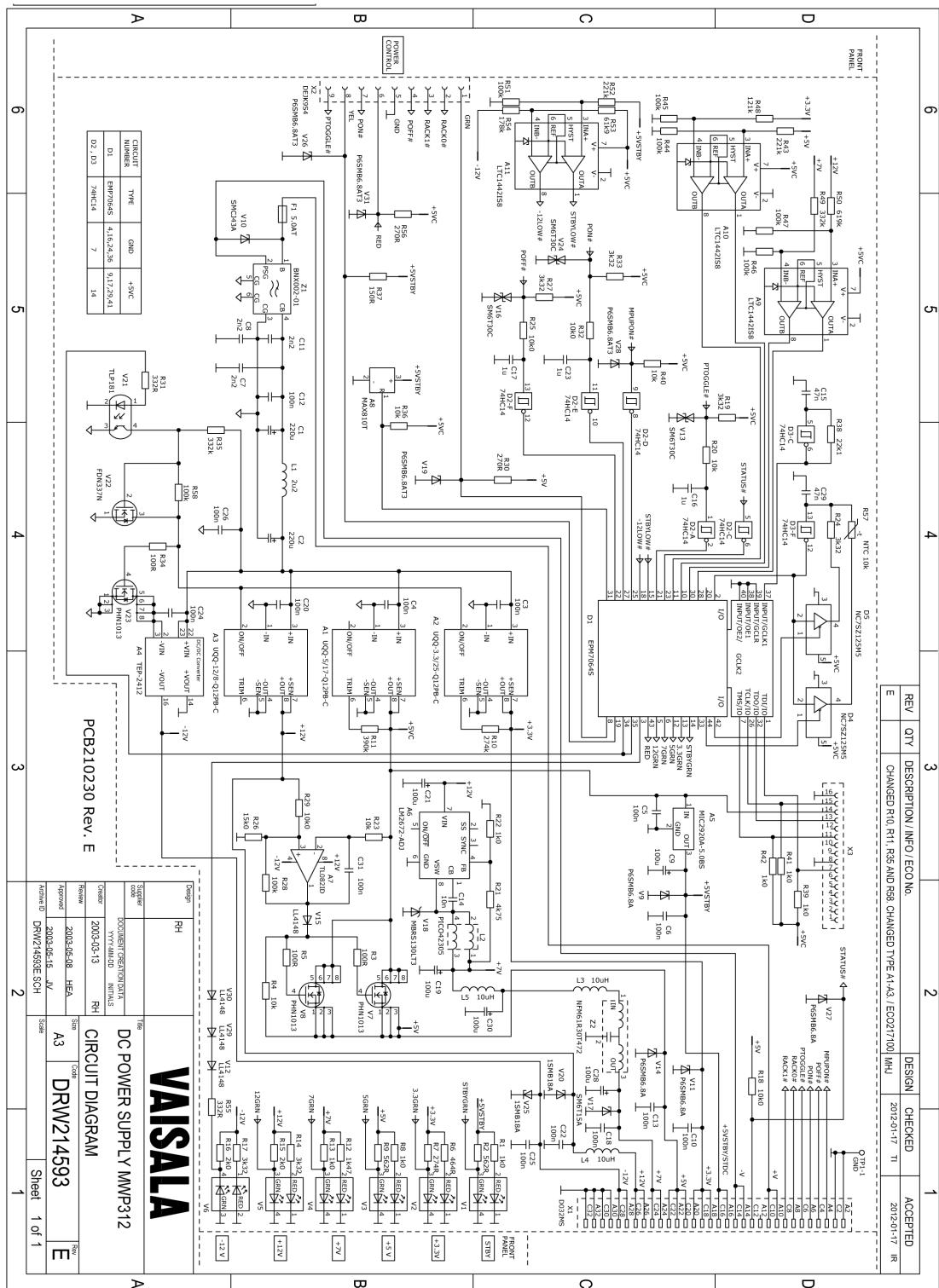
Part No.	Code	Description	Qty
V12, V15, V29, V30	15976	Diode, silicon, Ex, LL4148/PMLL4148 (SMD)	4
V13, V16, V24	17311	Diode, Transil, SM6T30CA (SMD)	3
V17	19241	Diode, Transil, SM6T15A (SMD)	1
V18	19463	Diode, Schottky, MBR130LT3 (SMD)	1
V20, V25	25030	Diode, Transil, 1SMB18AT3 (SMD)	2
V21	16982	Optocoupler, Ex, TLP 181 (SMD)	1
V22	15495	Transistor, NPN, SST3904 SOT-23	1
Resistors			
R1, R8, R13, R22, R39, R41, R42	18117	Resistor, chip, 1k0 1% 100 ppm 0805	7
R2, R9	18730	Resistor, chip, 562R 1.0% 100 ppm 0805	
R3, R5, R34	19459	Resistor, chip, 100R 0.5% 25 ppm 0603	3
R4, R18, R20, R23, R25, R29 R32, R36, R40	25262	Resistor, chip, 10k0 1% 100 ppm 0603	9
R6	18683	Resistor, chip, 464R 1.0% 100 ppm 0805	1
R7	18683	Resistor, chip, 274R 1% 100 ppm 0805	1
R10, R11, R38	19710	Resistor, chip, 22k0 5% 200 ppm 0603	3
R12	18734	Resistor, chip, 1k47 1% 50 ppm 0805	1
R14, R17, R19,R27, R33	18410	Resistor, chip, 3k32 1% 50 ppm 0805	5
R15, R16	18119	Resistor, chip, 1k82 1% 100 ppm 0805	2
R21	26126	Resistor, chip, 4k75 0.5% 25 ppm 0603	1
R24, R44, R45, R46, R47, R51	25451	Resistor, chip, 100k 1.0% 100 ppm 0603	6
R26, R35	25169	Resistor, chip, 15k0 1% 100 ppm 0603	2
R30, R37	18120	Resistor, chip, Ex, 2k0 1% 50 ppm 0805	2
R30, R56	16416	Resistor, chip, 270R 1% 50 ppm 1206	1
R31, R55	25210	Resistor, chip, 332R 1.0% 100 ppm 0603	2
R37	16415	Resistor, chip, 150R 1% 50 ppm 1206	1
R43, R52	18797	Resistor, chip, 221k 1% 50 ppm 0805	2
R48	18888	Resistor, chip, 121k 1% 50 ppm 0805	1
R49	18604	Resistor, chip, 332R 1% 50 ppm 0805	1
R53	26125	Resistor, chip, 61k9 1% 100 ppm 0603	1
R54	18734	Resistor, chip, 1k47 1% 50 ppm 0805	1

Part No.	Code	Description	Qty
R57	18857	Resistor, chip, NTC,10k 5% B3630K 1206	1
Capacitors			
C1, C2	19482	Cap., electrolytic SMD, 220 µF 35 V 20%	2
C3,C4,C5, C6, C10, C12, C13, C18, C20, C22, C24, C25, C26	15621	Cap., chip ceramic, Ex, 100n 10% X7R 50V 0805	13
C7, C8, C11	16390	Cap., chip ceramic 2n2	3
C9, C19, C21,C28,	25560	Cap., electrolytic SMD 100µF	5
C14	15160	Cap., chip ceramic 10nF X7R 50V 0805	1
C16, C17, C23	25066	Cap., chip ceramic, Ex, 1000nF X5R 1206	3
C25, C29	18287S	Cap, chip polyester, 47nF 5% 25V 1812	1
C27	15750	Cap., chip ceramic 330nF X7R 2220	1
C30			
Filters and Chokes			
Z1	16826	Filter, DC, BNX002-01	1
Z2	25036	Filter, EMI, NFM61R30T472 (SMD)	1
L1	26708	Choke, power, 2.2uH 7.4A 0.011 Ohm	1
L2	16302	Choke, PICO42305	1
L3, L4, L5	19604	Choke, power, 10uH 1.1A 0.14R (SMD)	3
Connectors			
X1	1812	Connector, Euro, D032MS-C1A-0.8/5253	1
X2	19285	Connector, D, DEJK9S4-1A7N-146	1
X3	19640	Connector, horizontal (SMD) 2x8 0.1"	1
	6014	Connector accessory, D20418-2	2
Miscellaneous			
F1	7048	Fuse, glass tube, 5.0AT	1
	7028	Fuse holder, 1611PR 1/12 OSA	1
	211740	Hexag. tapped spacer 5,03. 13.53 M3-13.5	2
	0840	Rivet, 2,5 x 9,9 /Ms/Tin	2
	18574	Screw, crosshead, M 3 x 6 /A4m	2
	211738	Screw, crosshead, M2.5 x 6 /A4	6
	25015	Screw, crosshead, M 3 x 8 /A4m	14
	3939	Washer, spring, B3 /A4	2
	7067	Washer, spring, B2.5 /A4	2

4.4.12 Diagrams and Board Layouts MWP312

Table 53 MWP312 DC Power Supply Illustrations

Code	Description
DRW214593	Circuit Diagram
DRW214594	Components Layout, 2 pages



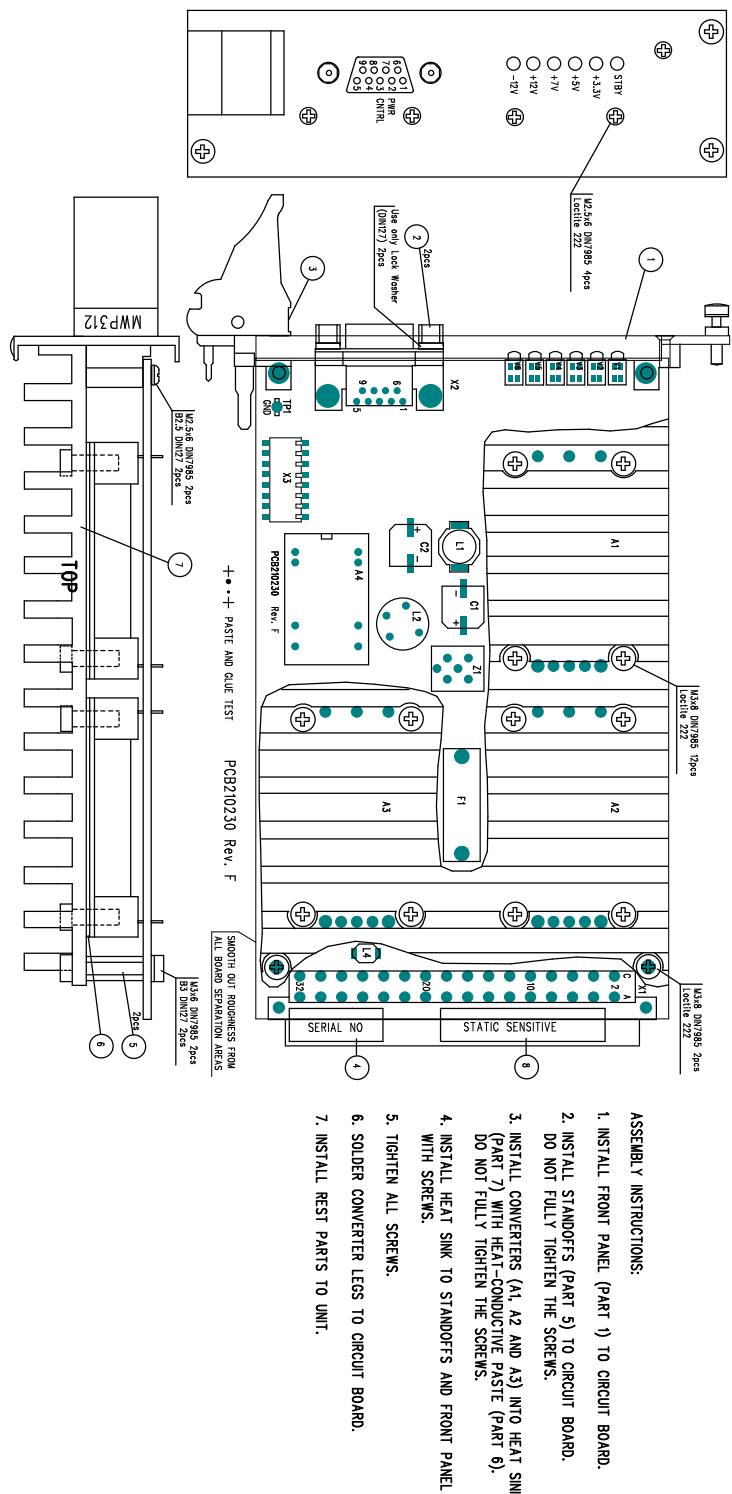


Figure 51 MWP312 Components Layout 1/2

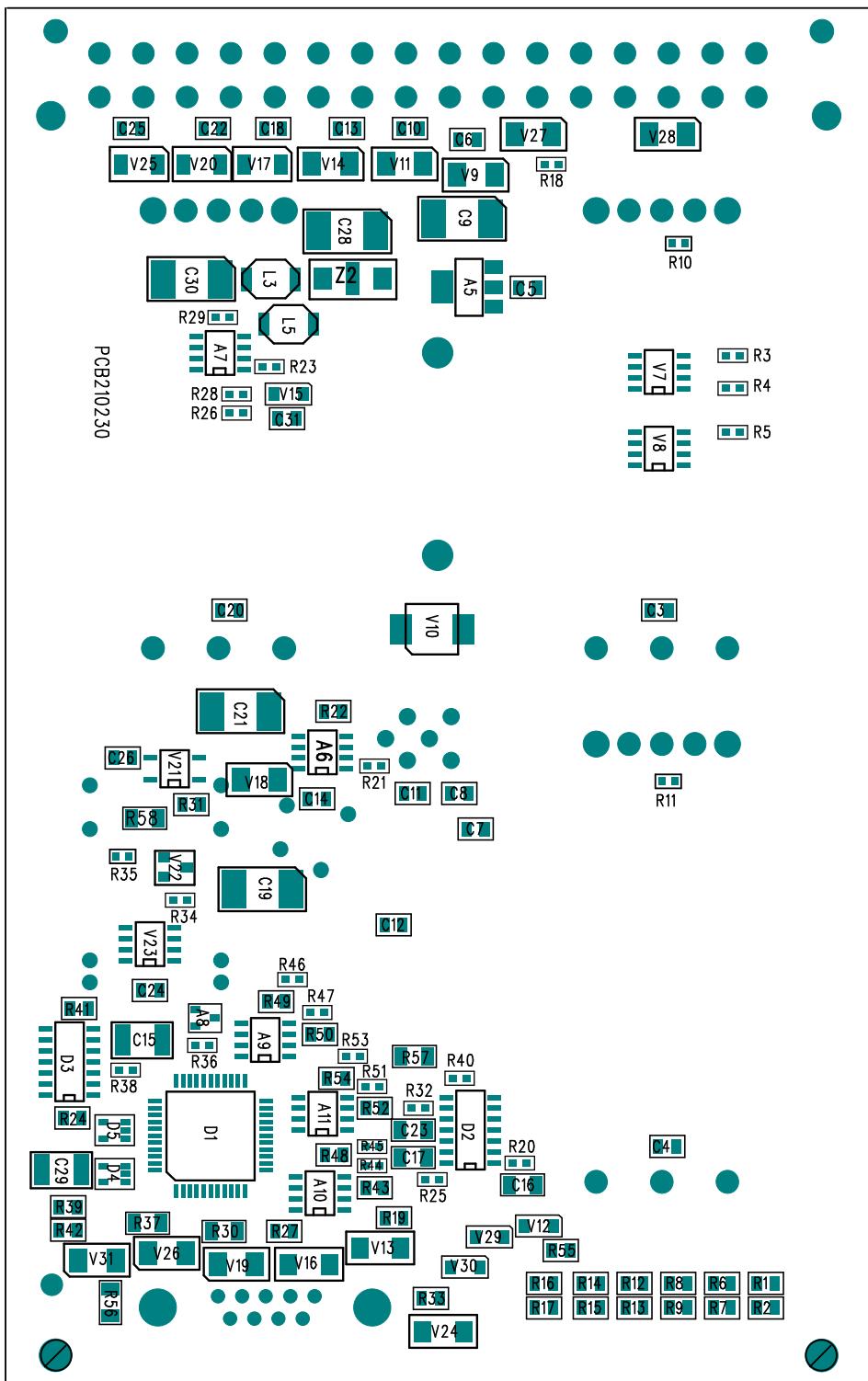


Figure 52 MWP312 Components Layout 2/2

4.5 AC Power Supply MWP411

The MWP411 AC Power Supply, an E1 size plug-in unit, is suitable to provide the feeding voltage for the MWP312 DC Power Supply Unit. MWP411 connects to the motherboard through a 32-pin Euro connector.



Figure 53 AC Power Supply MWP411

4.5.1 Operation

Input power is 100 ... 240 V AC line and output is 24V DC voltage. The total output power is 100 W (at +25 °C ambient temperature).

AC power is connected from a power cord via a filter plug X4 to a commercial, open frame switching AC/DC module. The output voltage is fed to the Euro connector.

The AC/DC module has no power switch - it operates continuously, if an appropriate mains input voltage is applied to the unit.

The module is protected against over loading. A tranzorb diode V1 protects the output against over and reverse voltages.

4.5.2 Technical Specifications MWP411

Table 54 MWP411 Technical Specifications

Property	Value/Description
Nominal Input Voltage	100 ... 240 V AC

Property	Value/Description
Input Voltage Range	80 ... 264 V AC
Frequency	47 ... 63 Hz
Input Current	1.9 A
Output	24 V DC, 4.2 A
Operating Temperature	0 +55°C
Storage Temperature	-40 +70°C
Humidity	Non-condensing
Dimensions	100(H), 160(D), 40(W) mm
Weight	0.4 kg

4.5.3 System Connector MWP411

- Connector: 32-pin, 2-row male power Euro connector
- Mating connector: 32-pin, 2-row female power Euro connector

Table 55 System Connectors

Pin	Row A		Row C	
	Signal	Description	Signal	Description
2	GND	Ground	GND	Ground
4				
6				
8				
10	+24V	Output Power +	+24V	Output Power +
12	0V	Output Power -	0V	Output Power -
14				
16				
18				
20				
22				
24				
26				
28				
30				
32	GND	Ground	GND	Ground

4.5.4 Parts List MWP411

Table 56 MWP411 Parts List

Part Number	Description	Qty
PCB210196	Printed Circuit Board	1
0946	Washer, serrated lock A4,3 DIN6798A A4	1
3939	Washer, spring lock B3 DIN127 A4	2
4337	Washer, spring lock B4 DIN127 A4	1
7067	Washer, spring lock B2,5 DIN127 A4	5
3050	Washer, flat A3, 2 DIN125 A4	5
211738	Screw, crosshead M2,5 x 6 DIN7985 PZ A4	2
211742	Screw, crosshead M2,5 x 12 DIN7985 PZ A4	4
211853	Screw, crosshead M4 x 12 DIN966 PZ A4	1
211854	Screw, crosshead M3 x 20 DIN966 PZ A4	2
223243	Screw, crosshead M2, 5 x 20 DIN7985 PZ A4	1
4776	Nut, hex M3 DIN934 A4	2
4812	Nut, hex M4 DIN934 A4	2
6779	Nut, hex M2, 5 DIN934 A4	5
5068	Screw-lock compound Loctite 222, 50ml	
240635	Filter, mains power IEC 3A 250 V AC, with wire leads	1
1780	Diode, transil 1N 6284 A / 1.5KE36A	1
1812	Connector, Euro D032MS-C1A-0,8/5	1
244970	Connector, pin 1 x 4, 3.96 mm, straight, SPOX, TH	1
244990	Connector, crimp housing 1 x 3 3.96 mm female SPOX	1
0172	Connector pin Ex E03096L02	1
DRW214089	Front Panel Assembly for MWP411	1
0840	Rivet 2.5 x 9.9 /Ms /Tin	2
16166	Plastic label	

Part Number	Description	Qty
MW45085	Flange for MWP411 mains filter	1
0760	Round sleeve spacer ENLIS 4 / 5.83.056	5
240634	Power supply 24 V DC / 4.2A 101.6x50.8 x 31.8 mm	1
4622	Cable mount D 5 mm, 9.5 mm black	2
0414	Ring terminal insulated 0.5-1.5 mm 2, M4, red	1
244992	Connector, crimp terminal 18-24 AWG, female, tin, SPOX	2
CBL210491	DC cable, internal MWP411 2 x housing and crimp terminals	1
DRW229559	Warning sticker, electric shock 55 x 25 mm	1
15223	Sticker set matt white, polyethylene	1
10948	Marking sticker OK46546	1

4.5.5 Diagrams and Board Layouts MWP411

Table 57 MWP411 AC Power Supply Illustrations

Code	Description
DRW214015	Circuit Diagram
DRW214016	Components Layout

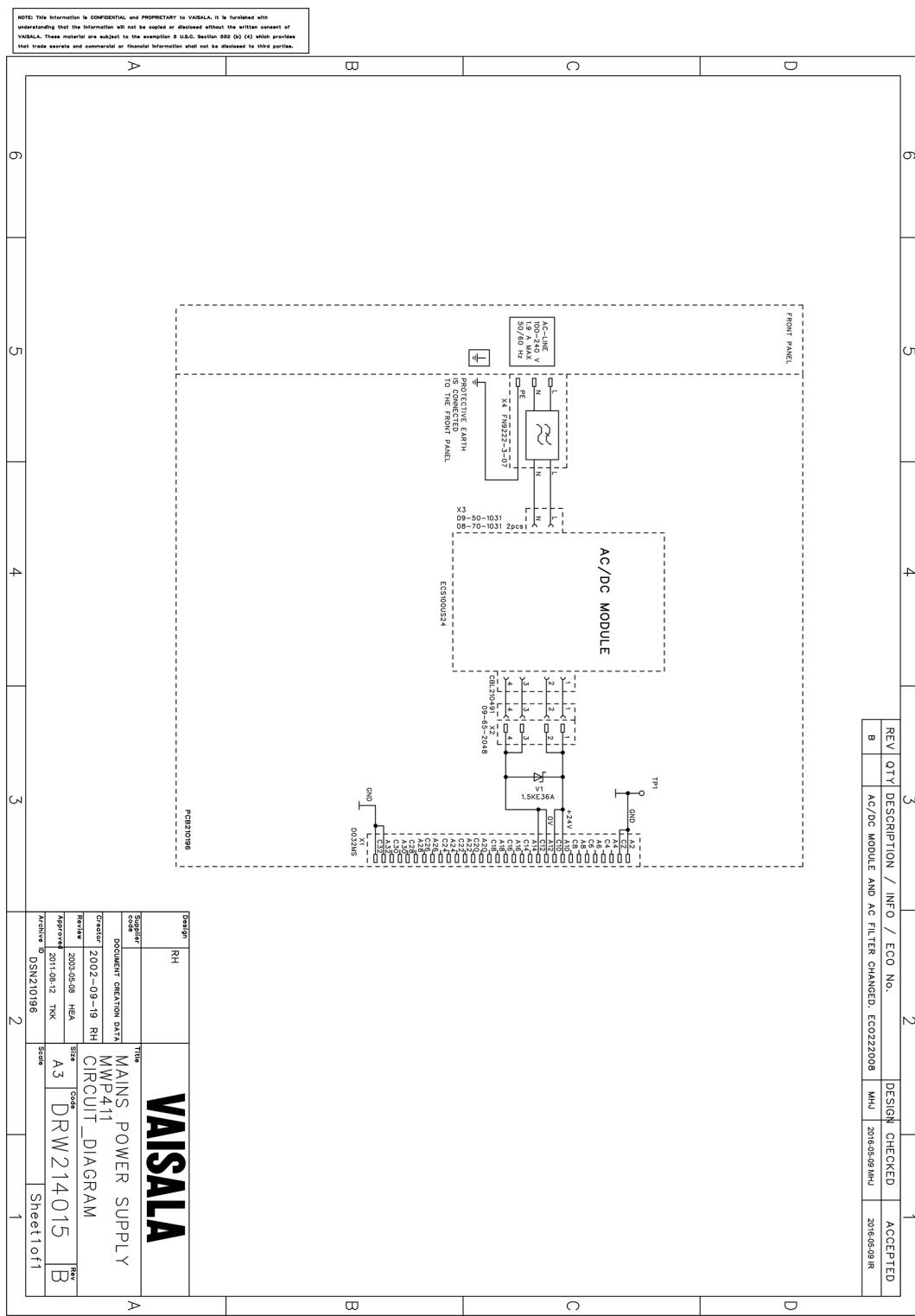


Figure 54 MWP411 Circuit Diagram

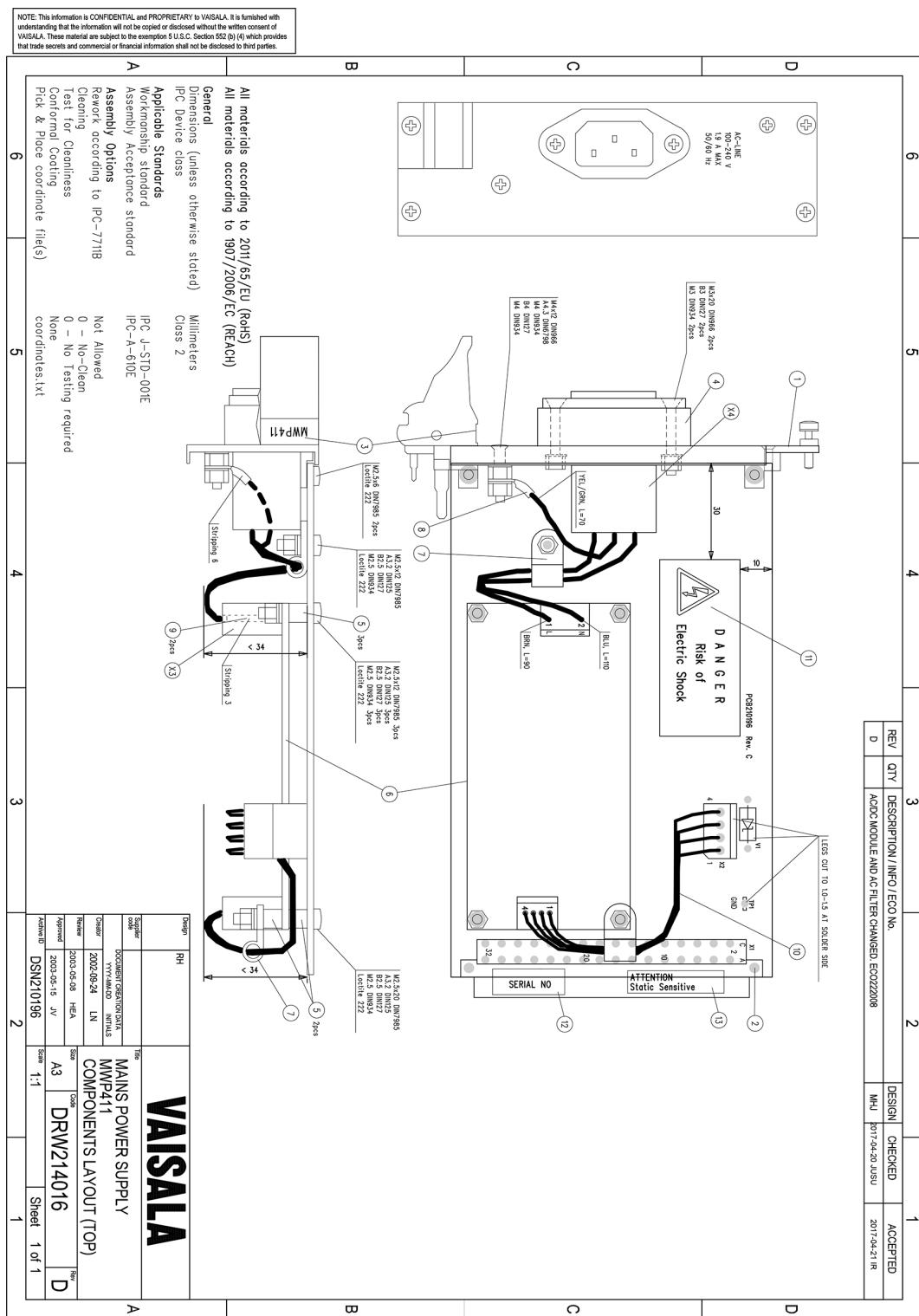


Figure 55 MWP411 Components Layout

5. Technical Data

5.1 Sounding Processing Subsystem Specifications

Table 58 Technical Specifications

Property	Description / Value
Dimensions	235 × 335 × 184 mm
Power consumption	70 W max.
Mains voltage nominal	100 ... 240 V AC
Mains frequency	50 / 60 Hz
DC power connection	19 ... 36 V DC, 60 W max.
Weight	7.5 kg max.
Cooling system	Forced air convection, three fans
UHF Connector	Coaxial N-type female
GPS Connector	Coaxial TNC-type female
VLF Connector	Coaxial C-type female
Antenna power	Antenna amplifiers are powered through antenna cables
Modulation	GFSK, GMSK, FM, FSK
Frequency range	400.15 ... 406 MHz
Sensitivity with RS41 and RS92 radiosondes	-120 dBm ¹⁾
Noise figure	<2.5 dB ¹⁾
Image rejection	70 dB ¹⁾
Spurious Free Dynamic Range with RS41 and RS92 radiosondes	90 dB ¹⁾
Third Order Intercept Point (IIP3)	0 dBm ¹⁾
Input impedance	50 Ohms
Environmental conditions	Indoor use
	Altitude up to 2000 meters
Operating temperature range	0 ... + 45° C
Operating humidity	10 ... 90 % RH (non-condensing)
Storage temperature	-55 ... + 70° C

Property	Description / Value
Storage humidity	5 ... 95 % RH

1) Specifications valid with Vaisala telemetry antennas

5.2 SPS341AG Spare Parts

Table 59 Spare Parts and Accessories

Code	Item
SPS341AGSPSET	Spare part set SPS341AG for DigiCORA System. Including: <ul style="list-style-type: none">• MRR111• MRP121• MPU121A• MWP312• MWP411
MRR111SP	400 MHz Receiver Unit
MRP121SP	Receiver Processor Unit
MPU121A	Main Processor Unit
MWP312SP	Power Supply Unit
MWP411SP	AC Power Supply Unit
Fuses:	
7048SP 5 AT, 10 pcs	
210704SP 2.0 AT, 10 pcs	
Other:	
DRW231652SP	Frame
212830SP	Fan

6. EU Declaration of Conformity

VAISALA

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EU DECLARATION OF CONFORMITY

Manufacturer: Vaisala Oyj
Post address: PL 26, FIN-00421 Helsinki
Street address: Vanha Nurmijärventie 21, Vantaa, Finland

This declaration of conformity is issued under the sole responsibility of the manufacturer.

Object of the declaration:

Vaisala Sounding Processor Subsystems;
SPS311, SPS311G, SPS311AG and SPS341AG

The object of the declaration described above is in conformity with Directives:

Low Voltage Directive (2014/35/EU)
Radio Equipment Directive (2014/53/EU)
RoHS-Directive (2011/65/EU)

The conformity is declared with using the following standards:

EN 61010-1:2010 Safety requirements for electrical equipment for measurement, control, and laboratory use – Part 1: General requirements

EN 61326-1:2013 EMC requirements - Immunity test requirements for equipment intended to be used in an industrial electromagnetic environment.

EN 61000-3-2:2014 Limits for harmonic current emissions

EN 61000-3-3:2013 Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems.

EN 50581:2012 Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Signed for and on behalf of:
Vantaa 2018-09-25

Jukka Lyömiö

.....

Jukka Lyömiö
Standards and Approvals Manager

Vaisala Oyj | PO Box 26, FI-00421 Helsinki, Finland
Phone +358 9 894 91 | Fax +358 9 8949 2227
Email firstname.lastname@vaisala.com | www.vaisala.com
Domicile Vantaa, Finland | VAT FI01244162 | Business ID 0124416-2

Appendix A. SPS341AG Plug-in Unit One-pagers

A.1. 400 MHz Receiver MRR111



Together with Receiver Processor Unit MRP111 and an external low-noise amplifier, 400 MHz Receiver Unit MRR111 builds up a digital radio receiver (software radio). MRR111 unit type is a Euro 1-sized (100 x 160 x 20 mm, weight 350 g) printed circuit board inside the Sounding Processing Subsystem chassis.

A.2. Receiver Processor MRP121A



Receiver Processor Unit MRP121A is used with a 400 MHz receiver unit to build up a digital radio receiver (software radio). MRP121A unit type is a Euro 1-sized (100 × 160 x 20 mm, weight 350 g) printed circuit board inside the Sounding Processing Subsystem chassis.

A.3. Main Processor Unit MPU121A



Main Processor Unit MPU121A is a computer unit intended for system control functions and external communication. MPU121A unit type is a Euro 1-sized (100 × 160 × 70.8 mm, weight 400 g) printed circuit board inside the Sounding Processing Subsystem chassis.

MPU121A contains operating system Windows 10 IoT Enterprise, build number 10240. As a new feature, Windows 10 contains a firewall. Windows 10 is the newest and the most secure operating system version. It is not possible to update the operating system.

MPU121A contains a module compatible with a 32-bit PC, running at the speed of 1.5 GHz with a 2GB-SODIMM memory. For program and data storage, MPU121 has 64-GByte Serial ATA (SATA) solid-state drive memory.

Vaisala application software in MPU121A is the same as in MPU121.

A.4. Power Supply MWP312



DC Power Supply Unit MWP312 provides DC operating voltages for the system. MWP312 unit type is a Euro 1-sized (100 x 160 x 20 mm, weight 400 g) printed circuit board inside the Sounding Processing Subsystem chassis.

A.5. AC Power Supply MWP411



AC Power Supply Unit MWP411 feeds DC voltage for MWP312 DC Power Supply Unit. MWP411 unit type is a Euro 1-sized (100 x 160 x 40 mm, weight 400 g) printed circuit board inside the Sounding Processing Subsystem chassis.

Technical Support



Contact Vaisala technical support at helpdesk@vaisala.com. Provide at least the following supporting information:

- Product name, model, and serial number
- Name and location of the installation site
- Name and contact information of a technical person who can provide further information on the problem

For more information, see www.vaisala.com/support.

Warranty

For standard warranty terms and conditions, see www.vaisala.com/warranty.

Please observe that any such warranty may not be valid in case of damage due to normal wear and tear, exceptional operating conditions, negligent handling or installation, or unauthorized modifications. Please see the applicable supply contract or Conditions of Sale for details of the warranty for each product.

Recycling



Recycle all applicable material.



Follow the statutory regulations for disposing of the product and packaging.

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www.vaisala.com

