

Technical Reference

Vaisala Sounding Processing Subsystem
SPS31G

VAISALA

PUBLISHED BY

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1. About this Document

1.1 Version Information

This manual provides technical reference information for Sounding Processing Subsystem SPS311G and its plug-in units. SPS311G is used as part of Vaisala sounding systems.

Instructions for updating the sounding processing subsystem software are included in *Vaisala DigiCORA Sounding System MW41 Technical Reference*. Instructions for connecting the sounding processing subsystem to the sounding system are included in *Vaisala DigiCORA Sounding System MW41 Getting Started Guide* and *AUTOSONDE AS15 Installing and Configuring Software Technical Reference*.

Table 1 Manual Revisions

Manual Code	Description
M211596EN-D	January 2019. Figure updates. Updated Sounding Processing Subsystem name SPS311 into SPS311G.
M211596EN-C	April 2017. Updated information on MWP411.
M211596EN-B	February 2016. Updated information on grounding.
M211596EN-A	June 2013. First version. This document combines the information that was previously split into several different manuals: <ul style="list-style-type: none"> • Technical Reference for SPS311 M210651EN • Technical Reference for MRR111 M210643EN • Technical Reference for MRP111 M210620EN • Technical Reference for MWP312 M210644EN • Technical Reference for MWP411 M210645EN Information on MRG114 is new.

1.2 Related Manuals

Table 2 Related Manuals

Manual Code	Manual Name
M211429EN	<i>Vaisala DigiCORA Sounding System MW41 Getting Started Guide</i>
M211415EN	<i>Vaisala DigiCORA Sounding System MW41 Technical Reference</i>
M211730EN	<i>AUTOSONDE AS15 User Guide</i>
M211731EN	<i>AUTOSONDE AS15 Installing and Configuring Software Technical Reference</i>

1.3 Documentation Conventions



WARNING! **Warning** alerts you to a serious hazard. If you do not read and follow instructions carefully at this point, there is a risk of injury or even death.



CAUTION! **Caution** warns you of a potential hazard. If you do not read and follow instructions carefully at this point, the product could be damaged or important data could be lost.



Note highlights important information on using the product.



Tip gives information for using the product more efficiently.



Lists tools needed to perform the task.



Indicates that you need to take some notes during the task.

1.4 Trademarks

DigiCORA® is a registered trademark of Vaisala Oyj.

Microsoft® is either a registered trademark or trademark of Microsoft Corporation in the United States and other countries.

All other product or company names that may be mentioned in this publication are trade names, trademarks, or registered trademarks of their respective owners.

1.5 Safety

The product delivered to you has been tested for safety and approved as shipped from the factory. Note the following precautions:



WARNING! If the equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.



WARNING! Do not replace the detachable main supply cord with an inadequately rated cord.



WARNING! The equipment must be connected to an earthed mains socket outlet.
FI: VAROITUS: Laite on liitettävä suojakoskettimilla varustettuun pistorasiaan.
DA: ADVARSEL: Apparatet må tilkoples jordet stikkontakt.
SE: VARNING: Apparaten skall anslutas till jordat uttag.



CAUTION! Do not modify the unit. Improper modification can damage the product or lead to malfunction.

1.6 ESD Protection

Electrostatic Discharge (ESD) can cause immediate or latent damage to electronic circuits. Vaisala products are adequately protected against ESD for their intended use. It is possible to damage the product, however, by delivering electrostatic discharges when touching, removing, or inserting any objects inside the equipment housing.

To make sure you are not delivering high static voltages yourself:

- Handle ESD sensitive components on a properly grounded and protected ESD workbench.
- When an ESD workbench is not available, ground yourself to the equipment chassis with a wrist strap and a resistive connection cord.
- If you are unable to take either of the above precautions, touch a conductive part of the equipment chassis with your other hand before touching ESD sensitive components.
- Always hold component boards by the edges and avoid touching the component contacts.

2. Product Overview

2.1 Introduction to SPS311G

Vaisala Sounding Processing Subsystem SPS311G is a subsystem for Vaisala sounding systems. It consists of a front panel, a chassis, plug-in units and a connector panel.



Figure 1 Vaisala Sounding Processing Subsystem SPS311G

2.2 Front Panel

The power control switch and the system indicator LEDs are located on the front panel. The power control dip switches are located on the backside of the front panel.

2.2.1 Power Control Switch

The power of the subsystem can be switched on and off from the power control switch located on lower left corner of the front panel.

2.2.2 Indicator LEDs

The standby and power/status indicator LEDs are located on lower left corner of the front panel beside the power control switch.

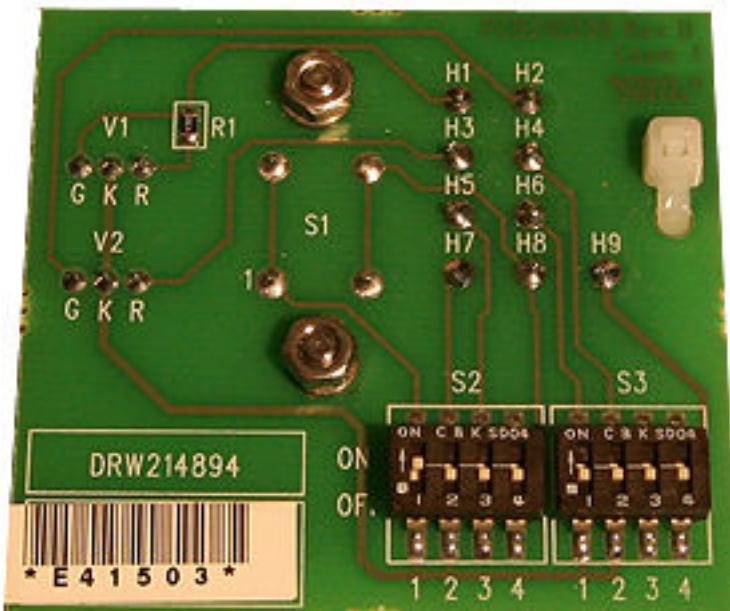
The status of the subsystem is indicated by the two LEDs as explained in [Table 3 \(page 12\)](#):

Table 3 Indicator LED Colors

Standby LED Color	Power/Status LED Color	System Status
Blank	Blank	Power is not applied
Yellow	Blank	Power is applied
Blank	Blinking green	Powering up
Blank	Green	Ready for operation
Blank	Red	Unit failure during power-up or operation, failure in network connection

2.2.3 Power Control Dip Switches

The functionality of the power switch can be configured using the eight DIP switches located behind the front panel, see [Figure 2 \(page 12\)](#).

**Figure 2 Power Control DIP Switches****Table 4 Power DIP Switches Default Setting**

Switch No.	Default Setting	Description
S2-1	ON	Signal PTOGGLE1#. When the front power switch is pushed, the PTOGGLE1# signal is set to Low. The unit is then switched ON by the power control logic. If the setting is OFF, the front power switch is disabled. This option is useful for AUTOSONDE and remote use.

Switch No.	Default Setting	Description
S2-2	OFF	Signal PON#. Remote PON# functions normally. Remote control capability is available with the Power CTRL connector. If the setting is ON, the unit is always on. This option is useful for AUTOSONDE use. The unit is switched on automatically after a blackout.
S2-3	OFF	Signal POFF#. Remote POFF# functions normally. Remote control capability is available with the Power CTRL connector. If the setting is ON, and S2-1 and S2-2 are ON, the unit is always on. Pushing the front power switch resets the unit.
S2-4	OFF	Not used.
S3-1	OFF	Signal RACK0#. S3-1 and S3-2 can be used to identify the units, if multiple units are used. See Table 5 (page 13) .
S3-2	OFF	Signal RACK1#. S3-1 and S3-2 can be used to identify the units, if multiple units are used. See Table 5 (page 13) .
S3-3	OFF	Not used.
S3-4	OFF	Not used.

Rack address is a binary number formed from signals RACK1# and RACK0#, where RACK1# is MSB (most significant bit) and RACK0# is LSB (least significant bit).

Table 5 Rack Identification

DIP Settings	Rack Address
S3-1 OFF, S3-2 OFF	00
S3-1 ON, S3-2 OFF	01
S3-1 OFF, S3-2 ON	10
S3-1 ON, S3-2 ON	11

2.3 Frame and Plug-in Units



WARNING! Make sure the SPS311G power cable is grounded.

2.3.1 Unit Slots

The chassis contains a card frame with nine slots for the plug-in units, motherboard, and an I/O extension board. The slots are numbered from left to right (front view) with numbers 1 to 9. The figure below shows you the plug-in units inside the chassis.

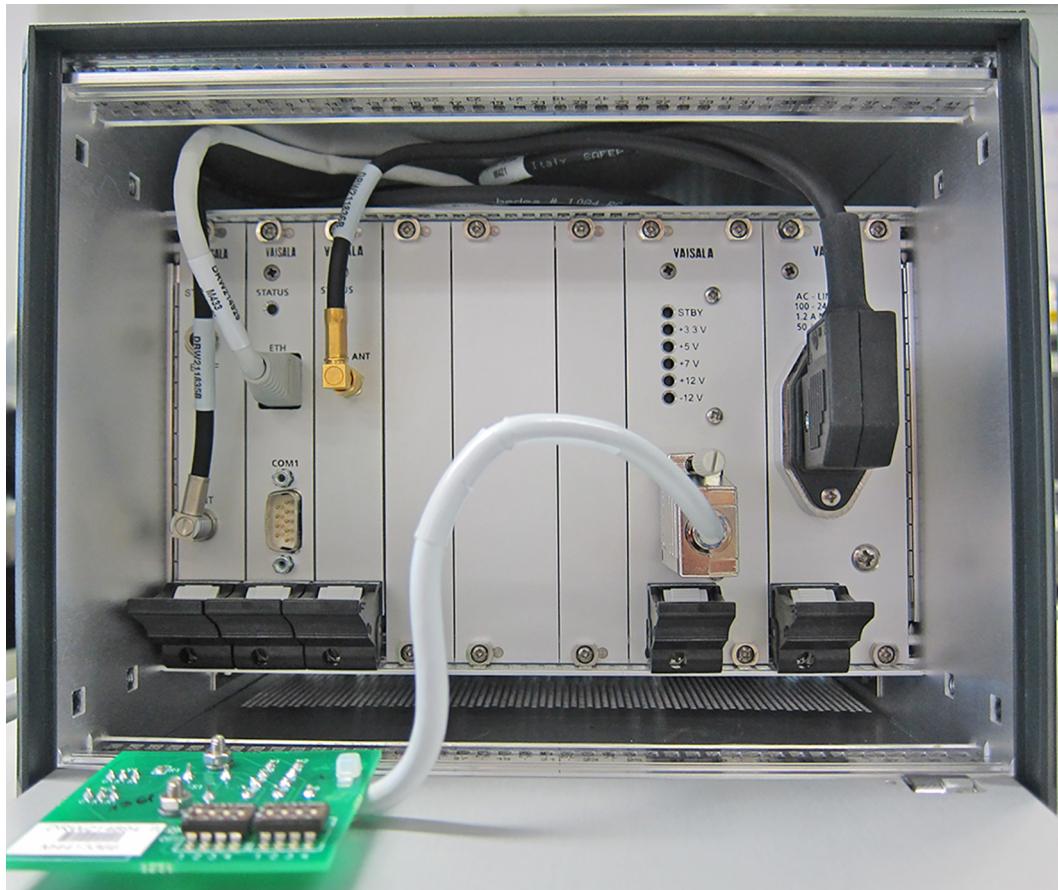


Figure 3 Plug-in Units inside the Chassis

2.3.2 Motherboard

The operating voltages as well as signal connections between different units are carried through the motherboard. The motherboard is fully passive. It does not contain any active electronic or electromechanical components.

2.3.3 I/O Extension Board

The I/O extension board is a printed circuit board which connects the I/O signals between the motherboard and the I/O connectors.

Signals to the connector panel are fed through an extension board connector on the back side of the motherboard.

2.3.4 Connector Panel

The connector panel at the back has connectors for antenna signals, LAN, I/O signals, and power.

The panel includes I/O connectors, a printed circuit board which connects the I/O signals between the connector board, and an I/O extension board.

Antenna signals and LAN are connected to the plug-in units via cables and the power inputs are wired from the connector to the motherboard. See [Table 6 \(page 15\)](#) for details.

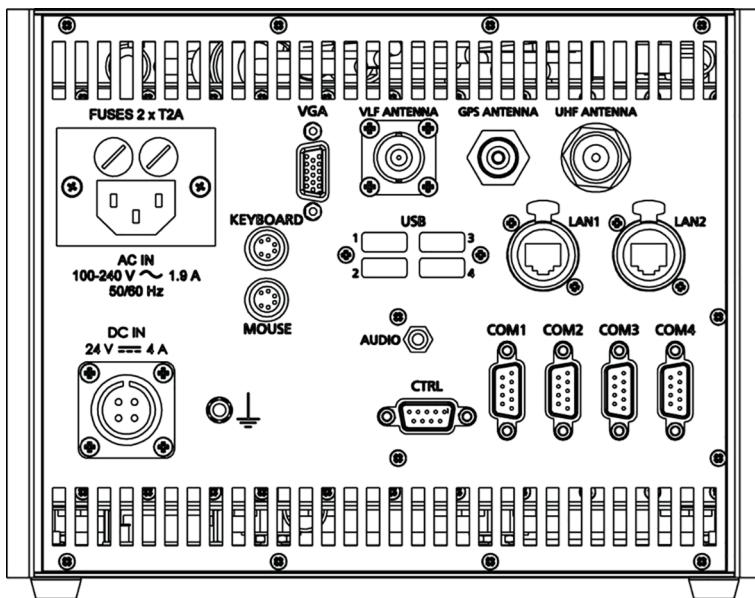


Figure 4 Power, Signal, and I/O Connectors in the Connector Panel

Table 6 Connector Panel Connectors

Connector	Description	Note
AC IN	Mains power connector	
DC IN	DC power connector	
UHF ANTENNA	UHF antenna connector	
GPS ANTENNA	GPS antenna connector	
VLF ANTENNA	VLF antenna connector	Not used
LAN1	LAN connector	
LAN2	LAN connector	For future use
CTRL	Control	
COM1	COM1	For future use
COM2	COM2	For future use
COM3	COM3	For future use
COM4	COM4	For future use
VGA	VGA display	For future use
KEYBOARD	Keyboard	Not used
MOUSE	Pointing device	Not used

Connector	Description	Note
USB1...4	Universal Serial Bus	For future use
AUDIO	Speakers	For future use

2.3.4.1 AC In

Connector type:

IEC power inlet with fuse holder (Shurter 0040.5001.2)

2.3.4.2 DC In

Connector type:

Glenair MIL-C-5015, 4-socket, shell size 14, IT3102A14S-2SF7

Table 7 DC In Connections

Pin	Signal	Note
A	+VDC input (+24 V)	
B	- VDC input	
C		
D		

2.3.4.3 UHF Antenna

Connector type:

Coaxial N female



+12 VDC power is supplied to the antenna.

2.3.4.4 GPS Antenna

Connector type:

Coaxial TNC female



+5 VDC power is supplied to the antenna.

2.3.4.5 LAN1

Connector type:

RJ-45 Connector (Neutrik NE8FAV)

Table 8 LAN Connections

Pin	Signal	Note
1	Transmit data +	
2	Transmit data -	
3	Receive data +	
4		
5		
6	Receive data -	
7		
8		

2.3.4.6 CTRL

Connector type:

9 pin D female

Table 9 CTRL Connections

Pin	Signal	Note
1	+12V	Power out
2	StartIn	For future use
3	StartOut	For future use
4	POFF#	Power control
5	GND	Ground
6	RES#	System reset
7	PON#	Power Control
8	TEST#	For future use
9	PTOGGLE#	Power control

3. Maintenance

3.1 Sounding Processing Subsystem Maintenance

SPS311G does not need any regular maintenance.

At higher operating temperatures, regular checking of the operation of the cooling fan is recommended.

In all maintenance work, remember to proceed in accordance with electrical safety regulations.



WARNING! Switch the subsystem POWER OFF before replacing any plug-in units. Unplug the mains connector before replacing the AC power supply MWP411. Switch External 24 VDC supply OFF before replacing the DC power supply MWP312.



CAUTION! To avoid damaging the front panel hinges, always open the front panel so that it is supported on a flat surface.

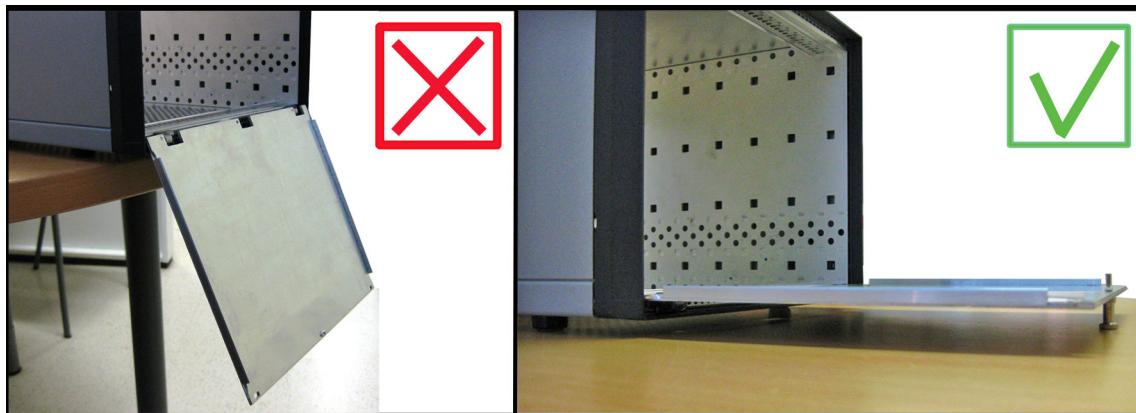


Figure 5 Opening the Front Panel

3.2 Replacing Fuses

Check the fuses in case power is connected to the subsystem, but the standby LED light on the front panel remains blank. There are three user-replaceable fuses in the system: two in connection with the AC power inlet and one in DC Power Supply MWP312.

The two fuses in connection with the AC power inlet are located in fuse holders in the connector panel. The fuse is a glass tube 5 × 20 mm, slow blow T2A/250VAC.

The MWP312 fuse is located in a hole in the middle of the cooling plate of the unit. The fuse is a glass tube 5 × 20 mm, slow blow T5A/250VAC.



You need a flat-head screwdriver to perform this maintenance procedure.

3.2.1 Replacing AC Power Inlet Fuses

- ▶ 1. Open the two adjacent fuse holders using a flat-head screwdriver or a coin.



Figure 6 Opening the AC Power Inlet Fuse Holder

- 2. Remove the fuse from the holder with your fingers.

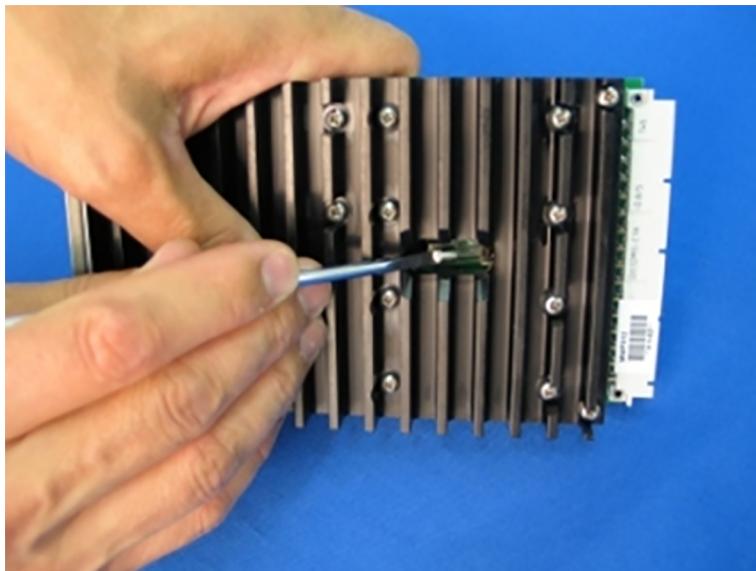


Figure 7 Removing the AC Power Inlet Fuses

- 3. Replace the fuses if needed.
- 4. Close the fuse holder with the screwdriver.

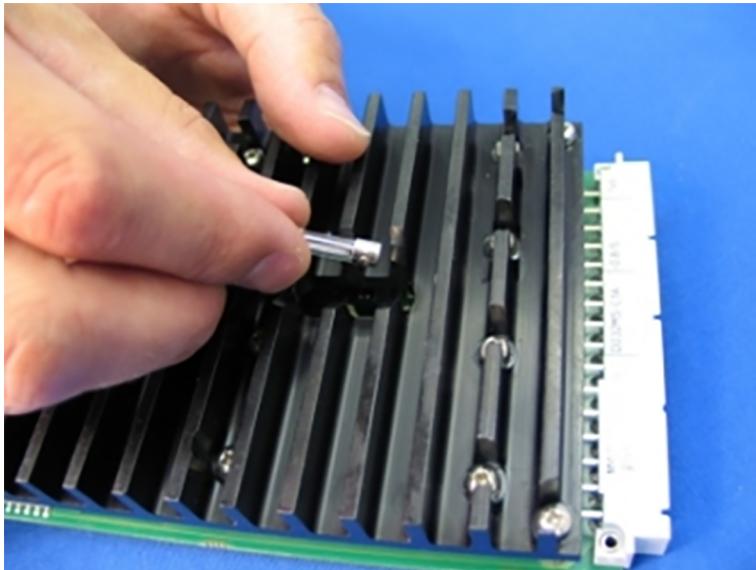
3.2.2 Replacing DC Power Unit Fuses

- ▶ 1. Remove the MWP312 unit as instructed in section [Replacing Plug-in Units \(page 22\)](#).
The fuse is located in a small hole in the middle of the cooling plate of the unit.
- 2. Lift the other end of the fuse carefully with the tip of the screwdriver and remove it with your fingers.



- 3. Replace the fuse if needed.

4. Install the fuse by dropping it carefully to the fuse holder and pressing it to its place.



5. Install the MWP312 unit as instructed in section [Replacing Plug-in Units \(page 22\)](#).

3.3 Replacing Plug-in Units

In the event of a fault, it is possible to replace the plug-in units in the field.



WARNING! Switch SPS311G POWER OFF before replacing any plug-in units.
Unplug the mains connector before replacing the AC power supply MWP411.
Switch External 24 VDC supply OFF before replacing the DC power supply MWP312.

To remove a unit:

- Disconnect the unit cable in the front panel.
- Open the upper and lower attachment screws.
- Push first the handle lock button to release the latch and then push the whole handle down to unplug the unit.
- Pull out the unit.

To install a unit:

- Place the unit into lower and upper card slide rails in the correct card slot.
- Unlock the handle latch and push the unit almost completely into the slot.
- Finally, lift the handle up to complete the push until the card is fully in the slot and the handle latch is locked.
- Fasten the attachment screws.
- Connect the cable.



CAUTION! Do not damage the EMC strips in the front panel of the unit or in the adjacent front/blank panel when pulling out or pushing in a plug-in unit. Move the unit slowly in the card guides and avoid bending them.

3.4 Checking the Operation of Cooling Fans

There are three fans on the lower part of the chassis.

- ▶ 1. For a rough check:
 - a. Switch the subsystem power off and back on.
 - b. Check if you can hear the noise of the fans when power is on.
- 2. For a thorough check:
 - a. Remove all plug-in units except MWP312.
 - b. Connect the subsystem to 24 VDC power system using the 24 VDC input in the connector panel.
 - c. Check the air flow in the empty slots to see if the fans work.

4. Plug-in Unit Descriptions

4.1 400 MHz Receiver MRR111

400 MHz Receiver MRR111 is a Euro 1-sized (160 mm × 100 mm) unit. Together with Receiver Processor MRP111 and an external low-noise amplifier it builds up a digital radio receiver. The main emphasis on the design of this radio receiver has been on improving spurious free dynamic range and sensitivity over its predecessors.



Figure 8 Receiver MRR111

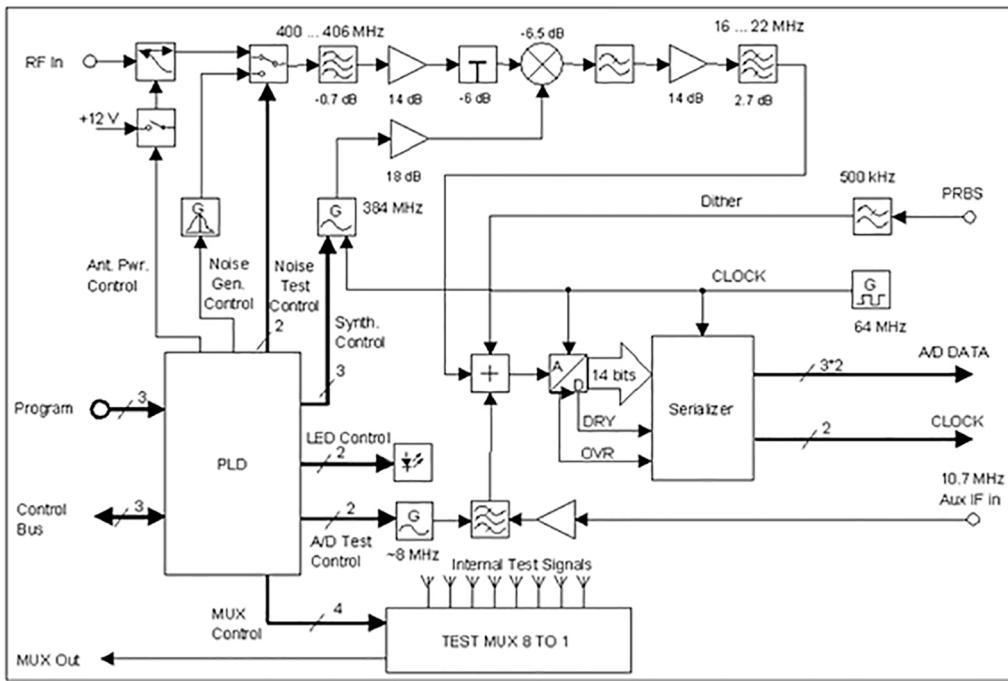


Figure 9 MRR111 Block Diagram

MRR111 performs a down conversion for the signal entering the RF input connector and translates the whole meteorological frequency band 400 ... 406 MHz to an intermediate frequency band 16 ... 22 MHz. The down conversion is carried out by a high-level diode mixer driven by a synthesized 384-MHz local oscillator. The IF signal is then sampled by a high-performance 14-bit analog to digital converter using a sampling rate of 64 Msamples / s. This “block down conversion” enables simultaneous multi-channel (multi-sonde) reception using multiple digital down converters and a common RF front end.

An external 10.7 MHz IF signal can also be fed to the A / D converter using connector “Ext IF In” on the front panel. It is possible to use this input simultaneously with normal 400 MHz reception.

The output signals from the A / D converter are transformed into serial format and fed via three 448 Mbit/s symmetric lines to MRP111 for further processing. The last down conversion, filtering, and signal demodulation are performed digitally in MRP111.

A crystal oscillator module with high spectral purity (low jitter) provides the 64-MHz sampling clock and also the reference signal for the 384-MHz local oscillator synthesizer.

For testing purposes, an onboard noise generator and test oscillator with associated electronic switches are provided.

All functions of the unit are controlled by Radio Processor MRP111 via a three-line serial control bus.

4.1.1 RF Section

The RF signal enters MRR111 through connector X8 (ANT) at the front panel. The signal is routed through a solid state RF switch A11 (UPG2009TB) to the RF filter. The purpose of the switch is to select either input signal or noise from the onboard noise source to the receiver (see section [Noise Test Circuitry \(page 33\)](#)). The antenna input signal is coupled to the RF section when logic 0 is applied to NTEST+ and logic 1 to NTEST-.

RF filter Z7 is a ceramic coaxial filter with three resonators and has a -3 dB pass band of 15 MHz centered at 403 MHz.

The filter is followed by an RF amplifier stage which consists of a monolithic wideband amplifier A7 (SGA-6289). It provides 14 dB of gain and a high dynamic range due to its low noise figure and high third order intercept point.

A simple LC-filter consisting of C74, C60, L14 and C55 at the output of the amplifier forms a band rejecting (notch) filter at 364 MHz. It increases the image rejection of the receiver and also prevents the image frequency noise of the amplifier to reach the down converter.

A resistive 6 dB attenuator formed by R48, R53, and R56 provides a good wideband impedance matching between the RF amplifier and mixer. It also increases the third order intercept point of the receiver without increasing the noise figure of the receiver too much.

The output signal of the RF amplifier is available for measurements at a test point with MMCX connector X6 (RF). When loaded with a 50-ohm impedance it provides 20.8 dB of attenuation.

A typical frequency response of the RF section measured from test point X6 is shown in the figure below.

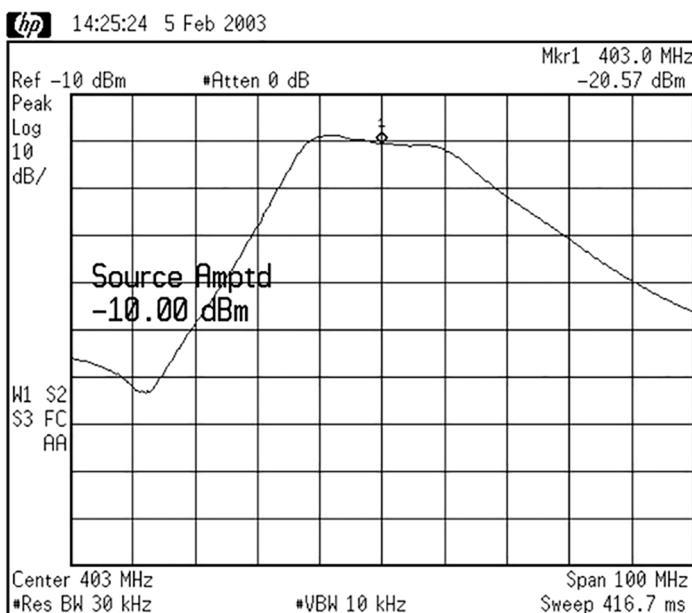


Figure 10 RF Response

4.1.2 Down Conversion

The RF signal at 400 ... 406 MHz is converted to an intermediate frequency (IF) at 16 ... 22 MHz. The down conversion is done using a fixed local oscillator frequency of 384 MHz. A double-balanced diode ring mixer A6 (SYM-18H) operates as a down converter. Due to its high local oscillator drive level (17 dBm), it has a high third order intercept point resulting in a good dynamic range with low intermodulation products.

The output signal from the mixer is fed to the IF amplifier through an LC low pass filter formed by L11, C37 and L10. Its -3 dB cut off frequency is 37 MHz and it prevents the unwanted high-frequency components from the mixer to reach the IF amplifier.

The LCR network consisting of C48, L9 and R42 compensates for the inductive input impedance of the low pass filter at high frequencies and provides a good wide-band impedance match for the IF port of the mixer.

The output signal of the down converter is available for measurements at a test point with MMCX connector X4 (IF AMP). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

4.1.3 IF Section

The IF signal from the down converter is fed to a monolithic wideband amplifier A2 (SGA-6289). It provides 14 dB of gain and a high dynamic range due to its low noise figure and high third order intercept point.

The amplifier is followed by an LC band pass filter with three sections. The pass band of the filter is flat within ± 0.5 dB between 15 ... 22 MHz. The -3dB points are at 13 and 24 MHz. The three resonant circuits of the filter are tunable by trimmer capacitors C26, C40, and C61. The coupling between resonators is capacitive and fixed. The termination impedances of the filter are different, input 50 ohms and output 100 ohms, which produces about 2 dB of voltage gain including filter losses.

The output signal of the IF section is available for measurements at a test point with MMCX connector X7 (IF). When loaded with a 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

Typical frequency responses of the combined RF and IF sections measured from RF input to test point X7 is shown in the two figures below.

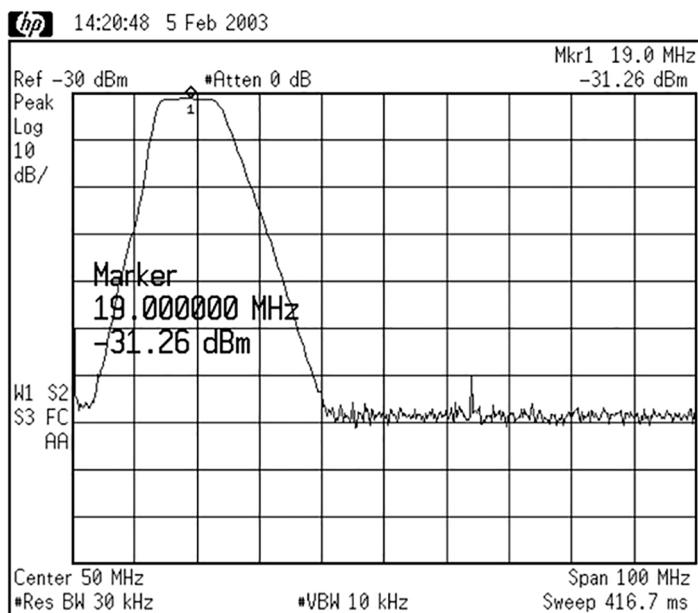


Figure 11 IF Response, Wide Span

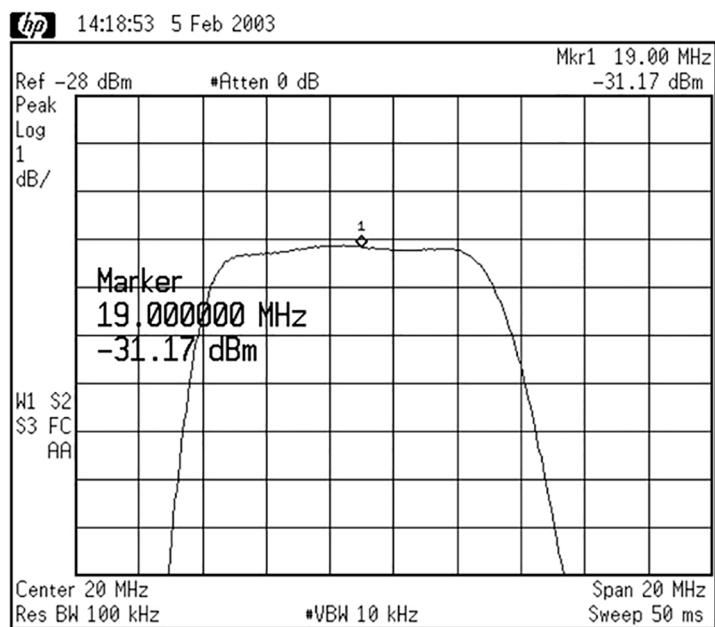


Figure 12 IF Response, Narrow Span

4.1.4 Analog to Digital Conversion

The analog to digital conversion is carried out by a high-performance 14-bit ADC A5 (AD6645). It has symmetrical (differential) inputs for both analog input and sampling clock signals to minimize cross talk. The analog input range is ± 1.1 V. The digital output is parallel, consisting of 14 bits (D0 ... D13), data ready (DRY) and over range (OVR). The output data is in twos complement format.

The signal coming from the IF section is first balanced by transformer T2 (ADTT4-1), which also steps up the voltage by two. The IF signal entering to the ADC can be measured from test connector X7 (IF). When loaded with a 50-ohm impedance it provides 23.9 dB of voltage attenuation compared to the actual voltage at the signal input of A5. Thus full scale voltage (2.2 Vp-p) equals to -13.1 dBm at X7.

The sampling frequency is 64 MHz and it originates from crystal oscillator Z2 (QEN60-AHR 64 MHz DT50). The sampling signal is at first balanced by transformer T1 (ADTT4-1) which also steps up the voltage by two. Then the sampling signal is clipped by two antiparallel coupled diodes V3 (BAV99) to limit the amplitude and retain the slew rate high at zero crossings.

The spurious signals generated by the small non-linearities and internal glitches of the ADC are attenuated by using a dither signal. It is a noise-like signal added to the analog input signal and located at a lower frequency than the signals of interest. It has a suitable (quite low) amplitude to linearize the ADC. The dither signal is a digital pseudo random signal generated in Receiver Processor MRP111 and fed to MRR111 via pin A4 of the card edge connector X1. The dither input signal is filtered with a two-section LC low pass filter (L1, C3, C4, L6 and C80) which has a cut off frequency of about 500 kHz to remove all spectral components from the IF signal range. The dither signal is attenuated to a suitable level by a series resistor (R59), which sums the dither signal to the output signal from the IF filter.

The 16 outputs of the ADC are fed to a parallel-to-serial converting device D1 (65LVDS95) through series resistors located at the close vicinity of the ADC to reduce noise generating capacitive load currents. The P-to-S converter has 21 inputs for parallel data and one for clock signal. The remaining five inputs are connected to either ground or +3.3 V supply for diagnostic purposes. It has three symmetrical (balanced) data outputs and one symmetrical clock output. The clock signal input frequency is multiplied by 7 using an internal phase locked loop frequency synthesizer. With the 64-MHz input clock frequency coming from crystal oscillator Z2, the P-to-S converter generates an internal clock frequency of 448 MHz, which is used as a clock for the three serial outputs. Thus the data rate at the serial outputs is 448 Mbit/s. These output signals and the clock signal are transmitted to Receiver Processor MRP111 via the card edge connector X1. The frequency of the output clock line is still 64 MHz.

To provide a noise-free supply voltage for the sensitive parts of the ADC and crystal oscillator, a special analog +5 V is provided by IC regulator A12 (MIC2920A-5.0BS) from the +7 V supply line.

4.1.5 Local Oscillator

The 384-MHz local oscillator signal for the down converter is generated by a phase-locked loop frequency synthesizer. Its core is an integrated circuit A10 (ADF4112BRU) which contains the phase detector, the prescaler, the programmable counters and the control logic for a dual modulus synthesizer. The loop filter and the voltage-controlled oscillator (VCO) are external.

ADF4112BRU is a very versatile circuit with many externally programmable parameters that are controlled via a three-line serial bus (LE, DATA and CLK). Among other parameters the division ratios of the internal counters are set as follows: R = 4 (reference counter), P = 8/9 (prescaler), B = 3 (N counter) and A = 0 (N counter swallow). With these settings the synthesizer multiplies the reference frequency (16 MHz) by 24 and produces 384 MHz. For diagnostic purposes, the ADF4112BRU contains a multiplexer through which several internal signals can be connected to one output (MUX) for monitoring. Normally the internal digital lock detector is chosen to this output. Details of the operation of ADF4112BRU can be found from its data sheet and MRR111 Control Functions Specification.

Reference frequency for the synthesizer is taken from the 64-MHz crystal oscillator Z2 and divided by four in the internal reference counter of A10 to obtain a reference frequency of 16 MHz for the phase detector. The output signal of the 64 MHz crystal oscillator is available for measurements at a test point with MMCX connector X2 (64 MHz). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

The loop filter is passive for the lowest possible phase noise and is comprised of R77, C91, R82, C118, R87, and input capacitance of A9. It sets for its part the loop band width to almost 300 kHz to efficiently reduce the phase noise at frequencies close to the center frequency.

VCO is a low-phase noise oscillator module A9 (VCO190-370T) which has a tuning range of 340 ... 400 MHz and a typical output level of +1 dBm. The output signal of the VCO is amplified by a monolithic wideband amplifier A8 (SGA-6489). It provides 20 dB of gain and enough power (18 dBm) to drive the local oscillator input of the high level mixer A6.

The output signal of the local oscillator is available for measurements at a test point with MMCX connector X5 (LO). When loaded with a 50-ohm impedance, it provides 20.8 dB of attenuation.

To provide a noise-free supply voltage for the sensitive parts of the synthesizer (especially VCO and phase detector), a special analog +5 V is provided by IC regulator A12 (MIC2920A-5.0BS) from the +7 V supply line.

4.1.5.1 External IF

MRR111 is equipped with an input for external IF to facilitate using the receiver with an external front end having 10.7 MHz IF output.

The IF signal entering connector X3 (EXT IF 10.7 MHz) is first scaled down with an attenuator formed by resistors R3, R4, and R5. With original resistance values the attenuation is 18.5 dB and the maximum input level is 0 dBm. Attenuation can easily be modified according to the signal level to be applied.

The attenuated input signal is fed to a monolithic wideband amplifier A4 (MAR-6SM) through selection switch A3 (uPG2009TB). The amplifier provides 20 dB of gain. The signal from EXT IF input is connected to the amplifier when a logic 0 is present at ADTEST+ and logic 1 at ADTEST-.

The amplifier is followed by an LC band pass filter formed by C57, L13, and C43. Its passband is 4 ... 11 MHz between -3 dB points. The output signal of the filter is summed with the so-called dither signal coming from a low-pass filter through resistor R59. This sum signal is then combined to the main IF signal through LC tank circuit L15 and C67. Due to this arrangement, no selection switches are needed and, furthermore, it is possible to use the external IF input simultaneously with normal receiver operation.

The output signal of the IF section is available for measurements at a test point with MMCX connector X7 (IF). When loaded with 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

A typical frequency response measured from the EXT IF input to test point X7 is shown in the figure below.

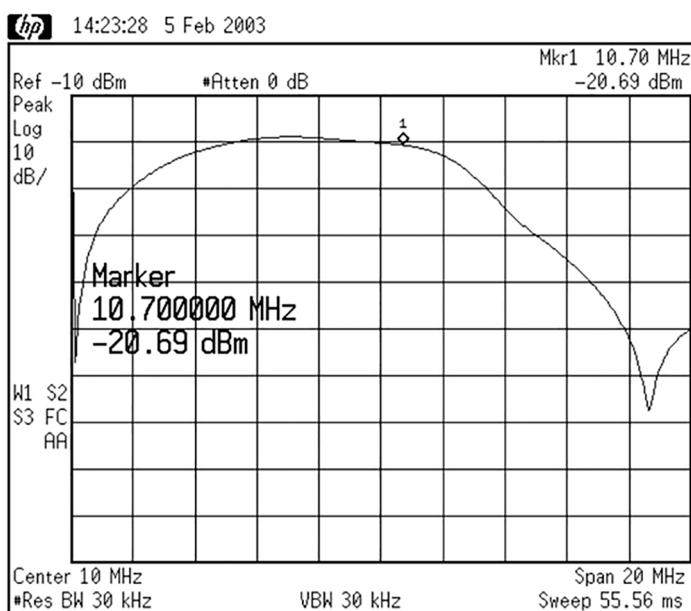


Figure 13 Ext If Response

4.1.6 ADC Test Circuitry

A test signal for verifying the operation of the analog to digital converter can be generated with an onboard oscillator. The EXT IF amplifier and filter are also utilized for this purpose by applying positive feedback to the input of amplifier A4 to get the circuit to oscillate.

Feedback is taken from the output of the filter via a loaded series resonant circuit (C35, R24, and L7) and connected to the amplifier input through selection switch A3. The test signal is set on by applying a logic 1 to ADTEST+ and logic 0 to ADTEST-.

This test oscillator generates a low distortion signal at about 6.5 MHz with an amplitude that is between half scale and full scale voltage of the ADC. Using this signal it is possible to check that all outputs of the ADC are active and also verify its linearity when a Fourier analysis is performed to the signal and levels of its harmonics are measured.

The output signal of the test oscillator is available for measurements at a test point with MMCX connector X7 (IF). When loaded with a 50-ohm impedance, it provides 17.9 dB of voltage attenuation.

4.1.7 Noise Test Circuitry

An onboard noise source is provided for verifying that the receiver is functioning normally.

Noise diode V6 (ST-2) produces wideband noise when reverse biased over its breakdown voltage and current limited to a suitable value. The bias current is switched on and off by transistor V2 (SST3904). The noise generator is switched on when NGEN- is at logic 0.

RF switch A11 (uPG2009TB) selects signal either from the antenna input connector or from the noise generator to the receiver RF section. When a logic 1 is applied to NTEST+ and a logic 0 to NTEST- the noise source is coupled to the receiver input.

4.1.8 Power Feed to Antenna

Power and control signal to an external low noise amplifier (LNA) and antenna selection switch is applied through the antenna input connector.

To prevent extra noise from entering the receiver input, the power is fed to the antenna cable through an LC low-pass filter (C77, L17, and C88) followed by a tank circuit (L21 and C95) resonating at 403 MHz.

The power feed is controlled by an intelligent power switch IC A1 (L6377D) that also contains all necessary safety features such as an adjustable current limit with power saving pulsed operation and over temperature protection. A diagnostic output is available, indicating the operating status of the circuit. Power to the antenna line is switched on and off with control signal ANTPWR applied to IN+ of A1. Power is on when ANTPWR is at logic 1.

Control for the external antenna selection switch is generated by sequences of fast on and off pulses of feed voltage.

4.1.9 Test Multiplexer

An analog 8-to-1 multiplexer D2 (4051B) is provided for automatic testing of various voltages of MRR111. The address bits set by the serial control bus define which of the following test signals is routed to the MRRMUX output: +3.3 V supply, A+5 V supply, +7 V supply, +12 V supply, antenna feed voltage, SCLOCK, SWDATA and SYNMUX. The signals are scaled and shifted by resistor networks to comply with the 0 ... 5 V range of the multiplexer output. Details of the scaling and addresses can be found from MRR111 Control Functions Specification.

4.1.10 Control

All functions of MRR111 are controlled by Radio Processor MRP111 via a three line serial control bus (SCLOCK, SWDATA and SRDATA). The commands entering the unit via the bus are interpreted by a programmable logic device (PLD) D4 (EPM7064S). It has numerous outputs that control the operation of the receiver. Details of the controlling functions can be found from MRR111 Control Functions Specification.

Programming of PLD is done by using JTAG interface (TDI, TDO, TCLK, and TMS) via the card edge connector X1.

4.1.11 Introduction to Test Points

Typical signals and voltages at the test connectors and some essential points under normal operating conditions are described to help possible fault diagnosis.

The aluminum cover of the unit has to be removed to get access to the measurement points.

Measurement setup if not stated otherwise is:

- MRRR111 initialized for normal receiver operation and antenna power set off.
- A signal generator set at 403 MHz, no modulation, and level -20dBm is connected to ANT connector.
- Warm up time before measurements is at least ten minutes.
- A spectrum analyzer is connected to the test connectors using a test cable with a male MMCX connector.
- The DC voltages are measured with a digital voltmeter.

4.1.11.1 X6 RF

Typical spectrum measured from test connector X6 is shown in the figure below.

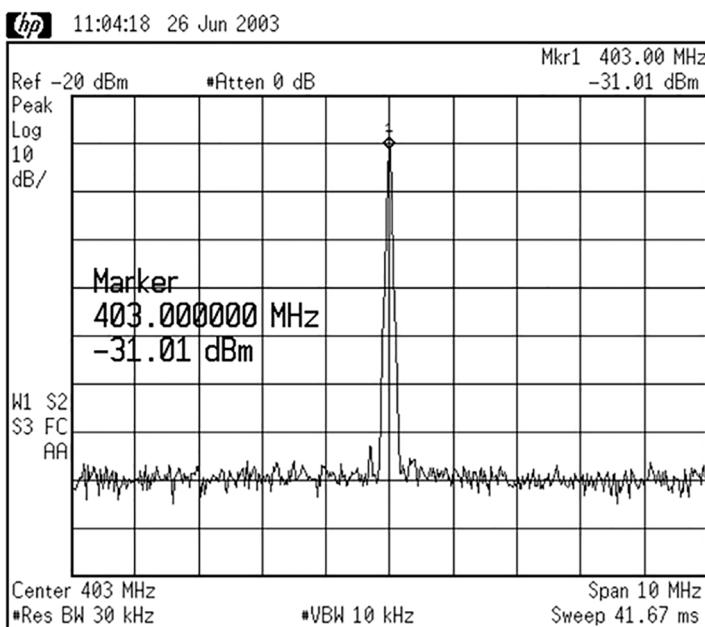


Figure 14 Spectrum from X6

4.1.11.2 X4 IF AMP

Typical spectrum measured from test connector X4 is shown in the figure below.

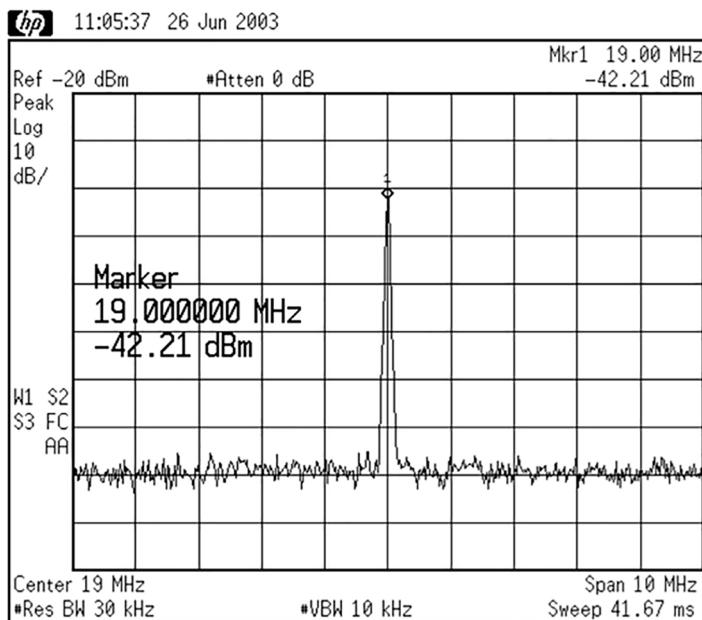


Figure 15 Spectrum from X4

4.1.11.3 X7 IF

Typical spectrum measured from test connector X7 is shown in the figure below.

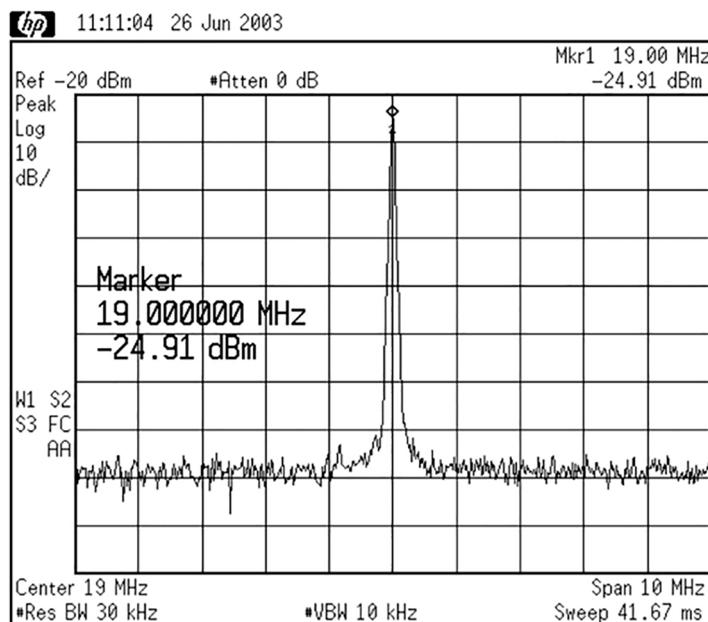


Figure 16 Spectrum from X7

4.1.11.4 X5 LO

Typical spectrum measured from test connector X5 is shown in the figure below.

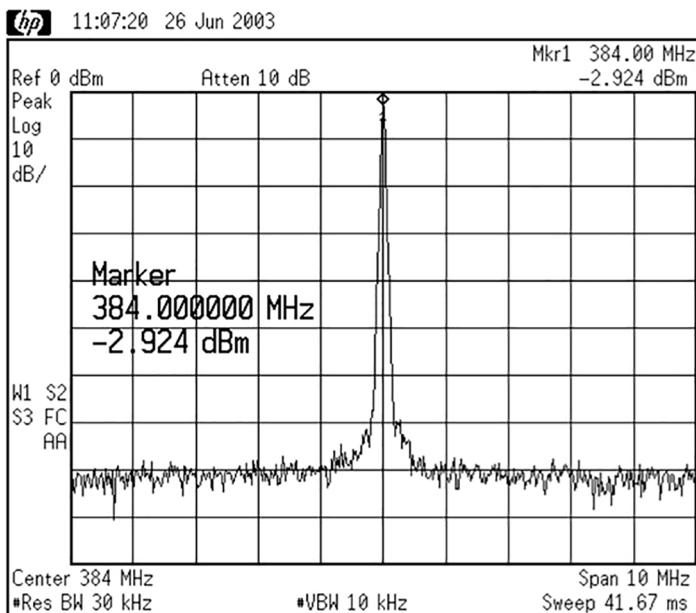


Figure 17 Spectrum from X5

4.1.11.5 X2 64 MHz

Typical spectrum measured from test connector X2 is shown in the figure below.

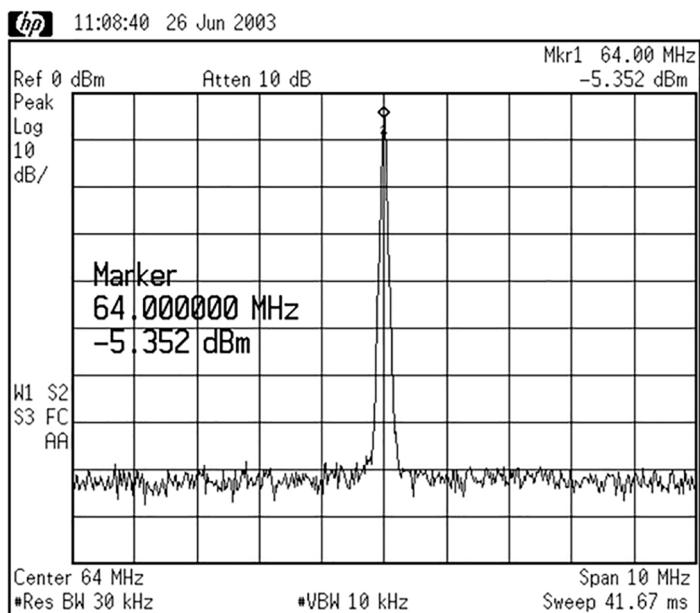


Figure 18 Spectrum from X2

4.1.11.6 EXT IF

Measurement setup is as described in 3.1 but the signal generator is connected to the EXT IF input (X3), frequency set at 10.7 MHz, modulation off and level -10 dBm.

Typical spectrum measured from test connector X7 is shown in the figure below.

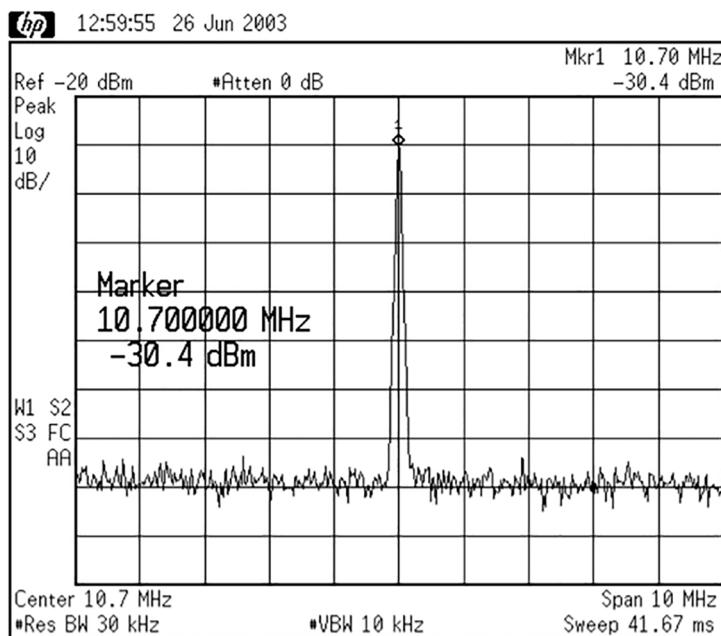


Figure 19 Spectrum from X7 (Input to EXT IF)

4.1.12 Typical Voltages

Typical DC voltages between some essential points and the ground are shown in the following table.

Table 10 Typical DC Voltages

Measurement Point	Description	Voltage [V]
A7 input pin 2	Amplifier input bias voltage	1.8
A7 output pin 1	Amplifier output bias voltage	3.9
A2 input pin 2	Amplifier input bias voltage	1.8
A2 output pin 1	Amplifier output bias voltage	3.9
A8 input pin 2	Amplifier input bias voltage	1.6
A8 output pin 1	Amplifier output bias voltage	4.5
A4 input pin	Amplifier input bias voltage	1.6
A4 output pin	Amplifier output bias voltage	3.4
T1 pin5 / C28	ADC clock input bias voltage	2.5
T2 pin5 / C78	ADC analog input bias voltage	2.5
C91 / R77	Phase detector voltage	3.2

4.1.13 Specifications

Table 11 MRR111 Technical Specifications

Property	Value/Description
Frequency Range	400 ... 406 MHz
Noise Figure	8 dB
Intermediate Frequency	16 ... 22 MHz
Image Rejection	45 dB
Spurious Free Dynamic Range	80 dB
Third Order Intercept Point (IIP3)	+16 dBm
Maximum Input Power Level	-9 dBm full scale +15 dBm absolute maximum
Antenna Power Feed	+12 V 150 mA
External IF input	10.2 ... 11.2 MHz +7 dBm full scale +15 dBm absolute maximum
Operating conditions	Temperature: -30 ... +55°C
Storage conditions	Temperature: -55 ... +80°C
Unit type	E1-size printed circuit board
Dimensions	210(L) x 130(W) x 21(H) mm
Weight	350 g

Table 12 MRR111 Power Requirements

V	mA
+3.3V	110 mA
+5.0 V	80 mA
+7.0 V	420 mA
+12.0 V	260 mA

Table 13 MRR111 Connectors

Connector	Description
System connector	220-pin female hard metric 2 mm
Antenna connector	LEMO EPS.00.250.NTN
External IF in connector	LEMO EPS.00.250.NTN

4.1.14 Signals and Connections

Table 14 Connector Pin Out for X1

Pin	Signal Name	I/O	Description
1A	GND		Ground, 0 V
1B	GND		Ground, 0 V
1C	GND		Ground, 0 V
1D	GND		Ground, 0 V
1E	GND		Ground, 0 V
2B	GND		Ground, 0 V
2C	MRRMUX	O	Output of analog test MUX (0 ... 5 V)
2D	GND		Ground, 0 V
4A	ADDITH	I	Dither signal input to A / D converter (0 / 5 VPRBS)
5C	GND		Ground, 0 V
6A	GND		Ground, 0 V
6B	GND		Ground, 0 V
6C	GND		Ground, 0 V
6D	GND		Ground, 0 V
6E	GND		Ground, 0 V
7A	SR1SD0	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7B	SR1SD0#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7C	GND		Ground, 0 V
7D	SR1SD1	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
7E	SR1SD1#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
8A	GND		Ground, 0 V
8B	GND		Ground, 0 V
8C	GND		Ground, 0 V
8D	GND		Ground, 0 V
8E	GND		Ground, 0 V
9A	SR1SD2	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
9B	SR1SD2#	O	Serialized data from ADC (448 Mbit/s, 1.1 / 1.4 V)
9C	GND		Ground, 0 V
9D	SR1CLK	O	Data clock from ADC (64 MHz, 1.1 / 1.4 V)
9E	SR1CLK#	O	Data clock from ADC (64 MHz, 1.1 / 1.4 V)

Pin	Signal Name	I/O	Description
10A	GND		Ground, 0 V
10B	GND		Ground, 0 V
10C	GND		Ground, 0 V
10D	GND		Ground, 0 V
10E	GND		Ground, 0 V
21B	SCLOCK	I	Serial control bus clock input (-8 / 8 V)
21C	SWDATA	I	Serial control data input (-8 / 8 V)
22B	SRDATA	O	Serial data output from PLD (active high 10 V)
23A	GND		Ground, 0 V
23B	GND		Ground, 0 V
23C	GND		Ground, 0 V
23D	GND		Ground, 0 V
23E	GND		Ground, 0 V
37B	GND		Ground, 0 V
38A	JTDO	O	JTAG
38B	JTCK	I	JTAG
38D	JTDI	I	JTAG
38E	JTMS	I	JTAG
39E	GND		Ground, 0 V
40C	+7 V	I	Power supply voltage for synthesizer
42A	+3.3 V	I	Power supply voltage for logic circuits
42B	+3.3 V	I	Power supply voltage for logic circuits
42C	+3.3 V	I	Power supply voltage for logic circuits
42D	+3.3 V	I	Power supply voltage for logic circuits
42E	+3.3 V	I	Power supply voltage for logic circuits
44A	+5 V	I	Power supply voltage for logic circuits
44B	+5 V	I	Power supply voltage for logic circuits
44C	+5 V	I	Power supply voltage for logic circuits
44D	+5 V	I	Power supply voltage for logic circuits
44E	+5 V	I	Power supply voltage for logic circuits
46A	+12 V	I	Power supply voltage for analog circuits
46B	+12 V	I	Power supply voltage for analog circuits
46C	GND		Ground, 0 V

Pin	Signal Name	I/O	Description
46D	-12 V	I	Not used
46E	-12 V	I	Not used
47A	GND		Ground, 0 V
47B	GND		Ground, 0 V
47C	GND		Ground, 0 V
47D	GND		Ground, 0 V
47E	GND		Ground, 0 V

- Coaxial connector X8 (ANT): 400 MHz RF input
- Coaxial connector X3 (EXT IF 10.7 MHz): External 10.7 MHz IF input

4.1.15 Parts List MRR111

Table 15 Parts List

Reference	Part Number	Description
Assembly ref. 001	DRW213000	Front panel machining MRR111
Assembly ref. 001	DRW213001	Front panel assembly for MRR111
Included in the part above.	210849	Front panel, shielded, 3U,4HP,Schroff
	210853	Injector/ejector handle, 4HP, IEL, Schroff
	210854	EMC gasket, 3U, Schroff 21101-854
	210855	Sleeve, M2.5 x 3,Schroff 21100-660
	210856	Board holder, Schroff
	210857	Collar screw, M2.5 x 12.3, Schroff
	212048	Screw, crosshead, M2,5 x 8 DIN7985 PZ A4
	212049	Screw, crosshead, M2,5 x 8 DIN966 PZ A4
	5068	Screw-lock compound, Loctite 222
Assembly ref. 002	16166	Plastic label 1180
Assembly ref. 002	210854	EMC gasket 3U, Schroff 21101-854
Assembly ref. 003	210853	Injector/ejector handle 4HP, IEL, Schroff
Assembly ref. 003	15223	Sticker set type, barcode and serial number
Assembly ref. 004	DRW212909	Screening cover for MRR111
Assembly ref. 004	210856	Board holder Schroff
Assembly ref. 005	210855	Sleeve M2.5x3, Schroff 21100-660
Assembly ref. 006	210857	Collar screw M2.5 x 12.3, Schroff

Reference	Part Number	Description
	PCB210106	Printed circuit board MRR111
Integrated Circuits		
A1	211859	IC, power switch ST L6377D
A2, 7	210635	IC, RF amplifier SGA-6289 (SMD)
A3, 11	210634	IC, RF switch NEC uPG2009TB
A4	16889	IC, amplifier MAR-6SM (SMD)
A5	010113	IC, converter A/D AD6645ASQ-80
A6	210630	IC, mixer SYM-18H (SMD)
A8	210636	IC, RF amplifier SGA-6489 (SMD)
A9	210638	IC, VCO VCO190-370T
A10	210633	IC, freq. synth. ADF4112BRU
A12	19991	IC, voltage reg. MIC2920A-5.0BS
D1	010029	IC, LVDS Serdes transmit SN65LVDS95
D2	15525	IC, analog MUX 4051B (SMD)
D3	15964	IC, inverter Ex 74HC14 (SMD Reel)
D4	25771	IC,EPLD EPM7064STC44-10, TQFP44
Transistors and Diodes		
V1	010192	Diode, LED 591-3001, red and green
V2,5	15495	Transistor, NPN SST3904 SOT-23
V3	18135	Diode, silicon BAV99 (SMD)
V4	25184	Transistor, PNP BCP53-10
V6	210627	Diode, noise ST-2 (SOT-23)
Resistors		
R1, 4, 6	18601	Resistor, chip 221R 1% 100 ppm
R2, 7, 10, 11, 34, 35, 40, 41, 69, 75, 79-81	15304	Resistor, chip Ex 100R 1% 50 ppm
R3, 5	18151	Resistor, chip 68R 1% 100 ppm
R8, 12, 15, 24, 82-84	18409	Resistor, chip 100R 1% 100 ppm
R9, 14, 43, 46, 47, 64, 72	18600	Resistor, chip Ex 475R 1% 50 ppm
R13	18794	Resistor, chip 17k8 1% 50 ppm
R16-23, 25, 28-32, 36, 38	25264	Resistor, chip 464R 1.0% 100 ppm
R26, 44	18119	Resistor, chip 1k82 1% 50 ppm

Reference	Part Number	Description
R27, 39, 55, 58, 61, 63, 67, 68, 73	18123	Resistor, chip 10k 1% 50 ppm
R33	15830	Resistor, chip 1k2 5% 200 ppm
R37, 45	16384	Resistor, chip 56R 5% 200 ppm
R42, 76	18720	Resistor, chip Ex 56R2 1% 100 ppm
R48	18731	Resistor, chip 681R 1% 50 ppm
R49	16421	Resistor, chip 51R 5% 200 ppm
R50, 51	19240S	Resistor, chip 22R 5% 200 ppm
R52	18736	Resistor, chip Ex 2k15 1% 50 ppm
R53, 60	18153	Resistor, chip 39R 1% 100 ppm
R54, 57	16416	Resistor, chip 270R 1% 50 ppm
R56	18724	Resistor, chip 147R 1% 100 ppm
R59	18118	Resistor, chip 1k2 1% 50 ppm
R62, 70, 71	18117	Resistor, chip Ex 1k0 1% 50 ppm
R65	18723	Resistor, chip 121R 1% 50 ppm
R66	18716	Resistor, chip Ex 27R4 1% 100 ppm
R74	15889	Resistor, chip 1M0 1% 50 ppm
R77	18725	Resistor, chip 178R 1% 100 ppm
R78	18596	Resistor, chip 4k75 1% 50 ppm
R85, 86	15878	Resistor, chip 10R 5% 200 ppm
R87	18732	Resistor, chip 825R 1% 50 ppm
R89	26101	Resistor, chip 221R 1.0% 100 ppm
R90	25210	Resistor, chip 332R 1.0% 100 ppm
RA1-5	25800	Resistor network RA4C1632-203-F
Capacitors		
C1,10,16,46,58,59,64-66,75,76,79,83,85, 87,88,90,96-99,104,105,107,109,111,113- 115,118,119	18524	Cap., chip ceramic Ex 1n 5% NPO 50V
C2,5,7,12,18,28,31,41,42,71,73,78,82,84	15158	Cap., chip ceramic Ex 100 nF X7R
C3	25900	Cap., chip ceramic Ex 2222 580 16523
C4, 8, 11, 14, 17, 19, 23, 24, 27, 29, 30, 33, 34, 44, 45, 47, 51, 53, 54, 56, 62, 63, 68-70, 72, 77, 80, 89	15160	Cap., chip ceramic Ex 10n 10% X7R 63V
C6, 13, 25, 36, 81, 93, 108, 110, 116	15621	Cap., chip ceramic Ex 100n 10% X7R 50V
C9, 50	15804	Cap., chip ceramic 4p7 p25 NPO 50V

Reference	Part Number	Description
C15	17515	Cap., chip ceramic 2222 861 14279 RC12G
C20	15164	Cap., chip ceramic 22P 5 % NPO
C21, 86, 94, 101-103, 106, 112, 117, 120	26074	Cap., chip tantalum 22uF 16V 20% C LowESR
C22, 49	15803	Cap., chip ceramic Ex 3,3pF NPO
C26	16023	Cap., trimmer TZBX4Z250BA
C32	15166	Cap., chip ceramic
C35, 99, 100, 121	15163	Cap., chip ceramic Ex 100p 5% NPO 63V
C37 ,43	16391	Cap., chip ceramic Ex GRM40C0G181F50PT
C38, 39	26225	Cap., chip ceramic 6p8 p25 N750 50V
C40, 55, 61	18633S	Cap., chip trimmer 3p0-10p N150 TZBX4N100AB
C48	15933	Cap., chip ceramic 39pF NPO 5%
C52, 57	15608	Cap., chip ceramic 120pF N750
C60	15165	Cap., chip ceramic
C67	15488	Cap., chip ceramic 33pF NPO
C74	15376	Cap., chip ceramic 2222 861 15129
C91	15750	Cap., chip ceramic 330nF X7R
C92	19442	Cap., chip tantalum 220uF 10V 20% Case E
C95	15802	Cap., chip ceramic 1,5pF NPO
Connectors		
X1	210249	Connector, 2 mm Metric 5 x 44 socket, press-fit
X1	10948	Marking sticker OK46546, fixed on to the connector
X2, 4-7	210778	Connector, MMCX 90 MMCX-S50-0-51/119 OH
X3, 8	16799	Connector, coaxial EPS.00.250.NTN
Miscellaneous		
Z1, 3-6, 8, 9	25036	Filter, EMI (SMD) NFM61R30T472
Z2	210632	Crystal oscillator 64 MHz, (SMD)
Z7	210637	Filter, ceramic CF12S3-403
L1, 6, 7	17555S	Choke 18uH 10% SMD
L2, 16, 17, 19, 20, 22-24	18637S	Choke, chip 470n 5% coilcraft
L3	17506	Inductor, chip 1.0uH 10%
L4, 18	25312S	Choke 330uH 20% coilcraft
L5	25089S	Choke, chip 1 4700n 10% coilcraft
L8, 12, 13, 15	16398	Inductor, chip 2.2uH 10% 1210 250mA

Reference	Part Number	Description
L9-11	17559S	Choke 220n 5% SMD
L14, 21	17367S	Choke, RF 47 nH 10% SMD
T1, 2	210631	Transformer, RF, (SMD) ADTT4-1
	211738	Screw, crosshead M2,5 x 6 DIN7985 PZ A4
	211741	Therm. conductive liquid gap filler 1000, 50cc
	212048	Screw, crosshead M2,5x8 DIN7985 PZ A4
	212049	Screw, crosshead M2,5x8 DIN966 PZ A4
	5068	Screw-lock compound, Loctite

4.1.16 Diagrams and Board Layouts MRR111

Table 16 MRR111 Diagrams and Board Layouts

Code	Description
DRW230935	Circuit Diagram, 2 pages
DRW228506	Components Layout

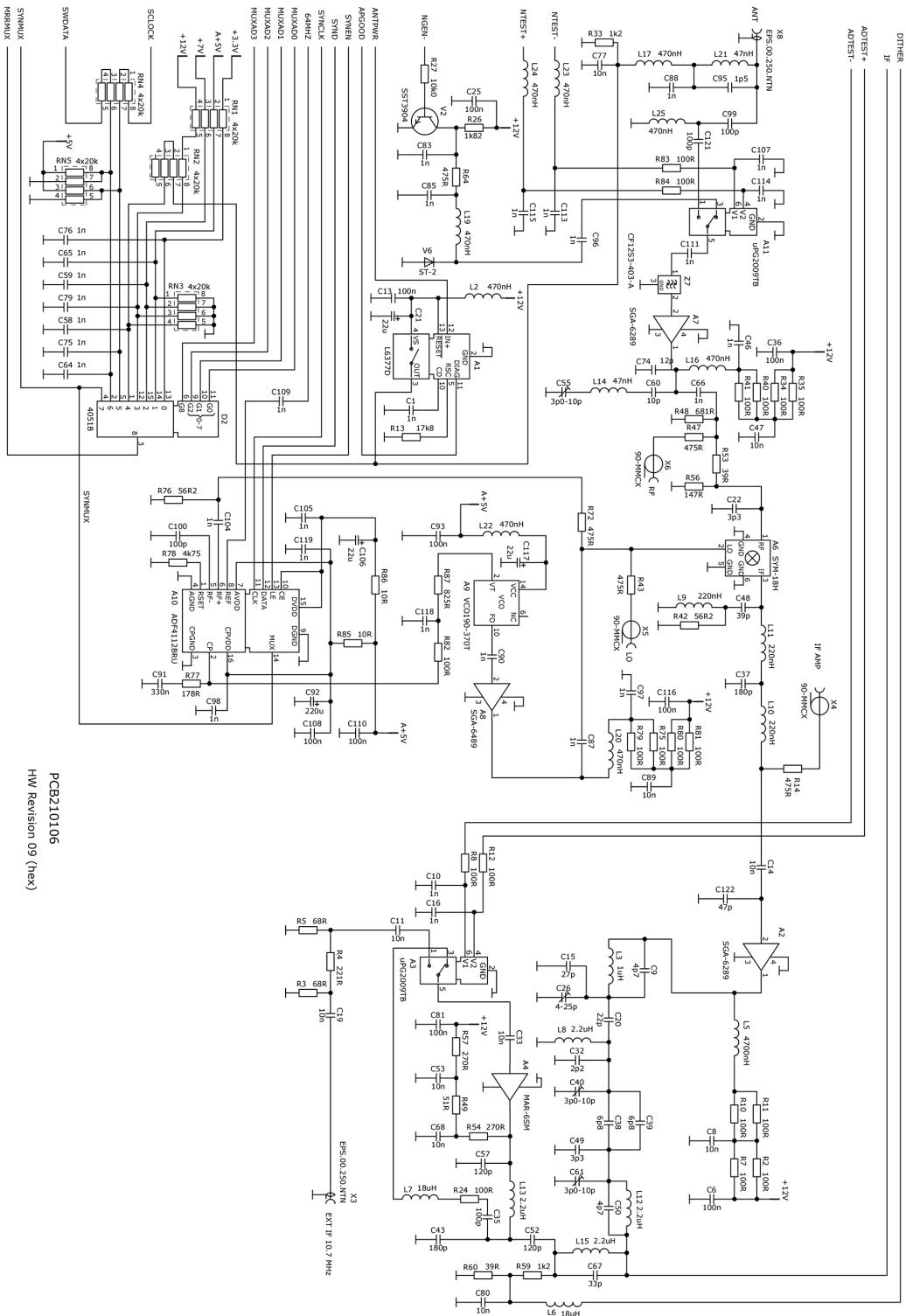


Figure 20 MRR11 and MWR321 Circuit Diagram, 1/2

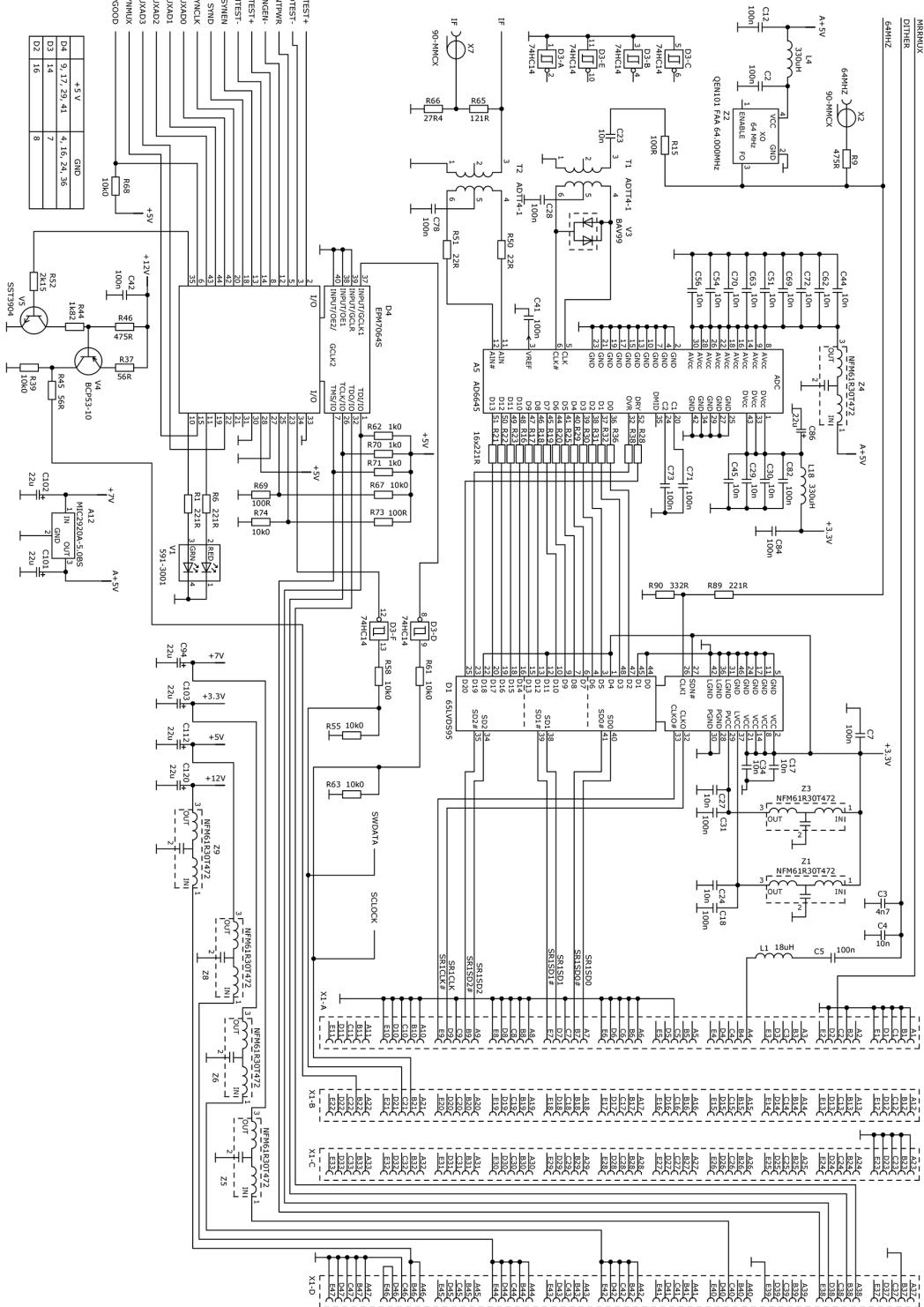


Figure 21 MRR111 and MWR321 Circuit Diagram, 2/2

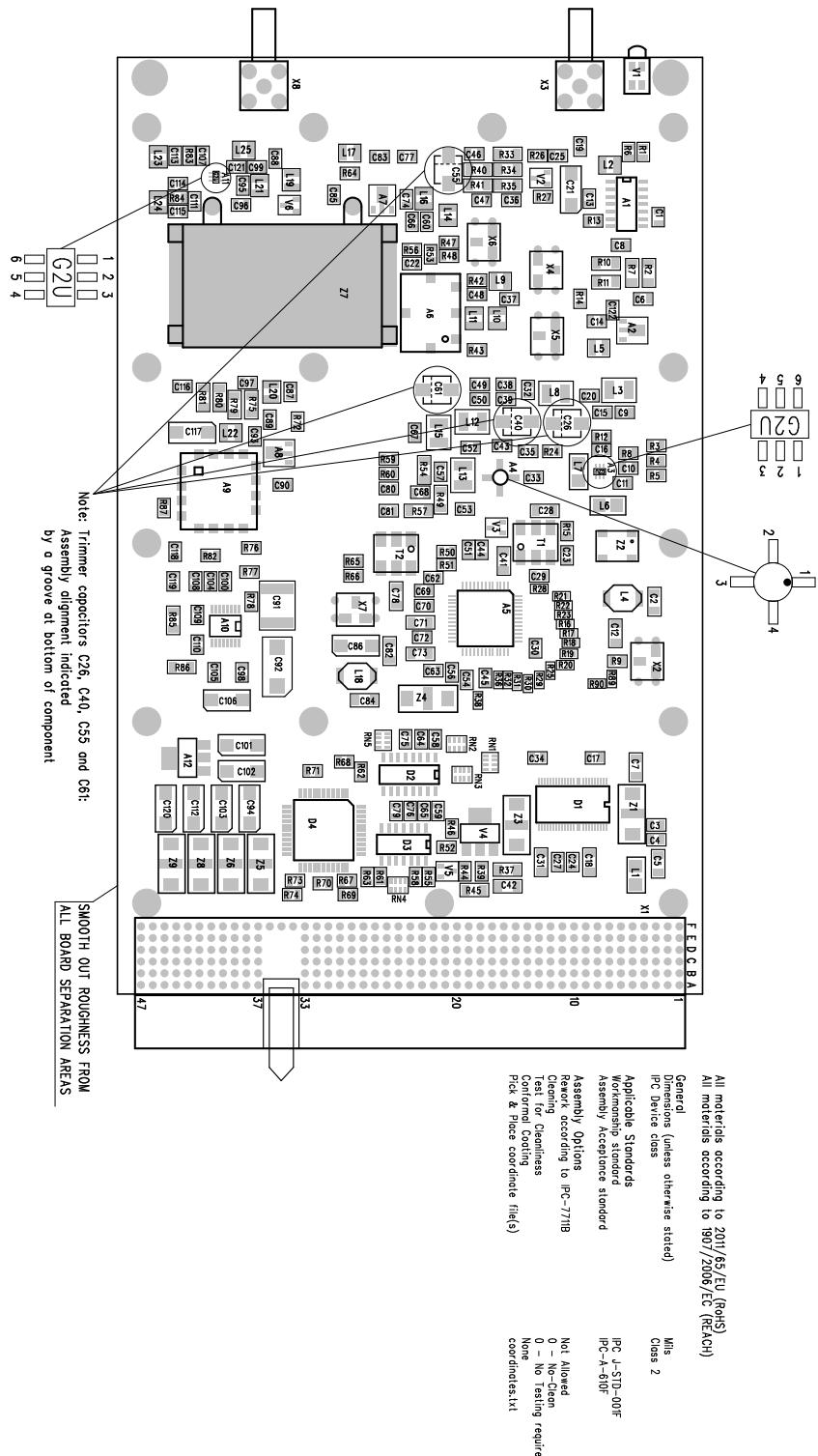


Figure 22 MRR111 and MWR321 Components Layout

4.2 Receiver Processor MRP111

Receiver Processor MRP111 is an E1-size Euro card unit. It is used with a 400 MHz receiver unit or with 1680 MHz receiver units to build up a digital radio receiver (software radio). The receiver processor takes the digital IF data input from receiver units at a rate of 64 Msamples / s and all further receiver functions are performed digitally in receiver processor.

The receiver processor contains three digital down converter (DDC) chips, a digital signal processor (DSP), a control processor, a programmable logic device (PLD), an ATA/IDE flash disk, an Ethernet line interface, two serial communication channels, and input/output signals for receiver controls.

Each DDC chip is a four-channel device containing digital mixers, a quadrature carrier numerically controlled oscillator (NCO), digital filters, a resampling filter, an automatic gain control (AGC) loop and a cartesian-to-polar coordinate converter providing magnitude and phase output data at each channel.

The digital signal processor is a complete 32-bit floating-point device integrating data processing elements, a large high-speed memory (SRAM), and I/O peripherals. In addition, fast external synchronous burst memory (SBSRAM) is provided.

The control processor is a 32-bit PC-compatible microprocessor system with floating-point math instructions and 64-MByte synchronous dynamic system memory (SDRAM).

The programmable logic device (PLD) is an in-circuit-configurable logic chip, which is used to handle control and data connections between system blocks.

ATA flash disk is a 64-MByte memory chip for program and data storages.

The Ethernet communication interface consists of an Ethernet controller and a five-channel Ethernet switch. Three switch channels are available for external connections at 10 or 100 Mbits/s line speed.

Two asynchronous serial channels are provided for RS232-compatible external connections.



Figure 23 Receiver Processor MRP111

4.2.1 CPU

MRP111 contains an ZFx86-type 32-bit microprocessor running at the speed of 96 MHz. The microprocessor chip is PC-compatible and contains the following main parts:

- SDRAM controller
- PCI bus interface
- ISA bus interface
- IDE bus interface
- Serial channels COM1 and COM2

The SDRAM controller is for connecting to the 32-bit synchronous system memory.

PCI bus is used to connect to the 10/100 MBits/s Ethernet controller.

ISA bus is used for flash-type BIOS memory and system logic PLD connections.

IDE bus connects to onboard ATA flash disk memory.

Serial channel COM1 is for diagnostics and channel COM2 is used as a system interface.

In the circuit diagram, the processor D7 is divided into six parts:

- D7-A contains common control signals, interrupt inputs, chip select outputs, IDE interface, and a floppy disk interface.
- D7-B contains PCI bus interface.
- D7-C contains ISA bus interface.

- D7-D contains SDRAM interface
- D7-E contains parallel port, serial ports COM1/2, USB bus, keyboard, I2C bus and watchdog interfaces.
- D7-F contains power connections.

After reset the processor starts operation by executing the BIOS (Basic Input/Output System) code from the flash memory in ISA bus. The BIOS code verifies the correct operation of the main system components, and later in operation, the BIOS code and further code execution are transferred to the SDRAM system memory.

After the BIOS is complete, the processor boots from onboard ATA flash disk memory, loads logic code to PLD and starts the execution of the actual application program.

4.2.2 Flash Memory

The flash-type program memory is for the BIOS program. The memory consists of 512k x 8-bit circuit D34. The flash-type memory allows loading and modification of programs via the communication lines. In normal operation, the flash memory works as a read-only code memory. The first code byte, after reset, is fetched from memory location 7FFF0 (hex) in a boot block. The chip select MEMCS0# selects the device and the read control MEMRD# activates the output data buffers of the memory.

During normal operation, the write signal PMEMWR# to the D34 connects via PLD and is locked to the inactive high state. A special unlock command sequence to PLD D8 is required to enable flash programming.

4.2.3 SDRAM Memory

Synchronous Dynamic Random Access Memory (SDRAM) is the main system memory for program code and data. The size of the memory is 64 MBytes (16 M x 32-bits) and it consists of four SDRAM circuits, each having 8M x 16 bits.

The SDRAM is divided into two banks; chip select signal SDCS0# selects the lower 32-MByte bank (D10, D14) and SDCS1# selects the higher 32-MByte bank (D11, D15).

The operation of the memory is synchronous to the clock signals SDCLK0 and SDCLK1. Column and row addresses are loaded by SDCAS# and SDRAS# signals and SDWE# controls the write operation. Byte mask signals SDQM0#, SDQM1#, SDQM2# and SDQM3# are used to enable single-byte wide writes, in a full 32-bit write cycle all are active low.

4.2.4 ATA-IDE Disk Chip

The ATA/IDE flash disk chip (D8) is an embedded flash memory data storage system. It has a built-in ATA/IDE controller and a built-in embedded flash file system. It has a capacity of 64,028,672 bytes in 977 cylinders with 4 heads and 32 sectors.

The 16-bit IDE interface of the ZFx86 is directly connected to the ATA/IDE standard interface of disk chip D8.

Write-protect input WP# is connected to the PLD for possible future use.

4.2.5 Serial Channels

ZFx86 has two serial channels for external serial communication:

- Channel 1 is for testing and it is connected to the front panel connector.
- Channel 2 is the main system channel and it is connected to the system connector pins A30 (TXD2) and A31 (RXD2). This channel is normally used for main external RS232 compatible connection.

4.2.6 Boot Code Resistors

The ZFx86 processor reads the boot code from ISA bus address lines after reset is released. The processor has weak internal resistors for default values. In address lines SA06, SA17, SA18, and SA19, the desired value is different from the default and external resistors are required.

In addition, weak external pull-down resistors are required in lines SA00-SA05 and SA09 which have default value 0 and are connected to the PLD (D5), because the PLD connects weak internal pull-ups to the lines during reset. Resistors in lines SA07 and SA08 are for possible future use.

The value of line SA23 selects the boot mode by TEST# signal input. In normal operation TEST# is high, D46 does not drive SA23 and normal boot is selected. If TEST# is active, SA23 is driven high and internal boot is selected.

4.2.7 Introduction to PLD

Programmable logic device (PLD) D5 is digital, user-configurable integrated circuit (IC), which is used to implement custom logic functions. The D5 is a SRAM-based PLD, which is in-circuit configurable. Its configuration (program) code is stored in the disk memory and the configuration takes place during the system power-up. The PLD D5 is used to implement various timing, control and interface logic functions in the MRP111.

In the circuit diagram (see section [Diagrams and Board Layouts MRP111 \(page 79\)](#)), the PLD D5 is divided into six parts:

- D5-A contains common control signals, special I/O signals, and five general purpose I/O signals.
- D5-B contains 76 general purpose I/O signals.
- D5-C contains 76 general purpose I/O signals.
- D5-D contains 76 general purpose I/O signals.
- D5-E contains 76 general purpose I/O signals.
- D5-F contains power connections.

The main functional blocks are described in more detail in the following sections.

4.2.7.1 Clock Dividers

25-MHz clock input is multiplied by fractional number 16384/12500000 to get 32768-Hz output for ZFx86 processor real time clock. This clock signal overrides the RC oscillator D47/4 output when PLD code is loaded

4.2.7.2 ISA Bus Interface

ISA bus control, data and address signals are connected from ZFx86 ISA block to the PLD for DSP interface, serial channel, and general purpose I/O functions.

Address lines SA00-SA03 with chip select inputs IOCS0# and IOCS1# are used to select desired control functions. Control lines IORD# and IOWR# are used for read and write commands, and data lines SDO to SD15 are used for data transfer.

Output ZWS# is activated in all IOCS0# / IOCS1# commands, output IOCS16# is activated in IOCS1# commands, and interrupt line MZIRQ5 is used for interrupts.

Other connected lines are reserved for possible future use.

4.2.7.3 PLL Programmer and Serial DAC Interface

PLL programmer sets the clock multiplier D27 for 40-MHz clock output by loading a 24-bit serial control word 330C02 (hex) into D27 with 1-MHz data clock. MSB is sent first and data load signal PLLLD is generated at the end. One programming cycle is automatically generated after PLD configuration.

After PLL programming the same data and clock signals are used for serial DAC A9 control. A 12-bit DAC code 800 (hex) is automatically sent after PLL programming and later on the interface runs under DSP control. Clock rate is 3.125 MHz and signal DA4LD is used to load the data.

4.2.7.4 DSP Control and Data Interface

DSP control interface connects reset, clock, and clock mode control signals to the DSP. The reset signal is released after the clock and clock mode control signals are active.

The operation of the DSP is controlled by reset setting. After reset the DSP starts reading boot code from link port 4.

Data flow from ZFx86 to DSP via link port 4:

- Data to DSP is written from the ISA bus as 16-bit words in two or four byte packets.
- PLD logic writes the data in byte or nibble serial format to DSP link port 4.
- In a 16-bit mode, four nibbles are written after each ISA word and in a 32-bit mode, four bytes are written after every two ISA words. The nibbles are written in lower four bits of link port data.
- The PLD logic and link port receiver are fast enough to keep the ISA port always ready for next word write. For special use and diagnostics purposes, the port status can be checked by reading the status word.

Byte and nibble order at link port 4 are according to the following tables (B1 and B3 are high bytes at ISA bus, N3 is the highest nibble):

Table 17 Byte Order in 32-bit Mode

Words Written by ZF	Bytes Written to Link Port
1. W1 (B1, B0)	1. B3
2. W2 (B3, B2)	2. B2
	3. B1

Words Written by ZF	Bytes Written to Link Port
	4. BO

Table 18 Nibble Order in 16-bit Mode

Words Written by ZF	Nibbles Written to Link Port
1. W1 (N3, N2, N1, N0)	1. N3
	2. N2
	3. N1
	4. N0

Data flow from DSP to ZFx86 via link port 5:

- Data from DSP is written in four byte packets to four data registers in PLD, and further writes are inhibited until the registers are read as two 16-bit words by ZFx86 processor.
- The link port is fast enough to provide data for continuous full speed read at ZFx86 ISA bus. Data availability can also be checked by reading the status word. For diagnostics purposes, an empty read condition is indicated.

Table 19 Byte Order in ZFx86 Read

Bytes from Link Port	Words Read by ZF
1. B0	
2. B1	1. W1 (B2, B3)
3. B2	
4. B3	2. W2 (B0, B1)

4.2.7.5 DSP Command Interface

The command interface connects to serial port 0 of the DSP. The rising edge of the transmit frame sync signal (DSTFSO) starts the operation and a serial 32-bit command is clocked in from transmit data line (DSDTO) and latched in parallel register at every 32 clocks (DSTCLK0) as long as the frame sync signal stays high. After reception, each command is executed and the required actions are generated.

The 32-bit command word contains a direction bit, 7 device address bits, 8 register address bits, and 16 data bits.

In a read command (direction bit = 1) frame sync signal (DSRFSO) for input port is generated followed by 16 data bits to the serial input data line (DSDRO).

The interface supplies continuous 25 MHz external bit clock signals for output (DSTCLK0) and input port (DSRCLK0) data clocks.

4.2.7.6 DDC Control Interface

DDC control interface generates control signals to the DDC chips, SERDES receivers, and clock selectors, and, in addition, transfers control data to/from data bus of the DDC chips. See section [Control Bus \(page 62\)](#) for bus signals.

The control interface works under the control of the DSP command interface.

4.2.7.7 DDC Data Interface

The DDC data interface receives two serial data streams from the output ports of each DDC and converts both 224-bit serial data streams into byte format (28 bytes each), and writes the bytes in two separate FIFO memories. When complete data frames are received, the interface starts writing the data to the DSP link port and, simultaneously, the serial inputs are ready to receive next data frames. The frame sync signal starts the reception of a new data frame.

The frame rates depend on DDC processing parameters.

Serial bit burst rates are 2×32 Mbits/s and link port byte burst rates are 16 Mbytes/s in each DDC connection.

DDC1, DDC2, and DDC3 are connected to link ports 1, 2, and 3, respectively.

4.2.7.8 Frequency Meter

The programmable frequency meter supports cycle time measurements of MUXFREQ and 1PPS input signals. Also the cycle times of all PLL frequencies can be measured. The frequency meter is used by DSP command interface.

4.2.7.9 A-D Control Interface

The A/D control interface is used to set desired control outputs for the A/D converter according to the control commands via DSP command interface.

Serial output data and sync signals from A/D converter are passed via PLD to the serial port 1 of the DSP.

4.2.7.10 Dual D-A Interface

The dual D/A interface connects DSP link port 0 or DDC3 output data to the dual DAC A6. The converter has two operating modes:

- normal mode: DAC is connected to the 0.
- Direct DDC3 mode: DAC is connected to the DDC3.

In normal mode, the link port data is written to DAC in four byte packets. Bytes 0/1 are the DAC1 LSB/MSB and Bytes 2/3 are the DAC2 LSB/MSB. Bits 4 - 7 in the MSB bytes are not used.

Port output rate is externally controlled by LPOACK according to the rate setting.

In direct DDC3 mode, the 12 most significant bits of DDC3 serial data stream A are converted in parallel and are directed to DAC1. Output rate is the frame rate of the DDC3 output.

4.2.7.11 ADC Dither Generator

ADC dither generator is a pseudorandom digital noise generator whose output can be used to add dither signal to the input of an external A/D converter.

The generator is a 15-bit linear feedback shift register operating at 3.125 MHz clock frequency. The generator can be enabled/disabled by a DSP command.

4.2.7.12 Receiver Control Interface

This interface is addressed by the command interface of the DSP and it writes control data to the serial synchronous control bus for the receiver modules. The bus comprises the following signals:

- Bus clock (GPOUT1)
- Serial control data (GPOUT2)
- Serial received data (GPIN1)

The following fixed-length 21-bit format is used in bus commands:

Table 20 Bus Command Format

	Start	Dev. Addr.	Reg. Addr.	Data	Stop
Bit	0	bits 1 ... 4	bits 5 ... 9	bits 10 ... 17	bits 18... 20
Signal	STA	DAO ... 3	RAO ... 4	D0 ... 7	STO 0 ... 2

A control command starts with a single start bit followed by device address, register address, control data, and stop bit fields.

The device address is used to select a unit in the bus and register addresses are used to select control functions inside a unit. Each unit has a unique fixed device address.

In read command, the 4-bit device address and a 8-bit data byte is received from the addressed unit.

Standard bit clock frequency is 100 kHz but some special commands may use lower bit rates. Bus clock is running only during active commands.

MRP11 is a bus master and only it can drive clock and control data lines. Received data line has pull-down resistors (R3,R4) in MRP11 and each addressed unit can drive the line to a high level when transmitting serial data in a read command.

4.2.7.13 MAS Control Interface

This interface is addressed by the command interface of the DSP and it writes control data to the serial synchronous control bus for the Vaisala MAS unit. The bus comprises the following signals:

- Bus clock (GPOUT5)
- Serial control data (GPOUT6)
- Serial received data (GPIN2)

The following fixed-length 33-bit format is used for control messages:

Table 21 Control Message Format

	Start	Device address	Register address	Data
Bit position	bit 0	bits 1 ... 8	bits 9 ... 16	bits 17 ... 32
Signal name	STA	DA 0 ... 7	RA 0 ... 7	D 0 ... 16

A control message starts with a single start bit followed by device address, register address, and control data word.

Register addresses are used to select control functions. The MAS unit has a fixed device address 51[hex].

The MAS unit replies to every valid command by sending back a fixed-length message, which contains a start bit and a 512-bit data block. The data block is received in the memory of the control interface to be further read by DSP via command interface.

The standard bus clock frequency is 100 kHz and the clock is running continuously.

4.2.7.14 Antenna Switch Control

Antenna switch control provides reset and clock signals for an external antenna switch. The interface has two operating modes:

In command mode, the control signals are used under direct DSP control.

In automatic rotation mode, a repeated sequence of reset signals followed by 12 clock pulses are generated at programmable clock pulse interval, and the current antenna positions (clock pulse counts after reset) are inserted in the data frame of the DDC2.

Reset signal is GPOUT3 (X1/D21) and clock signal is GPOUT4 (X1/E21).

4.2.7.15 Boot Flash Write Protection

Write signal PMEMWR# to flash memory D13 is connected via PLD and can be activated only with a special unlock control sequence.

4.2.7.16 Data Output Registers

Control signals for LED lights, status output, and general purpose I/O lines are provided. The outputs are controlled by ZFx86 via ISA interface.

4.2.7.17 Ethernet Controller

The AM79C793 (D3) is a single-chip fast Ethernet controller. It contains the following main functional blocks and features:

- 32-bit PCI host interface
- 10/100 Mbps Physical Layer Interface (PHY)
- Dual-speed CSMA/CD (10 Mbps and 100 Mbps) media access controller (MAC)
- Internal TX and RX FIFOs
- EEPROM interface

In the circuit diagram, the controller is divided into three parts: D3-A for PCI bus connection, D3-B for Ethernet line connections and D3-C for power connections.

The controller is directly connected to the PCI bus of the ZFx86 processor, and the 25.0 MHz clock is connected through divider D44-A from the 50 MHz output of the PLL clock multiplier D40.

The receive (TXP/M) and transmit (RXP/M) pairs of the Ethernet line are directly connected to the port 1 of the Ethernet switch.

The EEPROM D18 is for programmable initialization parameters, which are automatically loaded to the controller registers at system reset or power-up.

The power connections include extensive filtering of the analog supply voltages.

4.2.7.18 Ethernet Switch

The KS8995 (D2) is a five-port integrated Ethernet switch. It contains five 10/100 physical layer transceivers, five media access control (MAC) units with an integrated layer 2 switch.

In the circuit diagram, D2 is divided into three parts: D2-A is for common control and port five connections, D2-B is for port 1 to 4 connections and part D2-C is for power connections.

Port 1 is connected to the Ethernet controller. Ports 2, 3, and 4 are for external connections and are connected through transformers to the front panel connector ETH (port 2) and to the system connector (port 3, 4). Port 5 is not used.

Operation of each port is identical and includes the transmit and receive functions for a 100 Mbits/s (100BaseTX) and 10 Mbits/s (10BaseT) Ethernet lines.

The PLL clock synthesizer in the KS8995 generates 125, 50, 25 and 10 MHz clocks for internal system timing. All internal clocks are generated from an external 25 MHz clock input.

The power connections include extensive filtering of the analog supply voltages.

4.2.8 Introduction to DSP

D12 (ADSP-21160) is a general-purpose 32-bit Digital Signal Processor (DSP). It contains a processor core, 524 Kbyte internal RAM, I/O processor and external port. The I/O processor provides six 8-bit link ports and two serial ports for external communication. The external port is used for 64-bit external memory connection.

External clock frequency is 40 MHz and the core runs at 80 MHz. During power-up, a separate clock signal is supplied through a resistor. The final 40 MHz clock overrides this clock when the PLD code is loaded.

In the circuit diagram, the processor D12 is divided into four parts:

- D12-A contains common control signals.
- D12-B contains data bus interface.
- D12-C contains serial ports and link ports.
- D12-D contains power connections.

4.2.8.1 Boot Loading

The DSP has an internal ROM-based boot loader program. At power-up, the processor reset input signal (DSPRST#) is held active until the control processor is ready to communicate with DSP. After the DSP reset is released, the internal boot loader program of the DSP is directed (by setting inputs LBOOT=1, EBOOT=0 and BMS#=1) to fetch an external program code from link port 4. The control processor writes the code to the port in a half-byte serial format and after the whole start code block is transferred, it is executed by the DSP and a response is sent back to the control processor.

4.2.8.2 External SBSRAM

High-speed synchronous burst static random access memory (SBSRAM) chips D51 and D13 are connected to the 64-bit external bus of the DSP. The chip size is 524288 x 32 bits (2 MBytes) and the total memory size is 524288 x 64 bits (4 MBytes). The standard system uses this memory as data storage. Address signals DSPA20 and DSPA21 are connected for possible future use with larger capacity memory ships.

4.2.8.3 Interrupts, Flags, and Timer

The DSP has three external interrupt pins (DSPIRQ0#, DSPIRQ1#, DSPIRQ2#), four flag pins (DSPFLO ... 3) and one timer pin (DSPTIMER).

Interrupts are used in external communication. Flags and timer are for special needs and for possible future use.

4.2.8.4 Link Ports

The DSP has six bi-directional link ports for external data transfer. Each port has internal FIFO (First-In-First-Out) buffer memories for input and output data. Each port has two control signals for data transfer, port direction is set by DSP software. All port signals are connected to the PLD, which includes the interface logic between the port and destination connection.

The ports are used for the following data transfer channels:

- Port 0 is for dual DAC data output.
- Port 1 is for DDC1 data input.
- Port 2 is for DDC2 data input.
- Port 3 is for DDC3 data input.
- Port 4 is for data input from the control processor.
- Port 5 is for data output to the control processor.

4.2.8.5 Serial Ports

The DSP has two bi-directional high-speed serial ports for external data transfer. Each port has internal first-in-first-out (FIFO) buffer memories for input and output data. Each port has three signals for both directions: clock, frame sync, and serial data.

Port 0 is used as command interface between PLD and DSP.

Port 1 is used for A/D converter data input. Bit clock frequency is 12.5 MHz.

4.2.8.6 JTAG Port

The serial JTAG test access port (TCK,TMS, TDI, TDO and TRST#) and EMU# control signal are for product development purposes only and are not used in normal operation.

4.2.9 SERDES Receivers

Sample data from external A/D converter(s) are connected to MRP111 with high-speed serializer/deserializer (SERDES) data link(s). Data from each converter uses three serial data streams and a reference clock signal. At the transmitter end, the parallel A/D converter data is clocked in the serializer circuit as three 7-bit groups, and the circuit transmits these groups serially with a bit rate of seven times the clock frequency.

In MRP111, the deserializer circuit (D16, D22 or D28) multiplies the clock signal by seven and samples the incoming data streams by this multiplied clock rate to get the 7-bit groups back in the original parallel format. The resulting 21-bit data word is clocked out at the basic clock rate.

All data streams and clock signals use low-voltage differential signaling (LVDS).

The standard basic clock rate is 64 MHz, which results in a 448 Mbits/s rate at the data bit streams.

Data bits D0 ... 3, D5 ... 10 and D12 ... 17 are used for A/D data (bits D0 ... 1 are permanently low level with a 14-bit converter).

Bits D4, D11, and D18 are permanently high-level (for diagnostics purposes) and bit D19 indicates over range signal at the converter. Data bit D20 is not used.

4.2.10 Converter Circuits

Circuits D1, D4, and D6 are identical digital down converters (HSP50216), each having four data input ports and four internal converter channels. Each channel includes digital mixers, a quadrature carrier NCO, digital filters, a resampling filter, an AGC loop, and a converter for phase and magnitude data output.

All converter channels have data selectors for connecting to the desired data input port.

4.2.10.1 Data Inputs and Clock Selection

Data outputs from SERDES receiver 1(D16) and 2 (D22) are connected to all DDC circuits, receiver 1 to A input ports and receiver 2 to B input ports. Data from receiver 3 (D28) is connected to C input port of converter D4.

In addition, for diagnostics purposes, data from receiver 1 is connected to the PLD. This connection can also be used to feed test data from PLD to all converter circuits.

Clock selectors are provided for all down converters to allow connection to a clock signal which corresponds to the selected data connection.

Buffer circuits D26 and D29 are used to select clock signal for converter 1: SERDES clock 1 is selected when D26 is active ($DC1SEL1 = 0$), and clock 2 is selected when D29 is active. Test clock signal from PLD is selected when both buffers are inactive.

In the same way, buffers D30, D33, D53 are used to select clock for converter 2, and buffers D36, D41 are used to select clock for converter 3.

4.2.10.2 Control Bus

DDC circuits are controlled via control bus from DSP via PLD. Chip select signals (DC1CE#, DC2CE#, DC3CE#) select an active converter, address signals (DCA0..2) select internal registers, control strobes (DCWR#, DCRD#) select write or read operation, and data lines (DCD00...15) carry the control data.

In addition, reset (DC1RST#, DC2RST#, DC3RST#) and synchronize (DC1SYNC, DC2SYNC, DC3SYNC) inputs and interrupt outputs (DC1INR#, DC2INR#, DC3INR#) are provided.

4.2.10.3 Data Output

The DDC circuit has four serial ports for data output. In MRP111, ports A and B from all converters are in use. Each port comprises data and synchronizes signals (DC1SD1A and DC1SYNA for converter 1 port A) and each converter chip uses a common data clock signal (DC1SLK for DDC 1). Standard bit rate is 32 Mbit/s.

All serial data streams are converted as 8-bit byte streams in PLD and are further fed to the DSP via link ports.

4.2.11 Input Selector and Buffer Amplifier

Input selector D19 is controlled by ADSEL0...2 signals. The following input channels are available:

Table 22 Available Input Channels

Channel	Signal	Description
0	ANTIN	Antenna input for possible future use
1	GND	Ground (0 V)
2	MRRMUX	MRR111 multiplexer output
3	+3.3VOSC	+3.3 V oscillator supply voltage
4	DA1T	D/A converter 1 test output
5	DA2T	D/A converter 2 test output
6	+2.5V	+2.5 V supply voltage
7	-12/+5V	-12/+5 V test voltage (+3.45 V nom.)

The active input voltage range for all inputs is 0.0 to 4.75 V (limited by the supply voltage of the selector).

Buffer op amp A5-B connects the selector output to the single-ended differential input circuit A2, which further buffers the signal to the A/D converter. The gain of the circuit is 2/3.

The output of A5-B is also fed to PLD (signal MUXFREQ) for direct frequency measurements.

Converter active input voltage range is +0.5 ... +4.5V, which corresponds to a range of -0.5 ... +5.5V at the selector input.



The description of input selector and buffer amplifier corresponds to MRP111 units with HW revision 10 or higher. For earlier units, channels 1, 3, 6, and 7 are not connected and the A2 gain 1 corresponds to an input range of +0.5 ... +4.5 V.

4.2.11.1 Converter Circuit

The A4 (AD7723) is a 16-bit, sigma-delta analog to digital converter (ADC). The converter is used with 12.5 MHz clock signal (ADCLK), resulting in 390 kHz sample rate.

The converter data interface is serial and connects through PLD to the DSP. Signals serial clock output (ADCSCO), serial data output (ADCSDO), and frame sync output (ADCFSO) are used in serial data connection.

The output code is in twos complement binary format and the output equation is:

$$Dout = (Vin - 2.5) / 0.000091552$$

where

Callouts	Description
Dout	Digital output code [twos complement binary]
Vin	Analog voltage at selector input [V]



The equation corresponds to MRP111 units with HW revision 10 or higher. For earlier units, replace the divisor with figure 0.000061.

4.2.11.2 Dual D-A Converter

D/A converter A6 is a dual channel 12-bit digital to analog converter. Converter output currents are set by 12-bit binary data from link port 0 of the DSP. Byte-wide data from the link port are combined to proper 12-bit codes in the PLD.

In direct DDC mode, data to converter 1 is taken from the serial output of the DDC3 and converted to 12-bit parallel values in PLD.

The converter output current is converted to voltage output by op amp A3-A and op amp A3-B for converter 1 and 2, respectively.

Voltage output equation is:

$$Vout = 4.22 * (\text{DAC Code})/4096 \text{ V}$$

The outputs of the op amps are connected via resistors to system connector for external use. Test signals DA1T and DA2T are connected to the A/D converter.

4.2.12 Clock Oscillator

TCXO type clock oscillator Z2 provides 10 MHz timing reference for MRP111. The oscillator frequency is fine-tuned by control voltage from D/A converter A9 via amplifier A8-A to the VC input.

The oscillator output is amplified by A8-B and buffered by D23 to the main 10 MHz reference.

Alternative clock oscillator Z1 is not installed.

Linear regulator A11 supplies +3.3 V operating voltage to the clock oscillator and PLL circuits.

4.2.12.1 PLL Clock Multipliers

PLL (Phase Locked Loop) clock multipliers are used to generate all required system clock signals from the 10 MHz reference clock source.

PLL circuits D35, D31 and D40 are pin-programmed for desired output frequency. Circuit D35 generates 14.3 MHz clock for ZFx86, D31 generates 48 MHz for ZFx86, and D40 generates 50 MHz for PLD logic and Ethernet clocking. The 25 MHz Ethernet clock is divided from 50 MHz output by D44-A.

PLL circuit D27 is serially programmable for desired output frequency. In standard MRP111, the output frequency is programmed to 40 MHz for DSP clock.

4.2.12.2 Voltage Regulators

Linear voltage regulators are used to generate the required +2.5 V internal operating voltages from +3.3 V system voltage.

Regulator A1 generates +2.5 V for Ethernet switch D2 and for core voltages of ZFx86 and PLD.

Regulator A7 generates +2.5 V core voltage (+VDSP) for DSP.

4.2.12.3 Reset Circuit

Circuit A10 controls the reset signal RES#, which is forced to the active low state if at least one of the following conditions appear:

- +5V operating voltage falls below +4.5 V
- +3.3V operating voltage falls below +3.0 V
- +2.5V operating voltage falls below +2.2 V
- internal reset line SELFRES# is in 0-state
- external reset line MRES# is in 0-state

The reset output signal is typically held active for 200 ms after the reset condition has disappeared.

4.2.12.4 LED Lights

The test light V1 is a red/green bi-color LED type light. The red and green lights are controlled by signals REDLED# and GRNLED# from the PLD D5. Yellow color is produced when both lights are on.

During system reset, yellow color is shown. After reset, red light remains on during the boot sequence of the control processor. When booting is complete, the red light is switched off and the green light is switched on to indicate normal device operation.

4.2.12.5 Temperature Sensor and Voltage Monitor

The temperature sensor and voltage monitor circuit A12 measures the circuit board temperature, three system voltages (+3.3V, +5V, +12V) and internal voltage +VDSP.

The sensor is controlled serially via clock (SBCLK) and data line (SBDATA). Control is performed by PC processor via chip interface in PLD.

4.2.12.6 Remote Start

The signals STRTOUT (X1/A40) and STRTIN (X1/B40) are intended for a remote start or a general-purpose event marker input. In the external circuit, STRTOUT is looped back to STRTIN via a momentary switch, and a closing (or opening) switch contact is used to indicate sounding start or an event mark. The minimum detectable pulse length is 0.1 s.

Alternatively, a ground-referenced TTL or RS232 level pulse connected to the STRTIN input can be used.

The external switch or a signal should be in an idle state during system power-up to allow the correct idle reference to be read.

4.2.12.7 Rack Code

The rack code inputs R0IN#, R1IN#, R2IN#, R3IN# and R4IN# from system connector pins A45 ... E45 are fed to control processor via PLD for information about the operating environment.

4.2.12.8 Hardware Code

The 4-bit HW code from PLD (D5-D) input pins H21, D20, E20 and J21 are fed to control processor via PLD for information about the operating hardware environment of MRP11.

4.2.12.9 Status Output

The STAT_OK control output from PLD controls the D54 buffer which drives the status signal output at system connector pin E37 to a low level when STAT_OK = 0.

Status signal output line is used at system level to indicate the status of internal units.

4.2.12.10 Test Input

Test input from system connector pin B39 is fed to control processor via PLD for testing purposes. In normal operation, the input should be left unconnected.

4.2.13 Parts List MRP111

Table 23 MRP111 Parts List

Reference	Part Number	Description
Assembly ref. 001	DRW213148	Front panel machining, A MRP111
Assembly ref. 002	210854	EMC gasket A 3U, Schroff 21101-854
Assembly ref. 003	210853	Injector/ejector handle A 4HP, IEL, Schroff
Assembly ref. 004	210856	Board holder A Schroff
Assembly ref. 005	210855	Sleeve A M 2.5x3, Schroff 21100-660
Assembly ref. 006	210857	Collar screw A M 2.5x12.3, Schroff
Assembly ref. 007	16097	ESD warning sticker A
Assembly ref. 008	210615	License sticker A EMBOS Dos 6.22 FULL RUN
Assembly ref. 009	210616	License sticker A WIN NT embedded 4.0
Assembly ref. 011	211522	MAC address for A embedded network contr.
Integrated Circuits		
A1,7	27139	IC, voltage regulator, LT1764EQ-2.5
A2, 3, 5, 8	210452	IC, op. amp. (Dual) AD8042AR (SMD)
A4	010247	IC, converter A/D, AD7723
A6	010032	IC, converter D/ AD9765AST
A9	25116	IC, converter D/AEx, LTC1453CS8
A10	010148	IC, supervisor, MAX6355SYUT-T
A11	25757	IC, voltage reg, LT1521CST-3.3
A12	25815	IC, converter A/D, AD7417ARU
D1,4,6	27162	IC, dig. down converter, HSP50216
D2	27132	IC, Ethernet switch, KS8995
D3	27129	IC, Ethernet controller, AM79C973BVC/W
D5	27133	IC, SRAM-based PLD, EP1K100F1484-2
D7	27079	IC, PC System-on-a-Chip, SOC-MZP-Q-01, ZFx86
D8	27128	IC, ATA flash disk, SST58LD064-80-I-P1H
D9, 32, 37, 42	26108	IC, RS232C transceiver, MAX208EEAG
D10,11,14,15	210862	IC, SDRAM, K4S281633D-RN75
D12	27170	IC, DSP, ADSP-21160
D13,51	27182	IC, SB SRAM 2 EA 15.04. B 512k x 32 synchronous SR

Reference	Part Number	Description
D16, 22, 28	010030	IC, LVDS serdes receiver SN65LVDS96
D17, 25, 45, 47	19568	IC, inverter tiny, NC7S14 (SMD Reel)
D18	16734	IC, EEPROM, CAT93C46JI (SMD)
D19	25495	IC, analog MUX 8ch, MAX4051ACSE
D20, 21, 23, 24, 26, 29, 30, 33, 36, 38, 39, 41, 43, 46, 48, 53, 54	26570	IC, buffer Tiny, NC7SZ125M5
D27	210412	IC, freq. synthesizer, ICS307M-02I
D31,35,40	27135	IC, freq. synthesizer, ICS525R-02I
D34	25022	IC, FLASH sectored, S29AL016DB-90EI
D44	212177	IC, Flip-Flop, 74AHC74PW
D49, 50, 52	26249	IC, bus tranceiver, 74LV245 (SMD)
Z2	210744	IC, clock oscillator, VCTCXO 10MHz, SMD
Diodes		
V1	010192	Diode, LED, 591-3001
V2,V3	210575	Diode, TVS-array 2 EA 13.02. A SMDA03LCC
Resistors		
R1, 2,10-12, 14, 15, 17, 18, 20, 31-34, 40, 42, 51, 60, 62, 67, 68, 71-73, 81, 82, 85, 87, 92, 93, 95-97, 109, 110, 125, 126, 185, 187, 188, 193, 194, 196, 203, 205, 208, 216, 220, 224, 226-229, 233, 235	26100	Resistor, chip, 100R 1.0% 100ppm 0603
R3, 4, 9, 13, 22, 27, 38, 39, 41, 45, 48, 50, 54, 64, 66, 75, 77-80, 83, 84, 86, 88-91, 99, 101-106, 112-115, 117, 118, 120-123, 127-129, 132-135, 137, 138, 140, 143, 144, 146-147, 149-151, 153-156, 159, 160, 163, 164, 166-171, 176, 178, 180-182, 184, 189, 190, 219, 230, 232, 234, 237	25262	Resistor, chip, 10K0 1.0% 100ppm 0603

Reference	Part Number	Description
R5-8,16,23-26, 29, 30, 35-37, 44, 46, 47, 49, 52, 53, 55-59, 61, 63, 65, 70, 74, 76, 94, 98, 100, 111, 116, 124, 131, 136, 139, 142, 145, 148, 152, 157, 161, 162, 165, 172-174, 177, 179, 183, 191, 192, 195, 197, 199, 202, 204, 206, 207, 209, 211-215, 217, 218, 221-223, 225, 231, 236, 238, 240, 241	25263	Resistor, chip, 1K0 1.0% 100ppm 0603
R19, 43, 69, 107, 130, 141, 158, 175, 186, 198, 200, 201, 210, 239	010014	Resistor, chip, 21R5 1% 100ppm 0603
R21, 28	25208	Resistor, chip, 1M01.0% 100ppm 0603
Capacitors		
C1	27140	Cap., chip ceramic, 1nF 10% X7R 2kV 1808
C2, 3, 5, 8, 14, 38, 40, 48, 54, 69, 70, 81	19959	Cap., chip tantalum ,10uF 10V 20% case A
C4, 6, 7, 10-13	25560	Cap., chip tantalum, 100uF 16V 20% E LowESR
C9	18524	Cap., chip ceramic Ex 1 EA 13.02. A 1n 5% NPO 50V 0805
C15-20, 23-25, 28-31, 33-37, 39, 41, 42, 45-47, 49-53, 55-57, 59, 61-68, 71-75, 77-80, 83-87, 89-92, 94-114, 117	19941	Cap., chip ceramic, 100nF 10% X7R 16V 0603
C21, 22, 93	25186	Cap., chip ceramic, 100p 5% NPO 50V 0603
C26, 27, 58, 60, 76, 88, 115, 116, 118	19405	Cap., chip ceramic, 10n 10% X7R 50V 0603
C32	19915	Cap., chip ceramic, 470nF 10% X7R 16V 0805
C43,44	15621	Cap., chip ceramic Ex, 100n 10% X7R 50V 0805
Connectors		
TP1	0172	Connector PinEx, E-309/6
X1	210249	Connector, 2 mm metric 5 x 44 socket, press-fit
X2	27134	Connector, RJ45, 95040-6885
X3	25056	Connector, D, DEJK9P4-1A7N
Miscellaneous		
L1-L4,6-14,17-23	25097	Ferrite bead inductor Ex , 2250 ohm @100MHz, 0R8
T1-3	27130	Transformer, pulse, H0013

Reference	Part Number	Description
	211738	Screw, crosshead, M2,5 x 6 DIN7985 PZ A4
	212048	Screw, crosshead A M2,5 x 8 DIN7985 PZ A4
	212049	Screw, crosshead A M2,5 x 8 DIN966 PZ A4
	5068	Screw-lock compound, Loctite 222
	6779	Nut, hexagon, M 2,5 /A4m
	7067	Washer, spring, B2,5 /A4
	DRW213149	Front panel assembly for MRP111
	PCB210052	Printed circuit board MRP111
	211284	SYM ghost 7.5 license A VAR corporate 7.5 SVLP
	15223	Sticker set A, type, barcode and serial number
	211741	Therm. conductive liquid
	16166	Plastic label
	210849	Front panel, shielded A 3U, 4HP, Schroff

4.2.14 Technical Data

Table 24 Technical Data

Digital Down Converters	
Number of converters	3
Channels in a converter	4
Clock rate	64 MHz
Programmable carrier	NCO 32-Bit
FIR out of band attenuation	110 dB
Digital AGC	96 dB gain range
Digital Signal Processor	
Processor type	ADSP-21160
Clock rate	80 MHz
Internal memory	524 Kbyte
External memory	4 MBytes
Link ports	6
Serial ports	2
Control Processor	

Digital Down Converters	
Processor type	ZFx86
Clock rate	96 MHz
SDRAM	64 MBytes
FLASH PROM	2 MBytes
ATA/IDE flash disk	64 MBytes
Communication channels	
Ethernet port	10/100 Mbits/s
Switch port outputs	3 ports
Serial lines	RS232-C, two channels
Power requirements	
+3.3 V	4500 mA
+5 V	200 mA
+12 V	2 mA
-12 V	10 mA
Operating temperature	-30 ... +55°C
Storage temperature	-55 ... +80°C
Unit type	E1-size circuit board
Length, width, height	190 x 128 x 20.5 mm
Weight	350 g
System connector	220-pin female
Status indicators	LED light

4.2.15 COM1 Connector

Serial port 1 with handshake controls is for testing and maintenance.

Type of connector: 9 pin male D connector.

Table 25 COM1 Connector Signal List and Layout

Signal	Pin	Description	Level
DCD	1	Carrier detect	RS232
RXD	2	Received serial data	RS232
TXD	3	Transmitted serial data	RS232
DTR	4	Data terminal ready	RS232
GND	5	Common (signal ground)	-

Signal	Pin	Description	Level
DSR	6	Data set ready	RS232
RTS	7	Request to send	RS232
CTS	8	Clear to send	RS232
RI	9	Ring indicator	RS232

4.2.16 Ethernet Connector

Type of connector: RJ45

Table 26 ETH Connector Signal List and Layout

Signal	Pin	Description
E1TX+	1	Transmit signal pair
E1TX-	2	Transmit signal pair
E1RX+	3	Receive signal pair
	4	
	5	
E1RX-	6	Receive signal pair
	7	
	8	

4.2.17 System Connector MRP111

System connector is a 220-pin, 5-row female Euro connector.

Table 27 System Connector Signal Layout

Pin/Row	A	B	C	D	E
1	GND	GND	GND	GND	GND
2	SPCTRL	GND	MRRMUX	GND	ANTIN
3	TS1	TS2	TS3	TS4	TS5
4	ADDITH				
5	FOUT+	FOUT-	GND	DSPEMU#	JTDIPLD
6	GND	GND	GND	GND	GND
7	SR1SD0	SR1SD0#	GND	SR1SD1	SR1SD1#
8	GND	GND	GND	GND	GND
9	SR1SD2	SR1SD2#	GND	SR1CLK	SR1CLK#

Pin/Row	A	B	C	D	E
10	GND	GND	GND	GND	GND
11	SR2SD0	SR2SD0#	GND	SR2SD1	SR2SD1#
12	GND	GND	GND	GND	GND
13	SR2SD2	SR2SD2#	GND	SR2CLK	SR2CLK#
14	GND	GND	GND	GND	GND
15	SR3SD0	SR3SD0#	GND	SR3SD1	SR3SD1#
16	GND	GND	GND	GND	GND
17	SR3SD2	SR3SD2#	GND	SR3CLK	SR3CLK#
18	GND	GND	GND	GND	GND
19	TXD4	GPIOUT5	GPIOUT6	GPIOUT7	
20	RXD4	GPIN5	GPIN6		
21	TXD3	GPIOUT1	GPIOUT2	GPIOUT3	GPIOUT4
22	RXD3	GPIN1	GPIN2	GPIN3	GPIN4
23	GND	GND	GND	GND	GND
24	E2RX+	E2RX-	GND	E2TX+	E2TX-
25	GND	GND	GND	GND	GND
26	E1RX+	E1RX-	GND	E1TX+	E1TX-
27	GND	GND	GND	GND	GND
28					
29					
30	TXD2				
31	RXD2				
32	TXD1SC				
33	RXD1SC				
Key area					
37	DA1OUT	GND	SYSRES#		STATUS
38	JTDO	JTCKIN	JTRIN#	JTDIN	JTMSIN
39	1PPS	TEST#		DA2OUT	GND
40	STRTOUP	STRTIN			
41				BTOUT5#	BTOUT6#
42	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V
43	BTOUT0#	BTOUT1#	BTOUT2#	BTOUT3#	BTOUT4#
44	+5V	+5V	+5V	+5V	+5V

Pin/Row	A	B	C	D	E
45	ROIN#	R1IN3	R2IN#	R3IN#	R4IN#
46	+12V	+12V	GND	-12V	-12V
47	GND	GND	GND	GND	GND

4.2.18 List of Signals

The following signal names and abbreviations are used throughout the text and drawings of MRP111.

Table 28 List of Signals

Signal	Description
+12V	+12 V operating voltage
+2.5V	+2.5 V operating voltage
+3.3V	+3.3 V operating voltage
+3.3VOSC	+3.3 V oscillator operating voltage
+5V	+5 V operating voltage
+VDSP	+ V DSP operating voltage
10MHZ	10 MHz clock signal
10MHZ+	10 MHz clock signal
10MHZ-	10 MHz clock signal
12M5HZ	12.5 MHz clock signal
14.3MHZ	14.3 MHz clock signal
1PPS#	1 pulse per second
25MHZ	25 MHz clock signal
48MHZ	48 MHz clock signal
50MHZ	50 MHz clock signal
ADAOR	Analog to digital converter A overrange
ADBOR	Analog to digital converter A overrange
ADCCFMT	Analog to digital converter serial clock format
ADCCLK	Analog to digital converter clock
ADCFSI	Analog to digital converter frame sync input
ADCFSO	Analog to digital converter frame sync output
ADCOR	Analog to digital converter A overrange
ADCSCO	Analog to digital converter serial clock output

ADCSCR	Analog to digital converter serial clock rate select
ADCSDO	Analog to digital converter serial data output
ADCSFMT	Analog to digital converter serial data format select
ADCSLDR	Analog to digital converter serial low data rate
ADCSLP	Analog to digital converter serial mode low pass filter
ADCUNI	Analog to digital converter unipolar input
ADDITH	Analog to digital converter dither
ADSELO ... 2	Analog to digital converter input select signals
AGND	Analog ground
ANTIN	Antenna input
BALE	Bus address latch enable
BT0# ... 6#	Boot signal
BTOUT0# ... 6#	Boot signal out
CS16#	Chip select 16-bit
CTS1ZF	Clear to send 1 to ZFx86 processor
DA1OUT	Digital to analog converter 1 output
DA1T	Digital to analog converter 1 test signal
DA2OUT	Digital to analog converter 2 output
DA2T	Digital to analog converter 2 test signal
DA4LD#	Digital to analog converter data load
DAD00 ... 11	Digital to analog converter data 00 ... 11
DC1(2,3)CE#	Digital down converter 1 (2,3) chip enable
DC1(2,3)CLK	Digital down converter 1 (2,3) clock
DC1(2,3)CSEL1	Digital down converter 1 (2,3) clock select 1
DC1(2,3)CSEL2	Digital down converter 1 (2,3) clock select 2
DC1(2,3)ENI#	Digital down converter 1 (2,3) enable
DC1(2,3)INTR#	Digital down converter 1 (2,3) interrupt
DC1(2,3)RST#	Digital down converter 1 (2,3) reset
DC1(2,3)SCLK	Digital down converter 1 (2,3) serial data clock
DC1(2,3)SD1A	Digital down converter 1 (2,3) serial data 1 A
DC1(2,3)SD1B	Digital down converter 1 (2,3) serial data 1 B
DC1(2,3)SYNA	Digital down converter 1 (2,3) sync A
DC1(2,3)SYNB	Digital down converter 1 (2,3) sync B
DC1(2,3)SYNC	Digital down converter 1 (2,3) sync input

DC2CSEL3	Digital down converter 2 clock select 3
DCA0 ... 2	Digital down converter address 0 ... 2
DCD00 ... 15	Digital down converter data 00 ... 15
DCD1	Data carrier detect 1
DCD1ZF	Data carrier detect 1 to ZFx86
DCRD#	Digital down converter read
DCWR#	Digital down converter write
DD00 ... 15	Disk data 00 ... 15
DEVSEL#	Device select
DISKWP#	Disk write protect
DRQ1 (5)	Direct memory access request 1 (5)
DSCLDIS#	DSP start clock disable
DSDRO (1)	DSP serial port data 0 (1) receive
DSDTO (1)	DSP serial port data 0 (1) transmit
DSP	Digital signal processor
DSPA01 ... 21	DSP address 00 ... 21
DSPBRST	DSP burst
DSPCLK	DSP clock
DSPCLKM0	DSP clock mode
DSPD00 ... 63	DSP data 00 ... 63
DSPEMU#	DSP emulator
DSPFLO ... 3	DSP flag 0 ... 3
DSPIRQ0# ... 2#	DSP interrupt request 0# ... 2#
DSPMS0#	DSP memory select 0
DSPRDH#	DSP read high end data
DSPRDL#	DSP read low end data
DSPRST#	DSP reset
DSPTIMER	DSP timer
DSPWRH#	DSP write high end data
DSPWRL#	DSP write low end data
DSR1	Data set ready 1
DSR1ZF	Data set ready 1 to ZFx86
DSRCLK0	DSP serial port receive clock 0
DSRCLK1	DSP serial port receive clock 1

DSRFS0	DSP serial port receive frame sync 0
DSRFS1	DSP serial port receive frame sync 1
DSTCLK0	DSP serial port transmit clock 0
DSTCLK1	DSP serial port transmit clock 0
DSTFS0	DSP serial port transmit frame sync 0
DSTFS1	DSP serial port transmit frame sync 1
DTR1	Data terminal ready 1
E1(2,3)RX+/-	Ethernet port 1 (2,3) receive signal pair
E1(2,3)TX+/-	Ethernet port 1 (2,3) transmit signal pair
ET1(2,3,4)ADIS	Ethernet port 1 (2,3,4) automatic configure disable
FRAME#	Cycle frame (PCI bus signal)
FSA20	Flash address 20
GND	Ground
GNT0#	Grant 0 (PCI bus signal)
GPIN1(#)...6(#)	General purpose input 1 ... 6
GPIO5 ... 7	General purpose input/output 5 ... 7
GPIOUT1(#)...7(#)	General purpose output 1 ... 7
GRNLED#	Green LED light control
I/O	Input / output
IOCHRDY	I/O channel ready (ISA bus signal)
IOCS0#...3#	I/O chip select 0 ... 3 (ISA bus signal)
IOCS16#	I/O chip select 16-bit (ISA bus signal)
IORD#	I/O bus read strobe (ISA bus signal)
IOWR#	I/O bus write strobe (ISA bus signal)
IRDY#	Initiator Ready (PCI bus signal)
ISA	Industry Standard Architecture
ISACLK	ISA bus clock
ISAERR#	ISA bus error
JTAG	Joint test action group
JTCDIS	JTAG test clock disable
JTCK	JTAG test clock
JTCKIN	JTAG bus test clock input
JTDI	JTAG test data input
JTDIN	JTAG bus test data input

JTDIPLD	JTAG test data input PLD
JTDO	JTAG test data output
JTMS	JTAG bus test mode select
JTMSIN	JTAG test mode select
JTR#	JTAG test reset input
JTRIN#	JTAG bus test reset input
KSRES#	Ethernet switch reset
LP0(1,2,3,4,5)ACK	Link port 0 (1,2,3,4,5) acknowledge
LP0(1,2,3,4,5)CLK	Link port 0 (1,2,3,4,5) clock
LP0(1,2,3,4,5)DO ... 7	Link port 0 (1,2,3,4,5) data 0 ... 7
MEMCS0(1)#	Memory select 0 (1) (ISA bus signal)
MEMRD#	Memory read strobe (ISA bus signal)
MEMWR#	Memory write strobe (ISA bus signal)
MRRMUX	Receiver board (MRR) multiplexer output signal
MUXFREQ	Multiplexer output signal frequency
MZINTA#	ZFx86 processor interrupt acknowledge
MZIRQ10	ZFx86 processor interrupt request 10
MZIRQ12	ZFx86 processor interrupt request 12
MZIRQ14	ZFx86 processor interrupt request 14
MZIRQ15	ZFx86 processor interrupt request 15
MZIRQ5	ZFx86 processor interrupt request 5
MZIRQ7	ZFx86 processor interrupt request 7
PAR	PCI parity
PCAD00 ... 31	PCI address / data 00 ... 31
PCBE0# ... 3#	PCI byte enable 0 ... 3
PCICLK	PCI clock
PCRES#	PCI reset
PERR#	PCI parity error
PLD	Programmable logic device
PLLID	Phase locked loop load
PMEMWR#	Protected memory write
RO(1,2,3,4)IN#	Rack code 0 (1,2,3,4) input
RA0# ... 4#	Rack address 0 ... 4
RD1FP	Received data 1 from front panel

RD1SC	Received data 1 from system connector
RD1ZF	Received data 1 to ZFx86
RD2ZF	Received data 2 to ZFx86
RD3P	Received data 3 to PLD
RD4P	Received data 4 to PLD
RDA00 ... 15	Received data A 00 ... 15
RDB00 ... 15	Received data B 00 ... 15
RDC00 ... 15	Received data C 00 ... 15
REDLED#	Red led control
REQ0#	PCI bus request
RES#	Reset
RI1ZF	Ring indicator to ZFx86
ROM	Read only memory
RSTDdrv	Reset drive
RTCLK	Real time clock
RTS1	Request to send 1
RXD1 ... 4	Received data line 1 ... 4
RXD1SC	Received data line 1 from system connector
SA00 ... 19	ISA address 00 ... 19
SBCLK	Serial bus clock
SBDATA	Serial bus data
SBHE#	ISA bus high byte enable
SD00 ... 15	ISA bus data 00 ... 15
SDRAM	Synchronous dynamic random access memory
SDA00	SDRAM address 00 ... 13
SDCAS#	SDRAM column address strobe
SDCLK0 ... 1	SDRAM clock 1 ... 2
SDCLKE	SDRAM clock enable
SDCS0# ... S1#	SDRAM chip select 0 ... 1
SDD00 ... 32	SDRAM data 00 ... 31
SDQMO# ... 3#	SDRAM byte mask 0 ... 3
SDRAS#	SDRAM row address strobe
SDWE#	SDRAM write enable strobe
SELFRES#	Self-reset

SERCCLK	Serial control clock
SERCD	Serial control data
SERR#	PCI system error
SPCTRL	Spare control
SPOUT1	Spare output 1
SR1(2,3)CLK/CLK#	SERDES 1 (2, 3) clock signal pair
SR1(2,3)SD0/0#	SERDES 1 (2,3) data 0 signal pair
SR1SD1/1#	SERDES 1 (2,3) data 1 signal pair
SR1SD2/2#	SERDES 1 (2,3) data 2 signal pair
SR1(2,3)TDO ... 2	SERDES 1 (2,3) test data 0 ... 2
SRSDN#	SERDES shut down
STAT_OK	Status OK
STOP#	PCI stop
STRTIN#	Start signal input
STRTOOUT#	Start signal output
SYSRES#	System reset
TD1(2)ZF	Transmitted data 1 (2) from ZFx86
TD3P	Transmitted data 3 (4) from PLD
TEST#	Test signal
TRDY#	PCI target ready
TS1 ... 5	Test signal 1 ... 5
TXD1 ... 4	Transmitted data line 1 ... 4
TXD1SC	Transmitted data line 1 system connector
ZFWDI	ZFx86 watchdog input
ZFWDO	ZFx86 watchdog output
ZWS#	Zero wait states

4.2.19 Diagrams and Board Layouts MRP111

Table 29 MRP111 Diagrams and Board Layouts

Code	Description
DRW216030	Receiver Processor MRP111 Block Diagram
DRW211705	Receiver Processor MRP111 Circuit Diagram,7 pages
DRW211706	Receiver Processor MRP111 Components Layout, 2 pages

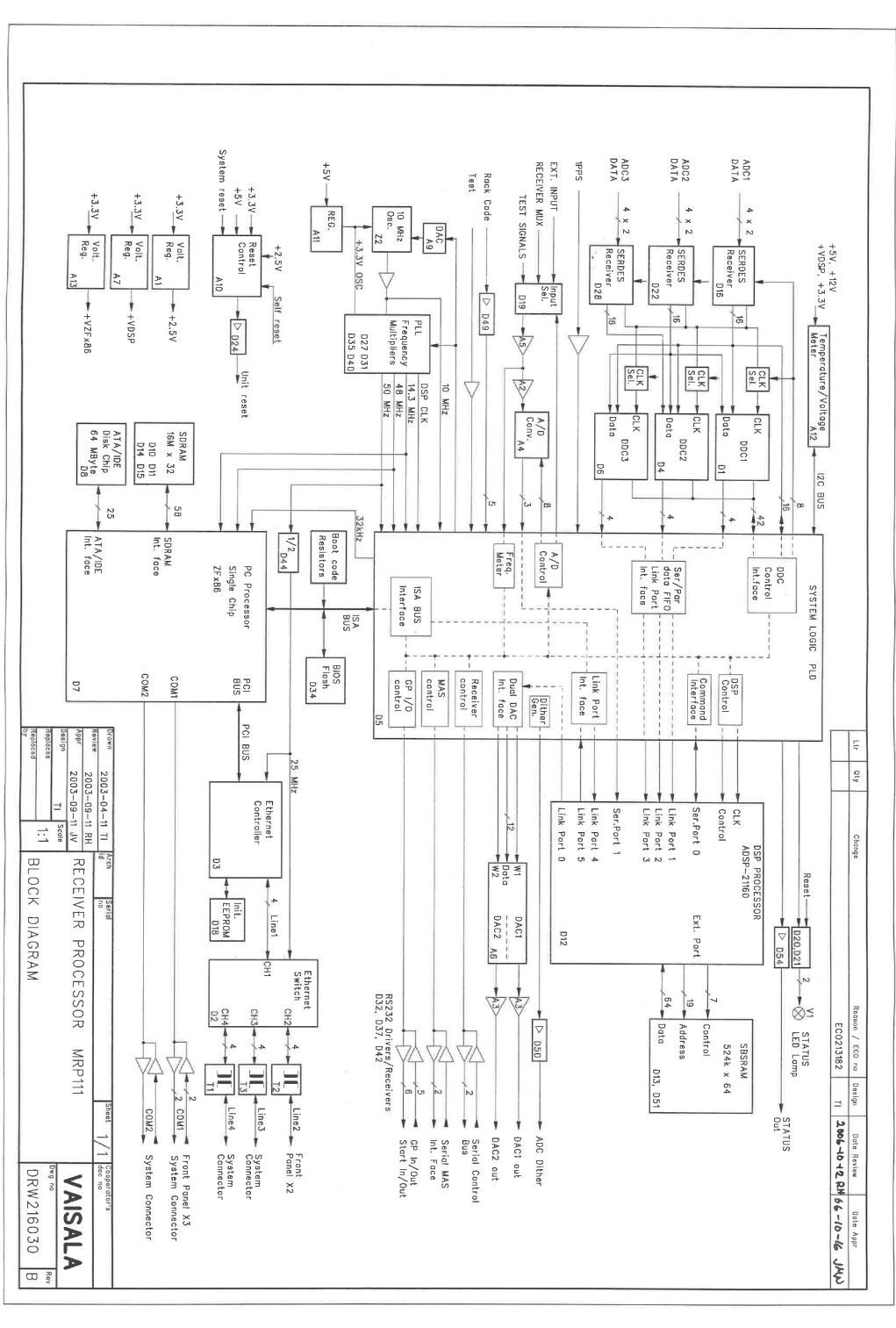


Figure 24 MRP111 Block Diagram

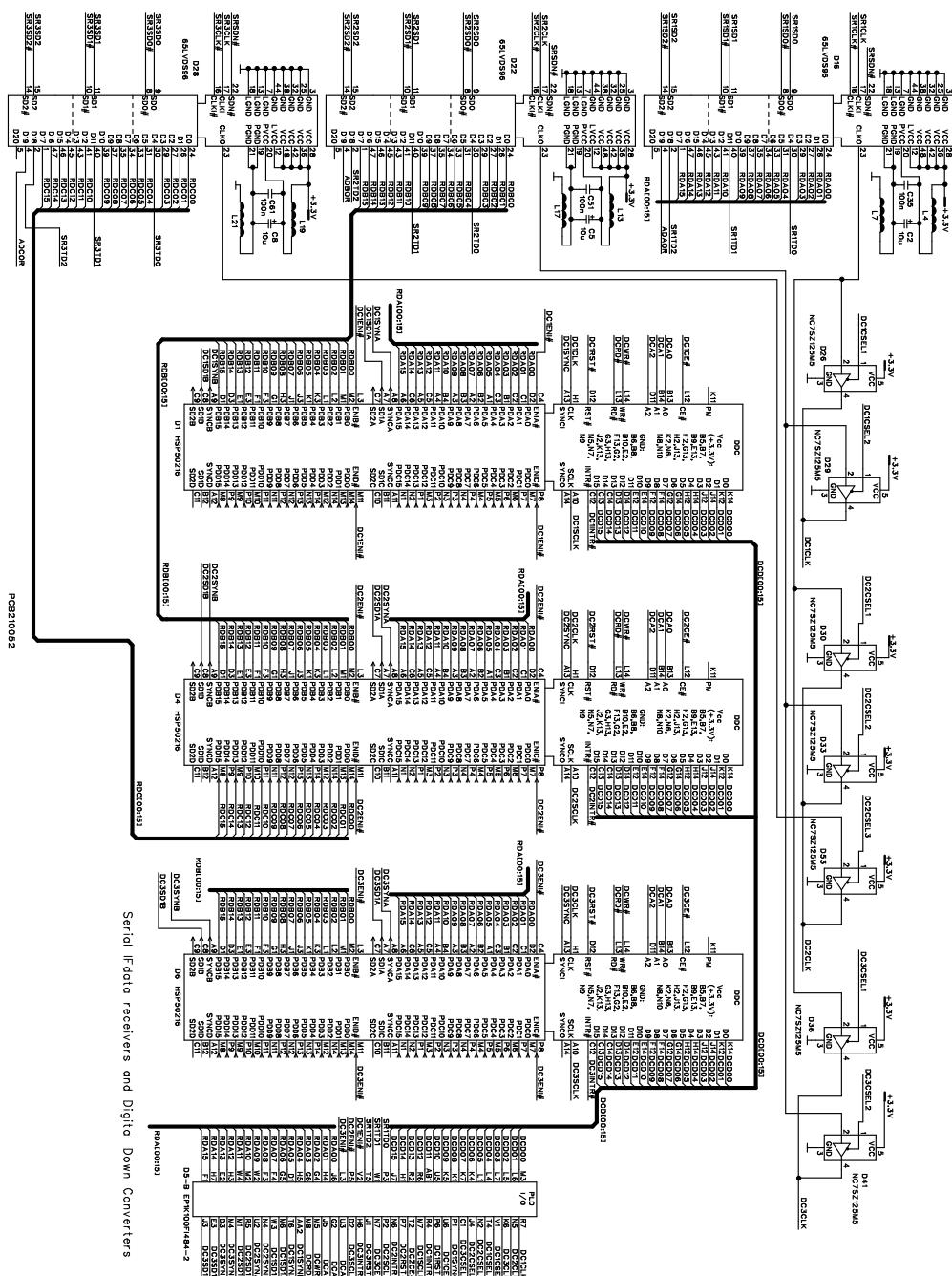


Figure 25 MRP11 Circuit Diagram 1/7

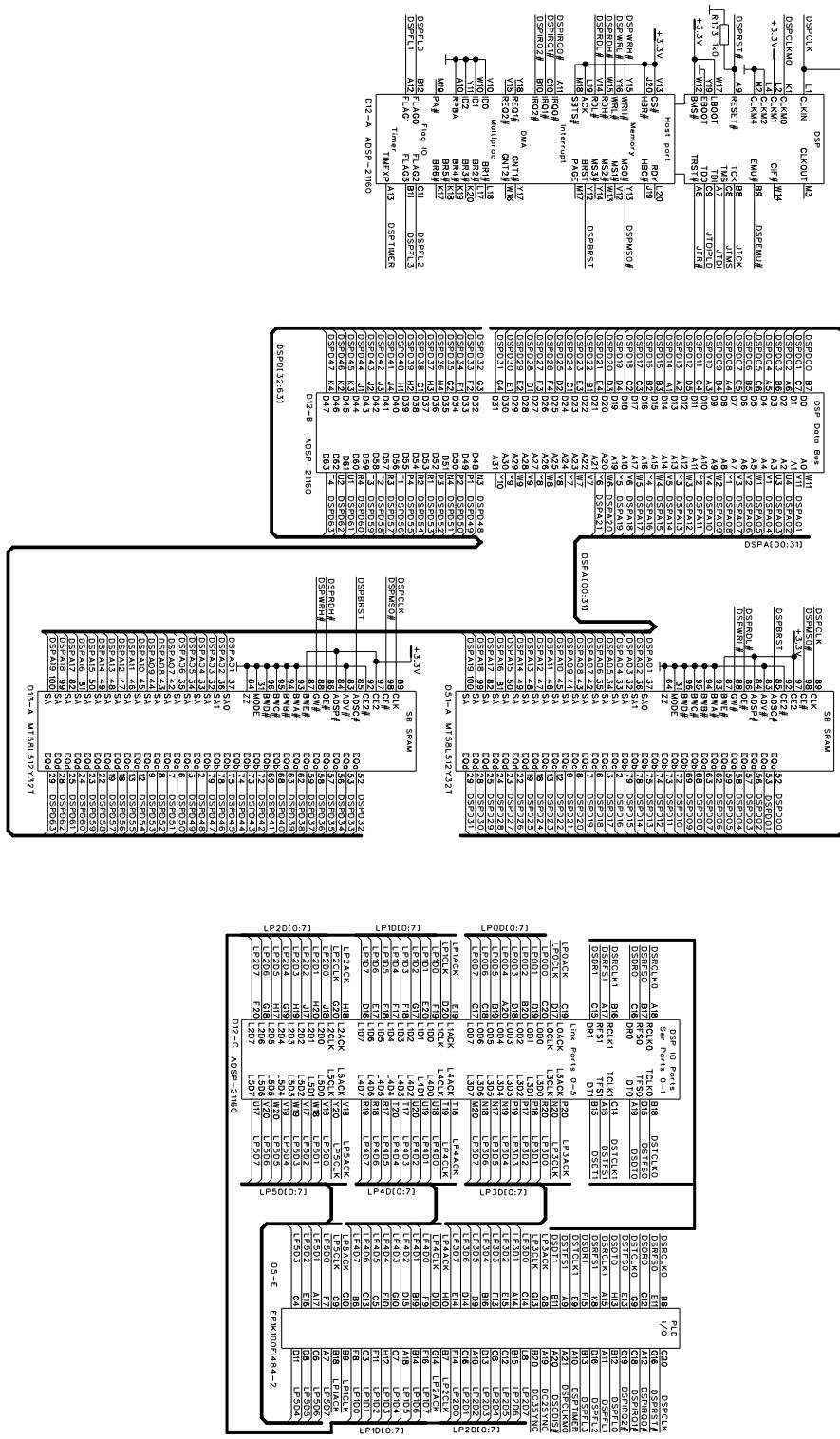


Figure 26 MRP111 Circuit Diagram 2/7

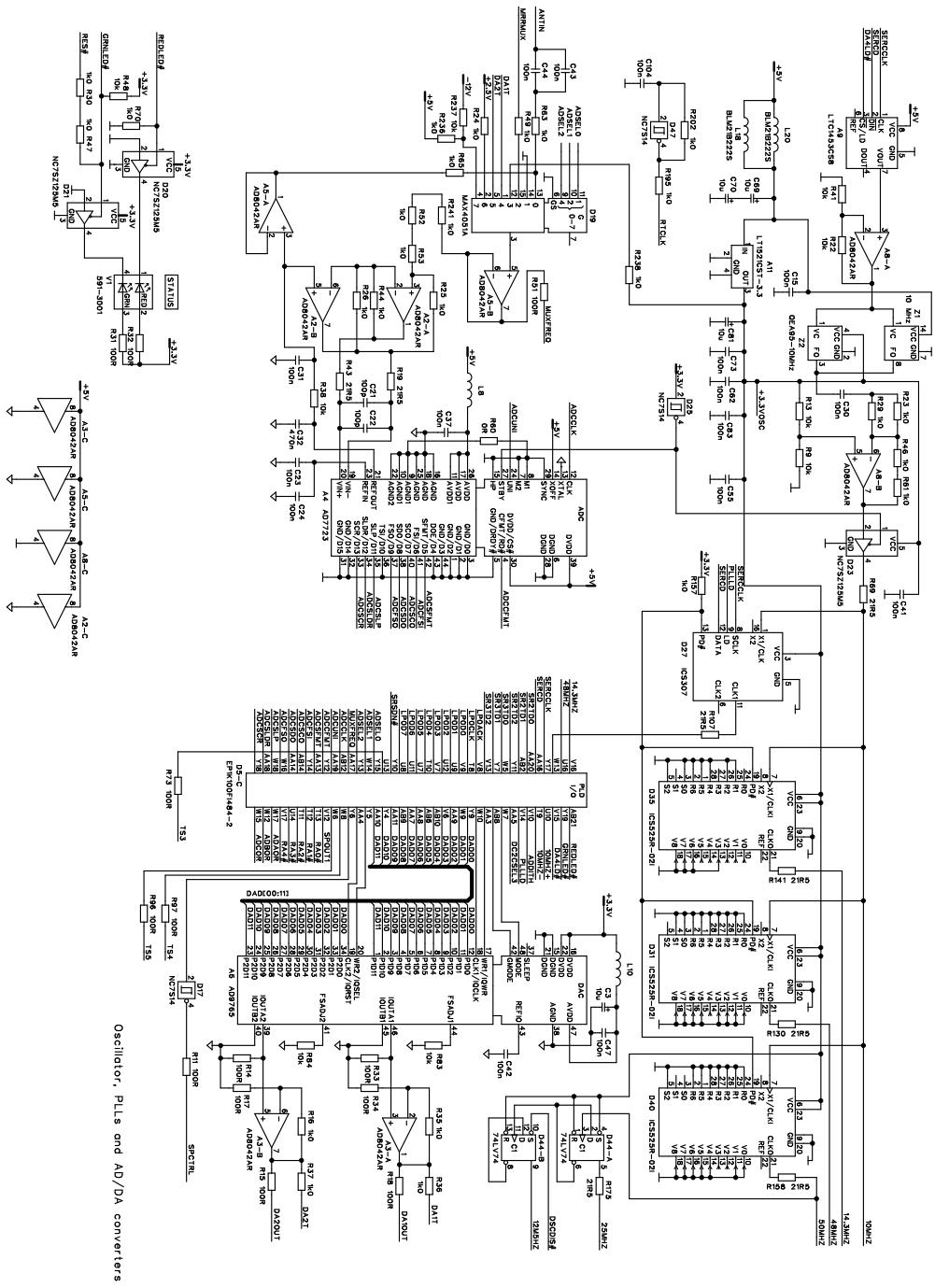


Figure 27 MRP111 Circuit Diagram 3/7

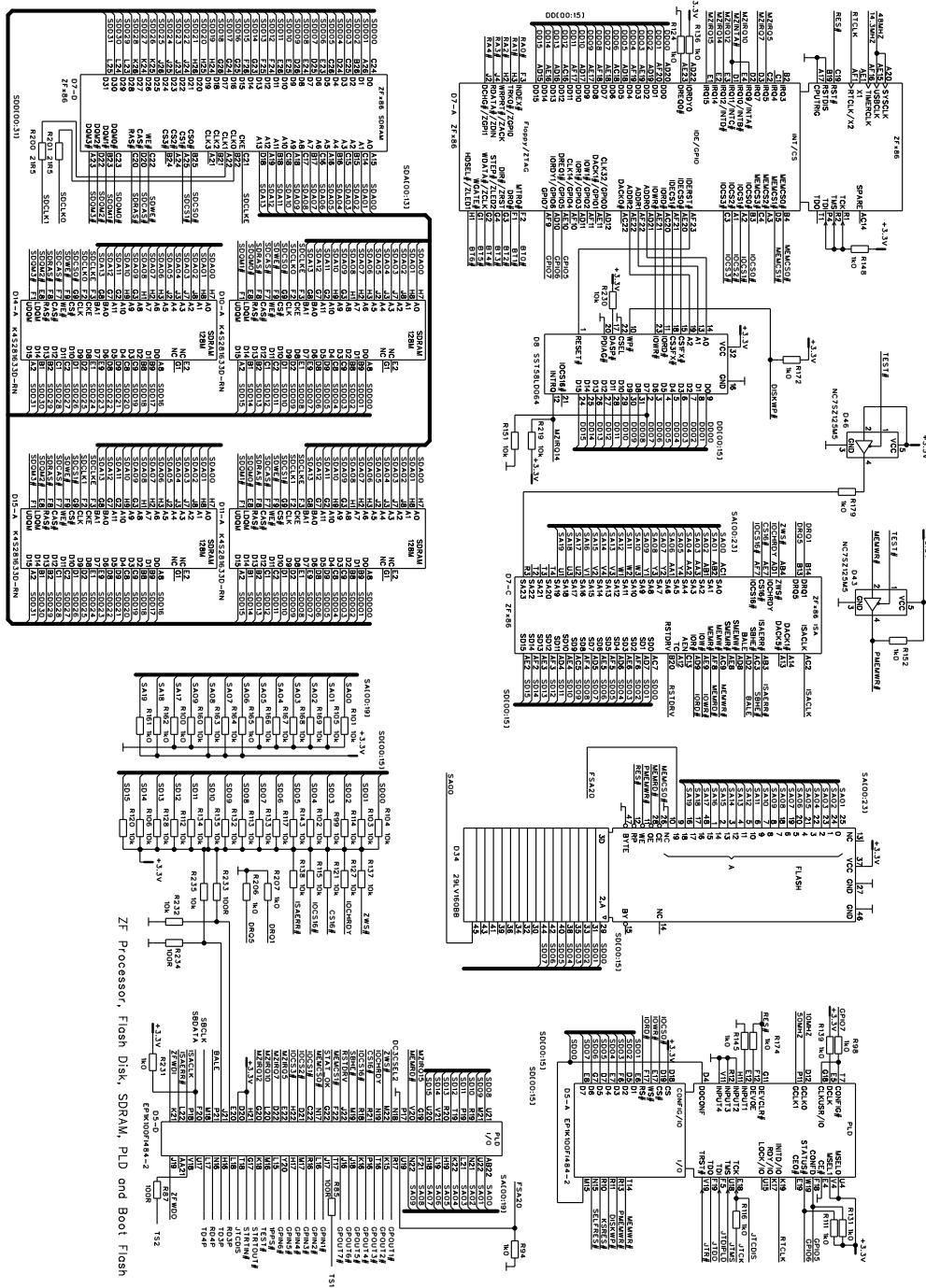


Figure 28 MRP111 Circuit Diagram 4/7

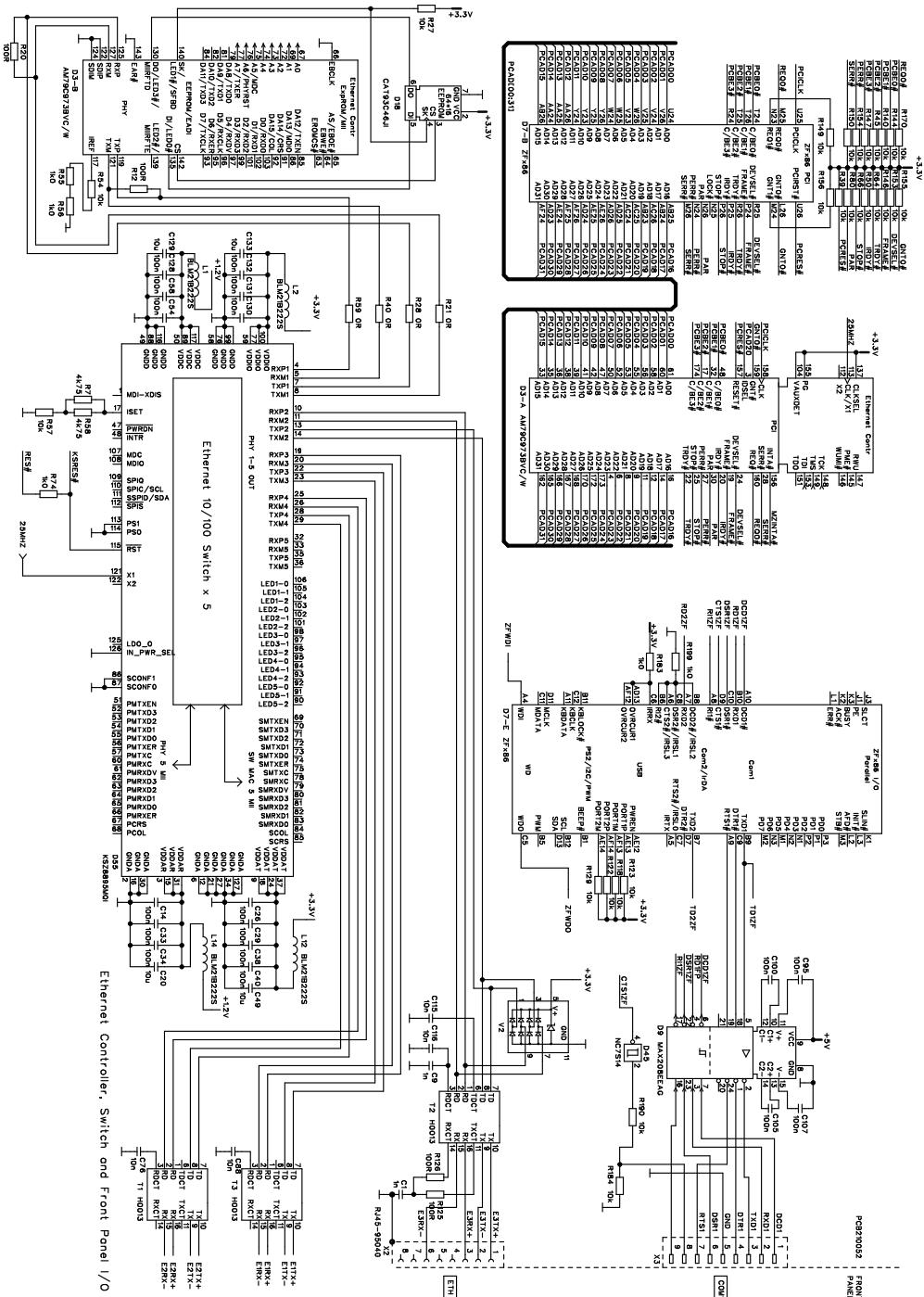


Figure 29 MRP11 Circuit Diagram 5/7

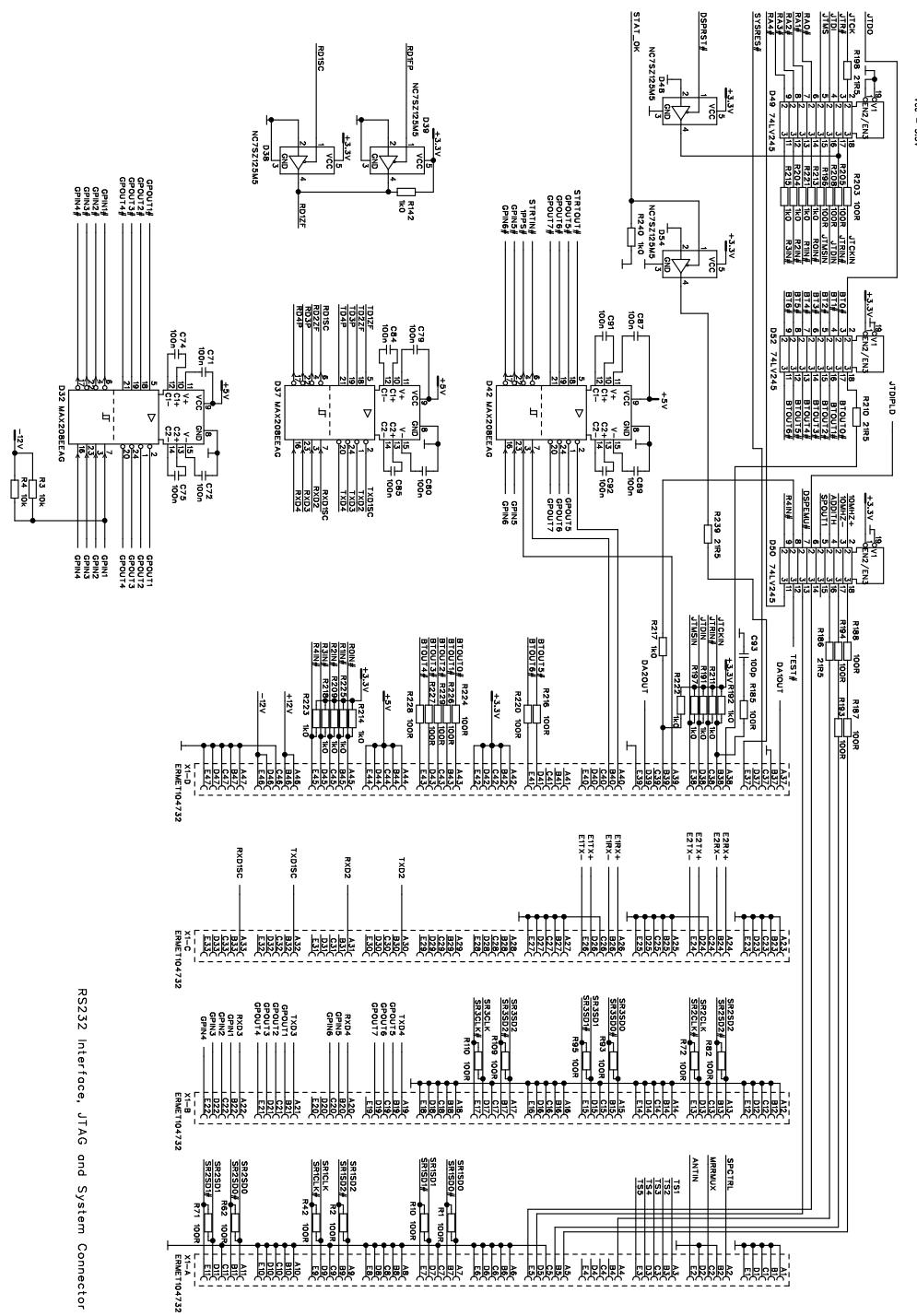


Figure 30 MRP111 Circuit Diagram 6/7

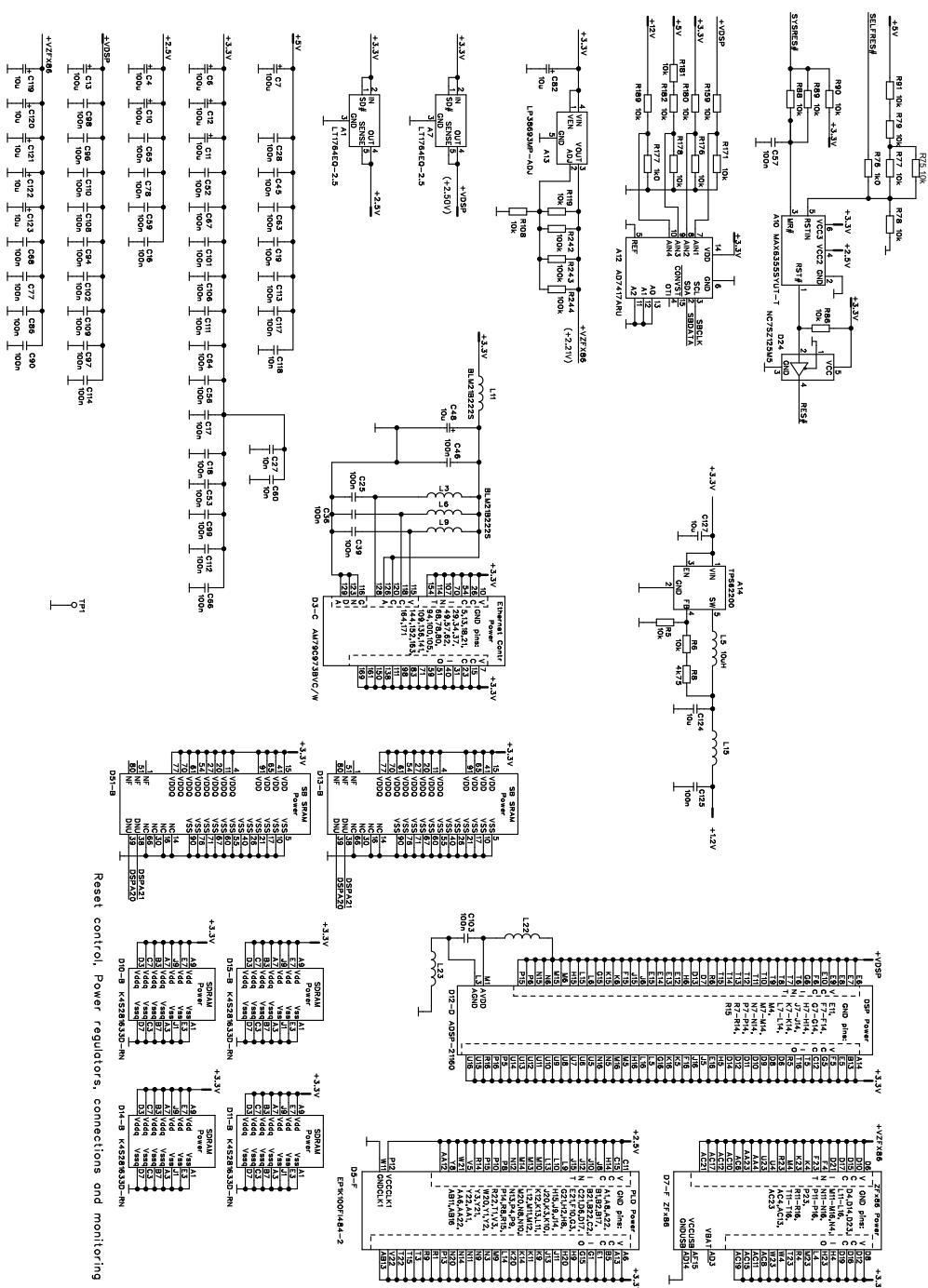


Figure 31 MRP111 Circuit Diagram 7/7

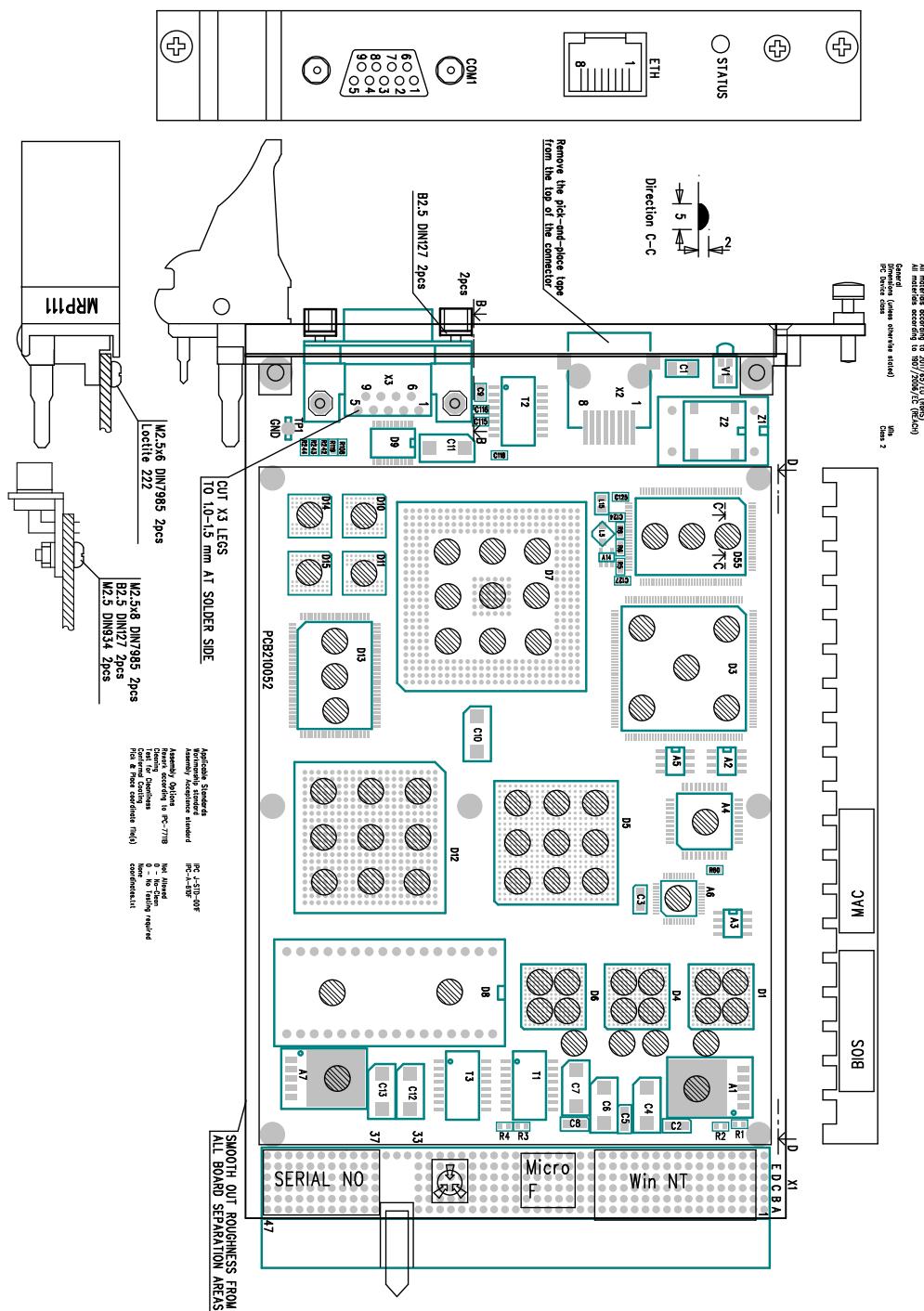


Figure 32 MRP111 Components Layout 1/2

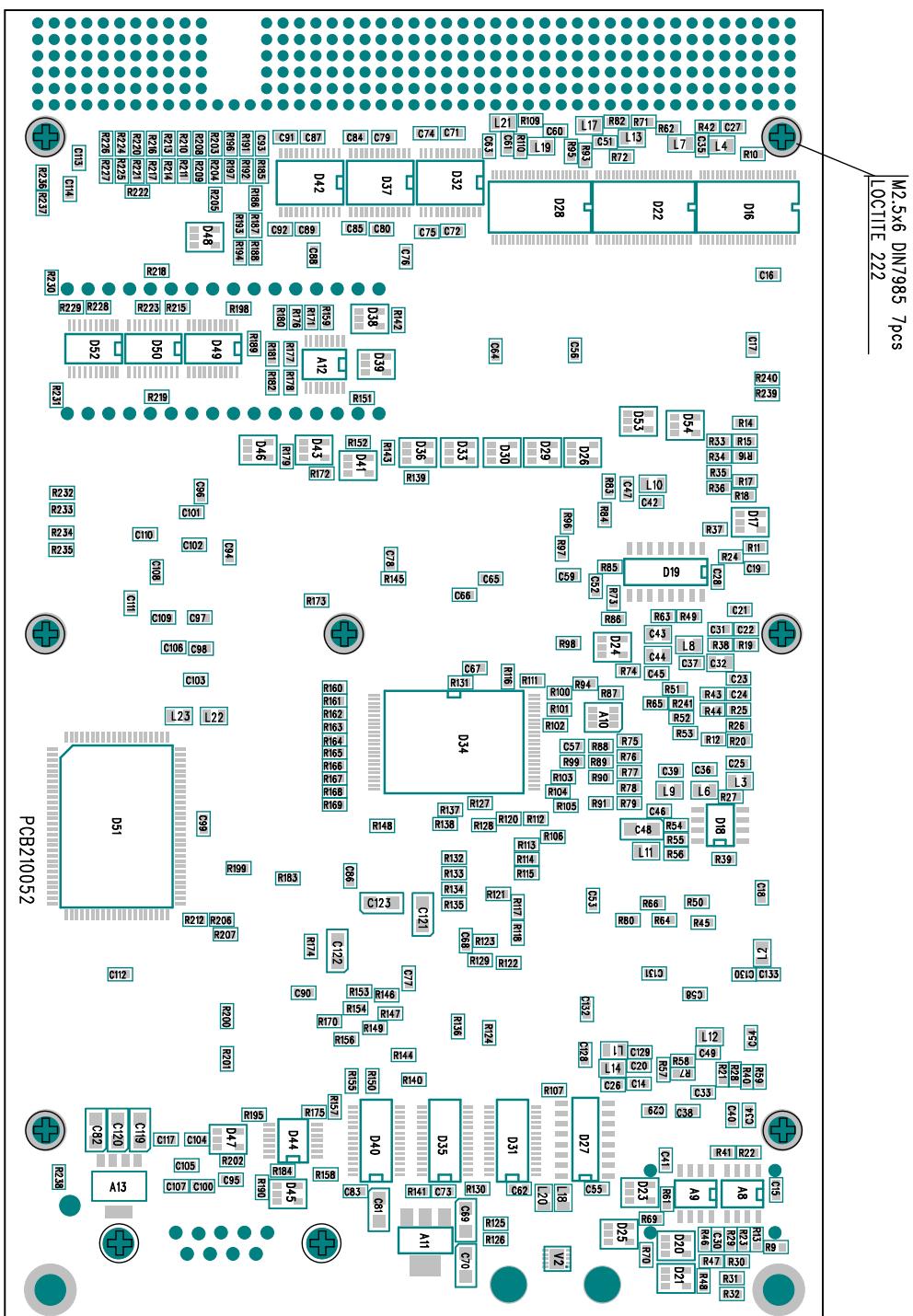


Figure 33 MRP11 Components Layout 2/2

4.3 GPS Receiver Unit MRG114

GPS Receiver Unit MRG114 is a plug-in unit of E1-size Euro card. It is used to add GPS-based wind finding capability to the sounding system. The GPS module is installed on the Euro card base unit. The signal from the local GPS antenna is connected via a base unit to the GPS module. One serial data channel is provided for external communication.

The GPS module is used for receiving satellite orbital data, synchronizing with GPS time, extracting local receiver position and velocity and for receiving local GPS signals to be used in differential wind calculation.

The base unit contains a component board, a system connector and a front plate. The local antenna connector and the status LED light is located on the front plate. An automatic line switch is also located in the base unit.

The automatic serial line switch is provided for the main serial channel. The switch enables MRG114 to be used in parallel with an optional external GPS receiver using the same communication channel. At power-up, MRG114 monitors the line voltage levels and does not connect into the line, if an active external device is present.

4.3.1 GPS Receiver and Connections

The GPS receiver is based on LEA-6T-0 receiver module (A1). The GPS module is an independent GPS receiver for local channel L1-band GPS signals. The GPS receiver is based on a commercial 50-channel receiver module, which provides precision timing and raw data outputs.

The local signal is connected from the local GPS antenna to the module via the front panel GPS antenna connector (X2). The current limited supply voltage +5 V is connected via the module to the low-noise-amplifier of the local antenna. The RF signal and the supply voltage share the same path.

The reset input MRES# is provided for full initialization of the GPS module (A1) and PLD (D2). The signal is activated when MRES# (X1/c37) is active low, or buffer D3/4 output is active high.

The exact GPS timing is provided with the 1PPS signal. Signal 1PPS is connected via buffer D5 to the system connector X1. Signal 1PPS is optional.

4.3.2 Programmable Logic Device

The programmable logic device (PLD) D2 is used to control the reset function, the LED light, and the serial channel connections in the unit.

The PLD is factory-programmed via a programming interface consisting of signals TDI, TDO, TCK, and TMS.

The inverter gate D1 is connected as an oscillator and it supplies a 150-kHz clock signal for D2.

4.3.3 Antenna Connection

The GPS antenna signal is connected from the GPS ANT connector via a strip line to the RF input (A1/16) of the GPS module.

The power feed for the external antenna amplifier is provided from +5 VDC system voltage via an RF input. The regulator A2 is used to limit the worst-case short circuit current below 450 mA. The regulator output is fed via an open circuit detector and filter chokes (Z1, Z3) to the receiver module V_ANT input, from where it is internally connected to the RF input via a short circuit protection switch and bias-T coil.

Transistors V2 and V3 with shunt resistor R12 work as detectors for the open antenna circuit. If the antenna current is below 3...5 mA, the transistor V5 conducts the driving D2/R1 input at high level for indication of an open antenna circuit. The antenna detector is optional.

The short circuit detector and the protection switch are provided as internal functions of the GPS module.

4.3.4 Serial Line Switch

Serial channel 1 from system connector (TXD1, RXD1) is connected to the GPS module via RS232 transceiver D4 and PLD D2.

Transceiver lines D4/7 and D4/9 are used to connect transceiver signal TXD1 from the GPS module. Line can be open (D4/TXEN is low) or connected (D4/TXEN is high), and it is controlled by PLD D2/H16.

Line signal TXD1 is connected to the line voltage detector, which consists of diode V4 and resistor R10. The detector output at V4 cathode is at low state if the line voltage is below -3 V. The output is connected to the PLD for line switch control.

Receiver line D4/13 is used to connect the receive signal RXD1 to the GPS module.

After power-up or reset, D4/TXEN is low to allow the line voltage detector to monitor the TXD1 line. According to the detector output D4/11, the PLD logic determines the line status as “idle” or “externally driven” at 200 ms intervals. The status is “externally driven” if the line voltage has been below -3 V for more than 5% of the time in the preceding 200 ms period. Otherwise the status is determined as idle.

The current line status is used to lock the transceiver control at the time when the first rising edge is received in RXD1 line at D2/F16. Outputs D4/7 and D4/9 are high impedance, if the line status is “externally driven”. In this case the system uses external receiver and MRG114 is left unconnected. In the opposite case the switches are closed and the system starts to communicate with MRG114. Outputs D4/7 and D4/9 are always high impedance at the time of switch locking. The locked switch settings are permanent until the next power-up or reset.

In the RS232 transceiver D4 both TXD and RXD signals are ESD-protected ± 15 kV. TXD signals can withstand ± 13 V voltages and continuous short circuit. RXD signals can withstand ± 25 V voltages.

4.3.5 LED Light Operation

The tricolor STATUS LED light V1 shows the status of the MRG114 unit. It is controlled by signals D2/E1 and D2/D1. Depending on the status of MRG114, the light is

- red ($D2/E1 = 0$)
- green ($D2/D1 = 0$)
- yellow ($D2/E1 = 0$ and $D2/D1 = 0$), or
- the light is dark (both controls are inactive).

During an active reset the LED light V1 is yellow, and after reset the light flashes green until the serial line switch is set for external or internal operation. Internal operation is indicated by a solid green light, and external operation is indicated by a yellow light.

4.3.6 Parts List MRG114

Table 30 Special Parts

Reference	Part Number	Description
Assembly ref. 1	DRW227304	Front panel
Assembly ref. 2	16166	Type sticker
Assembly ref. 3	10948	Static Sensitive sticker
Assembly ref. 4	15223	Serial No sticker

Table 31 Integrated Circuits

Reference	Part Number	Description
D1, 3	19568	IC, inverter Tiny, NC7S14
D2	217031	IC, CPLD, EPM570F256I5N
D4	219192	IC, RS232 transceiver, MAX3322EEUP
D5-7	26570	IC, buffer Tiny, NC7SZ125
A1	234471	GPS receiver module, uBlox LEA-6T-0
A2	217103	IC, voltage reg., LP2981IM5-5.0
A3	226474	IC, voltage reg., LT1521IST-3.3

Table 32 Transistors and Diodes

Reference	Part Number	Description
V1	010192	Diode, tricolor LED, 591-3001
V2, 3	11138	Transistor, PNP, MMBT3906
V4	16059	Diode, Zener, BZV55C3V9
V5, 6	17311	Diode, Transil, SM6T30CA
V7	17332	Diode, Transil, P6SMB6.8AT3

Table 33 Resistors

Reference	Part Number	Description
R1, 2, 18	26100	Resistor, chip, 100R 1.0% 100ppm 0603
R3, 8-11, 13, 14, 17, 19, 20	25262	Resistor, chip, 10K 1.0% 100ppm 0603
R4-7, 15	25263	Resistor, chip, 1k0 1.0% 100ppm 0603
R12	214629	Resistor, chip, 10R 1.0% 50ppm 1206

Table 34 Capacitors

Reference	Part Number	Description
C1, 5, 19	18524	Cap., chip ceramic, 1n 5% NPO 50V 0805
C2-4, 6-12, 15-17	19941	Cap., chip ceramic, 100n 10% X7R 16V 0603
C13, 18, 21	19462	Cap., chip ceramic, 2u2 20% X5R 16V 1206
C14, 20	217767	Cap., chip tantalum, 100uF 16V 10% Case D

Table 35 Filter

Reference	Part Number	Description
Z1-3	25036	Filter, EMI, NFE61PT472C1H9L

Table 36 Connectors

Reference	Part Number	Description
TP1	0172	Connector pin, E-309/6
X1	210249	Connector, 2 mm Metric, Ermet104732
X2	220114	Connector, SMA, PE4545

Table 37 Miscellaneous

Reference	Part Number	Description
	211738	Screw, crosshead, M2.5x6, DIN7985 PZ A4
	5068	Screw-lock compound, Loctite 222
	PCB217984	FR-4 1.6 mm 4-layer

4.3.7 Technical Data for MRG114

Table 38 GPS Receiver Module

Explanation	Value
Type	LEA-6T-0
Features:	50
Number of channels	26/26 seconds (warm/cold)
Time to first fix	
Frequency	1575.42 MHz (L1-band)
Tracking level	-162 dBm
Connector	SMA, female
LNA power	+4.5 ... +5.0 V, 100 mA max.
Signal levels	RS232
Output protocol	NMEA 0183

Table 39 General

Explanation	Value
Power requirements:	
+5 V ($\pm 5\%$)	200 mA
Operating conditions:	
Temperature	+5 ... +55 °C
Humidity	Non-condensing
Storage conditions:	
Temperature	-55 ... +80 °C
Humidity	Non-condensing
Dimensions and mass:	
Unit type	E1-size printed circuit board
Length, width, height	190 × 128 × 20.6 mm
Weight	145 g
System connector:	
Connector type	220-pin female
LED light:	
Status indicator	Tricolored LED light

4.3.8 Connector Signal Layout

System connector is a 220-pin, 5-row female connector.

Table 40 System Connector Signal Layout

Pin/Row	a	b	c	d	e
1	GND	GND	GND	GND	GND
2					
3					
4					
5					
6					
7					
8					
9					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23	GND	GND	GND	GND	GND
24					
25					
26					
27					
28					

Pin/Row	a	b	c	d	e
29					
30	TXD1				
31	RXD1				
32					
33					
34					
35					
36					
37			MRES#		
38	TDO	TCK		TDI	TMS
39	1PPS	TEST#			
40					
41					
42					
43					
44	+5 V	+5 V	+5 V	+5 V	+5 V
45					
46			GND		
47	GND	GND	GND	GND	GND

4.3.9 Connector Signal List

Table 41 System Connector Signal List

Signal	Pin	Description	Level
GND	a-e1,a-e23, c46, a-e47	Ground	
TxD1	a30	Data output for serial channel 1	RS232
RxD1	a31	Data input for serial channel 1	RS232
MRES#	c37	Optional external reset input	+3.3 V CMOS
TDO	A38	Data output in PLD programming	+5 V CMOS
TCK	B38	Clock input in PLD programming	+3.3/5 V CMOS
TDI	D38	Data input in PLD programming	+3.3/5 V CMOS
TMS	E38	Mode select in PLD programming	+3.3/5 V CMOS
1PPS	a39	One-pulse-per-second output	+5 V CMOS

Signal	Pin	Description	Level
+5 V	a-e44	+5 V operating voltage	



Signal marked by # is 0-level active.

4.3.10 GPS ANT Connector

- Signal input for GPS local antenna.
- Type of connector: SMA female
- Corresponding cable connector: SMA male



The center wire of the cable feeds a supply voltage +4.8 VDC to the antenna amplifier.

4.3.11 List of Signals MRG114

The following signal names are used throughout the text and drawings of MRG114.

Table 42 List of Signals

Signal	Description
1PPS	One-pulse-per-second
GND	Ground
LED	Light emitting diode
MHZ	Megahertz
MRES	Master reset
RXD1	Received serial line data to GPS Module
TCK	Test clock
TDI	Test data in
TDO	Test data out
TMS	Test mode select
TXD1	Transmitted serial line data from GPS Module

4.3.12 Diagrams and Board Layouts MRG114

Table 43 List of Diagrams

Description	Picture Code
GPS Receiver Unit MRG114 Circuit Diagram	SCH210887
GPS Receiver Unit MRG114 Components Layout	LAY210025

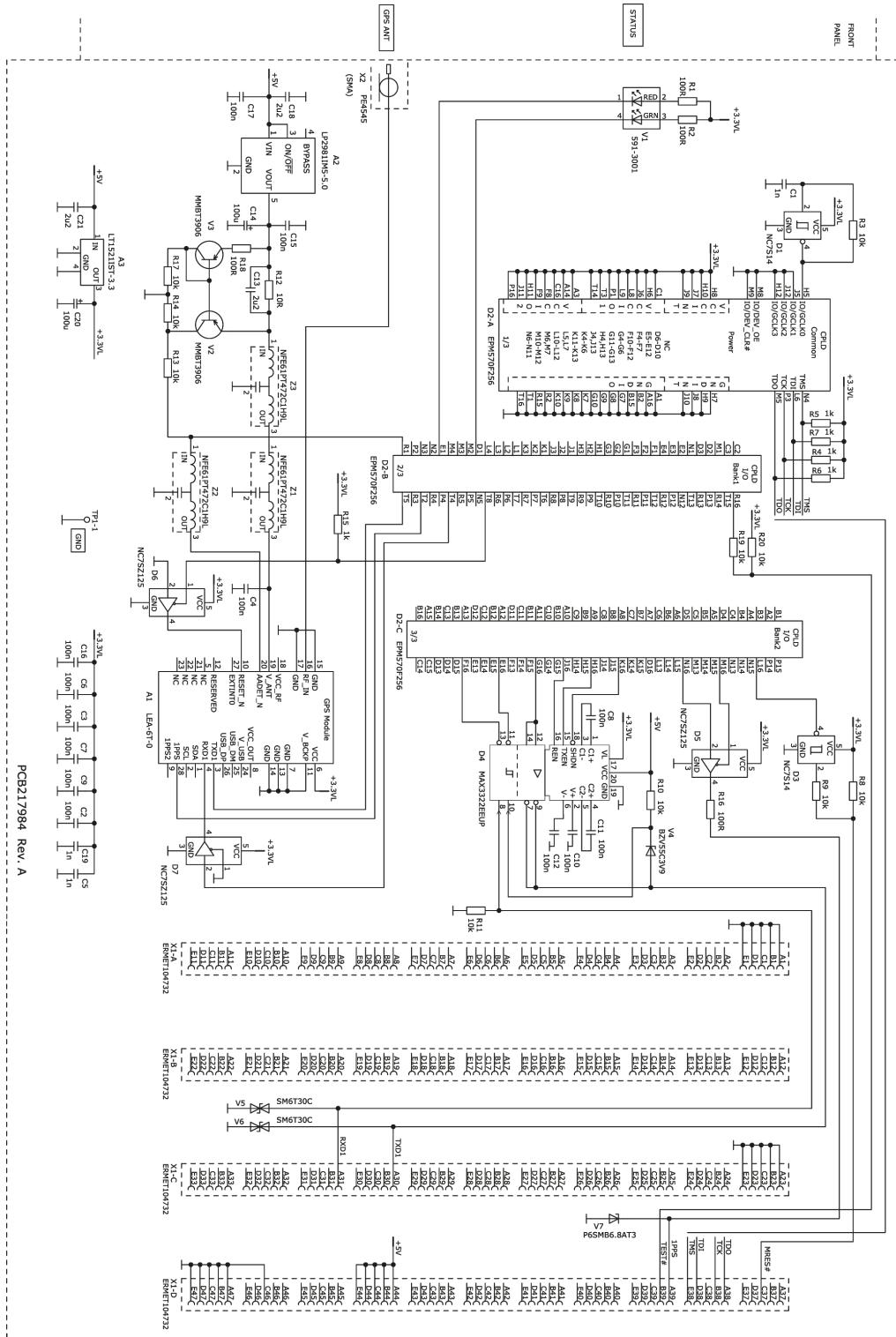


Figure 34 GPS Receiver Unit MRG114 Circuit Diagram

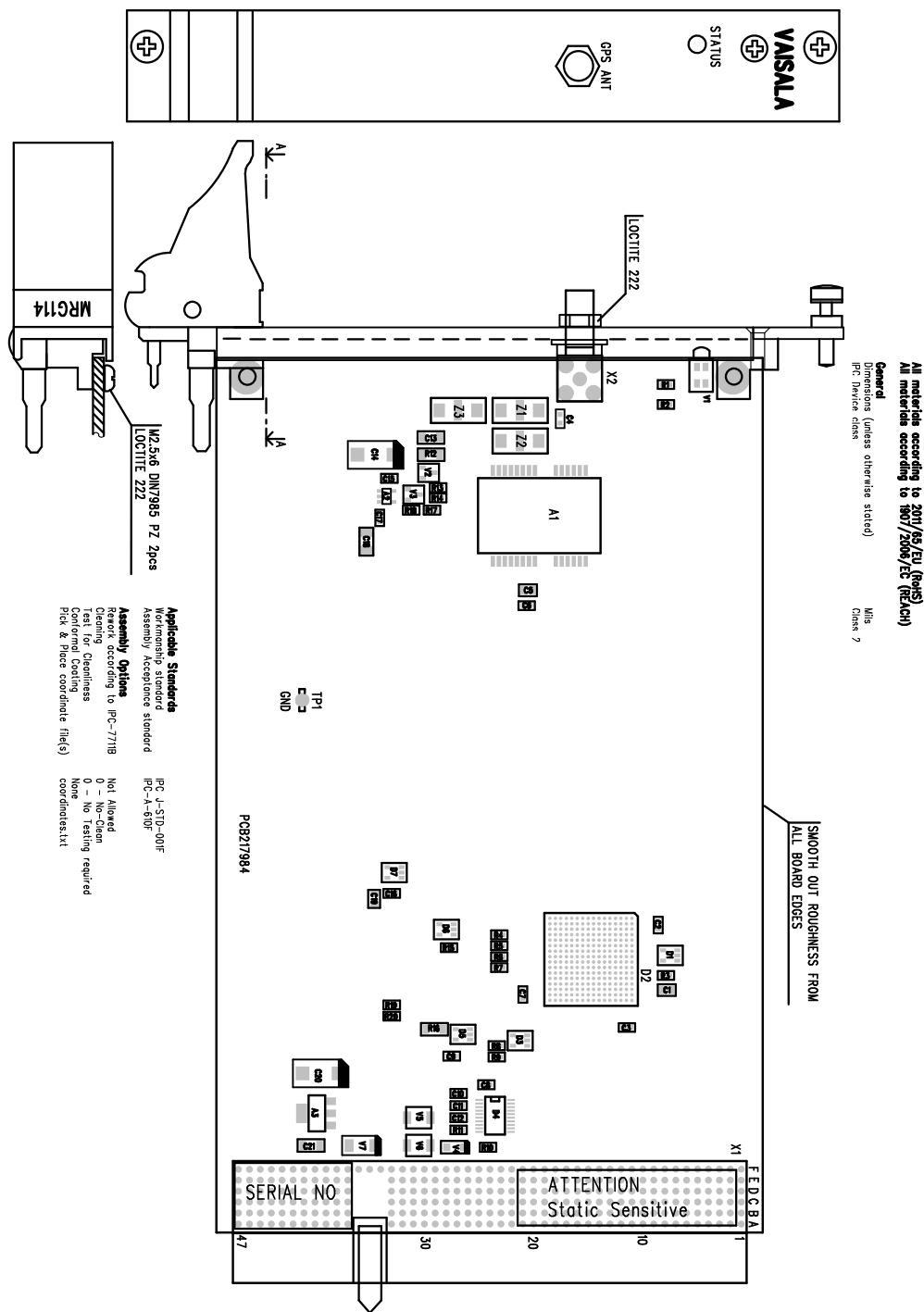


Figure 35 GPS Receiver Unit MRG114 Components Layout

4.4 Power Supply MWP312

Power Supply MWP312 is an E1-sized plug-in system power unit. MWP312 connects to the motherboard through a 32-pin Euro connector and provides DC operating voltages for the system.

The input power is a 24 V DC voltage. The regulated output voltages +3.3 V, +5 V, +7 V, +12 V and -12 V DC are fed to the Euro connector. The input power connection is floating and the output voltages are short-circuit protected.

MWP312 automatically enters standby state when the input power is connected. In this state, only +5 V internal DC voltage is on and a +5 V standby voltage for low power external use is available. All other DC/DC converters are disabled and the +5 V power switch is off.

The system power on/off is controlled by logic signals. Two alternative control methods are provided: direct on/off control with separate on and off control signals; or alternating control with a single on/off (toggle) control line. The control signals are available in the Euro connector and in the front panel power control connector. LED lights for all DC output voltages are provided for monitoring purposes.



Figure 36 Power Supply MWP312

4.4.1 Control Logic

The PLD circuit D1 controls the state of the power unit. During power-up, the reset controller A8 keeps the reset signal input (D1/31) active and the D1 enters power-off (standby) state where only internal +5V voltage and +5VSTBY output voltage are on.

The control inputs PON#, POFF#, PTOGGLE#, and MPUPON# are used to set the supply in power-on or in standby state. The signal PON# switches the power on. The signal POFF# switches the power off. The signal PTOGGLE# is used to change the state of the supply. The MPUPON# signal is optionally used for delayed power off (see section [Controlled Shut Down \(page 103\)](#)).

The output signal at pins 34 and 35 of D1 is used to control the A2, A3 and A4 DC/DC converters. The high-level output signal switches the converters on by feeding current to the optocoupler V21 which turns V21 collector voltage at low level. This further turns off the transistor V22 and enables the DC/DC converters A2 and A3 and turns on the FET V23 which feeds the input voltage to the -12 V DC/DC converter. Converter A3 output +12 V is further used to control the +5V power switch and as power input for +7V DC/DC converter A6.

4.4.2 Standby Regulator

The linear voltage regulator A5 is used as 400 mA current limiter in the +5 VSTBY output.

4.4.3 Output Switch

N-channel FET transistors V7 and V8 are used to connect +5 V output voltage on/off. Two 13.5 milliohm devices in parallel are used to keep the worst case on-state voltage loss below 40 mV.

+12 V output voltage is used to control the +5 V output switch V7 and V8. The +12 V switches the +5 V power on by turning the gate voltage of FET transistors at high level via operational amplifier A7. Gate voltage is not switched high if the +12 V voltage is below +8 V.

4.4.4 Power Indicators

The output voltages are monitored by comparator circuits A9, A10 and A11. When a voltage falls below 80 % of its nominal value, the output of the comparator changes state to indicate low voltage condition. The comparator outputs are connected to the PLD circuit D1 which turns the corresponding indicator LED light to red by switching off the green LED in a bi-color lamp. At the same time, blinking control is activated at control signal RED (power control connector X2 pin 6) for external indication of the power fault condition.

4.4.5 Power-up

At power-up, D1 sets the GRN control output (X2/1) blinking until the low drive of STATUS# input signal (X1/c12) is released by all external system units. A unit typically releases the common STATUS# line when its power-up test routines are completed successfully.

If STATUS# remains active for more than 6 minutes, the D1 turns the RED control on to indicate that at least one system unit has failed in the power-up procedure.

4.4.6 Controlled Shut Down

The signal MPUON# (X1/a4) is used for a controlled shut down if the system includes optional embedded PC computer. In that case when the PTOGGLE# control is activated the active MPUPON# signal delays power off until the computer is completed its shutdown operations and releases the MPUPON# control. The delayed power-off period is indicated by blinking GRN control for external status indicator.

4.4.7 Temperature Monitor

The unit includes a temperature monitor circuit for an over temperature warning and shut down features. The circuit consists of temperature sensing NTC resistor R57, fixed resistor R24, capacitor C29, inverter gate D3-F, and 3-state buffers D4,D5. In operation the PLD D1 alternatively connects NTC resistor and fixed resistor R24 as a feedback resistor for the RC oscillator and calculates the unit temperature by comparing the oscillator frequencies.

When temperature rises over +70 °C, a temperature warning is given by blinking the RED control for the external indicator.

At temperatures over +90 °C, a temperature shut-down to the standby state is performed and the RED control for external indicator is set.

4.4.8 Technical Specifications MWP312

Table 44 MWP312 Technical Specifications

Property	Value / Description
Nominal Input Voltage	24 V
Input Voltage Range	18 36 V
Typical Input Current	2.7 A, Vin 24 V (50 W load) 3.6 A, Vin 18 V (50 W load)
Outputs	+3.3 V (3.1... 3.4 V) / 7 A +5 V (4.75 ... 5.25 V) / 5 A +7 V (6.7 ... 7.2V) / 1 A +12 V (11.0 ... 13.0) / 1 A -12 V (-11.0 ... -13.0) / 0.1 A +5 V stby (4.25 ... 5.25) / 0.4 A
Operating Temperature	-30+55°C
Storage Temperature	-55+70°C
Humidity	Non-condensing
Dimensions (height, depth, width)	100 mm × 160 mm × 20 mm
Weight	0.4 kg

4.4.9 Power Control Connector

- Connector: 9-pin female D
- Mating cable connector: 9-pin male D

Table 45 Power Control Connectors

Pin	Signal	Description
1	GRN	Power on indicator output
2	RACK0	Rack code LSB
3	RACK1	Rack code MSB
4	POFF#	Power off control input
5	GND	Ground
6	RED	Error indicator output
7	PON#	Power on control input
8	YEL	Standby power indicator output
9	PTOGGLE#	Power toggle control input

4.4.10 System Connector MWP312

- Connector: 32-pin, 2-row male power Euro connector
- Mating connector: 32-pin, 2-row female power Euro connector

Table 46 System Connectors

Pin	Row A		Row C	
	Signal	Description	Signal	Description
2	GND	Ground	GND	Ground
4	MPUPON#	Power control input from MPU-unit	POFF#	Power off control input
6	PON#	Power on control input	PTOGGLE#	Power toggle control input
8	RACK0	Rack code LSB	RACK1	Rack code MSB
10	+V	Input Power +	+V	Input Power +
12			STATUS#	Status indicator input
14	-V	Input Power -	-V	Input Power -
16	+5VSTBY	+5 V standby voltage	+5VSTBY	+5 V standby voltage
18	+3.3V	+3.3 V DC power	+3.3V	+3.3 V DC power
20	+3.3V	+3.3 V DC power	+5V	+5 V DC power
22	+5V	+5 V DC power	+5V	+5 V DC power

24	+7V	+7 V DC power	+7V	+7 V DC power
26	+12V	+12 V DC power	+12V	+12 V DC power
28	-12V	-12 V DC power	-12V	-12 V DC power
30	GND	Ground	GND	Ground
32	GND	Ground	GND	Ground

4.4.11 Parts List MWP312

Table 47 MWP312 Parts List

Part No.	Code	Description	Qty
Chassis			
	DRW212800	Front panel assembly for MWP312	1
	DRW212802	Front panel, machined, for MWP312	-
	PCB210230(B)	Printed circuitboard for MWP312	1
	DRW212802	Heat sink for MWP311	1
Integrated Circuits			
A1	210846	Converter, DC/DC, QS075YG-A	1
A2	210845	Converter, DC/DC, QS050YE-A	1
A3	210847	Converter, DC/DC, QS100YH-A	1
A4	210300	Converter, DC/DC, TEP-2412	1
A4	16730	IC, op. amp., TL082ID (SMD)	1
A5	19991	IC, voltage regulator, MIC2920A-5.0BS	1
A6	25073	IC, voltage regulator LM2672-ADJ	1
A8	25330	IC, supervisor, MAX810EUR-T (SMD)	1
A9, A10, A11	19784	IC, comparator, LTC1442IS8(SMD)	3
D1	25771	IC, EPM7064STC44-10 (SMD)	1
D2,D3	15964	IC, inverter, Ex, 74HC14 (SMD)	2
D4, D5	26570	IC, buffer, NC7SZ125M5 (SMD)	2
Transistors and Diodes			
V1, V2, V3, V4,V5, V6	010192	Diode, LED, 591-3001	6
V7, V8, V23	25302	Transistor, FET, PHN1013 (SMD)	3
V9, V11, V14, V19, V26, V27, V28, V31	17332	Diode, Transil, P6SMB6.8AT3 (SMD)	8
V10	17448	Diode, Transil, SMCJ43A, (SMD)	1

Part No.	Code	Description	Qty
V12, V15, V29, V30	15976	Diode, silicon, Ex, LL4148/PMLL4148 (SMD)	4
V13, V16, V24	17311	Diode, Transil, SM6T30CA (SMD)	3
V17	19241	Diode, Transil, SM6T15A (SMD)	1
V18	19463	Diode, Schottky, MBR130LT3 (SMD)	1
V20, V25	25030	Diode, Transil, 1SMB18AT3 (SMD)	2
V21	16982	Optocoupler, Ex, TLP 181 (SMD)	1
V22	15495	Transistor, NPN, SST3904 SOT-23	1
Resistors			
R1, R8, R13, R22, R39, R41, R42	18117	Resistor, chip, 1k0 1% 100 ppm 0805	7
R2, R9	18730	Resistor, chip, 562R 1.0% 100 ppm 0805	
R3, R5, R34	19459	Resistor, chip, 100R 0.5% 25 ppm 0603	3
R4, R18, R20, R23, R25, R29 R32, R36, R40	25262	Resistor, chip, 10k0 1% 100 ppm 0603	9
R6	18683	Resistor, chip, 464R 1.0% 100 ppm 0805	1
R7	18683	Resistor, chip, 274R 1% 100 ppm 0805	1
R10, R11, R38	19710	Resistor, chip, 22k0 5% 200 ppm 0603	3
R12	18734	Resistor, chip, 1k47 1% 50 ppm 0805	1
R14, R17, R19,R27, R33	18410	Resistor, chip, 3k32 1% 50 ppm 0805	5
R15, R16	18119	Resistor, chip, 1k82 1% 100 ppm 0805	2
R21	26126	Resistor, chip, 4k75 0.5% 25 ppm 0603	1
R24, R44, R45, R46, R47, R51	25451	Resistor, chip, 100k 1.0% 100 ppm 0603	6
R26, R35	25169	Resistor, chip, 15k0 1% 100 ppm 0603	2
R30, R37	18120	Resistor, chip, Ex, 2k0 1% 50 ppm 0805	2
R30, R56	16416	Resistor, chip, 270R 1% 50 ppm 1206	1
R31, R55	25210	Resistor, chip, 332R 1.0% 100 ppm 0603	2
R37	16415	Resistor, chip, 150R 1% 50 ppm 1206	1
R43, R52	18797	Resistor, chip, 221k 1% 50 ppm 0805	2
R48	18888	Resistor, chip, 121k 1% 50 ppm 0805	1
R49	18604	Resistor, chip, 332R 1% 50 ppm 0805	1
R53	26125	Resistor, chip, 61k9 1% 100 ppm 0603	1
R54	18734	Resistor, chip, 1k47 1% 50 ppm 0805	1

Part No.	Code	Description	Qty
R57	18857	Resistor, chip, NTC,10k 5% B3630K 1206	1
Capacitors			
C1, C2	19482	Cap., electrolytic SMD, 220 µF 35 V 20%	2
C3,C4,C5, C6, C10, C12, C13, C18, C20, C22, C24, C25, C26	15621	Cap., chip ceramic, Ex, 100n 10% X7R 50V 0805	13
C7, C8, C11	16390	Cap., chip ceramic 2n2	3
C9, C19, C21,C28,	25560	Cap., electrolytic SMD 100µF	5
C14	15160	Cap., chip ceramic 10nF X7R 50V 0805	1
C16, C17, C23	25066	Cap., chip ceramic, Ex, 1000nF X5R 1206	3
C25, C29	18287S	Cap, chip polyester, 47nF 5% 25V 1812	1
C27	15750	Cap., chip ceramic 330nF X7R 2220	1
C30			
Filters and Chokes			
Z1	16826	Filter, DC, BNX002-01	1
Z2	25036	Filter, EMI, NFM61R30T472 (SMD)	1
L1	26708	Choke, power, 2.2uH 7.4A 0.011 Ohm	1
L2	16302	Choke, PICO42305	1
L3, L4, L5	19604	Choke, power, 10uH 1.1A 0.14R (SMD)	3
Connectors			
X1	1812	Connector, Euro, D032MS-C1A-0.8/5253	1
X2	19285	Connector, D, DEJK9S4-1A7N-146	1
X3	19640	Connector, horizontal (SMD) 2x8 0.1"	1
	6014	Connector accessory, D20418-2	2
Miscellaneous			
F1	7048	Fuse, glass tube, 5.0AT	1
	7028	Fuse holder, 1611PR 1/12 OSA	1
	211740	Hexag. tapped spacer 5,03. 13.53 M3-13.5	2
	0840	Rivet, 2,5 x 9,9 /Ms/Tin	2
	18574	Screw, crosshead, M 3 x 6 /A4m	2
	211738	Screw, crosshead, M2.5 x 6 /A4	6
	25015	Screw, crosshead, M 3 x 8 /A4m	14
	3939	Washer, spring, B3 /A4	2
	7067	Washer, spring, B2.5 /A4	2

4.4.12 Diagrams and Board Layouts MWP312

Table 48 MWP312 DC Power Supply Illustrations

Code	Description
DRW214593	Circuit Diagram
DRW214594	Components Layout, 2 pages

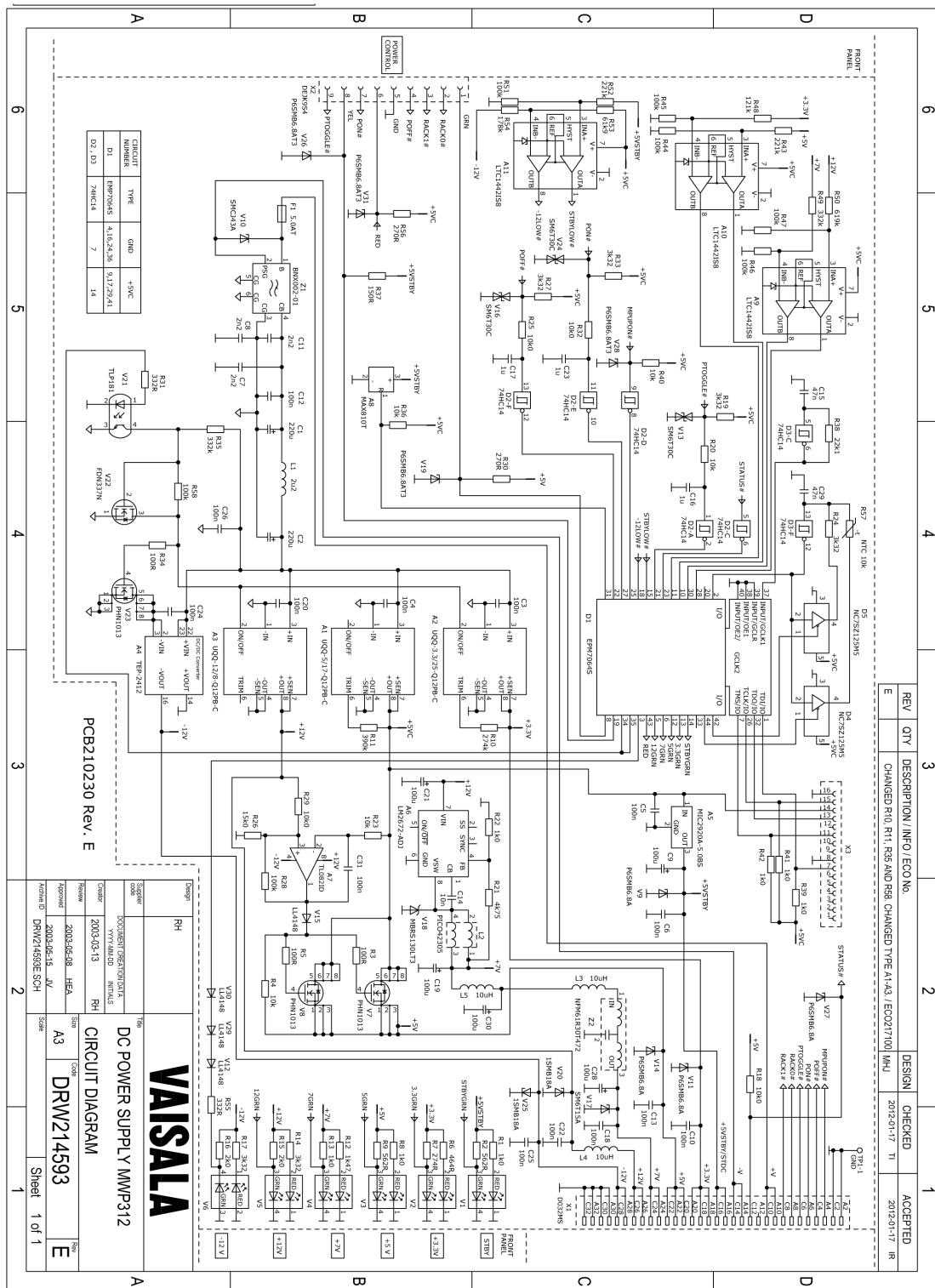


Figure 37 MWP312 Circuit Diagram

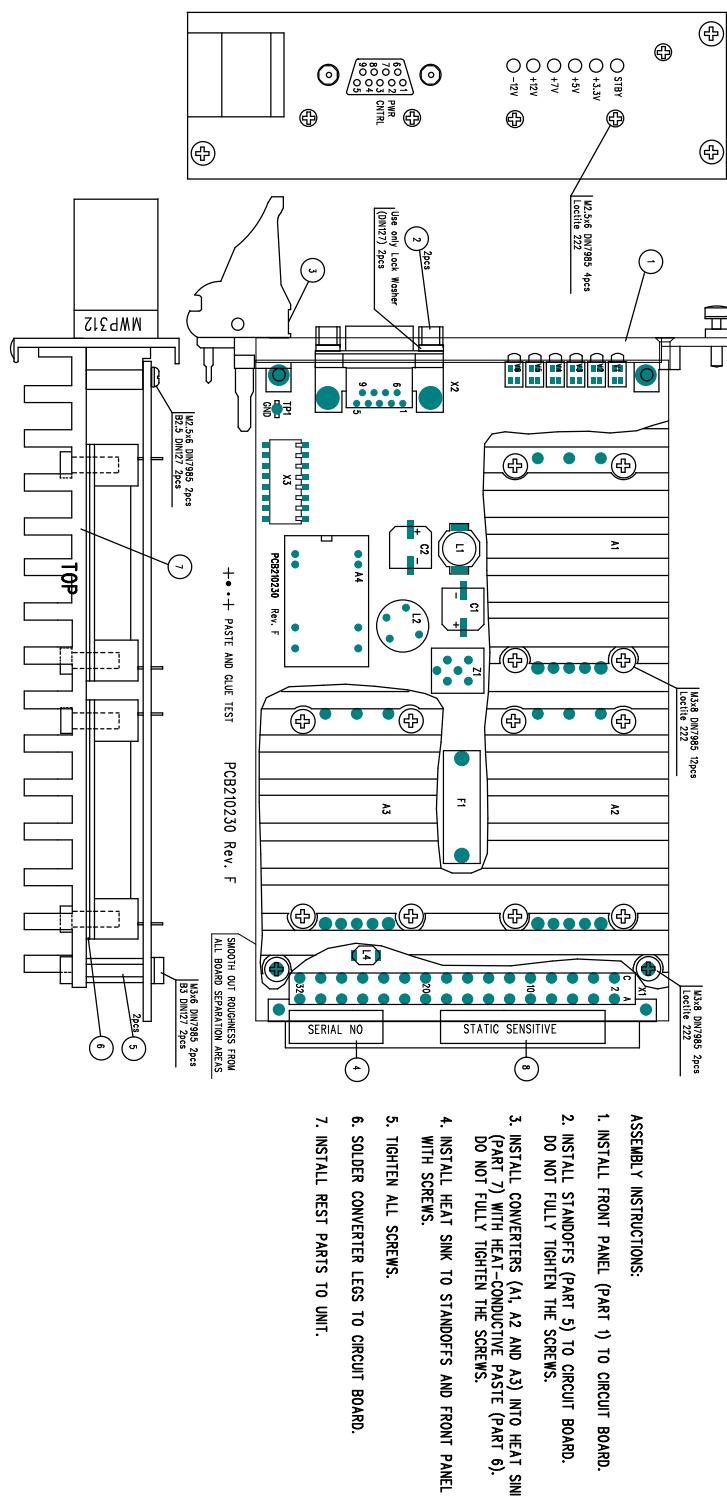


Figure 38 MWP312 Components Layout 1/2

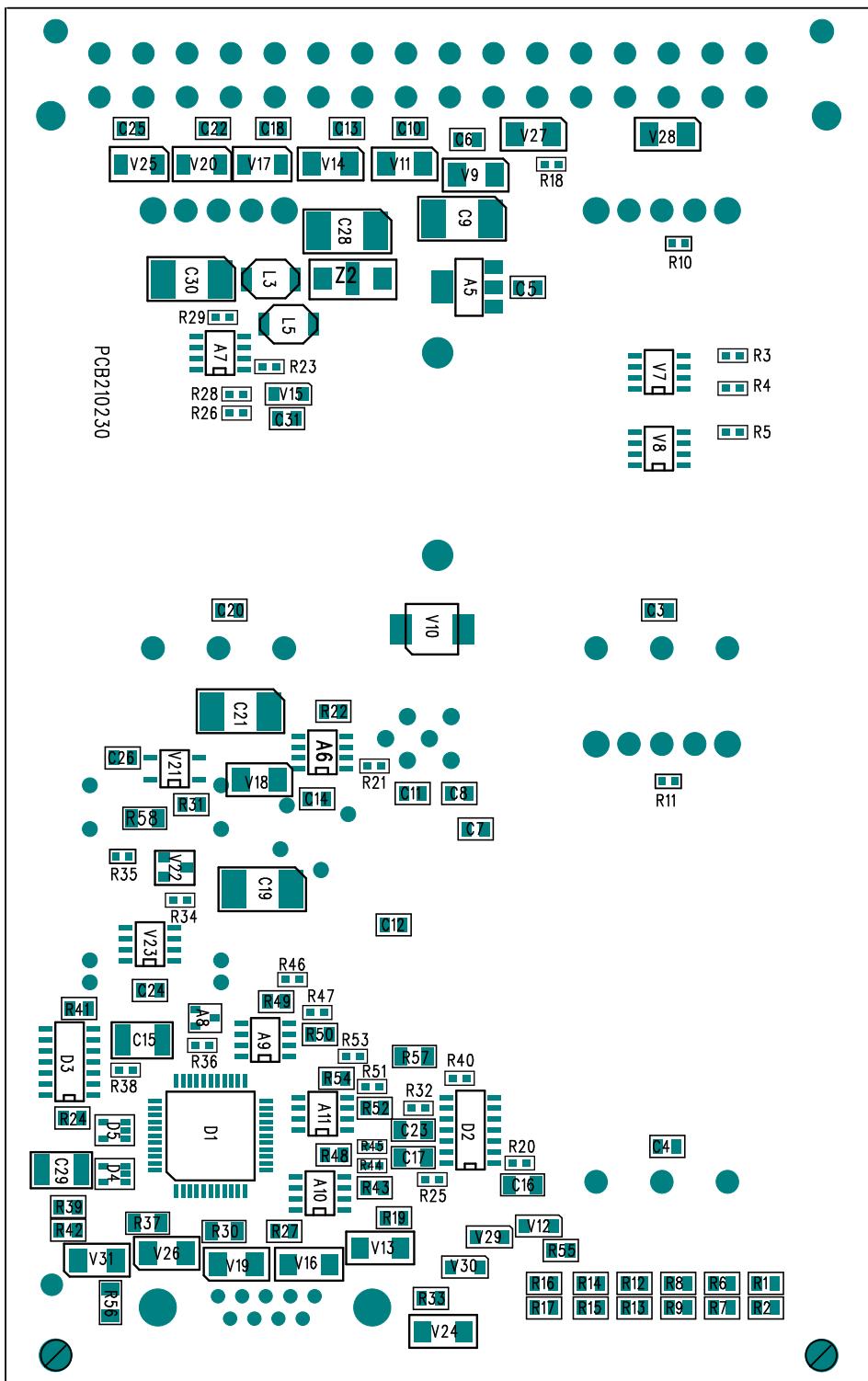


Figure 39 MWP312 Components Layout 2/2

4.5 AC Power Supply MWP411

The MWP411 AC Power Supply, an E1 size plug-in unit, is suitable to provide the feeding voltage for the MWP312 DC Power Supply Unit. MWP411 connects to the motherboard through a 32-pin Euro connector.



Figure 40 AC Power Supply MWP411

4.5.1 Operation

Input power is 100 ... 240 V AC line and output is 24V DC voltage. The total output power is 100 W (at +25 °C ambient temperature).

AC power is connected from a power cord via a filter plug X4 to a commercial, open frame switching AC/DC module. The output voltage is fed to the Euro connector.

The AC/DC module has no power switch - it operates continuously, if an appropriate mains input voltage is applied to the unit.

The module is protected against over loading. A tranzorb diode V1 protects the output against over and reverse voltages.

4.5.2 Technical Specifications MWP411

Table 49 MWP411 Technical Specifications

Property	Value/Description
Nominal Input Voltage	100 ... 240 V AC

Property	Value/Description
Input Voltage Range	80 ... 264 V AC
Frequency	47 ... 63 Hz
Input Current	1.9 A
Output	24 V DC, 4.2 A
Operating Temperature	0 +55°C
Storage Temperature	-40 +70°C
Humidity	Non-condensing
Dimensions	100(H), 160(D), 40(W) mm
Weight	0.4 kg

4.5.3 System Connector MWP411

- Connector: 32-pin, 2-row male power Euro connector
- Mating connector: 32-pin, 2-row female power Euro connector

Table 50 System Connectors

Pin	Row A		Row C	
	Signal	Description	Signal	Description
2	GND	Ground	GND	Ground
4				
6				
8				
10	+24V	Output Power +	+24V	Output Power +
12	0V	Output Power -	0V	Output Power -
14				
16				
18				
20				
22				
24				
26				
28				
30				
32	GND	Ground	GND	Ground

4.5.4 Parts List MWP411

Table 51 MWP411 Parts List

Part Number	Description	Qty
PCB210196	Printed Circuit Board	1
0946	Washer, serrated lock A4,3 DIN6798A A4	1
3939	Washer, spring lock B3 DIN127 A4	2
4337	Washer, spring lock B4 DIN127 A4	1
7067	Washer, spring lock B2,5 DIN127 A4	5
3050	Washer, flat A3, 2 DIN125 A4	5
211738	Screw, crosshead M2,5 x 6 DIN7985 PZ A4	2
211742	Screw, crosshead M2,5 x 12 DIN7985 PZ A4	4
211853	Screw, crosshead M4 x 12 DIN966 PZ A4	1
211854	Screw, crosshead M3 x 20 DIN966 PZ A4	2
223243	Screw, crosshead M2, 5 x 20 DIN7985 PZ A4	1
4776	Nut, hex M3 DIN934 A4	2
4812	Nut, hex M4 DIN934 A4	2
6779	Nut, hex M2, 5 DIN934 A4	5
5068	Screw-lock compound Loctite 222, 50ml	
240635	Filter, mains power IEC 3A 250 V AC, with wire leads	1
1780	Diode, transil 1N 6284 A / 1.5KE36A	1
1812	Connector, Euro D032MS-C1A-0,8/5	1
244970	Connector, pin 1 x 4, 3.96 mm, straight, SPOX, TH	1
244990	Connector, crimp housing 1 x 3 3.96 mm female SPOX	1
0172	Connector pin Ex E03096L02	1
DRW214089	Front Panel Assembly for MWP411	1
0840	Rivet 2.5 x 9.9 /Ms /Tin	2
16166	Plastic label	

Part Number	Description	Qty
MW45085	Flange for MWP411 mains filter	1
0760	Round sleeve spacer ENLIS 4 / 5.83.056	5
240634	Power supply 24 V DC / 4.2A 101.6x50.8 x 31.8 mm	1
4622	Cable mount D 5 mm, 9.5 mm black	2
0414	Ring terminal insulated 0.5-1.5 mm 2, M4, red	1
244992	Connector, crimp terminal 18-24 AWG, female, tin, SPOX	2
CBL210491	DC cable, internal MWP411 2 x housing and crimp terminals	1
DRW229559	Warning sticker, electric shock 55 x 25 mm	1
15223	Sticker set matt white, polyethylene	1
10948	Marking sticker OK46546	1

4.5.5 Diagrams and Board Layouts MWP411

Table 52 MWP411 AC Power Supply Illustrations

Code	Description
DRW214015	Circuit Diagram
DRW214016	Components Layout

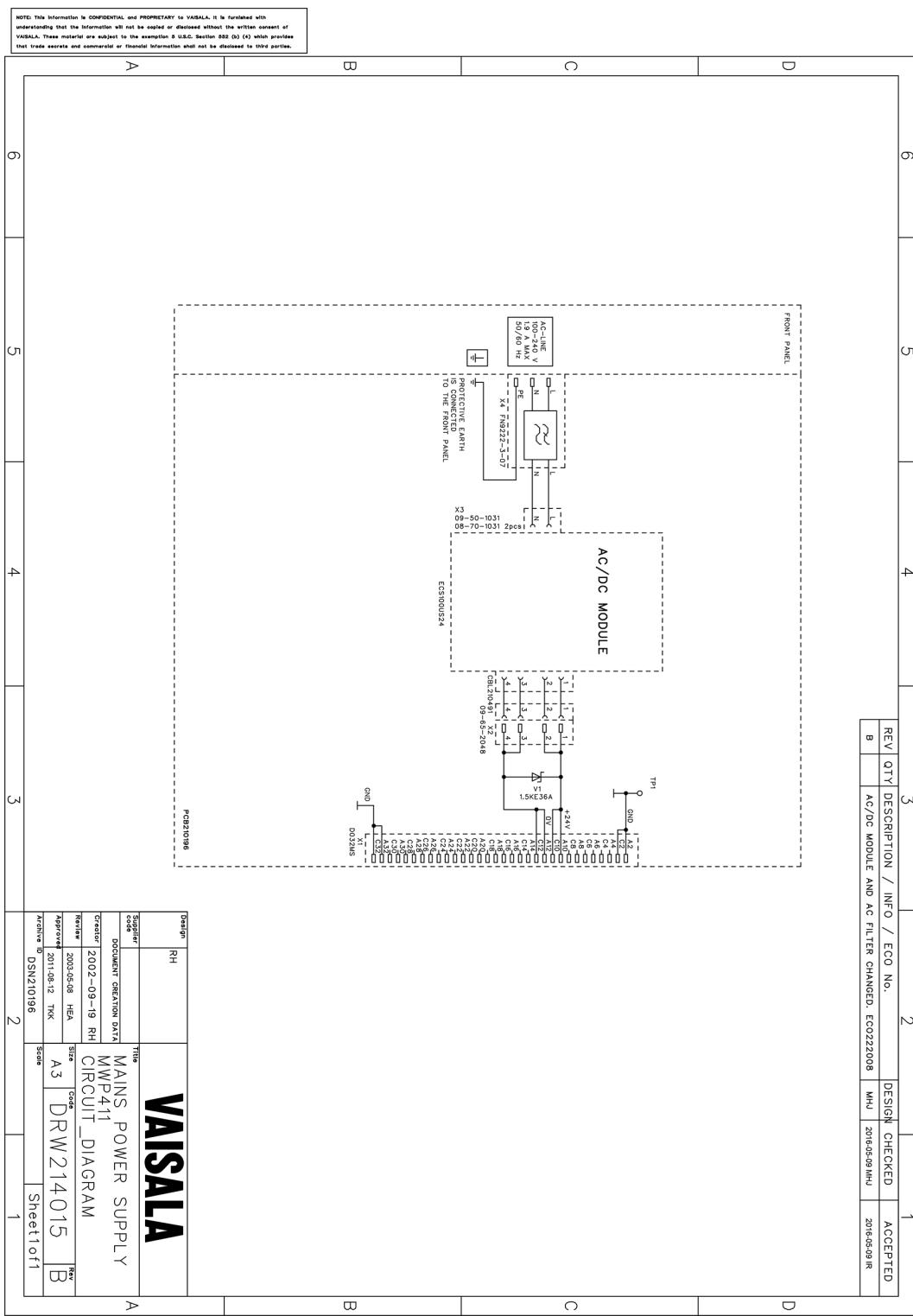


Figure 41 MWP411 Circuit Diagram

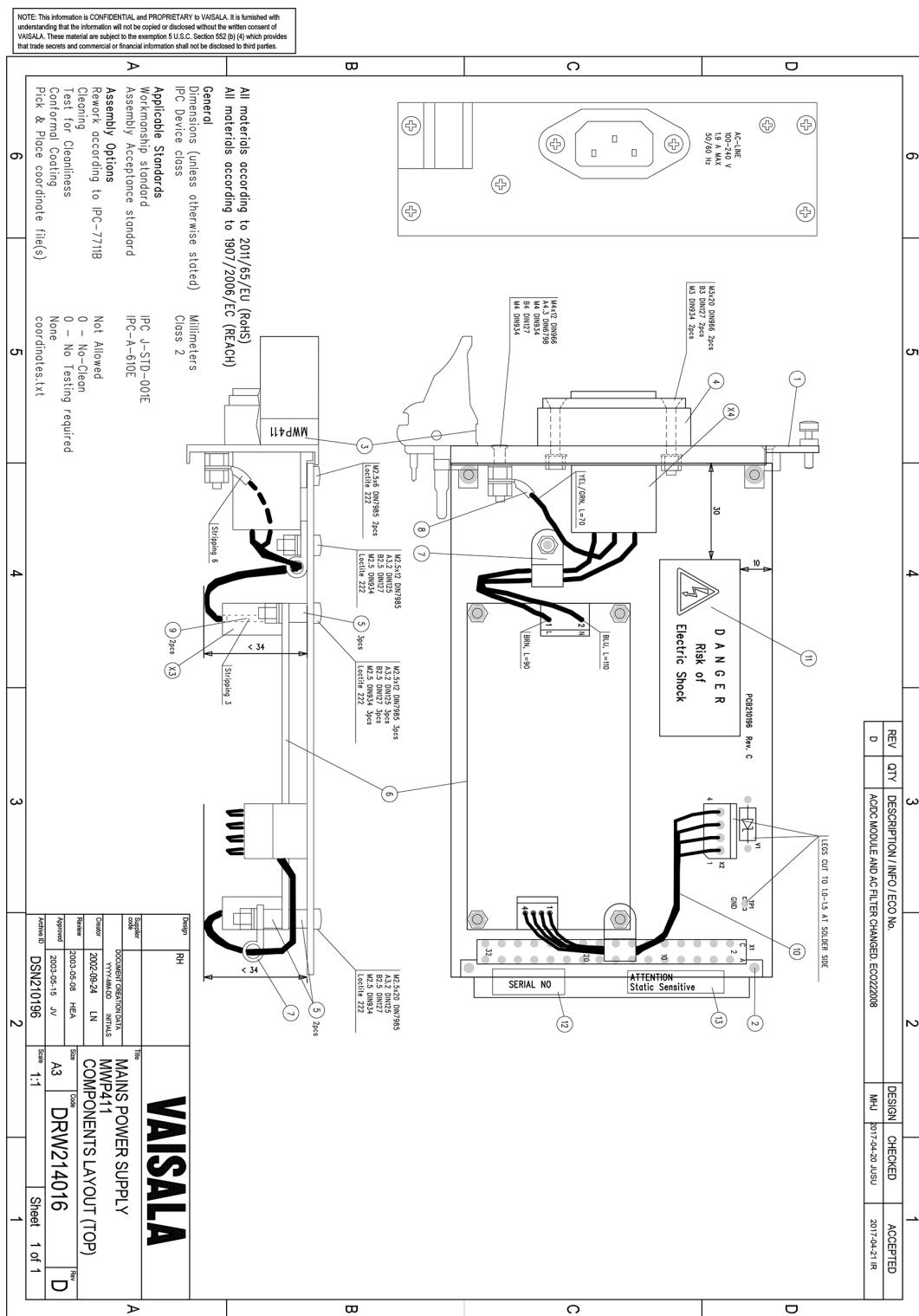


Figure 42 MWP411 Components Layout

5. Technical Data

5.1 Sounding Processing Subsystem Specifications

Table 53 Technical Specifications

Property	Description / Value
Dimensions	235 × 335 × 184 mm
Power consumption	70 W max.
Mains voltage nominal	100 ... 240 V AC
Mains frequency	50 / 60 Hz
DC power connection	19 ... 36 V DC, 60 W max.
Weight	7.5 kg max.
Cooling system	Forced air convection, three fans
UHF Connector	Coaxial N-type female
GPS Connector	Coaxial TNC-type female
VLF Connector	Coaxial C-type female
Antenna power	Antenna amplifiers are powered through antenna cables
Modulation	GFSK, GMSK, FM, FSK
Frequency range	400.15 ... 406 MHz
Sensitivity with RS41 and RS92 radiosondes	-120 dBm ¹⁾
Noise figure	<2.5 dB ¹⁾
Image rejection	70 dB ¹⁾
Spurious Free Dynamic Range with RS41 and RS92 radiosondes	90 dB ¹⁾
Third Order Intercept Point (IIP3)	0 dBm ¹⁾
Input impedance	50 Ohms
Environmental conditions	Indoor use
	Altitude up to 2000 meters
Operating temperature range	0 ... + 45° C
Operating humidity	10 ... 90 % RH (non-condensing)
Storage temperature	-55 ... + 70° C

Property	Description / Value
Storage humidity	5 ... 95 % RH

1) Specifications valid with Vaisala telemetry antennas

5.2 SPS311G Spare Parts

Table 54 Spare Parts and Accessories

Code	Item
SPS311GSPSET	Spare part set SPS311G for DigiCORA System. Including: <ul style="list-style-type: none"> • MRR111 • MRP111 • MRG114 • MWP312 • MWP411
Plug-in units:	
MRR111SP	400 MHz Receiver Unit
MRP111SP	Receiver Processor Unit
MRG114SP	GPS Receiver Unit
MWP312SP	Power Supply Unit
MWP411SP	AC Power Supply Unit
Fuses:	
7048SP 5 AT, 10 pcs	
210704SP 2.0 AT, 10 pcs	
Other:	
DRW231652SP	Frame
212830SP	Fan

6. EU Declaration of Conformity

VAISALA

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EU DECLARATION OF CONFORMITY

Manufacturer: Vaisala Oyj
Post address: PL 26, FIN-00421 Helsinki
Street address: Vanha Nurmijärventie 21, Vantaa, Finland

This declaration of conformity is issued under the sole responsibility of the manufacturer.

Object of the declaration:

Vaisala Sounding Processor Subsystems;
SPS311, SPS311G, SPS311AG and SPS341AG

The object of the declaration described above is in conformity with Directives:

Low Voltage Directive (2014/35/EU)
Radio Equipment Directive (2014/53/EU)
RoHS-Directive (2011/65/EU)

The conformity is declared with using the following standards:

EN 61010-1:2010 Safety requirements for electrical equipment for measurement, control, and laboratory use – Part 1: General requirements

EN 61326-1:2013 EMC requirements - Immunity test requirements for equipment intended to be used in an industrial electromagnetic environment.

EN 61000-3-2:2014 Limits for harmonic current emissions

EN 61000-3-3:2013 Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems.

EN 50581:2012 Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Signed for and on behalf of:
Vantaa 2018-09-25

Jukka Lyömiö

.....

Jukka Lyömiö
Standards and Approvals Manager

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Technical Support



Contact Vaisala technical support at helpdesk@vaisala.com. Provide at least the following supporting information:

- Product name, model, and serial number
- Name and location of the installation site
- Name and contact information of a technical person who can provide further information on the problem

For more information, see www.vaisala.com/support.

Warranty

For standard warranty terms and conditions, see www.vaisala.com/warranty.

Please observe that any such warranty may not be valid in case of damage due to normal wear and tear, exceptional operating conditions, negligent handling or installation, or unauthorized modifications. Please see the applicable supply contract or Conditions of Sale for details of the warranty for each product.

Recycling



Recycle all applicable material.



Follow the statutory regulations for disposing of the product and packaging.

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www.vaisala.com

