

VERILOG CODE : DEPARTMENT OF CSE

EXPERIMENT : 1

AND GATE : <https://www.edaplayground.com/x/euBZ>

OR GATE : <https://www.edaplayground.com/x/JvNH>

NAND : <https://www.edaplayground.com/x/QrwX>

NOR : <https://www.edaplayground.com/x/pXdj>

NOT : <https://www.edaplayground.com/x/EDWh>

XOR : <https://www.edaplayground.com/x/EDWt>

XNOR : <https://www.edaplayground.com/x/76KE>

EXPERIMENT : 2

TRI STATE BUFFER :

<https://www.edaplayground.com/x/uSie>

UNDIRECTIONAL BUS :

<https://www.edaplayground.com/x/rD4L>

EXPERIMENT : 3

IMPLEMENTATION OF BOOLEAN FUNCTION :

<https://www.edaplayground.com/x/7gB4>

TWO COMPLEMENT :

<https://www.edaplayground.com/x/8kiq>

FUNCTION MINIMIZATION :

<https://www.edaplayground.com/x/GKdE>

EXPERIMENT : 4

IMPLEMENT 4*1 MULTIPLEXER :

<https://www.edaplayground.com/x/f2Sm>

IMPLEMENT 8*1 MULTIPLEXER :

<https://www.edaplayground.com/x/Tg6f>

IMPLEMENT 3 TO 8 DECODER (Xilin ISE) :

<https://www.edaplayground.com/x/XWcp>

EXPERIMENT : 5

IMPLEMENT PRIORITY ENCODER :

<https://www.edaplayground.com/x/jwXg>

IMPLEMENT MAGNITUDE COMPARATOR :

<https://www.edaplayground.com/x/f8be>

FUNCTION IMPLEMENTATION :

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