DESIGN AND IMPLEMENTATION OF A VENDING MACHINE & ITS PERFORMANCE EVALUATION USING EDA TOOLS

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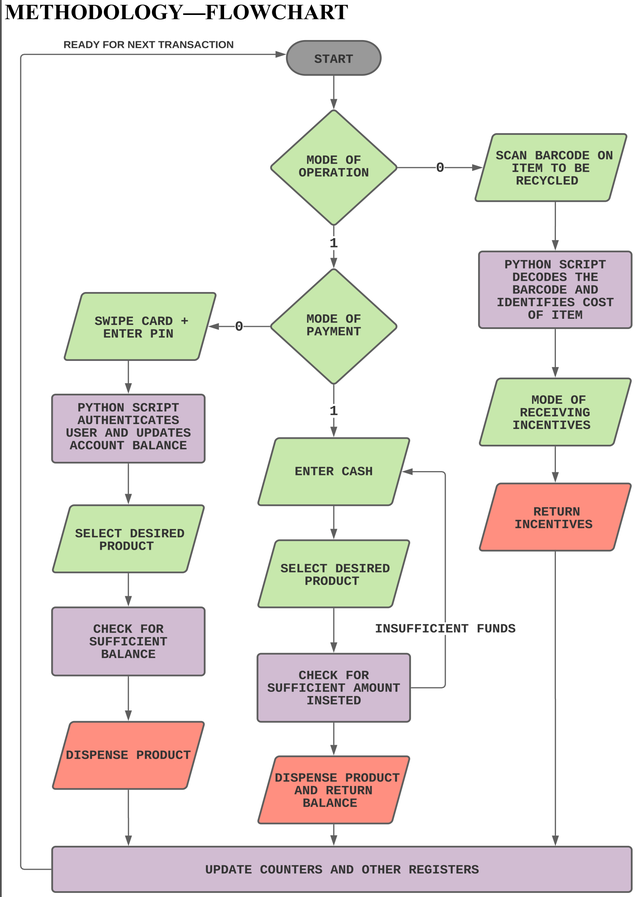
ABSTRACT

To design a vending machine with an additional feature (reverse vending machine) which enables a consumer to recycle the container/wrapper of the item purchased by them for which appropriate incentives are returned. It offers the person to carry out their transaction via cash/card /online payment modes. Unique QR codes/ Barcodes are associated with each product to have information about the product and its cost. The reverse vending machine consists of a scanner that scans the code of the product which is inserted into the machine and completes the transaction accordingly. The vending machine is programmed using Verilog HDL and is simulated on ModelSIM – Intel FPGA Edition Software. Chip planning, timing, power, and various other design and performance analysis are carried out using Intel Quartus Prime Software Suite.

SCAN ME

METHODOLOGY—FLOWCHART



MATHEMATICAL EXPRESSIONS INVOLVED

-> Slack of a particular gate is defined as the difference between required arrival time & arrival time.

- When the data arrives before the time at which it is required, it results in a positive setup slack. This means that the design is functioning within the specified frequency and it has some more timing margin as well.
- When the data does not arrive before the time at which it is required, it results in a negative setup slack. This means that the design doesn't comply to the constrained frequency and timing, which results into a setup violation.

Slack(n) = Data Required Time – Data Arrival Time = RAT(n) – AT(n)

$$\mathrm{RAT(n)} = \begin{cases} cycle\ time & if\ n == Sink \\ \min\big(RAT(n) - \Delta(n,s)\big) & otherwise \end{cases}$$

$$\mathrm{AT(n)} = \begin{cases} 0 & if\ n = Source \\ \max\big(AT(p) + \Delta(p,n)\big) & otherwise \end{cases}$$

s = *successor node*

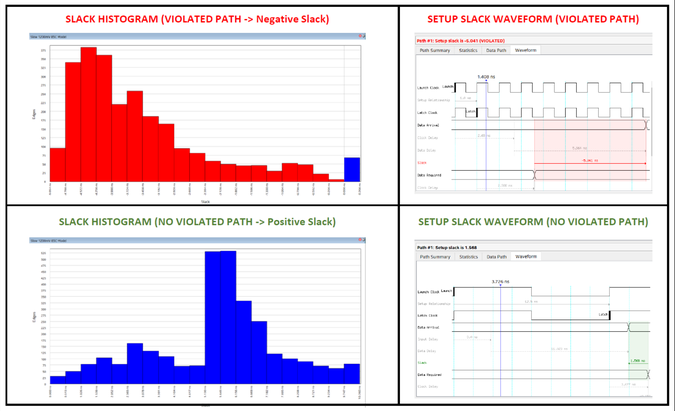
p = *predecessor node*

-> HPWL = **[max {x-coordinate of all gates} - min {x-coordinate of all gates}] + [max {y-coordinate of all gates} - min {y-coordinate of all gates}]***

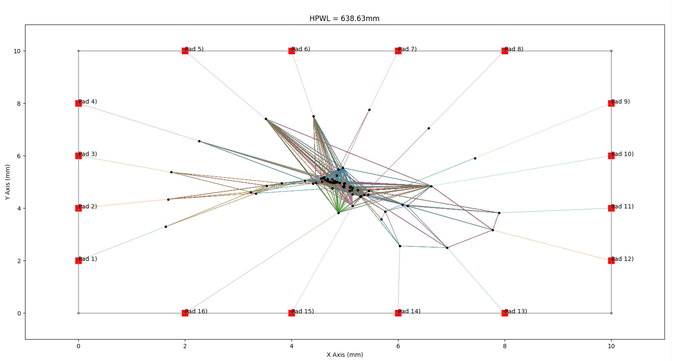
*for multipoint nets

RESULTS

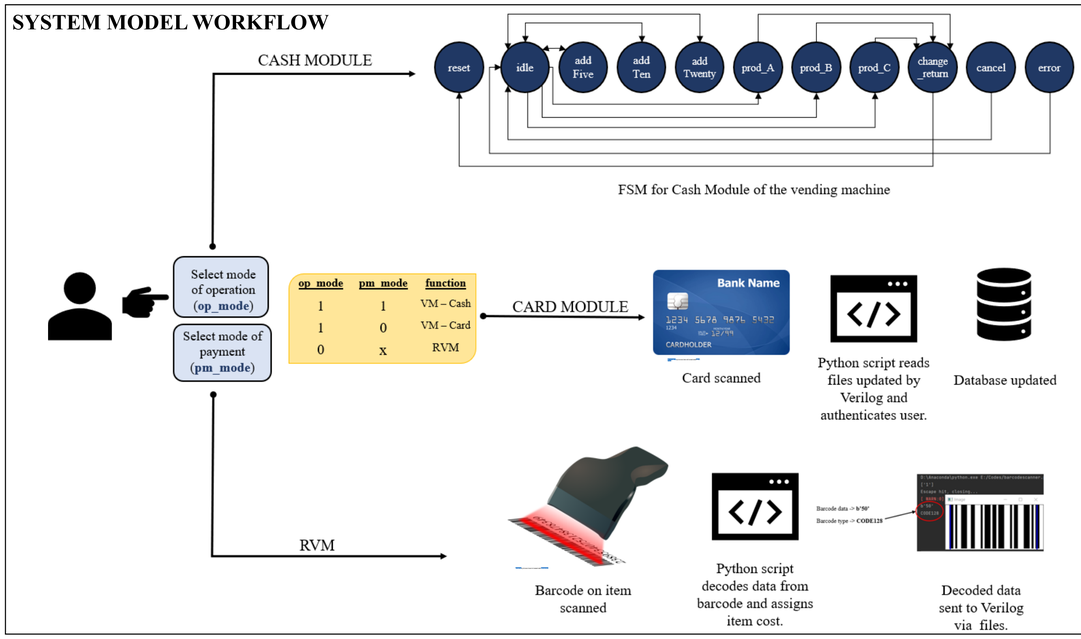
HISTOGRAM & WAVEFORM COMPARISION



HPWL OUTPUT PLOT GENERATED



SYSTEM MODEL WORKFLOW



SLACK COMPARISION

Initial setup slack summary

Clock	Slack	End Point TNS
clk	-5.470	-281.022

Final setup slack summary

Clock	Slack	End Point TNS
clk1	1.568	0.000

DESIGN REQUIREMENTS & CONSTRAINTS

- For development of RTL schematic, the Verilog code must be synthesizable.
- Target FPGA board/required ASIC deign constraints must be known prior optimization. For the synthesis of this model, we have used MAX10 FPGA Dev Kit.
- To implement Half Perimeter Wirelength analytical placement technique for minimization of quadratic wirelength between gates, the RTL schematic must be studied and all the gates, nets and pads must be compiled into a netlist file for input.
- For item identification. Barcode must be present on object.

CONCLUSION/FUTURE SCOPE

- The system so designed is dynamic and can be personalized for the retailer meaning, they can customize the type, number, and cost of the product as required. The overall performance metrics were tested using the EDA tools and optimized to achieve the required performance characteristics.
  - *We were able to improve the overall slack of the system by 7.038ns to achieve a positive slack and minimized the wire length using Half Perimeter Wire Length placement technique to improve timing further.*
- The system can further be developed into ASICs (Application Specific Integrated Circuits) with the design specifications obtained.
- A UPI payment mode can be integrated for a complete contactless experience. The UPI option is available on most card readers nowadays and is a feasible option.

REFERENCES

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