* Fall time is found to match with actual data
* But rise time (t_r) is found to be

$$t_r = \frac{60\,C_{out}}{W_2/L_2}\ ns$$

- This is because of body effect
- As the output rises, the threshold voltage of T_2 also rises, reducing current to delay the rise time

Example:

$T_1 \Rightarrow$ aspect ratio 3/1

$T_2 \Rightarrow$ " 1/2

input capacitance = 0.05 pF

output " = 0.10 pF

$$t_r = \frac{60 \times 0.10}{1/2}\ ns = 12\ ns$$

$$t_f = \frac{35\,C_{out}}{3/1} = 35 \times 0.10 \times \frac{1}{3} = 1.2\ ns$$

$t_r = 12\ ns$

$t_f = 1.2\ ns$

Maximum freq (in hertz) at which the gate can operate

$$= \frac{1}{t_r + t_f}$$

2.11 Ratioed and Ratioless Design

* previously, we have seen depends on aspect ratio W_1/L_1 and W_2/L_2
* So it is necessary to choose suitable gate geometry to obtain desired output.

↳ **Ratioed circuits**

The W/L ratio determines

(i) Circuit speed since edge times are inversely proportional to W/L

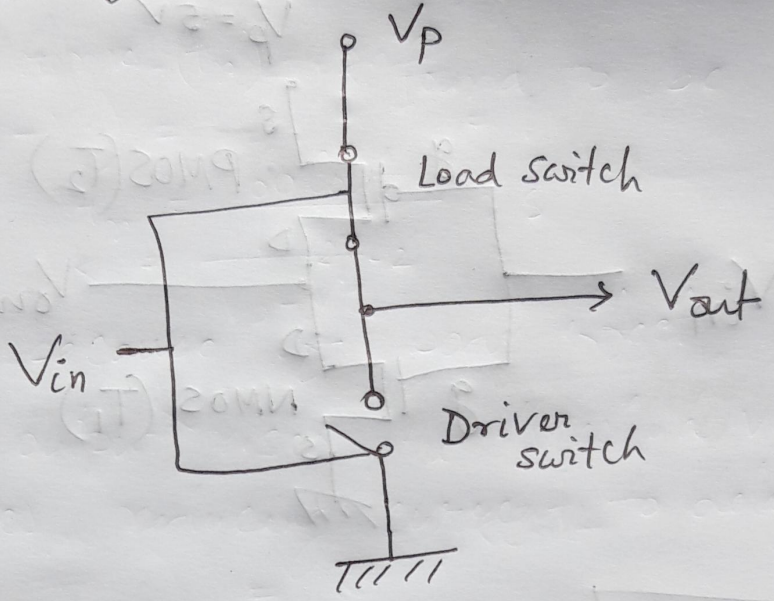
$$t_r \propto \frac{1}{W_2/L_2}$$

$$t_f \propto \frac{1}{W_1/L_1}$$

Ratioed CKt

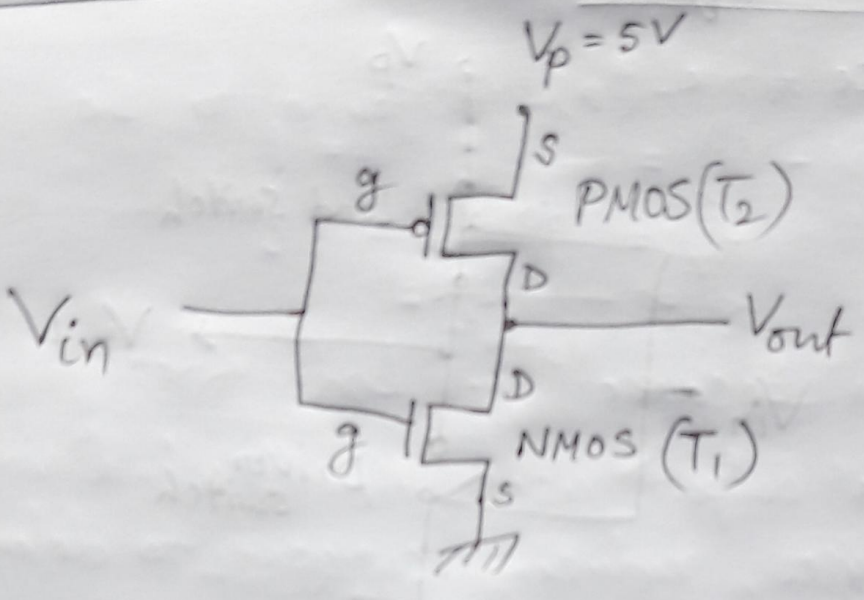
(ii) Power dissipation is also determined by gate geometry Since current flow through a device is dependent on its aspect ratio.

Ratioless Design



* Both switch will NOT be closed at the same time
* One switch is closed, another remains OPEN.
* No current flows betⁿ V_p and 0.
  So no static power dissipation.
* However, both switches may get closed at transition states, causing transient current flow.
* Output voltage does not depends on aspect ratio. So **ratioless inverter**

2.12 CMOS Inverter



(i) When $V_{in} = 0$.

* NMOS (T_1) off

* PMOS $\Rightarrow$ $V_{sg} = V_s - V_g = 5 - 0 = 5 > V_{tp}$

So PMOS on.

* The current flow through T_1 is very less (only some leakage current).

* So voltage drop across T_2 is 0.

Hence $V_{out} = 5V$

T_2 For $V_{in} = 0V$,

$V_{sg} = 5 - 0 = 5$, $V_{tp} = 1$

$V_{sg} - V_{tp} = 4$

$V_{sd} = V_p - V_{out} = 5 - V_{out}$

So When $V_{out} = 0$ to 1 V

$V_{sd} = 5 - V_{out} \approx$ between 5 to 4 Volt

So $V_{sd} \geq V_{sg} - V_{tp}$

Hence T_2 is in Sat^n region when $V_{out} = 0$ to 1 V

Otherwise, T_2 is in Resistive region

(ii) When $V_{in} = 5V$

$T_2 \Rightarrow V_{sg} = 5 - 5 = 0$ V,

So T_2 off (PMOS off)

T_1: $V_{gs} = 5 - 0 = 5$, T_1 (NMOS) $\Rightarrow$ on

So $V_{ds_1} = V_{out} = 0$ V

$V_{gs} - V_t = 5 - 1 = 4$

$V_{ds} = 0$ V

$\therefore V_{ds} < V_{gs} - V_t$ for T_1

So T_1 is ~~sad~~ resistive region

If the current capability of T_1 and T_2 during switching is the same, the rising and falling edge will be equal.