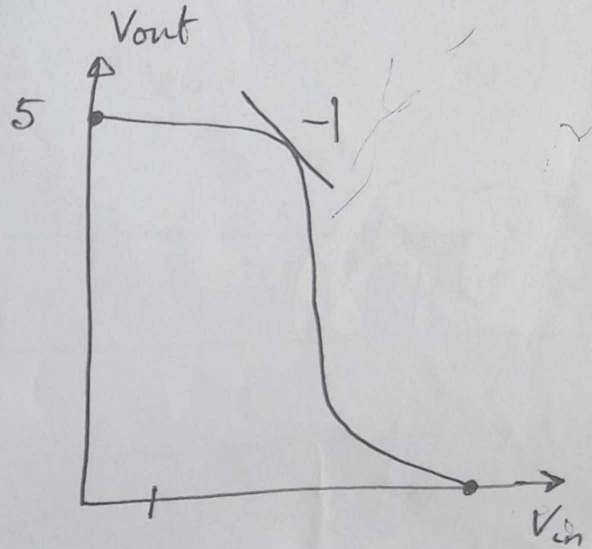
Noise Margin

V_{IL} : Highest voltage reliably recognized as logic LOW

V_{OL} : Nominal logic LOW voltage generated by a stage

V_{IH} : Lowest voltage reliably recognized as logic HIGH

V_{OH} : Nominal logic HIGH voltage generated by a stage



Say $V_{in} = 1.5$

in NMOS, $V_{gs} = 1.5$

$V_{ds} = 4.5$

$V_{gs} - V_t = 1.5 - 1 = 0.5 < V_{ds}$

So NMOS in Saturation

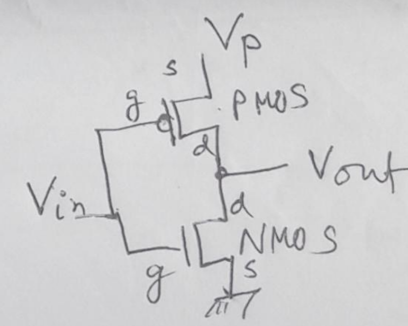
PMOS

$V_{sg} = V_p - V_{in} = 5 - 1.5 = 3.5$

$V_{sd} = V_p - V_{out} = 5 - 4.5 = 0.5$

$\therefore V_{sd} < V_{sg} - V_t$

So PMOS in Resistive



$\therefore I_{P(res)} = I_{N sat}$

$$\frac{\epsilon \cdot \mu_p}{D} \cdot \frac{W_p}{L_p} \left[(V_{sg} - V_{tp}) V_{sd} - \frac{V_{sd}^2}{2} \right]$$

$$= \frac{\epsilon \mu_N}{D} \cdot \frac{W_N}{L_N} \cdot \frac{1}{2} (V_{gs} - V_{tn})^2$$

We know $\mu_p = \frac{1}{2} \mu_N$

Let $\frac{W_p}{L_p} = 2 \cdot \frac{W_N}{L_N}$

$$\therefore \left(V_{sg} - V_{tp}\right)V_{sd} - \frac{V_{sd}^2}{2} = \frac{1}{2}\left(V_{gs} - V_{tn}\right)^2$$

$$\Rightarrow 2\left(V_p - V_i - V_{tp}\right)\left(V_p - V_o\right) - \left(V_p - V_o\right)^2 = \left(V_i - V_{tn}\right)^2$$

$$\Rightarrow \underbrace{\left(V_p - V_o\right)^2}_{x^2} - 2\underbrace{\left(V_p - V_o\right)}_{x}\left(V_p - V_i - V_{tp}\right) + \left(V_i - V_{tn}\right)^2 = 0$$

$$\therefore V_p - V_o = \frac{+2\left(V_p - V_i - V_{tp}\right) \pm \sqrt{4\left(V_p - V_i - V_{tp}\right)^2 - 4\left(V_i - V_{tn}\right)^2}}{2 \cdot 1}$$

$$\Rightarrow \cancel{V_p} - V_o = \cancel{V_p} - V_i - V_{tp} \pm \sqrt{\left(V_p - V_i - V_{tp}\right)^2 - \left(V_i - V_{tn}\right)^2}$$

$$\Rightarrow V_o = V_i + V_{tp} \pm \sqrt{\left(V_p - \cancel{V_i} - V_{tp} + \cancel{V_i} - V_{tn}\right) \times \left(V_p - V_i - V_{tp} - V_i + V_{tn}\right)}$$

$$= V_i + V_{tp} \pm \sqrt{\left(V_p - V_{tp} - V_{tn}\right)\left(V_p - 2V_{in} - V_{tp} + V_{tn}\right)}$$

Differentiating w.r.t. v_i

$$\therefore \frac{dv_o}{dv_i} = 1 + 0 + \left(V_p - V_{tp} - V_{tn}\right)^{1/2} \cdot \cancel{\frac{1}{2}} \cdot -\cancel{2}\left(V_p - 2V_i - V_{tp} + V_{tn}\right)^{-\frac{1}{2}}$$

$\Rightarrow$ putting $\frac{dv_o}{dv_i} = -1$

$$-1 = +1 - \frac{\sqrt{V_p - V_{tp} - V_{tn}}}{\sqrt{V_p - 2V_i - V_{tp} + V_{tn}}}$$

$$\therefore 4V_p - 8V_i - 4V_{tp} + 4V_{tn} = V_p - V_{tp} - V_{tn}$$

$$\Rightarrow 3V_p - 3V_{tp} + 5V_{tn} = 8V_i$$

$$\therefore V_i = \frac{3V_p - 3V_{tp} + 5V_{tn}}{8} = V_{IL}$$

putting $V_p = 5$

$V_{tp} = 1$

$V_{tn} = 1$

$$V_{IL} = \frac{3.5 - 3.1 + 5.1}{8} = \frac{15 - 3 + 5}{8} = \frac{17}{8} = 2.13\text{ V}$$

So Noise Margin for low

$= V_{IL} - V_{OL} = 2.13 - 0 = 2.13$ volts

$$\text{Similarly}\quad V_{IH} = \frac{5V_p - 5V_{tp} + 3V_{tn}}{8}$$

$$V_{IH} = \frac{25 - 5 + 3}{8} = \frac{23}{8} = 2.875$$

$$\therefore NM(1) = 5 - 2.875 = 2.125 \approx 2.13\text{ V}$$