4.7 Power consumption

There are two components that establish the amount of power dissipated in a CMOS circuit. These are:

1 Static dissipation — due to leakage current.
2 Dynamic dissipation — due to:
   a. switching transient current
   b. charging and discharging of load capacitances.

4.7.1 Static dissipation

Considering a complementary CMOS gate, as shown in Fig. 4.20, if the input = '0', the associated n-device is 'OFF' and the p-device is 'ON'. The output voltage is V_{DD} or logic '1'. When the input =

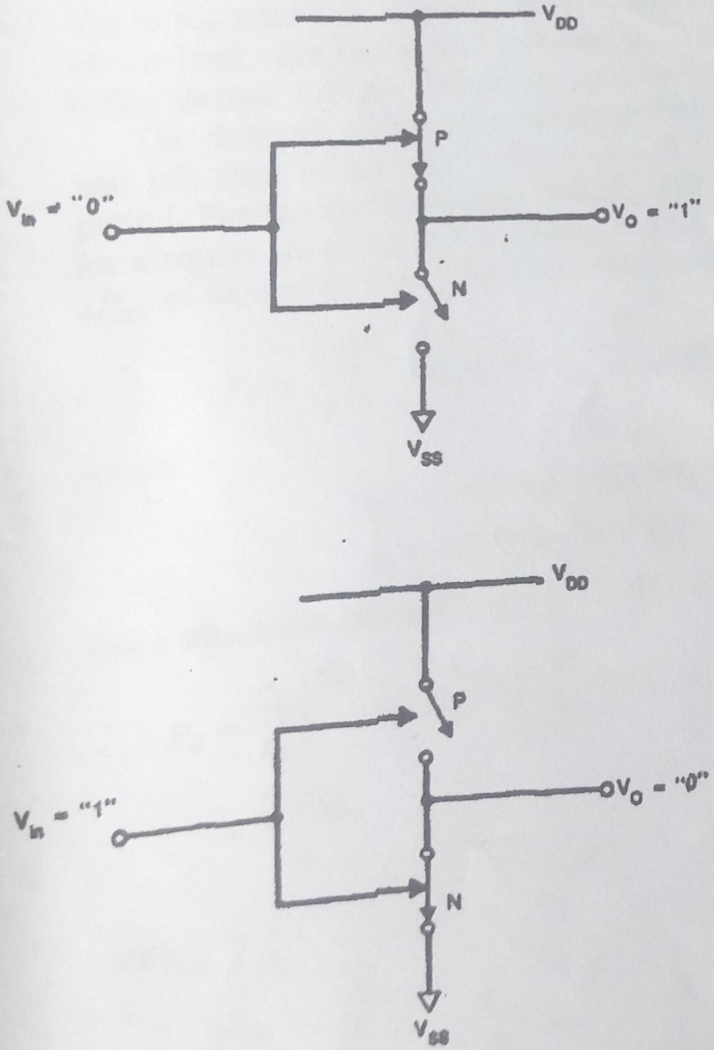

FIGURE 4.20. CMOS inverter states for static dissipation calculations

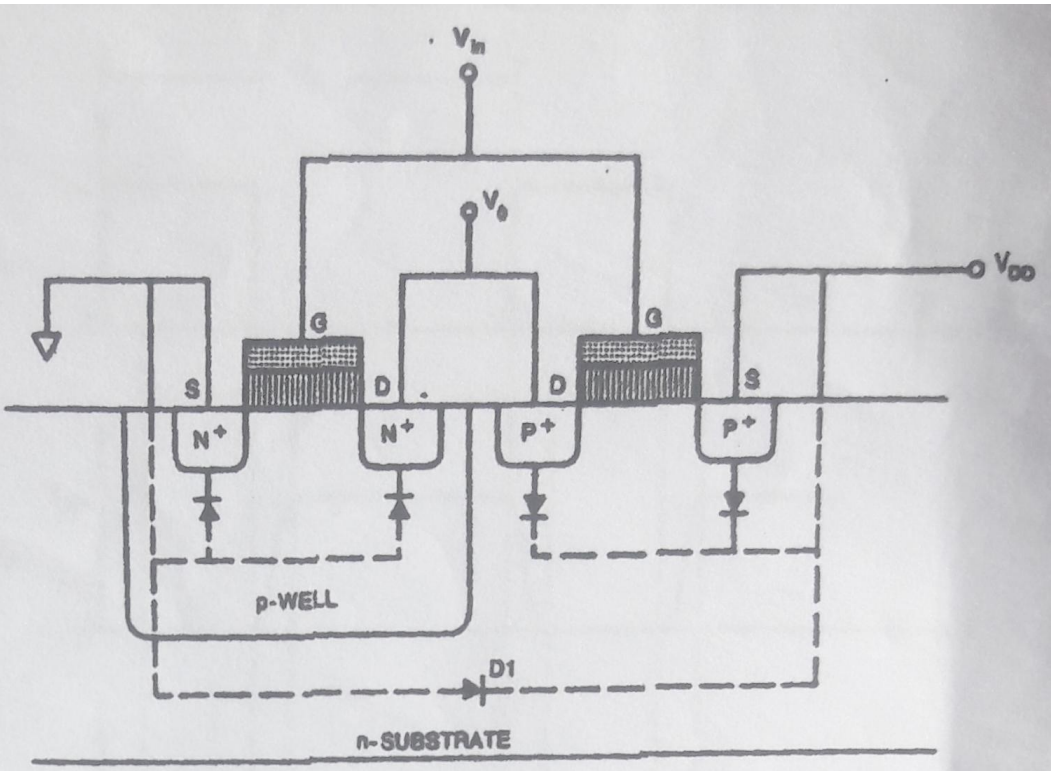

FIGURE 4.21. Model describing parasitic diodes

'1', the associated n-channel device is biased 'ON' and the p-channel device is 'OFF'. The output voltage is 0 volts (V_{SS}). Note that one of the transistors is always 'OFF' when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no D.C. current path from V_{DD} to V_{SS}, the resultant quiescent (steady state) current, and hence power P_s, is zero.

However, there is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate. We need to look at a simple model that describes the parasitic diodes for a CMOS inverter in order to have an understanding of the leakage involved in the device. The source-drain diffusions and the p-well diffusion form parasitic diodes. This can be represented in the profile of an inverter shown in Fig. 4.21. In the model, diode D1 is a parasitic diode between p-well to substrate. Since parasitic diodes are reverse biased, only their leakage current contributes to static power dissipation. The leakage current is described by the diode equation

$$i_o = i_s(e^{qV/kT} - 1), \tag{4.36}$$

where

i_s = reverse saturation current

V = diode voltage

q = electronic charge

k = Boltzmann's constant

T = temperature.

The static power dissipation is the product of the device leakage current and the supply voltage. A useful estimate is to allow a leakage current of 0.1nA to 0.5nA per gate at room temperature. Then total static power dissipation P_S is obtained from

$$P_S = \sum_{1}^{n} \text{leakage current} * \text{supply voltage}, \qquad (4.37)$$

where

n = number of devices.

For example, typical static power dissipation due to leakage for an inverter operating at 5 volts is between 1–2 nano-watts.

4.7.2 Dynamic dissipation

During transition from either '0' to '1' or, alternatively, from '1' to '0', both n- and p-transistors are on for a short period of time. This results in a short current pulse from V_{DD} to V_{SS}. Current is also required to charge and discharge the output capacitive load. This latter term is generally the dominant term. The current pulse from V_{DD} to V_{SS} results in a "short-circuit" dissipation which is dependent on the load capacitance and gate design. This is of relevance to I/O buffer design. Further discussion may be found in [Veen84].

The dynamic dissipation can be modeled by assuming the rise and fall time of the step input is much less than the repetition period. The average dynamic power, P_d, dissipated during switching for a square-wave input V_{in}, having a repetition frequency of $f_p = 1/t_p$, as shown by Fig. 4.22 (page 148), is given by

$$P_d = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)V_0\,dt + \frac{1}{t_p}\int_{t_p/2}^{t_p} i_p(t)(V_{DD} - V_0)\,dt, \qquad (4.38)$$

where

i_n = n-device transient current

i_p = p-device transient current.

For a step input and with $i_n(t) = C_L\,dV_0/dt$ (C_L = load capacitance)

$$P_d = \frac{C_L}{t_p}\int_0^{V_{DD}} V_0\,dV_0 + \frac{C_L}{t_p}\int_{V_{DD}}^{0} (V_{DD} - V_0)\,d\,(V_{DD} - V_0)$$

$$= \frac{C_L V_{DD}^2}{t_p} \qquad (4.39)$$

with $f_p = \dfrac{1}{t_p}$,

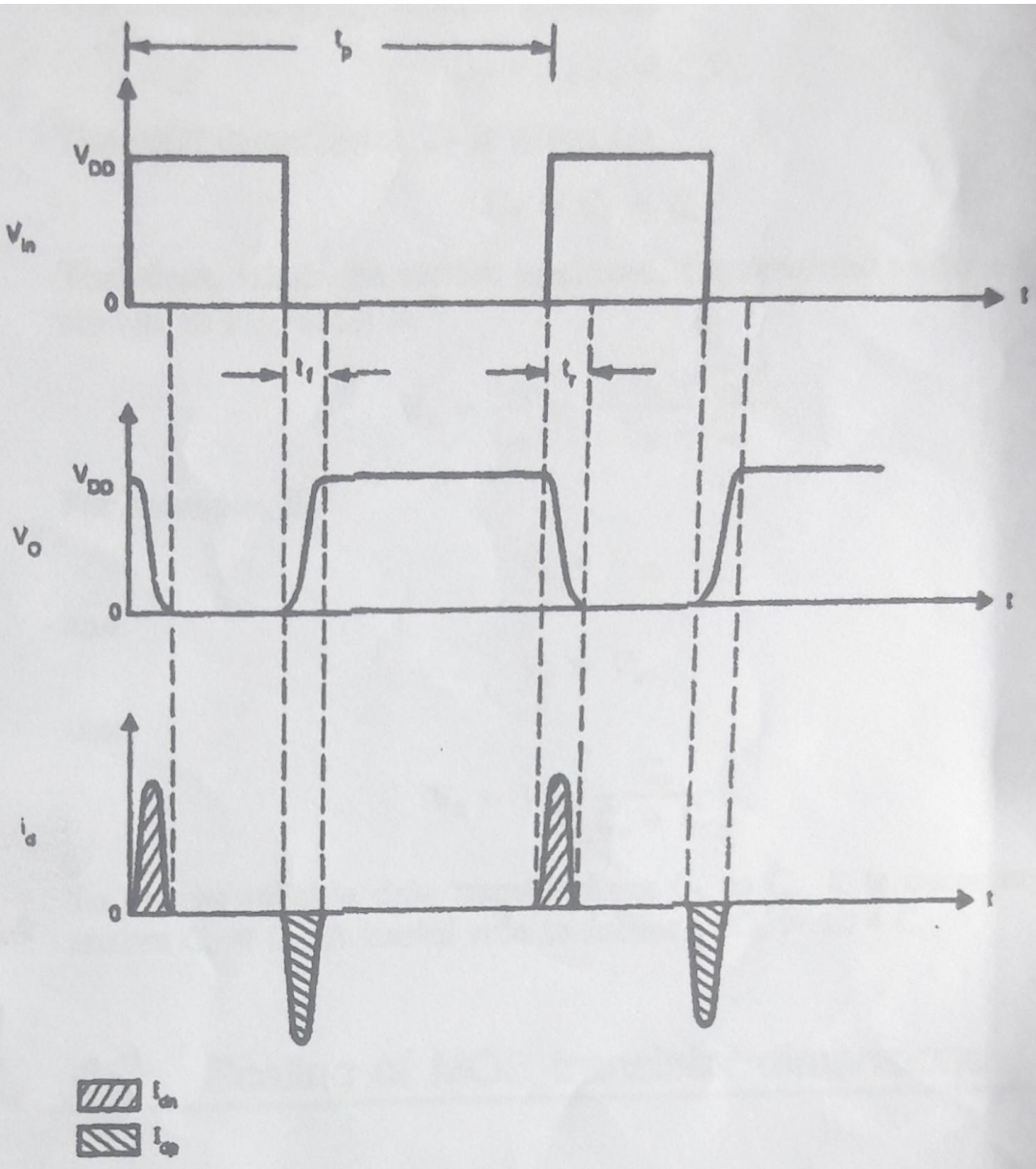

FIGURE 4.22. Waveforms for determination of dynamic power dissipation

resulting in

$$P_d = C_L V_{DD}^2 f_p. \tag{4.40}$$

Thus for a repetitive step input the average power that is dissipated is proportional to the energy required to charge and discharge the circuit capacitance. The important factor to be noted here is that Eq. (4.40) shows power to be proportional to switching frequency but independent of the device parameters.

Total power dissipation can be obtained from the sum of the two dissipation components, so

$$P_{total} = P_s + P_d. \tag{4.41}$$

When calculating the power dissipation, a rule of thumb is to add all capacitances operating at a particular frequency and calculate the power. Then the power from other groups operating at different frequencies may be summed. The dynamic power dissipation may be used to estimate total power consumption of a circuit and also