CSE-411

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Ans. to the ques. no. - 01

We know that,

edge time $\propto \frac{C_{out}}{W/L}$

where, $\frac{W}{L}$ is the pull-down transistor aspect ratio

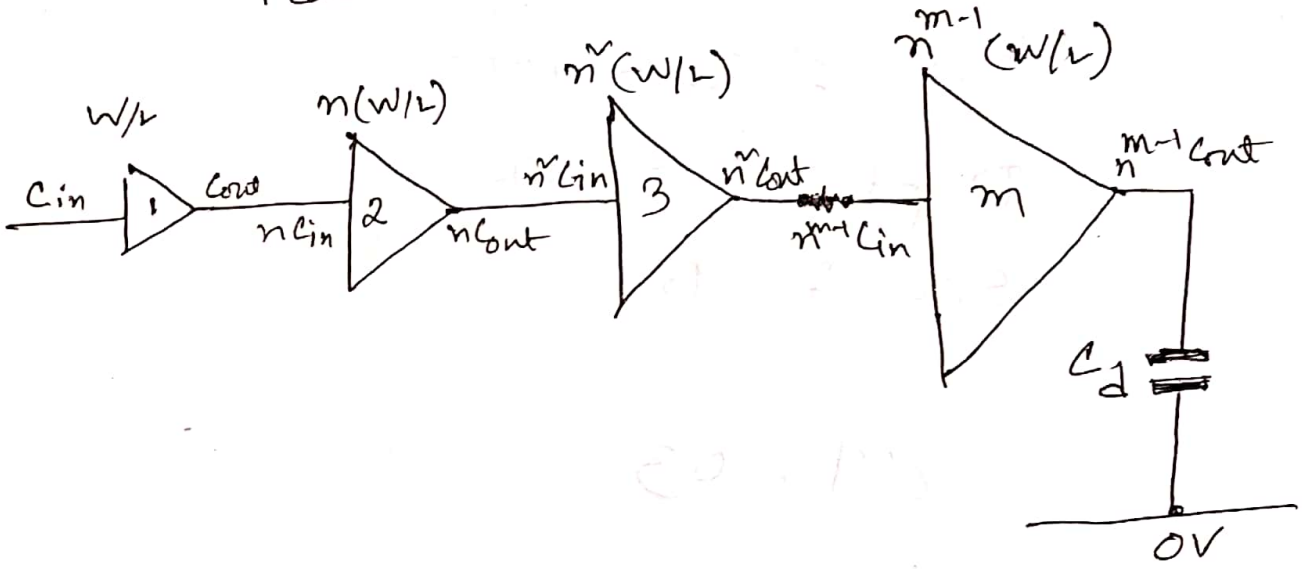

Fig: Buffer Gate Chain

We can say that, the load capacitance on each output increases by a factor of n at each stage and,

$$C_d = n^m C_{in}$$

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So,

$$C_d = n^m C_{in}$$

$$\Rightarrow \frac{C_d}{C_{in}} = n^m$$

$$\Rightarrow \log_e (C_d/C_{in}) = \log_e (n^m)$$

$$\Rightarrow \log_e (C_d/C_{in}) = m \cdot \log_e n$$

$$\Rightarrow m = \frac{\log_e (C_d/C_{in})}{\log_e n}$$

Now,

The load capacitance of gate 'i' is: $n^{i-1}(C_{out} + nC_{in})$ and its aspect ratio: $n^{i-1}(W/L)$ So,

$$\text{edge time of gate 'i'} \propto \frac{n^{i-1}(C_{out} + nC_{in})}{n^{i-1}(W/L)}$$

$$\propto \frac{C_{out} + nC_{in}}{W/L}$$

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which is independent of the gate's position in the chain.

The edge time can be regarded as a measure of the delay through a gate and so the delay t_d through the chain is:

$$t_d \propto \frac{(C_{out} + nC_{in})m}{W/L}$$

substituting in $\frac{\log_e (C_g/C_{in})}{\log_e n}$ for m gives:

$$t_d \propto \frac{(C_{out} + n C_{in}) \log_e (C_g/C_{in})}{(W/L) \log_e n}$$

$$\propto \frac{C_{out}/C_{in} + n}{\log_e n}$$

Also differentiating with respect to n:

$$\frac{dt_d}{dn} \propto \frac{\log_e n - (C_{out}/C_{in} + n)/n}{(\log_e n)^2}$$

(8)

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Ans. to the ques. no.- 02

Main problems of NMOS pass transistors:

① NMOS pass transistor allows designer to implement function in a much smaller silicon area than other design allow. However, it should be noted that the pass transistor is a dynamic circuit and once the transistor is off, the output state is held change on the capacitor ~~on~~ Cout. Dynamic logic circuits therefore have a minimum frequency of operation (around 5 KHz) in order to avoid a significant deterioration of the output signal.

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(2) when removing ϕ is equivalent to applying negative step of voltage to two capacitors. This causes V_{out} to fall for a minimum geometry device where $L = W = 6\,\mu m$ is of the order of 0.1 fF. drives a restoring inverter.