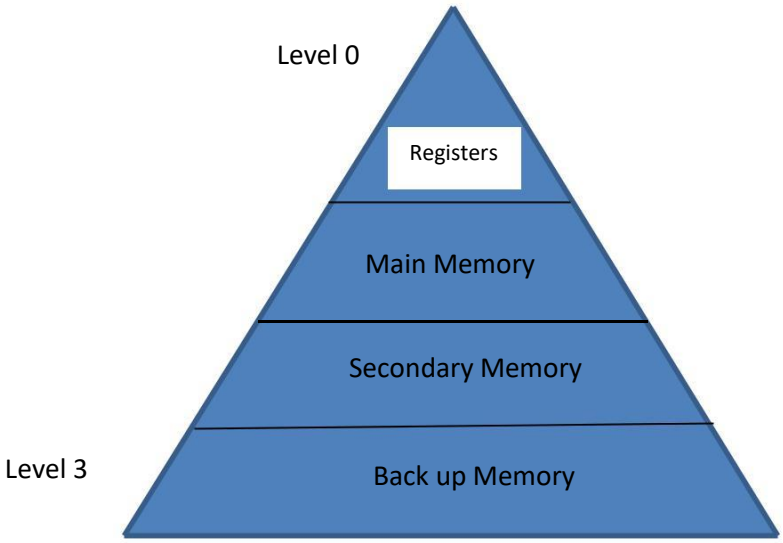
CSE 3027.2
Introduction to Embedded Systems
MEMORY MANAGEMENT

In computing, **memory** refers to the computer hardware devices involved to store information for immediate use in a computer.

Hierarchy of Memory Organization:



Category them in term of parameters:

1. Memory Size (Gradually increasing from level 0 to level 3)
2. Access time (Gradually increasing from level 0 to level 3)
3. Cost Per Byte (Gradually decreasing from level 0 to level 3)
4. Unit per Transfer (Gradually increasing from level 0 to level 3)
5. Transfer Bandwidth (Gradually increasing from level 0 to level 3)

Semiconductor Memory Fundamentals

In the design of all computers, semiconductor memories are used as primary storage for data and code. They are connected directly to the CPU and they are the memory that the CPU asks for information (code or data). Among the most widely used are RAM and ROM.

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Memory Capacity

The number of bits that a semi conductor memory chip can store is called its chip capacity (bits or bytes)

Memory Organization

- Each memory chip contains 2^x locations where x is the number of address pins on the chip
- The entire chip will contain 2^x x y bits. Ex. Memory organization of 4K x 4: 212 = 4096 locations, each location holding 4 bits.

Memory Speed (Access time)

Types of ROM

Programmable Read-Only Memory (PROM)

This type of ROM can be re-programmed by using a special device called a PROM programmer. Generally, a PROM can only be changed/updated once.

Erasable Programmable Read-Only Memory (EPROM)

This type of ROM can have its contents erased by ultraviolet light and then reprogrammed by an RPROM programmer. This procedure can be carried out many times; however, the constant erasing and rewriting will eventually render the chip useless.

Electrically Erasable Programmable Read-Only Memory (EEPROM)

This type of ROM works in a similar way to Flash memory in that it can its contents can be 'flashed' for erasure ad then written to without having to remove the chip from its environment. EEPROMs are used to store a computer system's BIOS, and can be updated without returning the unit to the factory. In many cases, BIOS updates can be carried out by computer users wishing a BIOS update.

Organization:

- Each block is made of either diode/transistor. If there is no diode in a memory cell then it is depicted as 0 otherwise 1. Diodes are fabricated at the time of manufacturing. Using of transistor is also the same. If the line of Base is fabricated, it is considered as 1 otherwise 0

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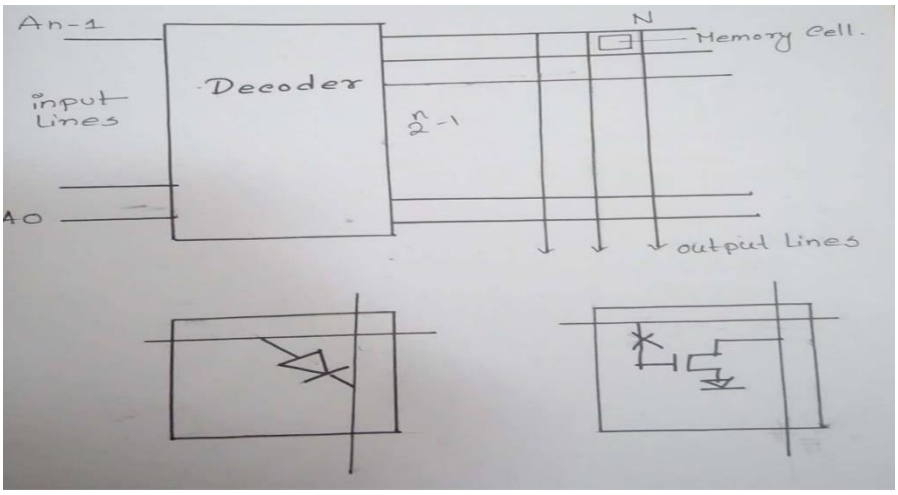

Random Access Memory (RAM)

- Random-access memory, or RAM, provides large quantities of temporary storage in a computer system.
  - Memory cells can be accessed to transfer information to or from any desired location, with the access taking the same time regardless of the location

- ***SRAM (Static RAM)***
  - Memory behaves like latches or flip-flops
- ***DRAM (Dynamic Memory)***
  - Memory lasts only for a few milliseconds
  - Must "refresh" locations by reading or writing

Dynamic RAM is the most common type of memory in use today. Inside a dynamic RAM chip, each memory cell holds one bit of information and is made up of two parts: a transistor and a capacitor. These are, of course, extremely small transistors and capacitors so that millions of them can fit on a single memory chip. The capacitor holds the bit of information -- 0 or a 1 The transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state. A capacitor is like a small bucket that is able to store electrons. To store a 1 in

the memory cell, the bucket is filled with electrons. To store a 0, it is emptied. The problem with the capacitor's bucket is that it has a leak. In a matter of a few milliseconds a full bucket becomes empty. Therefore, for dynamic memory to work, either the CPU or the memory controller has to come along and recharge all of the capacitors holding a 1 before they discharge. To do this, the memory controller reads the memory and then writes it right back. This refresh operation happens automatically thousands of times per second.

This refresh operation is where dynamic RAM gets its name. Dynamic RAM has to be dynamically refreshed all of the time or it forgets what it is holding. The downside of all of this refreshing is that it takes time and slows down the memory.

SRAM (Static RAM) is random access memory (RAM) that retains data bits in its memory as long as power is being supplied. Unlike dynamic RAM (DRAM), which stores bits in cells consisting of a capacitor and a transistor, SRAM does not have to be periodically refreshed. In static Ram, flip flop hold the data. Each flip flop needs 4 or 6 transistors. Static RAM provides faster access to data and is more expensive than DRAM. SRAM is used for a computer's cache memory and as part of the random access memory digital-to-analog converter on a video card.

Architecture of SRAM

RAM is organized in 2 dimensions Row and Column. If the Ram was organized in one dimension, then all the 16 bit of address bus (16 bit address bus Mp) will go directly to the decoders and will generate 2^{16} functions. The output of the decoder will be 16 bit for each which will cause a great load on the decoder. By dividing the address is row and column, the complexity of the decoder reduced from n to $\sqrt{n}$.

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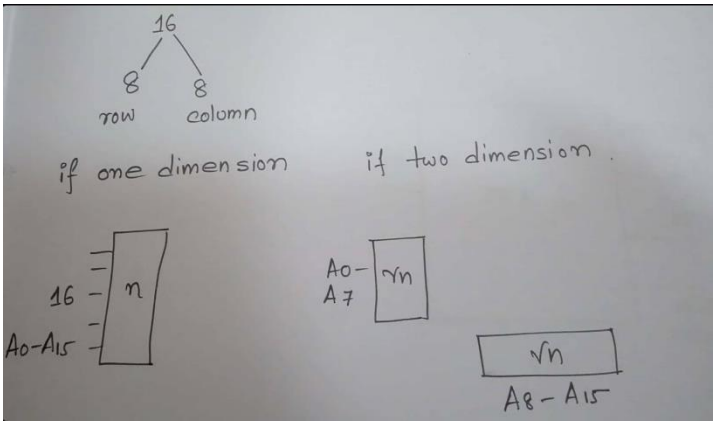
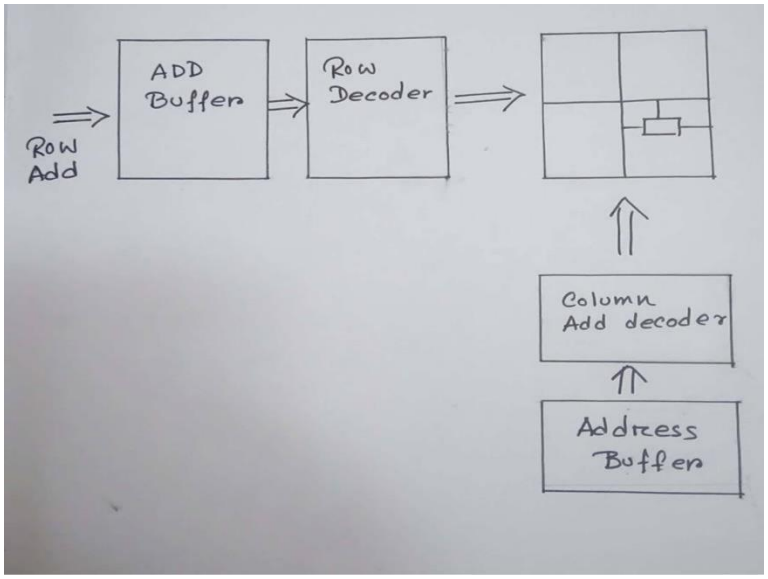


For example:

Suppose, a microprocessor has 4 bit address bus. If the addresses are considered as one dimension then 4 bits will go to one decoder and generate a function of 2^4=16, the complexity of this decoder is N=16. Again if we decompose then in row and column, then each decoder will get 2 inputs and generate 2^2=4 , the complexity will be N=4 each. Here the complexity of the decoders reduced from N to √N.



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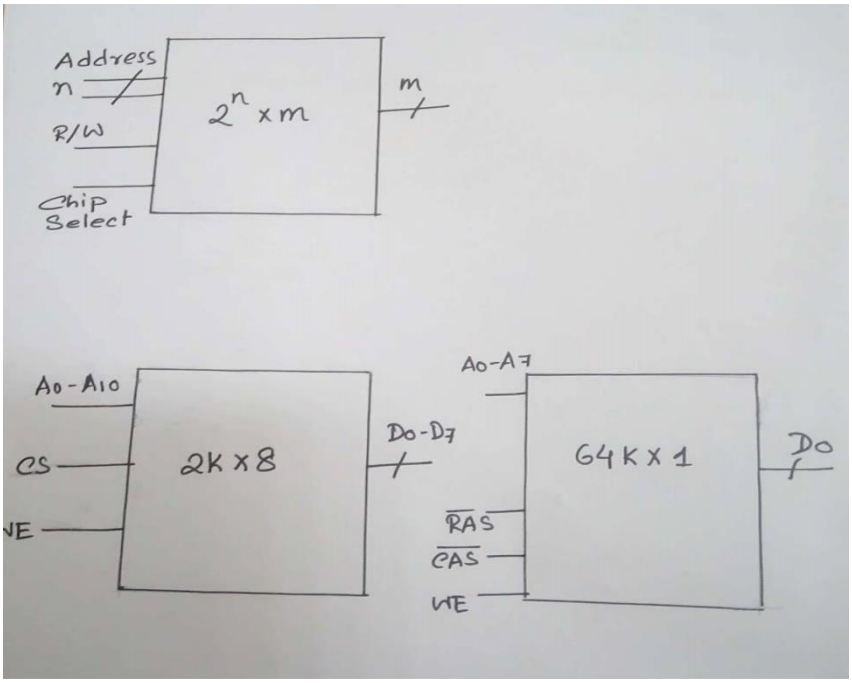
Difference between SRAM and DRAM

Static RAM	Dynamic RAM
➢ SRAM uses transistor to store a single bit of data	➢ DRAM uses a separate capacitor to store each bit of data
➢ SRAM does not need periodic refreshment to maintain data	➢ DRAM needs periodic refreshment to maintain the charge in the capacitors for data
➢ SRAM's structure is complex than DRAM	➢ DRAM's structure is simplex than SRAM
➢ SRAM are expensive as compared to DRAM	➢ DRAM's are less expensive as compared to SRAM
➢ SRAM are faster than DRAM	➢ DRAM's are slower than SRAM
➢ SRAM are used in Cache memory	➢ DRAM are used in Main memory

Typical Organization of a memory chip



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Incompatibility in Memory Interface:

- **Bus incompatibility:** In some microprocessor the address is generated in time division multiplexed form. Same bus used for address and data (AD0-AD7). So it need to be demultiplexed before going to RAM , otherwise RAM cannot decode the actual address and data sent by the microprocessor. Need extra hardware for compatibility.
- **Read/Write incompatibility:** CPU generated R/W and memory understandable read/write may not be in same form. Need additional gates to make them compatible.
- **Electrical incompatibility:** CPU is provided with some driving capability ie voltage, current. CPU may not able to drive a large number of chips simultaneously, need tristate buffer as a solution here.

Tristate buffer is useful device that allows us to control when current passes through the device and when it is not.

C	Z
0	Z – high impedence
1	X – the input

- **Timing/Speed incompatibility:** provide wait state to mitigate this incompatibility.

Address Spaces

Book: (From Rafiquzzaman)

- Linear addressing
- Full decoding
- Partial decoding