বাংলাদেশ ইউনিভার্সিটি অব প্রফেশনালস্

সেকশন/গ্রুপ..... B (Section-B)

ইনভিজিলেটরের স্বাক্ষর

মোট পৃষ্ঠা সংখ্যা.....10.....টি

BSc. in CSE-17, Final Exam (Fall) Dec-2020 পরীক্ষা(Examination), 20 20

বিষয় (Subj): VLSI Design পত্র/কোর্স নং (Paper/Course No): CSE-411

পত্র/কোর্সের নাম (Paper/Course Name): CSE-17 কেন্দ্র (Center): MIST

রেজিঃ নম্বর (Regn No): 1314011700018 শিক্ষাবর্ষ (Session): 2019-2020

রোল নম্বর (Roll No): 201714018 তারিখ (Date): 13-12-2020

INSTRUCTIONS FOR EXAMINEE

1. Examinees are forbidden to write their names either on outer cover page or anywhere of the answer scripts. In case of violation, the answer script will not be evaluated.
2. Examinees must mention their roll and registration number along with session on the outer cover page of the answer scripts clearly. Otherwise, answer scripts may not be evaluated.
3. Students will write his examination roll number on the top left corner and section-A/B on the top right corner of each page. All pages must be numbered chronologically at the bottom center in x of y format. (for example: 1 of 21)
4. All rough works should be done in the same paper used as answer scripts. Answer scripts should be submitted intact. Papers used for rough work should be pen through by the examinees.
5. In no case, an examinee will be allowed to start the examination half an hour after the commencement of examination.
6. Examinees must abide by the instructions of chief invigilator if there are no definite instructions on any subject/matter.
7. No examinee will be allowed to leave the examination session until an hour has elapsed from the commencement of examination.
8. Legal action will be taken against the examinees those are caught for copying and found guilty for any breach of discipline as per rule.

পরীক্ষক কর্তৃক পূরণীয়

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নিরীক্ষকের স্বাক্ষর

Continued.....

INSTRUCTIONS FOR EXAMINEE

9. Smoking is strictly prohibited during examination.

10. The Camera of the examinee MUST always be ON during the examination and answer script submission. If Camera is OFF then that online examination will be treated as CANCELLED.

11. The answer scripts submitted beyond specified time will be treated as CANCELLED.

12. The examinee has to share his/her computer screen to the invigilator throughout the examination time.

13. The focus of the camera should be such that the invigilator(s) can see the script and examinee with his/her surroundings.

14. The examinee will send his/her scanned examination script in PDF format to the following e-mail addresses:

(a) e-mail address of subject invigilator/examiner.

(b) Central Database Scheme (coursecode@mist.ac.bd)

Example: EECE433@mist.ac.bd

15. The examinee has to preserve the original answer script of every examination and be ready to submit whenever asked for.

16. Answer script should be the A4 size papers with a cover page provided by Department. Examinee has to fill up his/her necessary details on the cover page. Section A and section B must be clearly marked on the cover page like. **Section A** or **Section B**

17. Examination duration for each subject will be two hours (section-A for one hour + section B for One hour). In between students will get 20 minutes time to submit the answer script of section A and 10 minutes time to issue the question for section B . After completion of 01 hour examination time for section B, students will get 20 minutes to submit the answer script of section B.

18. After completion of written examination (online/physical), viva will be conducted by the respective faculty of that subject.

Section-B

Ans. to the ques. no.-05(a)

Below is a drawing of circuit diagram and stick diagram of the eqn, $Y = AB' + CD + E$ with CMOS gates:

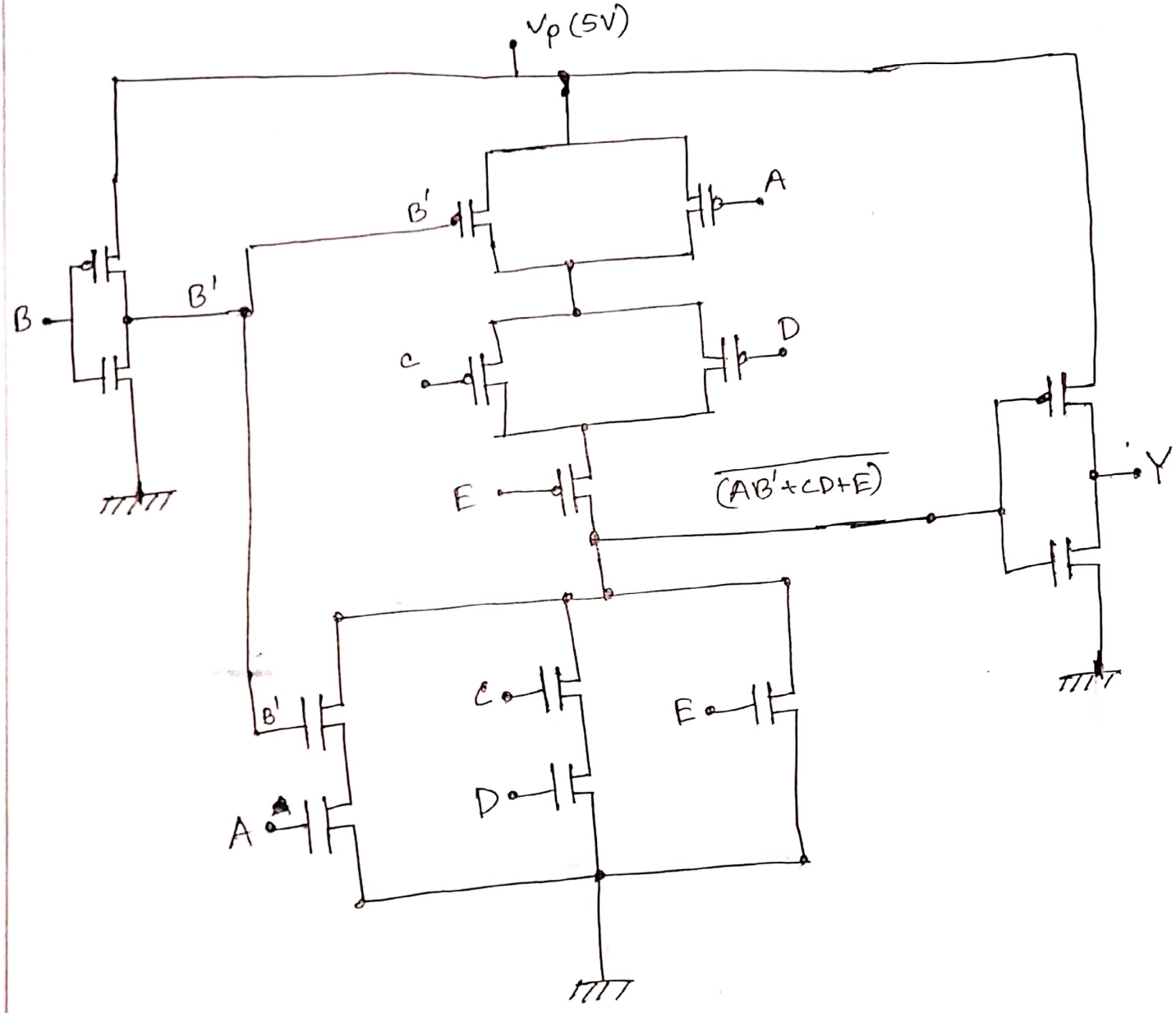


Fig: Circuit Diagram of Y with CMOS gates

P.T.O →

Stick diagram: $Y = AB' + CD + E$

'D' → Drain
'S' → Source

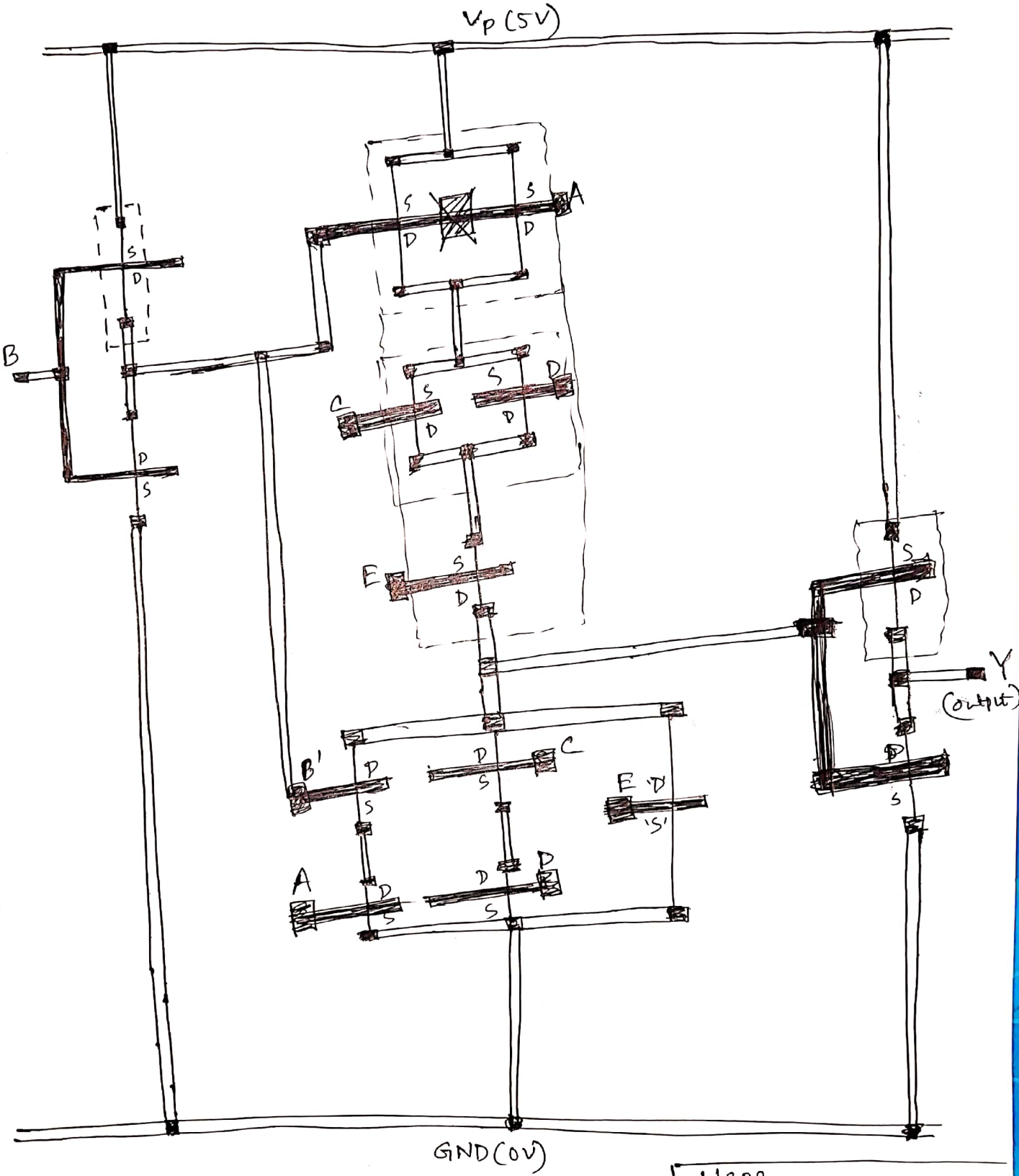


fig: Stick diagram of Y

Here,
- Diffusion (NMOS)
- P-Diffusion (PMOS)
- Metal
- Contact cut
- Polysilicon

Ans. to the ques. no. - 05(b)

"The minimum distance between N-well and p-diffusion is 4λ" - I donot agree with the statement.

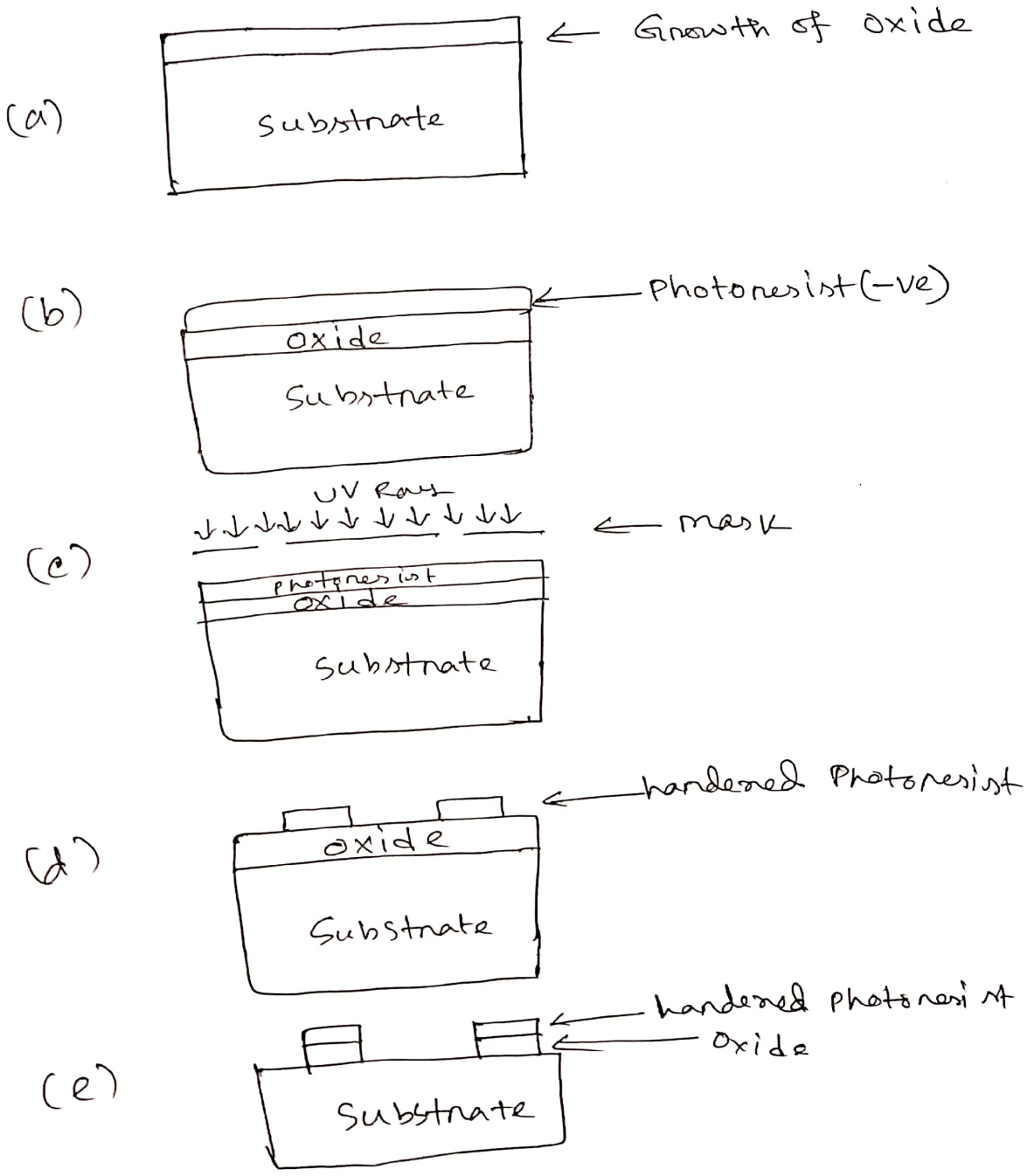
From the Design Rules from VLSI Fabrication we know that " N-well surrounds PMOS with a distance of 6λ and avoids NMOS with a minimum of 6λ".

So, N-well and p-diffusion distance should be atleast 6λ (instead of 4λ).

The reason for this distance is, to create a N-well in a p-substrate ion-implementation is needed (with pentavalent diffusion also). For that fabrication process if the distance between N-well and p-diffusion is lesser, than the fabrication will fail. That is why to properly fabricate the distance between N-well and p-diffusion must be atleast 6λ.

Ans. to the ques. no.-05(c)

Photoresist hardens when UV ray is given to its surface with an appropriate mask in the fabrication process. The fabrication process is shown in the below:



P.T.O.

(f)

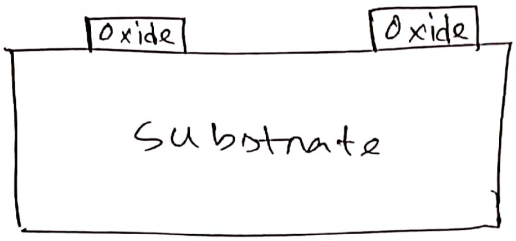


Fig: Fabrication Process.

Steps:

(a) Oxide surface is grown.

(b) Photoresist is applied on entire surface

(c) With mask, UV is given to to surface. to get disired pattern for hardening photoresists.

(d) Soft photoresists are removes with solvent.

(e) Oxide is etched, photoresist protects underlying oxide layers.

(f) photoresists is removed with solvent.

So, at step (c) photoresist is hardened, when UV is put on surface with a mask in the fabrication Process.

Ans. to the ques. no.-06(a)

CMOS inverter circuit:

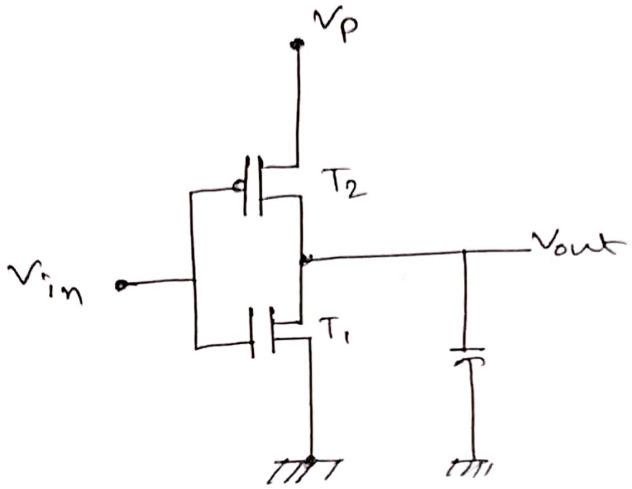


Fig: CMOS Inverter.

Short-circuit occurs when both T_1(NMOS) and T_2 (PMOS) are on. There exists a path from V_p to the Ground. So, short circuit occurs and a current flows from V_p to GND. This current creates the short-circuit power dissipation.

The fig for this scenario can be expressed:

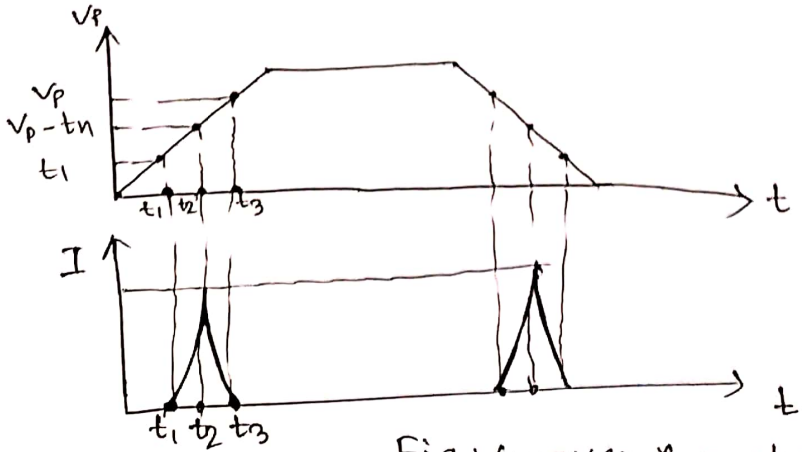


Fig: Curves for short-circuit of CMOS inverter.

So, we can get:

$$I_{mean} = \frac{1}{t_p}\int_0^{t_p} I(t)\,dt$$

$$= \frac{2}{t_p}\int_0^{t_3} I(t)\,dt$$

$$= \frac{4}{t_p}\int_{t_1}^{t_2} I(t)\,dt$$

$$= \frac{4}{t_p}\int_{t_1}^{t_2} \left\{ \frac{\epsilon \mu_n}{D}\frac{W}{L}\frac{(V_{gs}(t)-V_{tn})^2}{2} \right\} dt$$

$$= \frac{4}{t_p}\left(\frac{\epsilon \mu_n}{D}\frac{W}{L}\right)\frac{1}{2}\int_{t_1}^{t_2} (V_{gs}(t)-V_{tn})^2\,dt$$

$$= \frac{2}{t_p}\beta\int_{t_1}^{t_2} (V_i(t)-V_{tn})^2\,dt$$

$$= \frac{2\beta}{t_p}\int_{\frac{V_{tn}t_{r2}}{V_p}}^{\frac{t_{r2}}{2}} \left(\frac{V_p}{t_{r2}}t - V_{tn}\right)^2 dt$$

$$= \frac{2\beta}{t_p}\left[\frac{\left(\frac{V_p}{t_{r2}}t - V_{tn}\right)^3}{3\frac{V_p}{t_{r2}}}\right]_{\frac{V_{tn}t_{r2}}{V_p}}^{\frac{t_{r2}}{2}}$$

$$= \frac{2\beta}{t_p}\cdot\frac{t_{r2}}{3V_p}\left[\left(\frac{V_p}{t_{r2}}t - V_{tn}\right)^3\right]_{\frac{V_{tn}t_{r2}}{V_p}}^{\frac{t_{r2}}{2}}$$

Here,
$\because \beta = \frac{\epsilon \mu_n}{D}\frac{W}{L}$

we can get from fig circuit

$V_{gs}(t) = V_i(t)$

Also, we get

$V_i(t) = \frac{V_p - 0}{t_{r2} - 0}\,t$

$\Rightarrow \boxed{V_i(t) = \frac{V_p}{t_{r2}}\,t}$

when, $t = t_1$, $V_i = V_{tn}$

So, $V_{tn} = \frac{V_p}{t_{r2}}t_1$

$\Rightarrow t_1 = \frac{V_{tn}t_{r2}}{V_p}$

$t_2 = \frac{t_{r2}}{2}$

P.T.O.

So,

$$I_{mean} = \frac{2\beta}{t_p} \cdot \frac{t_{r2}}{3.V_p} \left[\left(\frac{V_p}{t_{r2}} t - V_{tn}\right)^3\right]_{\frac{V_{tn}\,t_{r2}}{V_p}}^{\frac{t_{r2}}{2}}$$

$$= \frac{2\beta\, t_{r2}}{3\, t_p V_p} \left[\left(\frac{V_p}{t_{r2}} \cdot \frac{t_{r2}}{2} - V_{tn}\right)^3 - \left(\frac{V_p}{t_{r2}} \cdot \frac{V_{tn}\, t_{r2}}{V_p} - V_{tn}\right)^3\right]$$

$$= \frac{2\beta\, t_{r2}}{3\, t_p V_p} \left(\frac{V_p}{2} - V_{tn}\right)^3$$

$$= \frac{2\beta\, t_{r2}}{3\, t_p V_p} \cdot \frac{1}{2^3} \left(V_p - 2V_{tn}\right)^3$$

$$= \frac{\beta\, t_{r2}}{12\, t_p V_p} \left(V_p - 2V_{tn}\right)^3$$

So,

$$I_{mean} = \frac{\beta t_{r2}}{12 t_p V_p} \left(V_p - 2V_{tn}\right)^3$$

We know,

power = I x V

So,

short-circuit power, $P_{sc} = I_{mean} \times V_p$

$$P_{sc} = \frac{\beta t_{r2}}{12 t_p V_p} \left(V_p - 2V_{tn}\right)^3 \times V_p$$

$$\boxed{P_{sc} = \frac{\beta t_{r2}}{12 t_p} \left(V_p - 2V_{tn}\right)^3}$$

this is the P_{sc} power-dissipation of CMOS INVERTER.

Ans. to the ques. no.-06(b)

given, eqn:

$$Y = (AB + C)'$$

circuit diagram (with NMOS) we get:

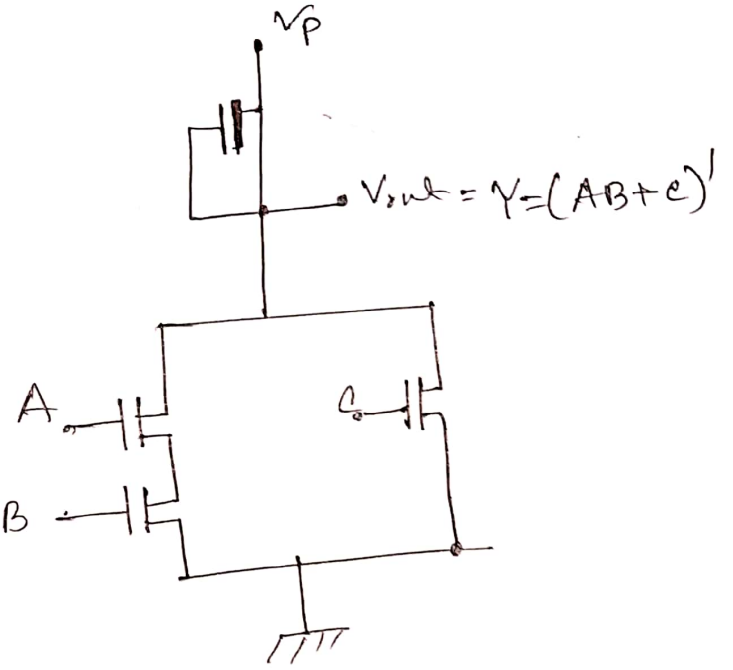


Fig: circuit diagram of Y

Stick diagram:

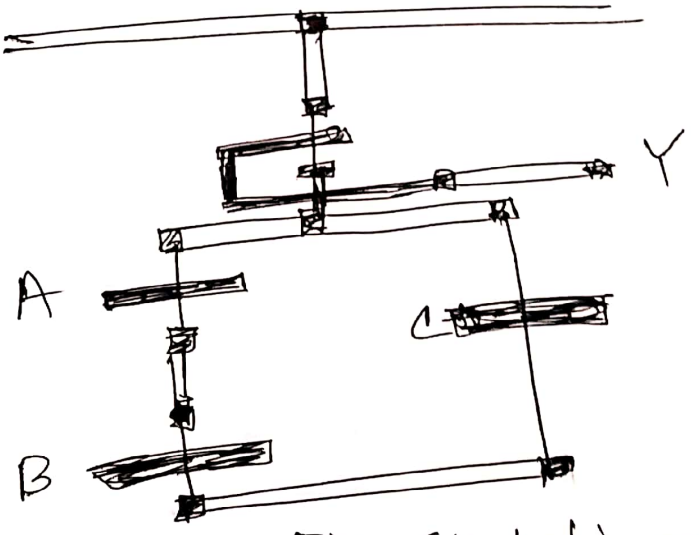


Fig: Stick diagram of Y.

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Graphical Layout of Y: