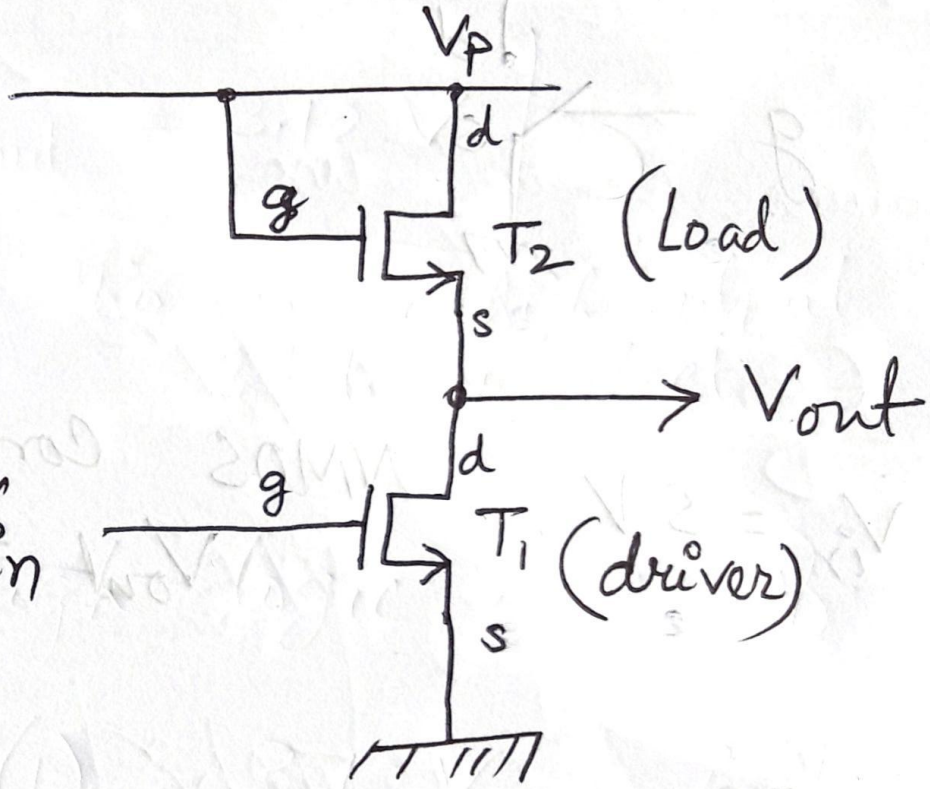
2.8 NMOS Inverter with an NMOS enhancement transistor load:



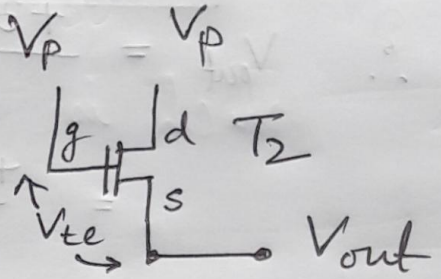
$T_2 \Rightarrow$ load transistor, $T_1 \Rightarrow$ driver transistor (ON/OFF switch)

gate of T_2 is V_p, so $V_{gs_{T_2}}$ is maximum.
So T_2 is always ON.

① When V_{in} = low

So T_1 is off
However, T_2 is ON,
So V_{te} drop

Small leakage current through T_1 brings T_2 just to Conduction.



$\therefore V_{out} = V_p - V_{te}$ ... (i)
$= 5 - 1 = 4\ V$

~~② When $V_{in} = V_p = 5$~~

However, source terminal of T_2 is not fixed (not grounded). So there exists significant body effect.

$$V_{te} = V_{teo} + \gamma \sqrt{V_{sb}} \quad \text{... (ii)}$$

putting the value of V_{te} in eqn (i)

$$V_{out} = V_p - V_{teo} - \gamma \sqrt{V_{sb}} \quad \text{.... (iii)}$$

$V_p = 5V$, $V_{teo} = 1V$, $V_s = V_{out}$, $V_b = 0V$
and $\gamma = 0.5\ V$

So $V_{out} = 5 - 1 - 0.5\sqrt{V_{out} - 0}$

$\Rightarrow 0.5\, V_{out}^{1/2} = 4 - V_{out}$

$\Rightarrow V_{out}^{1/2} = 8 - 2V_{out}$

Squaring both sides,

$$V_{out} = 64 + 4V_{out}^{2} - 32V_{out}$$

$$\Rightarrow 4V_{out}^{2} - 33V_{out} + 64 = 0$$

$$\therefore V_{out} = \frac{+33 \pm \sqrt{33^2 - 4\times4\times64}}{2\times4}$$

$$= \frac{+33 \pm \sqrt{65}}{8} = \frac{+33 \pm 8.06}{8}$$

$$= 5.13 \text{ or } 3.12 V$$

Since V_{out} cannot be higher than V_p

$$\boxed{V_{out} = 3.12 V}$$

This is the high output voltage due to body effect.

So the high logic value of this ckt is

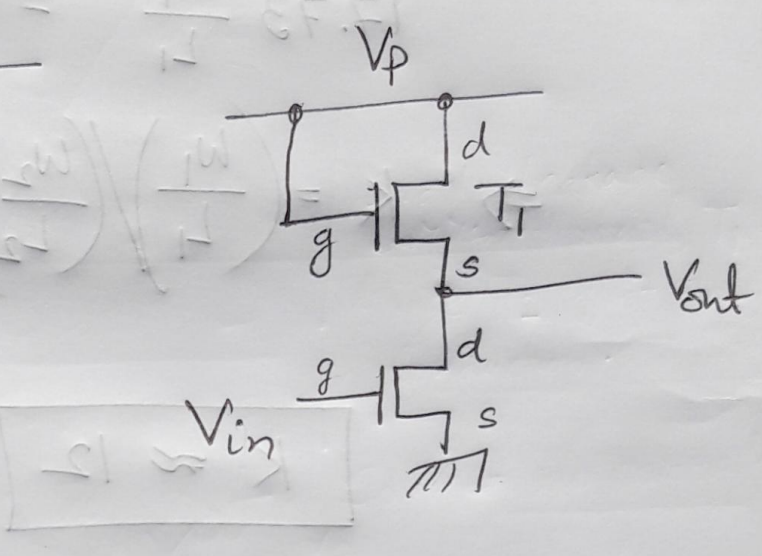
$$\boxed{V(1) = 3.12 V \quad V(0) = 0 V}$$

instead of 5V

Inverter Ratio Calculation

For this Calculation, we have to select the case when both Transistors conduct.

When V_{in} = high



T_1

$V_{gs_1} = 3.12\ V$

$V_{ds_1} = 0.3$

V_{ds_1}	$V_{gs_1} - V_t$
$=0.3$	$3.12 - 1$
	$= 2.12$

$\therefore V_{ds_1} < V_{gs_1} - V_t$

$\therefore T_1$ is in Resistive region

$$\therefore I_{ds_1} = 30 \times \frac{W_1}{L_1} \times \left[(3.12-1)0.3 - \frac{0.3^2}{2}\right]$$

$$= 17.73\left(\frac{W_1}{L_1}\right)\ \mu A$$

T_2

$V_{gs_2} = 5 - 0.3 = 4.7$

$V_{ds_2} = 5 - 0.3 = 4.7$

$\therefore V_{ds_2} > V_{gs_2} - V_t$

$4.7 > 4.7 - 1$

So T_2 is in Satⁿ

$$I_{ds_2} = 30 \times \frac{W_2}{L_2} \times \frac{1}{2}\left(V_{gs_2} - V_t\right)^2$$

$$= 30 \times \frac{W_2}{L_2} \times \frac{1}{2} \times (4.7-1)^2$$

$$= 205.4 \times \frac{W_2}{L_2}$$

Putting $I_{ds_1} = I_{ds_2}$

$$17.73 \frac{W_1}{L_1} = 205.4 \frac{W_2}{L_2}$$

$$\Rightarrow K = \left(\frac{W_1}{L_1}\right) / \left(\frac{W_2}{L_2}\right) = \frac{205.4}{17.73} = 11.6$$

$$\boxed{K \approx 12}$$

which is high for this inverter