BANGLADESH UNIVERSITY OF PROFESSIONALS
Military Institute of Science and Technology
B.Sc. in Computer Science and Engineering
Student Group : Earned Credit Hour >108, Final Examination (Fall) : Dec 2020

Subject: CSE – 411 VLSI Design

Total: 2.00 hours **Full Marks: 180**
Section B : 1.00 hour **Section B : 90**

INSTRUCTIONS:

a. Use **SEPARATE** answer scripts for each section.
b. **Question – 5 and Question – 8 (Viva Voce)** in **Section B** are compulsory.
c. Answer any **OTHER ONE** question from this section **(From Q - 6 & Q - 7)**.
d. Figures in the margin indicate full **marks**.
e. Assume reasonable data if necessary.
f. **Symbols** used have their usual meanings.

SECTION-B

Question – 5 (Compulsory)

a. Draw the circuit diagram and the stick diagram of the following using CMOS gates: **18**

$$Y = AB' + CD + E$$

b. " The minimum distance between N-well and p-diffusion is 4λ" – Do you agree with this statement? Why or why not? **10**

c. When does photoresist harden during fabrication process? Give an example scenario with figure. **8**

Question – 6

a. Derive the expression for short-circuit power dissipation of CMOS inverter. When does such power dissipation occur? **18**

b. Draw the geometrical layout of the following circuit using graph paper. **18**

$$Y = (AB + C)'$$

Question – 7

a. What is the noise margin of CMOS inverter for logic high input? Show all necessary assumptions and calculation. **20**

b. Find out the noise margin for NMOS inverter when **8**
$V_{te} = 1V$, $V_{td} = -4V$, $K=5$, $V_{out} = 0.2V$

c. What is the impact of scaling factor a on the gate-power of each NMOS transistor gate? Also find out the impact on total current and total speed-power product. **8**

Question – 8 Viva Voce (Compulsory) **18**