$$17.73 \frac{W_1}{L_1} = 205.4 \frac{W_2}{L_2}$$

$$\Rightarrow K = \left(\frac{W_1}{L_1}\right) \Big/ \left(\frac{W_2}{L_2}\right) = \frac{205.4}{17.73} = 11.6$$

$$\boxed{K \approx 12}$$

which is high for this inverter

$$\frac{W_1}{L_1} = \frac{3}{1} \qquad \frac{W_2}{L_2} = \frac{1}{4}$$

$$K = 3/1 \big/ 1/4 \approx 12$$

Such high inverter ratio

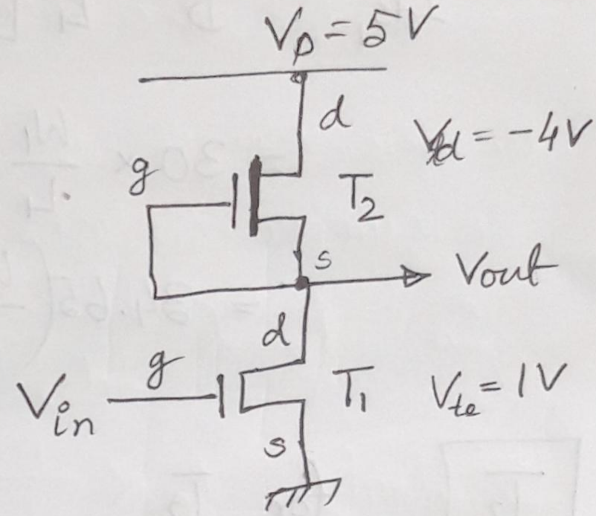
Drawbacks : (NMOS inverter with Enh. Transistor load)

1) Loss of Voltage for high output, $V(1) = 3.12\,V$
2) High rising time of Output voltage (Why??) Explain
3) Cascading issue
4) High inverter ratio, $K = 12$

2.9 NMOS inverter with an NMOS Depletion Transistor Load

T_1 : Driver, $V_{te} = 1V$

T_2 : Load, $V_{td} = -4V$



So for T_2 $V_{gs} = 0V$ (short)
$> V_{td}$

Hence $\boxed{T_2 \text{ is always ON}}$

When $V_{in} = 0$

T_1 is off

T_2 is ON

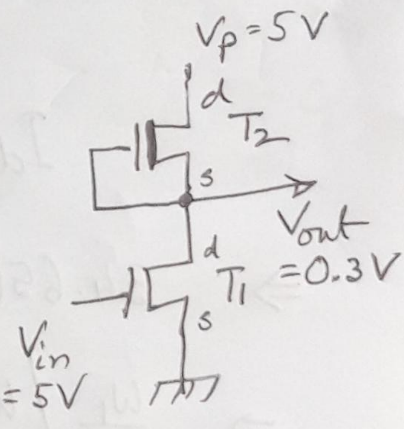
V_{out} charges through T_2 to $V_p = 5V$

(No loss of high voltage, it is 5V)
$V(1)$

When $V_{in} = 5V$, T_1 on, T_2 ON

So $V_{out} = 0.3V$

Calculation of Inverter Ratio (K)



So when $V_{in} = 5V$, $V_{out} = 0.3V$

$\boxed{T_1}$ $V_{gs_1} = 5V$, $V_{ds} = 0.3$ $V_{te} = 0.3 \times 1 = 0.3$

$V_{ds} < V_{gs} - V_{te}$

$0.3 \qquad 5 - 1$

So T_1 is in Resistive region

$$I_{ds_1} = \frac{\epsilon \mu_n}{D} \times \frac{W_1}{L_1}\left[(V_{gs_1} - V_{te})V_{ds_1} - \frac{V_{ds_1}^2}{2}\right]$$

$$= 30 \times \frac{W_1}{L_1}\left[(5-1)0.3 - \frac{0.3^2}{2}\right]$$

$$= 34.65\left(\frac{W_1}{L_1}\right) \mu A$$

$\boxed{T_2}$ for T_2

$V_{gs_2} = 0$, $V_{td} = -4V$, $V_{ds_2} = 5 - V_{out}$
$= 5 - 0.3 = 4.7$

$\therefore V_{ds_2} > V_{gs_2} - V_{td}$

Hence, T_2 is in Sat^n region

$V_{ds_2} = 4.7$
$V_{gs_2} - V_{td} = 0-(-4)$
$= 4$

$$I_{ds_2} = \frac{\epsilon \mu_n}{D} \times \frac{W_2}{L_2} \times \frac{1}{2}(V_{gs_2} - V_{td})^2$$

$$= 25 \times \frac{W_2}{L_2} \times \frac{1}{2}(0+4)^2$$

$$= 200\left(\frac{W_2}{L_2}\right) \mu A$$

$$I_{ds_1} = I_{ds_2}$$

$$\Rightarrow 34.65\left(\frac{W_1}{L_1}\right) = 200\left(\frac{W_2}{L_2}\right)$$

$$\Rightarrow \frac{W_1}{L_1} \Big/ \frac{W_2}{L_2} = \frac{200}{34.65} = 5.8 \approx 6$$

$$\Rightarrow \boxed{K = 6}$$

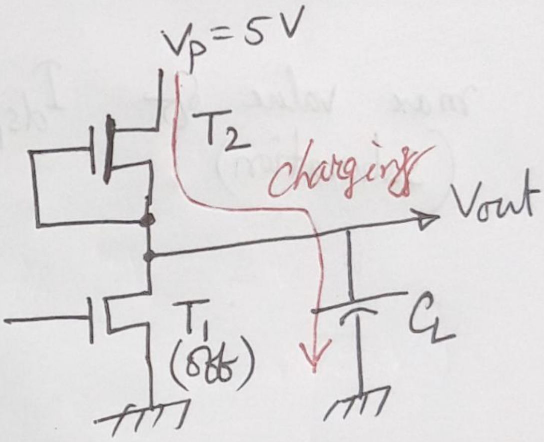
for Inverter with NMOS depletion Trans. load

Thus, for this case, inverter ratio is much less than the previous case (2.8).

Advantages:

1) High voltage is $V(1) = 5V$
2) Cascading is possible
3) lower value of K

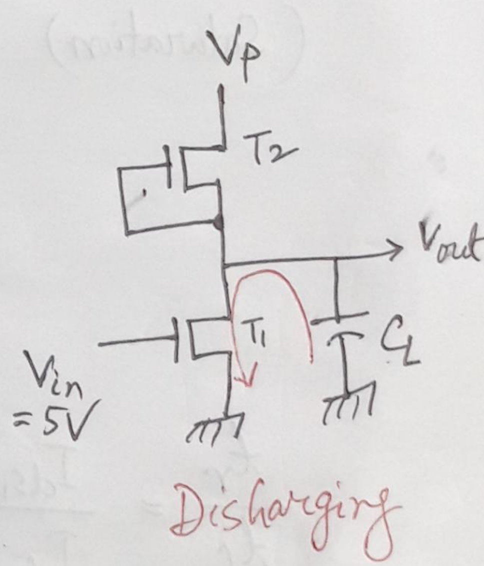
2.10 Edge times for NMOS inverter with a Depletion Load



$\boxed{\text{Charging}}$ of Load capacitor (C_L) is done from V_p to C_L through transistor T_2.

Thus, $V_{out} = 5V$ after charging finishes.

So I_{ds_2} plays the role while charging.

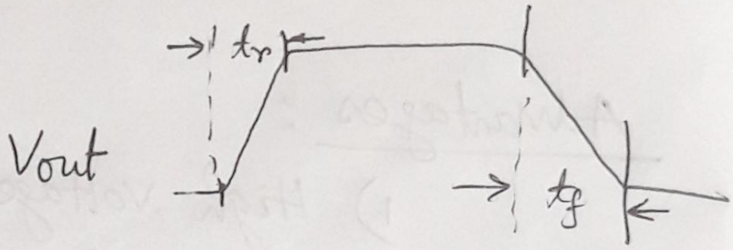


$\boxed{\text{Discharging}}$ When $V_{in} = 5V$, T_1 is on

Now C_L is discharged through T_1 to ground (0V)

So I_{ds_1} plays the role while discharging.

t_r = rise time
= output voltage rises from 0 to 5V



The more value of I_{ds_2}, the quicker V_{out} rises

So $t_r \propto \frac{1}{I_{ds_2}}$

Similarly $t_f \propto \frac{1}{I_{ds_1}}$

fall time

max value of (Saturation) $I_{ds_1} = \frac{\epsilon \mu_n}{D} \times \frac{W_1}{L_1} \times \frac{1}{2}(V_{gs_1} - V_t)^2$

$$= 30 \times \frac{W_1}{L_1} \times \frac{1}{2}(5-1)^2$$

$$= 240\left(\frac{W_1}{L_1}\right) \mu A$$

max value of (Saturation) $I_{ds_2} = \frac{\epsilon \mu_n}{D} \times \frac{W_2}{L_2} \times \frac{1}{2}(V_{gs_2} - V_{td})^2$

$$= 25 \times \frac{W_2}{L_2} \times \frac{1}{2}(0+4)^2$$

$$= 200\left(\frac{W_2}{L_2}\right) \mu A$$

$$\frac{t_r}{t_f} = \frac{I_{ds_1}}{I_{ds_2}} = \frac{\overset{6}{\cancel{240}}}{\underset{5}{\cancel{200}}} \times \frac{(W_1/L_1)}{(W_2/L_2)}$$

$$\therefore \boxed{\frac{t_r}{t_f} = \frac{6K}{5}}$$