বাংলাদেশ ইউনিভার্সিটি অব প্রফেশনালস্

সেকশন/গ্রুপ A (Section- A)

ইনভিজিলেটরের স্বাক্ষর

মোট পৃষ্ঠা সংখ্যা 13 টি

BSc in CSE-17, Fall, Final Exam, Dec-2020 পরীক্ষা(Examination), 20 20

বিষয় (Subj): VLSI Design পত্র/কোর্স নং (Paper/Course No): CSE-411

পত্র/কোর্সের নাম (Paper/Course Name): CSE-17 কেন্দ্র (Center): MIST

রেজিঃ নম্বর (Regn No): 1314011 70018 শিক্ষাবর্ষ (Session): 2019-2020

রোল নম্বর (Roll No): 201714018 তারিখ (Date): 13-12-2020

INSTRUCTIONS FOR EXAMINEE

1. Examinees are forbidden to write their names either on outer cover page or anywhere of the answer scripts. In case of violation, the answer script will not be evaluated.
2. Examinees must mention their roll and registration number along with session on the outer cover page of the answer scripts clearly. Otherwise, answer scripts may not be evaluated.
3. Students will write his examination roll number on the top left corner and section-A/B on the top right corner of each page. All pages must be numbered chronologically at the bottom center in x of y format. (for example: 1 of 21)
4. All rough works should be done in the same paper used as answer scripts. Answer scripts should be submitted intact. Papers used for rough work should be pen through by the examinees.
5. In no case, an examinee will be allowed to start the examination half an hour after the commencement of examination.
6. Examinees must abide by the instructions of chief invigilator if there are no definite instructions on any subject/matter.
7. No examinee will be allowed to leave the examination session until an hour has elapsed from the commencement of examination.
8. Legal action will be taken against the examinees those are caught for copying and found guilty for any breach of discipline as per rule.

পরীক্ষক কর্তৃক পূরণীয়

প্রশ্ন নম্বর	প্রদত্ত নম্বর
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পরীক্ষকের স্বাক্ষর

নিরীক্ষকের স্বাক্ষর

Continued......

INSTRUCTIONS FOR EXAMINEE

9. Smoking is strictly prohibited during examination.

10. The Camera of the examinee MUST always be ON during the examination and answer script submission. If Camera is OFF then that online examination will be treated as CANCELLED.

11. The answer scripts submitted beyond specified time will be treated as CANCELLED.

12. The examinee has to share his/her computer screen to the invigilator throughout the examination time.

13. The focus of the camera should be such that the invigilator(s) can see the script and examinee with his/her surroundings.

14. The examinee will send his/her scanned examination script in PDF format to the following e-mail addresses:

    (a) e-mail address of subject invigilator/examiner.

    (b) Central Database Scheme (coursecode@mist.ac.bd)
    Example: EECE433@mist.ac.bd

15. The examinee has to preserve the original answer script of every examination and be ready to submit whenever asked for.

16. Answer script should be the A4 size papers with a cover page provided by Department. Examinee has to fill up his/her necessary details on the cover page. Section A and section B must be clearly marked on the cover page like. **Section A** or **Section B**

17. Examination duration for each subject will be two hours (section-A for one hour + section B for One hour). In between students will get 20 minutes time to submit the answer script of section A and 10 minutes time to issue the question for section B . After completion of 01 hour examination time for section B, students will get 20 minutes to submit the answer script of section B.

18. After completion of written examination (online/physical), viva will be conducted by the respective faculty of that subject.

Section-A

Ans. to the ques. no.- 01(a)

Given,

$W = L$ so, $\frac{W}{L} = 1$,

$\frac{\epsilon \mu_p}{D} = 12\ \mu A/V^2$,

$V_{tp} = 1V$

We know, for, PMOS :

$$I_{SD(sat)} = \frac{\epsilon \mu_p}{D}\left(\frac{W}{L}\right)\frac{(V_{sg} - V_{tp})^2}{2}$$

$$= 12 \times 1 \times \frac{(V_{sg} - 1)^2}{2}$$

$$= 6(V_{sg} - 1)^2$$

Creating a table for multiple values of V_{sg} :(Let $V_p = 5V$, $V_s = 5V$(for PMOS))

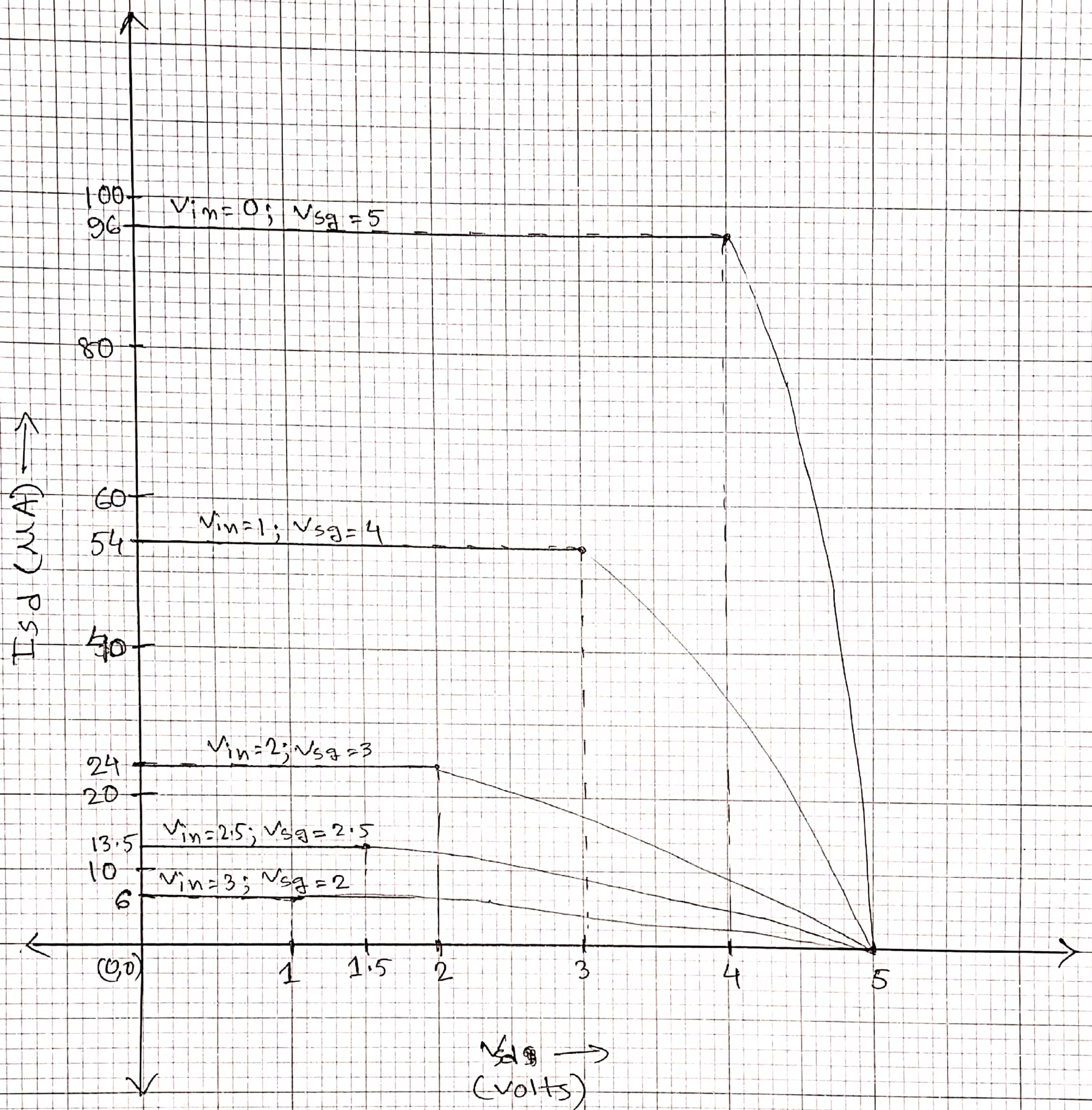
V_{in} (V)	$V_{sg} = V_s - V_g = 5 - V_{in}$ (V)	$V_{sd} = V_{sg} - V_{tp} = V_{sg} - 1$ (V)	$(V_{sg} - V_{tp})^2 = (V_{sg} - 1)^2$ (V^2)	$I_{SD} = 6(V_{sg} - 1)^2$ (μA)
3	2	1	1	6
2.5	2.5	1.5	2.25	13.5
2	3	2	4	24
1	4	3	9	54
0	5	4	16	96

P.T.O

Using the table above (previous page) the I-V characteristics curve for a PMOS is drawn in the graph paper: (attached Graph Paper)

P.T.O →
(Graph)

Roll No. 201714018



I-V characteristics curve for PMOS

MICRO

ARB 8 Inch x 10 Inch

Ans. to the ques. no.--01(b)

MOS inverter with enhancement trasistor:

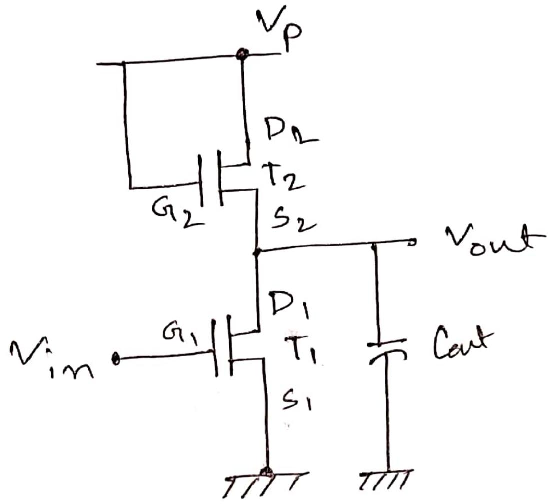


fig: NMOS inverter with enhancement type transistor(NMOS).

Here, the source (S_2) for T_2 transistor is not grounded. So, there will be a Body-effect associated with the transistor. We know, if there is a Body-effect then, threshold voltage increases, with, $V_t = V_{to} + \gamma\sqrt{V_{sb}}$, where, V_s= source voltage and V_b= substrate voltage.

So, we will not get the full output of High voltage. If $V_D = 5V$ and. $\gamma = 0.5$ ~~and~~ then, $V_t = 1 + 0.5\sqrt{1} = 1.5$

So, we will get high output around 3.12V instead of 5V for the input $V_{in} = 0V$. So, we can not use this circuit for cascading as then 3.12V will go lower further.

So we use depletion transistor for NMOS inverter.

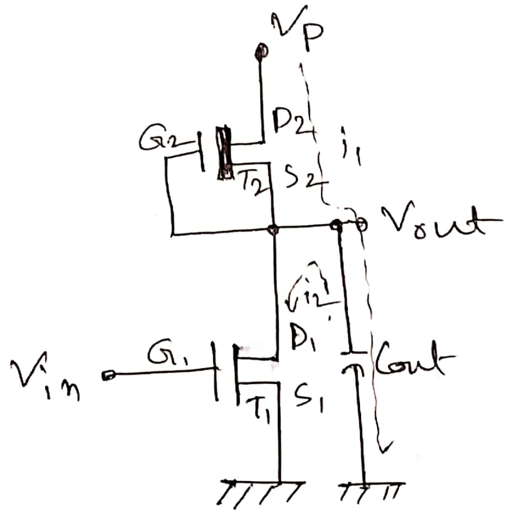


fig: NMOS inverter with depletion transistor.

For depletion, when, $V_{in} = 0V$ (High) T_1 will be Off, T_2 will be on. So, T_1 will charge C_{out} capacitor fully upto V_p(5V) as current through T_2, ($I_{ds_2} = 0$) (open circuit of T_1). So, output will be high (5V) V_p.

When, $V_{in} = 5V$ (Low), T_1 and T_2 will be on. So, C_{out} will discharge through T_1. So, V_{out} will be 0 V.

So, here we get 5V as Output High.

So we can use it as Cascading with other circuits. also ~~we~~ inverter ratio is lower in depletion.

201714018 Section-A

Ans. to the ques. no.-01 (c)

BJT:

- Faster than MOS
- But takes more area
- BJT is a current driven device
- BJT takes more power.

where,

MOS:

- slower than BJT
- Takes little area which is suitable for VLSI fabrication.
- consumes less power.

MOS can be fabricated very large scale and it consumes less power that is why one should prefer MOS over BJT.

Ans. to the ques. no. - 03(a)

Inverter ratio (K) for, NMOS inverter with depletion transistor load:

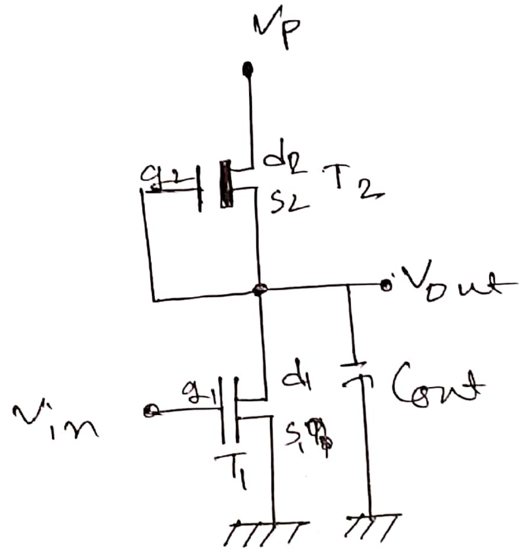


fig: NMOS inverter with depletion NMOS load.

Here, No voltage at g_2 of T_2 so, $V_{g_2} = 0V$, $V_{S_2} = 0V$.

$V_{gs_2} = 0V$,

So, $V_{gs_2} > -4V$ (depletion $V_{tD} = -4V$)

So, T_2 is always on.

Now, when:

$V_{in} = 0V$

T_1 is off; T_2 is on.

So, C_{out} capacitor will be charged by T_2 transistor and $V_{out} = 5V$.

P.T.O.

Case : 2 :

$v_{in} = 5V.$

T_1 & T_2 is on.

So, Cout will dischange through T_1 and v_{out} will be 0V.

Now, for T_1 :

$V_{g_1} = 5V$, $V_{S_1} = 0V$, $V_{d_1} = 0.3V$

So, $V_{gs_1} = V_{g_1} - V_{S1}$

$= 5V$

Here,
$\because V_{d_1} = V_{out} = 0.3 \times V_t$
$= 0.3$

$V_{g_1} = V_{in}$

$V_{S1} = 0V$

$V_{dS1} = V_{d_1} - V_{S1}$

$= 0.3V$

$V_{gs_1} - V_t = (5-1) = 4V$

So $\boxed{V_{ds.} < V_{gs_1} - V_t}$

So, T_1 is in resistive region.

So, $I_{ds_1(res)} = \frac{\epsilon \mu n_1}{D}\left(\frac{W_1}{L_1}\right)\left[(V_{gs_1} - V_t)V_{ds_1} - \frac{V_{ds_1}^2}{2}\right]$

$= 35 \times \frac{W_1}{L_1} \times \left[(5-1)0.3 - \frac{0.3^2}{2}\right]$

$= 40.425 \times \frac{W_1}{L_1}$

For, T_2:

$V_{g_2} = 0V = V_{s2}$ $\therefore$ $V_{gs_2} = V_{g_2} - V_{s2} = 0V$

$V_{tD} = -4V$ [depletion]

$V_{do_2} = V_p = 5V$

$V_{ds_2} = V_{d2} - V_{s2}$

$= 5 - 0.3$

$= 4.7$

$\therefore V_{gs_2} - V_{tD} = 0 - (-4) = 4V$

$\therefore V_{ds_2} > V_{gs_2} - V_{tD}$

So, T_2 is in saturation.

So, $I_{ds_2(sat)} = \frac{\epsilon \mu_{n2}}{D} \left(\frac{W_2}{L_2}\right) \frac{(V_{gs_2} - V_{tD})^2}{2}$

$= 25 \times \frac{16}{2} \times \frac{W_2}{L_2}$

$= 200 \frac{W_2}{L_2}$

$\therefore$ inverter ratio, $K = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = \frac{200 \times I_{ds_1}}{40.425 \times I_{ds_2}}$ $[I_{ds_1} = I_{ds_2}]$

$= 4.95 \approx 5$

(Ans)

Ans. to the ques. no. - 03(b)

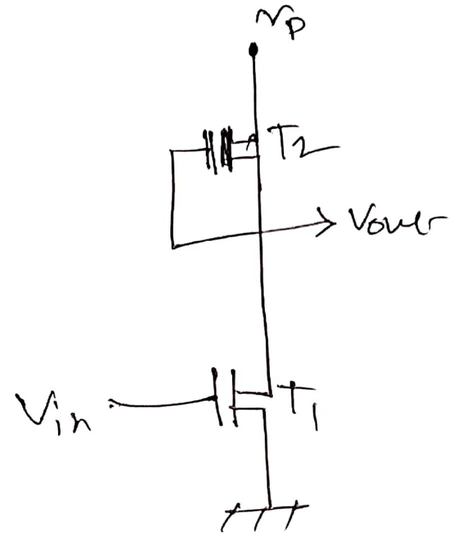


fig: NMOS inverter with depletion

$$R = \frac{\text{pinch off voltage } T_2}{\text{pinch off current of } T_2}$$

$$= \frac{V_{gs} - V_{tD}}{\frac{\epsilon \mu_n}{D} \frac{W_2}{L_2} \times \left[\frac{(V_{gs} - V_{tD})^2}{2}\right]}$$

$$= \frac{0 - (-4)}{25 \times \frac{W_2}{L_2} \times \frac{4^2}{2}}$$

$$\therefore R = \frac{20 K\Omega}{\frac{W_2}{L_2}} \quad \text{---(i)}$$

we know

$$i = \frac{V_p - V_{out}}{R} \quad \text{——(ii)}$$

again,

$$i = C_{out}\frac{dV_{out}}{dt} \quad \text{——(iii)}$$

(ii) & (iii)

$$\frac{V_p - V_{out}}{R} = C_{out}\frac{dV_{out}}{dt}$$

$$\Rightarrow \int \frac{dV_{out}}{V_p - V_{out}} = \frac{dt}{RC_{out}}$$

$$\Rightarrow -\ln(V_p - V_{out}) = \frac{t}{RC_{out}} + \ln x$$

$$\Rightarrow \frac{t}{RC_{out}} = -\ln[x(V_p - V_{out})]$$

$$\Rightarrow e^{-\frac{t}{RC_{out}}} = x(V_p - V_{out}) \quad \text{——(iv)}$$

$t=0$, $V_{out} = V_i$

$$\therefore K = \frac{1}{V_p - V_i}$$

So,

$$e^{-t/RC_{out}} = \frac{1}{V_p - V_i}(V_p - V_{out})$$

$$\Rightarrow V_{out} = V_p - (V_p - V_i)\, e^{-t/RC_{out}} \quad \text{—(v)}$$

$V_i = 1$, $V_{out} = 4.5$ $(5 + 5 \times 10\%)$

So,

$t_r = \cancel{t_1} + t_2$

$\Rightarrow t_r = t_2$ [$\cancel{t_1}$ is less]

$$4.5 = 5 - (5-1)\, e^{-t_2/RC_{out}}$$

$$4\, e^{-t_2/RC_{out}} = 0.5$$

$$\Rightarrow \frac{-t_2}{RC_{out}} = 0.125$$

$\Rightarrow t_2 = 2.08\, RC_{out}$

$$\Rightarrow t_2 = t_r = 2.08 \times \frac{20}{\frac{W_2}{L_2}} \times C_{out} = \frac{42\, C_{out}}{\frac{W_2}{L_2}} \text{ ns}$$

(proved)