

Subject: CSE – 411 VLSI Design

Total: 2.00 hours
Section A : 1.00 hour

Full Marks: 180
Section A : 90

INSTRUCTIONS:

- a. Use **SEPARATE** answer scripts for each section.
- b. **Question – 1 and Question – 4 (Viva Voce)** in **Section A** are compulsory.
- c. Answer any **OTHER ONE** question from this section (**From Q - 2 & Q - 3**).
- d. Figures in the margin indicate full **marks**.
- e. Assume reasonable data if necessary.
- f. **Symbols** used have their usual meanings.

SECTION-A

Question – 1 (Compulsory)

- a. Draw the I-V characteristics curve for a PMOS transistor, having $W=L$, $\epsilon\mu_p/D = 12 \mu_A/V^2$, $V_{tp} = 1V$ 12
 Show the necessary calculations for multiple values of V_{sg} .
- b. What are the advantages of using depletion transistor load instead of enhancement transistor in s MOS inverter? Explain with figure. 12
- c. Why should one prefer MOS over BJT? Show the conduction process of PMOS transistor. 12

Question – 2

- a. Consider a CMOS inverter with a NMOS transistor (T_1) whose aspect ratio $W_1/L_1 = 1$, $\epsilon\mu_n/D = 32 \mu_A/V^2$ and a PMOS transistor (T_2), having aspect ratio of $W_2/L_2 = 2$ and $\epsilon\mu_p/D = 16 \mu_A/V^2$. 16 + 10 = 26
 (i) Draw I vs V_{out} curves of T_1 and T_2
 (ii) Draw the power curve using the curve in (i)
- b. Draw the circuit diagram of non-inverting superbuffer. 10
 What are its main purpose? Explain briefly.

Question – 3

- a. Find out the inverter ratio of NMOS inverter with depletion transistor load, when $V_p = 5V$, $\epsilon\mu_{n1}/D = 35 \mu_A/V^2$ for enhancement NMOS and $\epsilon\mu_{n2}/D = 25 \mu_A/V^2$ for depletion NMOS. 16
- b. Show that the rise time of the NMOS inverters with depletion transistor load is given by 20

$$t_r = \frac{42 C_{out}}{\left(\frac{W_2}{L_2}\right)} ns$$

Why does the actual value rise from the theoretical value mentioned above? Write down the reason with brief explanation.

Question – 4 Viva Voce (Compulsory)

18