



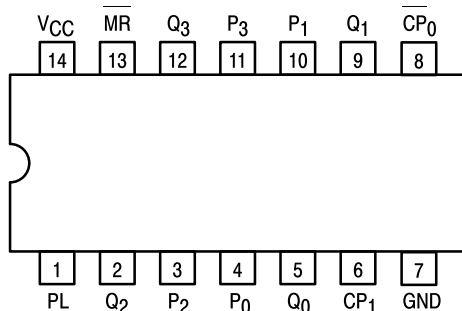
# 4-STAGE PRESETTABLE RIPPLE COUNTERS

The SN54/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset (MR) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (PL) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P<sub>n</sub>) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when PL is LOW and storing the data when PL is HIGH.

- Low Power Consumption — Typically 80 mW
- High Counting Rates — Typically 70 MHz
- Choice of Counting Modes — BCD, Bi-Quinary, Binary
- Asynchronous Presettable
- Asynchronous Master Reset
- Easy Multistage Cascading
- Input Clamp Diodes Limit High Speed Termination Effects

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version  
has the same pinouts  
(Connection Diagram) as  
the Dual In-Line Package.

## PIN NAMES

CP <sub>0</sub>	Clock (Active LOW Going Edge)
CP <sub>1</sub> (LS196)	Input to Divide-by-Two Section
CP <sub>1</sub> (LS197)	Input to Divide-by-Five Section
MR	Master Reset (Active LOW) Input
PL	Parallel Load (Active LOW) Input
P <sub>0</sub> -P <sub>3</sub>	Data Inputs
Q <sub>0</sub> -Q <sub>3</sub>	Outputs (Notes b, c)

## LOADING (Note a)

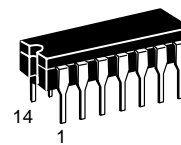
	HIGH	LOW
CP <sub>0</sub>	1.0 U.L.	1.5 U.L.
CP <sub>1</sub> (LS196)	2.0 U.L.	1.75 U.L.
CP <sub>1</sub> (LS197)	1.0 U.L.	0.8 U.L.
MR	1.0 U.L.	0.5 U.L.
PL	0.5 U.L.	0.25 U.L.
P <sub>0</sub> -P <sub>3</sub>	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> -Q <sub>3</sub>	10 U.L.	5 (2.5) U.L.

## NOTES:

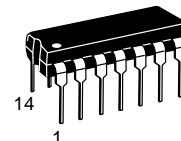
- a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.  
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.  
c. In addition to loading shown, Q<sub>0</sub> can also drive CP<sub>1</sub>.

# SN54/74LS196 SN54/74LS197

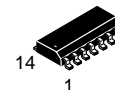
## 4-STAGE PRESETTABLE RIPPLE COUNTERS LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 632-08



**N SUFFIX**  
PLASTIC  
CASE 646-06

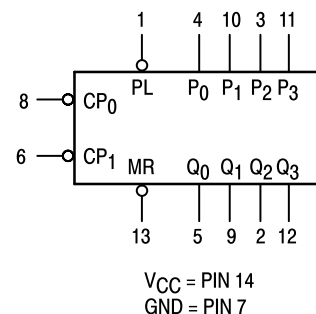


**D SUFFIX**  
SOIC  
CASE 751A-02

## ORDERING INFORMATION

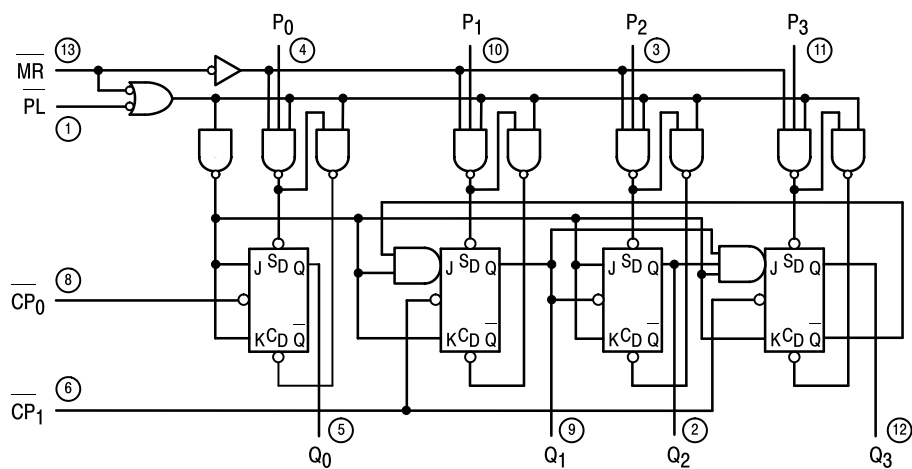
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

## LOGIC SYMBOL

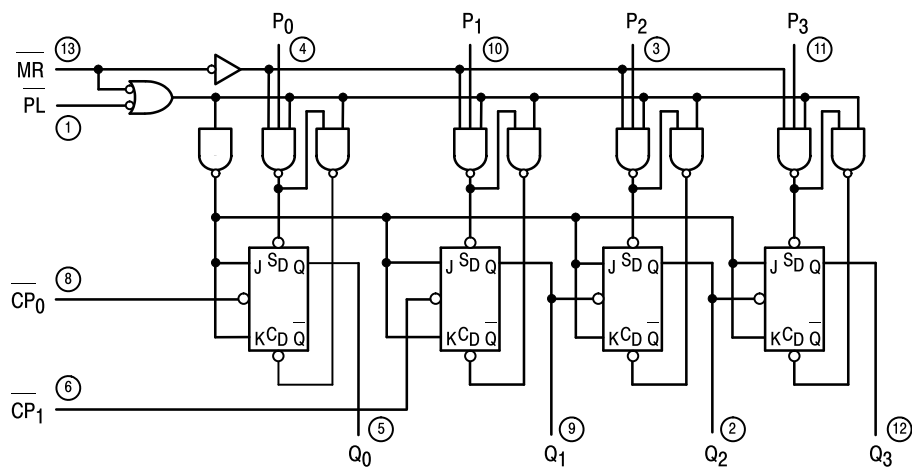


# SN54/74LS196 • SN54/74LS197

## LOGIC DIAGRAM



LS196



LS197

$V_{CC}$  = PIN 14  
 GND = PIN 7  
 ○ = PIN NUMBERS

# SN54/74LS196 • SN54/74LS197

## FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The  $\overline{CP_0}$  input serves the  $Q_0$  flip-flop in both circuit types while the  $CP_1$  input serves the divide-by-five or divide-by-eight section. The  $Q_0$  output is designed and specified to drive the rated fan-out plus the  $CP_1$  input. With the input frequency connected to  $CP_0$  and  $Q_0$  driving  $CP_1$ , the LS197 forms a straightforward module-16 counter, with  $Q_0$  the least significant output and  $Q_3$  the most

significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to  $CP_0$  and with  $Q_0$  driving  $CP_1$ , the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to  $CP_1$  and  $Q_3$  driving  $CP_0$ ,  $Q_0$  becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data ( $P_0-P_3$ ) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the  $P_n$  inputs will be reflected in the outputs.

Figure 2. LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	$Q_3$	$Q_2$	$Q_1$	$Q_0$	COUNT	$Q_0$	$Q_3$	$Q_2$	$Q_1$
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:

1. Signal applied to  $CP_0$ ,  $Q_0$  connected to  $CP_1$ .
2. Signal applied to  $CP_1$ ,  $Q_3$  connected to  $CP_0$ .

MODE SELECT TABLE

INPUTS			RESPONSE
MR	PL	CP	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	$\downarrow$	Count

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

$\downarrow$  = HIGH to Low Clock Transition

# SN54/74LS196 • SN54/74LS197

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			−0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V <sub>IK</sub>	Input Clamp Diode Voltage			−0.65	−1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
		74	2.7	3.5		V	
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
		74		0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current Data, PL MR, CP <sub>0</sub> (LS196) MR, CP <sub>0</sub> , CP <sub>1</sub> (LS197) CP <sub>1</sub> (LS196)				20 40 40 80	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Data, PL MR, CP <sub>0</sub> (LS196) MR, CP <sub>0</sub> , CP <sub>1</sub> (LS197) CP <sub>1</sub> (LS196)				0.1 0.2 0.2 0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Data, PL MR CP <sub>0</sub> CP <sub>1</sub> (LS196) CP <sub>1</sub> (LS197)				−0.4 −0.8 −2.4 −2.8 −1.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)		−20		−100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current				27	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS196 • SN54/74LS197

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	40		30	40		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>0</sub> Input to Q <sub>0</sub> Output		8.0 13	15 20		8.0 14	15 21	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>1</sub> Input to Q <sub>1</sub> Output		16 22	24 33		12 23	19 35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>1</sub> Input to Q <sub>2</sub> Output		38 41	57 62		34 42	51 63	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>1</sub> Input to Q <sub>3</sub> Output		12 30	18 45		55 63	78 95	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Data to Output		20 29	30 44		18 29	27 44	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	PL Input to Any Output		27 30	41 45		26 30	39 45	ns	
t <sub>PHL</sub>	MR Input to Any Output		34	51		34	51	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
t <sub>W</sub>	CP <sub>0</sub> Pulse Width	20			20			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	CP <sub>1</sub> Pulse Width	30			30			ns	
t <sub>W</sub>	PL Pulse Width	20			20			ns	
t <sub>W</sub>	MR Pulse Width	15			15			ns	
t <sub>s</sub>	Data Input Setup Time — HIGH	10			10			ns	
t <sub>s</sub>	Data Input Setup Time — LOW	15			15			ns	
t <sub>h</sub>	Data Hold Time — HIGH	10			10			ns	
t <sub>h</sub>	Data Hold Time — LOW	10			10			ns	
t <sub>rec</sub>	Recovery Time	30			30			ns	

## DEFINITIONS OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

# SN54/74LS196 • SN54/74LS197

## AC WAVEFORMS

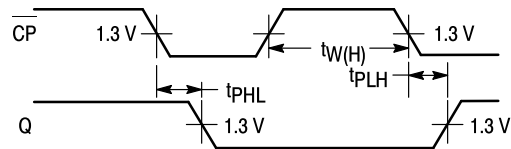
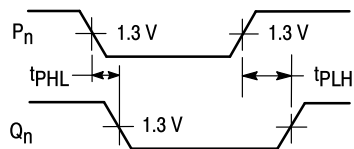


Figure 1



NOTE:  $\overline{PL} = \text{LOW}$

Figure 2

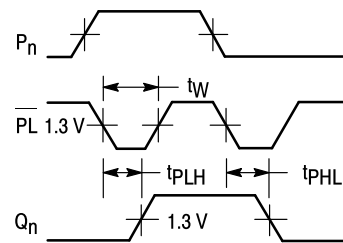


Figure 3

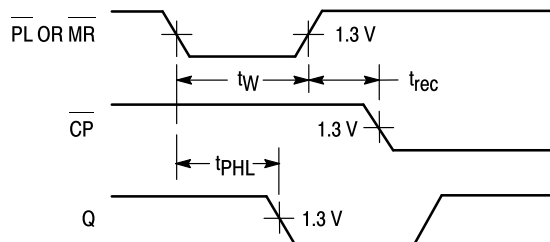
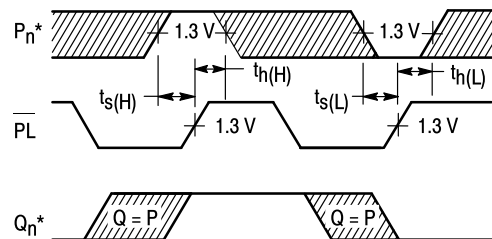


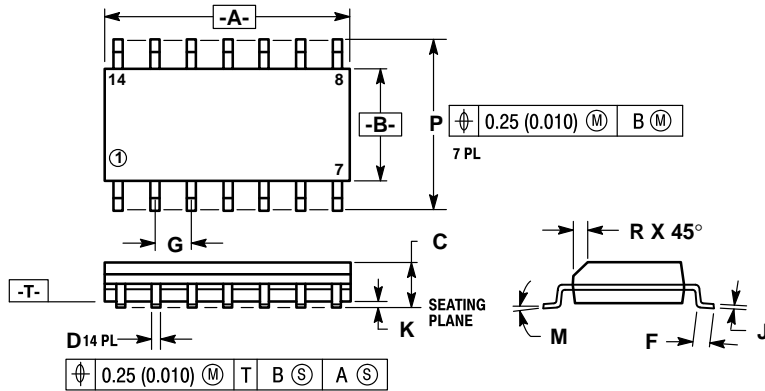
Figure 4



\* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 5

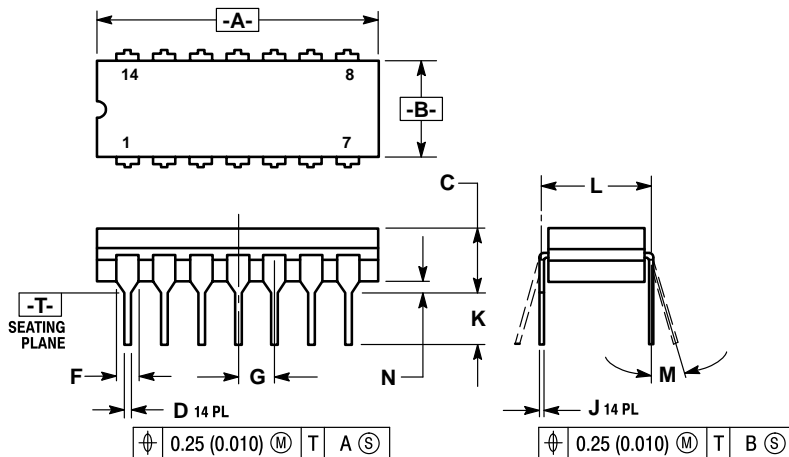
**Case 751A-02 D Suffix**  
**14-Pin Plastic**  
**SO-14**



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
  2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  3. CONTROLLING DIMENSION: MILLIMETER.
  4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

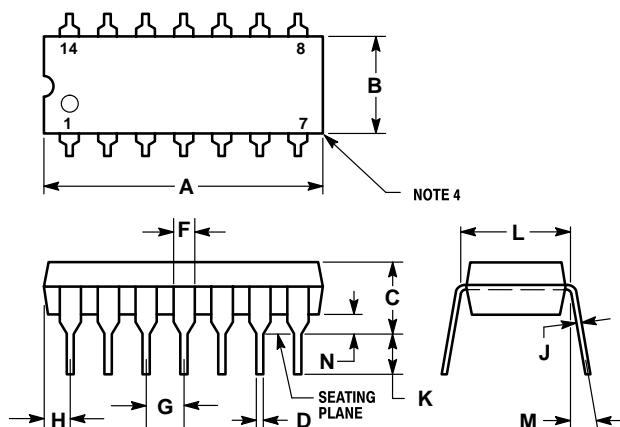
**Case 632-08 J Suffix**  
**14-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

**Case 646-06 N Suffix**  
**14-Pin Plastic**



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.
  5. 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**Literature Distribution Centers:**

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



**MOTOROLA**

