CSE-411

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Ans. to the ques. no. - 01

$Y = AB + C + DE$ So,

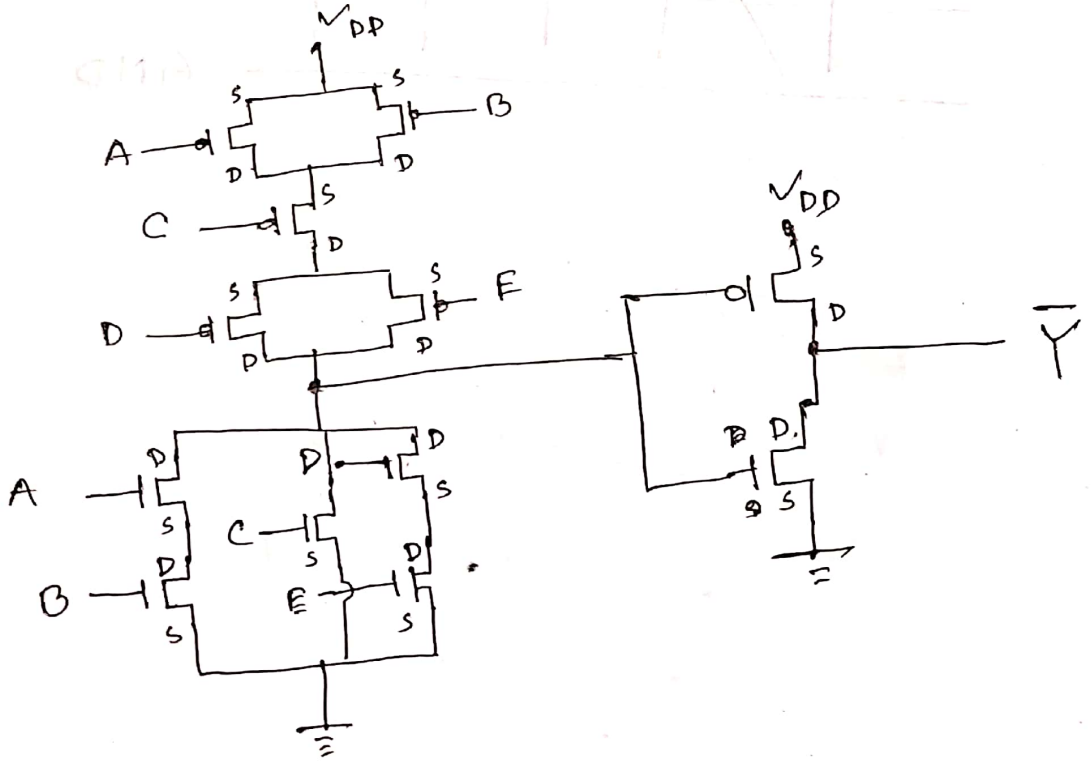
$\overline{A+B}$

$\overline{AB}$

$\overline{A+B} = \overline{A}\,\overline{B}$

$\bar{Y} = \overline{AB + C + DE}$ (since we need complementary)

So, Circuit diagram:



Circuit Diagram

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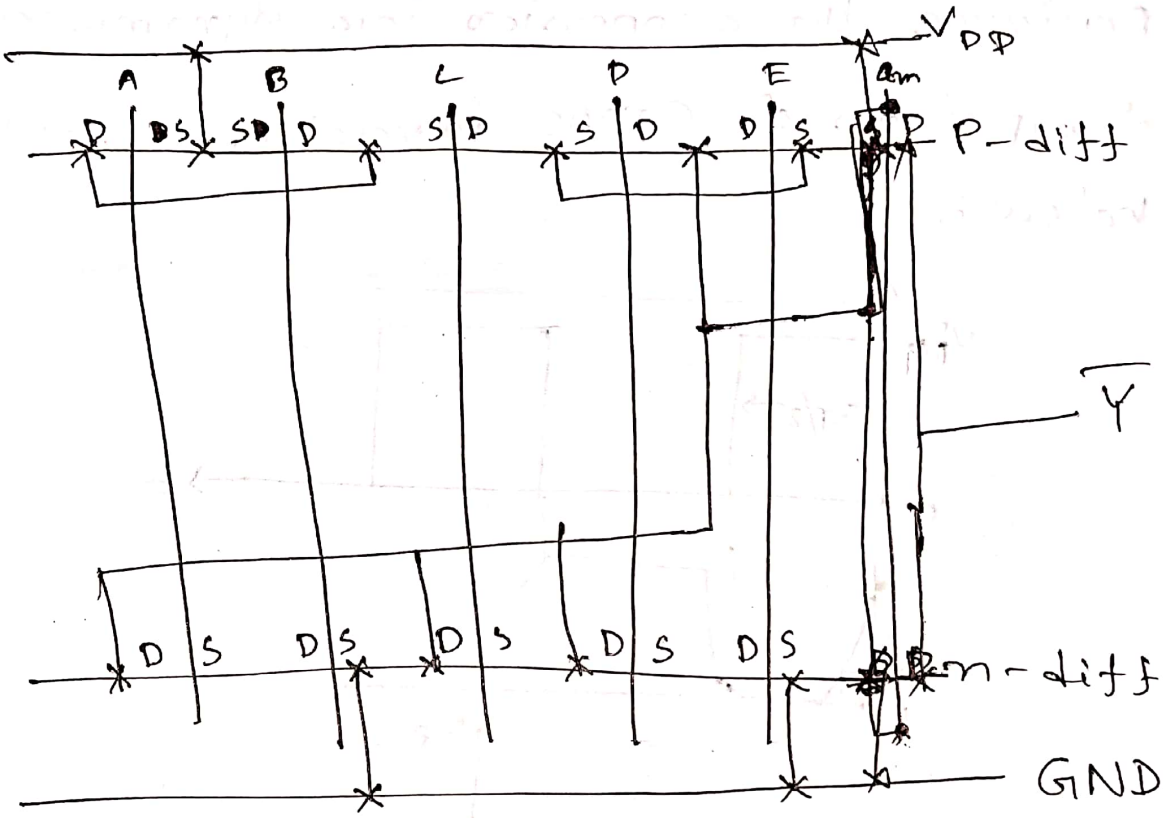
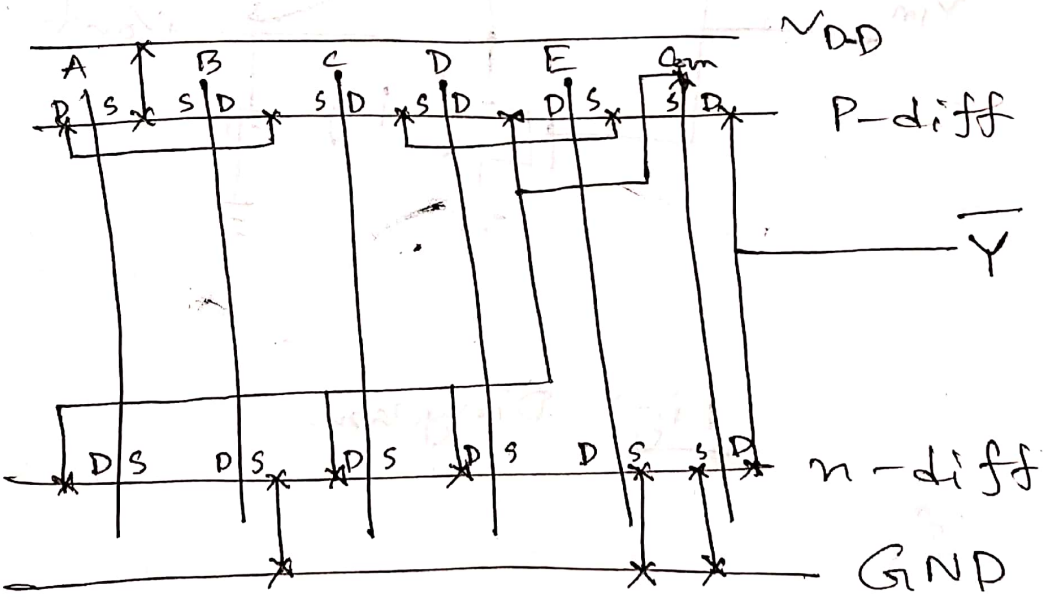
Stick diagram is drawn below:



with cleaning



Stick Diagram final

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Ans. to the ques. no. - 02

Deriving the expression for dynamic power dissipation of CMOS inverters is given below:

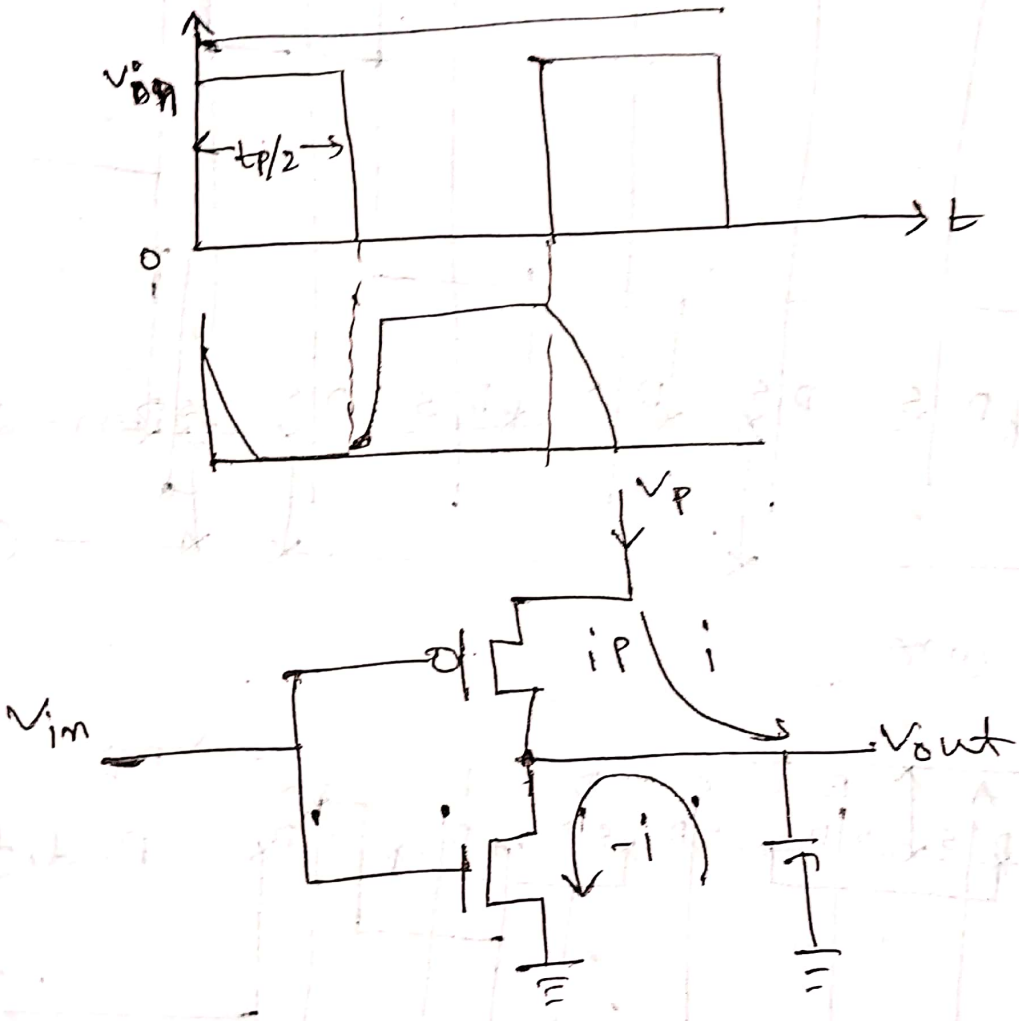

Fig: Diagram.

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Dynamic Power dissipation, P_d

$$P_d = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)\, V_0\, dt + \frac{1}{t_p}\int_{t_p/2}^{t_p} i_p(t)(V_p - V_0)\, dt$$

$$= \frac{C_L}{t_p}\left[\int_{V_p}^{0} -V_0\, dV_0 + \int_0^{V_p}(V_p - V_0)\, dV_0\right] \quad \left[\because i_n(t) = C_L\frac{dV_0}{dt}\right]$$

$$= \frac{C_L}{t_p}\int_0^{V_p}(V_0 + V_p - V_0)\, dV_0$$

$$= \frac{V_p C_L}{t_p}\int_0^{V_p} 1\cdot dV_0$$

$$= \frac{V_p^2 C_L}{t_p}$$

$\therefore P_d = \frac{C_L V_p^2}{t_p}$ and we know, $f_p = \frac{1}{t_p}$ So,

$$\boxed{P_d = f_p C_L V_p^2}$$

So, $P_d \propto f_p, C_L$

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So, P_d is proportional to both frequency and load capacitance.

So,

if both load ~~balance~~ capacitance and frequency are doubled than dynamic power dissipation will be 4X.

So, $P_d' = 4 \times 5mW$

$= 20mW$

Ans

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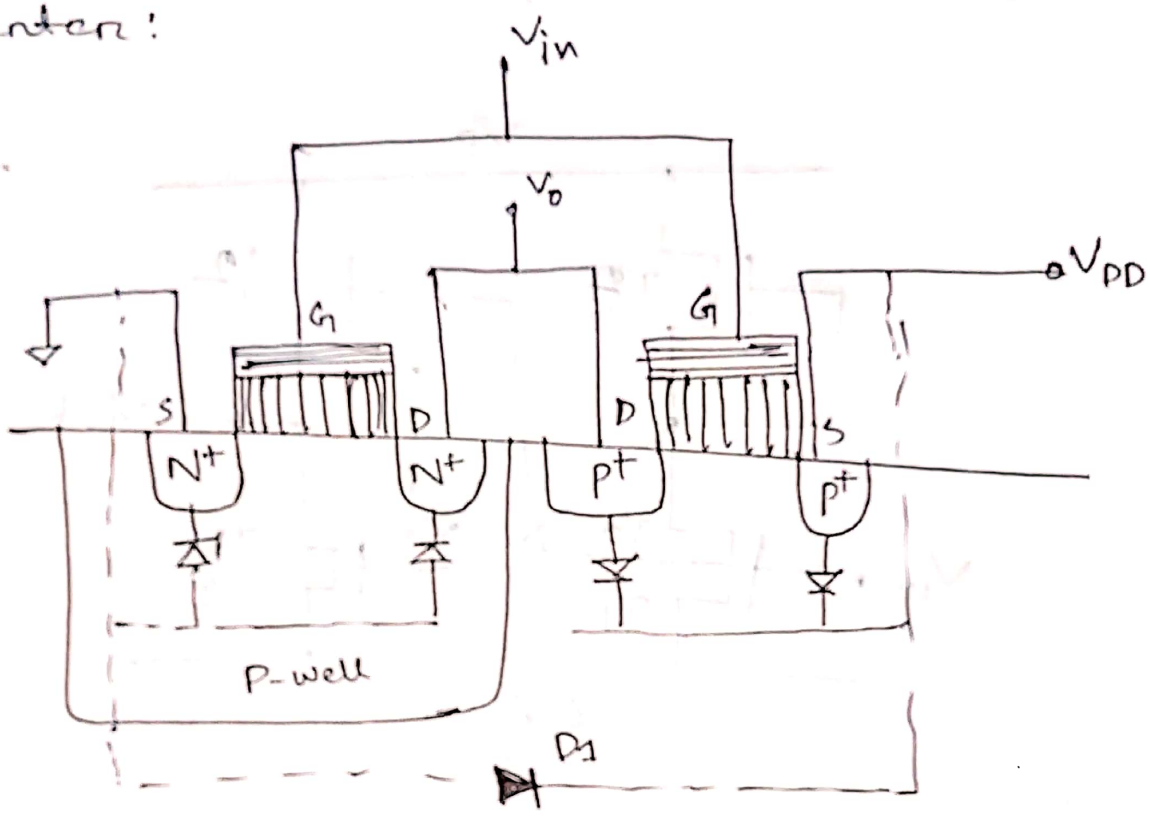
Ans to the ques. no. - 03

Drawing the cross section of a CMOS inverter:



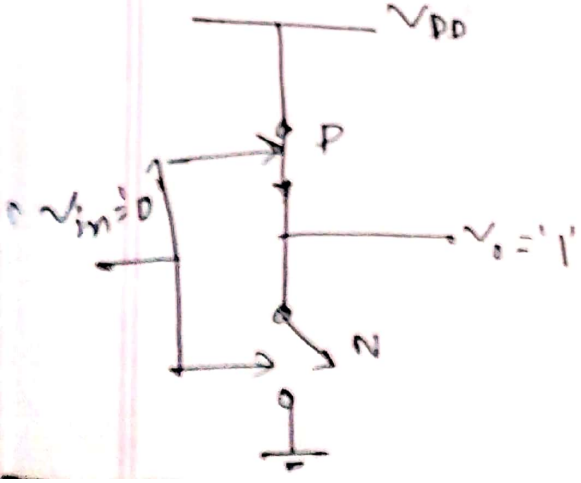


fig: cross section of CMOS inverter.

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Ans. to the ques. no. - 04

Drawing the NMOS inverting super-buffer circuit below:

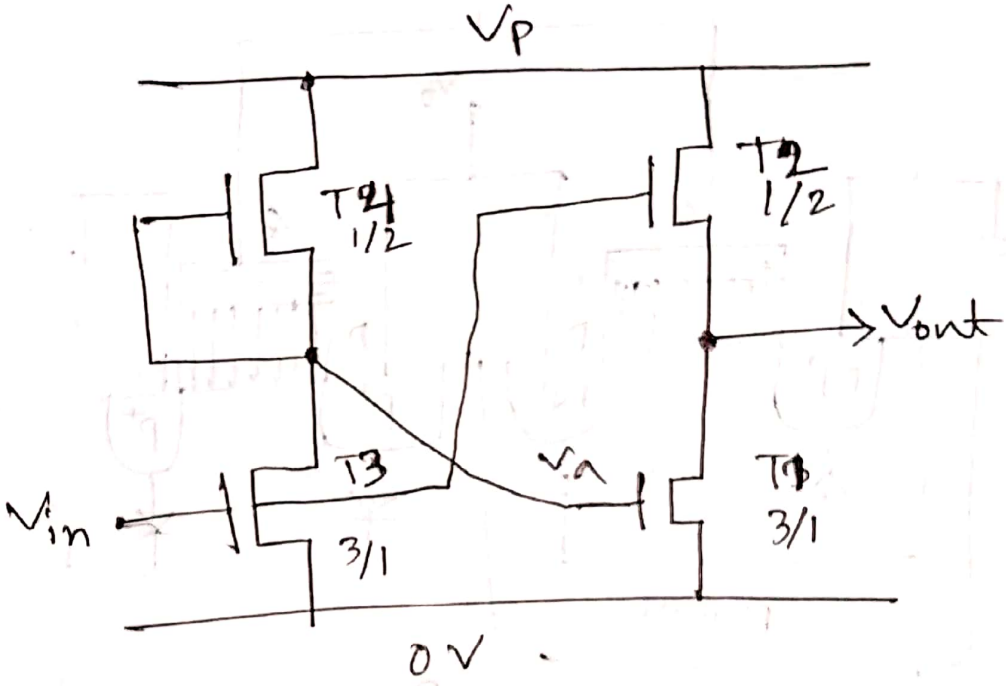

fig: NMOS inverting super buffer