INTEL 8257: PROGRAMMABLE DMA CONTROLLER

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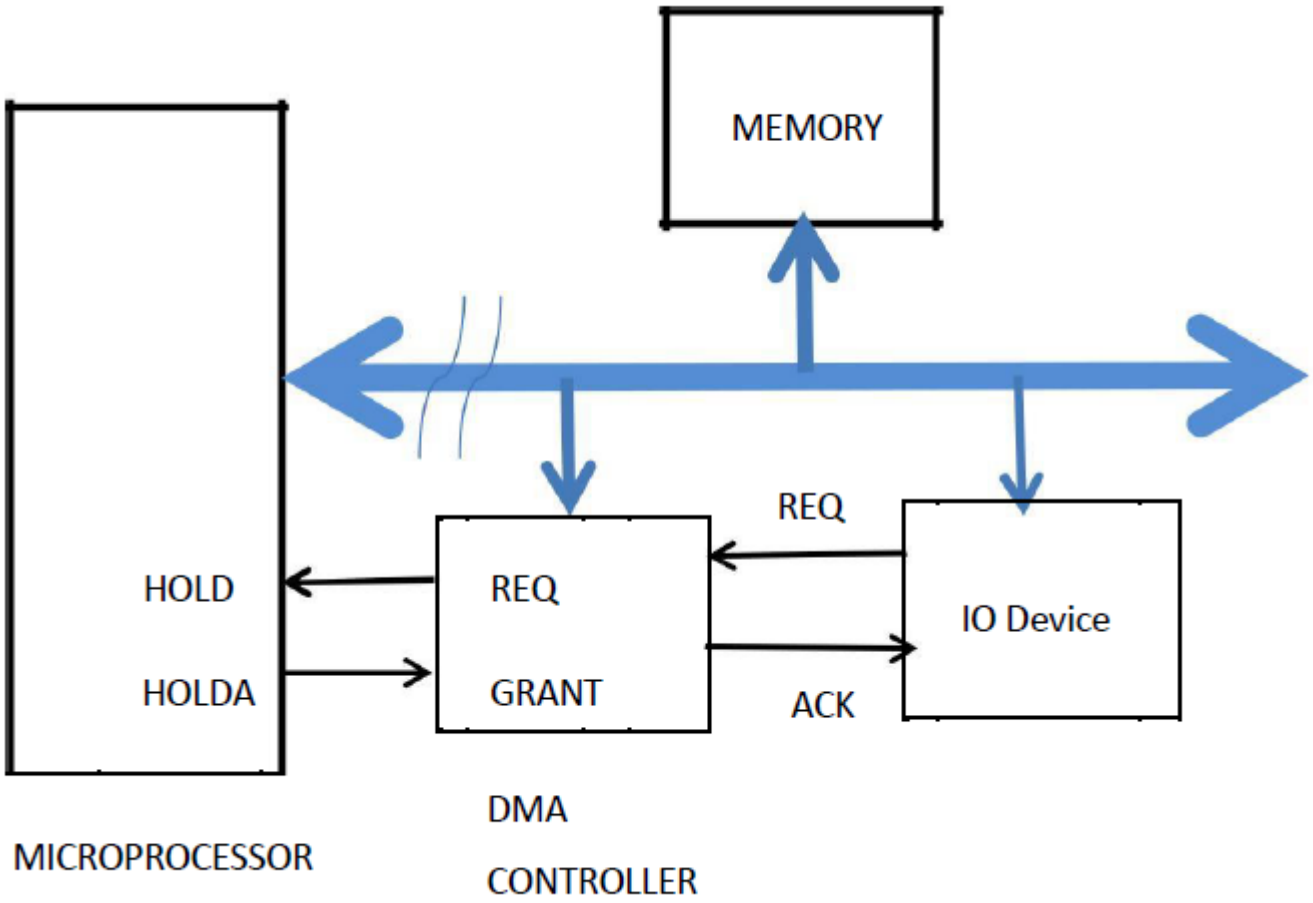
How DMA operations are performed?

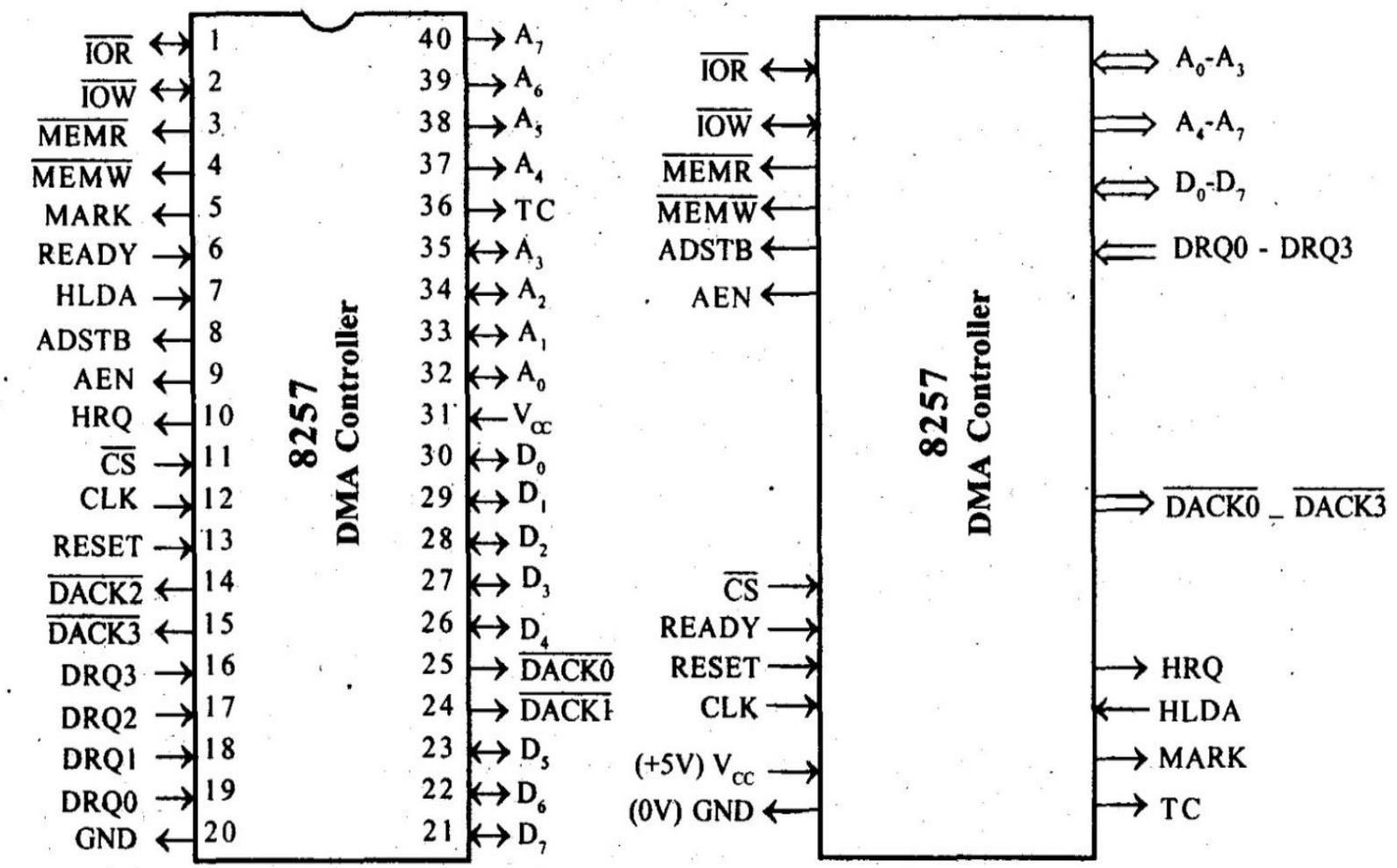
- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.


MEMORY
HOLD
HOLDA
REQ
GRANT
REQ
ACK
IO Device
MICROPROCESSOR
DMA
CONTROLLER

8257 Features

- It has four channels which can be used over four I/O devices.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- It requires a single phase clock.
- Its frequency ranges from 250Hz to 3MHz.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode.**
  - **Master mode** (When Controller has the access on System BUS) and
  - **Slave mode** (When Microprocessor has the access on BUS).
- Has Priority resolver

Pin Diagram


8257
DMA Controller
IOR 1
IOW 2
MEMR 3
MEMW 4
MARK 5
READY 6
HLDA 7
ADSTB 8
AEN 9
HRQ 10
CS 11
CLK 12
RESET 13
DACK2 14
DACK3 15
DRQ3 16
DRQ2 17
DRQ1 18
DRQ0 19
GND 20
40 A7
39 A6
38 A5
37 A4
36 TC
35 A3
34 A2
33 A1
32 A0
31 Vcc
30 D0
29 D1
28 D2
27 D3
26 D4
25 DACK0
24 DACK1
23 D5
22 D6
21 D7
IOR
IOW
MEMR
MEMW
ADSTB
AEN
CS
READY
RESET
CLK
(+5V) Vcc
(0V) GND
A0-A3
A4-A7
D0-D7
DRQ0 - DRQ3
DACK0 _ DACK3
HRQ
HLDA
MARK
TC

8257 Working Principle

- 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU.
- Upon receiving a DMA transfer request from an enabled peripheral, the 8257:
  - Acquires control of the system bus
  - Acknowledges that requesting peripheral which is connected to the highest priority channel
  - Outputs the least significant eight bits of the memory address onto system address lines A0-A7. Outputs the most significant eight bits of the memory address to the I/O port via the data bus.
  - Generates the appropriate memory and I/O read/write control signals that causes the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

8257 Working Principle

- 8257 will retain control of the system bus and repeat the transfer sequence as long as peripheral maintains its DMA request.

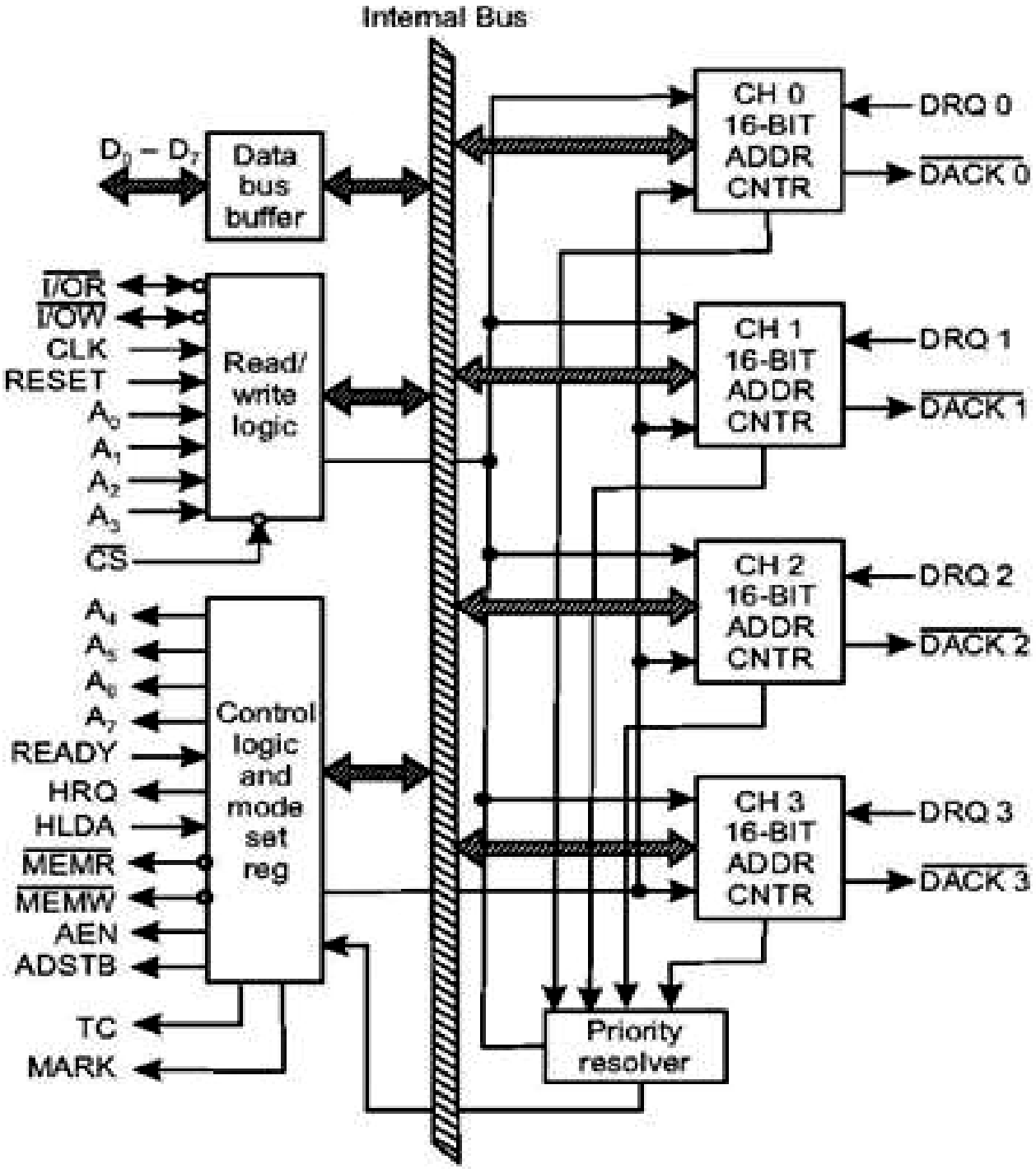
- When the specified number of data bytes have been transferred, the 8257 activates its terminal count and informs CPU that the operation is complete.

8257 Mode of Operation

- DMA Write: Data to be transferred from peripheral to memory (I/O read and Memory Write)
- DMA Read: Data to be transferred from memory to peripheral (I/O write and Memory Read)
- DMA Verify:
  - Same as transferred data but no memory or I/O read/write control signals will be generated,
  - The 8257 will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle.
  - The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) check word.

8257 Block Diagram

- DMA channels
- Data bus buffer
- Read/write logic
- Control logic
- Priority Resolver


Internal Bus
Data bus buffer
$D_0 - D_7$
Read/ write logic
I/OR
I/OW
CLK
RESET
A_0
A_1
A_2
A_3
CS
Control logic and mode set reg
A_4
A_5
A_6
A_7
READY
HRQ
HLDA
MEMR
MEMW
AEN
ADSTB
TC
MARK
CH 0 16-BIT ADDR CNTR
CH 1 16-BIT ADDR CNTR
CH 2 16-BIT ADDR CNTR
CH 3 16-BIT ADDR CNTR
DRQ 0
DRQ 1
DRQ 2
DRQ 3
DACK 0
DACK 1
DACK 2
DACK 3
Priority resolver

DMA Channels

- Intel 8257 has **four** DMA channel (CH0-CH-3).
- Each channel has two registers.
  - Address Register(16 bit)
  - Terminal Count Register(2 bit DMA Operation+14 bit data=16 bit)
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read, write and verify transfer operations.

Signals (DMA Channels)

- DRQ0-DRQ3:
  - These are individual channel request inputs used by the peripheral to obtain DMA cycles
  - If not in rotating priority DRQ0 has the highest priority and DRQ3 has the lowest.

- DACK0-DACK3:
  - DMA Acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle.

Signals (Data Bus Buffer)

- D0-D7
  - These are bi-directional data bas lines.
  - When 8257 is programmed by the CPU(Slave Mode), 8 bits of data for a DMA address register, a terminal count register or the mode set register is received on this lines.
  - When CPU reads a DMA address register, terminal count register or status register, the data is sent to the CPU over the data bus.
  - During DMA cycle (Master Mode), 8257 will output the most significant 8 bits of memory address (from one of the DMA address registers) to the i/o port latch via data bus.

Signals (Read/Write Signals)

- When CPU is programming 8257 (it is in the slave mode)
  - 8257 accepts either $\overline{\text{I/OR}}$ or $\overline{\text{I/OW}}$ signals
  - Decodes the least significant four address bits (A0-A3)
  - Either writes the contents of the data bus into the addressed register (it $\overline{\text{I/OW}}$ is true) or places the contents of the addressed register onto bus (if $\overline{\text{I/OR}}$ is true)
- During DMA cycles (when DMA is the master), it generates I/O read and memory write (DMA write cycle) or I/O write and memory read (DMA read cycle) signals.

Signals (Read/Write Signals)

- $\overline{\text{I/OR}}$:
  - An active-low bi-directional signal
  - In the slave mode, it is an input which allows status register, or the upper/lower byte of address register or terminal count register to be read.
  - In master mode, it is an output which is used to access data from a peripheral during DMA write cycle.

Signals (Read/Write Signals)

- $\overline{\text{I/OW}}$:
  - An active-low bi-directional signal
  - In the slave mode, it is an input which allows contents of data bus to be loaded on 8-bit status register, or the upper/lower byte of address register or terminal count register.
  - In master mode, it is an output which is used to access data from a memory during DMA read cycle.

Signals (Read/Write Signals)

- A0-A3:
  - Bi-directional
  - In slave mode, they are inputs which selects one of the registers to be read or write
  - In the master mode, they are outputs (outputs the least significant four bits of 16 bit memory address)
- A4-A7:
  - Constitutes bits 4 to7 of 16 bit memory address generated by 8257 DMA.

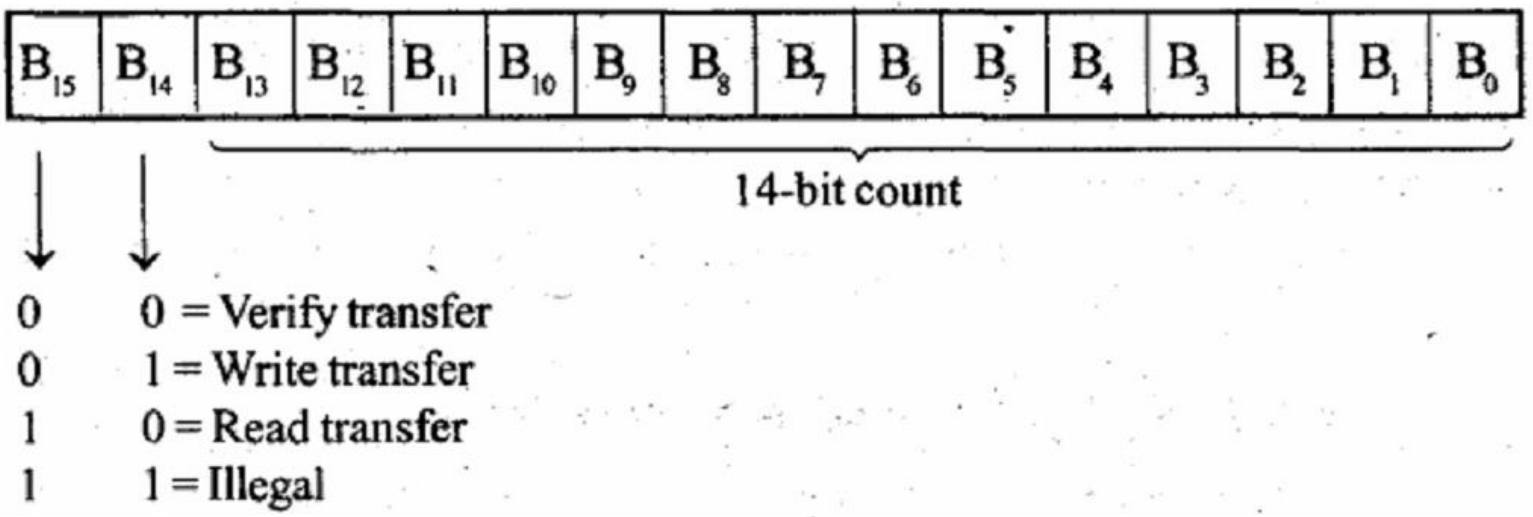
Signals (Control Logic)

- Control logic block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.
- Terminal Count:
  - This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block.
- Mark:
  - This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output.
- $\overline{\text{MEMR}}$:
  - Used to read data from addressed memory location during DMA read cycles
- $\overline{\text{MEMW}}$:
  - Used to write data to addressed memory location during DMA write cycles.

Registers of DMA Channels

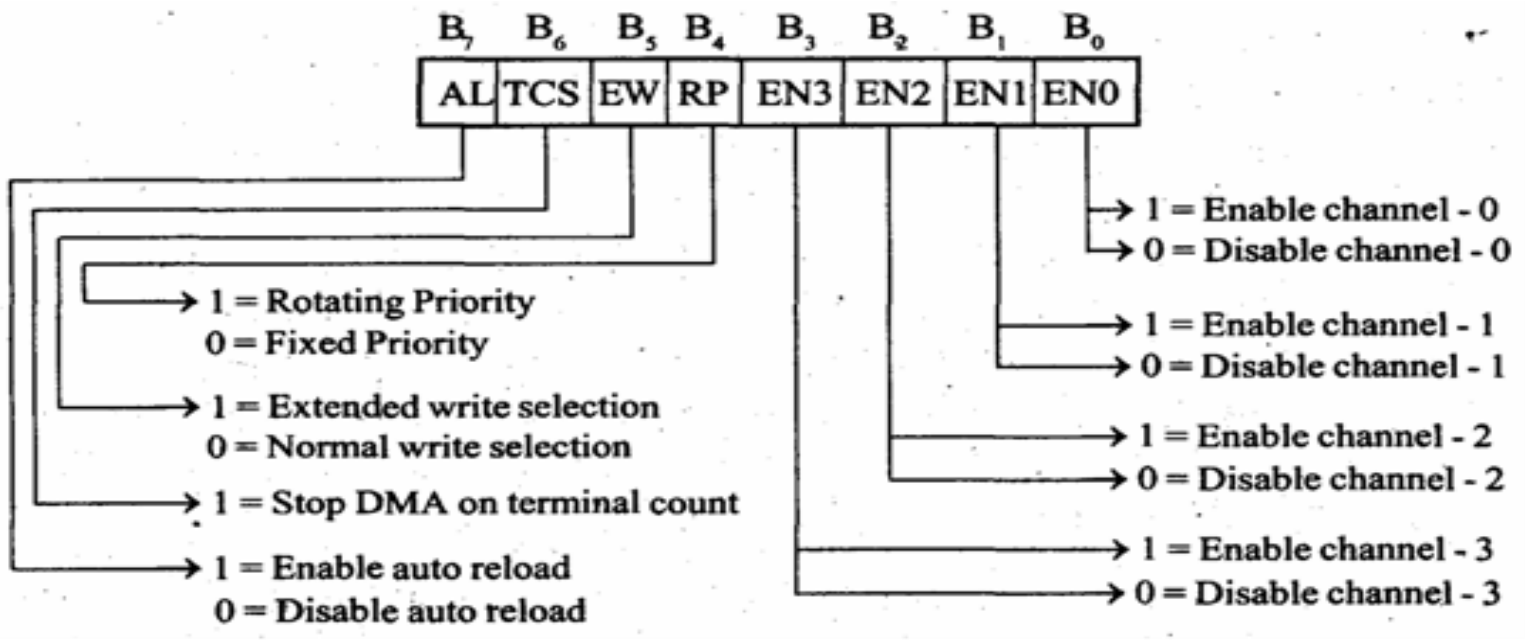
- Two registers: Both registers must be initialized before a channel is enabled.
  - DMA address register
    - It is loaded with the address of the first memory location to be accessed.
  - Terminal count register
    - The value loaded in the lower 14 bits specifies the number of DMA cycles minus one.
    - The most significant two bits specify type of DMA operation for the channel.

Terminal Count Register



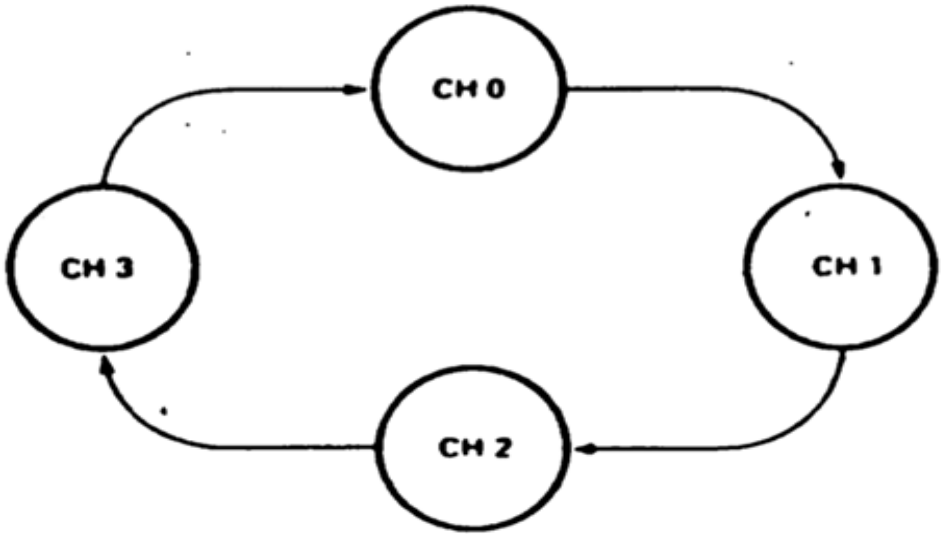
Mode Set Registers

- It is a write only registers.
- It is used to set the operating modes.
- This registers is programmed after initialization of DMA channel.



Mode Set Registers

- Rotating Priority:
  - In rotating Priority, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which has just serviced will have the lowest priority.
- Extended Write:
  - If the extended write bit is set, the duration of both MEMW and I/OW is signals is extended by activating them.
  - If a device cannot be accessed within a specific amount of time, it returns a “not ready” indication to 8257 that causes 8257 to insert one or more wait states.



	CHANNEL → JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
	↕	CH-2	CH-3	CH-0	CH-1
		CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

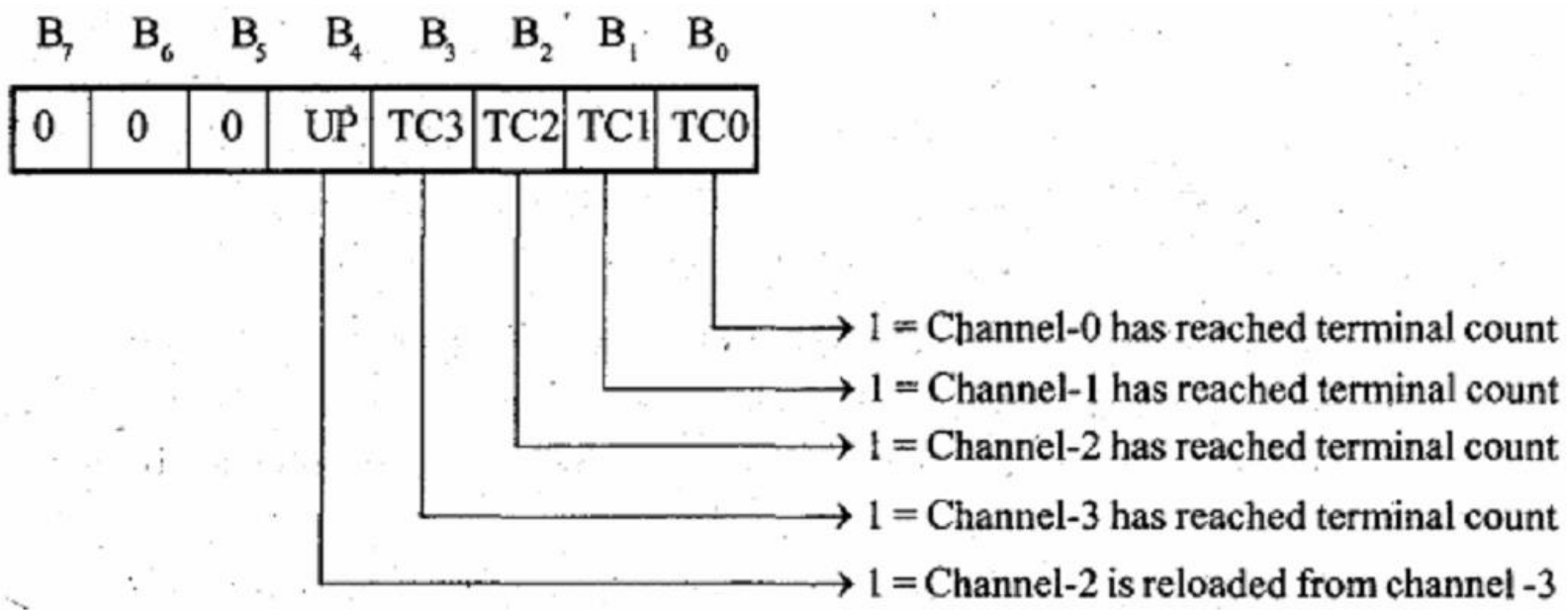
Mode Set Registers

- TC Stop Bit:
  - If the TC stop bit is set a channel is disabled after the terminal count goes reaches its count.
  - Automatically preventing further DMA operations on that channel.
  - The enable bit for that channel has to be re-programmed to begin another DMA operation.

Mode Set Registers

- Auto Load bit:
  - This allows Channel 2 to be used for block chaining operations.
  - Channel 2 registers are initialized as usual for the first data block; Channel 3 registers are used to store re-initialized parameters.
  - When bit B7 is set to one, then the content of Channel-3 count and address registers are loaded in Channel-2 count and address registers respectively whenever the channel-2 reaches terminal count.
  - When this mode is activated the number of channels available for DMA reduces from four to three.
  - TC STOP feature has no effect if auto load bit is set.

Status Register



Status Register

- The bit B0, B1, B2, and B3 of status register indicates the terminal count status of channel-0, 1,2 and 3 respectively. A **1** in these bit positions indicates that the particular channel has reached terminal count.
- These status bits are cleared after a read operation by microprocessor.
- The bit B4 of status register is called update flag and a **1** in this bit position indicates that the channel-2 register has been reloaded from channel-3 registers in the auto load mode of operation.

8257 Register Selection

REGISTER	BYTE	ADDRESS INPUTS				F/L	*BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

DMA Operation

- Single Byte Transfer
- Consecutive Transfer
- Control Override

DMA Operation: Single Byte Transfer

- A single byte transfer is initiated by the I/O device raising the DRQ line of one channel of the 8257. If the channel is enabled, the 8257 will output a HRQ to the CPU.
- The 8257 now waits until a HLDA is received insuring that the system bus is free for its use. Once HLDA is received the DACK line for the requesting channel is activated (LOW).
- The DACK line acts as a chip select for the requesting I/O device. The 8257 then generates the read and write commands and byte transfer occurs between the selected I/O device and memory.
- After the transfer is complete, the DACK line is set HIGH and the HRQ line is set LOW to indicate to the CPU that the bus is now free for use.
- DRQ must remain HIGH until DACK is issued to be recognized and must go LOW of the transfer sequence to prevent another transfer from occurring.

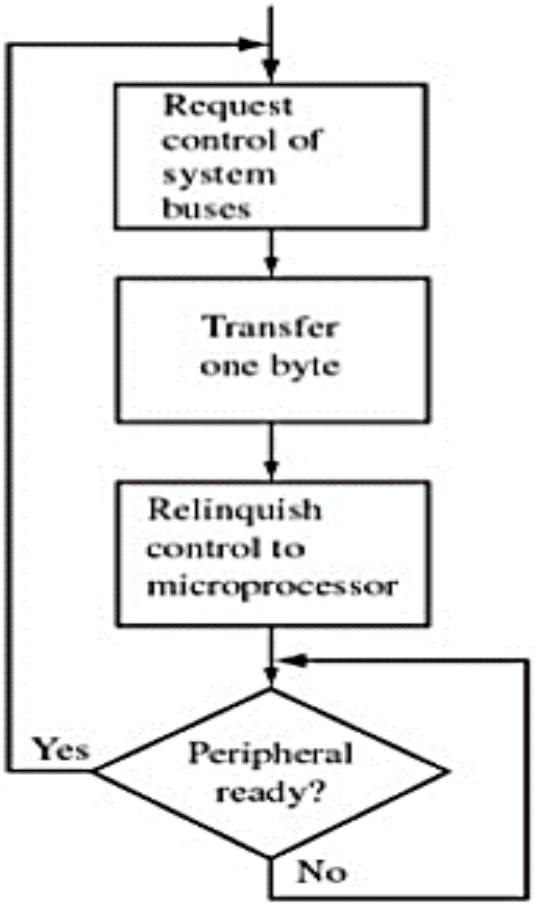
DMA Operation: Consecutive Transfer

- If more than one channel requests service simultaneously, the transfer will occur in the same way a burst does.
- DRQ lines are sampled and the highest priority request is recognized during the next transfer.
- A burst mode transfer in a lower priority channel will be overridden by a higher priority request.
- Once the high priority transfer has completed control will return to the lower priority channel if its DRQ is still active.
- The HRQ line remains active until all DRQ lines go LOW.

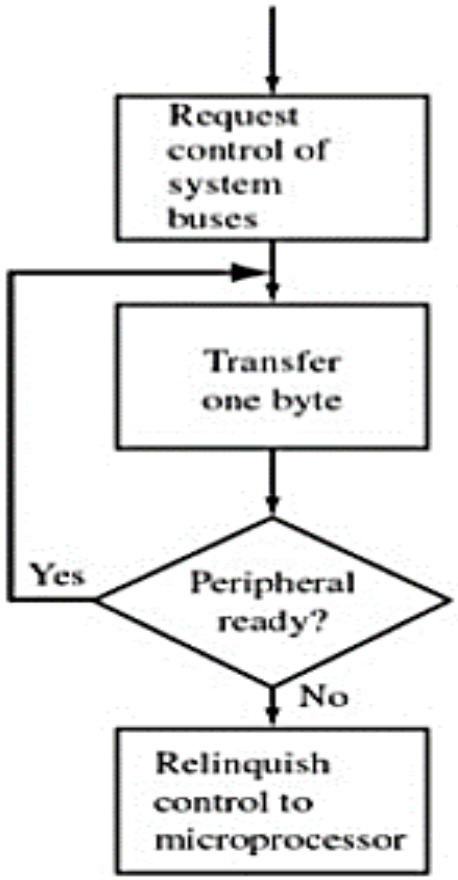
DMA Operation: Control Override

- The continuous DMA transfer mode described earlier can be interrupted by an external device by lowering the HLDA line.
- After each DMA transfer the 8257 samples the HLDA line to insure that it is still active.
- If it is not active, the 8257 completes the current transfer, releases the HRQ line (LOW) and returns to the idle state.
- If DRQ lines are still active the 8257 will raise the HRQ line in the third cycle and proceed normally.

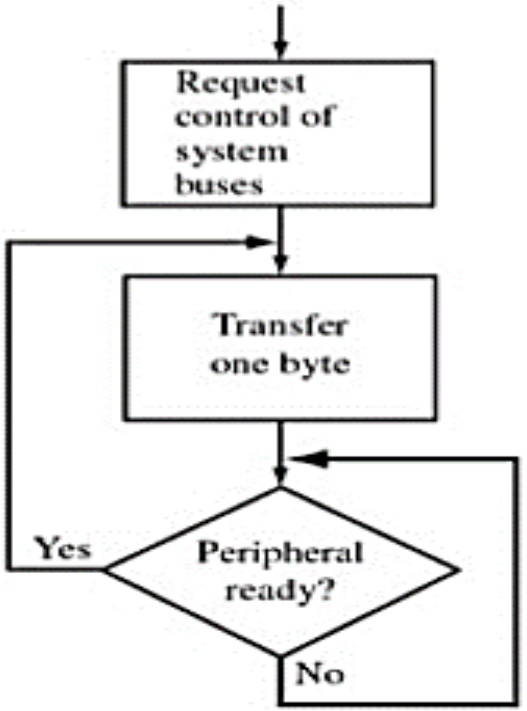
DMA Operation



(a) Single Byte



(b) Consecutive



(c) Control Override

"Be healthy and stay safe"