

## REVISION HISTORY

DATE:	DESCRIPTION	REVISION
Nov. 2009	First Created	1.0
April. 2012	Add an note for the inside 1.2V LDO controller, change R9 from 4.7K to 1K, remove FB2, etc. Update the SPI pull-up resistors value for R1/R2/R3/R4, add transformer recommendation, remove TMII for TMQ part, update strap pins to match current datasheet, remove interrupt indication LED, add JP49 and a table for VDDIO optional.	1.1
Dec., 2012	Add a R60 3.3K pull-down resistor on pin 126 for better using the internal 1.2V LDO controller in case of slow 3.3V power ramp-up.	1.2

Page 1: Revision History

Page 2: KSZ8895 Device

Page 3: Transformer & RJ45 Ports

Page 4: Port 5 SW5-MII, RMII Interface

Page 5: Port 5 PHY P5-MII/RMII Interface

Page 6: Power & Reset

# KSZ8895 Family Reference Design Schematics



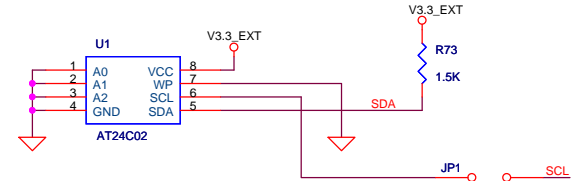
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Title		
KSZ8895 Reference Design		
Size	Document Number	Rev
	Revision History	1.2
Date:	Friday, December 14, 2012	Sheet 1 of 6

Note is for using internal 1.2V LDO controller and MOSFET,

1. Use resistors divider as below for IN\_PWR\_SEL pin 126.
2. R115 100-400ohm is an option only.

By the way, MOSFET 1.2V output Drain pin should close to VDDAR pin 3 without ferrite bead for a good 1.2V LDO feedback path in PCB layout.



The diagram illustrates the SPI interface circuit for the ATmega328P. It features four pull-up resistors, R1, R2, R3, and R4, each with a value of 10K. These resistors are connected to the VDDIO supply and the SPI pins: SPIQ, SCL, SDA, and SPIS-N. The pins are connected to a 4-pin header labeled J11, which is identified as HEADER 4.

VDDIO

R10 4.7K

R11 4.7K

JP6

1

2

3

MDIXDIS

CON3

JP7

1

2

3

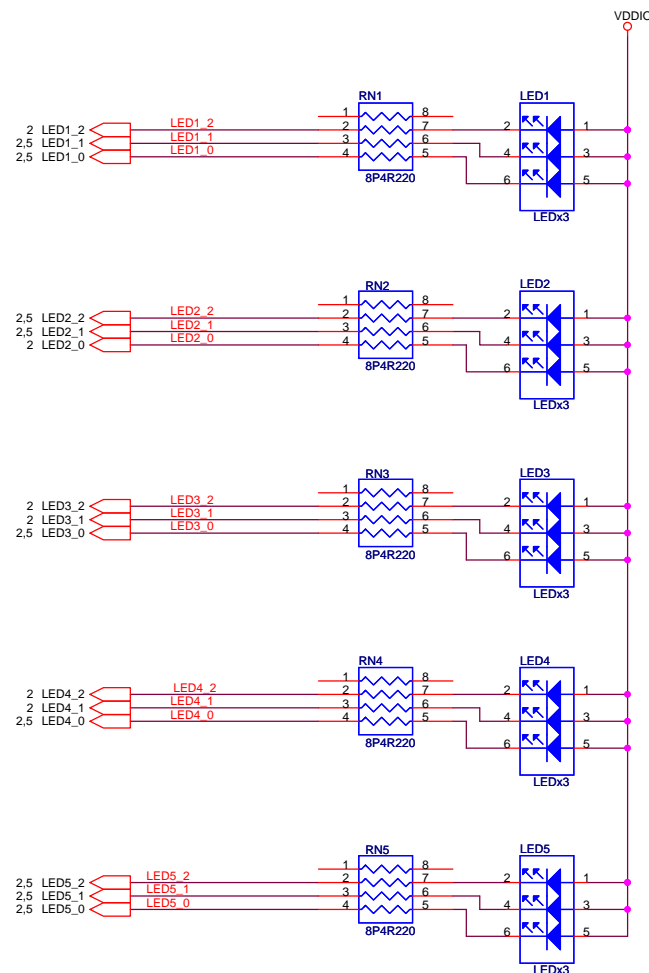
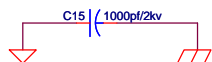
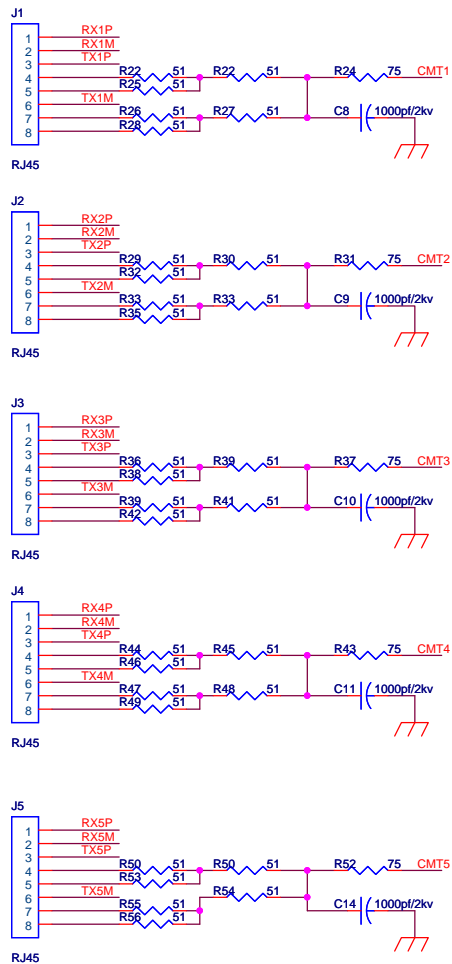
MDI/MDIX

CON3

Figure 10 illustrates the MII configuration for PS0, PS1, SCONF0, and SCONF1. The diagram shows four pins (JP8, JP9, JP10, JP11) connected to a common VDDIO supply line. Each pin is connected to VDDIO through a 4.7K resistor (R13, R14, R15, R16 respectively). The connections are as follows:

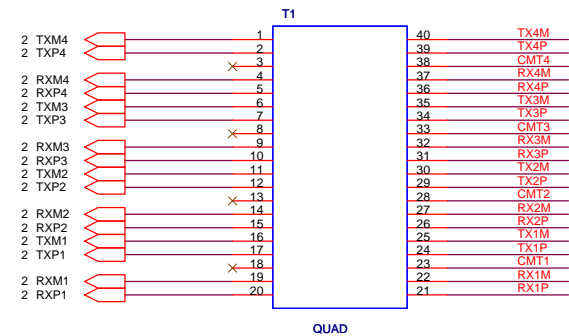
- JP8 (PS0) is connected to VDDIO via R13 (4.7K).
- JP9 (PS1) is connected to VDDIO via R14 (4.7K).
- JP10 (SCONF0) is connected to VDDIO via R15 (4.7K).
- JP11 (SCONF1) is connected to VDDIO via R16 (4.7K).

Note:  
RMII is for KSZ8895RQ only

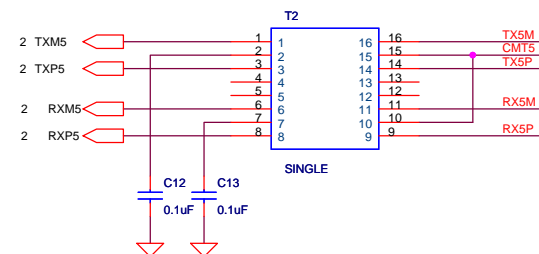


# Note:

1. There are no 50ohm termination resistors and external biasing due to support on-chip termination and internal biasing.
2. Please do not connect the center tap of transformer RX/TX together to an external analog power.



QUAD  
Pulse H1664NL  
YCL PH406082

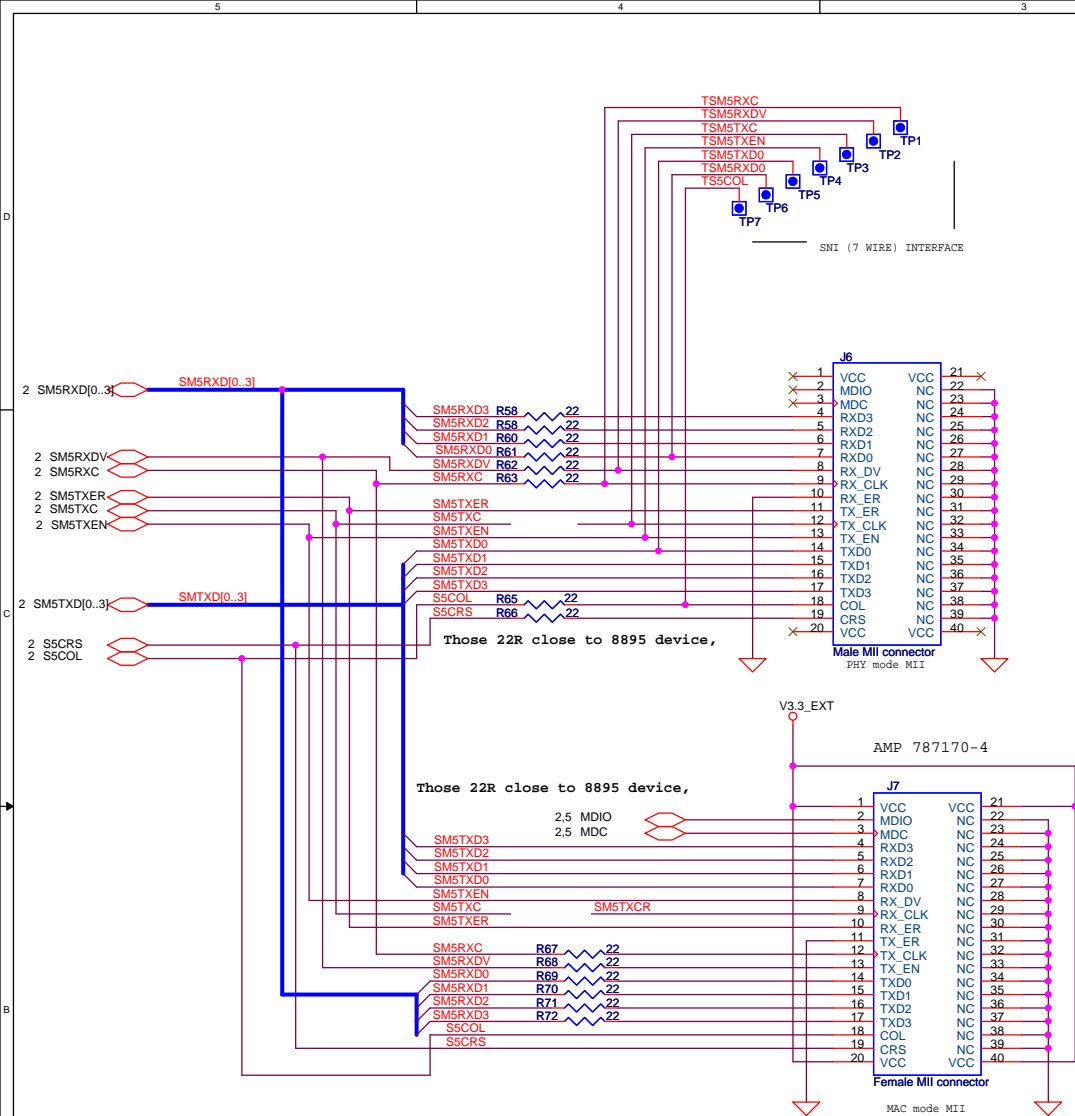


SINGLE  
Pulse H1102  
Bel Fuse S558-5999-U7  
YCL PT163020  
Transpower HB726  
DELTA LF8505  
Datatronic NT79075  
TLA-6T718A

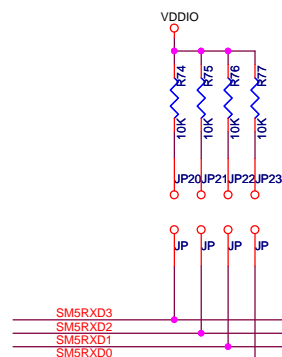


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Title KSZ8895 Reference Design		
Size	Document Number Copper Ports, Transformer and LEDs	Rev 1.2
Date:	Friday, September 07, 2012	Sheet 3 of 6



Port 5:SW5-MII/RMII MAC mode and PHY mode



22R close to 8895 device,

Jumper close to break point,

1-2 Close is RMII w/clock provided,  
The mode can be used to provide  
50MHz to both side of RMII interface  
2-3 Close is SW5-MII mode



22R close to 8895 device,

Jumper close to break point,

1-2 Close is MII mode,  
2-3 Close and 1-2-3 Open are for SW5/P5-RMII  
Detail see the table below

#### Port 5 MAC5 SW5-MII mode (Default):

JP17 Pin2-3 CLOSE, JP18 Pin1-2 CLOSE,

#### Port 5 SW5-RMII (Connection between clock and normal mode):

Clock mode: (board #1)  
Provide RMII Clock

Normal mode: (board #2)  
Receive RMII Clock

Port 5 MAC5 SW5-RMII to PHY  
by J7  
JP17 1-2 CLOSE,  
JP18 1-2-3 OPEN

Port 5 MAC5 SW5-RMII to MAC  
by J6  
JP17 1-2-3 OPEN,  
JP18 2-3 CLOSE.  
Or any single PHY with RMII

Port 5 MAC5 SW5-RMII to MAC  
by J6  
JP17 1-2 CLOSE,  
JP18 1-2-3 OPEN.  
Or any single PHY with RMII

Port 5 MAC5 SW5-RMII to PHY  
by J7  
JP17 2-3 CLOSE,  
JP18 1-2-3 OPEN

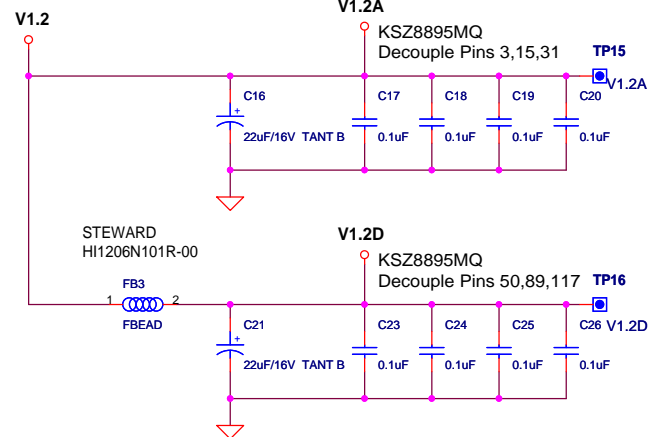
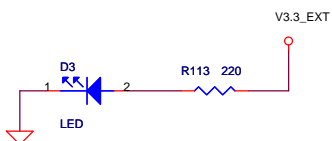
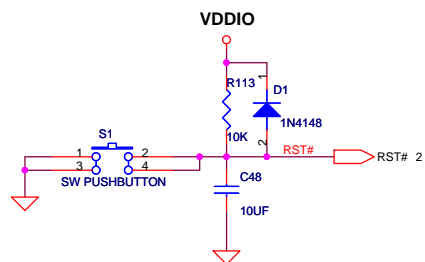
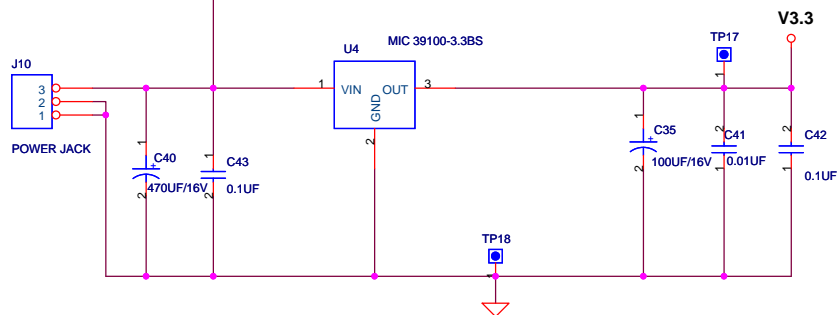
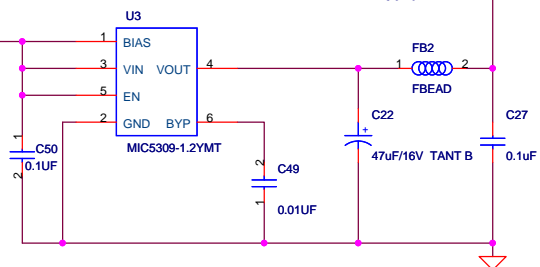
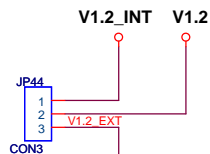
#### Note:

MII interface mode is for KSZ8895MQ  
RMII Interface mode is for KSZ8895RQ

Title		
KSZ8895 Reference Design		
Size	Document Number	Rev
	MII, RMII, SNI	1.2
Date:	Friday, September 07, 2012	Sheet 4 of 6



JP44 1-2 close as default	
1-2 CLOSE	Use internal 1.2V LDO
2-3 CLOSE	Use external 1.2V LDO



JP49 2-3 close as default	
1-2 CLOSE	Other 2.5V or 1.8V
2-3 CLOSE	VDDIO is 3.3V

