```
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t
source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_O0.out
ITLB:
    Load Hits:          220079
    Load Misses:            91
    Load Accesses:      220170
    Load Miss Rate:      0.04%

  Store Hits:               0
  Store Misses:             0
  Store Accesses:           0
  Store Miss Rate:        nan%

  Total Hits:          220079
  Total Misses:            91
  Total Accesses:      220170
  Total Miss Rate:     0.04%
  Flushes:                  0
  Stat Resets:              0

DTLB:
    Load Hits:           86895
    Load Misses:           333
    Load Accesses:       87228
    Load Miss Rate:      0.38%

  Store Hits:               0
  Store Misses:             0
  Store Accesses:           0
  Store Miss Rate:        nan%

  Total Hits:          86895
  Total Misses:          333
  Total Accesses:      87228
  Total Miss Rate:     0.38%
  Flushes:                  0
  Stat Resets:              0

L1 Instruction Cache:
    Load Hits:          218766
    Load Misses:          1404
    Load Accesses:      220170
    Load Miss Rate:      0.64%
```

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 218766
Total Misses: 1404
Total Accesses: 220170
Total Miss Rate: 0.64%
Flushes: 0
Stat Resets: 0

L1 Data Cache:
Load Hits: 59573
Load Misses: 4673
Load Accesses: 64246
Load Miss Rate: 7.27%

Store Hits: 15517
Store Misses: 7465
Store Accesses: 22982
Store Miss Rate: 32.48%

Total Hits: 75090
Total Misses: 12138
Total Accesses: 87228
Total Miss Rate: 13.92%
Flushes: 0
Stat Resets: 0

L2 Unified Cache:
Load Hits: 3142
Load Misses: 2935
Load Accesses: 6077
Load Miss Rate: 48.30%

Store Hits: 4867
Store Misses: 2598
Store Accesses: 7465
Store Miss Rate: 34.80%

Total Hits: 8009
Total Misses: 5533
Total Accesses: 13542

Total Miss Rate: 40.86%
Flushes: 0
Stat Resets: 0

L3 Unified Cache:
Load Hits: 71
Load Misses: 2864
Load Accesses: 2935
Load Miss Rate: 97.58%

Store Hits: 32
Store Misses: 2566
Store Accesses: 2598
Store Miss Rate: 98.77%

Total Hits: 103
Total Misses: 5430
Total Accesses: 5533
Total Miss Rate: 98.14%
Flushes: 0
Stat Resets: 0

段错误 (核心已转储)
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_O1.out
ITLB:
Load Hits: 175166
Load Misses: 90
Load Accesses: 175256
Load Miss Rate: 0.05%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 175166
Total Misses: 90
Total Accesses: 175256
Total Miss Rate: 0.05%
Flushes: 0
Stat Resets: 0

DTLB:

Load Hits: 58281
Load Misses: 340
Load Accesses: 58621
Load Miss Rate: 0.58%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 58281
Total Misses: 340
Total Accesses: 58621
Total Miss Rate: 0.58%
Flushes: 0
Stat Resets: 0

L1 Instruction Cache:
Load Hits: 173862
Load Misses: 1394
Load Accesses: 175256
Load Miss Rate: 0.80%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 173862
Total Misses: 1394
Total Accesses: 175256
Total Miss Rate: 0.80%
Flushes: 0
Stat Resets: 0

L1 Data Cache:
Load Hits: 37102
Load Misses: 4671
Load Accesses: 41773
Load Miss Rate: 11.18%

Store Hits: 9379
Store Misses: 7469
Store Accesses: 16848

Store Miss Rate: 44.33%

Total Hits: 46481
Total Misses: 12140
Total Accesses: 58621
Total Miss Rate: 20.71%
Flushes: 0
Stat Resets: 0

L2 Unified Cache:
Load Hits: 3208
Load Misses: 2857
Load Accesses: 6065
Load Miss Rate: 47.11%

Store Hits: 4903
Store Misses: 2566
Store Accesses: 7469
Store Miss Rate: 34.36%

Total Hits: 8111
Total Misses: 5423
Total Accesses: 13534
Total Miss Rate: 40.07%
Flushes: 0
Stat Resets: 0

L3 Unified Cache:
Load Hits: 1
Load Misses: 2856
Load Accesses: 2857
Load Miss Rate: 99.96%

Store Hits: 0
Store Misses: 2566
Store Accesses: 2566
Store Miss Rate: 100.00%

Total Hits: 1
Total Misses: 5422
Total Accesses: 5423
Total Miss Rate: 99.98%
Flushes: 0
Stat Resets: 0

段错误 (核心已转储)
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_O2.out
ITLB:
    Load Hits: 174453
    Load Misses: 87
    Load Accesses: 174540
    Load Miss Rate: 0.05%

    Store Hits: 0
    Store Misses: 0
    Store Accesses: 0
    Store Miss Rate: nan%

    Total Hits: 174453
    Total Misses: 87
    Total Accesses: 174540
    Total Miss Rate: 0.05%
    Flushes: 0
    Stat Resets: 0

DTLB:
    Load Hits: 57987
    Load Misses: 333
    Load Accesses: 58320
    Load Miss Rate: 0.57%

    Store Hits: 0
    Store Misses: 0
    Store Accesses: 0
    Store Miss Rate: nan%

    Total Hits: 57987
    Total Misses: 333
    Total Accesses: 58320
    Total Miss Rate: 0.57%
    Flushes: 0
    Stat Resets: 0

L1 Instruction Cache:
    Load Hits: 173153
    Load Misses: 1387
    Load Accesses: 174540

Load Miss Rate: 0.79%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 173153
Total Misses: 1387
Total Accesses: 174540
Total Miss Rate: 0.79%
Flushes: 0
Stat Resets: 0

L1 Data Cache:
Load Hits: 36912
Load Misses: 4658
Load Accesses: 41570
Load Miss Rate: 11.21%

Store Hits: 9276
Store Misses: 7474
Store Accesses: 16750
Store Miss Rate: 44.62%

Total Hits: 46188
Total Misses: 12132
Total Accesses: 58320
Total Miss Rate: 20.80%
Flushes: 0
Stat Resets: 0

L2 Unified Cache:
Load Hits: 3157
Load Misses: 2888
Load Accesses: 6045
Load Miss Rate: 47.78%

Store Hits: 4886
Store Misses: 2588
Store Accesses: 7474
Store Miss Rate: 34.63%

Total Hits: 8043

Total Misses: 5476
Total Accesses: 13519
Total Miss Rate: 40.51%
Flushes: 0
Stat Resets: 0

L3 Unified Cache:
Load Hits: 47
Load Misses: 2841
Load Accesses: 2888
Load Miss Rate: 98.37%

Store Hits: 21
Store Misses: 2567
Store Accesses: 2588
Store Miss Rate: 99.19%

Total Hits: 68
Total Misses: 5408
Total Accesses: 5476
Total Miss Rate: 98.76%
Flushes: 0
Stat Resets: 0

段错误 (核心已转储)
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_O3.out
ITLB:
Load Hits: 174456
Load Misses: 87
Load Accesses: 174543
Load Miss Rate: 0.05%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 174456
Total Misses: 87
Total Accesses: 174543
Total Miss Rate: 0.05%
Flushes: 0
Stat Resets: 0

DTLB:

Load Hits:	57985
Load Misses:	337
Load Accesses:	58322
Load Miss Rate:	0.58%
Store Hits:	0
Store Misses:	0
Store Accesses:	0
Store Miss Rate:	nan%
Total Hits:	57985
Total Misses:	337
Total Accesses:	58322
Total Miss Rate:	0.58%
Flushes:	0
Stat Resets:	0

L1 Instruction Cache:

Load Hits:	173157
Load Misses:	1386
Load Accesses:	174543
Load Miss Rate:	0.79%
Store Hits:	0
Store Misses:	0
Store Accesses:	0
Store Miss Rate:	nan%
Total Hits:	173157
Total Misses:	1386
Total Accesses:	174543
Total Miss Rate:	0.79%
Flushes:	0
Stat Resets:	0

L1 Data Cache:

Load Hits:	36915
Load Misses:	4655
Load Accesses:	41570
Load Miss Rate:	11.20%
Store Hits:	9290

Store Misses: 7462
Store Accesses: 16752
Store Miss Rate: 44.54%

Total Hits: 46205
Total Misses: 12117
Total Accesses: 58322
Total Miss Rate: 20.78%
Flushes: 0
Stat Resets: 0

L2 Unified Cache:
Load Hits: 3199
Load Misses: 2842
Load Accesses: 6041
Load Miss Rate: 47.05%

Store Hits: 4896
Store Misses: 2566
Store Accesses: 7462
Store Miss Rate: 34.39%

Total Hits: 8095
Total Misses: 5408
Total Accesses: 13503
Total Miss Rate: 40.05%
Flushes: 0
Stat Resets: 0

L3 Unified Cache:
Load Hits: 0
Load Misses: 2842
Load Accesses: 2842
Load Miss Rate: 100.00%

Store Hits: 0
Store Misses: 2566
Store Accesses: 2566
Store Miss Rate: 100.00%

Total Hits: 0
Total Misses: 5408
Total Accesses: 5408
Total Miss Rate: 100.00%

Flushes: 0
Stat Resets: 0

段错误 (核心已转储)
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_OS.out
../problem3/sim_OS.out : No such file or directory
liuyu@LIUYU:~/study/0architecture/homework1/pin311$ ./pin -t source/tools/Memory/obj-intel64/allcache.so -- ../problem3/sim_Os.out
ITLB:
Load Hits: 179257
Load Misses: 90
Load Accesses: 179347
Load Miss Rate: 0.05%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 179257
Total Misses: 90
Total Accesses: 179347
Total Miss Rate: 0.05%
Flushes: 0
Stat Resets: 0

DTLB:
Load Hits: 58285
Load Misses: 336
Load Accesses: 58621
Load Miss Rate: 0.57%

Store Hits: 0
Store Misses: 0
Store Accesses: 0
Store Miss Rate: nan%

Total Hits: 58285
Total Misses: 336
Total Accesses: 58621
Total Miss Rate: 0.57%
Flushes: 0
Stat Resets: 0

L1 Instruction Cache:

Load Hits:	177951
Load Misses:	1396
Load Accesses:	179347
Load Miss Rate:	0.78%
Store Hits:	0
Store Misses:	0
Store Accesses:	0
Store Miss Rate:	nan%
Total Hits:	177951
Total Misses:	1396
Total Accesses:	179347
Total Miss Rate:	0.78%
Flushes:	0
Stat Resets:	0

L1 Data Cache:

Load Hits:	37104
Load Misses:	4669
Load Accesses:	41773
Load Miss Rate:	11.18%
Store Hits:	9370
Store Misses:	7478
Store Accesses:	16848
Store Miss Rate:	44.39%
Total Hits:	46474
Total Misses:	12147
Total Accesses:	58621
Total Miss Rate:	20.72%
Flushes:	0
Stat Resets:	0

L2 Unified Cache:

Load Hits:	3185
Load Misses:	2880
Load Accesses:	6065
Load Miss Rate:	47.49%
Store Hits:	4912

Store Misses: 2566
Store Accesses: 7478
Store Miss Rate: 34.31%

Total Hits: 8097
Total Misses: 5446
Total Accesses: 13543
Total Miss Rate: 40.21%
Flushes: 0
Stat Resets: 0

L3 Unified Cache:
Load Hits: 24
Load Misses: 2856
Load Accesses: 2880
Load Miss Rate: 99.17%

Store Hits: 0
Store Misses: 2566
Store Accesses: 2566
Store Miss Rate: 100.00%

Total Hits: 24
Total Misses: 5422
Total Accesses: 5446
Total Miss Rate: 99.56%
Flushes: 0
Stat Resets: 0

段错误 (核心已转储)
liuyu@LIUYU:~/study/0architecture/homework1/pin311$