

**Colum major:**

[yliu79@lws5047 Memory]\$ .../.../.../pin -t obj-intel64/allcache.so - .../.../.../loop\_col.out

ITLB:

Load Hits: 2000158059

Load Misses: 45

Load Accesses: 2000158104

Load Miss Rate: 0.00%

Store Hits: 0

Store Misses: 0

Store Accesses: 0

Store Miss Rate: nan%

Total Hits: 2000158059

Total Misses: 45

Total Accesses: 2000158104

Total Miss Rate: 0.00%

Flushes: 0

Stat Resets: 0

DTLB:

Load Hits: 996960171

Load Misses: 103125175

Load Accesses: 1100085346

Load Miss Rate: 9.37%

Store Hits: 0

Store Misses: 0

Store Accesses: 0

Store Miss Rate: nan%

Total Hits: 996960171

Total Misses: 103125175

Total Accesses: 1100085346

Total Miss Rate: 9.37%

Flushes: 0

Stat Resets: 0

L1 Instruction Cache:

Load Hits: 2000156973

Load Misses: 1131

Load Accesses: 2000158104

Load Miss Rate: 0.00%

Store Hits: 0  
Store Misses: 0  
Store Accesses: 0  
Store Miss Rate: nan%

Total Hits: 2000156973  
Total Misses: 1131  
Total Accesses: 2000158104  
Total Miss Rate: 0.00%  
Flushes: 0  
Stat Resets: 0

L1 Data Cache:  
Load Hits: 799953188  
Load Misses: 100099886  
Load Accesses: 900053074  
Load Miss Rate: 11.12%

Store Hits: 200027751  
Store Misses: 4521  
Store Accesses: 200032272  
Store Miss Rate: 0.00%

Total Hits: 999980939  
Total Misses: 100104407  
Total Accesses: 1100085346  
Total Miss Rate: 9.10%  
Flushes: 0  
Stat Resets: 0

L2 Unified Cache:  
Load Hits: 93836017  
Load Misses: 6265000  
Load Accesses: 100101017  
Load Miss Rate: 6.26%

Store Hits: 4045  
Store Misses: 476  
Store Accesses: 4521  
Store Miss Rate: 10.53%

Total Hits: 93840062  
Total Misses: 6265476  
Total Accesses: 100105538

Total Miss Rate: 6.26%

Flushes: 0

Stat Resets: 0

L3 Unified Cache:

Load Hits: 2846

Load Misses: 6262154

Load Accesses: 6265000

Load Miss Rate: 99.95%

Store Hits: 0

Store Misses: 476

Store Accesses: 476

Store Miss Rate: 100.00%

Total Hits: 2846

Total Misses: 6262630

Total Accesses: 6265476

Total Miss Rate: 99.95%

Flushes: 0

Stat Resets: 0

### **Row major:**

[yliu79@lws5047 Memory]\$ ../.../pin -t obj-intel64/allcache.so - ../.../loop\_row.out

ITLB:

Load Hits: 2000158059

Load Misses: 45

Load Accesses: 2000158104

Load Miss Rate: 0.00%

Store Hits: 0

Store Misses: 0

Store Accesses: 0

Store Miss Rate: nan%

Total Hits: 2000158059

Total Misses: 45

Total Accesses: 2000158104

Total Miss Rate: 0.00%

Flushes: 0

Stat Resets: 0

DTLB:

Load Hits: 1099984466

Load Misses: 100880  
Load Accesses: 1100085346  
Load Miss Rate: 0.01%

Store Hits: 0  
Store Misses: 0  
Store Accesses: 0  
Store Miss Rate: nan%

Total Hits: 1099984466  
Total Misses: 100880  
Total Accesses: 1100085346  
Total Miss Rate: 0.01%  
Flushes: 0  
Stat Resets: 0

L1 Instruction Cache:  
Load Hits: 2000156974  
Load Misses: 1130  
Load Accesses: 2000158104  
Load Miss Rate: 0.00%

Store Hits: 0  
Store Misses: 0  
Store Accesses: 0  
Store Miss Rate: nan%

Total Hits: 2000156974  
Total Misses: 1130  
Total Accesses: 2000158104  
Total Miss Rate: 0.00%  
Flushes: 0  
Stat Resets: 0

L1 Data Cache:  
Load Hits: 887538637  
Load Misses: 12514437  
Load Accesses: 900053074  
Load Miss Rate: 1.39%

Store Hits: 200027750  
Store Misses: 4522  
Store Accesses: 200032272  
Store Miss Rate: 0.00%

Total Hits: 1087566387  
Total Misses: 12518959  
Total Accesses: 1100085346  
Total Miss Rate: 1.14%  
Flushes: 0  
Stat Resets: 0

L2 Unified Cache:  
Load Hits: 6263610  
Load Misses: 6251957  
Load Accesses: 12515567  
Load Miss Rate: 49.95%

Store Hits: 4050  
Store Misses: 472  
Store Accesses: 4522  
Store Miss Rate: 10.44%

Total Hits: 6267660  
Total Misses: 6252429  
Total Accesses: 12520089  
Total Miss Rate: 49.94%  
Flushes: 0  
Stat Resets: 0

L3 Unified Cache:  
Load Hits: 184  
Load Misses: 6251773  
Load Accesses: 6251957  
Load Miss Rate: 100.00%

Store Hits: 0  
Store Misses: 472  
Store Accesses: 472  
Store Miss Rate: 100.00%

Total Hits: 184  
Total Misses: 6252245  
Total Accesses: 6252429  
Total Miss Rate: 100.00%  
Flushes: 0  
Stat Resets: 0