EE 394J: 11 - Advanced Topics in Power Electronics

Project 1: Boost power factor correction (PFC) rectifier

Soham Roy (sr46579)

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Academic Integrity Statement: Please note that it is an individual project. The design and reports represent the student's own original work. Absolutely no sharing of schematics, designs, plots and write-ups was done. If found in violation of this policy, the student will be reported to the UT Austin Office of the Dean of Students, with repercussions including placement on academic probation and grade penalties including but not limited to receiving a zero on the design project.

Soham Roy

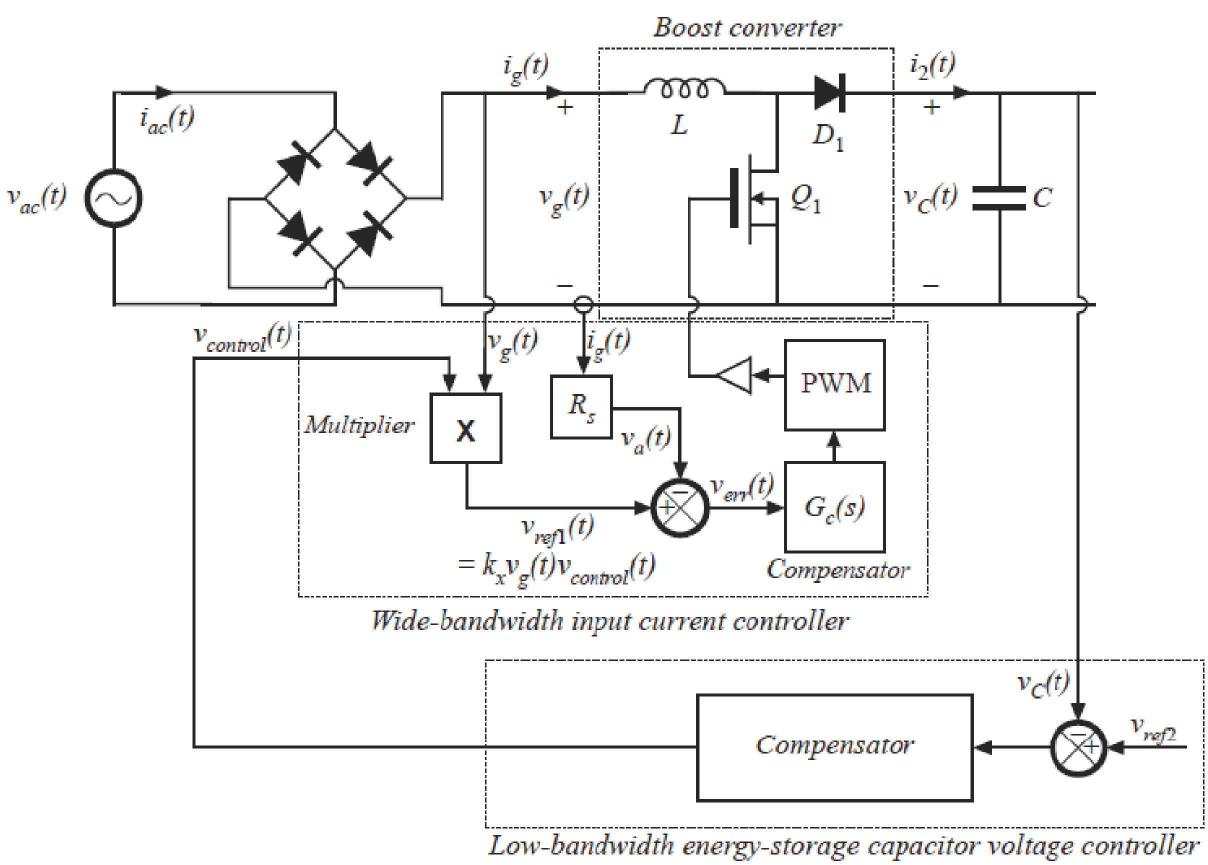
1. **Executive Summary:** This project involves the design of a boost power factor correction (PFC) rectifier based on a peak current mode controller (Current Programmed Mode or CPM) and an average current mode controller. Selection of appropriate switches and diodes to be used in the circuit is done based on the requirements of efficiency and current/voltage ratings. In general, average current mode control is better than CPM in terms of noise immunity and can even be used in a wide range of non-ideal conditions (current with significant ripple, pulsating current and DCM) [5]. The controller in a PFC rectifier varies the duty cycle as necessary to make the ac input current $i_{ac}(t)$ proportional to the ac voltage $v_{ac}(t)$. This topology gives low harmonic content (THD) in the ac input current at close to unity power factor. Such a 6.6 kW boost PFC can be used in the on-board charger for electric vehicles.

2. **Compliance Table (Final design of average current mode controller):**

	Specifications	**Simulated nominal performance**
Full load Output power	6.6 kW	6.6 kW
Full load Efficiency	97.8% (targeted)	98.19%
DC voltage peak-to-peak ripple	20 V	20 V
DC average voltage accuracy	0.5% (maximum)	0.0001%
AC current THD (half load to full load)	1% (maximum)	0.9995%

3. **Technical Discussion of Design:**

Schematic of boost PFC with average current mode controller:



3.1 Design of the boost PFC rectifier power stage: We are given $V_{ac,rms} = 230\ V$. The design is done assuming that the output of the rectifier is constant at $V_g = V_{ac,rms}\sqrt{2} = 230\sqrt{2}\ V$.

a. Preliminary design:

The given values are: $P_{out} = 6.6\ kW, f = 60\ Hz, V_c = 400\ V, \Delta V_{c,pp} = 20\ V, \eta_{min} = 0.978$. The loss in the inductor is $P_L = 0.5 * 0.01 * P_{out} = 33W$. We assume $f_s = 100\ kHz$. The initial calculations are done as follows:

$$\Delta V_c = \frac{\Delta V_{c,pp}}{2} = 10\ V$$
$$\omega = 2\pi f = 376.9911\ rad/s$$
$$D = 1 - \frac{V_g}{V_c} = 0.1868$$
$$D' = 1 - D = 0.8132$$
$$I_{out} = \frac{P_{out}}{V_c} = 16.5A$$
$$I_g = \frac{I_{out}}{D'} = 20.2909\ A$$
$$I_{ac} = \frac{P_{out}}{\eta_{min} V_{ac}} = 29.3412\ A$$

We assume peak-to-peak ripple as: $\%Ripple = 20\% = 0.2$

The capacitor is designed using:

$$C = \frac{P_{out}}{\omega V_c^2 \Delta V_c} \qquad [2]$$
$$= 0.0022\ F$$

So a Nippon Chemi-Con RHA series capacitor (see Appendix) with capacitance $2200\ \mu F$ is chosen.

The inductor is designed using:

$$L = \frac{V_{ac,rms}^2}{\%Ripple * f_s P_{out}}\left(1 - \frac{\sqrt{2}V_{ac,rms}}{V_c}\right) \qquad [2]$$
$$= 74.872\ \mu H$$

For this purpose, IHLP-8787MZ-5A (see Appendix) with inductance 75 μH is chosen.

For the boost converter, the MOSFET switch is chosen from the CoolMOS™ C7 series with lowest R_{on}. This is found to be IPB60R040C7 (see Appendix) with the following parameters:

$$R_{on} = 40\ m\Omega$$
$$C_{oss} = 85\ pF$$

For calculating losses, the conduction losses are first calculated. Here $V_M = 230\sqrt{2}\ V$

$$I_{Q1,rms} = I_{ac} * \sqrt{1 - \frac{8V_M}{3\pi V_c}} \qquad [3]$$
$$= 16.3301\ A$$
$$P_{Q1,conduction} = I_{Q1,rms}^2 R_{on} = 10.6669\ W$$

Next, the switching losses are calculated: $P_{Q1,switching} = 0.5 C_{oss} V_c^2 f_s = 0.68\ W$

The total losses in the switch are:

$$P_{Q1} = P_{Q1,conduction} + P_{Q1,switching} = 11.3469\ W$$

Next, a SiC Schottky diode from Wolfspeed is chosen: C3D20060D (see Appendix) with $V_{F,D1} = 1.5V$. Only the conduction losses are considered. This is calculated as follows:

$$I_{D1,rms} = I_{ac}\sqrt{\frac{8V_M}{3\pi V_c}} \qquad [3]$$

$$= 24.3769\ A$$

$$P_{D1} = I_{D1,rms}V_{F,D1} = 36.5653\ W$$

For the DBR, low frequency diodes with a reverse peak voltage greater than $230\ V$ are chosen. Therefore, D8320N (see Appendix) from Infineon is chosen. Each diode has forward voltage $V_{F,D2} = 0.795\ V$. The DBR losses are calculated as:

$$I_{avg} = \frac{2\sqrt{2}P_{out}}{\pi V_{ac,rms}} \qquad [2]$$

$$= 25.8352A$$

$$P_{DBR} = 2I_{avg}V_{F,D2} = 41.0779\ W$$

The total losses are obtained as:

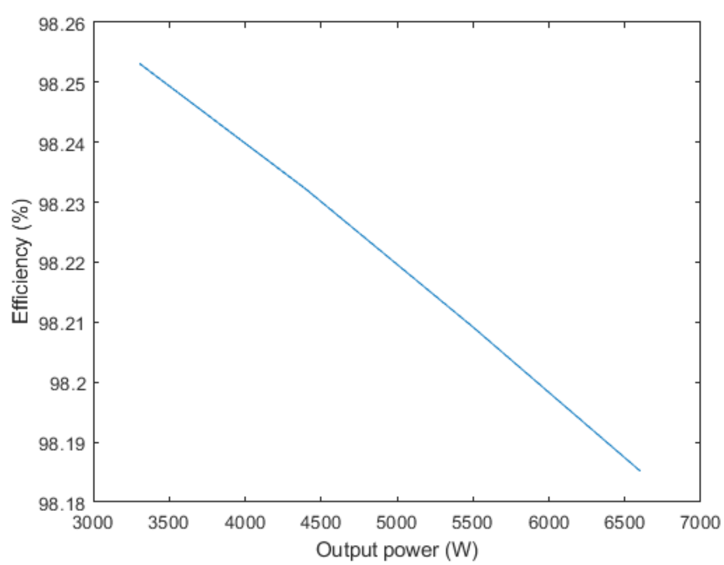
$$P_{loss} = P_L + P_{Q1} + P_{D1} + P_{DBR} = 121.9901\ W$$

The efficiency for this design is:

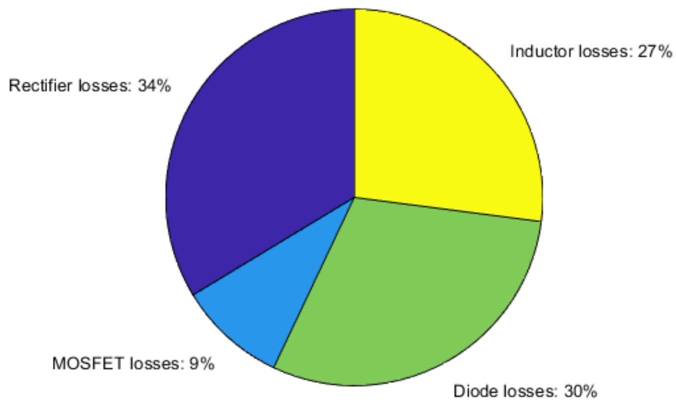
$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} * 100\% = 98.19\%$$

b. Final design: The preliminary design already gives an efficiency better than the targeted, and hence serves as the final design.

Power stage efficiency (half load to full load):



Loss distribution at full load:

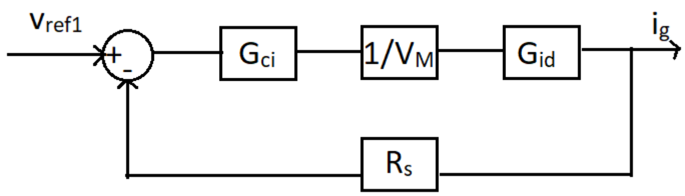


3.2 Design of averaged current-mode controller: The full load resistance is given by:

$$R = \frac{V_c^2}{P_{out}} = 24.2424\Omega$$

a. Preliminary design:

The current control loop can be simplified as follows:



We assume $R_s = 2\Omega, V_M = 1$

For the boost converter, we have:

$$G_{id0} = \frac{2V_c}{D'^2 R} = 49.9055$$

$$f_0 = \frac{D'}{2\pi\sqrt{LC}} = 319.728\ Hz \Rightarrow \omega_0 = 2\pi f_0 = 2.0089 * 10^3\ rad/s$$

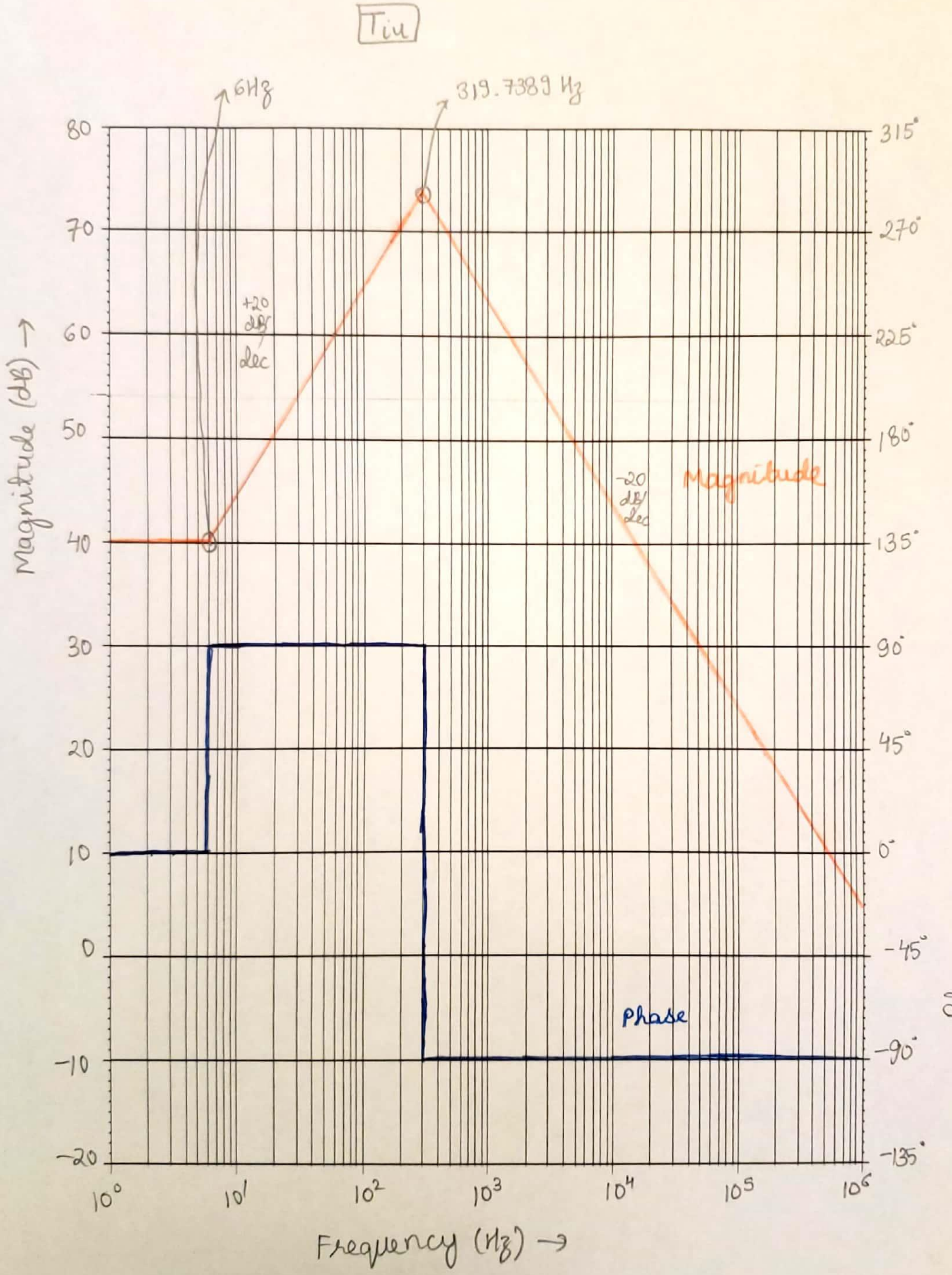
$$f_{zi} = \frac{1}{\pi RC} = 6\ Hz \Rightarrow \omega_{zi} = 37.6991\ \frac{rad}{s}$$

$$Q = D'R\sqrt{\frac{C}{L}} = 106.576$$

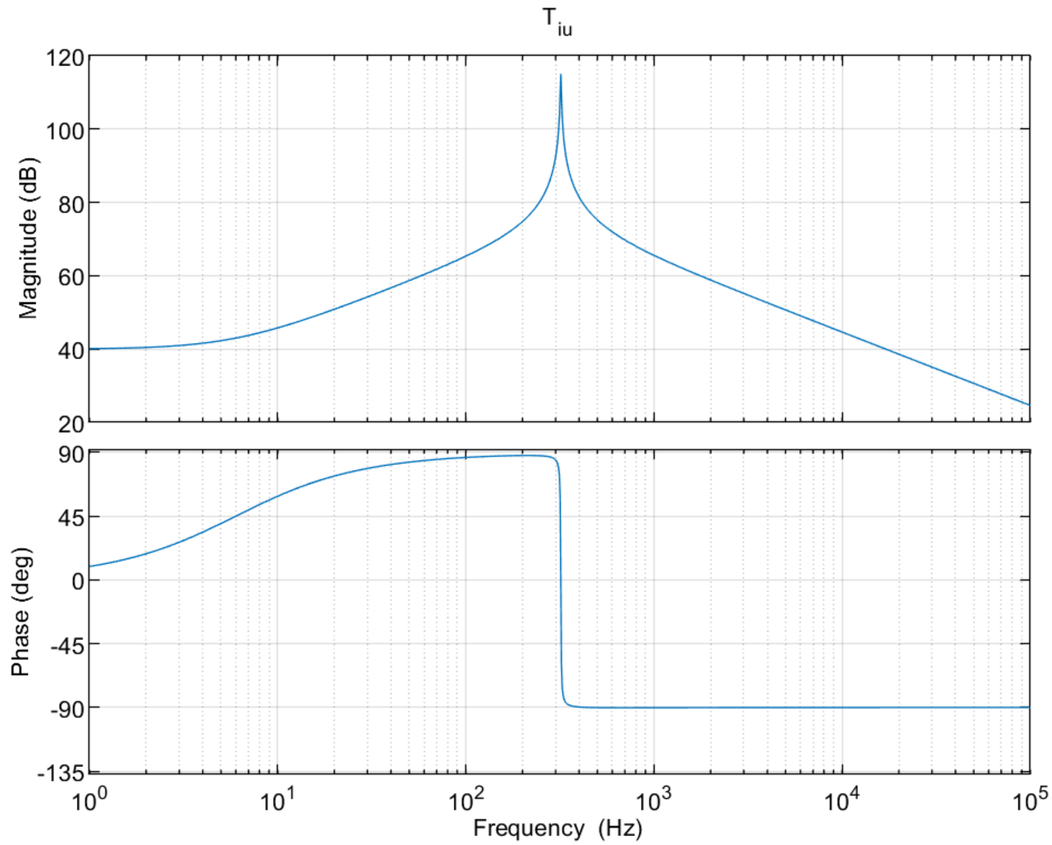
$$G_{id} = \frac{\hat{i}_g}{\hat{d}} = G_{id0}\frac{1 + \frac{s}{\omega_{zi}}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega^2}} = 5.3424 * 10^7 \frac{s + 37.7}{(s^2 + 18.85s + 4.036 * 10^6)}$$

The uncompensated current control loop gain is given by:

$$T_{iu}(s) = \left(\frac{1}{V_M}\right) G_{id} R_S = 1.068 * 10^7 \frac{s + 37.7}{(s^2 + 18.85s + 4.036 * 10^6)}$$



Tiu
6Hz
319.7389 Hz
+20 dB/dec
-20 dB/dec
Magnitude
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
80
70
60
50
40
30
20
10
0
-10
-20
315°
270°
225°
180°
135°
90°
45°
0°
-45°
-90°
-135°
10^0
10^1
10^2
10^3
10^4
10^5
10^6



To design the current controller, the crossover frequency is chosen as $f_{ci} = \frac{f_s}{6} = 16.67\ kHz$ or $\omega_{ci} = \frac{2\pi f_s}{6} = 1.0472 * 10^5\ rad/s$.

At the crossover frequency, the uncompensated system T_{iu} has an asymptotic behavior:

$$T_{iu}(s) = T_{iu0}\frac{1+\dfrac{s}{\omega_{zi}}}{1+\dfrac{s}{Q\omega_0}+\dfrac{s^2}{\omega^2}} \to T_{iu0}\frac{\dfrac{s}{\omega_{zi}}}{\dfrac{s^2}{\omega^2}} = T_{iu0}\frac{\omega_0^2\omega_{zi}}{s}$$

$$T_{iu0}\frac{\omega_0^2}{\omega_{zi}} = \frac{R_S V_c}{V_M L}$$

Therefore, around f_{ci} we have $T_{iu}(s) \to \frac{R_S}{V_M}\frac{V_c}{sL}$

The compensated closed loop transfer function would look like: $T_i(s) = \left(\frac{1}{V_M}\right) G_{ci} G_{id} R_S$

The phase margin of the uncompensated system is $-90°$. Therefore, we need to design a lag PI compensator (to reduce the steady state error) of the form: $G_{ci}(s) = G_{cm}\frac{1+\frac{\omega_{zci}}{s}}{1+\frac{s}{\omega_{pci}}}$

Around f_{ci} we have $T_i(s) \to G_{cm}\frac{R_S}{V_M}\frac{V_c}{sL}$ [4]

We first find G_{cm} to get the desired crossover frequency:

$$G_{cm}\frac{R_s}{V_M}\frac{V_c}{sL} = 1 \Rightarrow G_{cm} = \frac{L\omega_C}{V_c}\frac{V_M}{R_s} = 0.0098$$

We assume the compensated system to have a phase margin of 52°, so the k-factor method is applied with $boost = 52°$:

$$k = \tan\left(\frac{boost}{2} + 45°\right) \qquad [1]$$
$$= 2.9042$$

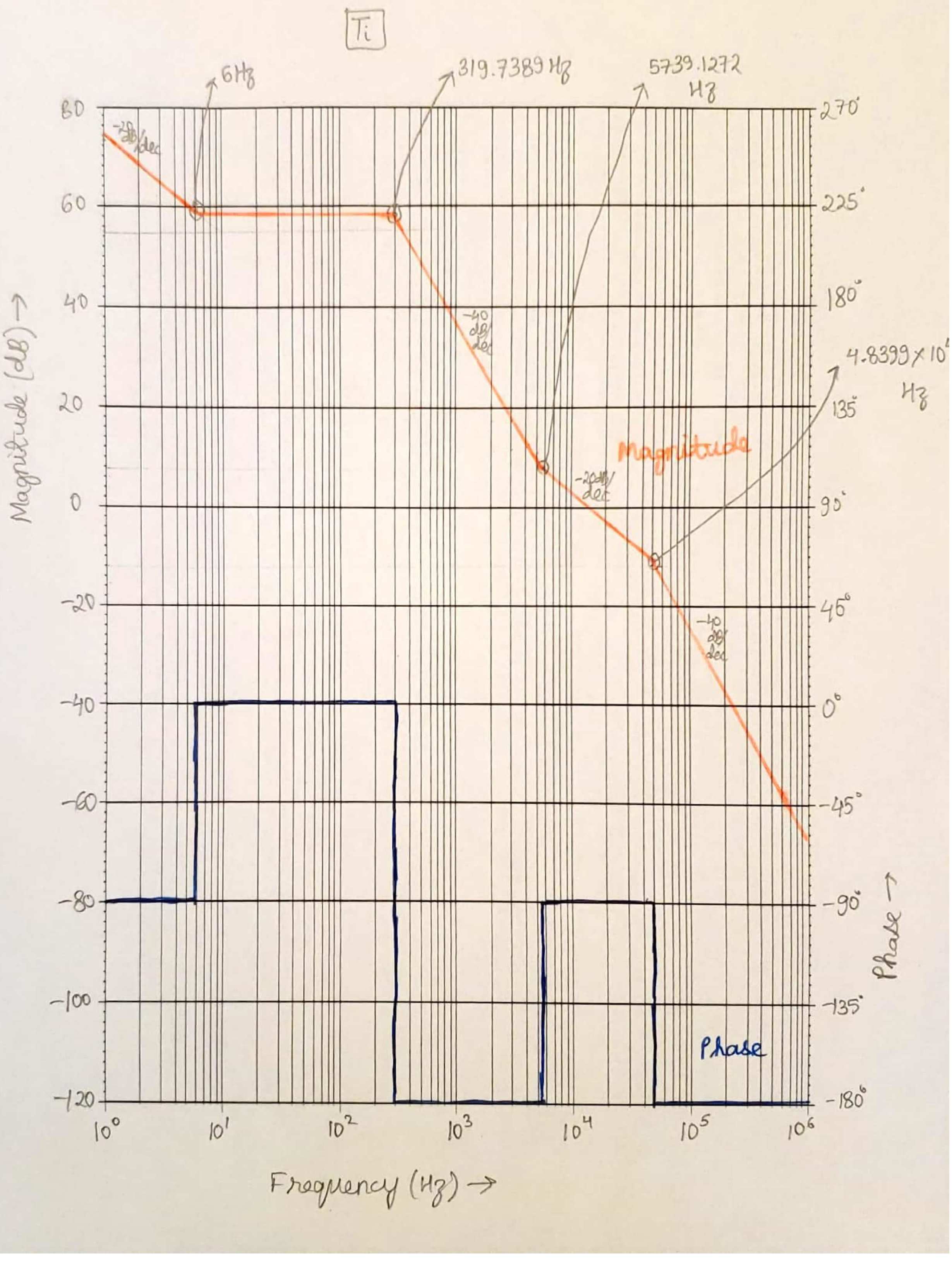
The pole and zero of the current control loop compensator are given by the following [1]:

$$\omega_{pci} = k\omega_{ci} = 3.0413 * 10^5 \frac{rad}{s}$$
$$\omega_{zci} = \frac{\omega_{ci}}{k} = 3.6058 * 10^4 \frac{rad}{s}$$

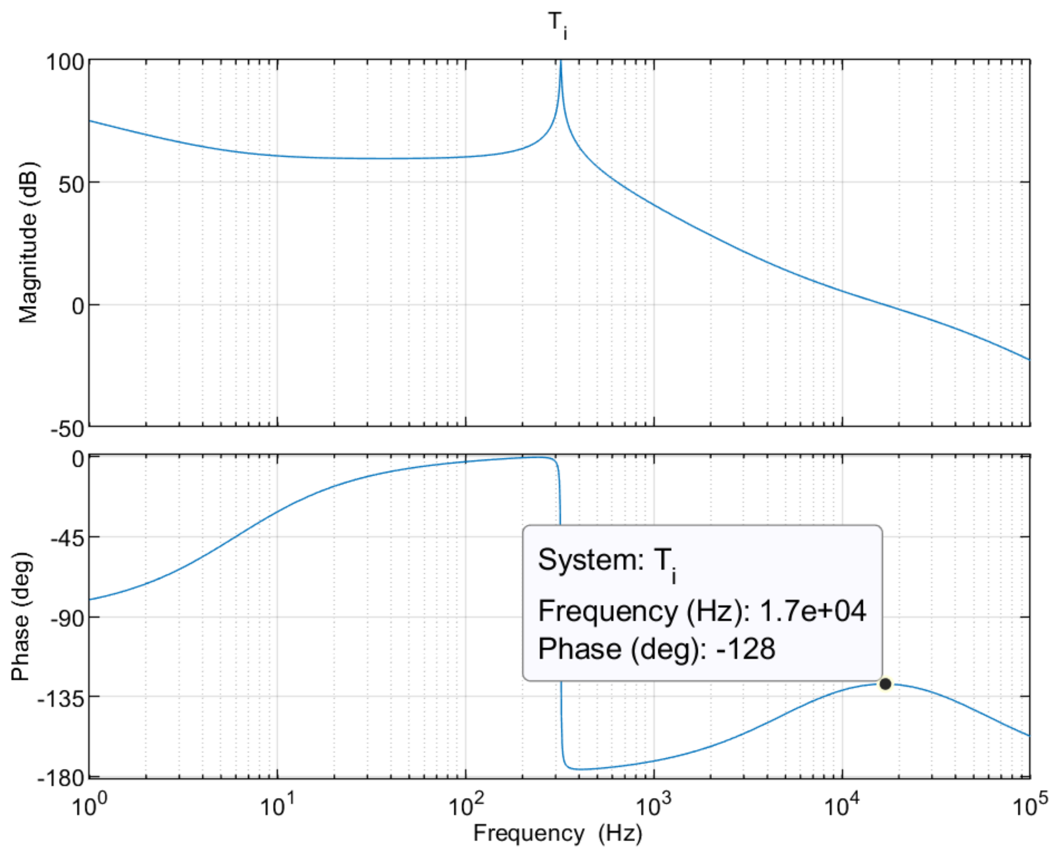
This gives the current control loop compensator as: $G_{ci}(s) = \frac{2981s + 1.075*10^8}{s^2 + 3.041*10^5 s}$

Thus the compensated current control loop gain is:

$$T_i(s) = 3.1848 * 10^{10} \frac{(s + 37.7)(s + 3.606 * 10^4)}{s\,(s + 3.041 * 10^5)\,(s^2 + 18.85s + 4.036 * 10^6)}$$



Ti
6Hz
319.7389 Hz
5739.1272 Hz
4.8399 × 10⁴ Hz
-20dB/dec
-40 dB/dec
-20dB/dec
-40 dB/dec
Magnitude
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
80
60
40
20
0
-20
-40
-60
-80
-100
-120
270°
225°
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
10⁰
10¹
10²
10³
10⁴
10⁵
10⁶



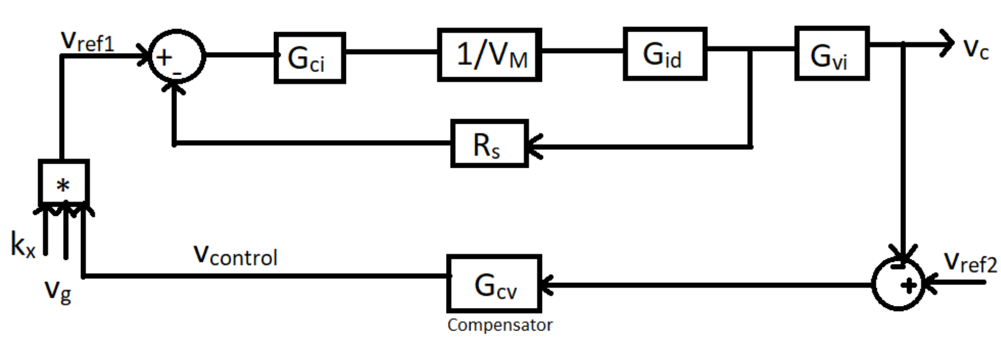
The closed loop control-to-current transfer function is given by:

$$G_{ic}(s) = \frac{\hat{\imath}_g}{\hat{v}_{ref1}} = \frac{1}{R_s}\frac{T_i}{T_i + 1}$$

The voltage control loop bandwidth is well below the crossover frequency of the current control loop. At such frequencies, we have:

$$G_{ic}(s) \approx \frac{1}{R_s}$$

The voltage control loop is obtained as:



The feedback of both v_c and v_g are assumed to be sensed using a sensor gain $H = \frac{5}{400}$ to allow the voltages in the control circuit to remain within $0 - 5V$.
Since the dynamics of the voltage control loop are much slower than that of the current control loop, we can calculate the value of k_x using the steady state value of $V_g = 230\sqrt{2}\,V$. For an initial assumption, let us take the gain of the multiplier block to be equal to $1 \Rightarrow k_x H V_g = 1$

$$k_x = \frac{1}{V_g H} = 0.246$$

The control-to-output transfer function of the voltage control loop can be given by:

$$G_{vc} = \frac{\hat{v}_c}{\hat{v}_{ref1}} = \frac{\hat{v}_c}{\hat{d}}\frac{\hat{d}}{\hat{v}_{ref1}}$$

For frequencies well below the crossover frequency of the current control loop:

$$\hat{\imath}_g = G_{id}\hat{d} \approx \hat{\imath}_{ref1} = \frac{\hat{v}_{ref1}}{R_s} \Rightarrow \frac{\hat{d}}{\hat{v}_{ref1}} = \frac{1}{R_s}\frac{1}{G_{id}}$$

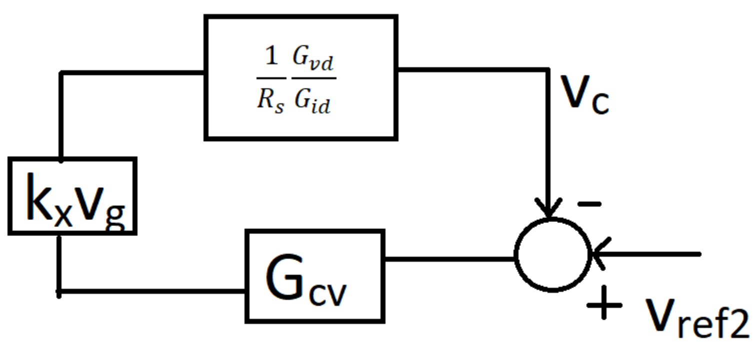
$$G_{vc} \approx \frac{1}{R_s}\frac{G_{vd}}{G_{id}}$$

Let $den(s) = 1 + \frac{sL}{(D')^2 R} + \frac{s^2 LC}{(D')^2}$

$$G_{vd} = \frac{\frac{V_c}{D'}\left(1 - \frac{sL}{(D')^2 R}\right)}{den(s)}$$

$$G_{id} = \frac{\frac{2V_c}{(D')^2 R}\left(1 + \frac{sRC}{2}\right)}{den(s)}$$

The approximate model of the voltage control loop looks like:



Let us first consider the uncompensated loop gain: $T_{vu} \approx H(k_x H V_g)G_{vc} = HG_{vc}$

$$\omega_{zv} = \frac{(D')^2 R}{L} = 2.141 * 10^5 \frac{rad}{s} \Rightarrow f_{zv} = \frac{\omega_{zv}}{2\pi} = 34.075\,kHz$$

$$\omega_{pv} = \frac{2}{RC} = 37.6991 \frac{rad}{s} \Rightarrow f_{pv} = \frac{\omega_{pv}}{2\pi} = 6Hz$$

$$G_{vc0} = \frac{D'R}{2R_s} = 4.9283$$

This gives:

$$G_{vc} = G_{vc0}\frac{\left(1-\dfrac{s}{\omega_{zv}}\right)}{(1+\dfrac{s}{\omega_{pv}})} = \frac{-185.8s + 3.978 * 10^7}{2.141 * 10^5 s + 8.071 * 10^6}$$

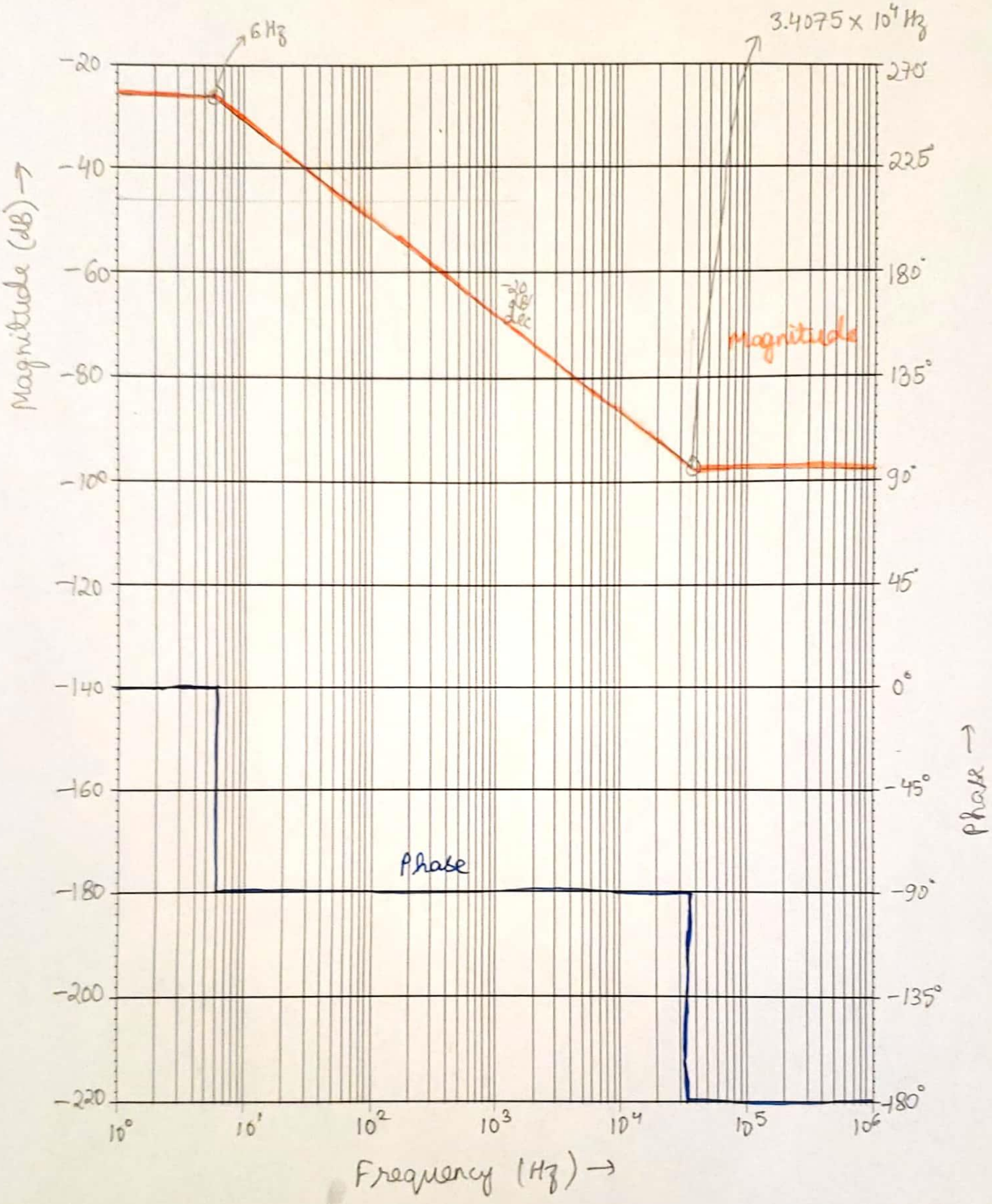
Let the crossover frequency of the voltage control loop be $f_{cv} = 30Hz$ or $f_{cv} = 188.4956\ rad/s$, which is below $120\ Hz$, the frequency of the rectified current. This is also above f_{pv} and well below f_{zv}. Therefore, T_{vu} behaves asymptotically around f_{cv}:

$$T_{vu} = H\frac{D'R}{2R_s}\frac{\left(1-\dfrac{sL}{(D')^2R}\right)}{1+\dfrac{sRC}{2}} \rightarrow H\frac{D'R}{2R_s}\frac{1}{\dfrac{sRC}{2}} = H\frac{D'}{R_sCs} \qquad [4]$$

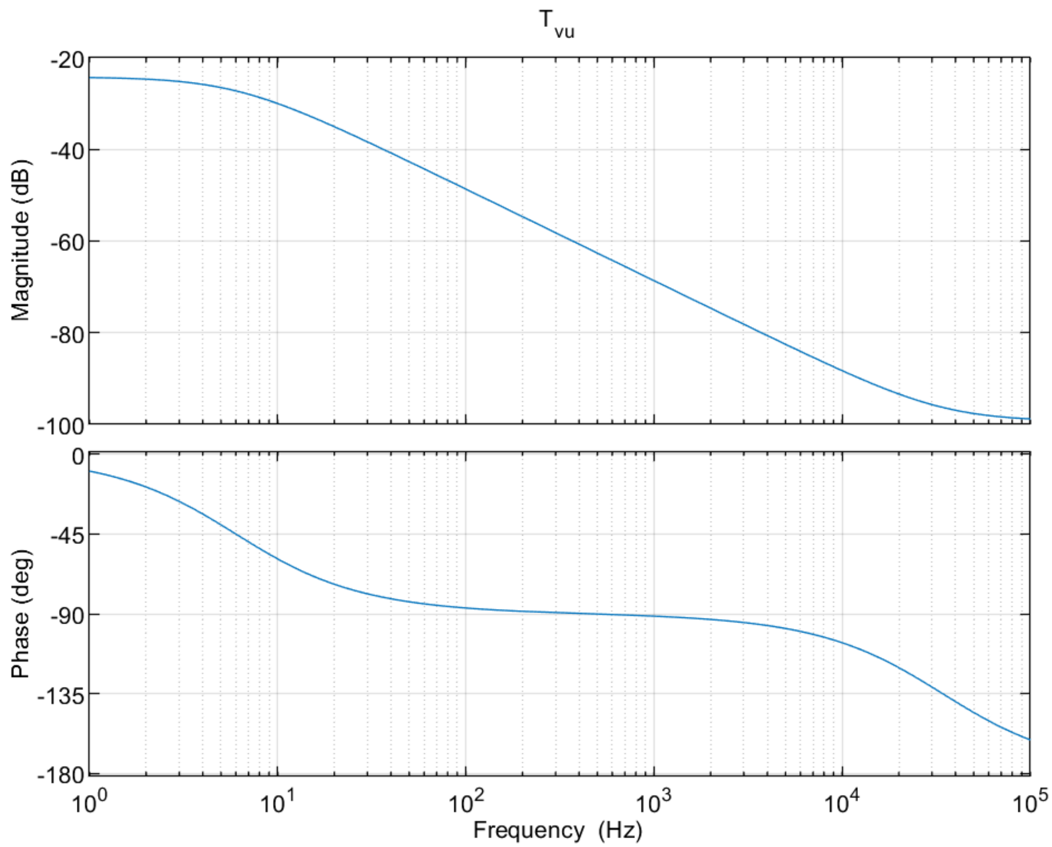
We first find G_{vm} using: $G_{vm}H\frac{D'R}{R_s}\frac{1}{2\pi f_{cv}RC} = 1 \Rightarrow G_{vm} = \frac{2\pi f_{cv}CR_s}{D'H} = 81.1636$

Thus we have $T_{vu} = -1.0847 * 10^{-5}\frac{(s-2.141*10^5)}{(s+37.7)}$

Tvu



6 Hz
3.4075 × 10^4 Hz
-20
-40
-60
-80
-100
-120
-140
-160
-180
-200
-220
Magnitude (dB) →
270°
225°
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
Phase →
-20 dB/dec
Magnitude
Phase
10^0
10^1
10^2
10^3
10^4
10^5
10^6
Frequency (Hz) →



The compensated loop gain would look like: $T_v \approx HG_{cv}G_{vc0}\frac{\left(1-\frac{s}{\omega_{zv}}\right)}{\left(1+\frac{s}{\omega_{pv}}\right)}$.

We can use a simple lag PI compensator $G_{cv}(s) = G_{vm}(1 + \frac{\omega_{zcv}}{s})$.

Around f_{cv} we have $T_v \to G_{cv}\frac{D'}{R_s C s}$

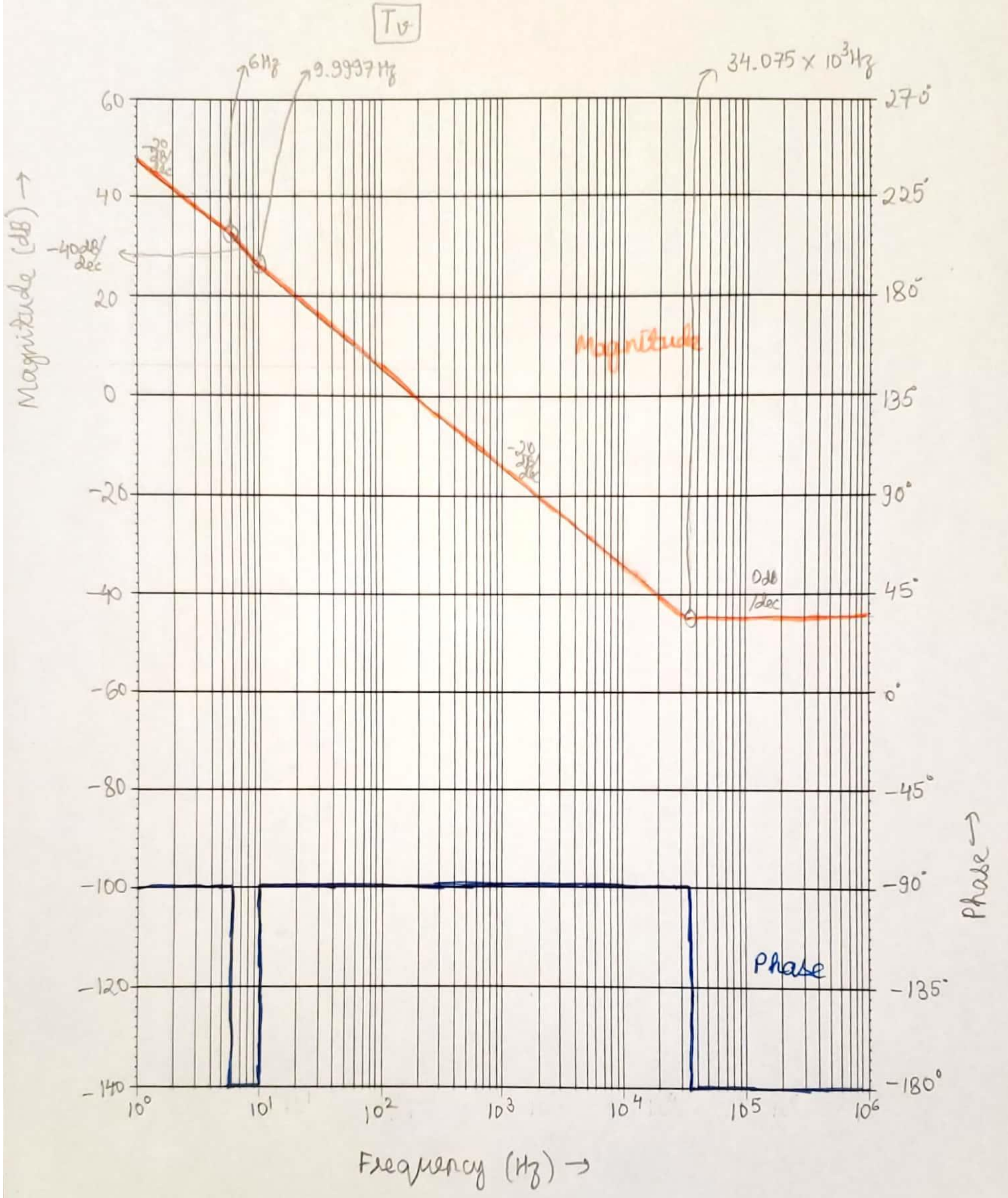
Now we place ω_{zcv} much below ω_{cv}: $\omega_{zcv} = \frac{\omega_{cv}}{3} = 62.8319\frac{rad}{s}$

Thus we obtain:

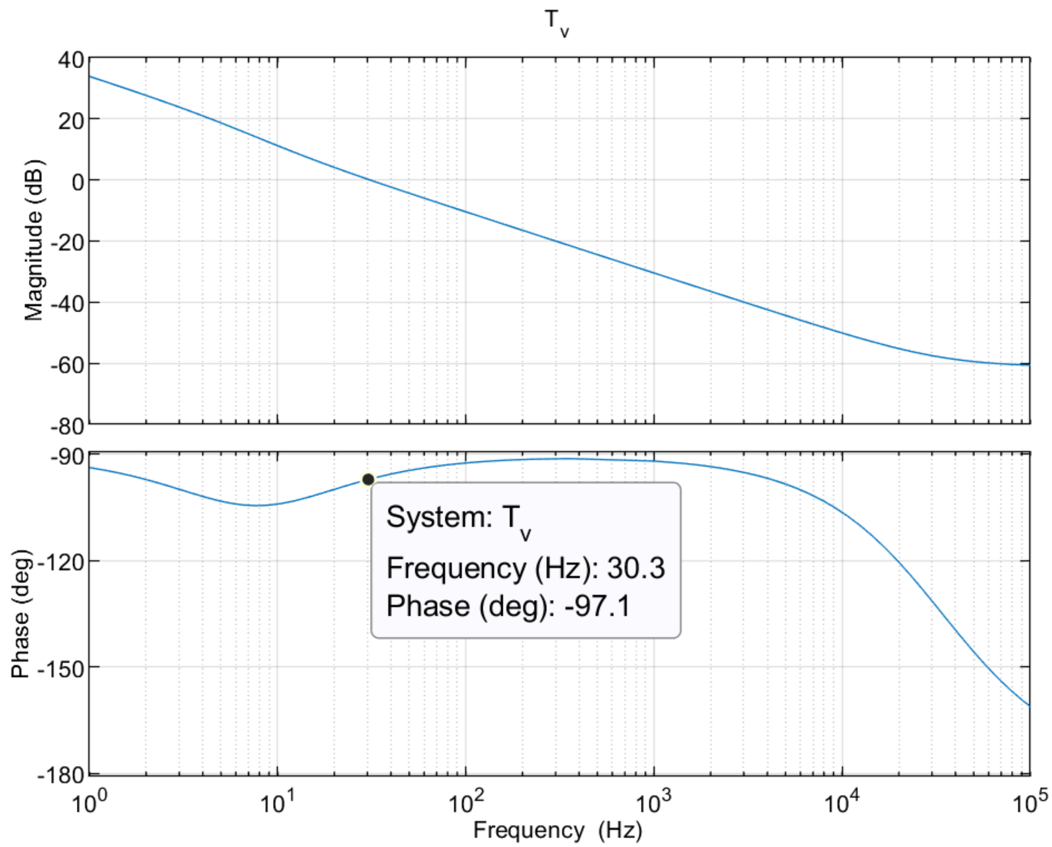
$$G_{cv}(s) = \frac{81.16s + 5100}{s}$$

$$T_v = -0.0008804\frac{(s - 2.141 * 10^5)(s + 62.83)}{s\ (s + 37.7)}$$

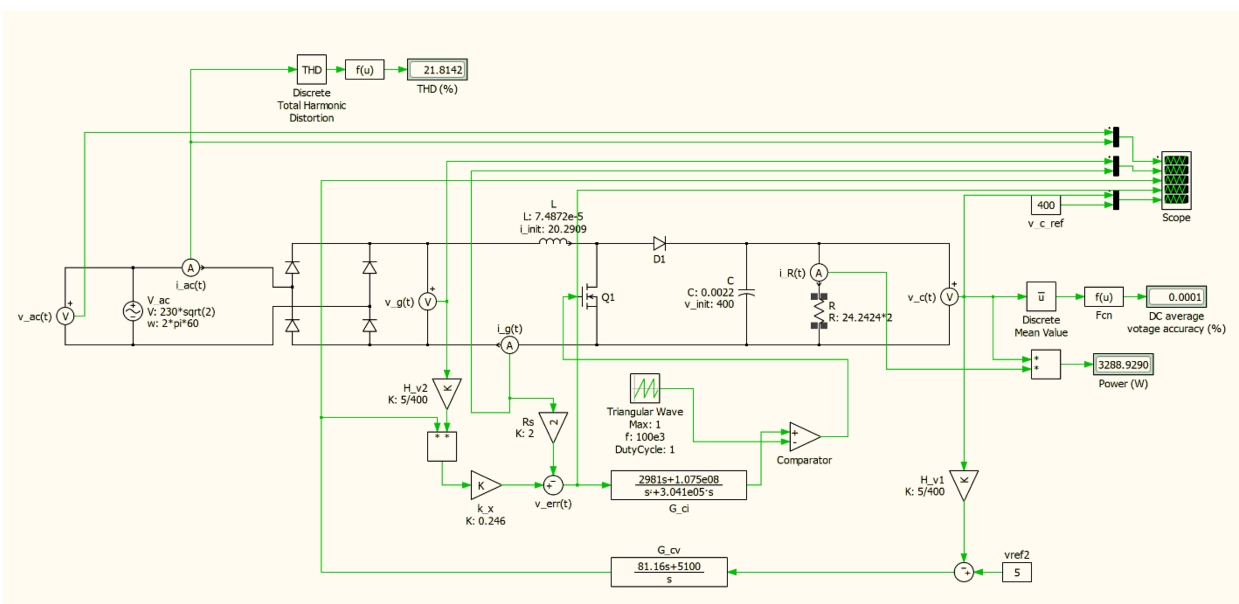
It can be observed that T_v has a high phase margin of $180° - 97° = 83°$.



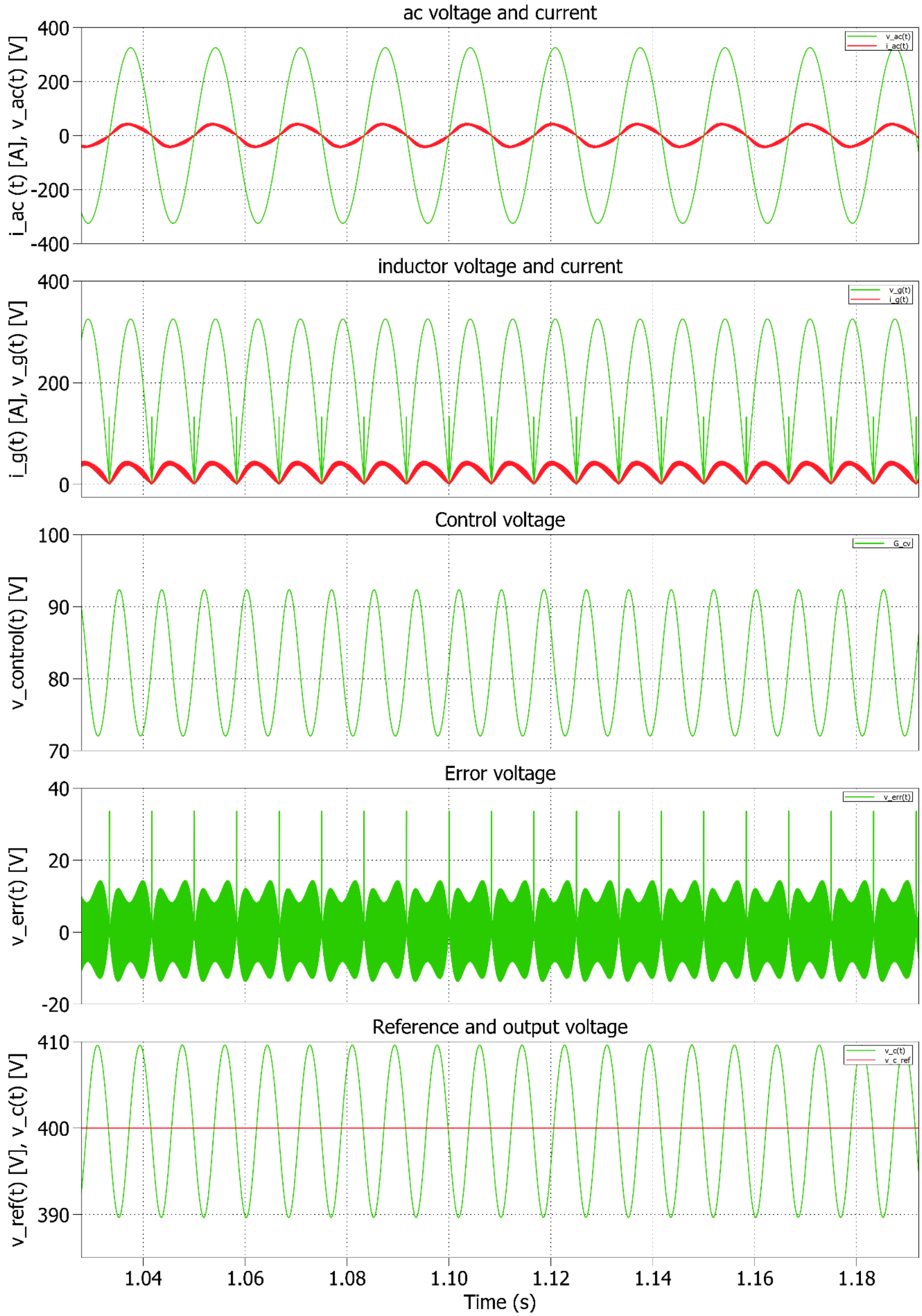
Tv
6Hz
9.9997 Hz
34.075 x 10^3 Hz
-20 dB/dec
-40dB/dec
-20 dB/dec
0dB /dec
Magnitude
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
60
40
20
0
-20
-40
-60
-80
-100
-120
-140
270°
225°
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
10^0
10^1
10^2
10^3
10^4
10^5
10^6



PLECS schematic of preliminary average mode design with half load condition (worst case THD: 21.8142%, average voltage accuracy: 0.0001%):



Full load steady state voltages and currents with preliminary average mode design:



b. **Final design:** The preliminary design is able to roughly achieve the required waveforms but the THD requirement is not met.

For the final design, first the voltage control loop uncompensated transfer function is compensated using the PID tuner in MATLAB.

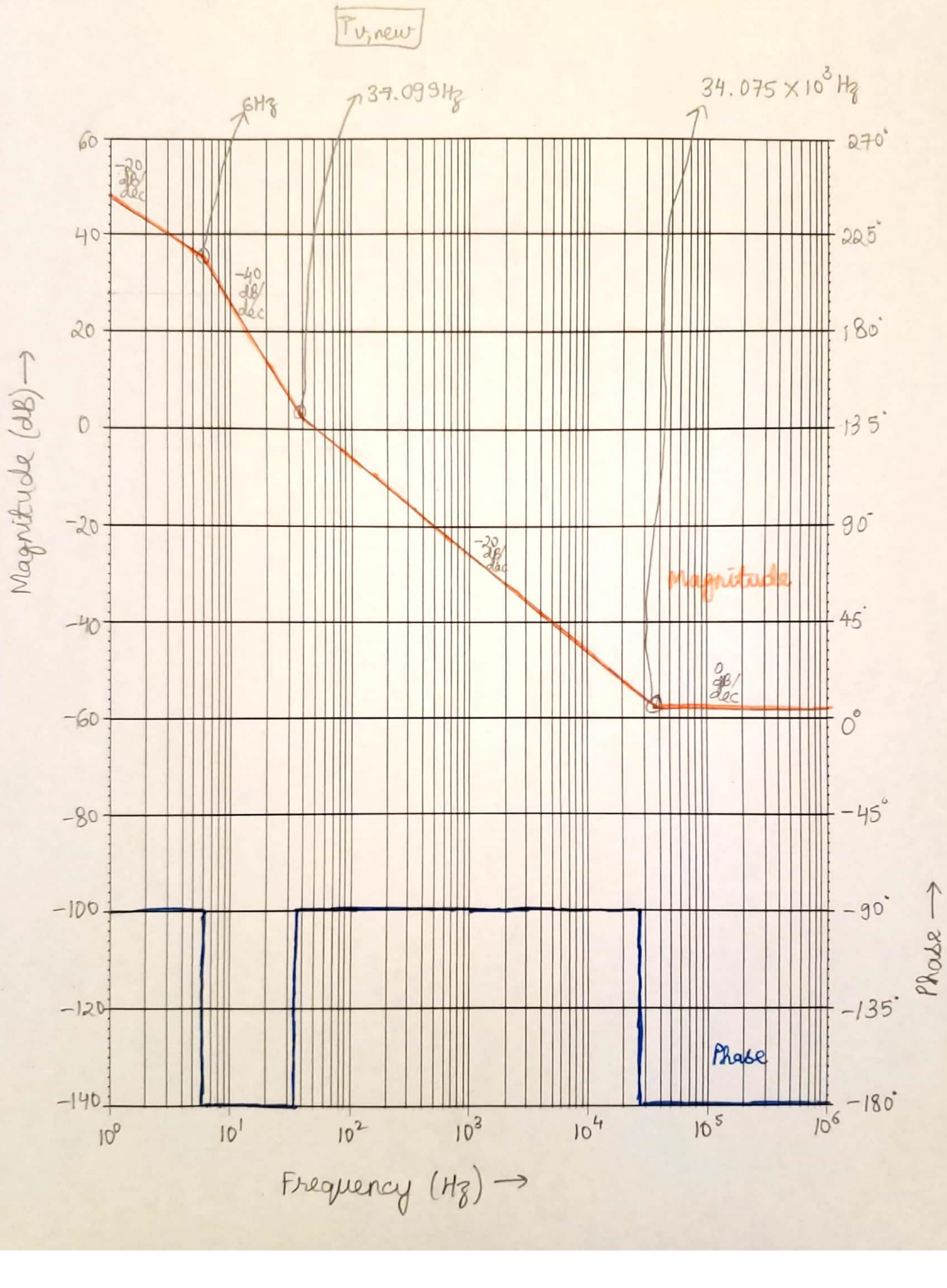
To obtain better harmonic performance, the harmonic at $f_h = 120\ Hz$ needs to be attenuated significantly.
Therefore, the bandwidth is reduced even further with:
$f_{cv,new} = \frac{f_h}{6} = 20\ Hz$ or $\omega_{cv,new} = 2\pi f_{cv,new} = 125.6637\ \frac{rad}{s}$

The preliminary design phase margin of $83°$ may not be needed and therefore that is reduced to $45°$. The PID tuner returns the new compensator transfer function as:

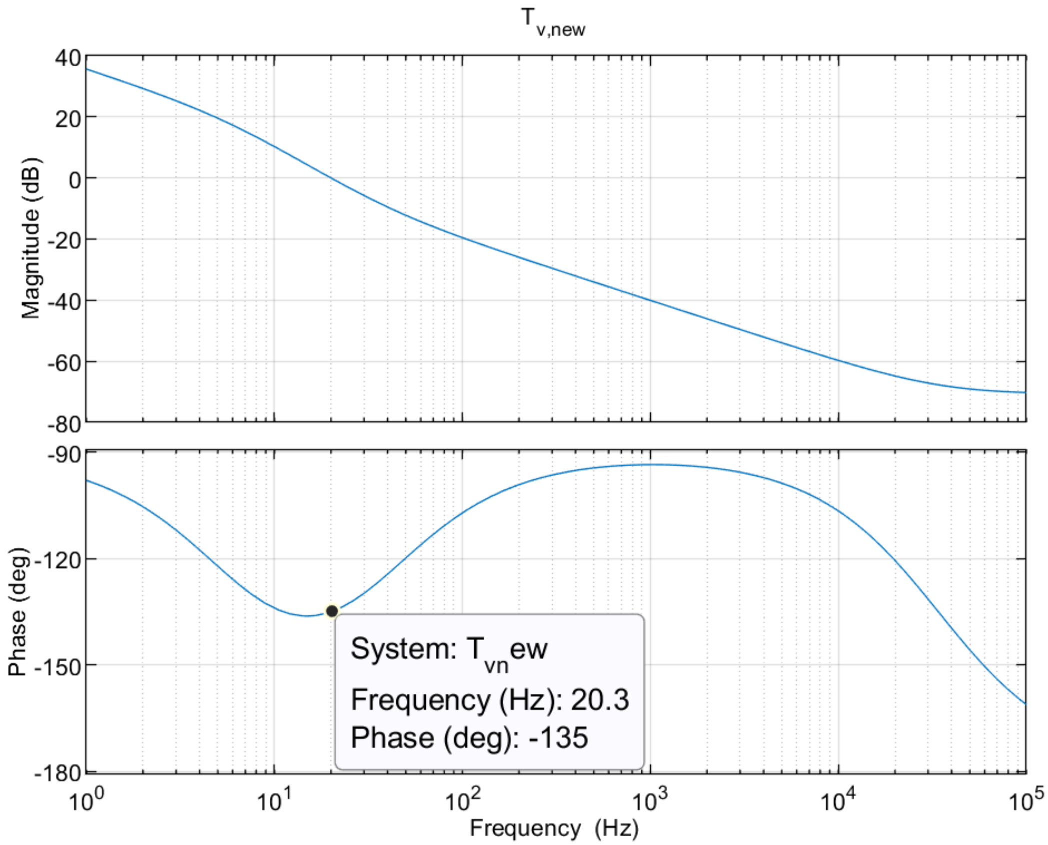
$$G_{cv,new} = \frac{0.115s + 26.8}{0.00429s}$$

The compensated closed loop gain is therefore:

$$T_{v,new} = T_{vu}G_{cv,new} = -0.00029071\frac{(s - 2.141 * 10^5)(s + 233.1)}{s\ (s + 37.7)}$$



$T_{v,new}$
6Hz
37.099Hz
34.075 × 10^3 Hz
-20 dB/dec
-40 dB/dec
-20 dB/dec
0 dB/dec
Magnitude
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
60
40
20
0
-20
-40
-60
-80
-100
-120
-140
270°
225°
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
10^0
10^1
10^2
10^3
10^4
10^5
10^6



A multiplier of $k_x, v_g(t)$ and $v_{control}(t)$ is used to control the average power. We can find the emulated resistance R_e as follows:

$$v_a(t) = R_s < i_g(t) >_{T_s}$$

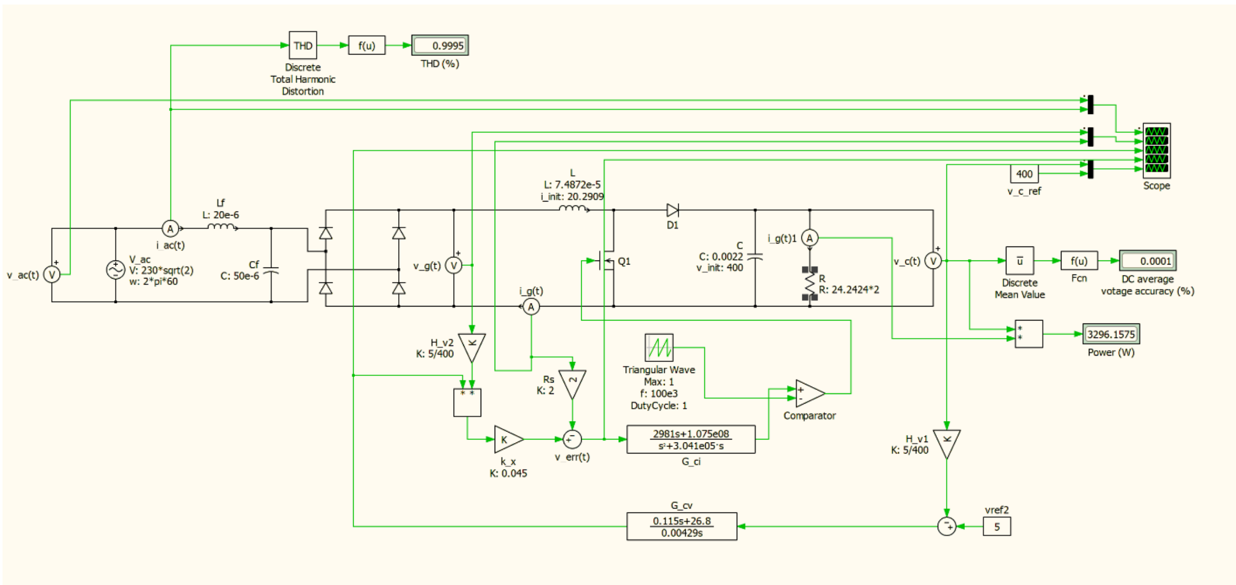
For a well-designed loop: $v_a(t) \approx v_r(t) \Rightarrow v_r(t) = k_x v_g(t) v_{control}(t)$

$$R_e = \frac{v_g(t)}{i_g(t)} = \frac{\frac{v_r(t)}{k_x v_{control}(t)}}{\frac{v_a(t)}{R_s}} = \frac{R_s}{k_x v_{control}(t)}$$

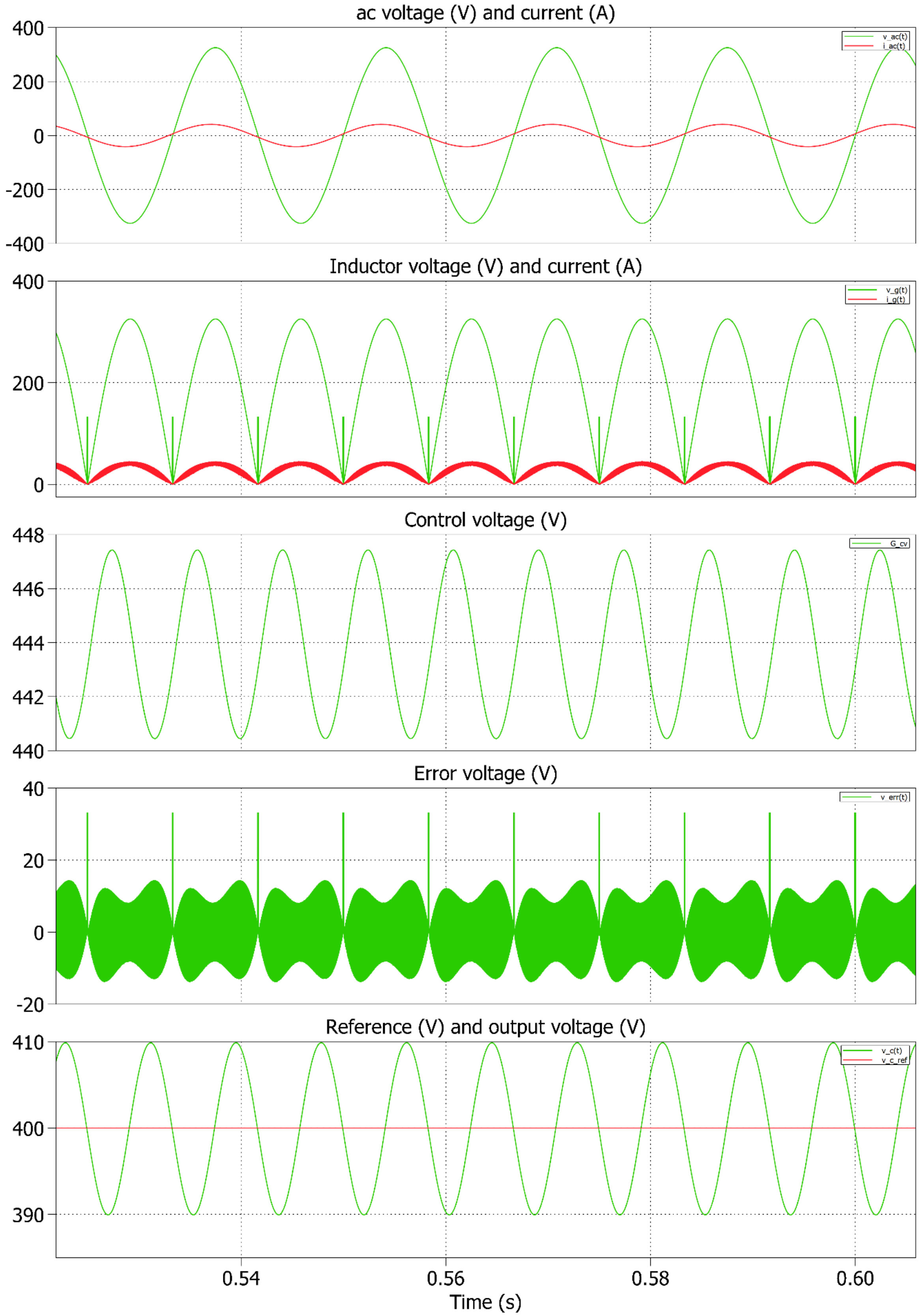
Therefore, a lower value of k_x can help emulate a larger resistance.
The value of k_x is manually tuned in the PLECS closed loop model to meet the THD requirement. Lower values of k_x are found to yield better THD performance.

Finally, an input $L_f - C_f$ filter is added on the ac side to reduce the harmonic content further. The final values used are: $L_f = 20\mu H, C_f = 50\mu F$ and $k_{x,new} = 0.045$

PLECS schematic of final average mode design with half load condition (worst case THD: 0.9995%, average voltage accuracy: 0.0001%):



Full load steady state voltages and currents with final average mode design:



3.3 Design of peak current-mode controller:

a. Preliminary design: The preliminary design of the peak current mode-controller is based on the final design of the average current mode-controller. The more accurate model for peak current mode-controller can be devised. The initial calculations are done below:

$$k_{x,new} = 0.045 \text{ (as before)}$$

$$M_a = M_2 = \frac{V_c - V_g}{L} = 9.9811 * 10^5 \frac{V}{H}$$

$$M_1 = \frac{V_g}{L} = 4.3443 * 10^6 \frac{V}{H}$$

The slope compensation for the peak current controller can be calculated as: $V_a = R_s M_a T_s = 19.9622$. Now the control-to-output transfer function is obtained as:

$$F_m = \frac{f_s}{M_a + \frac{M_1 - M_2}{2}} = 0.0374$$

$$G_{c0} = \frac{F_m V_c}{D' R_s (1 + \frac{2 V_c F_m}{(D')^2 R} + \frac{F_m F_v V_c}{D'})} = 13.1177$$

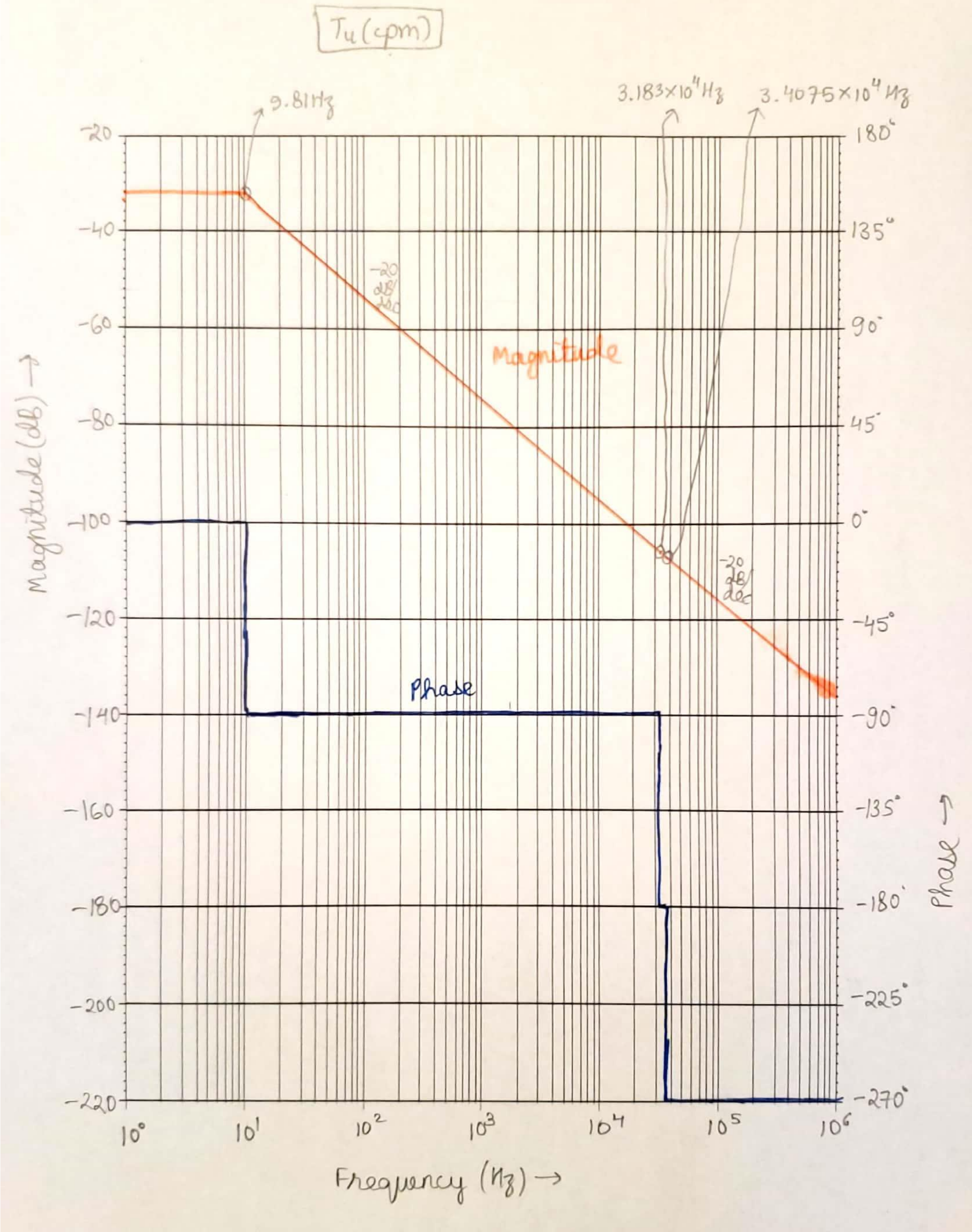
$$\omega_c = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{2 V_c F_m}{(D')^2 R} + \frac{F_m F_v V_c}{D'}} = 3.5113 * 10^3 \frac{rad}{s}$$

$$Q_c = \frac{D' R \sqrt{\frac{C}{L}} \sqrt{1 + \frac{2 V_c F_m}{(D')^2 R} + \frac{F_m F_v V_c}{D'}}}{1 + RC \frac{F_m V_c}{L} - \frac{F_m F_v V_c}{D'}} = 0.0176$$

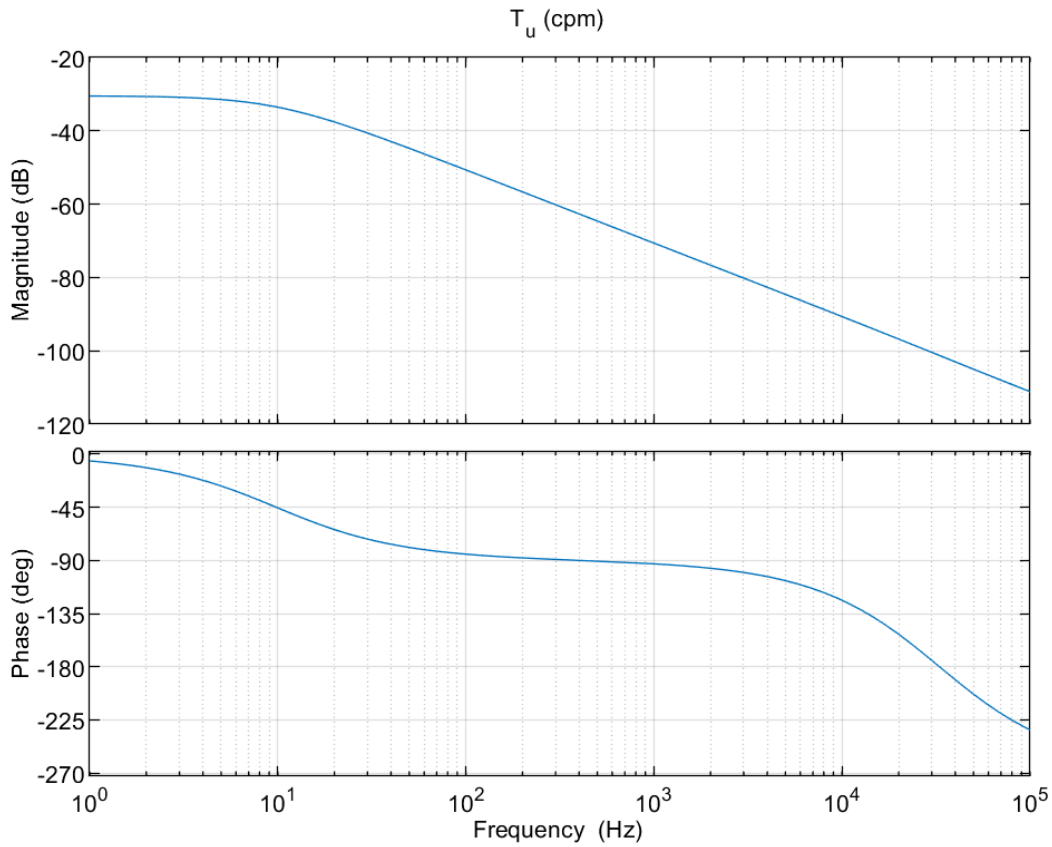
$$G_{vc(cpm)} = G_{c0} \frac{1 - \frac{sL}{(D')^2 R}}{1 + \frac{s}{Q_c \omega_c} + \frac{s^2}{\omega_c^2}} = \frac{-7.465 * 10^5\, s \;+\; 1.598 * 10^{11}}{988.2\, s^2 \;+\; 1.976 * 10^8\, s \;+\; 1.218 * 10^{10}}$$

Now the uncompensated loop transfer function can now be written as:

$$T_{u(cpm)} = H G_{vc(cpm)} k_{x,new} H V_g = -1.7277 \frac{(s - 2.141 * 10^5)}{(s + 2 * 10^5)\,(s + 61.66)}$$



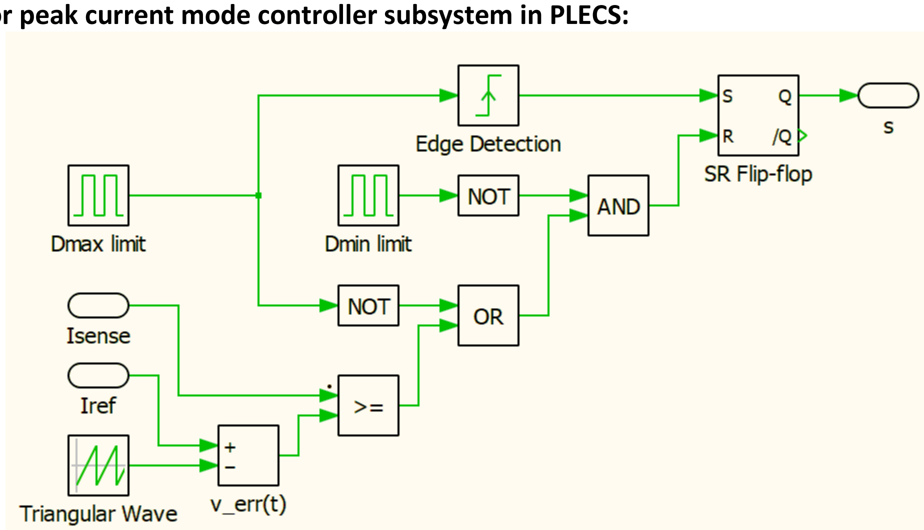
Tu (cpm)
9.81Hz
3.183×10^4 Hz
3.4075×10^4 Hz
-20 dB/dec
Magnitude
-20 dB/dec
Phase
Magnitude (dB) →
Phase →
-20
-40
-60
-80
-100
-120
-140
-160
-180
-200
-220
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
-225°
-270°
10^0
10^1
10^2
10^3
10^4
10^5
10^6
Frequency (Hz) →

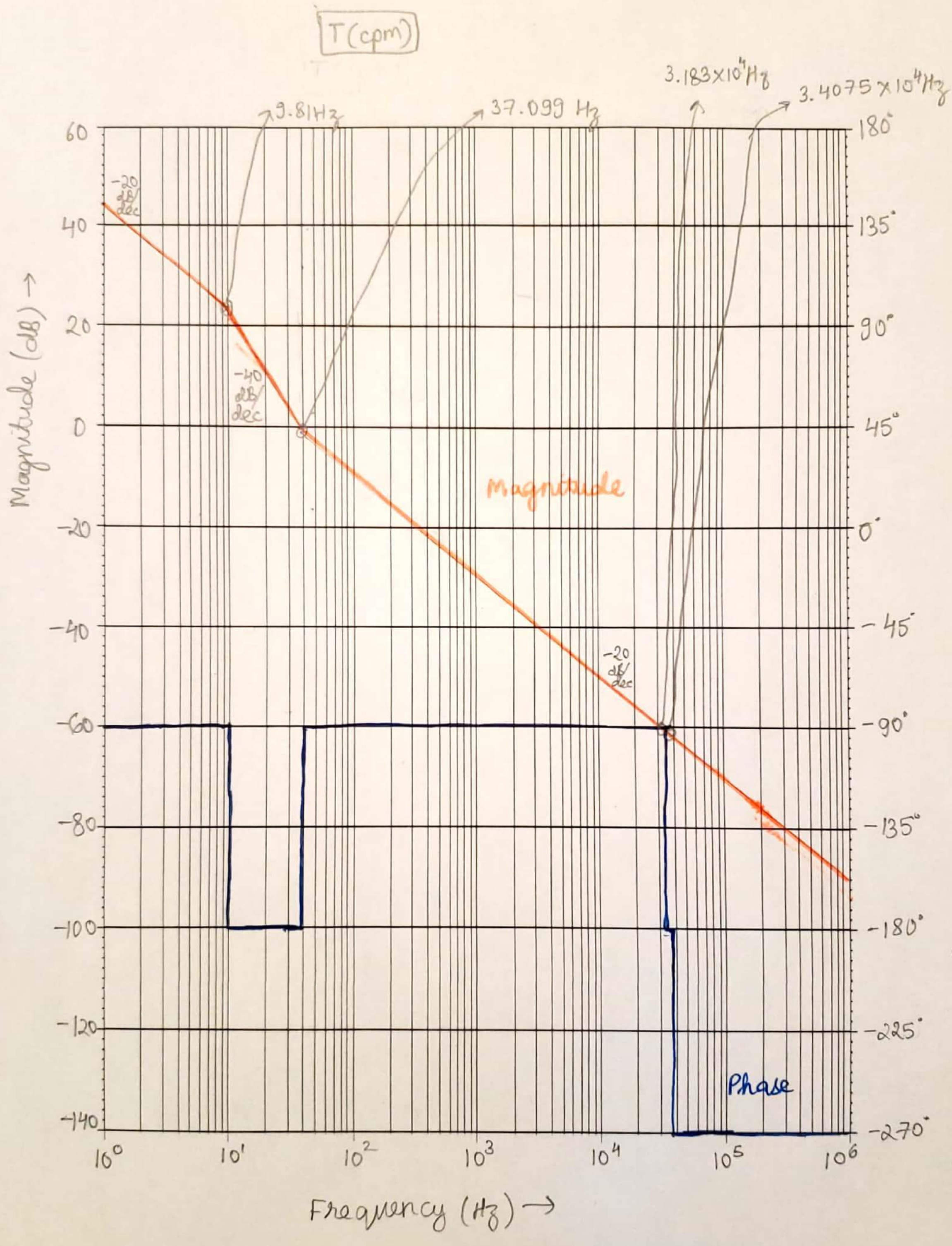


The same compensator $G_{cv,new}$ is added to the peak current mode-control loop to obtain the compensated transfer function as:

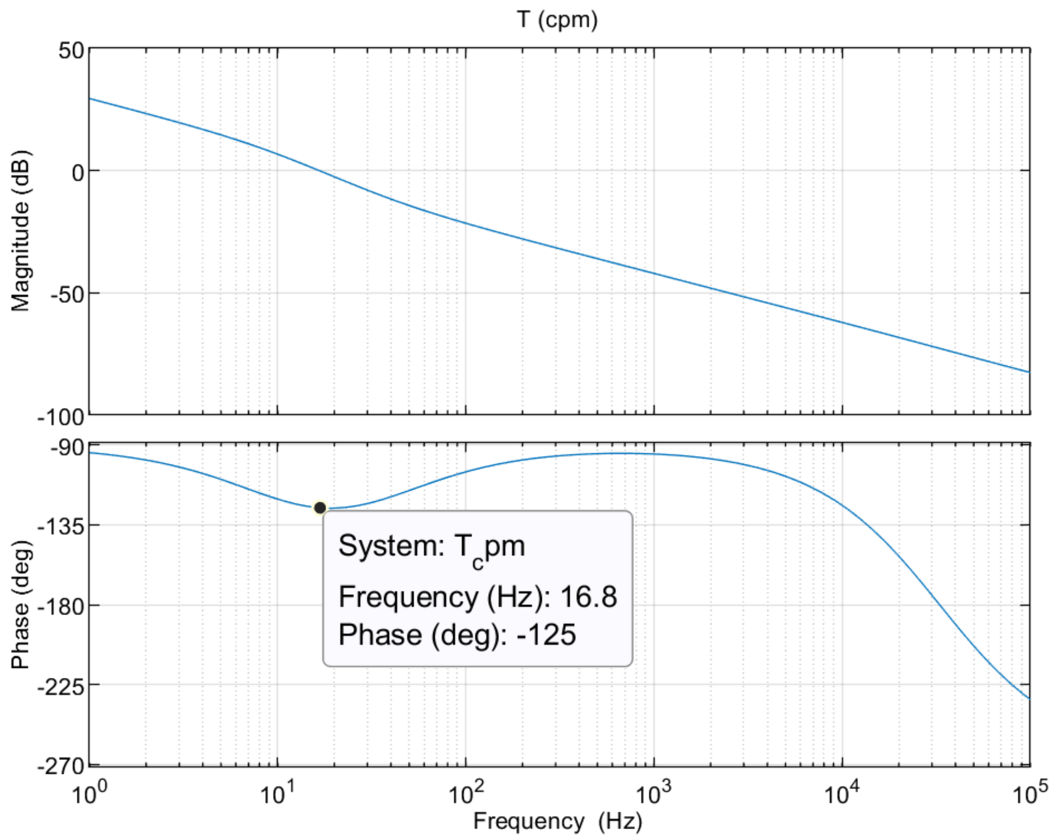
$$T_{cpm} = T_{u(cpm)} G_{cv,new} = -46.301 \frac{(s - 2.141 * 10^5)(s + 233.1)}{s\,(s + 2 * 10^5)\,(s + 61.66)}$$

Schematic for peak current mode controller subsystem in PLECS:

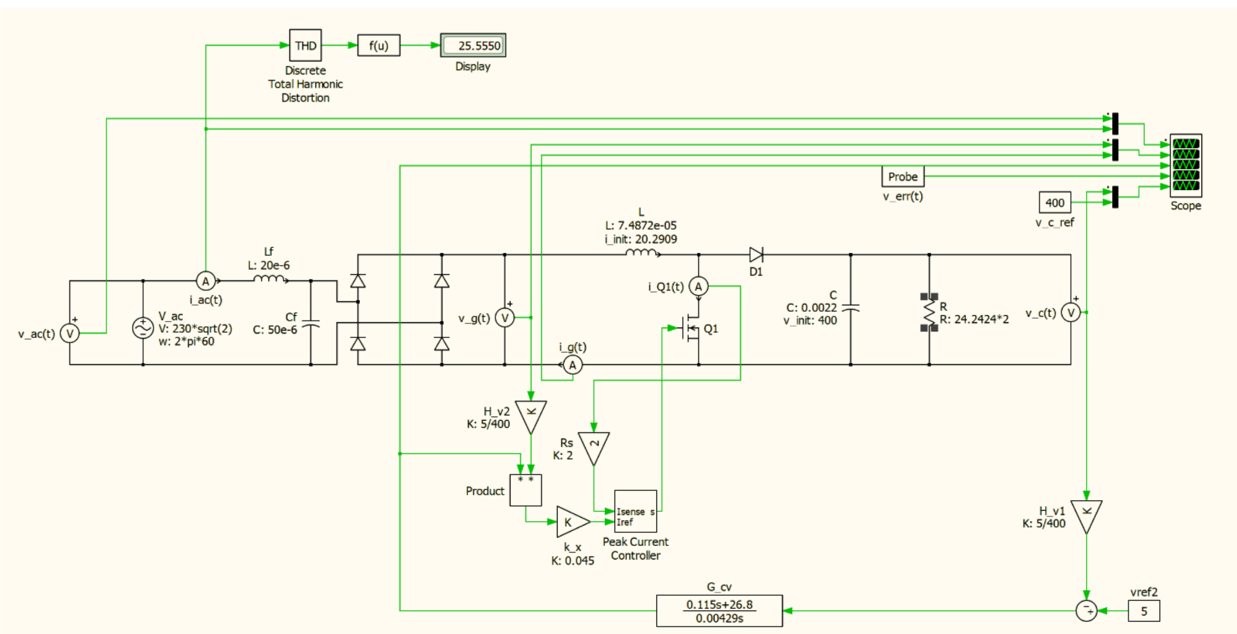




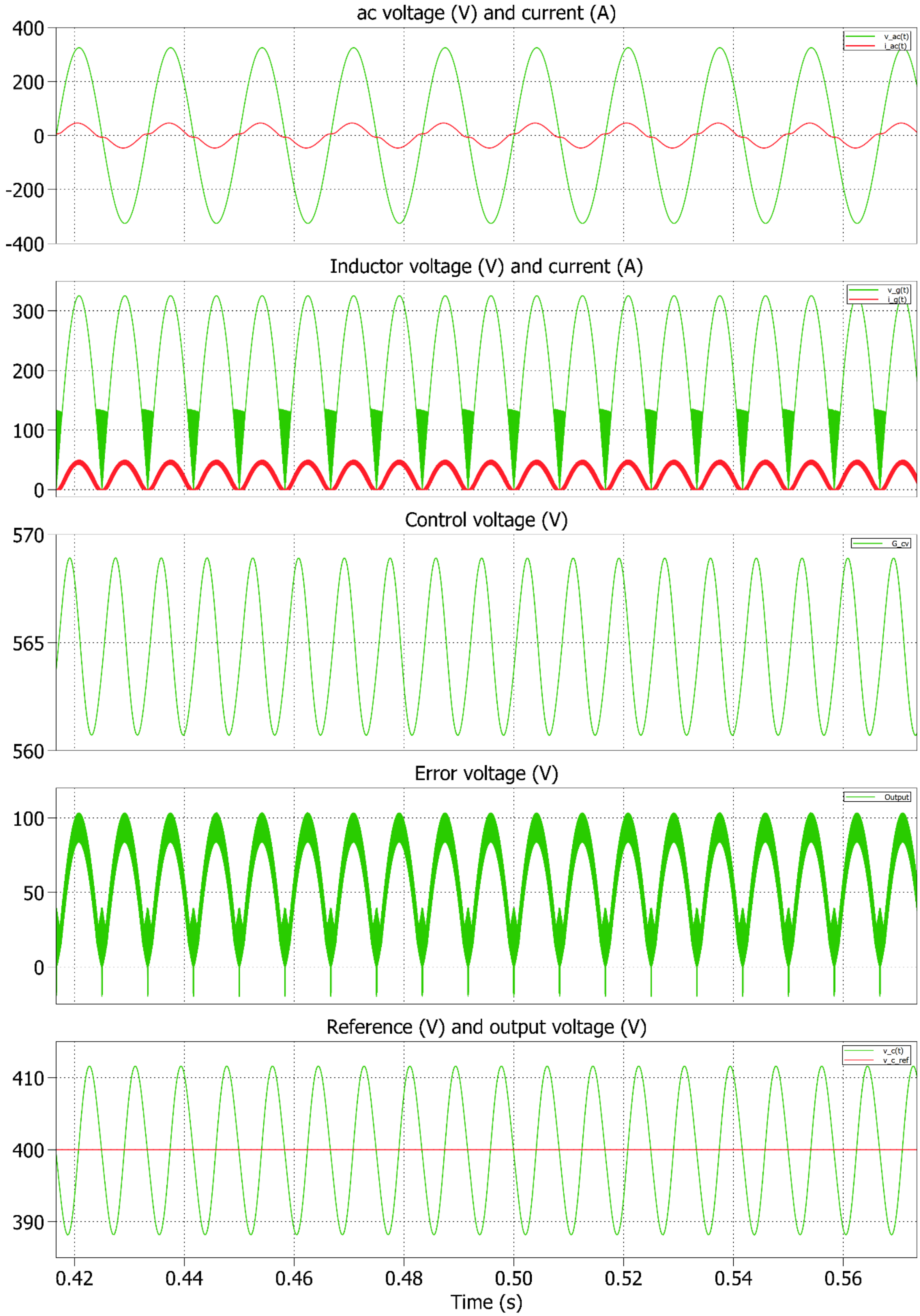
T(cpm)
9.81Hz
37.099 Hz
3.183×10^4 Hz
3.4075×10^4 Hz
-20 dB/dec
-40 dB/dec
-20 dB/dec
Magnitude
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
60
40
20
0
-20
-40
-60
-80
-100
-120
-140
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
-225°
-270°
10^0
10^1
10^2
10^3
10^4
10^5
10^6



PLECS schematic of preliminary peak mode design with half load condition (worst case THD: 25.5528%):



Full load steady state voltages and currents with preliminary peak mode design:



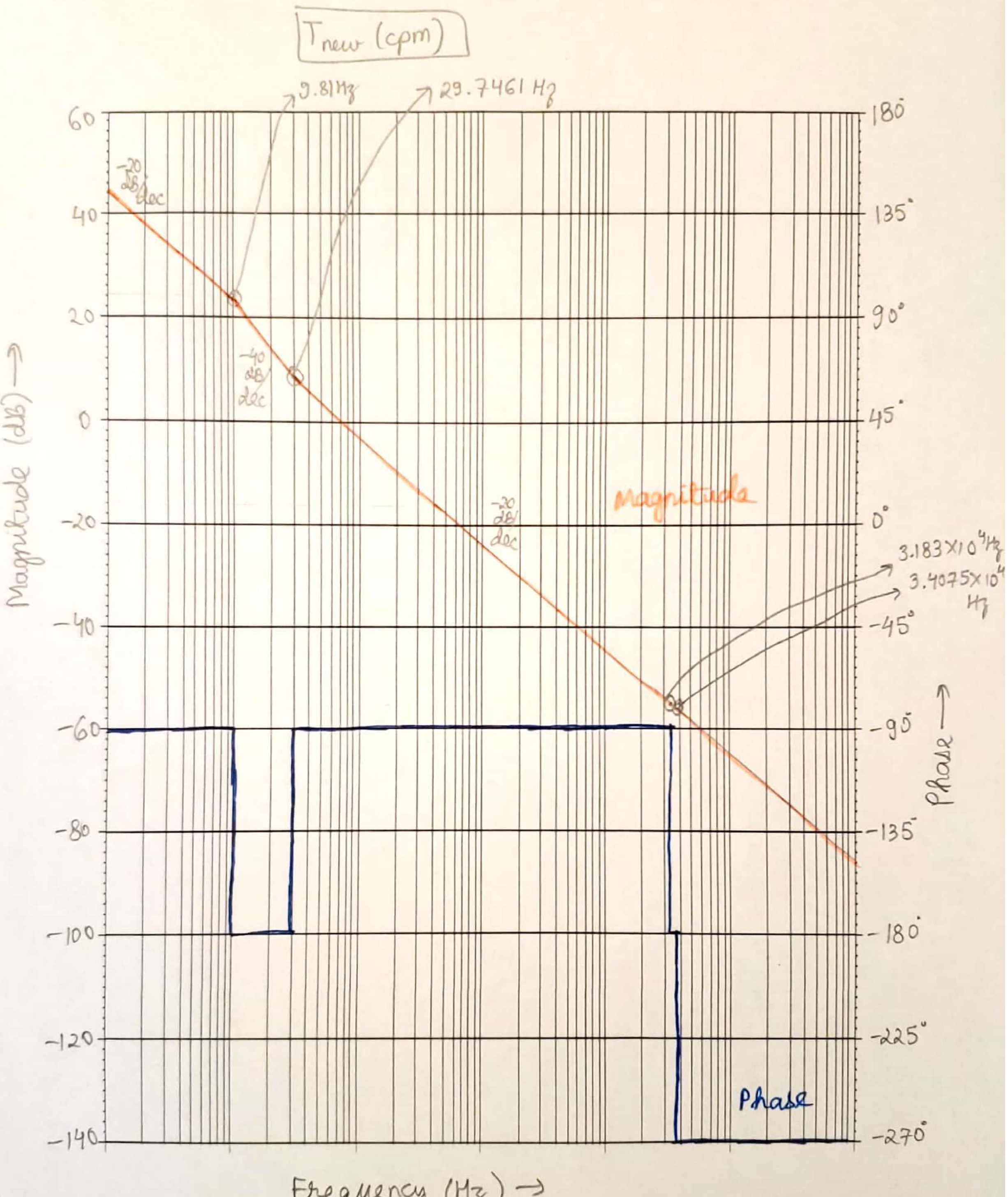
b. **Final design:** The final design can be improved by making a better controller design for the peak mode.

This is done by using the PID tuner in MATLAB to obtain a phase margin of $60°$ and bandwidth of $20\ Hz$ for the compensated loop. The new controller is obtained as:

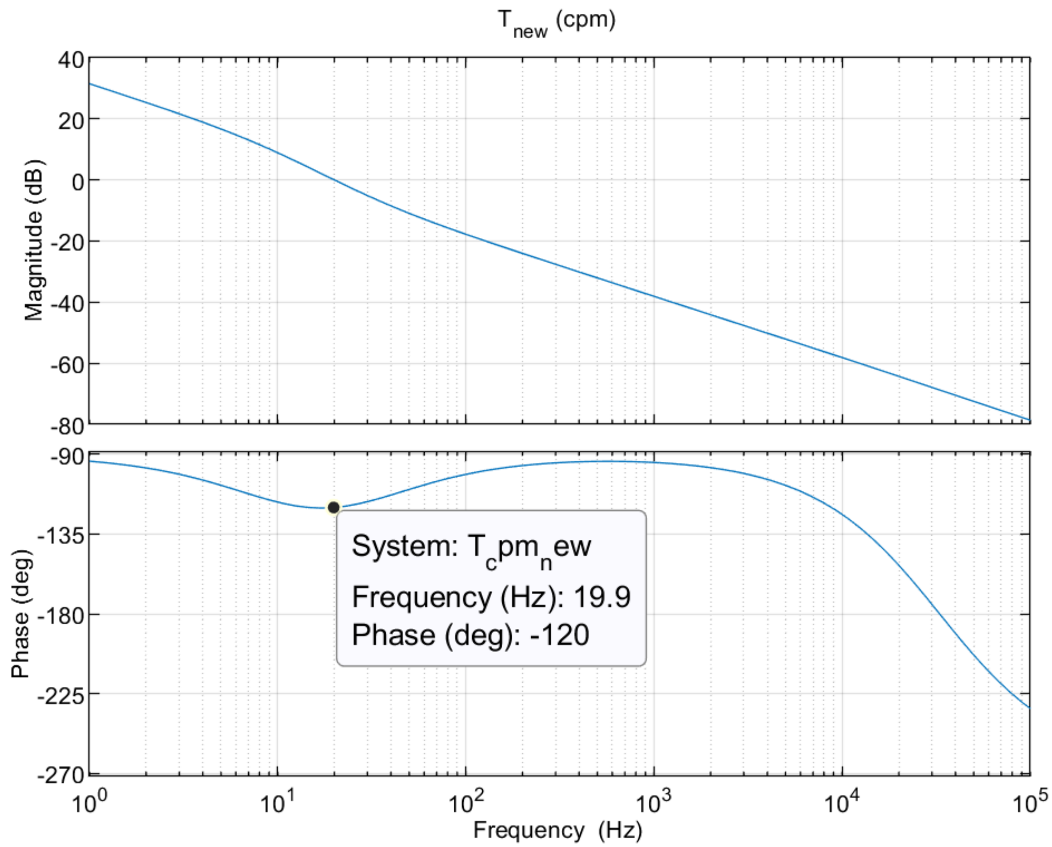
$$G_{cv(cpm),new} = \frac{0.2263s + 42.3}{0.00535s}$$

This gives the new compensated loop gain as:

$$T_{cpm,new} = -73.08\frac{(s - 2.141 * 10^5)(s + 186.9)}{s(s + 2 * 10^5)(s + 61.66)}$$

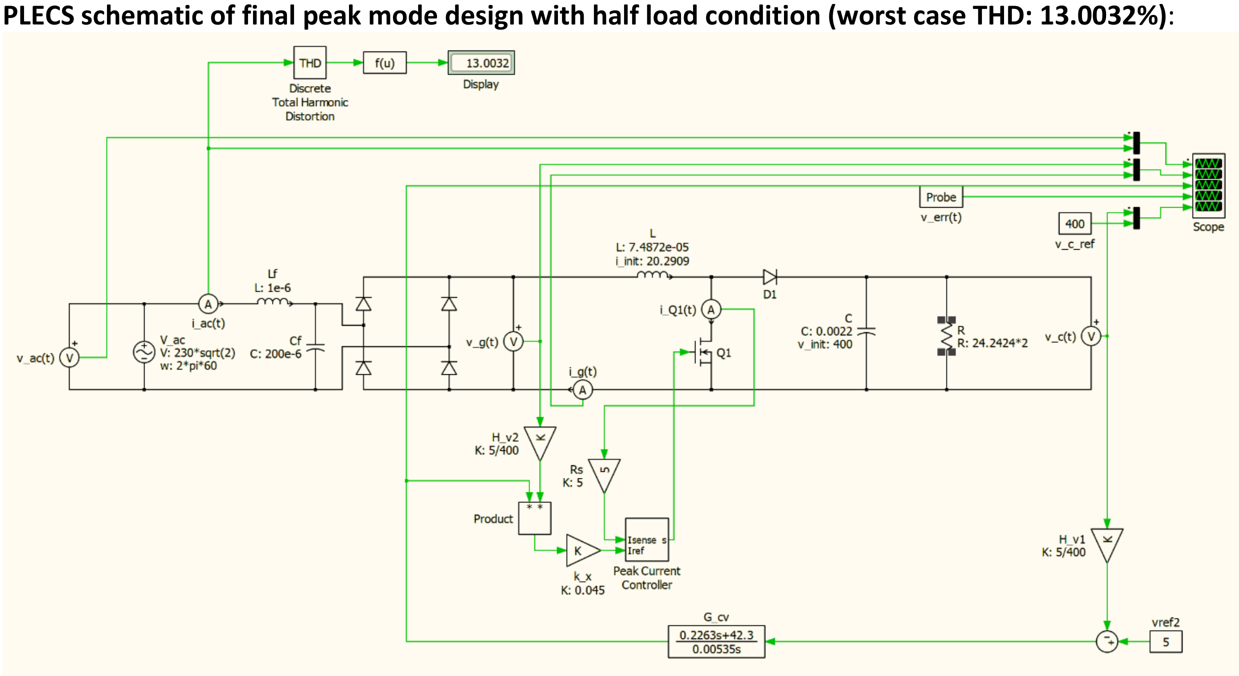


T new (cpm)
9.81 Hz
29.7461 Hz
-20 dB/dec
-40 dB/dec
-20 dB/dec
Magnitude
3.183×10^4 Hz
3.4075×10^4 Hz
Phase
Magnitude (dB) →
Phase →
Frequency (Hz) →
60
40
20
0
-20
-40
-60
-80
-100
-120
-140
180°
135°
90°
45°
0°
-45°
-90°
-135°
-180°
-225°
-270°

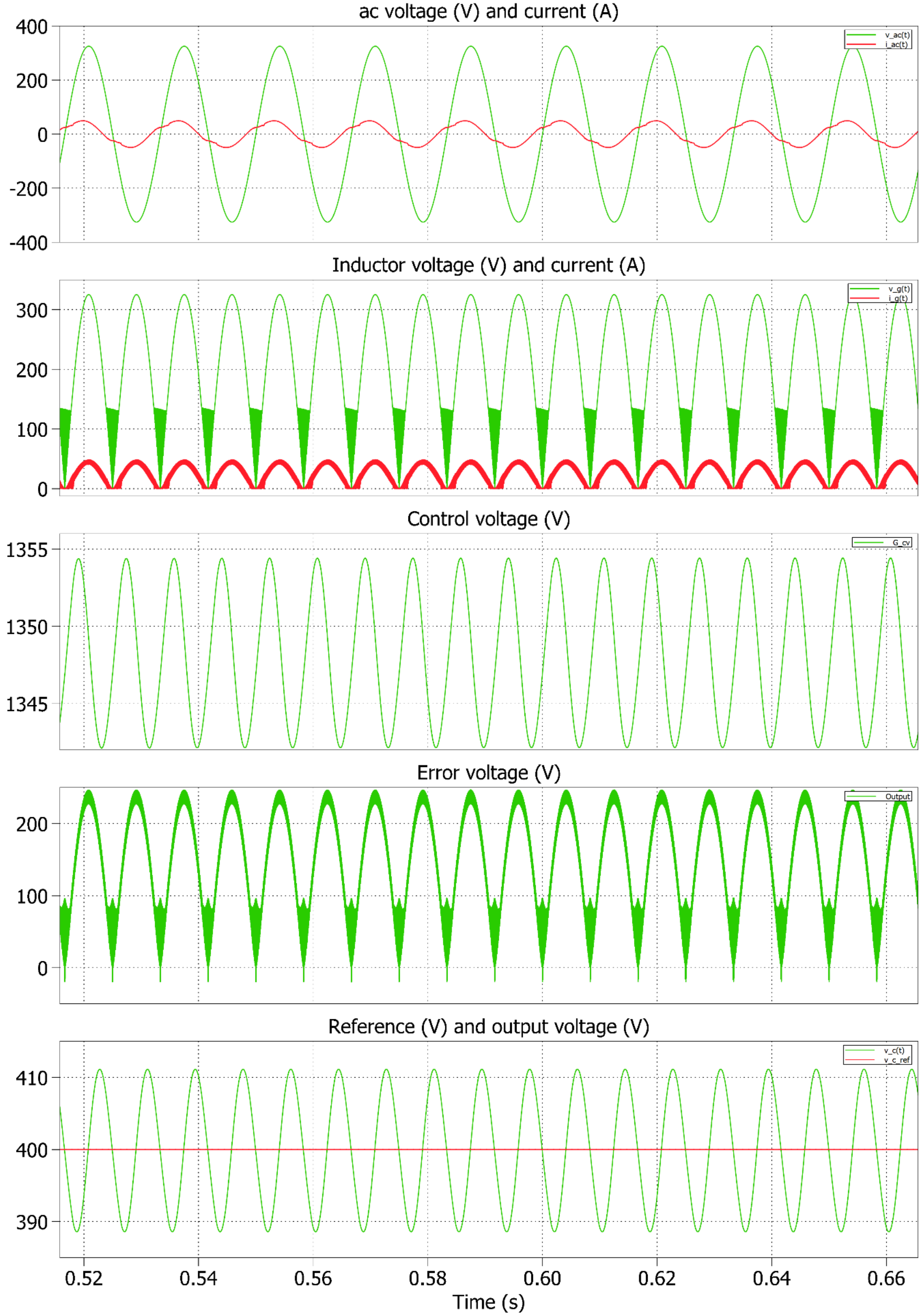


We now use $R_s = 5\ \Omega$ and an input filter with $L_{f1} = 1\mu H$ and $C_{f1} = 200\mu F$ for improved THD.

PLECS schematic of final peak mode design with half load condition (worst case THD: 13.0032%):



Full load steady state voltages and currents with final peak mode design:



4. **Conclusion:** Usual diode bridge rectifiers (DBRs) have a large ripple in the dc output voltage and discontinuous input currents with very high THD, thereby drastically reducing the power factor. The boost PFC rectifier comprises a dc-dc converter cascaded to the output of a DBR, a topology with only one active MOSFET switch which can be used in active power factor correction. It has a higher voltage at the output than the peak of the input ac voltage, because of which boost and buck-boost are the only possible dc-dc converters which can be used. The boost PFC typically has higher efficiency and is more commonly used than the buck-boost topology.

   In the presence of active power factor correction, the input current becomes continuous and sinusoidal which improves the power factor and THD, and increases the efficiency. The CCM boost converter designed in this project is driven by a controller which causes the input current to follow the input voltage and the output voltage to follow a voltage reference. The design of the two control loops for voltage and current are done keeping in mind the quasi-static approximation: the ac line variations are much slower than the converter dynamics, hence the rectifier always operates close to equilibrium. The current control loop has a much higher bandwidth and therefore operates much faster than the voltage loop.

   It is seen that upon designing suitable current and voltage loop compensators and appropriately adjusting the value of the multiplier k_x, we can get below 1% worst case (half load) THD in the average current mode control with an input filter that is not too big. However, the peak mode control witnesses much higher THD of about 13% in the worst case (half load) even with a filter. The values of $v_{err}(t)$ are found to be significantly higher in peak current mode control compared to average current mode control. The latter is able to control the power factor by supplying the required harmonic current, thereby eliminating harmonics from the ac side input current. But in peak current control, the peak current follows the reference sinusoidal wave while the average current does not. This causes large error in the control loop and high THD. [5]

   The THD of the input current in both topologies is affected by the size of the inductor used in the boost PFC rectifier. In this project, the minimum size inductance is used, keeping in mind the space constraints posed by inductors in an actual circuit. However, in absence of such space constraints, a larger inductor may be used to significantly decrease the THD.

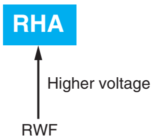
References

[1] Dr. John Schönberger, "Modeling a PFC controller using PLECS", Plexim GmbH [Online]. Available: https://www.plexim.com/sites/default/files/plecs_pfc.pdf
[2] S. Abdel-Rahman, F. Stückler, K. Siu, "PFC boost converter design guide", Infineon Technologies [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote_PFCCCMBoostConverterDesignGuide-AN-v02_00-EN.pdf?fileId=5546d4624a56eed8014a62c75a923b05
[3] R. Erickson, D. Maksimović , "Fundamentals of Power Electronics", 2nd ed., Kluwer Academic Publishers, 2004
[4] R. Erickson, D. Maksimović, K. Afridi, "Power Electronics Specialization", Coursera [Online]. Available: https://www.coursera.org/specializations/power-electronics
[5] Dhivya A, Murali D, "Average Current Mode Control Technique Applied to Boost Converter for Power factor Improvement and THD Reduction", International Journal of Innovative Science, Engineering and Technology, vol. 3 no. 2, Feb 2016, pp. 267-275

Appendix

RHA Series

- Realized higher voltage than RWF series (500 to 650Vdc)
- Endurance with ripple current : 5,000 hours at 85℃
- Suitable for high voltage inverter
- RoHS2 compliant

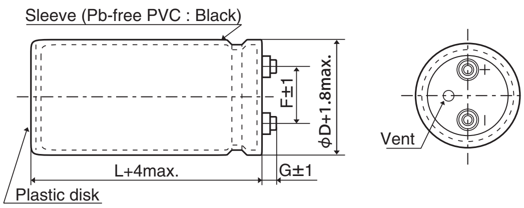


◆SPECIFICATIONS

Items	Characteristics		
Category Temperature Range	-25 to +85℃		
Rated Voltage Range	500 to 650Vdc		
Capacitance Tolerance	±20% (M)		(at 20℃, 120Hz)
Leakage Current	I=0.02CV or 5mA, whichever is smaller. Where, I : Max. leakage current (µA), C : Nominal capacitance (µF), V : Rated voltage (V)		(at 20℃ after 5 minutes)
Dissipation Factor (tan δ)	0.25 max.		(at 20℃, 120Hz)
Low Temperature Characteristics	Capacitance change C(-25℃)/C(+20℃)≧0.6		(at 120Hz)
Insulation Resistance	When measured between the terminals that are connected to each other and to the mounting clamp on the insulating sleeve covering the case by using an insulation resistance meter of 500Vdc, the insulation resistance shall not be less than 100MΩ.		
Insulation Withstanding Voltage	When a voltage of 2,000Vac is applied for 1 minute between the terminals that are connected to each other and to the mounting clamp on the insulating sleeve covering the case, there shall not be electrical damage.		
Endurance	The following specifications shall be satisfied when the capacitors are restored to 20℃ after subjected to DC voltage with the rated ripple current is applied (the peak voltage shall not exceed the rated voltage) for 5,000 hours at 85℃.		
	Capacitance change	≦±20% of the initial value	
	D.F. (tan δ)	≦200% of the initial specified value	
	Leakage current	≦The initial specified value	
Shelf Life	The following specifications shall be satisfied when the capacitors are restored to 20℃ after exposing them for 500 hours at 85℃ without voltage applied. Before the measurement, the capacitor shall be preconditioned by applying voltage according to Item 4.1 of JIS C 5101-4.		
	Capacitance change	≦±20% of the initial value	
	D.F. (tan δ)	≦200% of the initial specified value	
	Leakage current	≦The initial specified value	

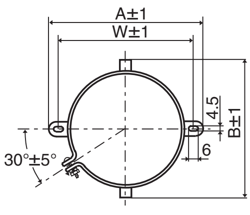
◆DIMENSIONS (Screw-Mount) [mm]

●Terminal Code : LG



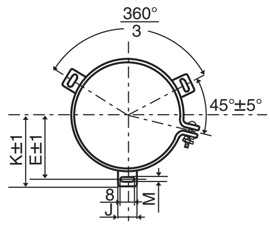
ϕ50 & ϕ63.5 : G=6
ϕ76.2 & ϕ89 : G=5
ϕ100 : G=10

●Mounting Clamp Code : B



ϕD	A	B	W	F
50	78.0	64.0	68.0	22.4
63.5	90.0	76.0	80.0	28.0
76.2	104.5	90.0	93.5	31.5

●Mounting Clamp Code : C



ϕD	E	K	M	F	J
50	32.5	37.0	4.5	22.4	14.0
63.5	38.1	43.5	4.5	28.0	14.0
76.2	44.5	50.0	4.5	31.5	14.0
89	50.8	56.5	4.5	31.5	16.0
100	56.5	63.4	5.5	41.5	18.0

<Screw specifications>

to ϕ89 Plus hexagon-headed screw :M5X0.8X10
Maximum screw tightening torque :3.23Nm

ϕ100 Cross-recessed head (phillips) screw : M8X1.25X16
Spring washer,Washer
Maximum screw tightening torque :6.31Nm

* The screw and the mounting clamp are separately supplied and not attached to the product.

◆PART NUMBERING SYSTEM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
E RHA □□□ LG □ □□□ M □□□ U

- Supplement code
- Size code
- Capacitance tolerance code
- Capacitance code (ex. 6,800µF:682, 12,000µF:123)
- Mounting clamp code (N, B, C)
- Terminal code
- Voltage code (ex. 500V:501, 650V:651)
- Series code
- Category

Please refer to "Product code guide (screw-mount terminal type)"

RHA Series

◆STANDARD RATINGS

WV (V_{dc})	Cap (μF)	Case size ϕD×L(mm)	tan δ	Rated ripple current (Arms/ 85℃,120Hz)	Part No.
500	1,200	50×95	0.25	5.90	ERHA501LGC122MC95U
	1,500	50×115	0.25	7.20	ERHA501LGC152MCB5U
	1,800	50×130	0.25	8.30	ERHA501LGC182MCD0U
	2,200	50×150	0.25	9.80	ERHA501LGC222MCF0U
	2,700	63.5×120	0.25	11.2	ERHA501LGC272MDC0U
	3,300	63.5×140	0.25	13.3	ERHA501LGC332MDE0U
	3,900	63.5×170	0.25	15.7	ERHA501LGC392MDH0U
	3,900	76.2×130	0.25	15.4	ERHA501LGC392MED0U
	4,700	76.2×150	0.25	18.1	ERHA501LGC472MEF0U
	5,600	76.2×170	0.25	20.8	ERHA501LGC562MEH0U
	5,600	89×130	0.25	17.1	ERHA501LGC562MFD0U
	6,800	89×150	0.25	20.0	ERHA501LGC682MFF0U
	8,200	89×190	0.25	24.4	ERHA501LGC822MFK0U
	10,000	89×210	0.25	28.2	ERHA501LGC103MFM0U
	12,000	100×210	0.25	32.9	ERHA501LGC123MGM0U
	15,000	100×250	0.25	39.8	ERHA501LGC153MGR0U
550	1,000	50×95	0.25	5.40	ERHA551LGC102MC95U
	1,200	50×110	0.25	6.30	ERHA551LGC122MCB0U
	1,500	50×130	0.25	7.60	ERHA551LGC152MCD0U
	1,800	63.5×105	0.25	8.60	ERHA551LGC182MDA5U
	2,200	63.5×120	0.25	10.1	ERHA551LGC222MDC0U
	2,700	63.5×150	0.25	12.4	ERHA551LGC272MDF0U
	2,700	76.2×105	0.25	11.7	ERHA551LGC272MEA5U
	3,300	63.5×170	0.25	14.5	ERHA551LGC332MDH0U
	3,300	76.2×130	0.25	14.2	ERHA551LGC332MED0U
	3,900	76.2×140	0.25	15.9	ERHA551LGC392MEE0U
	4,700	76.2×170	0.25	19.1	ERHA551LGC472MEH0U
	4,700	89×130	0.25	15.6	ERHA551LGC472MFD0U
550	5,600	89×150	0.25	18.2	ERHA551LGC562MFF0U
	6,800	89×170	0.25	21.1	ERHA551LGC682MFH0U
	8,200	100×170	0.25	24.8	ERHA551LGC822MGH0U
	10,000	100×200	0.25	29.4	ERHA551LGC103MGL0U
600	1,200	63.5×95	0.25	6.70	ERHA601LGC122MD95U
	1,500	63.5×110	0.25	8.00	ERHA601LGC152MDB0U
	1,800	63.5×125	0.25	9.30	ERHA601LGC182MDC5U
	1,800	76.2×95	0.25	9.10	ERHA601LGC182ME95U
	2,200	63.5×145	0.25	11.0	ERHA601LGC222MDE5U
	2,200	76.2×110	0.25	10.8	ERHA601LGC222MEB0U
	2,700	63.5×170	0.25	13.1	ERHA601LGC272MDH0U
	2,700	76.2×125	0.25	12.6	ERHA601LGC272MEC5U
	3,300	76.2×145	0.25	14.9	ERHA601LGC332MEE5U
	3,900	76.2×170	0.25	17.3	ERHA601LGC392MEH0U
	3,900	89×130	0.25	14.2	ERHA601LGC392MFD0U
	4,700	76.2×190	0.25	20.0	ERHA601LGC472MEK0U
	4,700	89×150	0.25	16.6	ERHA601LGC472MFF0U
	5,600	89×170	0.25	19.1	ERHA601LGC562MFH0U
650	1,000	63.5×100	0.25	6.30	ERHA651LGC102MDA0U
	1,200	63.5×110	0.25	7.20	ERHA651LGC122MDB0U
	1,500	63.5×130	0.25	8.60	ERHA651LGC152MDD0U
	1,800	63.5×150	0.25	10.1	ERHA651LGC182MDF0U
	2,200	63.5×170	0.25	11.7	ERHA651LGC222MDH0U
	2,700	76.2×150	0.25	13.6	ERHA651LGC272MEF0U
	3,300	76.2×170	0.25	15.8	ERHA651LGC332MEH0U
	3,900	89×155	0.25	15.3	ERHA651LGC392MFF5U
	4,700	89×190	0.25	18.4	ERHA651LGC472MFK0U

◆RATED RIPPLE CURRENT MULTIPLIERS

◉Frequency Multipliers

Frequency (Hz)	50	120	300	1k	3k
Coefficient	0.8	1.0	1.2	1.3	1.4

Note : The endurance of capacitors is reduced with internal heating produced by ripple current at the rate of halving the lifetime with every 5 to 10℃ rise. When long life performance is required in actual use, the rms ripple current has to be reduced. Also, for the RHA series capacitors, using them at operating voltage less than their rated voltage can extend their lifetime. For details, please contact a representative of Nippon Chemi-Con.

Mouser Electronics

Authorized Distributor

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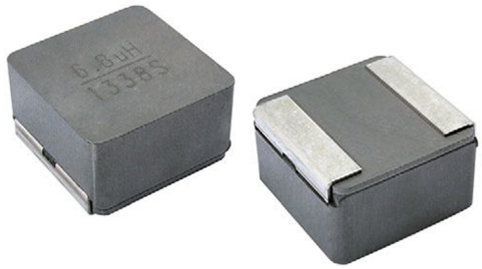
United Chemi-Con (UCC):

ERHA651LGC332MEH0M ERHA551LGC392MEE0M ERHA501LGC182MCD0M ERHA551LGC332MED0M
ERHA651LGC472MFK0M ERHA551LGC822MGH0M ERHA501LGC123MGM0M ERHA501LGC332MDE0M
ERHA551LGC472MEH0M ERHA551LGC122MCB0M ERHA601LGC332MEE5M ERHA501LGC562MEH0M
ERHA551LGC102MC95M ERHA651LGC392MFF5M ERHA601LGC182ME95M ERHA601LGC392MEH0M
ERHA501LGC682MFF0M ERHA601LGC472MFF0M ERHA501LGC103MFM0M ERHA601LGC562MFH0M
ERHA651LGC272MEF0M ERHA651LGC152MDD0M ERHA551LGC103MGL0M ERHA551LGC222MDC0M
ERHA651LGC122MDB0M ERHA551LGC272MDF0M ERHA501LGC122MC95M ERHA651LGC102MDA0M
ERHA551LGC562MFF0M ERHA501LGC472MEF0M ERHA651LGC182MDF0M ERHA651LGC222MDH0M
ERHA551LGC182MDA5M ERHA551LGC152MCD0M ERHA601LGC272MDH0M ERHA601LGC272MEC5M
ERHA501LGC562MFD0M ERHA501LGC153MGR0M ERHA501LGC222MCF0M ERHA551LGC682MFH0M
ERHA501LGC272MDC0M ERHA601LGC222MEB0M ERHA501LGC822MFK0M ERHA601LGC392MFD0M
ERHA501LGC392MED0M ERHA601LGC152MDB0M ERHA501LGC152MCB5M ERHA501LGC392MDH0M
ERHA601LGC222MDE5M ERHA551LGC332MDH0M ERHA551LGC272MEA5M ERHA551LGC472MFD0M
ERHA601LGC182MDC5M ERHA601LGC472MEK0M ERHA601LGC122MD95M

IHLP® Automotive Inductors, High Temperature (155 °C) Series



DESIGN SUPPORT TOOLS click logo to get started

3D Models Available | Design Tools Available

STANDARD ELECTRICAL SPECIFICATIONS

L_0 INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) (1)	SATURATION CURRENT DC TYP. (A) (2)	SRF TYP. (MHz)
0.47	0.56	0.67	80.0	100.0	47.5
1.0	0.82	0.89	69.0	71.0	25.7
2.2	1.23	1.25	58.0	48.0	17.5
3.3	1.63	1.77	49.0	41.0	12.8
4.7	1.69	1.84	47.0	37.0	10.2
6.8	2.84	3.09	36.0	36.0	8.03
10	4.04	4.14	28.0	28.0	6.04
15	5.62	6.11	23.5	24.0	4.71
22	10.60	10.80	17.5	16.0	3.88
33	15.10	15.40	15.5	10.5	3.01
47	17.30	17.70	13.5	10.0	2.99
75	29.76	32.35	10.6	9.5	2.01
82	31.46	34.20	10.2	9.0	2.07
100	36.25	39.40	9.1	7.0	2.01

Notes
- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +155 °C
- The part temperature (ambient + temp. rise) should not exceed 155 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application
- Rated operating voltage (across inductor) = 75 V

(1) DC current (A) that will cause an approximate ΔT of 40 °C
(2) DC current (A) that will cause L_0 to drop approximately 20 %

FEATURES

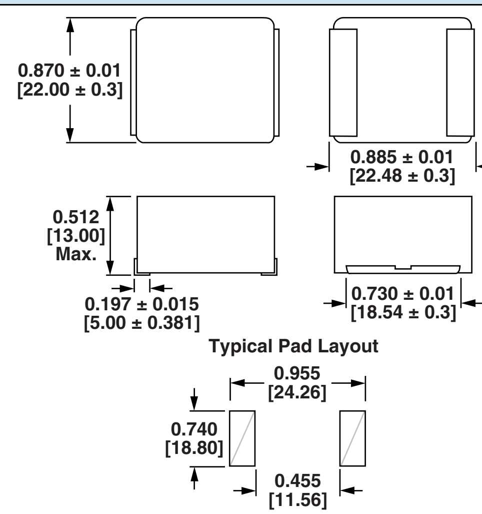
- High temperature rating, up to 155 °C
- Shielded construction
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up the SRF (see Standard Electrical Specifications table).
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- AEC-Q200 qualified
- IHLP design. PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

APPLICATIONS

- Engine and transmission control units
- Diesel injection drivers
- DC/DC converters for entertainment / navigation systems
- Noise suppression for motors: windshield wipers / power seats / power mirrors / heating and ventilation blower / HID lighting
- LED drivers

DIMENSIONS in inches [millimeters]



DESCRIPTION

IHLP-8787MZ-5A	100 µH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC® LEAD (Pb)-FREE STANDARD

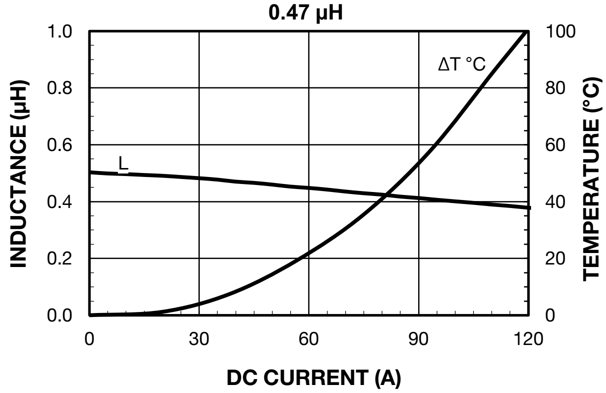
GLOBAL PART NUMBER

I	H	L	P	8	7	8	7	M	Z	E	R	1	0	1	M	5	A
PRODUCT FAMILY				SIZE						PACKAGE CODE		INDUCTANCE VALUE			TOL.	SERIES	

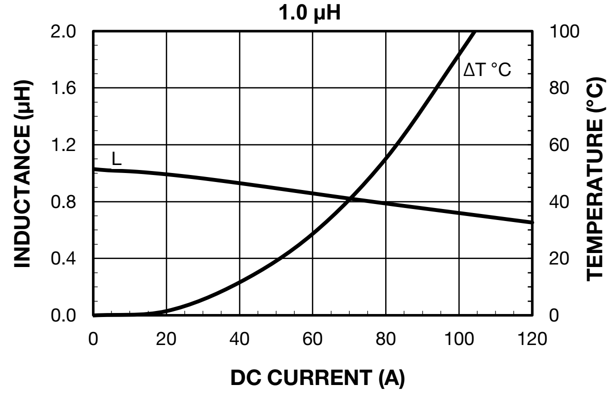
PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and international patents.

PERFORMANCE GRAPHS

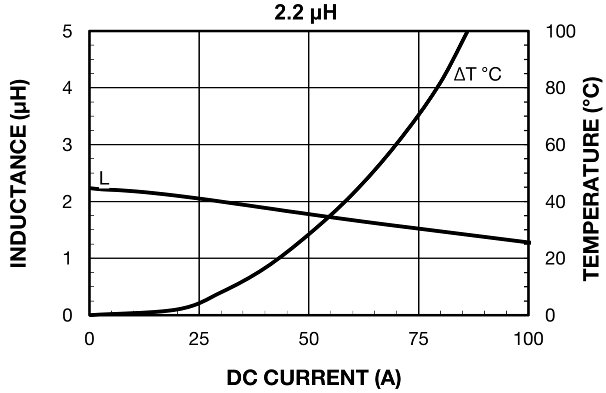
0.47 µH



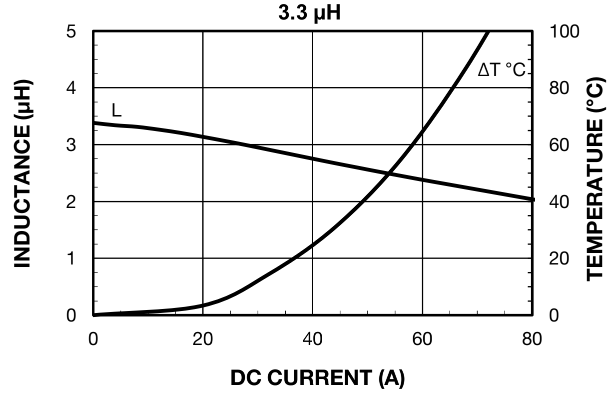
1.0 µH



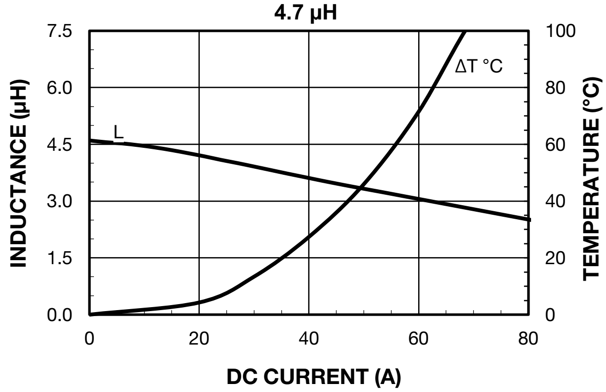
2.2 µH



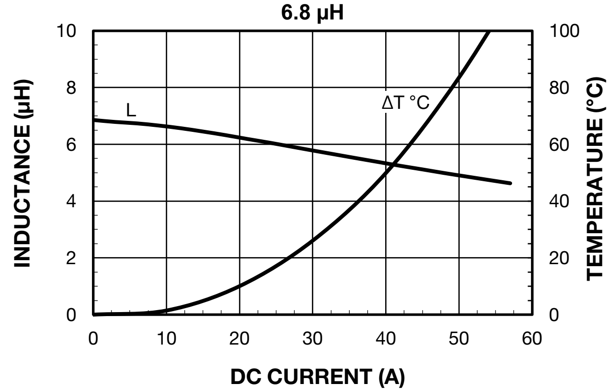
3.3 µH



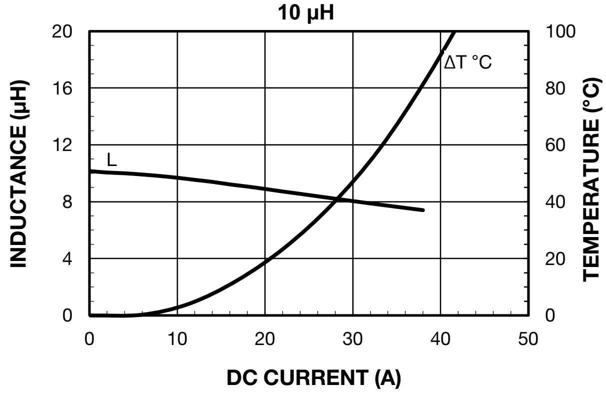
4.7 µH



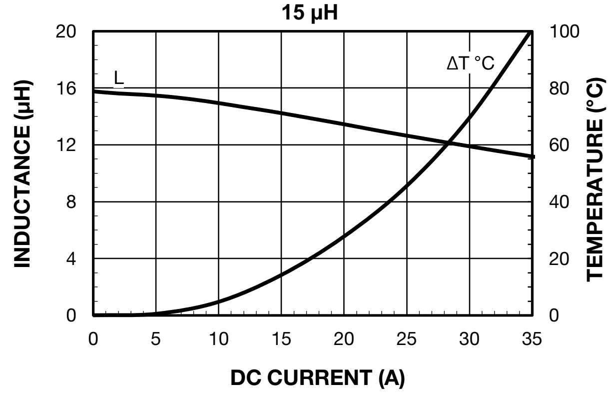
6.8 µH



10 µH



15 µH



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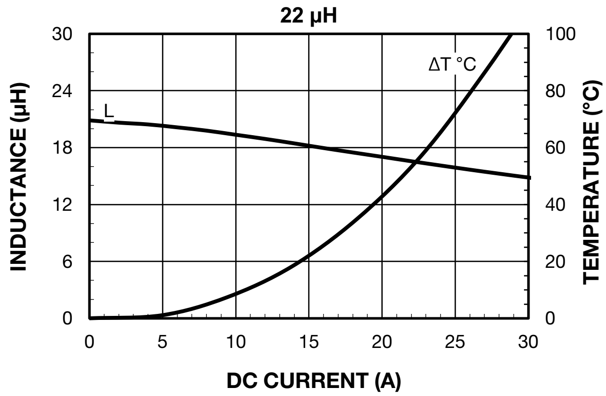
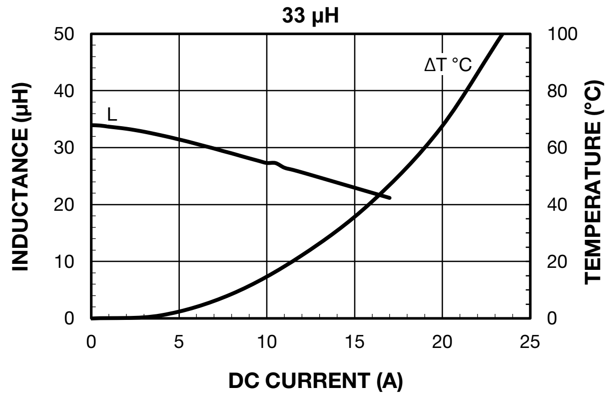
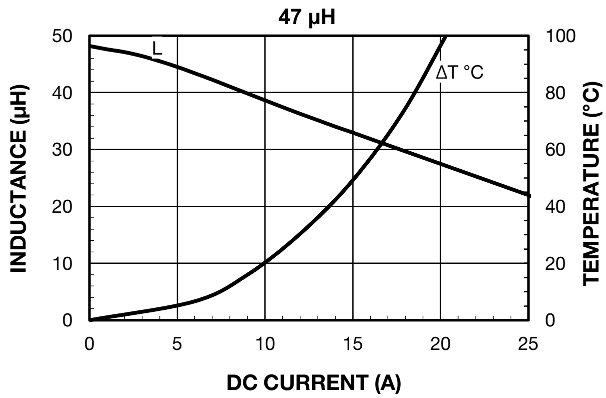
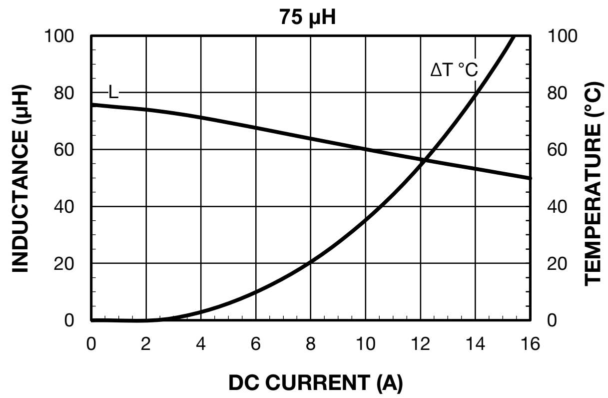
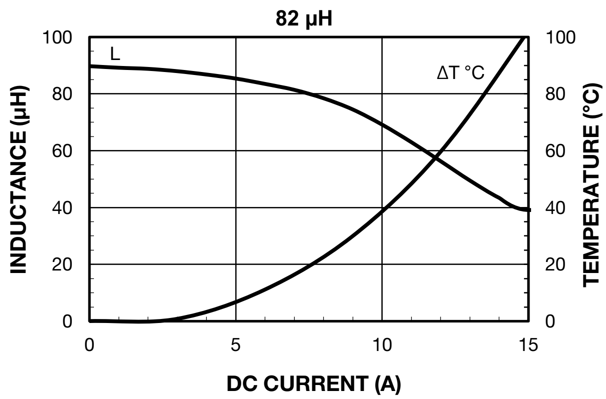
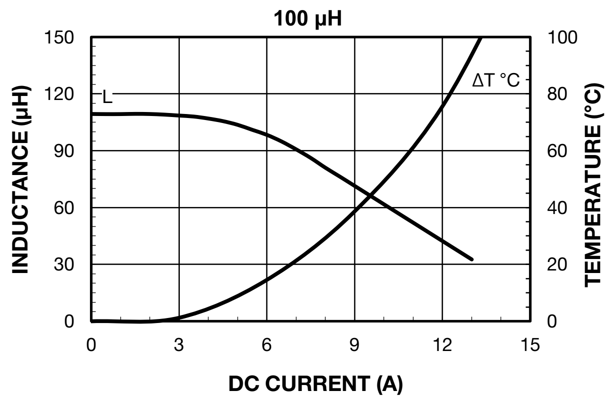








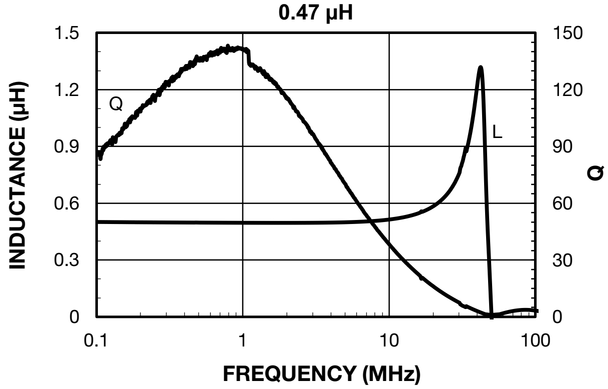




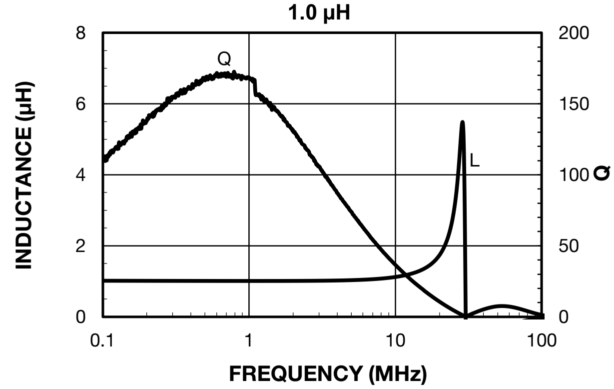
For technical questions, contact: magnetics@vishay.com

PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY

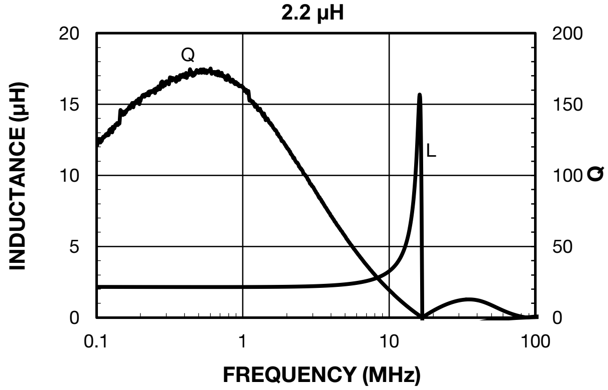
0.47 µH



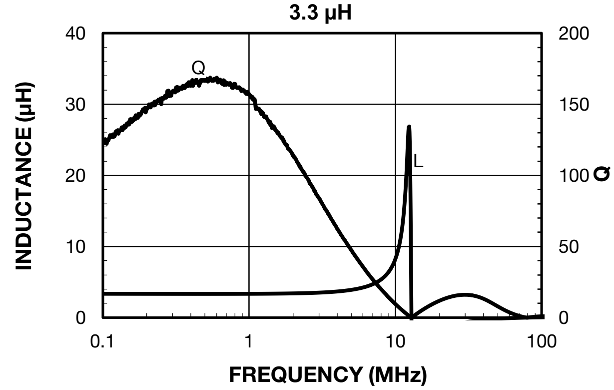
1.0 µH



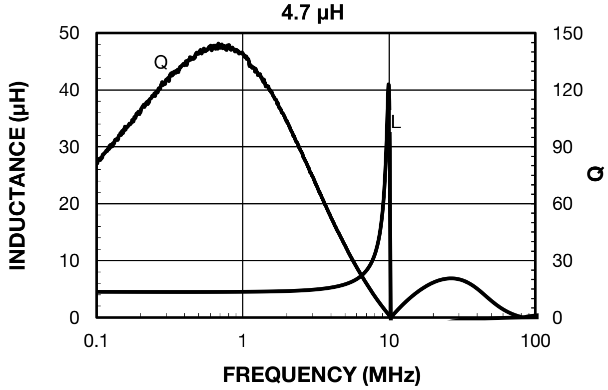
2.2 µH



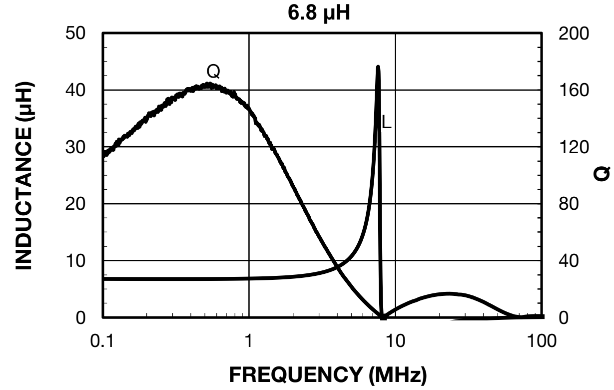
3.3 µH



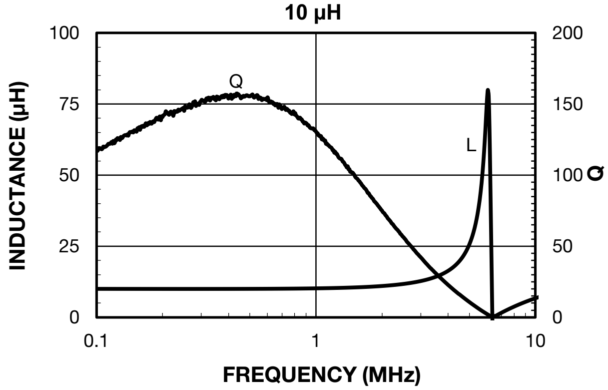
4.7 µH



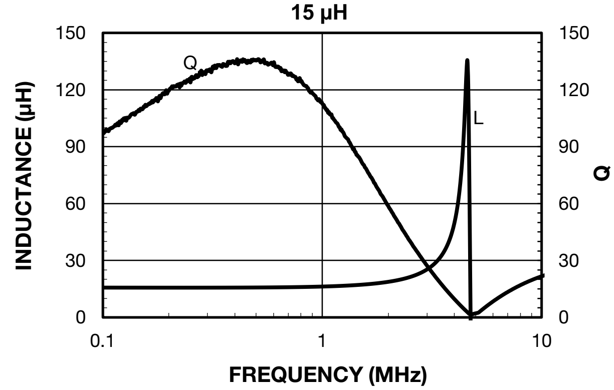
6.8 µH



10 µH

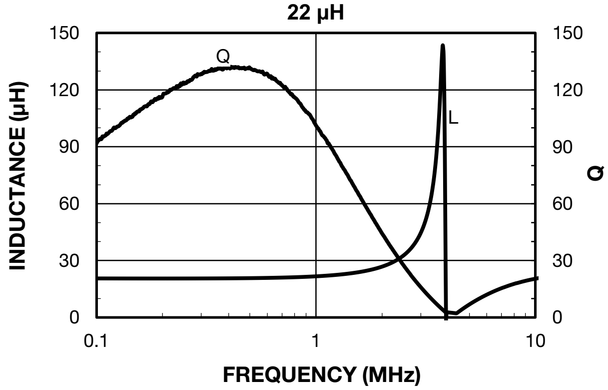


15 µH

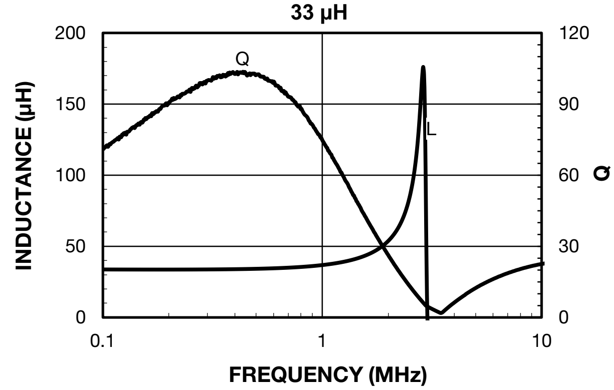


PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY

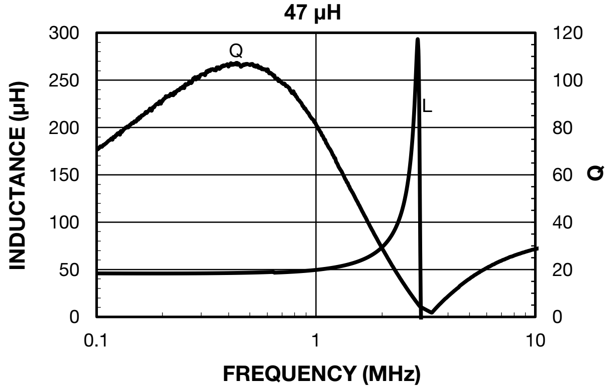
22 µH



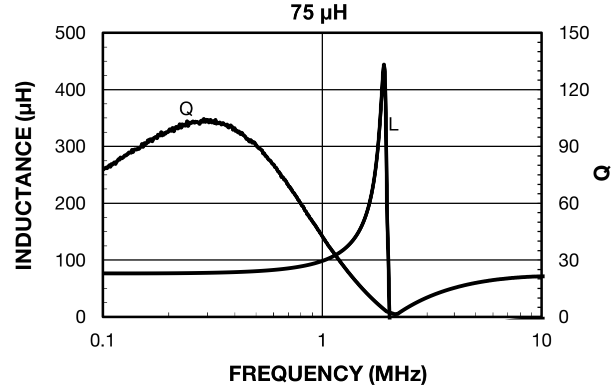
33 µH



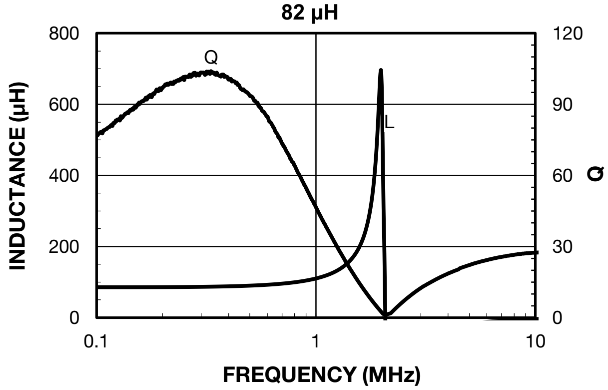
47 µH



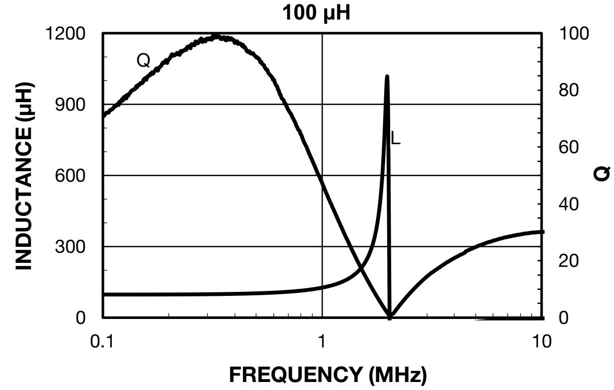
75 µH



82 µH



100 µH



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MOSFET

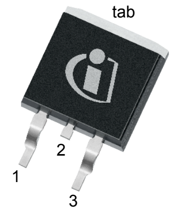
600V CoolMOS™ C7 Power Transistor

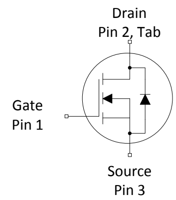
CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)}$*A below 1Ohm*mm².

D²PAK





Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g
- Best in class $R_{DS(on)}$ /package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Suitable for applications such as server, telecom and solar
- Higher switching frequencies possible without loss in efficiency due to low Eoss and Qg

Applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	40	mΩ
$Q_{g.typ}$	107	nC
$I_{D,pulse}$	211	A
$I_{D,continuous}$ @ T_j<150°C	73	A
E_{oss}@400V	12.6	µJ
Body diode di/dt	450	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPB60R040C7	PG-TO 263	60C7040	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	50 32	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	211	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	249	mJ	I_D=7.4A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	1.24	mJ	I_D=7.4A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	7.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	227	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	50	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	211	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	20	V/ns	V_{DS}=0...400V, I_{SD}<=11.4A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	450	A/µs	V_{DS}=0...400V, I_{SD}<=11.4A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.55	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=1.24mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.034 0.077	0.040 -	Ω	V_{GS}=10V, I_D=24.9A, T_j=25°C V_{GS}=10V, I_D=24.9A, T_j=150°C
Gate resistance	R_G	-	0.77	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4340	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	85	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	158	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	1640	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	18.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=24.9A, R_G=3.3Ω; see table 9
Rise time	t_r	-	11	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=24.9A, R_G=3.3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	81	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=24.9A, R_G=3.3Ω; see table 9
Fall time	t_f	-	3.2	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=24.9A, R_G=3.3Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	22	-	nC	V_{DD}=400V, I_D=24.9A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	36	-	nC	V_{DD}=400V, I_D=24.9A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	107	-	nC	V_{DD}=400V, I_D=24.9A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=400V, I_D=24.9A, V_{GS}=0 to 10V

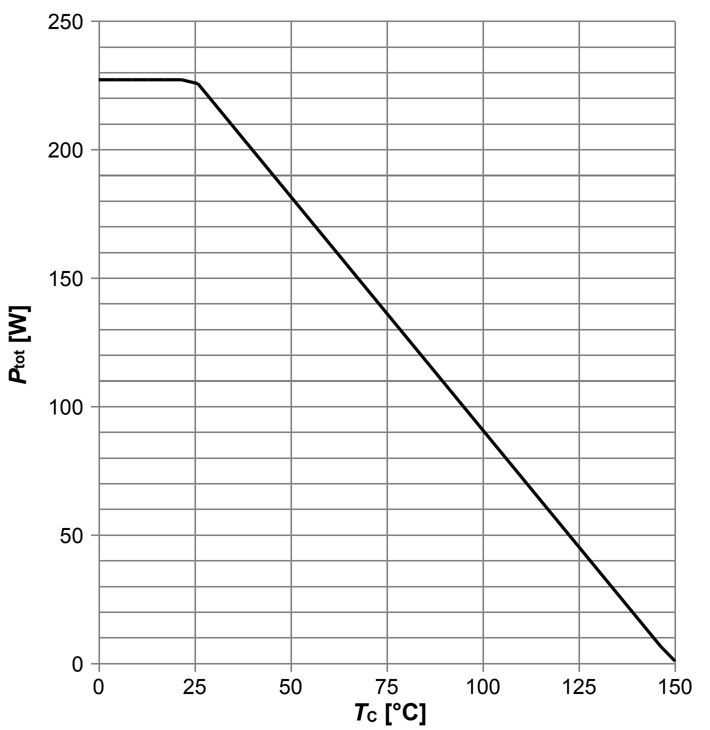
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=24.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	460	-	ns	V_R=400V, I_F=24.9A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	9.2	-	µC	V_R=400V, I_F=24.9A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	40	-	A	V_R=400V, I_F=24.9A, di_F/dt=100A/µs; see table 8

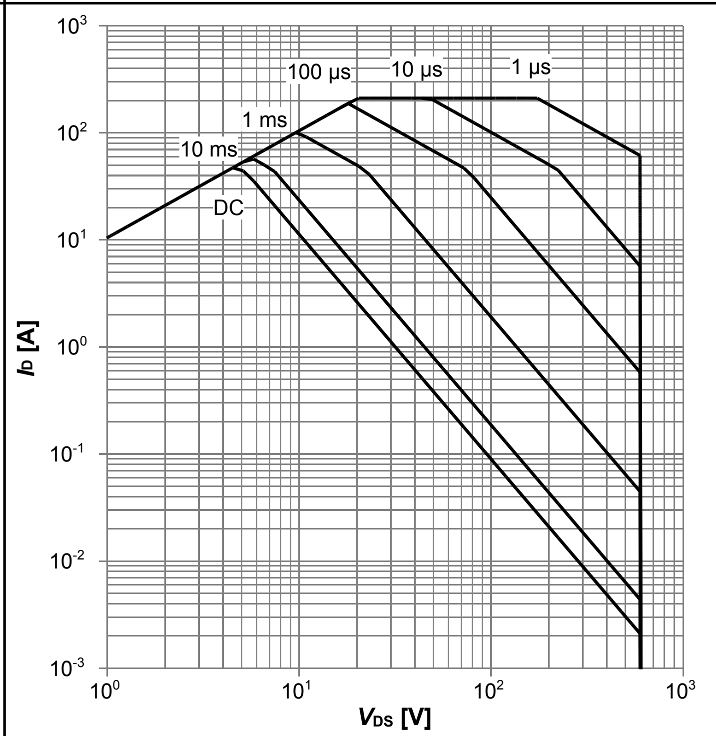
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



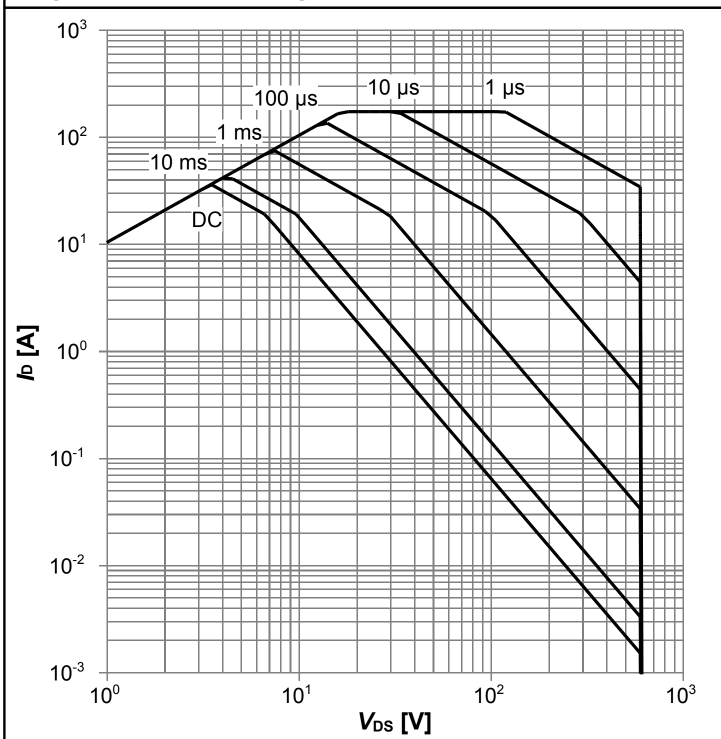
P_{tot}=f(T_C)

Diagram 2: Safe operating area



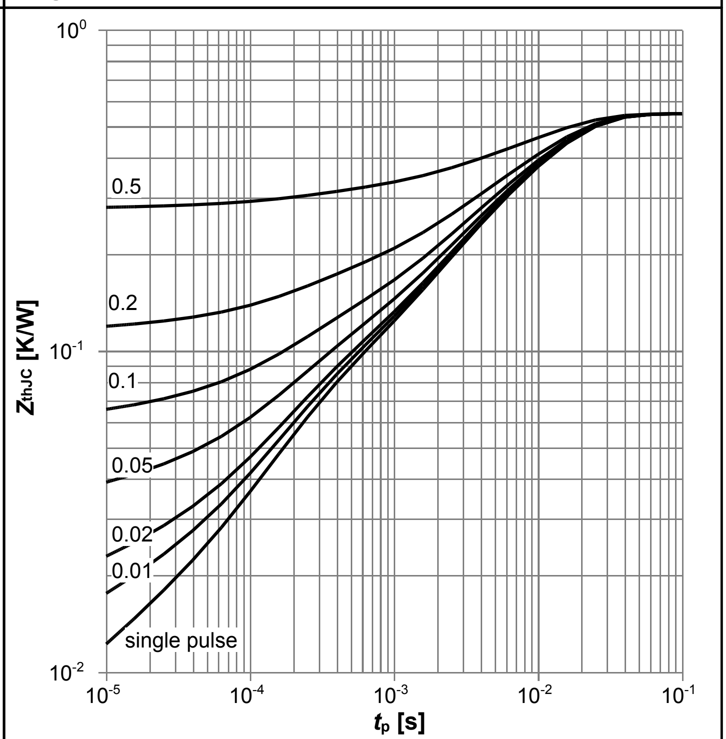
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



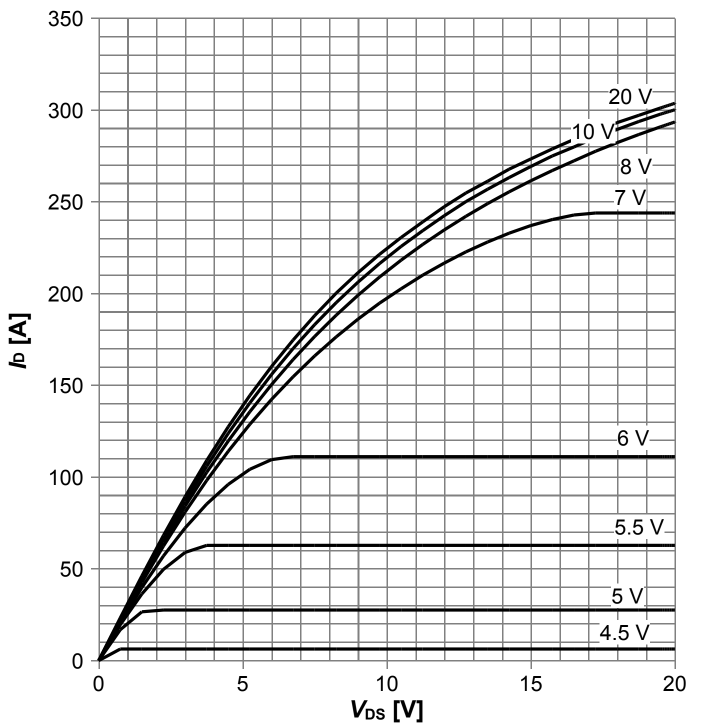
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



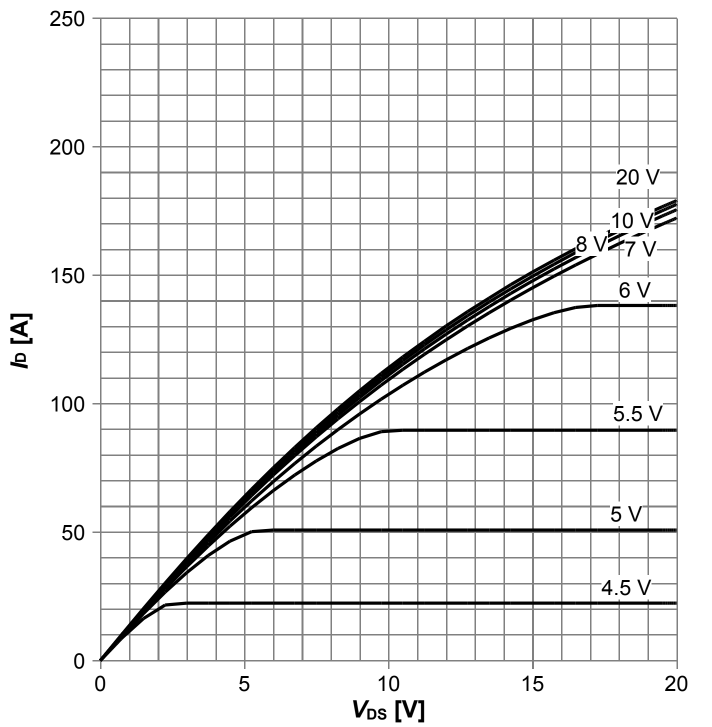
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



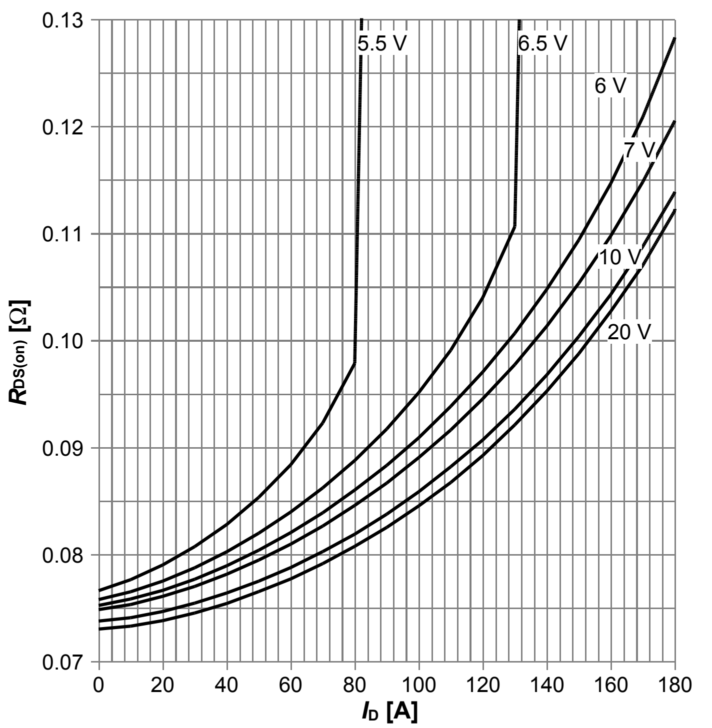
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



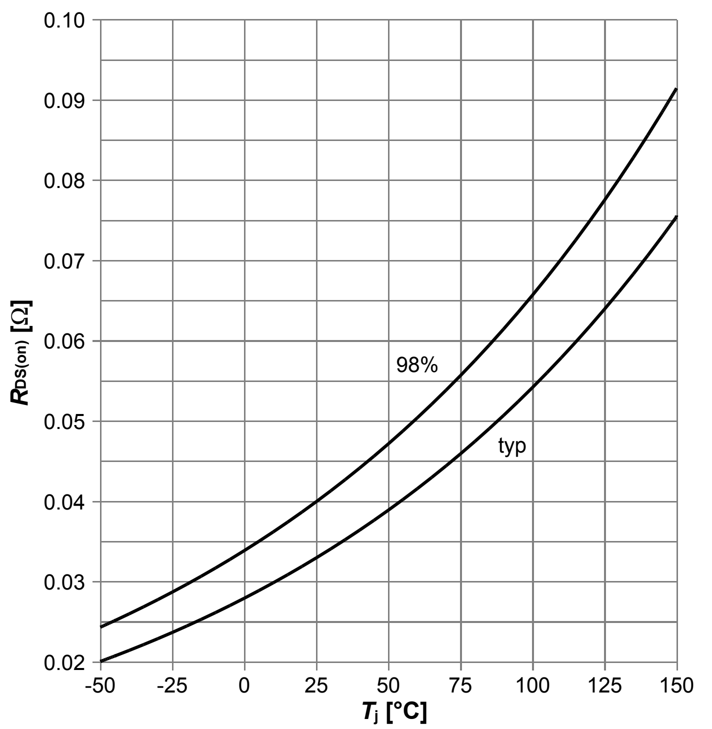
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



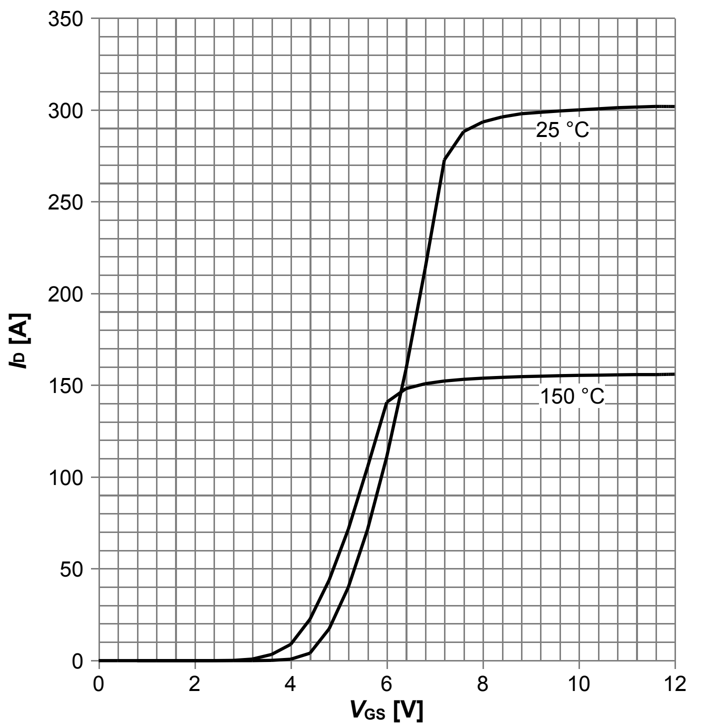
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



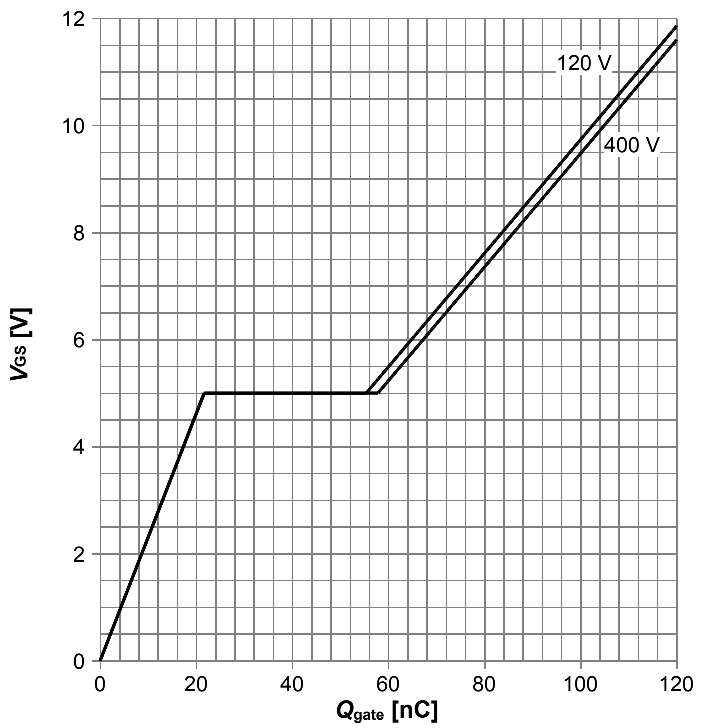
$R_{DS(on)}$=f(T_j); I_D=24.9 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



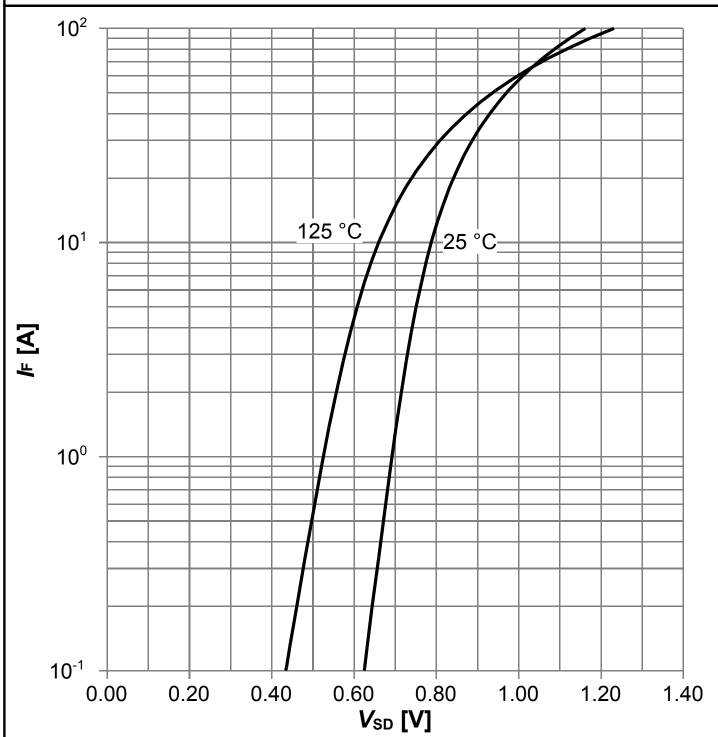
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



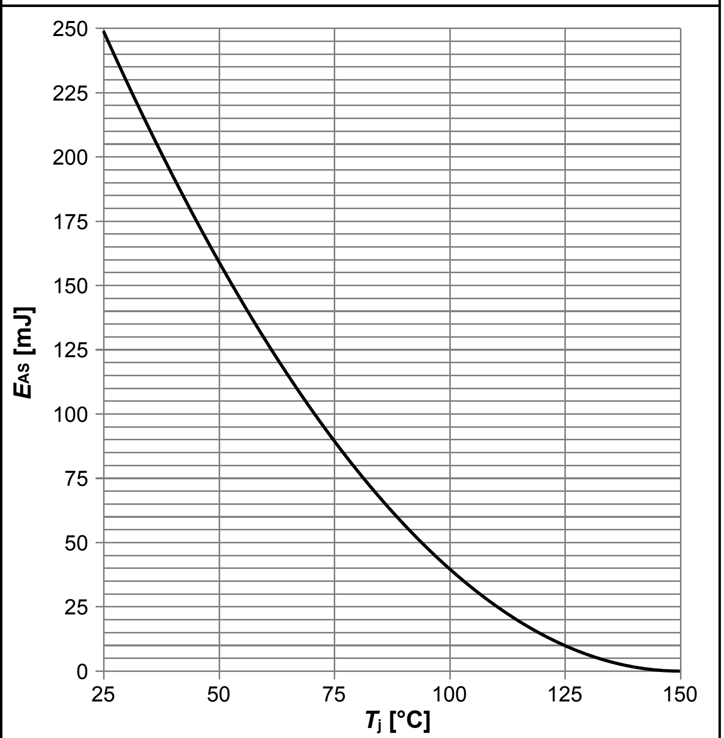
V_{GS}=f(Q_{gate}); I_D=24.9 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



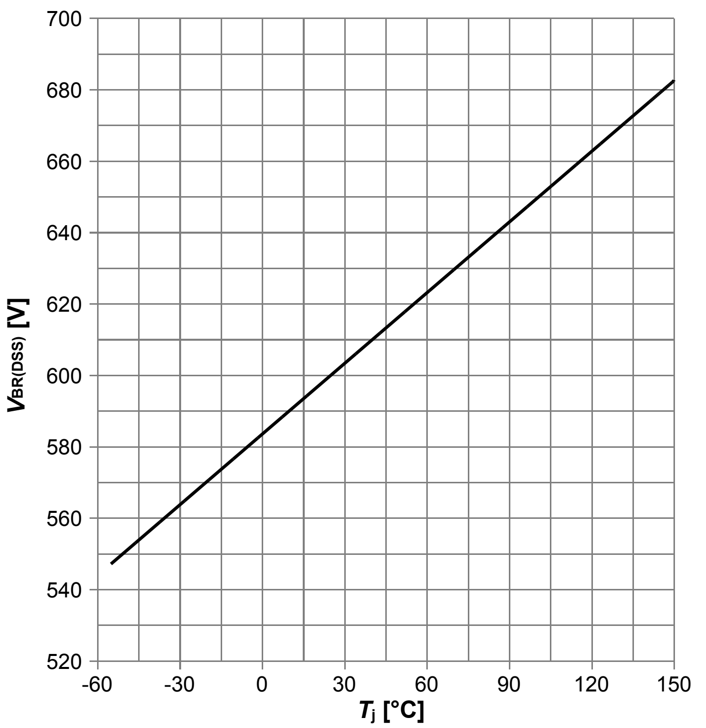
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



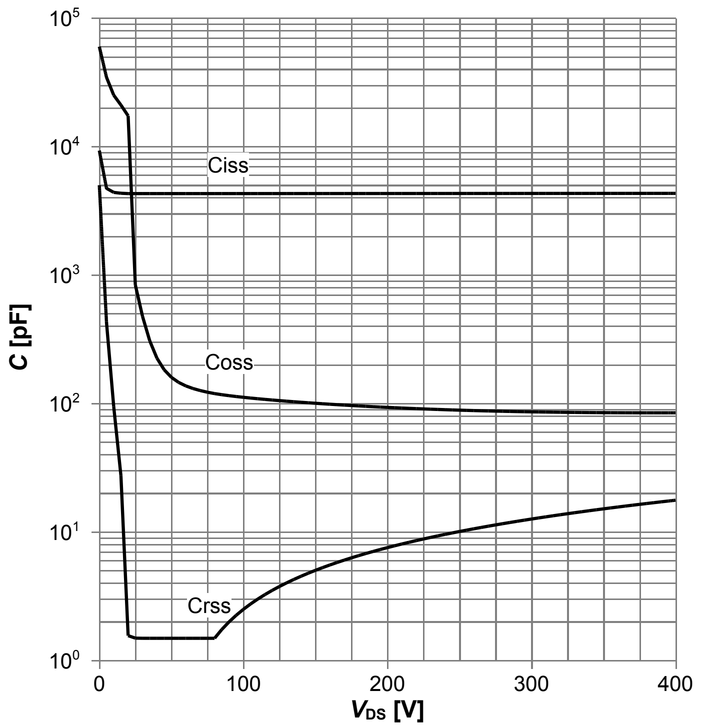
E_{AS}=f(T_j); I_D=7.4 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



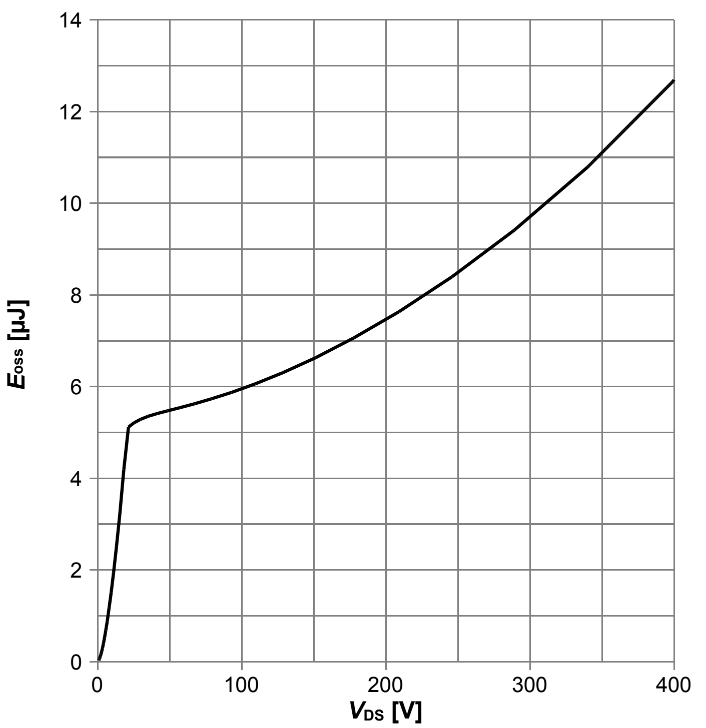
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

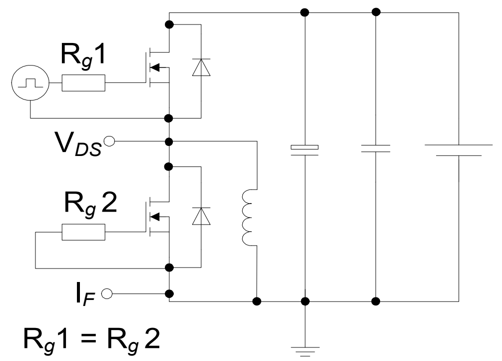
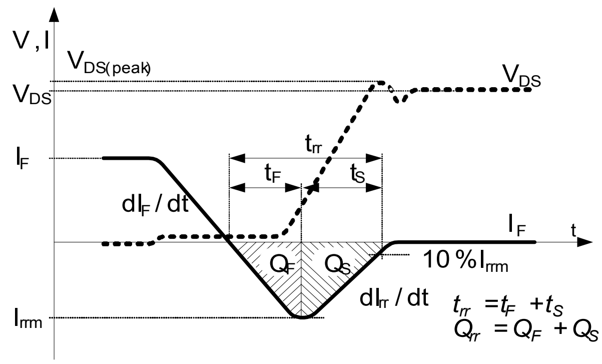
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

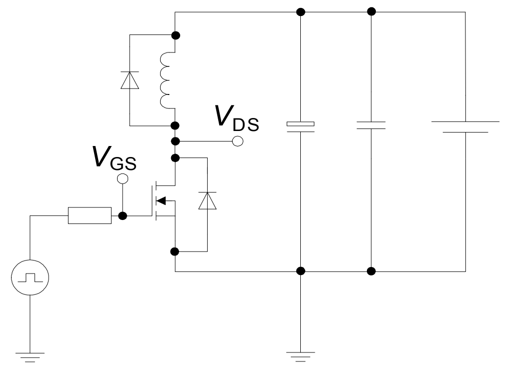
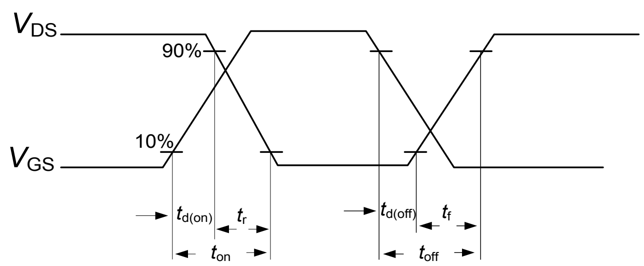
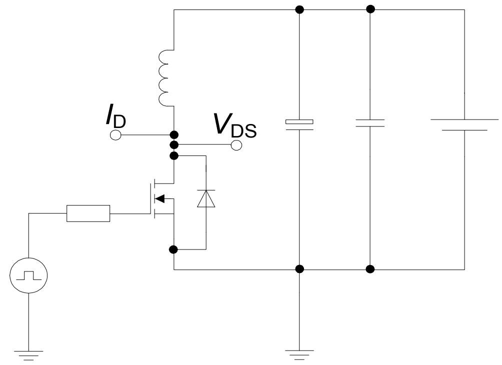
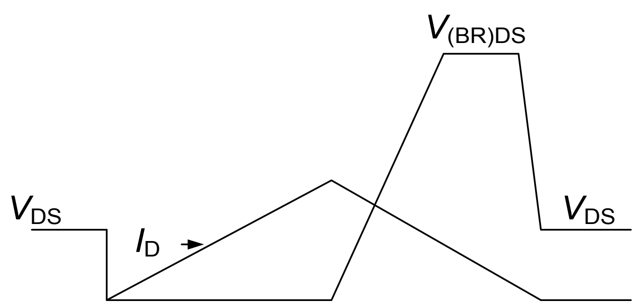
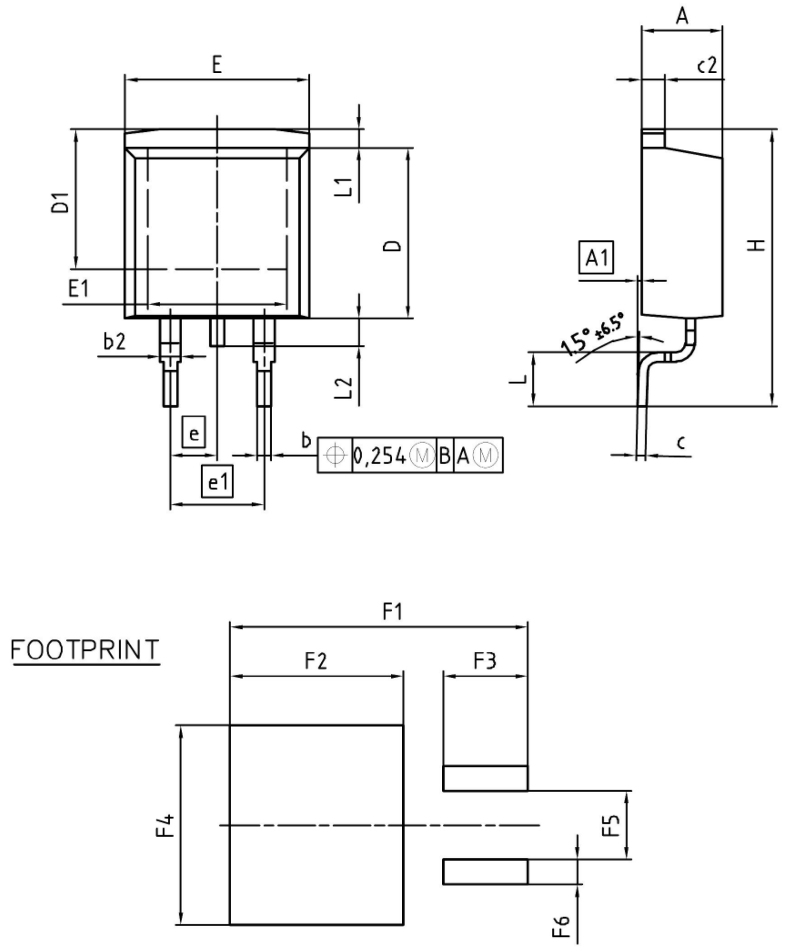
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO.
Z8B00003324

SCALE 0 5 0 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
30-08-2007

REVISION
01

Figure 1 Outline PG-TO 263, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS^{TM} C7 Webpage:** www.infineon.com
- **IFX CoolMOS^{TM} C7 application note:** www.infineon.com
- **IFX CoolMOS^{TM} C7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPB60R040C7

Revision: 2016-03-01, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2016-03-01	Release of final version

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CREE

C3D20060D

Silicon Carbide Schottky Diode

Z-Rec® Rectifier

V_{RRM}	=	600 V
I_F (T_C=135°C)	=	26 A**
Q_c	=	48 nC**

Features

- 600-Volt Schottky Rectifier
- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

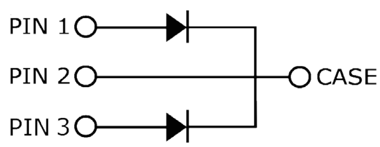
Package

TO-247-3

Halogen-Free

RoHS

AEC-Q101 Qualified



Part Number	Package	Marking
C3D20060D	TO-247-3	C3D20060

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	600	V		
V_{RSM}	Surge Peak Reverse Voltage	600	V		
V_{DC}	DC Blocking Voltage	600	V		
I_F	Continuous Forward Current (Per Leg/Device)	27.5/55 13/26 10/20	A	T_C=25°C T_C=135°C T_C=149°C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	46* 31*	A	T_C=25°C, t_P = 10 ms, Half Sine Wave T_C=110°C, t_P=10 ms, Half Sine Wave	
I_{FSM}	Non-Repetitive Peak Forward Surge Current	90* 71*	A	T_C=25°C, t_p = 10 ms, Half Sine Wave T_C=110°C, t_p = 10 ms, Half Sine Wave	Fig. 8
I_{FSM}	Non-Repetitive Peak Forward Surge Current	860* 680*	A	T_C=25°C, t_P = 10 µs, Pulse T_C=110°C, t_P = 10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation (Per Leg/Device)	136.5 59	W	T_C=25°C T_C=110°C	Fig. 4
dV/dt	Diode dV/dt ruggedness	200	V/ns	V_R=0-650V	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C		
	TO-247 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

* Per Leg, ** Per Device

Electrical Characteristics (Per Leg)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.5 2.0	1.8 2.4	V	I_F = 10 A T_J=25°C I_F = 10 A T_J=175°C	Fig. 1
I_R	Reverse Current	10 20	50 200	μA	V_R = 600 V T_J=25°C V_R = 600 V T_J=175°C	Fig. 2
Q_C	Total Capacitive Charge	24		nC	V_R = 400 V, I_F = 10 A di/dt = 500 A/μs T_J = 25°C	Fig. 5
C	Total Capacitance	460.5 44 40		pF	V_R = 0 V, T_J = 25°C, f = 1 MHz V_R = 200 V, T_J = 25°C, f = 1 MHz V_R = 400 V, T_J = 25°C, f = 1 MHz	Fig. 6
E_C	Capacitance Stored Energy	3.6		μJ	V_R = 400 V	Fig. 7

Note: This is a majority carrier diode, so there is no reverse recovery charge.

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.3** 0.65*	°C/W	Fig. 9

** Per Leg, * Both Legs

Typical Performance (Per Leg)

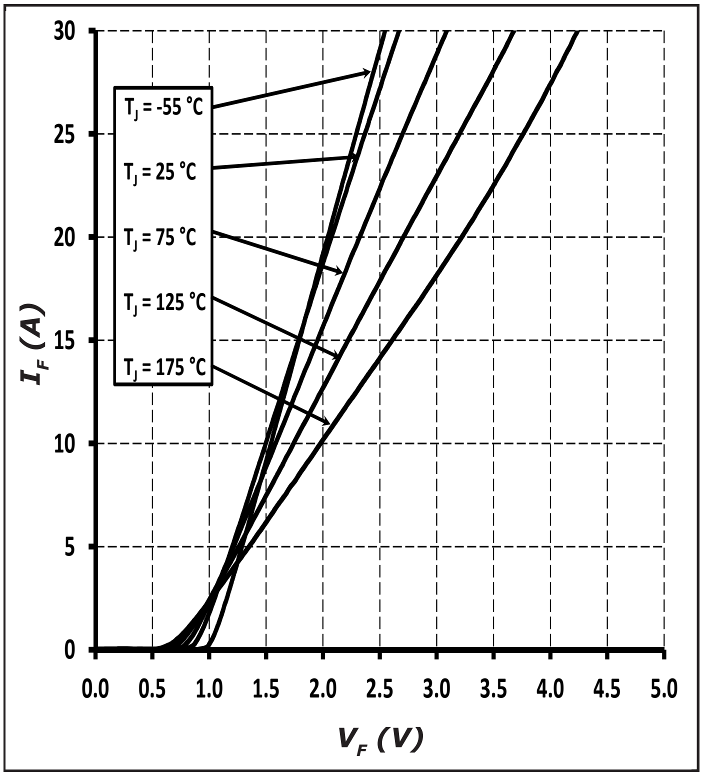


Figure 1. Forward Characteristics

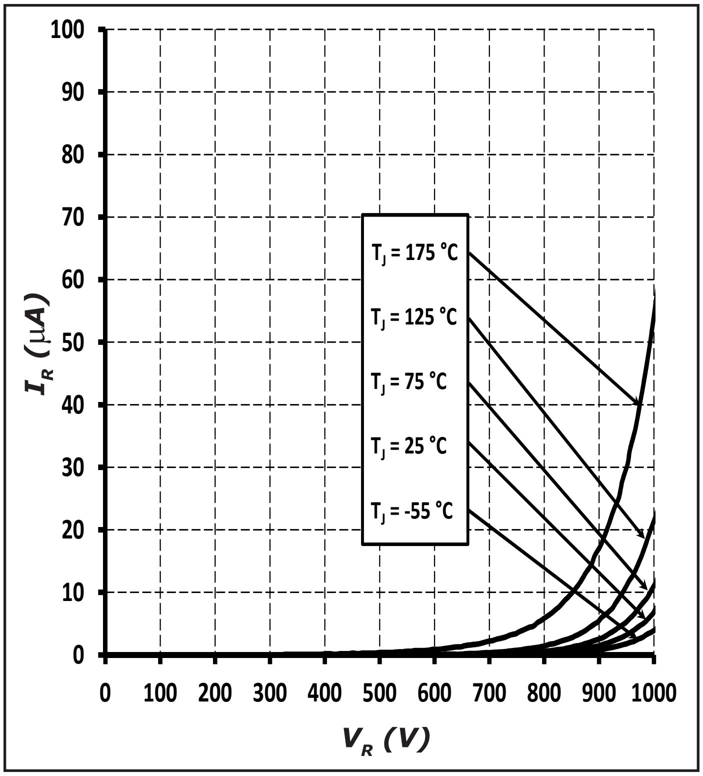


Figure 2. Reverse Characteristics

Typical Performance (Per Leg)

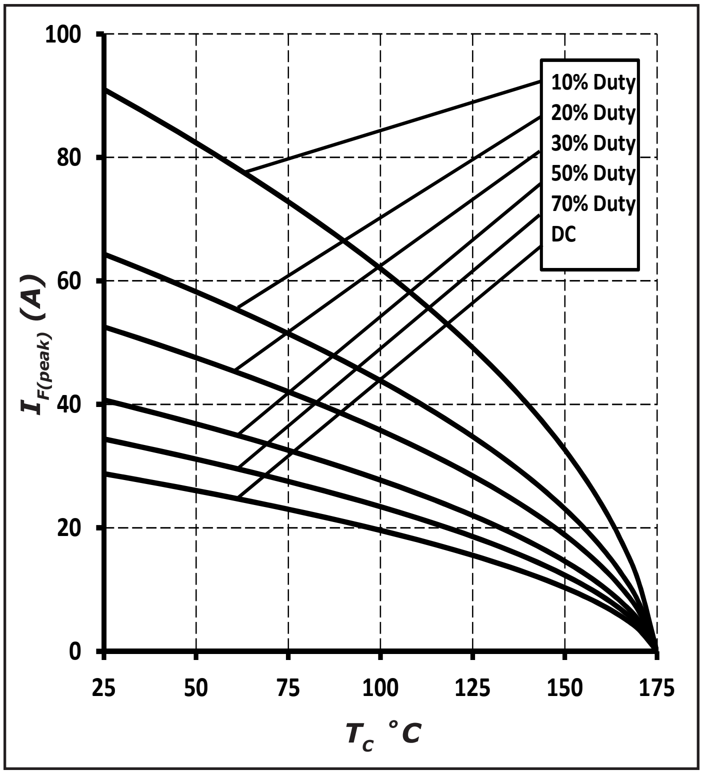


Figure 3. Current Derating

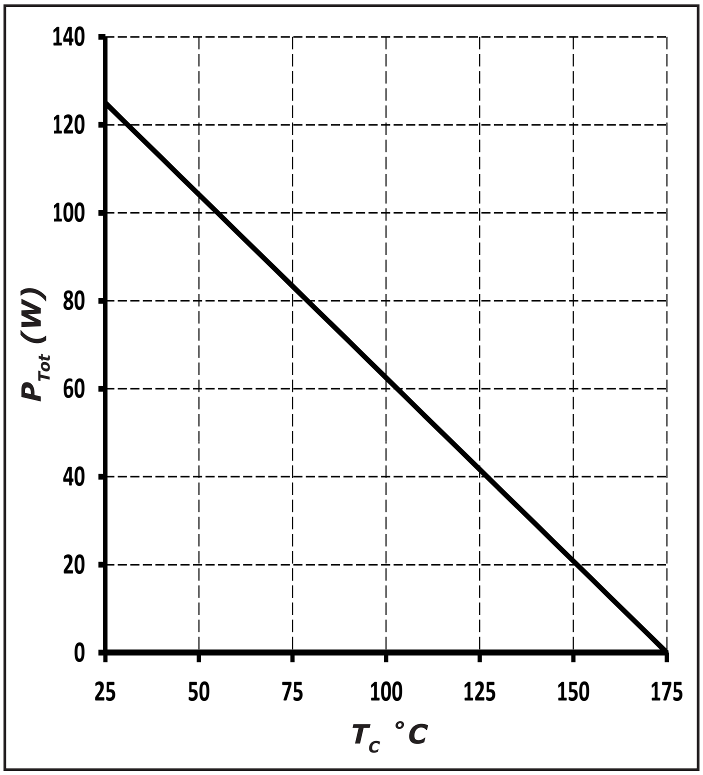


Figure 4. Power Derating

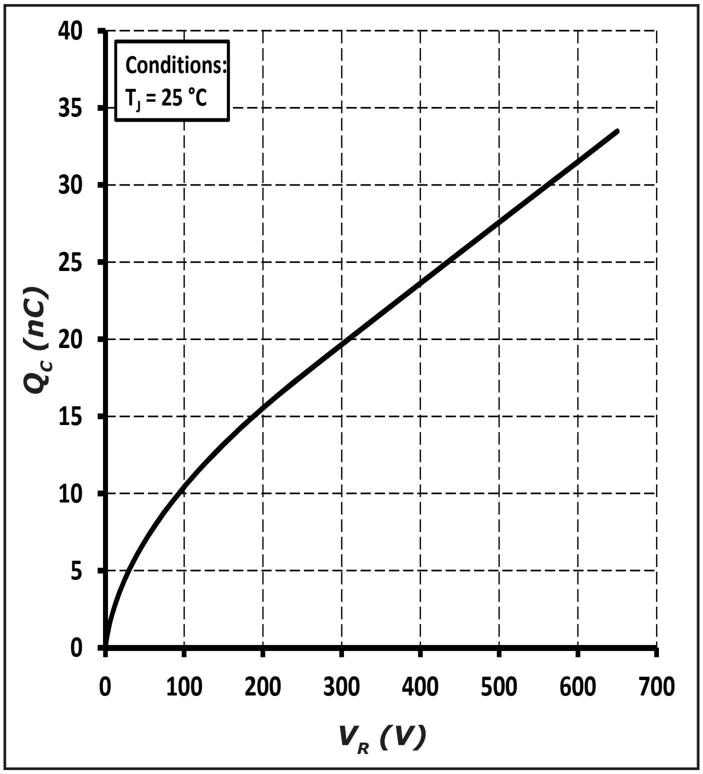


Figure 5. Total Capacitance Charge vs. Reverse Voltage

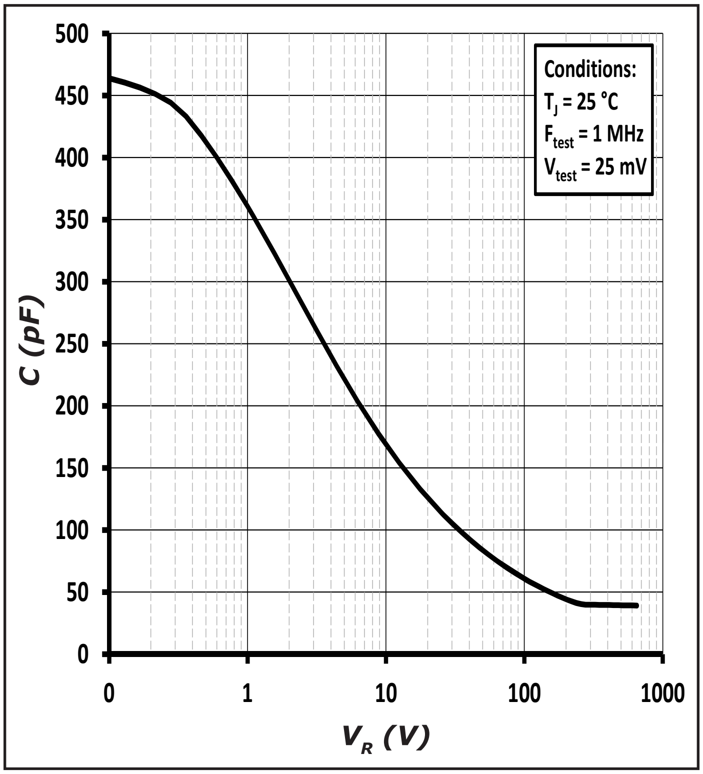


Figure 6. Capacitance vs. Reverse Voltage

Typical Performance

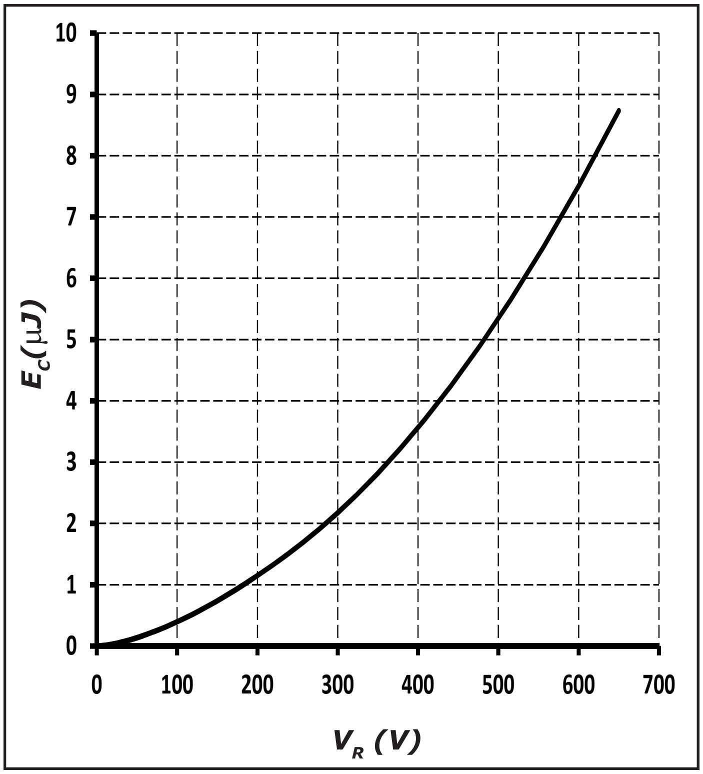


Figure 7. Capacitance Stored Energy

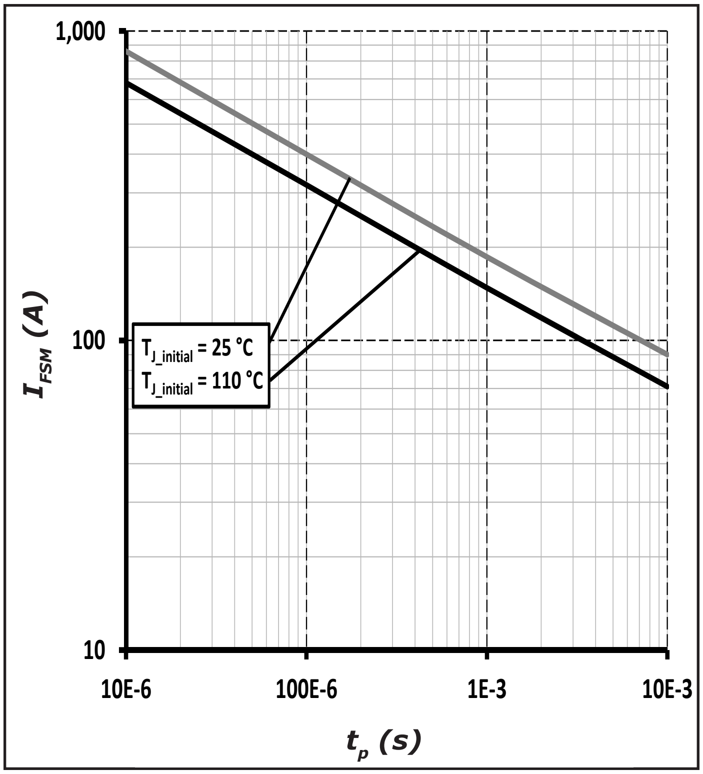


Figure 8. Non-repetitive peak forward surge current versus pulse duration (sinusoidal waveform)

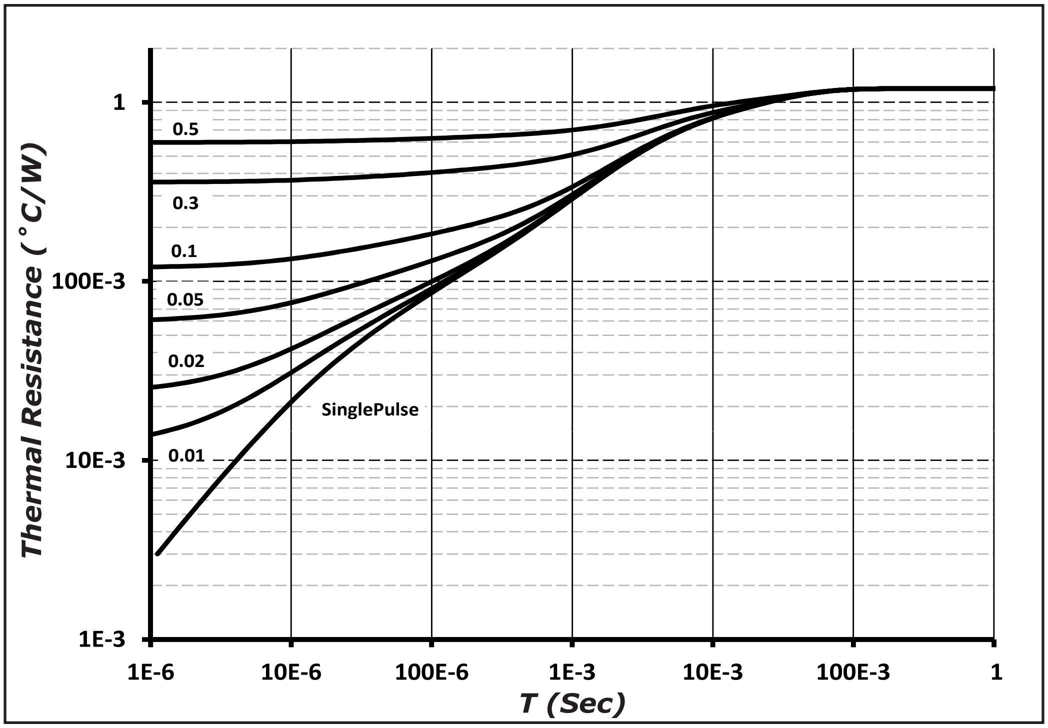
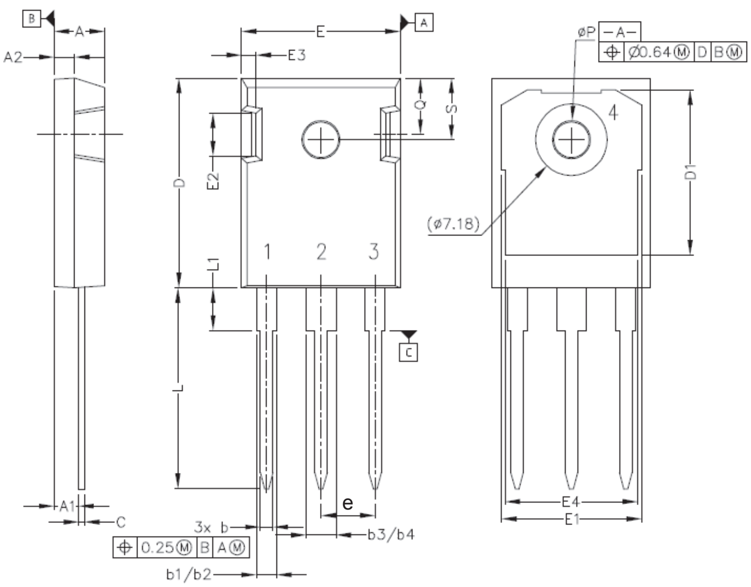
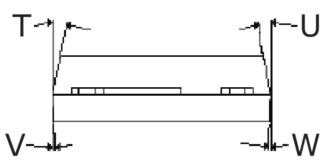


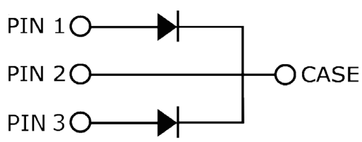
Figure 9. Transient Thermal Impedance

Package Dimensions

Package TO-247-3

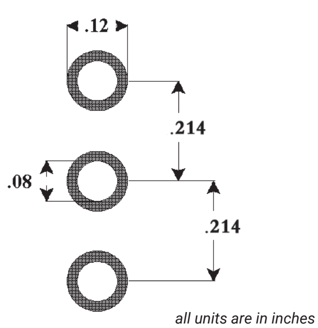






POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°

Recommended Solder Pad Layout

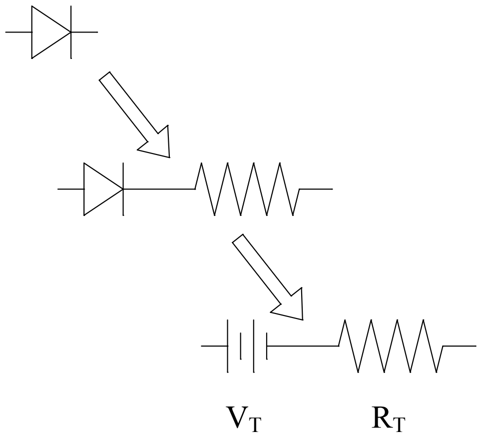


TO-247-3

Part Number	Package	Marking
C3D20060D	TO-247-3	C3D20060

Note: Recommended soldering profiles can be found in the applications note here:
http://www.wolfspeed.com/power_app_notes/soldering

Diode Model (Per Leg)



$$Vf_T = V_T + If * R_T$$

$$V_T = 0.94 + (T_J * -1.3*10^{-3})$$
$$R_T = 0.044 + (T_J * 4.4*10^{-4})$$

Note: T_j = Diode Junction Temperature In Degrees Celsius, valid from 25°C to 175°C

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Ecology section of our website at http://www.wolfspeed.com/Power/Tools-and-Support/Product-Ecology.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

Related Links

- Cree SiC Schottky diode portfolio: http://www.wolfspeed.com/SiCSchottkydiodes
- Schottky diode Spice models: http://www.wolfspeed.com/Schottky-diode-model-request
- SiC MOSFET and diode reference designs: http://www.wolfspeed.com/Power-reference-designs

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power

Elektrische Eigenschaften / Electrical properties

Höchstzulässige Werte / maximum rated values

Periodische Spitzensperrspannung repetitive peak reverse voltages	T_{vj} = -25°C... $T_{vj\,max}$	V_{RRM}	400 600	V V
Durchlaßstrom-Grenzeffektivwert maximum RMS on-state current		I_{FRMSM}	13300	A
Dauergrenzstrom average on-state current	T_C = 56 °C	I_{FAVM}	8320	A
Stoßstrom-Grenzwert surge current	T_{vj} = 25 °C, t_P = 10 ms $T_{vj} = T_{vj\,max}$ t_P = 10 ms	I_{FSM}	103000 95000	A A
Grenzlastintegral I²t-value	T_{vj} = 25 °C, t_P = 10 ms $T_{vj} = T_{vj\,max}$, t_P = 10 ms	I^2t	53000 45000	10^3A^2s 10^3A^2s

Charakteristische Werte / Characteristic values

Durchlaßspannung on-state voltage	$T_{vj} = T_{vj\,max}$, i_F = 10,0 kA $T_{vj} = T_{vj\,max}$, i_F = 4,0 kA	v_F	max. 0,940 max. 0,795	V V
Schleusenspannung threshold voltage	$T_{vj} = T_{vj\,max}$	$V_{(TO)}$	0,7	V
Ersatzwiderstand slope resistance	$T_{vj} = T_{vj\,max}$	r_T	0,024	mΩ
Durchlaßkennlinie 2500 A ≤ i_F ≤ 35000 A on-state characteristic $v_F = A + B \cdot i_F + C \cdot \ln(i_F + 1) + D \cdot \sqrt{i_F}$	$T_{vj} = T_{vj\,max}$	A= B= C= D=	8,869E-01 2,664E-06 -4,856E-02 4,741E-03	
Sperrstrom reverse current	$T_{vj} = T_{vj\,max}$, $v_R = V_{RRM}$	i_R	max. 100	mA

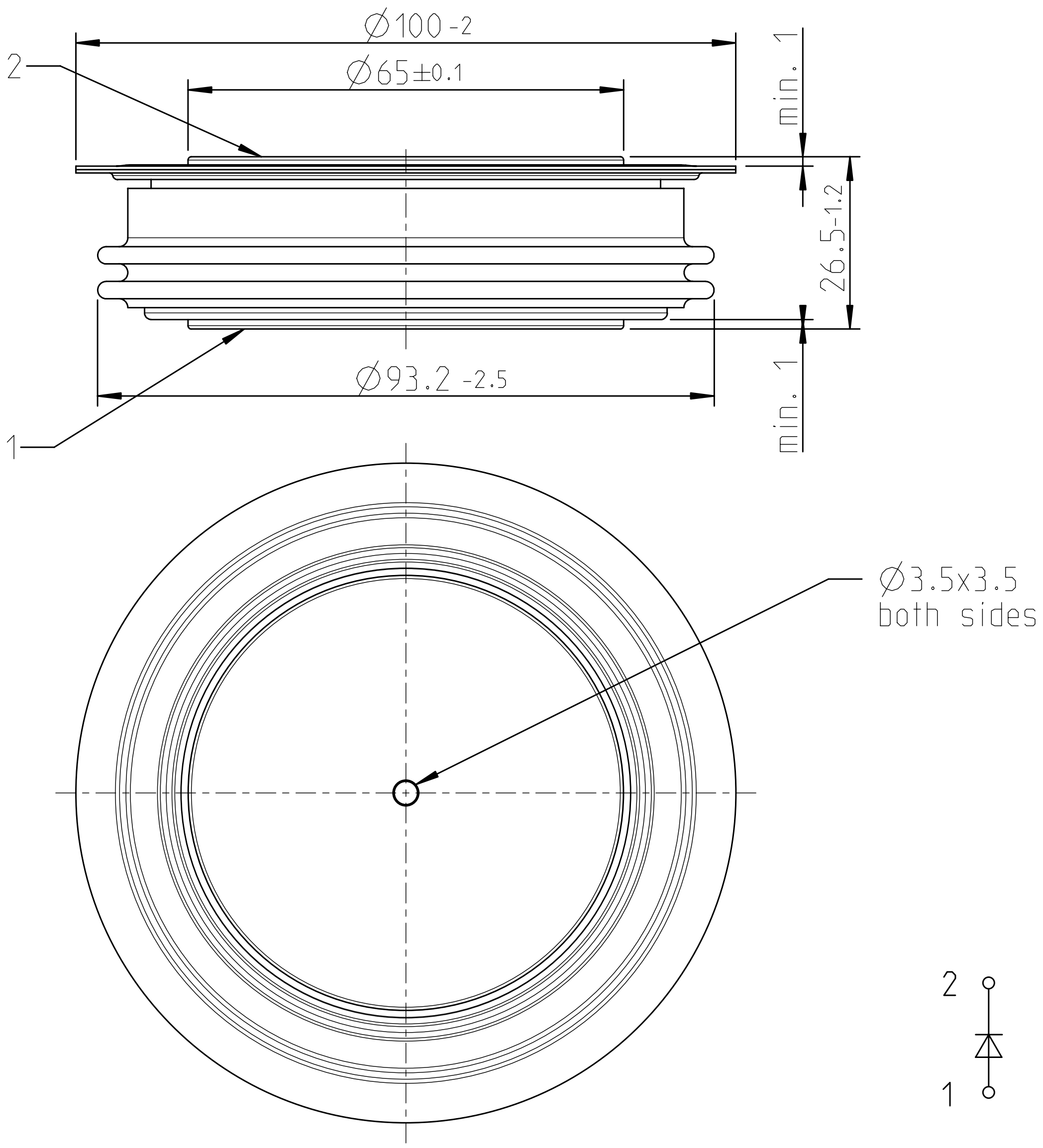
Thermische Eigenschaften / Thermal properties

Innerer Wärmewiderstand thermal resistance, junction to case	<u>Kühlfläche / cooling surface</u> beidseitig / two-sided, θ = 180°sin beidseitig / two-sided, DC Anode / anode, θ = 180°sin Anode / anode, DC Kathode / cathode, θ = 180°sin Kathode / cathode, DC	R_{thJC}	 max. 0,0125 max. 0,0117 max. 0,0232 max. 0,0225 max. 0,0250 max. 0,0245	 °C/W °C/W °C/W °C/W °C/W °C/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	<u>Kühlfläche / cooling surface</u> beidseitig / two-sided	R_{thCH}	max. 0,003	°C/W
Höchstzulässige Sperrschichttemperatur maximum junction temperature		$T_{vj\,max}$	180	°C
Betriebstemperatur operating temperature		$T_{c\,op}$	-25...+150	°C
Lagertemperatur storage temperature		T_{stg}	-25...+150	°C

prepared by:	H.Sandmann		date of publication:	2008-04-10
approved by:	M.Leifeld		revision:	1

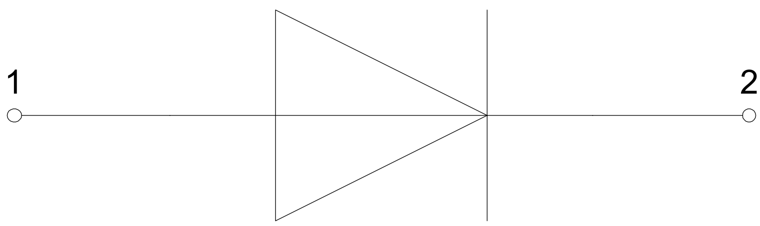
Mechanische Eigenschaften / Mechanical properties

Gehäuse, siehe Anlage case, see annex			Seite 3 page 3	
Si-Element mit Druckkontakt Si-pellet with pressure contact				
Anpreßkraft clamping force		F	40...80	kN
Gewicht weight		G	typ. 900	g
Kriechstrecke creepage distance			30	mm
Schwingfestigkeit vibration resistance	f = 50 Hz		50	m/s²



strike distance: 20mm
creepage distance: 30mm

overall height based
on contact pressure



1: Anode/
Anode

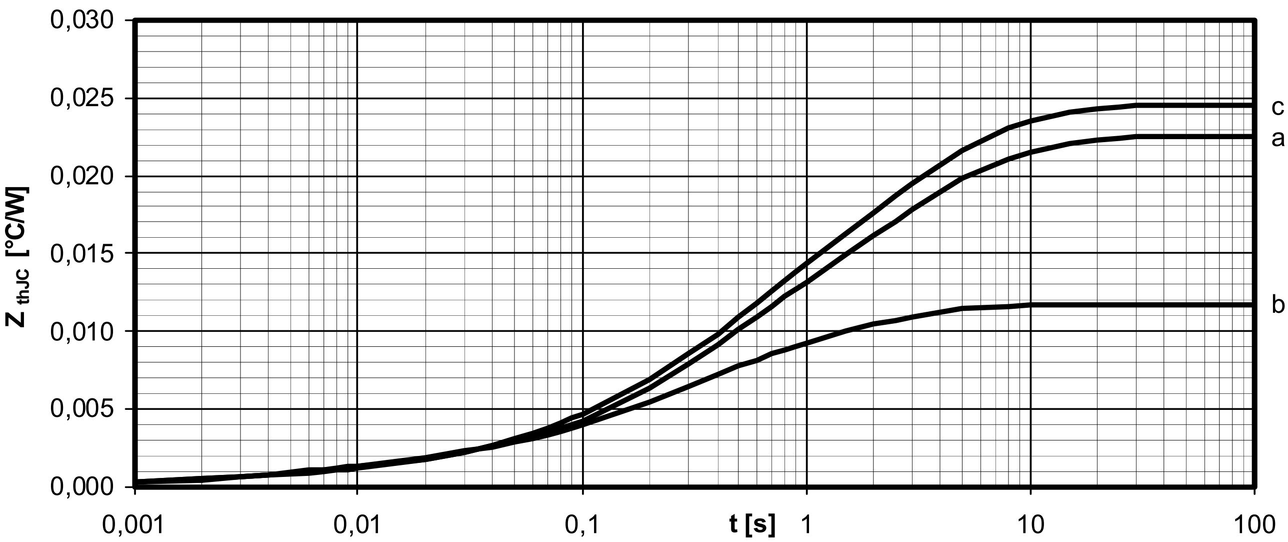
2: Kathode/
Cathode

Analytische Elemente des transienten Wärmewiderstandes Z_{thJC} für DC
Analytical elements of transient thermal impedance Z_{thJC} for DC

Kühlung / Cooling	Pos. n	1	2	3	4	5	6	7
beidseitig two-sided	R_{thn} [°C/W]	0,000034	0,00057	0,000912	0,00274	0,00425	0,00320	-
	τ_n [s]	0,000287	0,00298	0,013500	0,13400	0,44900	2,05000	-
anodenseitig anode-sided	R_{thn} [°C/W]	0,000035	0,00060	0,001050	0,00760	0,00850	0,00470	-
	τ_n [s]	0,000287	0,00230	0,024000	0,31000	1,90000	6,10000	-
kathodenseitig cathode-sided	R_{thn} [°C/W]	0,000035	0,00060	0,002050	0,00805	0,00900	0,00477	-
	τ_n [s]	0,000287	0,00300	0,057000	0,38000	2,05000	6,10000	-

Analytische Funktion / Analytical function:

$$Z_{thJC} = \sum_{n=1}^{n_{max}} R_{thn} \left(1 - e^{\frac{-t}{\tau_n}}\right)$$



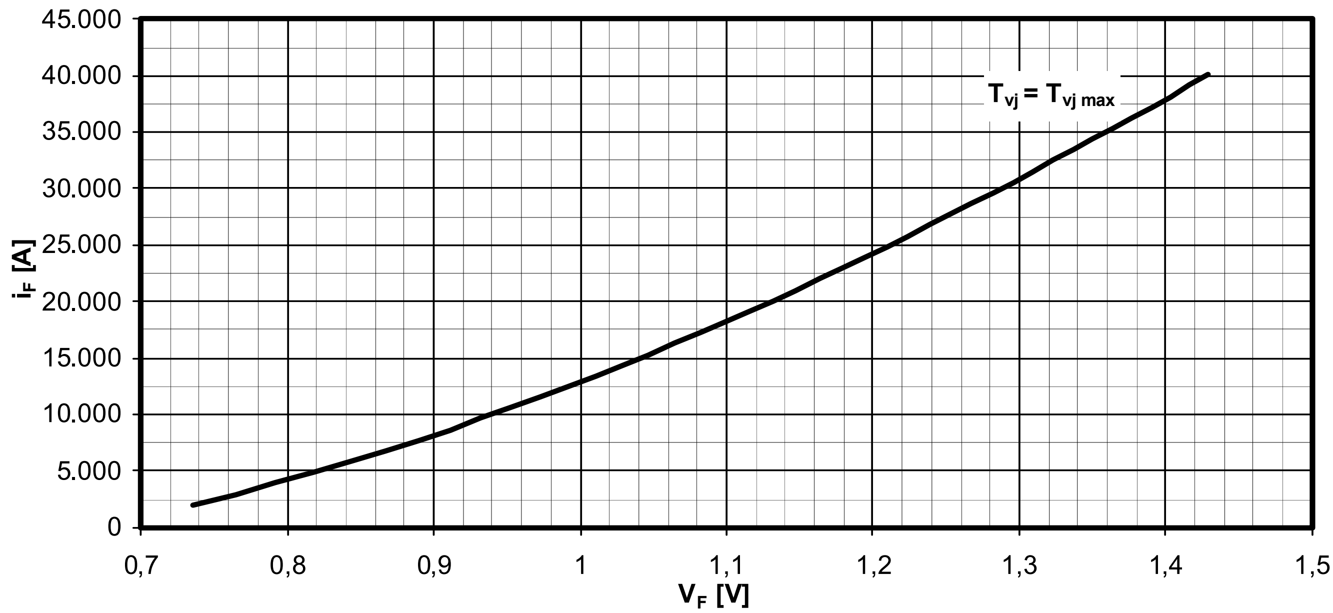
Transienter innerer Wärmewiderstand für DC / Transient thermal impedance for DC
Z_{thJC} = f(t)

a - Anodenseitige Kühlung / Anode-sided cooling
b - Beidseitige Kühlung / Two-sided cooling
c - Kathodenseitige Kühlung / Cathode-sided cooling

Erhöhung des $Z_{th\,DC}$ bei sinus- und rechteckförmigen Strömen für unterschiedliche Stromflusswinkel Θ
Rise of $Z_{th\,DC}$ for sinewave and rectangular current for different current conduction angles Θ
$\Delta Z_{th\,\Theta\,rec}$ / $\Delta Z_{th\,\Theta\,sin}$

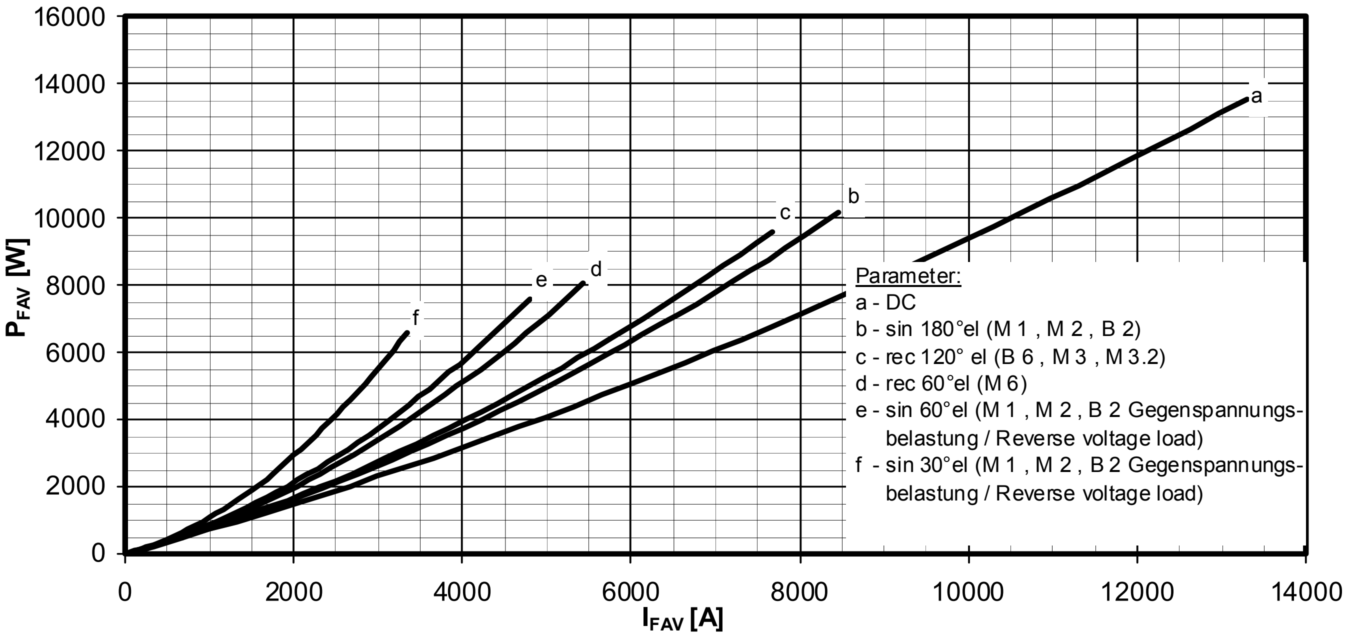
Kühlung / Cooling		Θ = 180°	Θ = 120°	Θ = 90°	Θ = 60°	Θ = 30°
beidseitig two-sided	$\Delta Z_{th\,\Theta\,rec}$ [°C/W]	0,00105	0,00170	0,00218	0,00281	0,00376
	$\Delta Z_{th\,\Theta\,sin}$ [°C/W]	0,00080	0,00112	0,00154	0,00215	0,00315
anodenseitig anode-sided	$\Delta Z_{th\,\Theta\,rec}$ [°C/W]	0,00090	0,00166	0,00220	0,00298	0,00422
	$\Delta Z_{th\,\Theta\,sin}$ [°C/W]	0,00064	0,00096	0,00140	0,00212	0,00345
kathodenseitig cathode-sided	$\Delta Z_{th\,\Theta\,rec}$ [°C/W]	0,00090	0,00149	0,00193	0,00253	0,00345
	$\Delta Z_{th\,\Theta\,sin}$ [°C/W]	0,00066	0,00094	0,00132	0,00188	0,00285

$$Z_{th\,\Theta\,rec} = Z_{th\,DC} + \Delta Z_{th\,\Theta\,rec}$$
$$Z_{th\,\Theta\,sin} = Z_{th\,DC} + \Delta Z_{th\,\Theta\,sin}$$



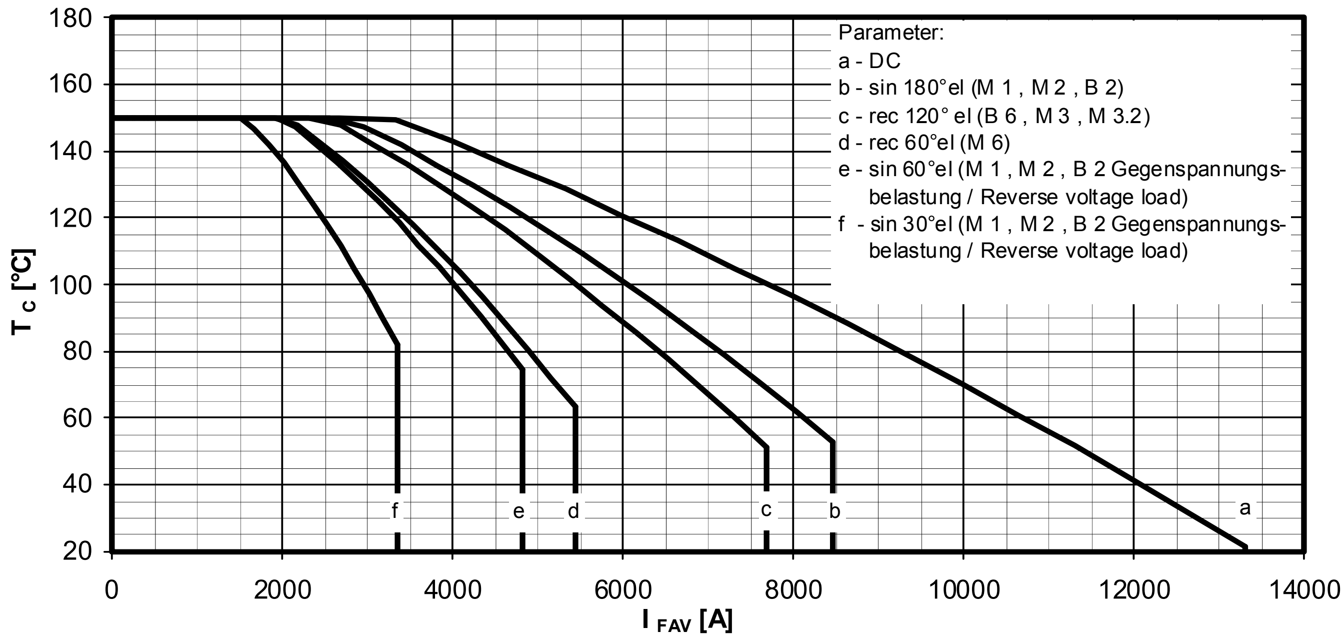
Grenzdurchlasskennlinie / Limiting on-state characteristic $i_F = f(v_F)$

$T_{vj} = T_{vj\,max}$



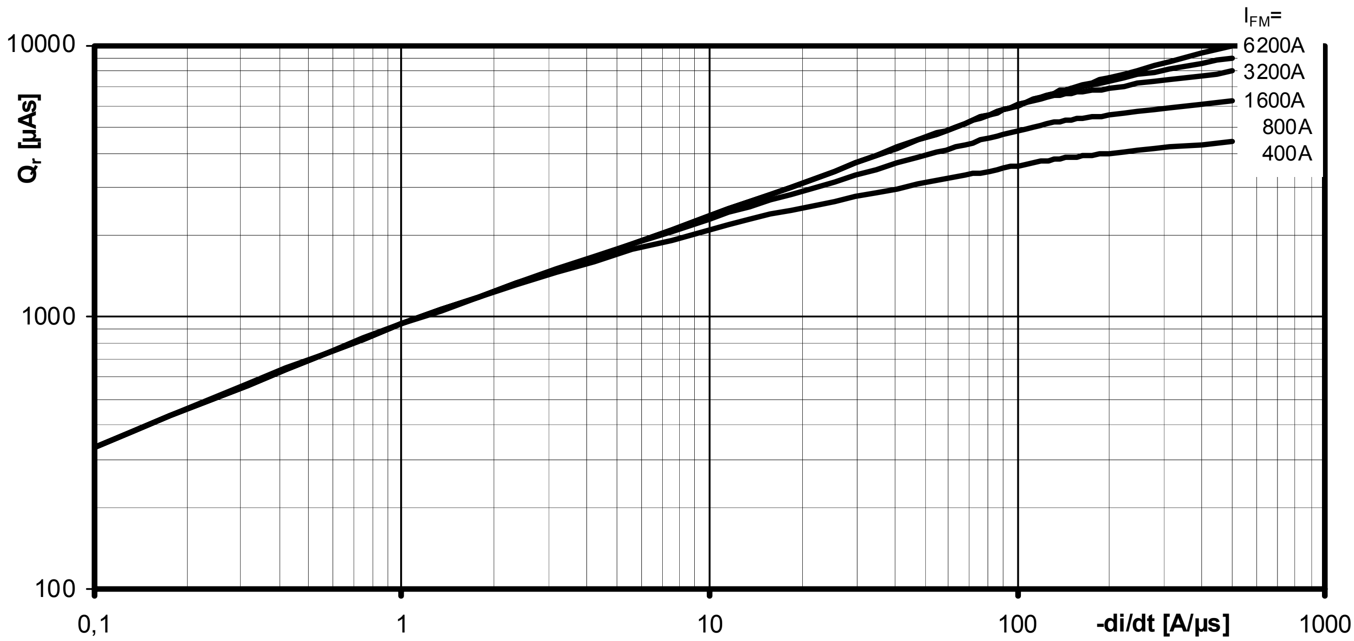
Durchlassverlustleistung / On-state power loss $P_{FAV} = f(I_{FAV})$

Beidseitige Kühlung / Two-sided cooling

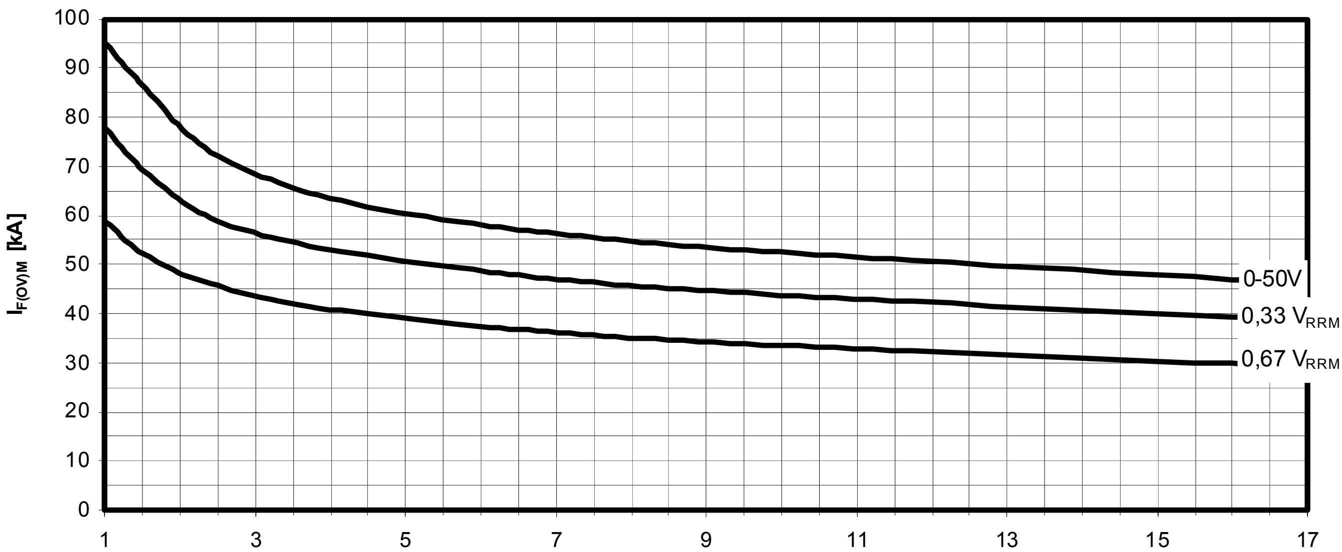


Höchstzulässige Gehäusetemperatur / Maximum allowable case temperature $T_C = f(I_{FAV})$

Beidseitige Kühlung / Two-sided cooling



Sperrverzögerungsladung / Recovered charge
Q_r =f(-di/dt)
T_{vj}= T_{vjmax} , $v_R \leq 0{,}5\ V_{RRM}$, v_{RM} = 0,8 V_{RRM}
RC-Glied / RC-Network: R = 2,7Ω, C = 1,5µF



Anzahl der Pulse bei 50Hz Sinus Halbwellen
Number of pulses of 50Hz sinusoidal half waves

Typische Abhängigkeit des Grenzstromes $I_{F(OV)M}$ von der Anzahl für eine Folge von Sinus Halbwellen bei 50Hz. Parameter: Rückwärtsspannung V_{RM}
Typical dependency of maximum overload on-state current $I_{F(OV)M}$ as a number of a sequence of sinusoidal half waves at 50Hz. Parameter: peak reverse voltage V_{RM}
$I_{F(OV)M}$ = f (pulses, V_{RM}) ; T_{vj} = $T_{vj\ max}$

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