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Power Electronics

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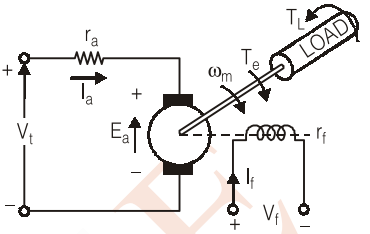
DC DRIVES

Separately-excited DC motor



- Voltage across field winding

  For field circuit

$$V_f = I_f \cdot r_f$$

where I_f = Field winding current, A

R_f = Field circuit resistance, Ω

- Motor terminal voltage

  For armature circuit

$$V_t = E_a + I_a r_a$$

where I_a = Armature current, A

r_a = Armature circuit resistance, Ω

E_a = Back emf, V

V_t = Armature terminal voltage, V

- Motor back emf

$$E_a = k_a \phi \omega_m = k_m \omega_m$$

where ϕ = Field flux per pole, Wb

ω_m = Angular speed of motor, rad/sec.

$k_m = k_a \phi$ = torque constant, Nm/A

- Motor torque

$$T_e = k_m I_a$$

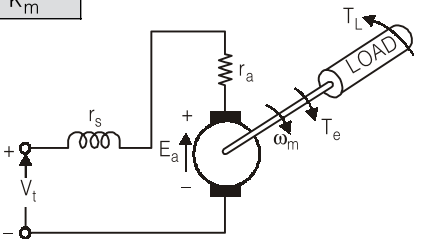
- Angular speed of motor

$$\omega_m = \frac{V_t - I_a r_a}{k_m}$$

DC Series motor

- Motor terminal voltage

$$V_t = E_a + I_a (r_a + r_s)$$



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Digital Electronics

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DIGITAL LOGIC CIRCUITS

Combinational circuits

- Output do not depends on previous value of input.
- No feedback is required.
- It consists of inptu variables, logic gate and output variables.
- No memory is required.

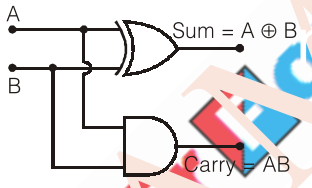
Sequential circuits

- Output depends on the present as well previous value of inputs.
- It consists input variables, Flip-flops, registers and output.
- Memory is required.

HALF ADDER (H.A)

- A logic circuit for the addition of two one-bit numbers is referred to as an "HALF ADDER (H.A)".

Symbol and Truth table



Inputs		Outputs	
A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

❑ Logical expression

$$\text{Sum, } S = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry, } C = AB$$

- Total number of NAND-gates required to implement half adder = 5
- Total number of NOR-gates required to implement half adder = 5
- Implement the H.A circuit by minimum number of logic gates if we have all gates except EXOR and EXNOR is "3".

FULL ADDER (F.A.)

- It performs the arithmetic sum of the three input bits i.e. addend bit, augend bit and carry bit.

❑ Logical expression

$$\text{Sum, } \boxed{S = A \oplus B \oplus C}$$

$$\text{Carry, } \boxed{C = AB + BC + CA = AB + C(A \oplus B)}$$

- A F.A. can be implemented by two H.A. and one OR-gate
- Total number of NAND-gate/NOR-gate required to implement a F.A is equals to "9".

HALF SUBTRACTOR (H.S)

❑ Logical expression

$$\text{Difference, } \boxed{D = \bar{A}B + A\bar{B} = A \oplus B}$$

$$\text{Borrow, } \boxed{B = \bar{A}B}$$

- Total number of NAND/NOR gates required to implement the H.S is equals to "5".

FULL SUBTRACTOR (F.S)

- It is a circuit which performs a subtraction between two bits taking into account that a '1' may have been borrowed by a lower significant stage.

❑ Logical expression

$$\text{Difference, } \boxed{D = A \oplus B \oplus C}$$

$$\text{Borrow, } \boxed{B = \bar{A}B + \bar{A}C + BC = \bar{A}B + \left(\overline{A \oplus B}\right) \cdot C}$$

- A F.S. can be implemented with two H.S. and one OR gate.
- Number of NAND/NOR gates required to implement the F.S is equals to "9".
- In paralller adder n F.A. or {(n – 1) F.A. and 1 H.A.} or {(2n – 1) H.A and (n – 1) OR-gate} are required to add two n bit numbers.

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Network Theory

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