

A Handbook on Electrical Engineering

3

Power Electronics

CONTENTS

1. Power Semiconductor Diodes & Transistors	101 - 102
2. Diode Circuits and Rectifiers	103 - 111
3. Thyristor Commutation Techniques	112 - 114
4. Phase Controlled Rectifiers	115 - 119
5. Choppers	120 - 121
6. Inverters	122 - 125
7. AC Voltage Controllers	126 - 127
8. Electric Drives	128 - 131

DC DRIVES

Separately-excited DC motor

- Voltage across field winding

For field circuit

$$V_f = I_f \cdot r_f$$

where I_f = Field winding current, A

r_f = Field circuit resistance, Ω

- Motor terminal voltage

For armature circuit

$$V_t = E_a + I_a r_a$$

where I_a = Armature current, A

r_a = Armature circuit resistance, Ω

E_a = Back emf, V

V_t = Armature terminal voltage, V

- Motor back emf

$$E_a = k_a \phi \omega_m = k_m \omega_m$$

where ϕ = Field flux per pole, Wb

ω_m = Angular speed of motor, rad/sec.

$k_m = k_a \phi$ = torque constant, Nm/A

- Motor torque

$$T_e = k_m I_a$$

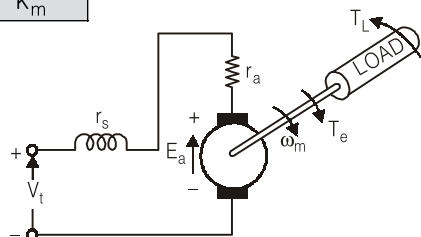
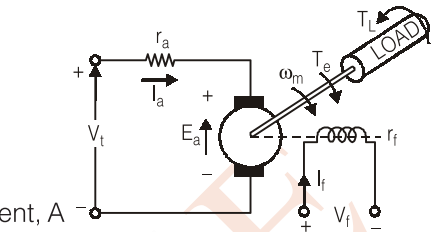
- Angular speed of motor

$$\omega_m = \frac{V_t - I_a r_a}{k_m}$$

DC Series motor

- Motor terminal voltage

$$V_t = E_a + I_a (r_a + r_s)$$



A Handbook on Electrical Engineering

9

Digital Electronics

CONTENTS

1. Number System and Codes	292-293
2. Logic Gates	294-300
3. Boolean Algebra & Reduction Techniques	301-303
4. Arithmetic Operation and Circuits	304-306
5. Code Converters, Multiplexers and Demultiplexers	307-311
6. Sequential Circuits (FFs and Latches)	312-316
7. Shift Registers	317-318
8. Counters	319-322
9. Digital ICs Family	323-326
10. ADCs and DACs	327-330

DIGITAL LOGIC CIRCUITS

Combinational circuits

- Output do not depends on previous value of input.
- No feedback is required.
- It consists of inptu variables, logic gate and output variables.
- No memory is required.

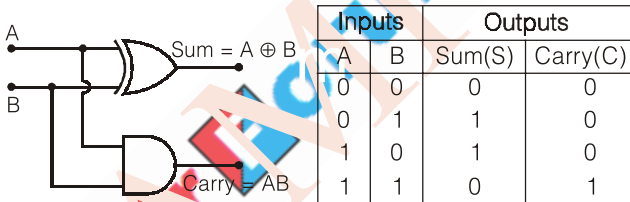
Sequential circuits

- Output depends on the present as well previous value of inputs.
- It consists input variables, Flip-flops, registers and output.
- Memory is required.

HALF ADDER (H.A)

- A logic circuit for the addition of two one-bit numbers is referred to as an "HALF ADDER (H.A)".

Symbol and Truth table



□ Logical expression

Sum, $S = \bar{A}B + A\bar{B} = A \oplus B$

Carry, $C = AB$



Remember

- Total number of NAND-gates required to implement half adder = 5
- Total number of NOR-gates required to implement half adder = 5
- Implement the H.A circuit by minimum number of logic gates if we have all gates except EXOR and EXNOR is "3".

FULL ADDER (F.A.)

- It performs the arithmetic sum of the three input bits i.e. addend bit, augend bit and carry bit.

□ Logical expression

Sum, $S = A \oplus B \oplus C$

Carry, $C = AB + BC + CA = AB + C(A \oplus B)$



Remember

- A F.A. can be implemented by two H.A. and one OR-gate
- Total number of NAND-gate/NOR-gate required to implement a F.A is equals to "9".

HALF SUBTRACTOR (H.S)

□ Logical expression

Difference, $D = \bar{A}B + A\bar{B} = A \oplus B$

Borrow, $B = \bar{A}B$



Remember

- Total number of NAND/NOR gates required to implement the H.S is equals to "5".

FULL SUBTRACTOR (F.S)

- It is a circuit which performs a subtraction between two bits taking into account that a '1' may have been borrowed by a lower significant stage.

□ Logical expression

Difference, $D = A \oplus B \oplus C$

Borrow, $B = \bar{A}B + \bar{A}C + BC = \bar{A}B + (\bar{A} \oplus \bar{B}) \cdot C$



Remember

- A F.S. can be implemented with two H.S. and one OR gate.
- Number of NAND/NOR gates required to implement the F.S is equals to "9".
- In parallel adder n F.A. or {(n - 1) F.A. and 1 H.A.} or {(2n - 1) H.A and (n - 1) OR-gate} are required to add two n bit numbers.

A Handbook on Electrical Engineering

5

Network Theory

CONTENTS

1. Circuits Elements and Signal Waveform	182 - 186
2. Network Laws and Theorems	187 - 192
3. Graph Theory	193 - 195
4. Laplace Transform Analysis and Circuit Transients	196 - 200
5. Resonance	201 - 203
6. Two Port Network	204- 206
