

# **BHARAT PHOTO STAT**

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## **NOTE BOOK**

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Boolean Algebra :-

→ G. Boole in 1854

ON - '1'

→ He used switches

OFF - '0'

Minimization:-

→ Boolean algebra is used when no. of variables are less and o/p is either '0' or '1'.

→ K-Map is used when no. of variables are upto 5 and o/p can be 0, 1 or X (Don't care)

→ Quine Mccluskey is used for any no. of variable

Theorems:-(I) NOT:-

$$A \rightarrow \bar{A} \text{ or } A'$$

$$\bar{\bar{A}} \rightarrow A$$

(II) AND Operation:-

0 · 0 = 0
0 · 1 = 0
1 · 0 = 0
1 · 1 = 1

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A · A = A
A · 0 = 0
A · 1 = A
A · \bar{A} = 0

(III) OR Operation:-

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1

A + A = A
A + 0 = A
A + 1 = 1
A + \bar{A} = 1

$$\rightarrow A + A + A = A$$

$$\rightarrow 1 + A + B + C + \dots + Z = 1$$

Ques:- Minimize  $AB + A\bar{B}$

$$\text{Soln:- } A(B + \bar{B}) = A$$

$\rightarrow$  B (Redundant)

Ques:-  $A\bar{B} + AB\bar{C} + ABC$  Min. no. of NAND

$$\text{Soln:- } A\bar{B} + ABC(C + \bar{C})$$

$$= A\bar{B} + AB = A(B + \bar{B}) = A$$

$\rightarrow$  Zero NAND gate

Advantages of Minimization:-

- (i) No. of logic gates will decrease
- (ii) Speed inc.
- (iii) Power dissipation dec.
- (iv) Cost dec
- (v) Complexity of ckt. dec.

Ques:- Minimize  $AB + AB + \bar{A}B + \bar{A}\bar{B} \rightarrow$  SOP

$$\text{Soln:- } A(\bar{B} + B) + \bar{A}(B + \bar{B})$$

$$= A + \bar{A} = 1$$

Ques:- Minimize  $(A+B)(A+C)$

$$\text{Soln:- } A \cdot A + AC + AB + BC$$

$$= A + AC + AB + BC$$

$$= A(1 + C + B) + BC = A + BC$$

Short-cut:-

$$(A+B)(A+C) = A + BC$$

$$(\bar{x}+y)(\bar{x}+z) = \bar{x} + yz$$

Ques:- Minimize  $(A+B+C)(A+\bar{B}+C)(A+\bar{B}+\bar{C})$

Soln:-  $(A+B+0)(A+\bar{B}+C)$

$$= A + B \cdot \bar{B} + BC = A + BC$$

Ques:- Minimize  $(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})$

Soln:-  $(A+0)(\bar{A}) = 0$

Distribution theorem:-

$$A + BC = (A+B)(A+C)$$

$$(1) \quad (2) \quad (3) \quad . \quad (1+2) \quad (1+3)$$

Ques:- Minimize the following expressions

$$(I) \quad A + \bar{A}B$$

$$\text{Soln}:- (I) \quad (A+\bar{A})(A+B) = A+B$$

$$(II) \quad A + \bar{A}\bar{B}$$

$$(II) \quad (A+\bar{A})(A+\bar{B}) = A+\bar{B}$$

$$(III) \quad \bar{A} + AB$$

$$(III) \quad (\bar{A}+A)(\bar{A}+B) = \bar{A}+B$$

$$(IV) \quad \bar{A} + A\bar{B}$$

$$(IV) \quad (\bar{A}+A)(\bar{A}+\bar{B}) = \bar{A}+\bar{B}$$

Ques:- Minimize  $ABC + \bar{A}BC + A\bar{B}C$

Soln:-  $(A+\bar{A})BC + A\bar{B}C$

$$= BC + A\bar{B}C$$

$$= B(C+A\bar{C}) = B[C(C+A)C(C+\bar{C})]$$

$$= AB + BC$$

Ques:- Minimize  $AB + \bar{A}B + \bar{A}\bar{B}$

Soln:-  $(A+\bar{A})B + \bar{A}\bar{B} = B + \bar{A}\bar{B}$

$$= (B+\bar{A})(B+\bar{B}) = \bar{A}+B$$

Ques:-  $\bar{A}\bar{B} + BC + B\bar{C} \rightarrow \text{Minimize}$

Soln:-  $\bar{A}\bar{B} + B(C+C\bar{C}) = B + A\bar{B}$

$$= (A+B)(B+\bar{B}) = A+B$$

Ques:- Minimize  $AB + \bar{A}C + BC$  & also find redundant

Soln:-  $AB + C(\bar{A} + B)$

$$= (AB + C)(AB + \bar{A} + B)$$

$$= (AB + C)(B(A+1) + \bar{A})$$

$$= (AB + C)(\bar{A} + B) = AB + \bar{A}C + BC$$

$$= AB + \bar{A}C + BC(A + \bar{A})$$

$$= AB + \bar{A}C + ABC + \bar{A}BC$$

$$= AB(1 + \bar{C}) + \bar{A}C(1 + B) = AB + \bar{A}C$$

Short cut :-

Consensus theorem:-

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

(I) Three variables      (II) Each variable twice

(III) Only one variable is complemented / uncomplemented

$$AB + AC + \bar{B}C = AB + \bar{B}C$$

For POS form:-

Ques:-  $(A+B)(\bar{A}+C)(B+C) \rightarrow \text{Minimize}$

Soln:-  $(A+B)(\bar{A}+C)$ , Ans

Ques:-  $(A+B)(B+C)(A+\bar{C}) \rightarrow \text{Minimize}$

Soln:-  $(B+C)(A+\bar{C})$

Ques:-  $(A+B)(\bar{B}+C)(A+C) \rightarrow \text{Minimize}$

Soln:-  $(A+B)(\bar{B}+C)$

Ques:-  $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C} \rightarrow \text{Minimize}$

Soln:-  $\bar{A}\bar{B} + \bar{A}\bar{C}$

Ques:-  $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C} \rightarrow \text{Minimize}$

Soln:-  $\bar{B}\bar{C} + \bar{A}\bar{C}$

Ques:-  $(\bar{A}+\bar{B})(\bar{B}+\bar{C})(A+\bar{C}) \rightarrow \text{Minimize}$

Soln:-  $(\bar{A}+\bar{B})(A+\bar{C})$

## Transposition theorem:

$$(A+B)(\bar{A}+C) = AC + \bar{A}B$$

## Gemorgan's theorem:

$$\overline{ABC} = \overline{A} + \overline{B} + \overline{C}$$

$$\overline{A+B+C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

## Boolean Algebra :-

## (1) Theorems → Minimization

(2)  $\sup$   $\longrightarrow$  Minimal

## Minimal

## Canonical

3. (3) POS

#### (4) Truth Tables

(5) dual (6) complement (7) Venn diagram

(8) switching circuits (9) statements

$$\text{Minimize} \rightarrow \frac{xy}{A} + \frac{\overline{xy}}{\overline{A}} \underline{wz} \quad B$$

$$\underline{\text{SOLN:}} \quad (A + \bar{A})(A + B) \equiv XY + WZ$$

SOP:—

→ SOP form is used when o/p logic expression is logic '1'.

$\rightarrow \underline{ABC} + \underline{ABc} + \underline{A\bar{B}\bar{C}}$   $\rightarrow$  each term is called minterm

$$\rightarrow \text{min term} = 5 \rightarrow [0] \rightarrow A\bar{B}C$$

Ques:- For the given truth table minimised SOP is

A	B	C
O	O	I
O	I	O
I	O	I
I	I	I

$$\begin{aligned}
 \text{Soln:- } Y &= A\bar{B} + A\bar{B} + AB \\
 &= \bar{B}(A+A) + AB = \bar{B} + AB \\
 &= (A+\bar{B})(B+\bar{B}) = A+\bar{B}
 \end{aligned}$$

standard SOP form :-

$$Y(A,B) = \sum m(0,2,3)$$

ques:- Minimize  $f(A,B) = \sum m(0,1,3)$

$$\begin{aligned}
 \text{Soln:- } &A\bar{B} + \bar{A}B + AB \\
 &= \bar{A}(\bar{B}+B) + AB = \bar{A} + AB \\
 &= (A+\bar{A})(\bar{A}+B) = \bar{A}+B
 \end{aligned}$$

Note:-

$$A + \bar{A}B = A+B \rightarrow \text{Minimal SOP (can't min. further)}$$

$$\begin{aligned}
 A\cdot 1 + \bar{A}B &= A \cdot (\bar{B}+\bar{B}) + \bar{A}B \\
 &= A \cdot (\bar{B}+\bar{B}) + \bar{A}B \\
 &= \underbrace{AB + A\bar{B} + \bar{A}B}_{\text{Canonical SOP (in variables)}}
 \end{aligned}$$

In canonical form each min term contains all variables

$\sum m(1,2,3) \rightarrow \text{Standard SOP (in numbers)}$

ques:- No. of minterms present in canonical expression of  $A+\bar{B}C$

- (a) 3    (b) 4    (c) 5    (d) 6

$$\begin{aligned}
 \text{Soln:- } &A(B+\bar{B})(C+\bar{C}) + \bar{B}C(A+\bar{A}) \\
 &= A(BC + B\bar{C} + \bar{B}C + \bar{B}\bar{C}) + A\bar{B}C + \bar{A}\bar{B}C \\
 &= ABC + A\bar{B}C + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C \\
 &= ABC + A\bar{B}C + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C \\
 &\rightarrow 5 \text{ minterms}
 \end{aligned}$$

$$\sum m(1,4,5,6,7)$$

- Canonical form is necessary used when implemented using MUX and decoders
- Minimal form is used when implemented using logic gates.

POS form :-

→ POS form is used when o/p is logic '0'

→  $(A+B+C) \cdot (A+\bar{B}+C) \cdot (A+\bar{B}+\bar{C})$ .

Max. term

→ 5 → Max. term



$$\begin{array}{ccc} 1 & 0 & 1 \\ \bar{A} + B + \bar{C} \end{array}$$

$$\rightarrow (\bar{A} + B + \bar{C})$$

Ques:- For the given truth table minimized POS expression

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

Soln:-  $y = A\bar{B} + \bar{A}\bar{B} = \bar{B}(A + \bar{A}) = \bar{B}$

$$Y(A, B) = \prod M(1, 3) = \bar{B}$$

$$Y(A, B) = \sum m(0, 2)$$



$$Y = \bar{A}\bar{B} + A\bar{B} = \bar{B}(\bar{A} + A) = \bar{B}$$

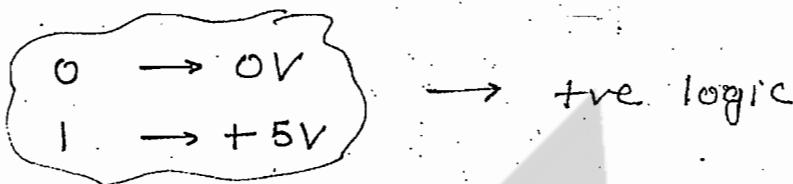
$$\boxed{\sum m(0, 2) = \prod M(1, 3)}$$

$$m_0 + m_2 = M_1 \cdot M_3$$

- With  $n$ -variable max. possible minterm or maxterm are  $2^n$
- With 2 variable possible no. of logical expression is 16

$$2 \rightarrow 16$$

- With  $n$ -variable max. possible logical expression are  $2^{2^n}$



### Dual :-

- In digital systems there are two types of logic (i) +ve logic (ii) -ve logic
- Dual expression is used to convert +ve logic to -ve logic or -ve logic to +ve logic.

+ve logic AND

+ve logic OR

A	B	Y
0 (0V)	0 (0V)	0 (0V)
0 (0V)	1 (+5V)	0 (0V)
1	0	0
1	1	1

A	B	Y
0 (0V)	0 (0V)	0 (0V)
0 (0V)	1 (+5V)	1 (+5V)
1	0	1
1	1	1

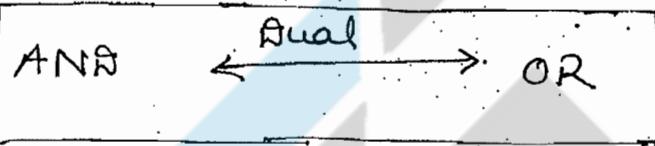
-ve logic OR:-

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A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

+ve logic AND = -ve logic OR

-ve logic AND = +ve logic OR



$$AB \xleftrightarrow{\text{dual}} A+B$$

In dual:-

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$$\text{AND} \longleftrightarrow \text{OR}$$

$$\cdot \longleftrightarrow +$$

$$1 \longleftrightarrow 0$$

→ Keep variable as it is

ques:- Find dual of  $A\bar{B}\bar{C} + \bar{A}BC + ABC$

Soln:-  $(A+B+\bar{C})(\bar{A}+B+C)(A+B+C)$

→ For any logical expression if two times dual is used resulting same expression.

ques:- Simplify  $(A+\bar{B}+C)(A+B+\bar{C})(A+B+C)$

Soln:- Taking dual

$$(A\bar{B}\bar{C}) + ABC + ABC$$

$$\Rightarrow AC(B+\bar{B}) + ABC(C+\bar{C})$$

$$= AC + AB$$

$\downarrow$  dual

$$= (A+C) (A+B)$$

### Self-Dual :-

→ In self dual expression if one time dual is used results in same expression.

e.g:-  $AB + BC + AC$

$\downarrow$  dual  
 $(A+B) (B+C) (A+C)$

$$= (AC + B) (A+C) = AC + AC + AB + BC$$

$$= AB + BC + AC$$

$$\rightarrow \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C} \rightarrow \text{self dual}$$

→ With  $n$ -variables max. possible self dual expression are  $2^{\frac{2^n-1}{2}} \cdot 2^{n-1}$

$n : \xrightarrow{\text{self dual}} 2^{n-1}$

$$\rightarrow n=1 \xrightarrow[\text{dual}]{\text{self}} 2^2 = 2$$

$$A \xrightarrow{\text{dual}} A$$

$$A \cdot 1 \xrightarrow{\text{dual}} A + 0 = A$$

$$\bar{A} \xrightarrow{\text{dual}} \bar{A}$$

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## Complement :-

$$Y = ABC + \bar{A}BC + A\bar{B}\bar{C}$$

$$\bar{Y} = ?$$

(I) AND

Complement

OR

• → +

(II)

1

→ 0

(III)

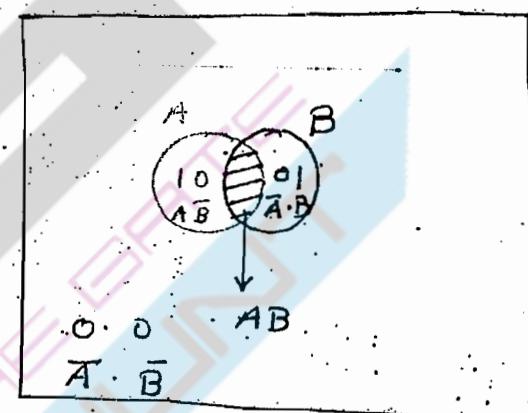
Complement each variable

$$\bar{Y} = 1(\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} + B + \bar{C}) (\bar{A} + B + C)$$

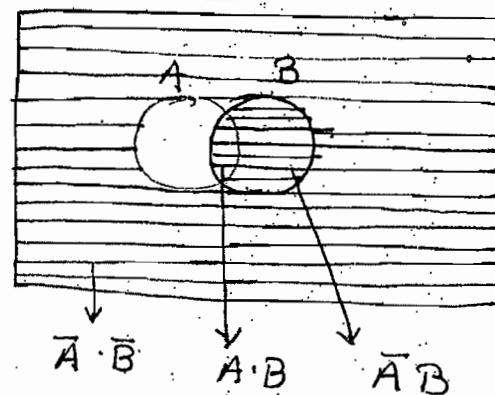
## Venn - Diagram :-

∩ → AND

∪ → OR



Ques:- For the given Venn-diagram minimize the SOP expression for the area shaded in figure.

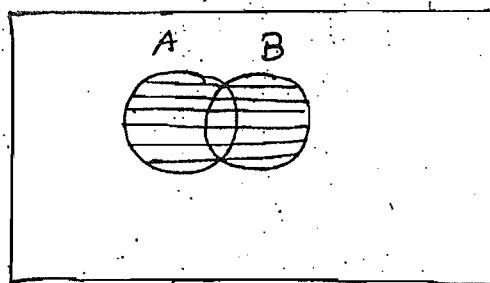


$$= \bar{A} \cdot \bar{B} + A \cdot \bar{B} + \bar{A} \cdot B$$

$$= \bar{A} \cdot \bar{B} + B = \bar{A} + B$$

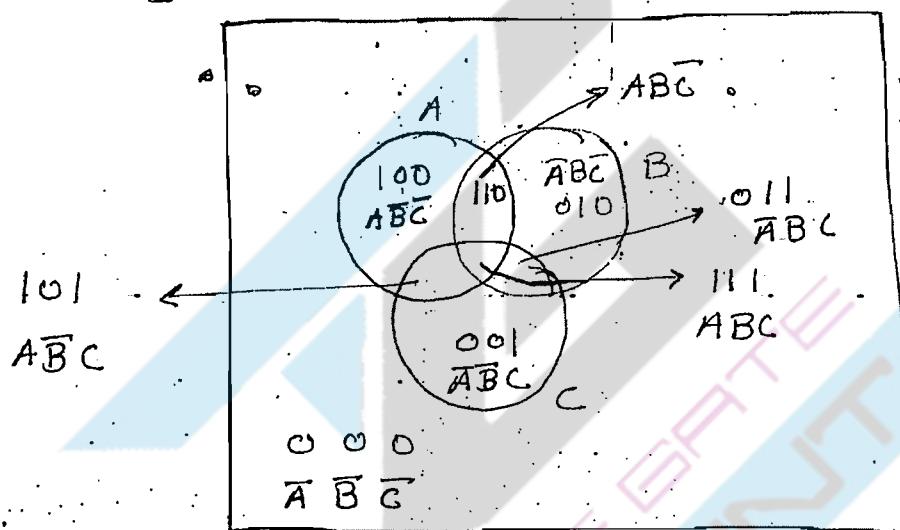
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Ques:- For the given Venn diagram minimize the SOP expression for the area shaded in figure

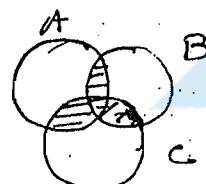


$$\text{SOP: } AB + AB + \bar{A}B = A + \bar{A}B = A + B$$

For 3-Variable System:-



Ques:- For the given Venn-diagram minimize the SOP expression for shaded area



$$\text{SOP: } ABC + ABC + A\bar{B}C + \bar{A}BC$$

$$\begin{aligned}
 &= AB(\bar{C}+C) + AC(B+\bar{B}) + BC(A+\bar{A}) \\
 &= AB + AC + BC
 \end{aligned}$$

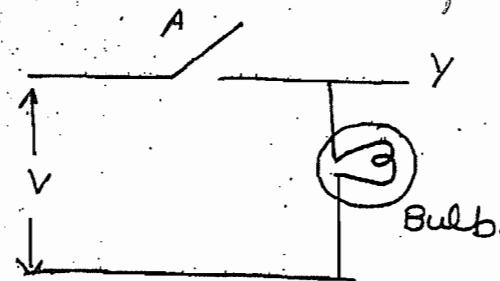
## Switching Circuits :-

### (a) Buffer :-

$$\rightarrow Y = A$$

$\rightarrow$  Use to improve fan out

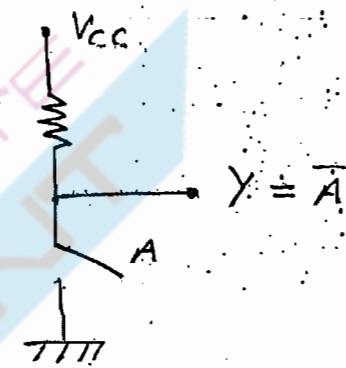
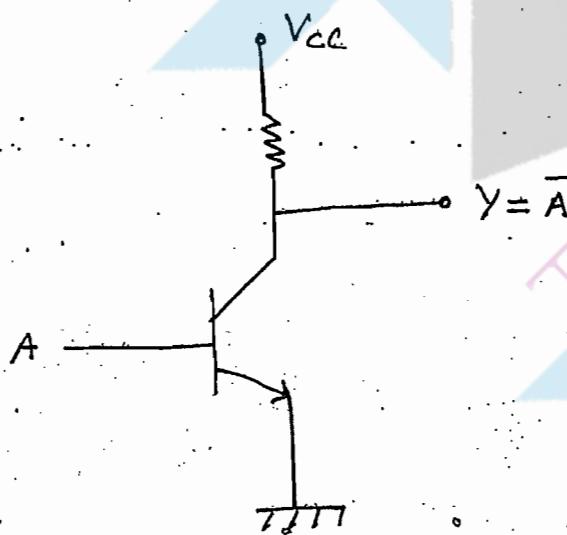
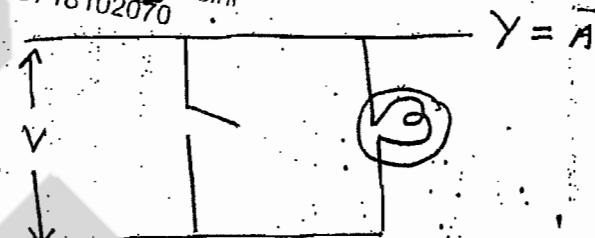
A	Y
0	0
1	1



### (b) NOT :-

A	Y
0	1
1	0

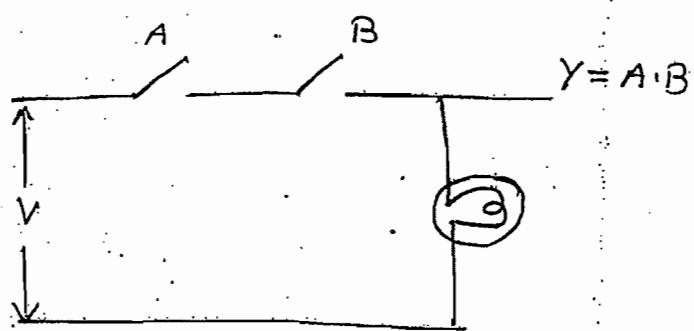
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A	T <sub>1</sub>	Y
0	OFF (cut-off)	1
1	ON (sat.)	0

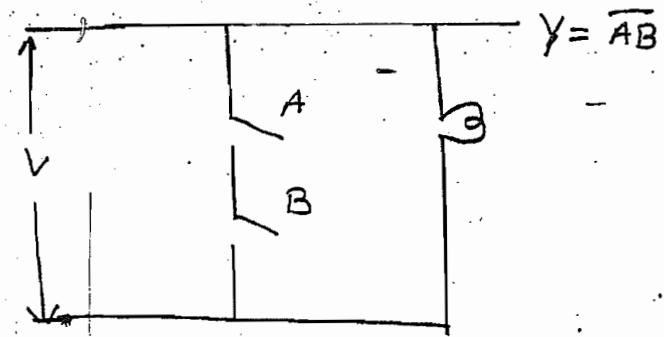
### (c) AND :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



(d) NAND :-

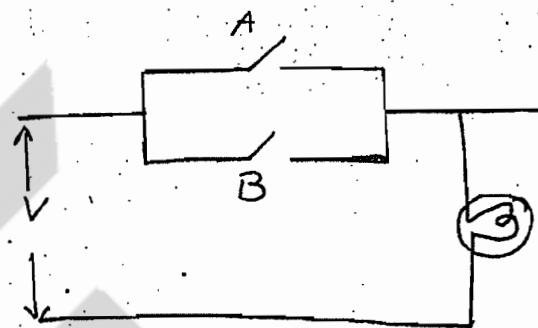
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



$$Y = \overline{AB}$$

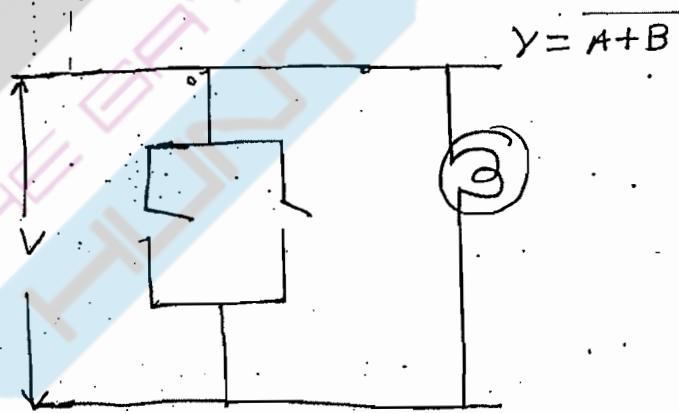
(e) OR :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

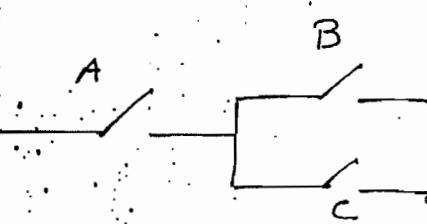


$$Y = A + B$$

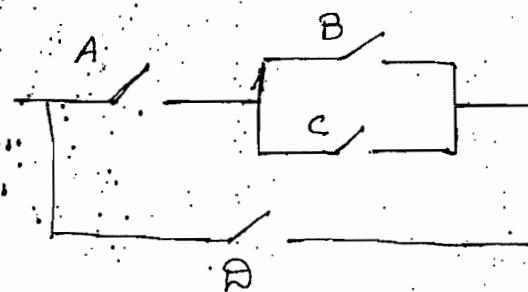
(f) NOR :-



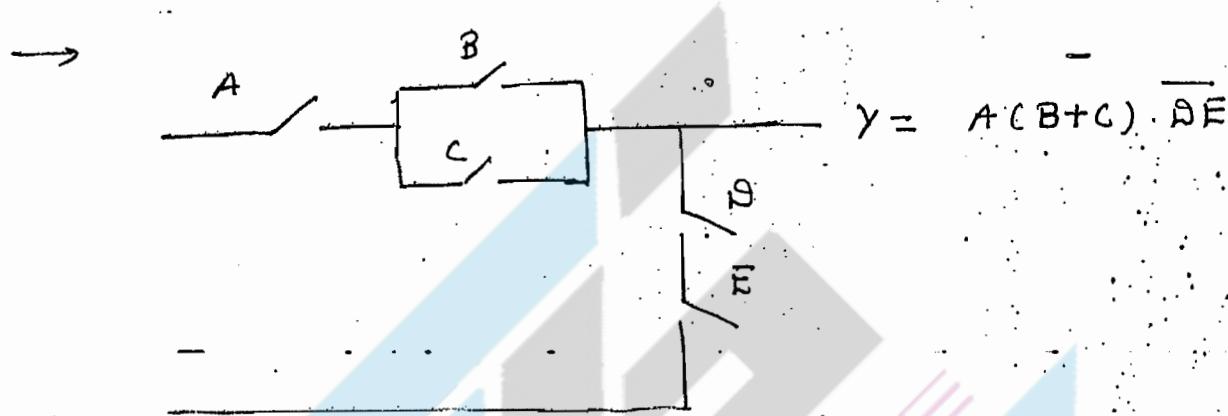
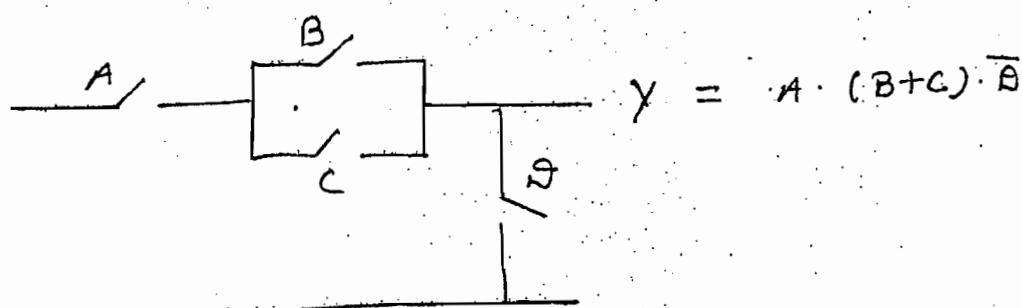
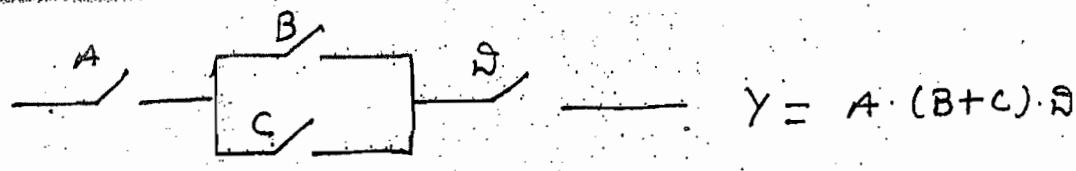
$$Y = \overline{A+B}$$



$$Y = A(B+C)$$



$$Y = A(B+C) + D$$



Statements:-

Ques:- A logic ckt have three i/p A, B, C & o/p Y  
Y is logic 1 for the following combination

- (1) A and C are true (logic 1)  $\rightarrow$
- (2) B and C are false
- (3) A, B and C are true
- (4) A, B and C are false

Soln:- then minimize o/p Y

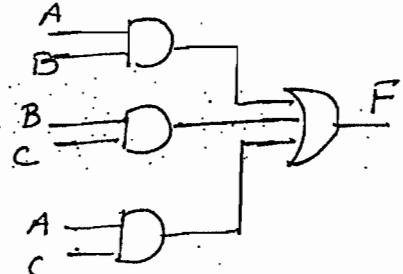
A	B	C	Y	F
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

$$\begin{aligned}
 Y &= AC + \bar{B}\bar{C} + ABC + A\bar{B}\bar{C} \\
 &= AC(1+B) + \bar{B}\bar{C}(1+A) \\
 &= AC + \bar{B}\bar{C}
 \end{aligned}$$

Ques:- A logic ckt has 3 i/p's & o/p F. O/P is logic 1 when majority no. of i/p's are logic 1. The minimise exp. for o/p F is

Soln:-

$$\begin{aligned}
 F &= \bar{A}BC + A\bar{B}C + ABC + A\bar{B}\bar{C} \quad \text{Alternatively} \\
 &= (\bar{A}B + A\bar{B})C + AB \\
 &= \bar{A}BC + A\bar{B}C + AB \\
 &= BC + AC + AB
 \end{aligned}$$



### LOGIC GATES

NOT  
AND  
OR

Basic gates

NAND  
NOR

Universal gate

EXOR  
EXNOR

Used in

- (I) Arithmetic circuits
- (II) Comparators
- (III) Parity generators / checker
- (IV) Code converter.

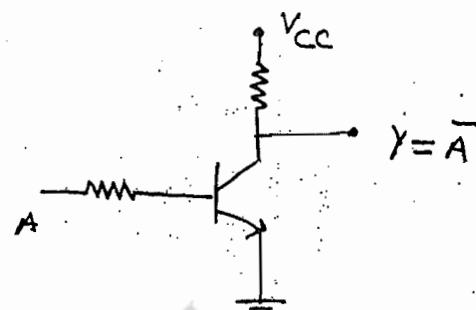
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NOT Gate :-

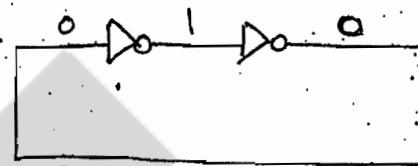
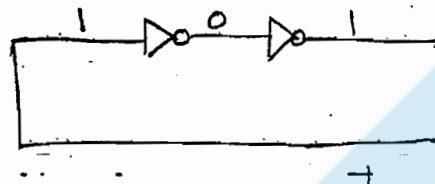


$$A \rightarrow \text{NOT} \rightarrow Y = \bar{A}$$



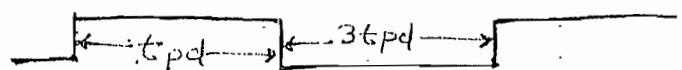
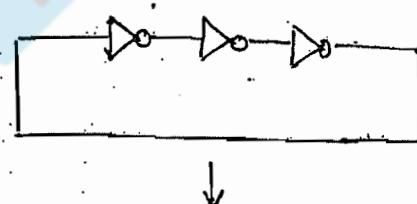
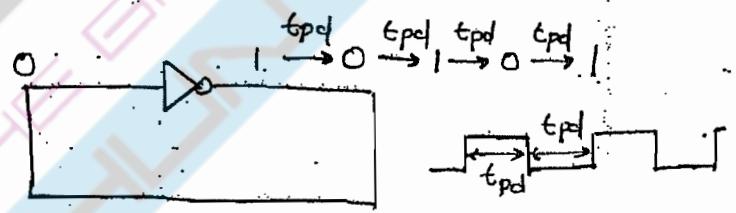
A	Y
0	1
1	0

→ Basic Memory ckt



Bistable Multivibrator (Two stable states  
(even no. of not gate) (0,1)

- (odd. no. of not gate)
- Astable Multivibrator
- Free Running ckt.
- Square Wave generator
- Clock generator
- Ring oscillator
- $T = 2Nt_{pd}$



where  $N$  = No. of gates in feedback

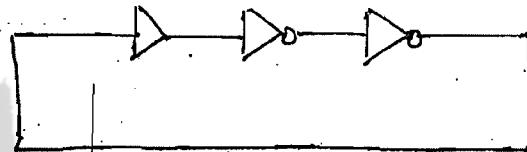
$$f = \frac{1}{T}$$

→ In Ring oscillator time period of generated square wave  $t_{\text{os}}$

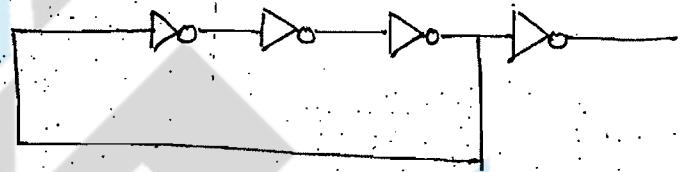
$$T = 2N t_{\text{pd}}$$

where  $N$  = no. of gates in feedback

→ Bistable multivibrator

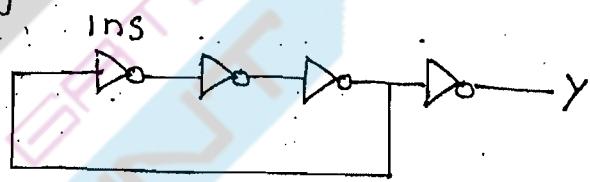


→ Astable multivibrator



Ques:- In the ckt shown in figure

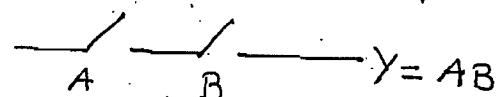
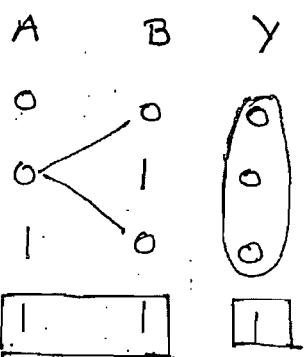
Find  $T$



Soln:- If  $T = 6 \text{ ns}$

→ The last not gate provide only delay and it doesn't change the time period.

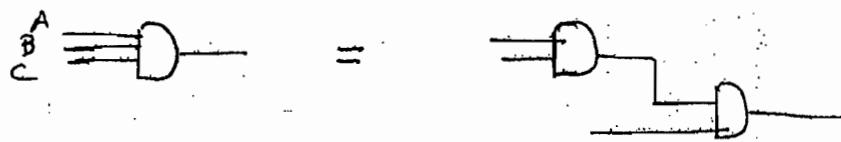
Ans Gate:-



→ Schmitt switch



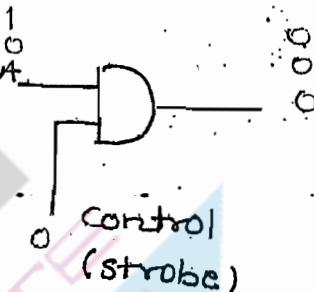
→ Follows commutative law



$$ABC = (AB)C = (AC)B = (BC)A \rightarrow \text{Associative Law}$$

→ Follows both commutative and associative law

- 0 → Disable (o/p doesn't change)
- 1 → Enable (o/p change)

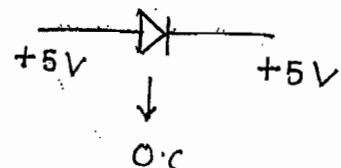
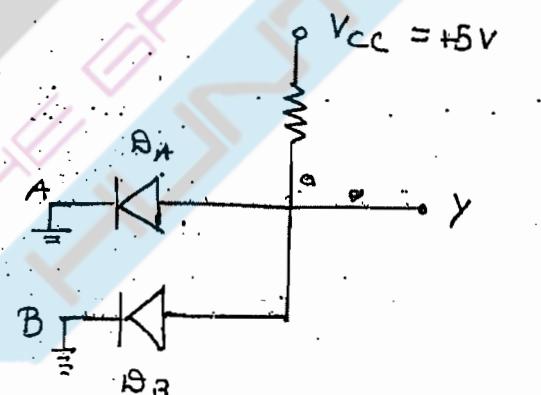


### ANS Gate Using Diode

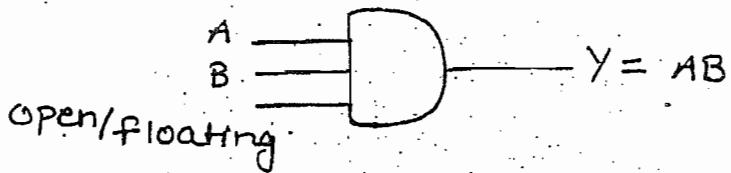
logic 0  $\rightarrow$  0V

logic 1  $\rightarrow$  5V

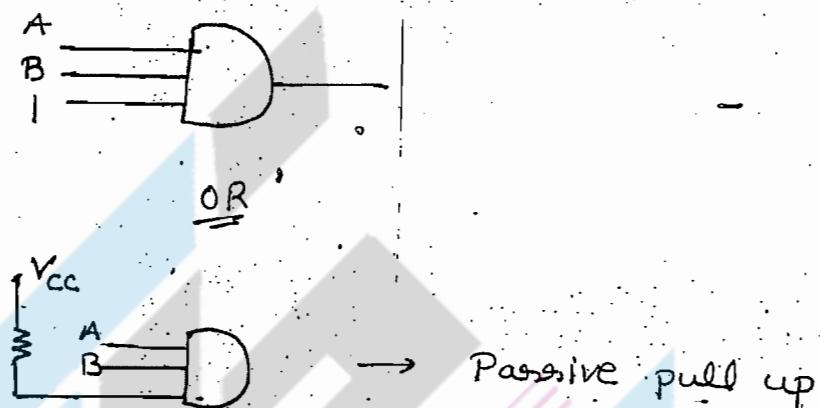
A	B	$S_A$	$S_B$	Y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1



→ Positive logic AND gate



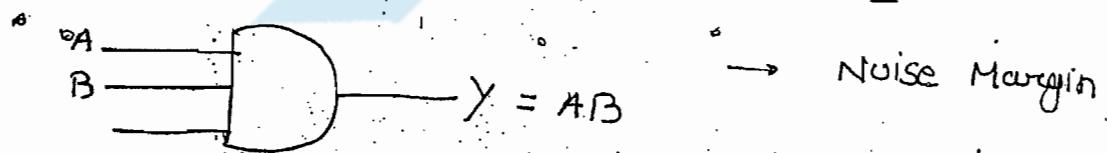
- In TTL logic circuits, if any i/p is open or floating then it acts as logic 1
- In ECL gate logic circuits floating i/p acts as logic '0'
- The unused i/p in ANS gate
  - (i) can be connected to logic '1' or pull up



- (ii) can be connected to one of used i/p



- (iii) If it is TTL gate then unused i/p can be open or float



Among these best way of connecting unused i/p in ANS gate is connecting to logic 1 or pull up.

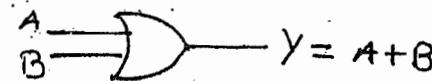
Note:-

- |                        |                               |                          |
|------------------------|-------------------------------|--------------------------|
| (I) symbol             | (II) Logical exp.             | (III) Truth Table        |
| (IV) Switch            | (V) Comm/Associate            | (VI) Enable/Disable      |
| (VII) Unused i/p       | (VIII) Diode                  | (IX) Transistor (X) Gate |
| (X) Alternative Symbol | (XI) Min.no. of NAND/NOR /MUX |                          |

OR Gate:-

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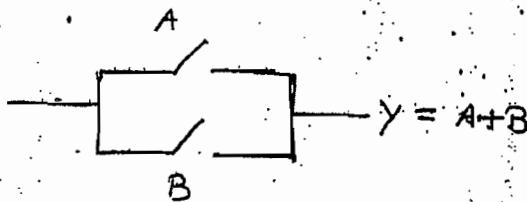
A	B	Y
0	0	0
0	1	1
1	0	1



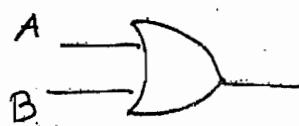
→ Enable  $\rightarrow 0$

→ Disable  $\rightarrow 1$

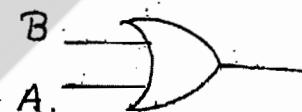
→ Parallel switches



→ Follows commutative law

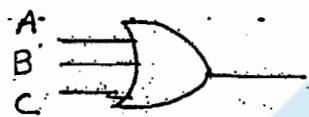


=



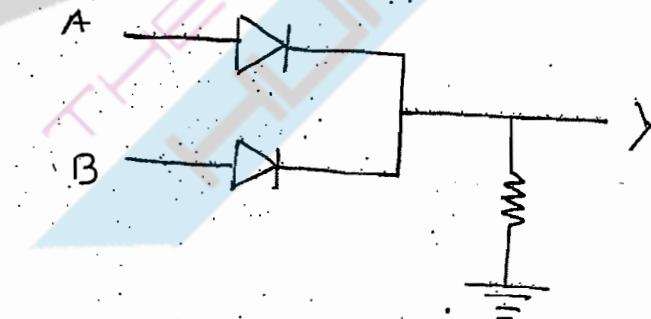
$$A+B = B+A$$

→ Follows associative law



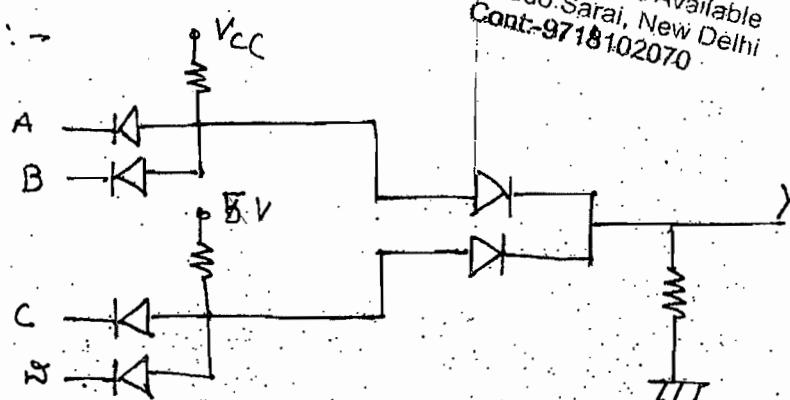
→ Using Diode Ckt :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



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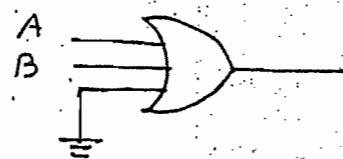
Ans:-



$$\text{Ans: } Y = AB + BC$$

→ The unused I/p in OR gate

- (i) can be connected to logic '0' or pull down

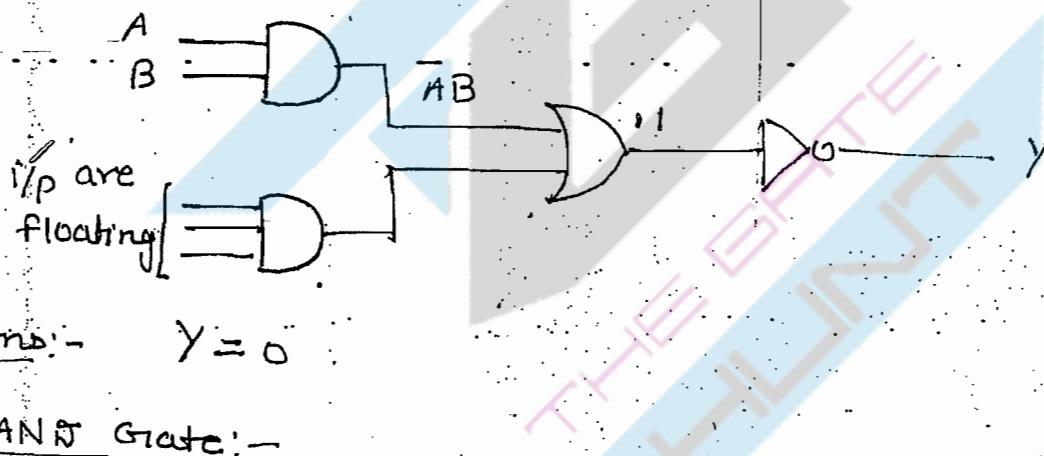


- (ii) Can be connected to one of used I/p



- (iii) If it is ECL gate then unused I/p can be open or float

Ques:- The ckt shown in fig. is TTL ANA-OR-Inverter (AOI) for given I/p , O/p = ?



Ans:-  $Y = 0$

NAND Gate:-



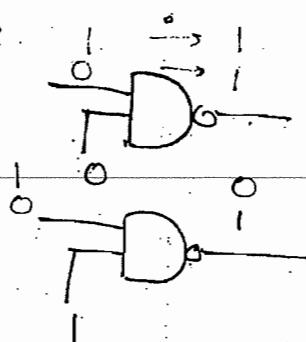
NAND → Bubbled OR =



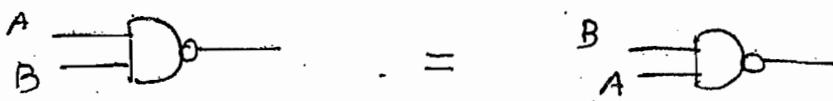
→ Enable  $\Rightarrow 1$

ANH  $\rightarrow 0 \rightarrow$  disable

NANB  $\rightarrow 1 \rightarrow$  enable

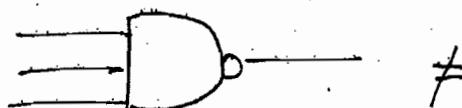


→ Follows commutative law

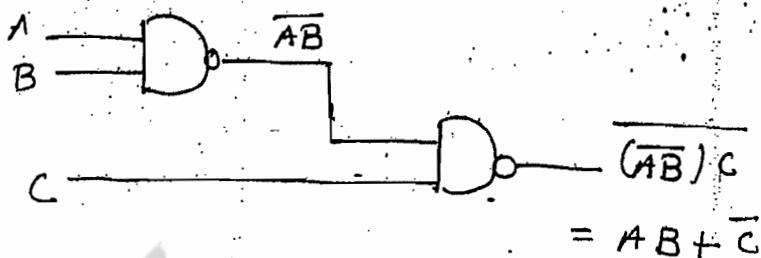


$$\overline{AB} = \overline{BA}$$

→ Doesn't follow associative law



≠



$$= AB + C$$

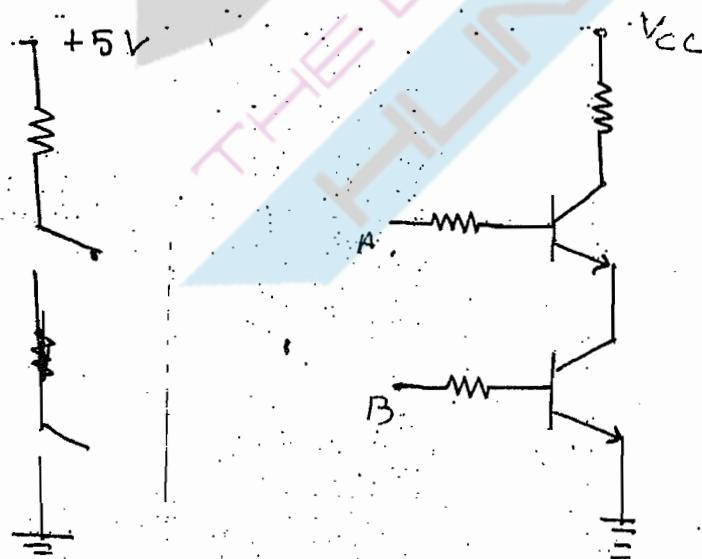
→ Truth Table :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

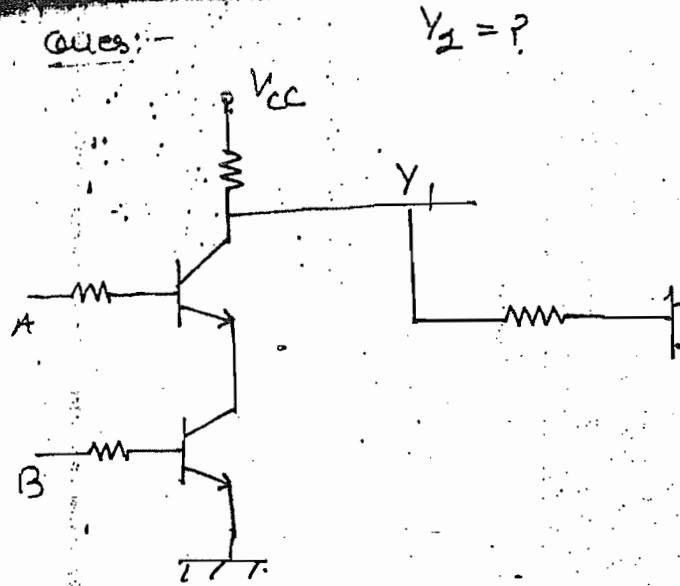
→ Series switches in parallel



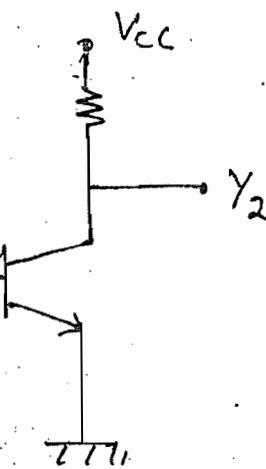
→ Using Diode Ckt :-



→ Unused I/P in NAND gate can be connected similar to unused I/P in AND gate



$$Y_2 = ?$$



Ans:-

$$Y = AB$$

NOR Gate :-

$$Y = \overline{A+B} = \overline{A} \cdot \overline{B}$$

Alternative symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

-OR

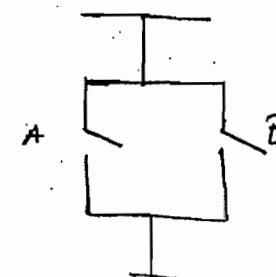
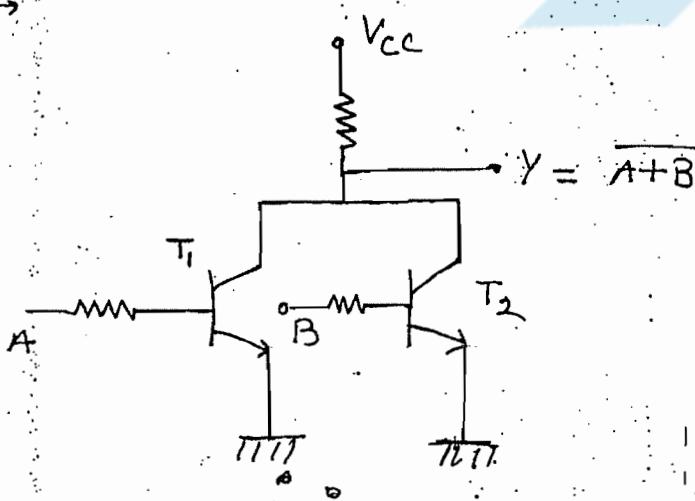
NOR

0 → Enable

1 → disable

→ Follows commutative law but doesn't follow associative law

→

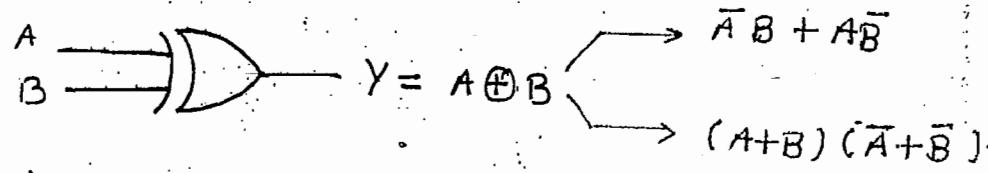


→ Except EXOR / EXNOR, all gates are present more than two i/p. (Multiple i/p)



→ In NOR gate unused i/p can be connected to similar to OR gate

• Exclusive OR → EXOR → XOR :-



A	B	Y
0	0	0
0	1	1
1	0	1

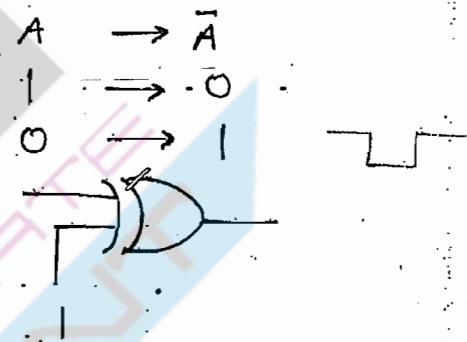
$$A = B \Rightarrow 0$$

$$A \neq B \Rightarrow 1$$

1	1	0
---	---	---



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(Inverter)

$$\rightarrow A \oplus A = 0$$

$$\Rightarrow A \oplus 0 = A$$

$$\rightarrow A \oplus \bar{A} = 1$$

$$\Rightarrow A \oplus 1 = \bar{A}$$

→ Follows commutative Law

$$A \oplus B = B \oplus A$$

→ Follows associative law

$$A \oplus B \oplus C = (A \oplus B) \oplus C$$

Soln:- Let  $A \oplus B = C$  then  $A \oplus C$ ,  $B \oplus C$ ,  $A \oplus B \oplus C$

Ans:-  $A \oplus C = B$        $B \oplus C = A$        $\underbrace{A \oplus B \oplus C}_{C} = 0$

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$$\rightarrow A \oplus A = 0$$

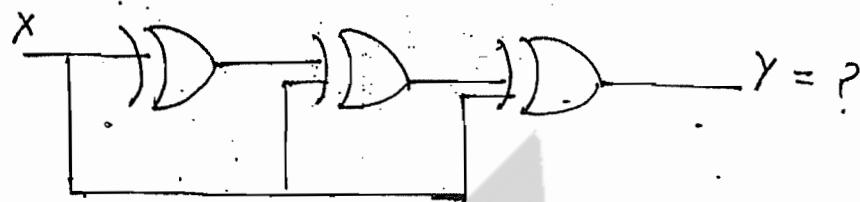
$$\rightarrow A \oplus A \oplus A = A$$

$$\Rightarrow A \oplus A \oplus A \oplus A = 0$$

$\rightarrow$  Odd no. of A then result = A

$\rightarrow$  Even no. of A then result = 0

Ques:-



$$\text{Ans:- } Y = 0$$

$$\text{Ques:- } A \oplus B \oplus AB = ?$$

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

$\rightarrow$  In EX-OR gate o/p is logic '1' when no. of one's in the i/p is odd. Hence it is known as odd no. of 1's detector ckt.

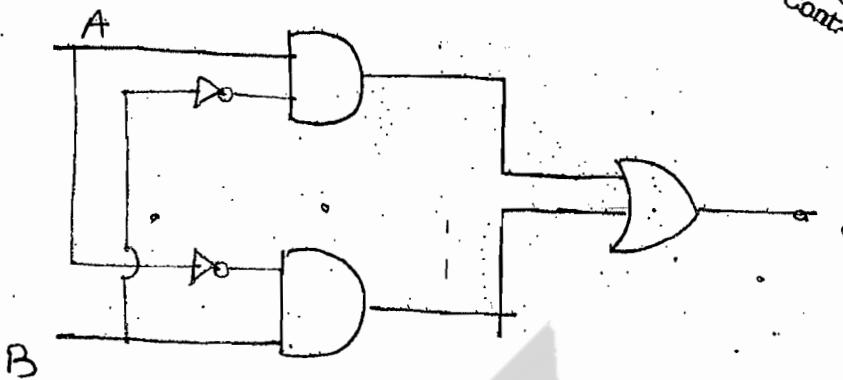
A	B	C	$Y = A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \sum m(1, 2, 4, 7)$$

- If  $n$ -variable XOR gate contains no. of minterms or max terms =  $2^{n-1}$

Internal diagram :-



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- EXOR/ENOR gates are available only with two i/p

Even Parity Generator



A	B	P
0	0	0
0	1	1
1	0	1
1	1	0

Parity checker (odd)

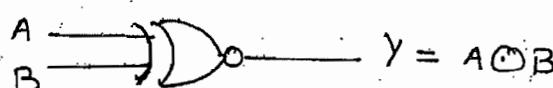


If all i/p are odd 1's

- EXOR gate is known as even parity generator and odd parity checker ckt.

Parity → including i/p + Parity

EX-NOR :-



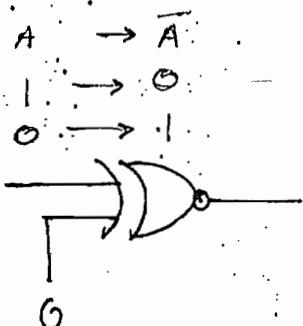
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

$$Y = A \oplus B \rightarrow \bar{A}\bar{B} + AB$$

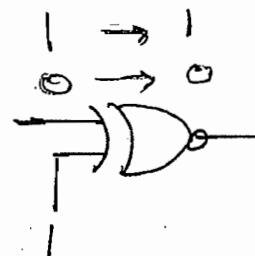
$$\rightarrow (A+\bar{B})(\bar{A}+B)$$

$\rightarrow A = B \Rightarrow$  coincidence logic ckt ( I/p are same)  
 $\rightarrow A \neq B \Rightarrow$  Equivalence logic ckt

$$A \neq B \Rightarrow \text{O/p} = 0$$



(Inverter)



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$\rightarrow$  EX-NOR gate follows commutative law but not associative law.

$$A \oplus B = B \oplus A$$

$$A \oplus B \oplus C \neq (A \oplus B) \oplus C$$

$$\rightarrow A \oplus A = 1 \Rightarrow A \oplus 1 = A$$

$$\rightarrow A \oplus \bar{A} = 0 \Rightarrow A \oplus 0 = A$$

Ques:- If  $A \oplus B = C$  then

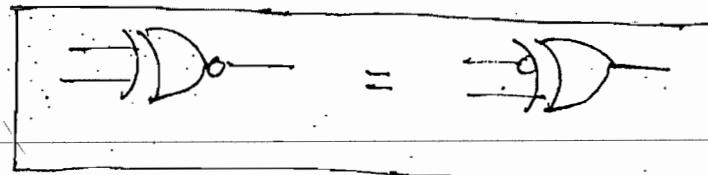
Soln -  $A \oplus C = B$  ,  $B \oplus C = A$

$$\boxed{A \oplus B \oplus C = 0}$$

$$\rightarrow A \oplus \bar{B} = A \oplus B$$

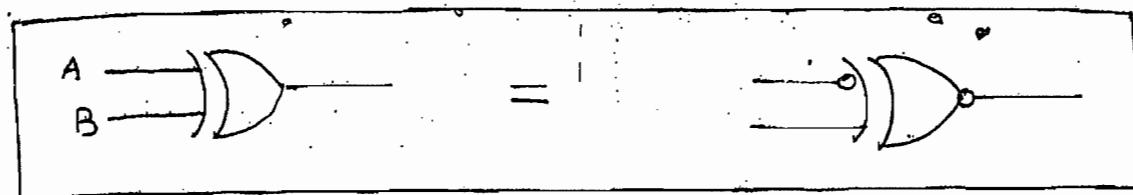
Alternate Symbol

$$\rightarrow \bar{A} \oplus \bar{B} = A \oplus B$$



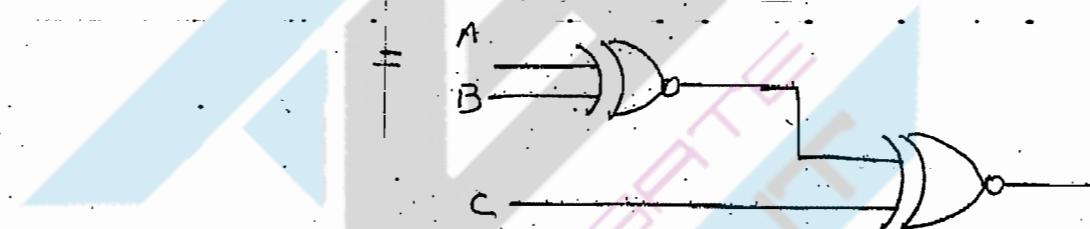
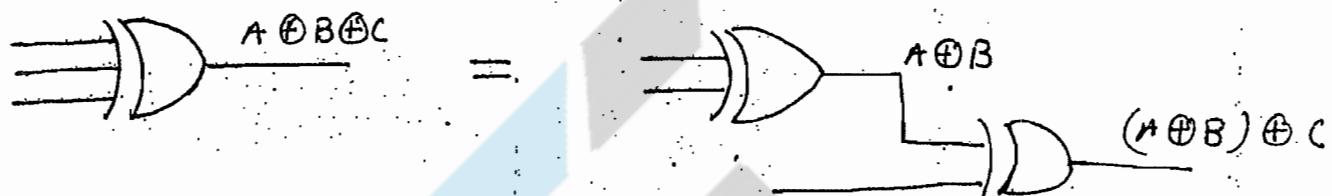
$$\rightarrow A \odot \bar{B} = A \oplus B$$

$$\rightarrow \bar{A} \odot \bar{B} = A \odot B$$



$$\rightarrow A \odot B \odot C = \overline{A \oplus B \oplus C}$$

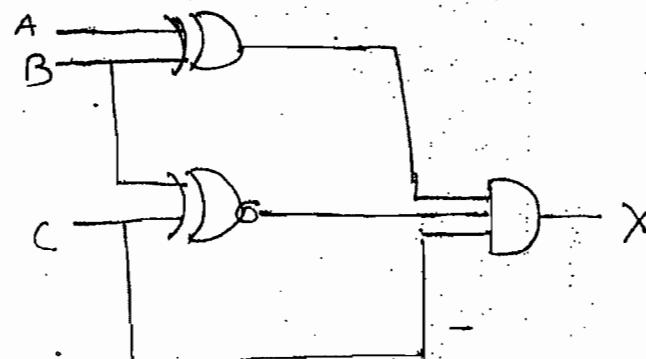
$$= \overline{(A \oplus B) \oplus C} = \overline{(A \odot B) \odot C}$$



$$\rightarrow A \oplus B \oplus C \rightarrow (A \oplus B) \oplus C$$

$$\rightarrow (A \odot B) \odot C$$

Ques:- In the ckt shown in fig. to provide o/p  $X = Y$   
I/p A, B, C respectively



(A) 101

(B) 011

(C) 110

(D) 111

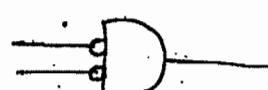
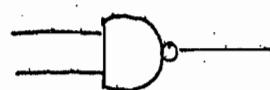
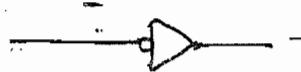
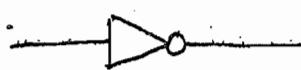
→ In XNOR gate O/p for logic '1' when no. of 1's in the i/p is even no. of 1's.

A	B	C	$Y = A \oplus B \oplus C$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

A	B	C	$Y = \overline{A \oplus B} \odot C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

## Logic Gate

## Alternative symbol



NAND as Universal gate:-

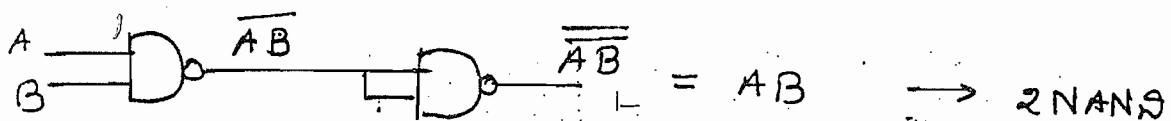
(1) NOT Gate:-

$$\begin{array}{c} \text{A} \\ \text{---} \\ \text{D} \end{array} \quad A \cdot \overline{A} = \overline{A}$$

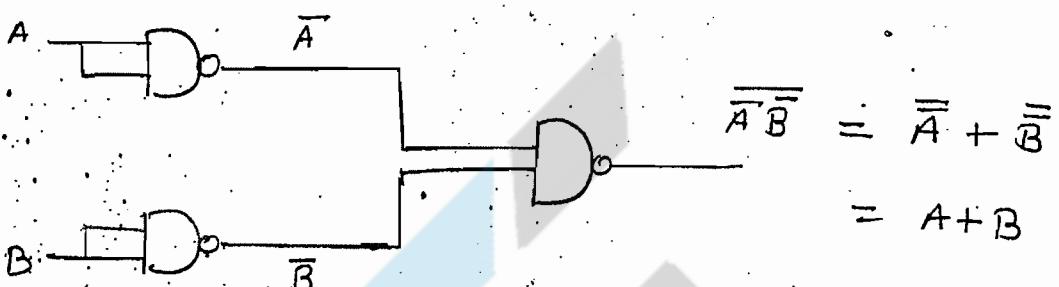
→ INAND

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(II) ANS :-



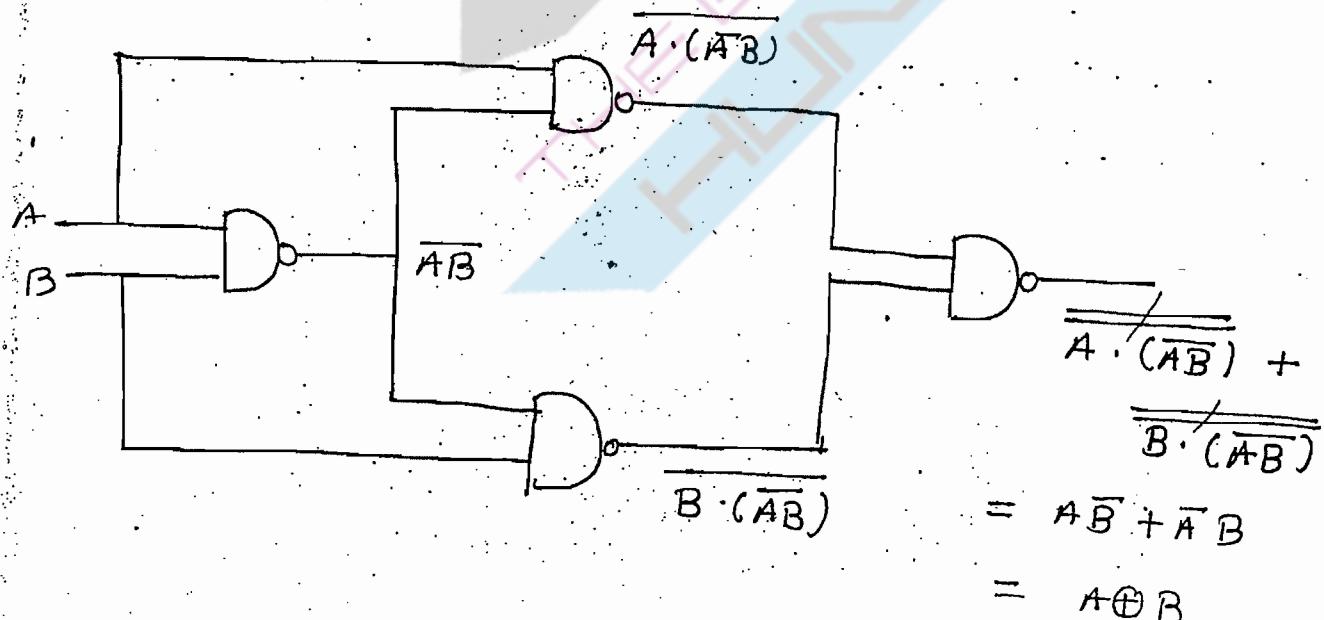
(III) OR :-



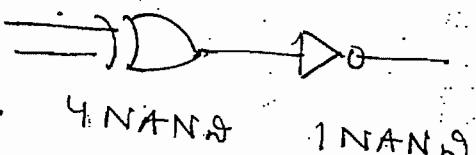
(IV) NOR :-

→ 4 NANDS

(V) EX-OR :-

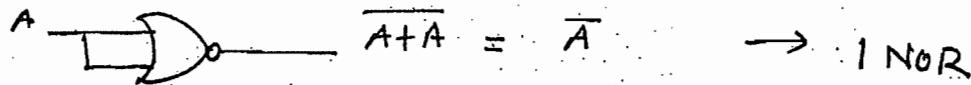


(VI) EX-NOR :-



## NOR as Universal :-

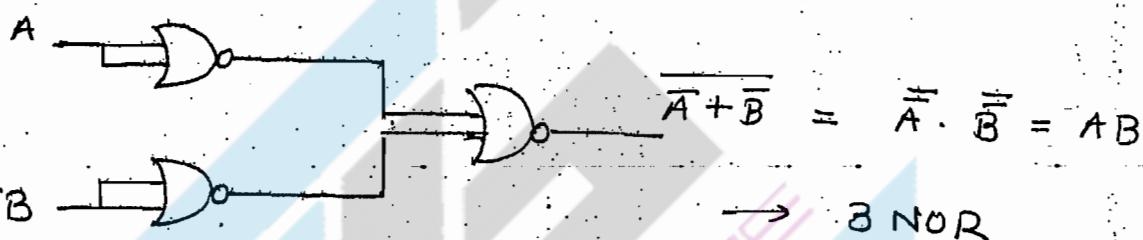
(i) NOT Gate :-



(ii) OR Gate :-



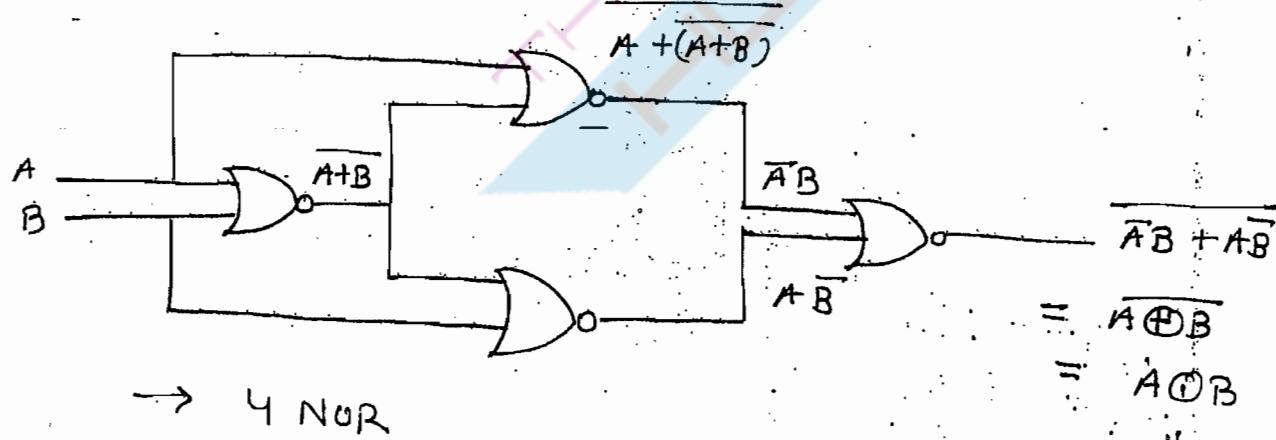
(iii) AND :-



(iv) NAND :-

→ 4 NOR

(v) EX-NOR :-



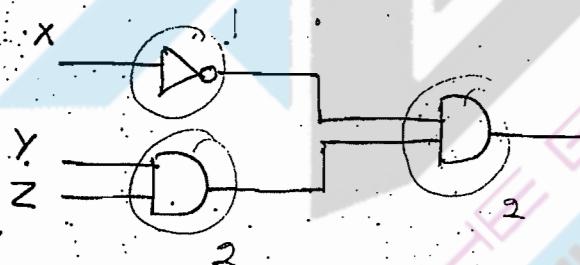
(vi) EX-OR :-

→ 5 NOR

Logic Gates	No. of NANDs	No. of NORs
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4
NOR	4	1
NAND	1	4

Ques!:- To implement  $\overline{XYZ}$  Min. no. of two i/p NAND gates used (A) 3 (B) 4 (C) 5 (D) 7

Soln!:-



Ques!:- To implement  $AB + CD$  Min. no. of NAND

Ans.



Note:-

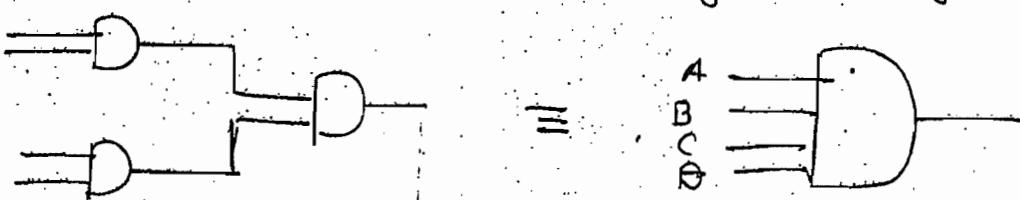
→ Two level AND-OR = Two level NAND-NAND

→ NAND-NAND is preferred over AND-OR

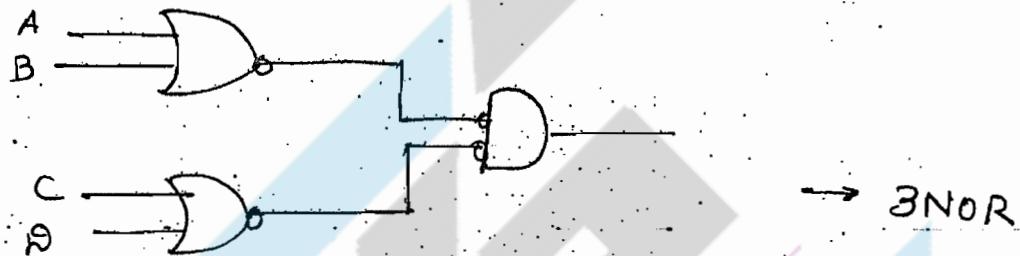
→ SOP exp. can be implemented with min. no. of NAND gate

Degenerative:-

→ Level changed but gate doesn't change



Ques:- To implement  $(A+B)(C+E+F)$  . Min. no. of NOR gate



Two level OR-AND = two level NOR-NOR

POS → Min. no. of NOR

Ques:- To implement  $A+BC$  . Min. no. of NAND  
or NOR

Ans:- NAND → 3      NOR → 3

Ques:- To implement  $(\bar{X}+\bar{Y})(W+Z)$  . Min. no. of  
two i/p NAND

(A) 3

(B) 4

(C) 5

(D) 6

## Number System :-

- (i) conversion
- (ii) Arithmetic operation
- (iii) Complements.

### Codes :-

- |             |                 |
|-------------|-----------------|
| → Gray Code | → Excess 3 code |
| → BCD code  | → 2421 code     |

### Data representation :-

↓ true, -ve

- (i) sign magnitude
- (ii) 1's complement
- (iii) 2's complement

### → Conversion :-

→ A number system with base  $r$  will have  $\text{eg}^r$  different digit and they are from 0 to  $(r-1)$

#### Number System

Binary (2)

0, 1

Octal (8)

0, 1, 2, ..., 7

decimal (10)

0, 1, 2, ..., 9

Hexadecimal (16)

0, 1, ..., 9, A, B, C, D, E, F

4

0, 1, 2, 3

6

0, 1, ..., 5

12

0, 1, ..., 9, A, B

### → Decimal to other

$$( \dots )_{10} \xrightarrow{\hspace{1cm}} ( \dots )_r$$

$$(x_2 \ x_1 \ x_0 \cdot y_1 \ y_2)_{10} \quad \text{---} \quad (\quad )_r$$

$$r \mid x_2 \ x_1 \ x_0$$

$$(y_1 \ y_2) \times 10$$

→ To convert decimal to any base  $r$ , divide integer part & multiply fraction part with base  $r$

$$\text{eg:- } (19.125)_{10} \quad \text{---} \quad (\quad )_2$$

$$2 \mid 19$$

$$2 \mid 9-1$$

$$2 \mid 4-1$$

$$2 \mid 2-0$$

$$2 \mid 1-0$$

$$2 \mid 0 \div 1$$

$$(19)_{10} \rightarrow (10011)_2$$

$$0.125 \times 2 = 0.25 \rightarrow 0$$

$$0.25 \times 2 = 0.50 \rightarrow 0$$

$$0.50 \times 2 = 1.0 \rightarrow 1$$

$$(19.125)_{10} \quad \text{---} \quad (10011.001)_2$$

$$\rightarrow (27.625)_{10} \quad \text{---} \quad (\quad )_8$$

$$8 \mid 27$$

$$8 \mid 3-3$$

$$8 \mid 0-3$$

$$(27)_{10} \quad \text{---} \quad (33)_8$$

$$0.625 \times 8 = 5.000$$

$$\rightarrow (27.625)_{10} \quad \text{---} \quad (\quad )_{16}$$

$$16 \mid 27$$

$$16 \mid 1-B$$

$$16 \mid 0-1$$

$$0.625 \times 16 = 10.000$$

$$= A$$

$$(1B.A)_{16}$$

$$\rightarrow (127.5)_{10} \longrightarrow (\quad)_{16}$$

$$\begin{array}{r} 16 | 127 \\ \hline 16 | 7 - F \\ \hline 0 - 7 \end{array} \quad 0.5 \times 16 = 8.00$$

$(7F.8)_{16}$

$$\rightarrow (27)_{10} \longrightarrow (\quad)_4$$

$$\begin{array}{r} 4 | 27 \\ \hline 4 | 6 - 3 \\ \hline 4 | 1. - 2 \\ \hline 0 - 1 \end{array} \quad (123)_4$$

(2) Others to Decimal :-

$$(x_2 x_1 x_0 \cdot x_{-1} x_{-2})_r \longrightarrow (\quad)_{10}$$

$$x_2 r^2 + x_1 r^1 + x_0 r^0 + x_{-1} r^{-1} + x_{-2} r^{-2} + \dots$$

$$\rightarrow (10111.11)_2 \longrightarrow (\quad)_2$$

$$1 \times 2^4 + 0 + 1 \times 2^2 + 1 \times 2^1 * 1 + 1 \times 2^{-1} + 1 \times 2^{-2}$$

$$16 + 4 + 2 + 1 + \cancel{+ 5\frac{1}{2}} + \cancel{+ 7\frac{1}{4}}$$

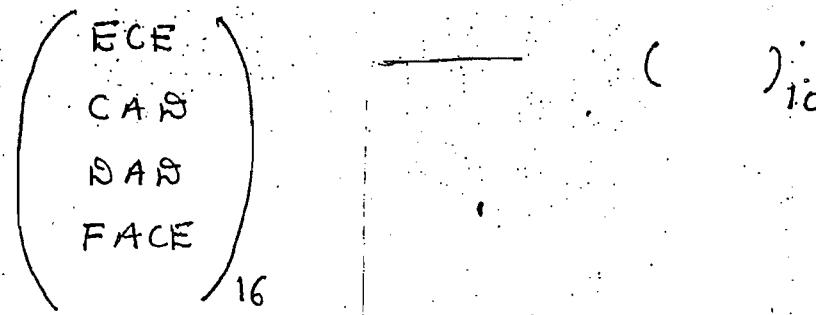
$$(23.75)_2$$

$$\rightarrow (-5.4)_8 \longrightarrow (61.5)_{10}$$

$$\rightarrow (B4D)_{16} \longrightarrow (2989)_{10}$$

$$11 \times 256 + 10 \times 16 + 13 \times 1$$

Ans:-



(III) Octal to Binary :-

$$8 \longrightarrow 2^3$$

each octal digit  $\rightarrow$  3 bit binary

$$0 \longrightarrow 000$$

$$1 \longrightarrow 001$$

$$2$$

$$3$$

$$4$$

$$5$$

$$6$$

$$7 \longrightarrow 111$$

$$(275.36)_8 \longrightarrow ( )_2$$

010 111 101. 011 110

(IV) Binary to Octal :-

$\rightarrow$  Group of 3bit into one digit in octal

$$(275.36)_8 \longrightarrow ( )_2$$

010 011 101. 101100<sub>2</sub>

(133.54)<sub>8</sub>

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(V). Hex to Binary:-

$$16 \rightarrow 2^4$$

$$0 \rightarrow 0000$$

$$F \rightarrow 1111$$

Ques:- No. of 1's present in binary form of  $(CAB)_{16}$ .

Soln:-

$$\begin{array}{ccc} C & A & B \\ \downarrow & \downarrow & \downarrow \\ 1100 & 1010 & 1101 \\ \bullet & \bullet & \bullet \end{array}$$

(VI). Binary to Hex:-

→ Gp of 4 bits  $\Rightarrow$  one hex digit.

$$\rightarrow 00011010 \cdot 11101000$$

$$(1.A.E8)_{16}$$

$$\rightarrow (1.1)_2 \quad \rightarrow (1.8)_{16}$$

$$0001 \cdot 1000 \rightarrow (1.8)_{16}$$

(VII). Hex to Octal:-

$$\begin{array}{ccc} \nearrow & \nearrow & \nearrow \\ \text{Binary} & & \\ \downarrow & \downarrow & \downarrow \\ 1101 & 1100 & 1101 \end{array} \quad (DAS)_{16} = ( )_8$$

$\rightarrow 6655$

## Arithmetic Operation on number system:-

(i) Binary System

(ii) Octal System

(Add, sub, Mult)

(Add, sub)

(iii) Hex (Add, sub)

(iv)  $\times$  (base) (Add, sub)

### Binary Addition:-

$$0+0 = 0$$

$$\begin{array}{r} 111001 \\ 101101 \end{array}$$

$$0+1 = 1$$

$$\begin{array}{r} 111001 \\ 101101 \end{array}$$

$$1+1 = 10$$

$$\begin{array}{r} 111001 \\ 101101 \end{array}$$

$$1+1+1 = 11$$

$$\begin{array}{r} 111001 \\ 101101 \end{array}$$

### Binary subtraction:-

$$\begin{array}{r} 11011 \\ 10110 \\ \hline 00100 \end{array}$$

### Binary Multiplication:-

$$(1011)_2 \times (1101)_2$$

$$\begin{array}{r} 1011 \\ 0000 \times \\ 1011 \times x \\ 1011 \times x x \\ \hline 10001111 \end{array}$$

Ques:- Multiply  $(111)_2 \times (111)_2$

Soln:-

$$\begin{array}{r} 111 \\ 111 \times \\ 111 \times x \\ 111 \times x x \\ \hline 11100001 \end{array}$$

### Octal System:-

$$0 \quad 1 \quad 2 \quad \dots \quad 7$$

$$10 \quad 11 \quad 12 \quad 13 \dots 17, 21, 22$$

$$\downarrow \quad \downarrow \quad \downarrow$$

$$8$$

$$9$$

$$10$$

$$1+1=2$$

$$7+1=10$$

Add:-

$$1+2=3$$

$$7+2=11$$

$$2 \quad 6 \quad 7 \quad 3$$

$$1+6=7$$

$$7+3=12$$

$$5 \quad 4 \quad 6 \quad 2$$

$$1+7=10$$

$$7+7=16$$

$$10 \quad 3 \quad 5 \quad 5$$

$$\begin{array}{r} 8 \quad 13 \\ 8 \quad 15 \\ \hline 0 \quad 1 \end{array}$$

### Octal subtraction:-

$$\begin{array}{r}
 7 \ 6 \ 5 \ 4 \\
 - 2 \ 3 \ 5 \ 2 \\
 \hline
 5 \ 3 \ 0 \ 2
 \end{array}$$

$$\begin{array}{r}
 7 \ 3 \ 2 \ 4 \\
 - 1 \ 6 \ 5 \ 3 \\
 \hline
 5 \ 4 \ 5 \ 1
 \end{array}$$

### Hexadecimal :-

0-9, A, B, C, D, E, F, 10, 11, 12

### Addition:-

$$1 + 1 = 2$$

$$1 + 2 = 3$$

:

$$1 + 8 = 9$$

$$1 + 9 = A$$

$$1 + A = B$$

$$1 + B = C$$

:

$$A + A = 14$$

$$F + F = 1E$$

$$A + A$$

$$\begin{array}{r}
 16 | 20 \\
 16 | 1-4 \\
 \hline
 0-1
 \end{array}$$

$$F + F$$

$$\begin{array}{r}
 16 | 30 \\
 16 | 1-14-E \\
 \hline
 0-1
 \end{array}$$

### Sum of two Hex No :-

$$\begin{array}{r}
 5 \ 6 \ 8 \ 9 \\
 + 7 \ 5 \ 4 \ 3 \\
 \hline
 C \ B \ C \ C
 \end{array}$$

$$\begin{array}{r}
 2 \ 6 \ 8 \ 9 \\
 + 5 \ 4 \ 7 \ 6 \\
 \hline
 7 \ A \ F \ F
 \end{array}$$

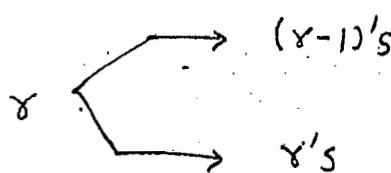
$$\begin{array}{r}
 A \ B \ B \\
 B \ A \ B \\
 \hline
 1 \ 8 \ 8 \ A
 \end{array}$$

### Subtraction:-

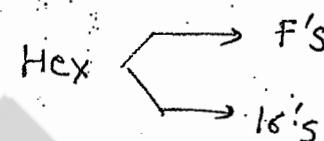
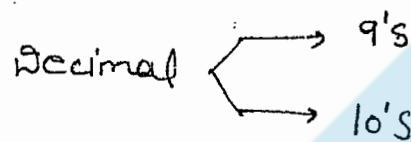
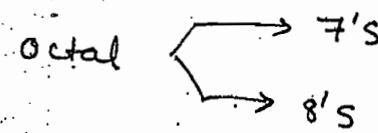
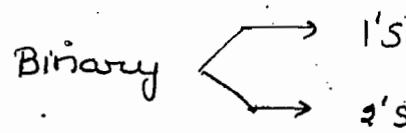
$$\begin{array}{r}
 9 \ 6 \ 5 \ 4 \\
 - 2 \ 6 \ 7 \ 3 \\
 \hline
 6 \ F \ E \ 1
 \end{array}$$

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## • Complements:-



A number system with base  $r$ , having two types of complements i.e.  $(r-1)$  compliment &  $r$ 's compliment



## 1's Complement:-

$$\rightarrow \begin{array}{r} 111111 \\ 110010 \\ \hline 001100 \end{array} \rightarrow \text{Max. No.}$$

To determine  $(r-1)$ 's complement, first write max. no. in given base then subtract the no.

## 7's Complement:-

$$\rightarrow \text{Octal No.} = 2673$$

$$\begin{array}{r} 7777 \\ 2673 \\ \hline 5104 \end{array}$$

## 9's Complement:-

$$\rightarrow 2689$$

$$\begin{array}{r} 9999 \\ 2689 \\ \hline 7310 \end{array}$$

F's compliment :-

→ 3579

$$\begin{array}{r}
 F F F F \\
 3 5 7 9 \\
 \hline
 C A 8 6
 \end{array}$$

X's compliment :-

→ To determine X's compliment, first write (X-1)'s compliment and add '1' to LSB (right most place)

2's compliment :-

$$\begin{array}{r}
 1 1 0 1 0 1 0 \\
 \hline
 2's compliment 0 0 1 0 1 1 0
 \end{array}$$

scanning upto first one  
and after that  
complement

1's compliment

0 0 1 0 1 0 |

|

2's

$$\begin{array}{r}
 1 1 0 1 0 1 1 \\
 \hline
 0 0 1 0 1 1 0
 \end{array}$$

→

$$\begin{array}{r}
 1 1 0 1 0 1 1 \\
 \hline
 0 0 1 0 1 1 0
 \end{array}$$

$$\begin{array}{r}
 0 0 1 0 1 1 0 \\
 \hline
 1
 \end{array}$$

$$\begin{array}{r}
 0 0 1 0 1 1 0 \\
 + 1 \\
 \hline
 1 0 1 0 1 0 1
 \end{array}$$

→ 1's

$$\begin{array}{r}
 1 0 1 0 1 0 1 \\
 + 1 \\
 \hline
 1 0 1 0 1 0 1
 \end{array}$$

→ 2's

Ques:- Determine 8's compliment 2670

Soln -

$$\begin{array}{r}
 7 7 7 7 \\
 \hline
 2 6 7 0
 \end{array}$$

$$\begin{array}{r}
 5 1 0 7 \\
 \hline
 2 6 7 0
 \end{array}$$

→ 7's.

8's

$$\begin{array}{r}
 1 \\
 \hline
 5 1 1 0
 \end{array}$$

→ 8's

Ques:- Determine 10's complement of 2690

Soln:-

$$\begin{array}{r} 9' \rightarrow 9 \ 9 \ 9 \ 9 \\ 2 \ 6 \ 9 \ 0 \\ \hline 7 \ 3 \ 0 \ 9 \\ 1 \\ \hline 7 \ 3 \ 1 \ 0 \end{array}$$

Ques:- Determine 16's complement of 2689

Soln:-

$$\begin{array}{r} 16' \rightarrow F \ F \ F \ F \\ 2 \ 6 \ 8 \ 9 \\ \hline 8 \ 9 \ 7 \ 6 \\ 1 \\ \hline 8 \ 9 \ 7 \ 7 \end{array}$$

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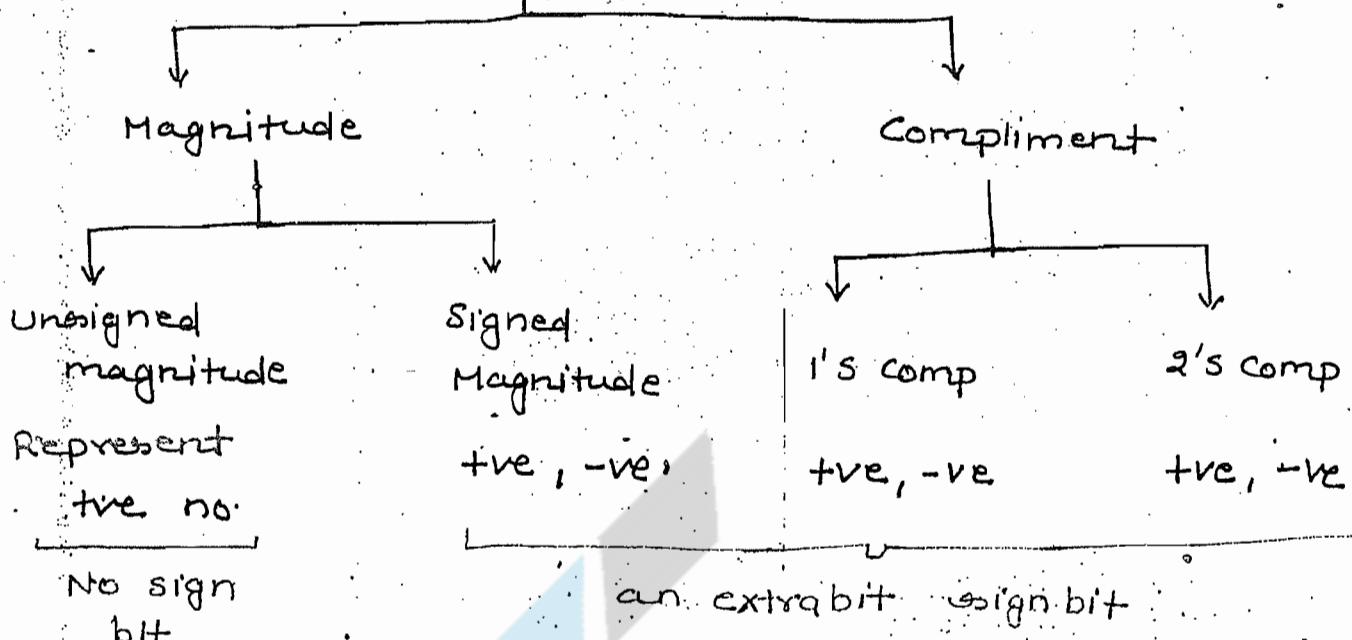
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## Data Representation



+5 in all system:-

+5 101 0101 0101 0101

→ compliment<sup>o</sup> are used only for -ve No.

-5 → For signed magnitude, separate sign and mag.  
(8 bit) put zero b/w them

→ For 1's & 2's copy MSB

$$\textcircled{a} \quad -5 \text{ (8 bits)} \quad x \quad 10000101 \quad 1111010 \quad 1111011$$

## Unsigned Magnitude:-

- only for the numbers
  - 4 bits range of integers  $\Rightarrow$  0 to 15
  - n bits " " "  $\Rightarrow$  0 to  $2^n - 1$
  - Signed

## Signed Magnitude :-



Ques:- A no. is represented in signed mag. representation as 1011.11. Its equivalent in decimal  
Soln:- - (3.75)

Signed Magnitude For Decimal No:

0	0	0	0				
0	0	0	1				
0	1	1	0				
0	1	1	1				
<hr/>				+ 6			
<hr/>				+ 7			
1	0	0	0		- 0		
1	0	0	1		- 1		
1	1	1	0				
1	1	1	0		- 6		
1	1	1	0		- 7		

### Range :-

→ For 4 bit No  $\Rightarrow$  -7 to +7 = ~~-8 to 8~~

→ For n bit  $\Rightarrow$   $-(2^{n-1} - 1)$  to  $(2^{n-1} - 1)$

### Disadvantage :-

- Two zeroes are present
- .

### 1's Compliment :-

→ Both true & -ve no.

→ In this true no. is represented as normal binary with MSB  $\rightarrow 0$

→ To represent -ve no.

(i) Write true no.

(ii) 1's compliment it.

e.g.: -13

+13  $\rightarrow$  0 1 1 0, 1

1 0 0 1 0  $\rightarrow$  1's compliment = -13

### 1's Compliment

0 0 0 0

0 0 0 1

0 0 1 0

0 1 1 1

1 0 0 0

1 0 0 1

1 0 1 0

1 1 1 1

### Decimal

+0

+1

+6

+7

-7

-6

-2

-0

→ Range of n-bit 1's compliment  $\Rightarrow -(2^{n-1}-1)$  to  $(2^{n-1}-1)$

Disadvantage:-

(i) Two zeros are present (+0)

(ii) During addition if any carry is present, it is added to LSB to get correct result. (Same for signed numbers)

Ques:- Perform (5-4) using 1's compliment

Soln:-

$$\begin{array}{r} +5 \Rightarrow 0101 \\ -4 \Rightarrow 1011 \\ \hline \text{Carry} \rightarrow 1 \quad 0000 \\ \downarrow \quad \downarrow \\ \text{EAC} \quad \text{Add in LSB} \quad \hline \\ 0001 \\ \hline \end{array}$$

End around carry.

2's Compliment:-

→ For both the +ve no.

→ The no. are represented as normal binary with MSB 0

→ To represent -ve no.

(i) Write the no.

(ii) 2's compliment if

$$+13 \rightarrow 2's \rightarrow 01101$$

$$-17 \rightarrow +17 \Rightarrow 010001$$

$$-17 \Rightarrow 101111$$

Ques:- A number is represented in 2's compliment as 1011. Then find equivalent decimal.

Soln:-

1011

Take 2's compliment

$$-(0101)$$

-5

Note:-

For -ve number =  $N - 2^n$

e.g:- 1 0 0 1

$$9 - 16 = -7$$

$$\rightarrow 1000 \Rightarrow 8 - 2^4 = -8$$

2's compliment :-

2's compliment

Decimal

0 0 0 0

+0

0 0 0 1

+1

0 1 1 0

+7

0 1 1 1

+7

1 0 0 0

-8

1 0 0 1

-7

1 1 1 0

-2

1 1 1 1

-1

Note:-

Discard carry present in 2's compliment representation

Swing 1's and 2's complements representation to extent no. of bit, copy MSB to required no. of bits

Range of 2's compliment :-

$2^{n-1}$  to  $2^{n-1} - 1$

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Ques:- Perform  $(5 - 4)$  using 2's complement operation

Soln:-  $+5 \Rightarrow 0101$

$-4 \Rightarrow 1100$

$$\begin{array}{r} \textcircled{1} \swarrow \\ \overline{0001} \end{array}$$

Discard

Ques:- Perform  $(5 + 4)$  using 2's complement

Soln:-  $+5 \rightarrow 0101$

$+4 \rightarrow \overline{0100}$

$$\underline{1001} = -7 \rightarrow \text{overflow}$$

Ques:- Perform  $(-5 - 4)$  using 2's complement operation

Soln:-  $-5 \Rightarrow \text{1011} \rightarrow \text{in 2's complement}$

$-4 \Rightarrow \overline{1100}$

$$\begin{array}{r} \textcircled{1} \swarrow \\ \overline{0111} \end{array}$$

Discard

Overflow  $\rightarrow$  May occur in signed arithmetic operations when two same sign no. are added and results exceeds with given no. of bits.

$\rightarrow$  To detect overflow there are two methods

(i) By using sign bits

Let  $X$  and  $Y$  are sign bit of no. and  $Z$  is result sign bit then condition for overflow is

$$XYz + XYZ$$

(ii) By using carry bit

Let  $c_{in}$  (carry into MSB) &  $c_{out}$  (carry from MSB)

$$c_{in} \oplus c_{out} = \begin{cases} 0 & \text{No overflow} \\ 1 & \text{Overflow} \end{cases}$$

$$c_{in} \oplus c_{out} = 0$$

$$c_{in} \oplus c_{out} = 1$$

(Overflow)

## K-Map:-

- deals with 0, 1, X
- When two bits are change then we can't minimize

$\begin{array}{c} 0 \\ \downarrow \\ 1 \end{array}$       
  $\begin{array}{c} 1 \\ \downarrow \\ 0 \end{array}$       Two bits change

- Gray code representation
- It is a graphical method
- In K-Map, Gray code representation is used to minimize logical expression

$$\begin{array}{c} f(A, B) \\ \downarrow \\ \text{MSB} \quad \text{LSB} \end{array}
 \quad
 \begin{array}{c} f(A, B, C) \\ \uparrow \\ \text{MSB} \end{array}
 \quad
 \begin{array}{c} f(A, B, C, D) \end{array}$$

## Two Variable :-

f(A, B)	
A	B
0	00
1	01

A		B	
0	1	0	1
00	01	10	11
10	11	2	3

→ Cell or Square

## Three Variable :-

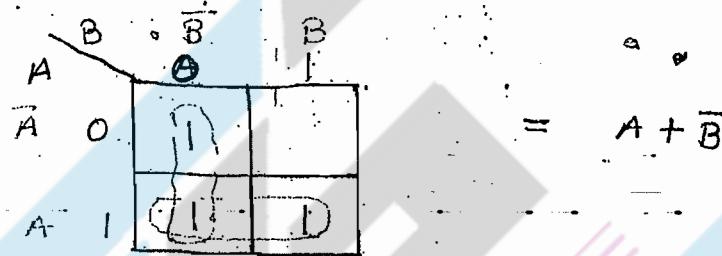
f(A, B, C)			
A		BC	
0	1	00	01
0	1	000	001
1	0	100	101
1	1	111	110

Four Variable :-

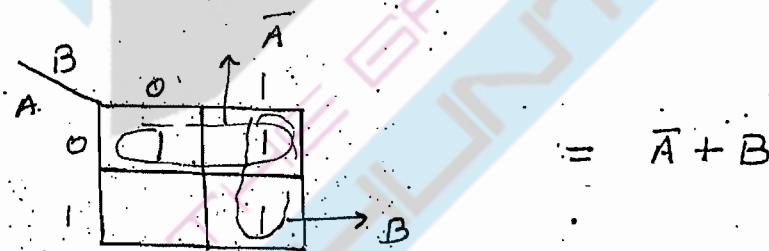
AB\CB	00	01	11	- 10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

SOP :-

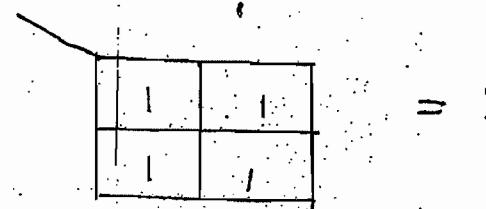
$$f(A, B) = \bar{A}\bar{B} + AB + A\bar{B}$$



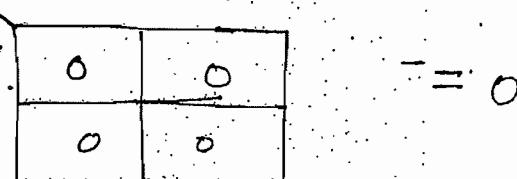
$$f(A, B) = \sum m(0, 1, 3)$$



$$f(A, B) = \sum m(0, 1, 2, 3)$$



Note :-



$$f(A, B) = \sum m(0, 3) + \sum d(1)$$

A	B	$\bar{B}$	B
$\bar{A}$		1	X
A		1	1

$$= \bar{A} + B$$

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$$f(A, B) = \sum m(0, 2) + \sum d(1)$$

A	B	$\bar{B}$	B
$\bar{A}$		1	X
A		1	

$$= \bar{B}$$

$$f(A, B) = \sum m(0, 2) + \sum d(1, 3)$$

A	B	$\bar{B}$	B
$\bar{A}$		1	X
A		1	X

$$= 1$$

Note:-

A	B				
		1	X		
		X	X		

$$= X$$

Three Variables:-

$$f(A, B, C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC + A\bar{B}C$$

		BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$\bar{B}\bar{C}$
		00	01	10	11	10
A	0	1	1	1	1	1
	1	1	1	1	1	

↓      ↓      ↓

$\bar{A}\bar{B}$      $\bar{B}C$      $AC$

$$= \bar{A}\bar{B} + \bar{B}C + AC + \bar{A}\bar{B}C$$

Ques:-  $f(A, B, C) = \sum m(3, 5, 6, 7)$

		$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$
		00	01	11	10	
A	0			1		
	1		1	1	1	1

$$= AC + AB + BC$$

Ques:-  $f(A, B, C) = \sum m(0, 1, 2, 4, 5)$

		$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$
		00	01	11	10	
A	0	1	1	1	1	1
	1	1	1	1	1	1

$$= \bar{B} + \bar{A}\bar{C}$$

Ques:-  $f(A, B, C) = \sum m(1, 3, 6, 7)$

		$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$
		00	01	11	10	
A	0	1	1	1	1	1
	1	1	1	1	1	1

$$= \bar{A}C + AB$$

Hazard ~~free~~

Note:-

free

In Hazard term, redundant term is added

Minimization:-

(1) Octet  $\Rightarrow$  group of 8 cells  $\Rightarrow$  eliminates 3 variables

(2) Quad  $\Rightarrow$  group of 4 cells  $\Rightarrow$  " " 2 "

(3) Pair  $\Rightarrow$  " " 2, " "  $\Rightarrow$  " " 1 "

(4) Single term  $\Rightarrow$  1 cell  $\Rightarrow$  " " 0 "

(5) Remove redundant term

Cause:-  $f(A, B, C) = \sum m(1, 2, 3, 7)$  Identify I, PI, EPI

		$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$
		00	01	11	10
A	0	1	1	1	1
	1	1	1	1	1

$$I = 4$$

$$PI = 3 (\bar{A}B, \bar{A}C, BC)$$

$$EPI = 3$$

$$= \bar{A}C + BC + \bar{A}B$$

Implicant :-

→ Each minterm in the given expression is known as implicant.

Prime Implicant :-

→ It is a product term obtained by combining max. possible cells.

Essential Prime Implicant (EPI) :-

→ It is the prime implicant which is possible to combine only in one way & there is no alternate (It is the term required compulsorily in our Ans)

Ques:-  $f(A, B, C) = \sum m(0, 1, 2, 4)$  Minimize & identify I, PI & EPI

Soln:-

A	BC	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$	
$\bar{A}$	1	1	1	1	1	
A	1					

$$= \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}C$$

$$I = 4, PI = 3, EPI = 3$$

Ques:-

$$f(A, B, C) = \sum m(1, 3, 4, 7)$$

Soln:-

A	BC	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$	
$\bar{A}$		1	1	1	1	
A			1	1	1	

$$= \bar{A}C + AB$$

$$I = 4, PI = 3 (\bar{A}C, AB, BC), EPI = 2$$

Ques:-  $f(A, B, C) = \sum m(0, 1, 5, 6, 7)$

Soln:-

A	BC	$\bar{B}\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$	
$\bar{A}$	1	1	1	1	1	
A		1	1	1	1	

$$\begin{aligned} I &= 5 \\ PI &= 4 \\ EPI &= 2 \end{aligned}$$

$$= \bar{A}\bar{B} + AC + A\bar{B}$$

ques:-  $f(A, B, C) = \sum m(0, 1, 2, 5, 6, 7)$

		$\bar{B}C$	$\bar{B}C$	$BC$	$B\bar{C}$
		A	1	1	1
		A	1	0	1

Another way.

Soln:-

$$I = 6, PI = 6, EPI = 0$$

$$\rightarrow \bar{A}\bar{B} + AC + B\bar{C}$$

$$\rightarrow \bar{B}C + AB + A\bar{C}$$

Both are correct

ques:-  $f(A, B, C) = \sum m(0, 1, 3, 4, 5)$

Soln:-

		$\bar{B}C$	$\bar{B}C$	$BC$	$B\bar{C}$
		A	1	1	1
		A	1	1	1

$$= \bar{B} + \bar{A}C$$

$$I = 5, PI = 2, EPI = 2$$

ques:-  $f(A, B, C) = \sum m(0, 1, 2, 3, 5, 7)$

Soln:-

		$\bar{B}C$	$\bar{B}C$	$BC$	$B\bar{C}$
		A	1	1	1
		A	0	1	1

$$= \bar{A} + C$$

$$I = 6, PI = 2, EPI = 2$$

ques:-  $f(A, B, C) = \sum m(0, 1, 6, 7) + \sum d(2, 3)$

Soln:-

		$\bar{B}C$	$\bar{B}C$	$BC$	$B\bar{C}$
		A	1	1	X
		A			1

$$= \bar{A} + B$$

ques:-  $f(A, B, C) = \sum m(0, 1, 6, 7) + \sum d(3, 5)$

Soln:-

		$\bar{B}C$	$\bar{B}C$	$BC$	$B\bar{C}$
		A	1	1	X
		A		X	1

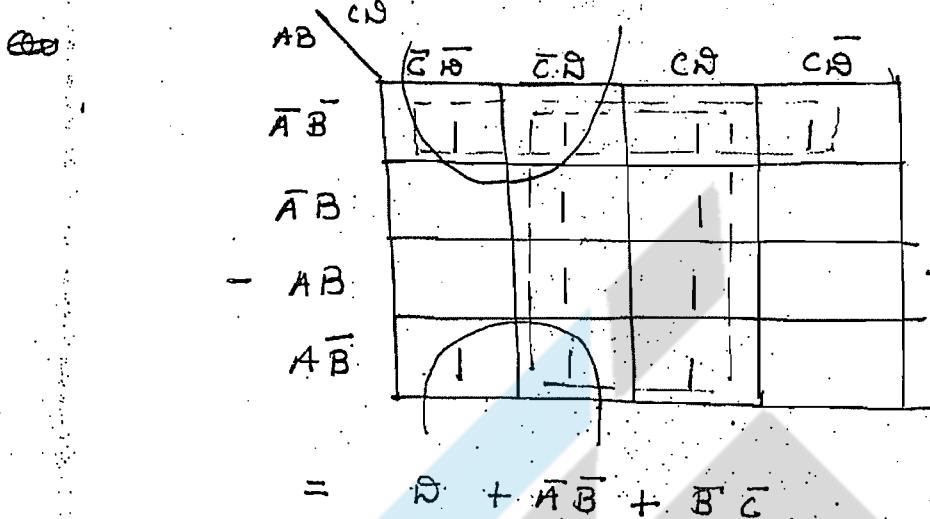
$$= \bar{A}\bar{B} + AB$$

Note:-

$\bar{A}$	1	1	X	
A	X	X	1	1

Four Variables:-

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 13, 15)$$



$$PI = 3$$

$$EPI = 3$$

Ans:-

~~WX~~  $YZ$

	00	01	11	10
00				
01	1	1		
11		1	1	1
10		1		

$$PI = ?$$

$$EPI = ?$$

Soln:-  $PI = 5$ ,  $EPI = 4$

Note:-

$$\frac{AB}{2} + \frac{CD}{2} \rightarrow \text{No. of variable} = 2 = \text{literal count.}$$

$$\text{fanin} = \text{No. of i/p}$$

$$\text{literal count} = 2+2 = 4$$

P/Os:-

5 Variable :-

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f.(A, B, C, D, E)

	A	B	C	D	E
0	0	0	0	0	0
1	6	0	0	0	1
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
31	1	1	1	1	1

$A = 0$

$A = 1$

BC AE

AE BC

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

16	17	19	18
20	21	23	22
28	29	31	30
24	25	27	26

- If pair/quadruplet is present in both then  $A \otimes A$  gets cancelled then result is acc. to only Map
- If pair/quadruplet is present in only one Map then it is multi. result is multiply either by  $A$  or  $\bar{A}$  acc. to condition/presence

Pos:-

$$f(A, B) = \Pi M (0, 1, 3)$$

A	B	$\bar{B}$
$\bar{A}$	10	01
A	0	0

$$= (A)(\bar{B})$$

$$f(A, B) = \Pi M (0, 2, 3)$$

A	B	$\bar{B}$
$\bar{A}$	10	
A	0	0

$$= (\bar{A}) \cdot (B)$$

$$f(A, B) = \Pi M (0, 4, 3) + \Pi d (1)$$

A	B
$\bar{A}$	0 X
A	0

$$= A \cdot \bar{B}$$

$$f(A, B, C) = \Pi M (0, 1, 2, 5, 6)$$

A	$\bar{B}C$	$B+C$	$B+\bar{C}$	$\bar{B}+\bar{C}$	$\bar{B}+C$
$\bar{A}$	0	0	0	0	0
A	0	0	0	0	0
$\bar{B}$	0	0	0	0	0

$$B+\bar{C}$$

$$\bar{B}+C$$

$$\rightarrow (\bar{B}+C)(B+\bar{C})(A+B)$$

$$\rightarrow (\bar{B}+C)(\bar{B}+C)(A+C)$$

$$\rightarrow B \cdot (A+C)$$

A	$\bar{B}C$	$B+C$	$B+\bar{C}$	$\bar{B}+\bar{C}$	$\bar{B}+C$
$\bar{A}$	10	01	0	0	0
A	0	0	0	0	0
$\bar{B}$	1	0	0	0	0

Ques:- Minimize POS

	$B+C$	$B+\bar{C}$	$\bar{B}+C$	$\bar{B}+\bar{C}$
$A$	0	X	1	0
$\bar{A}$	X	0	1	0

Ans:- 1 → removed then  $Ans = B \cdot C$

Ques:-  $f(A, B, C, \bar{A})$  ~~POS~~ =  $\prod M(0, 1, 4, 5, 8, 9, 13, 15)$

Soln:-

$AB$	$C\bar{A}$	$C+B$	$C+\bar{B}$	$\bar{C}+\bar{A}$	$\bar{C}+B$
$A+B$	1 0	— 0	— —	— —	— —
$A+\bar{B}$	1 0	— —	0 —	— —	— —
$\bar{A}+B$	— —	— 0	— —	0 —	— —
$\bar{A}+\bar{B}$	— —	— —	— —	— —	— —
	0	0	— —	— —	— —

$$= (\bar{A} + \bar{B} + \bar{B}) (B + C) (A + C)$$

↓  
literal count = 3 + 2 + 2 = 7

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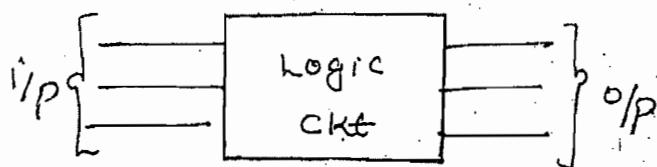
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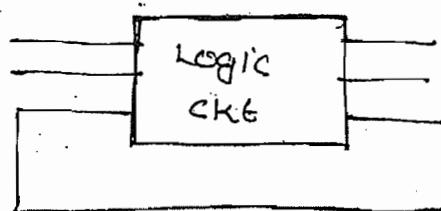
## Digital Circuits

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### Combinational



### Sequential Circuit



→ Present o/p depends on only present i/p's

→ No feedback

→ No Memory

→ eg:- HA, FA, MUX, DEMUX

→ Present o/p depends

Present i/p Previous/  
feedback Past o/p's

Memory

eg:- FF, Registers, counters

### Combinational Circuit :-



### Procedure for Design :-

- Identify no. of i/p's and o/p's
- Construct truth table
- Write logical expression in SOP or POS
- Minimize logical expression
- Implement logic ckt

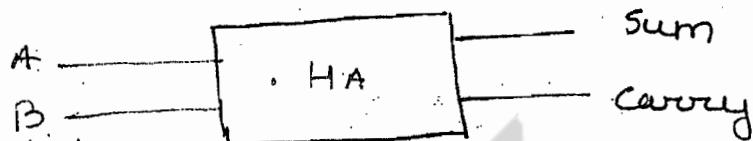
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## Arithmetic Circuits :-

### (i) Half Adder :-

0	0	1	1
<u>0</u>	<u>1</u>	<u>0</u>	<u>1</u>
0 0	0 1	0 1	1 0

↓  
 sum  
 carry



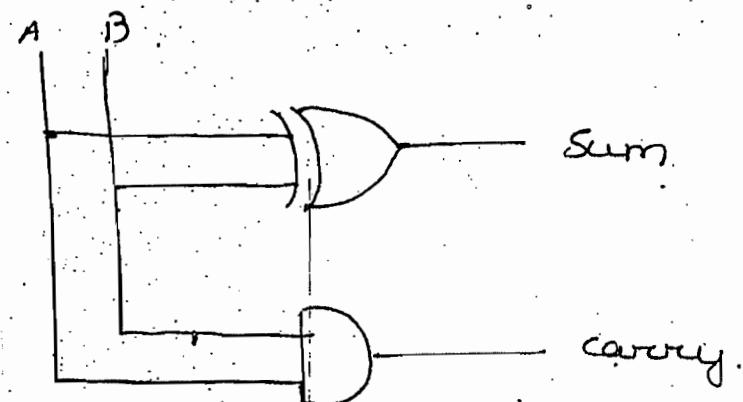
### Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

### Logical Expression :-

$$\text{sum} \Rightarrow \overline{A}B + A\overline{B} = A \oplus B$$

$$\text{carry} \Rightarrow AB$$



## HA Questions! -

→ Logical expression for sum  $\rightarrow A \oplus B$

Carry  $\rightarrow AB$

→ Min. no. of NAND

$\rightarrow 5$

→ " " " NOR

$\rightarrow 5$

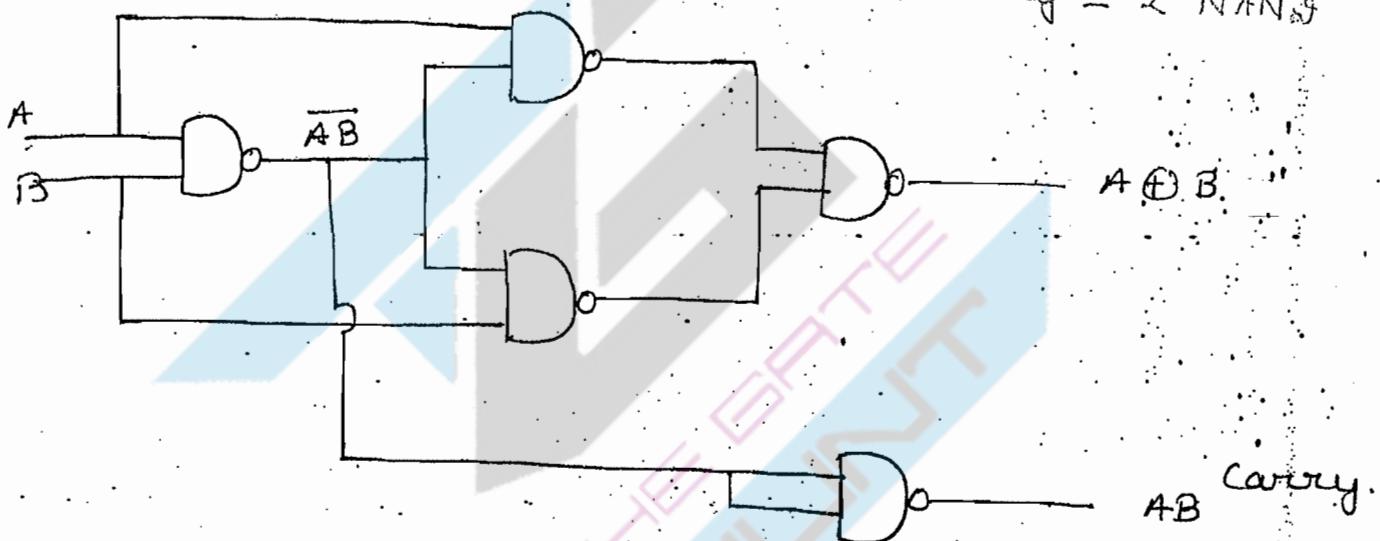
→ " " " MUX

→ " " " Decoder

## HA using NAND Gate! -

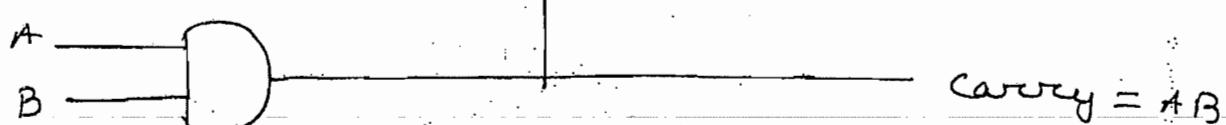
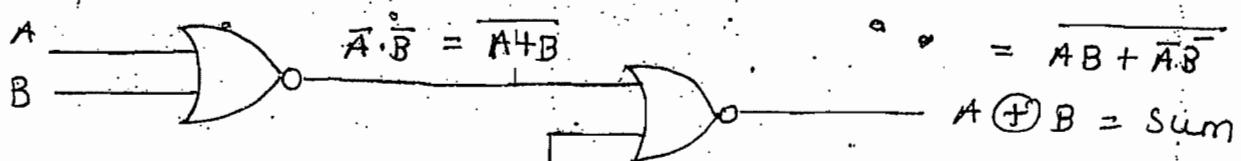
Sum = 4 NAND

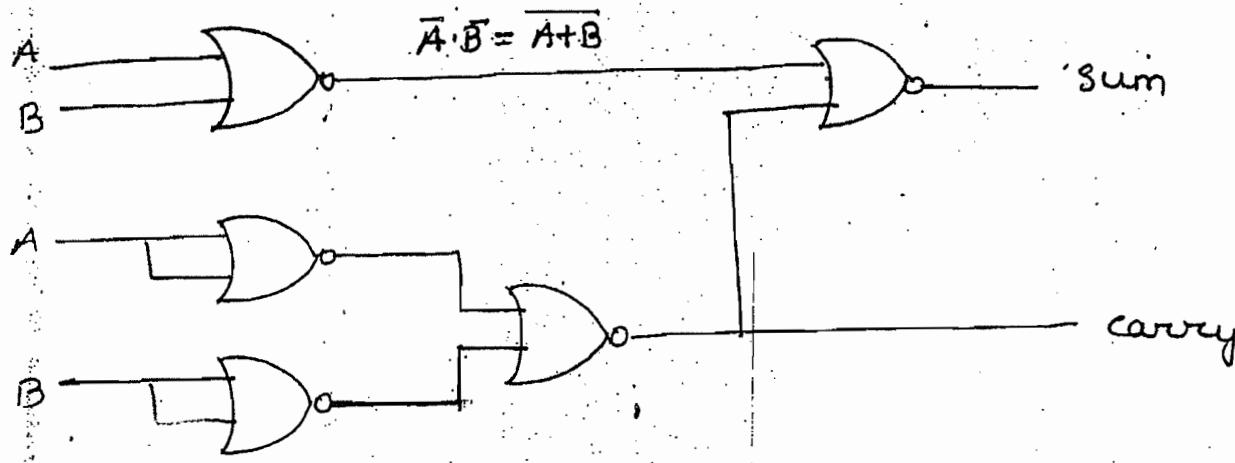
Carry = 2 NAND



## HA using NOR Gate! -

$$A \oplus B = \overline{A \odot B} = \overline{\overbrace{AB + \overline{A}\overline{B}}^3} \quad ①$$





Half subtractor :-

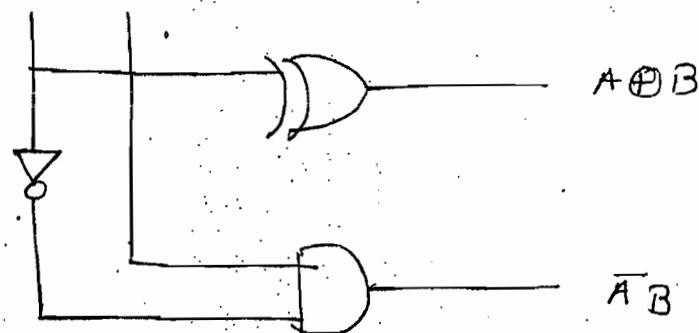


Truth Table :-

A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic CKT :-

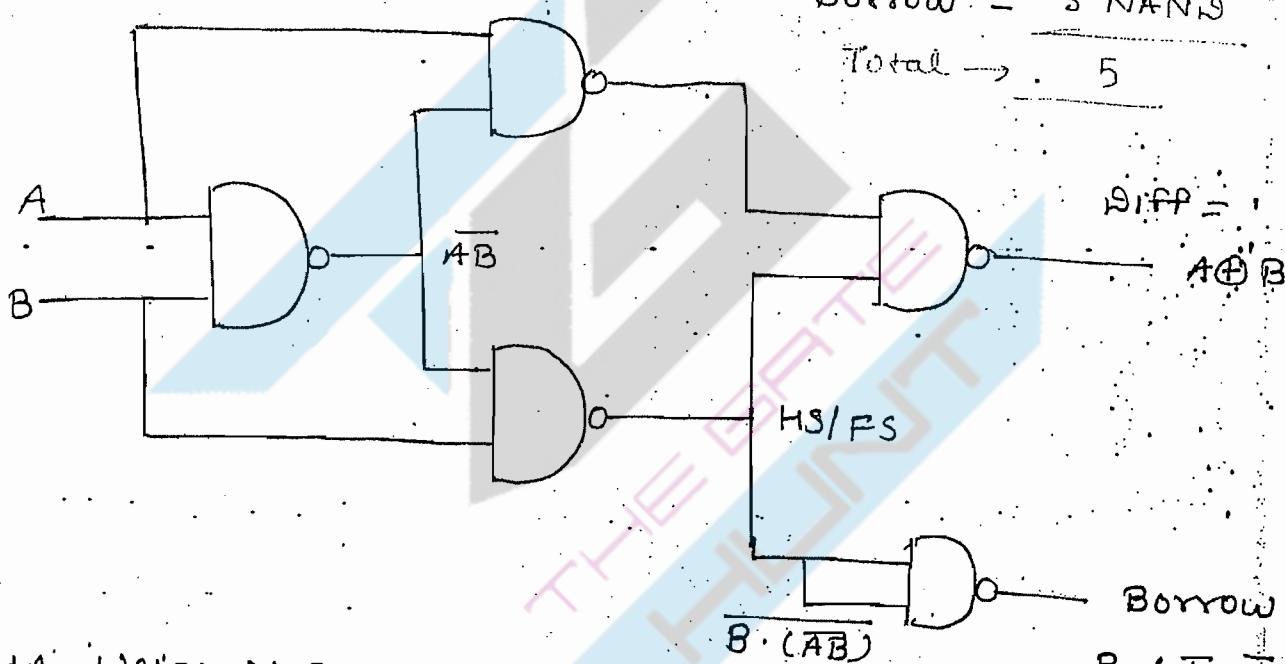
$$\text{Diff.} \Rightarrow A \oplus B \quad \text{Borrow} \Rightarrow \bar{A}B$$



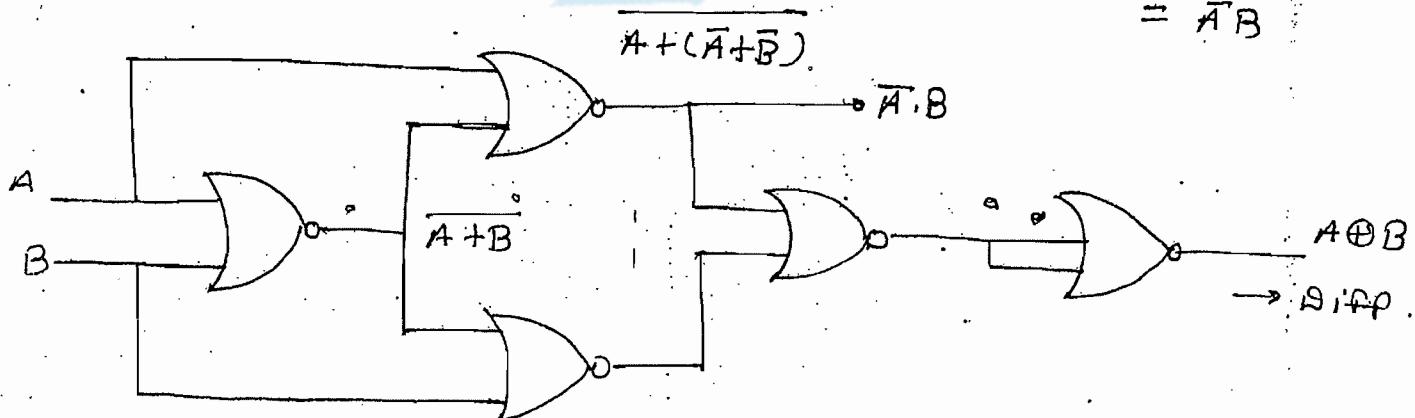
Question of HS :-

- $\rightarrow$  Logical exp. for Diff.  $\rightarrow A \oplus B$
- $\rightarrow$  Logical exp. for Borrow  $\rightarrow \bar{A}B$
- $\rightarrow$  Min. no. of NANDS  $\rightarrow 5$
- $\rightarrow$  Min. no. of NOR  $\rightarrow 5$
- $\rightarrow$
- $\rightarrow$

HA Using NANDs :-

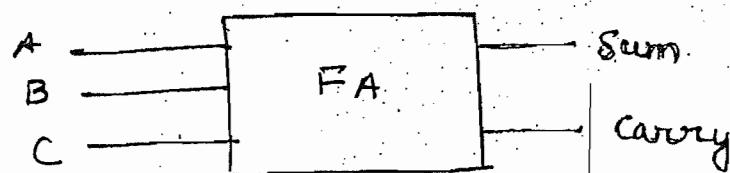


HA Using NORs :-



Full Adder :-

→ Add 3 bits.

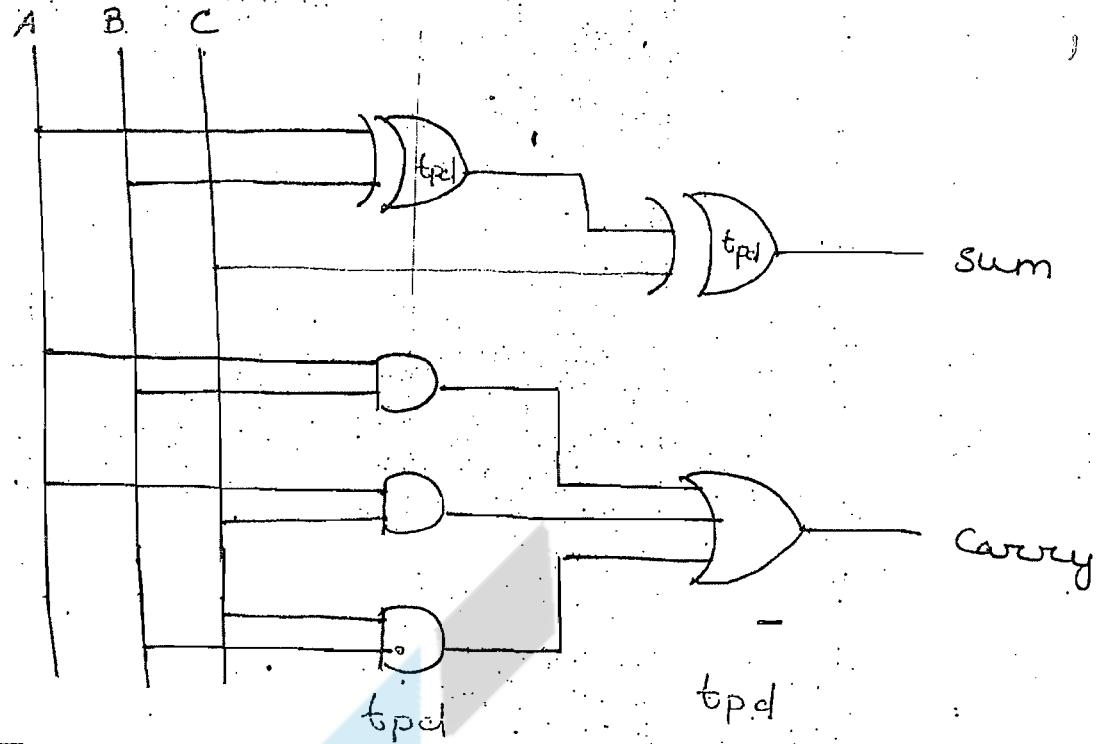


A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logical Expression :-

$$\begin{aligned}
 \text{Sum} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\
 &= A \oplus B \oplus C \\
 &= \Sigma m(1, 2, 4, 7)
 \end{aligned}$$

$$\begin{aligned}
 \text{Carry} &= \Sigma m(3, 5, 6, 7) \quad \text{--- (1)} \\
 &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC
 \end{aligned}$$

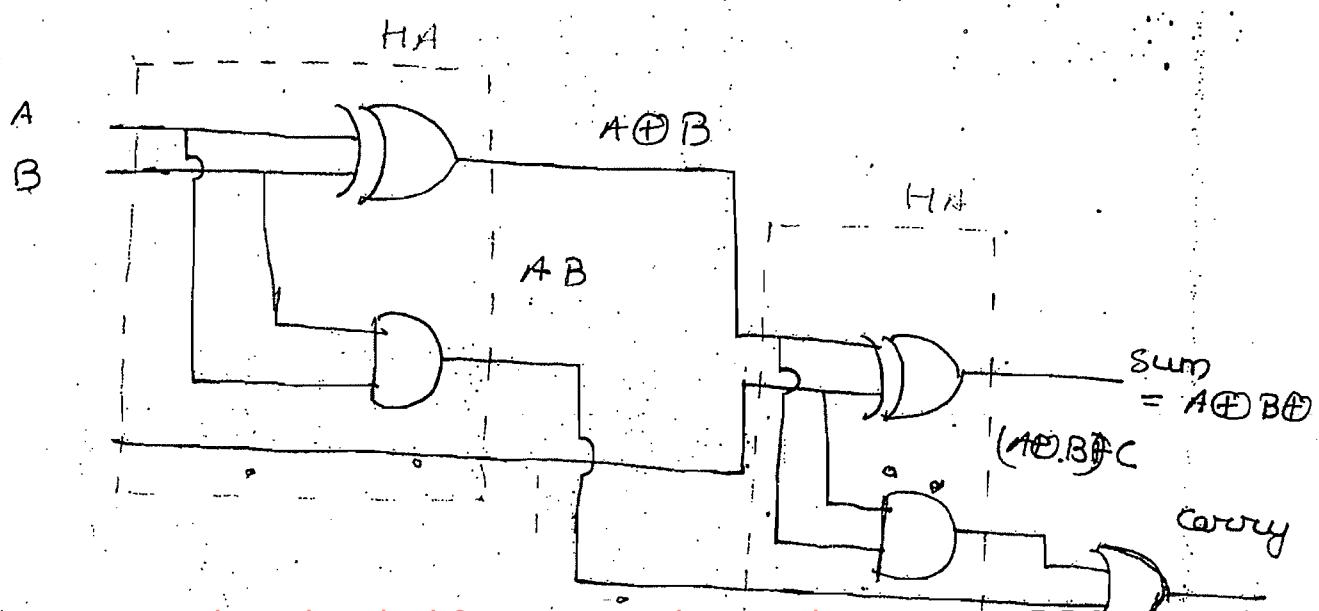


Note:-

→ In FA if all logic gate have same propagation delay  $t_{pd}$ . then to provide sum or carry o/p minimum two  $t_{pd}$  delay is required

Alternate carry expression:-

$$\begin{aligned}
 \text{Carry} &= \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC \\
 &= AB(C + \overline{C}) + (\overline{A}B + A\overline{B})C \\
 \text{Carry} &= AB + (A \oplus B)C \quad - \text{--- (3.)}
 \end{aligned}$$



$$FA = 2HA + 1OR$$

→ Sum  $\rightarrow A \oplus B \oplus C$   
 $\rightarrow \Sigma m(1, 3, 4, 7)$

→ Carry  $\rightarrow \Sigma m(3, 5, 6, 7)$   
 $\rightarrow AB + BC + AC$   
 $\rightarrow AB + (A \oplus B)C$

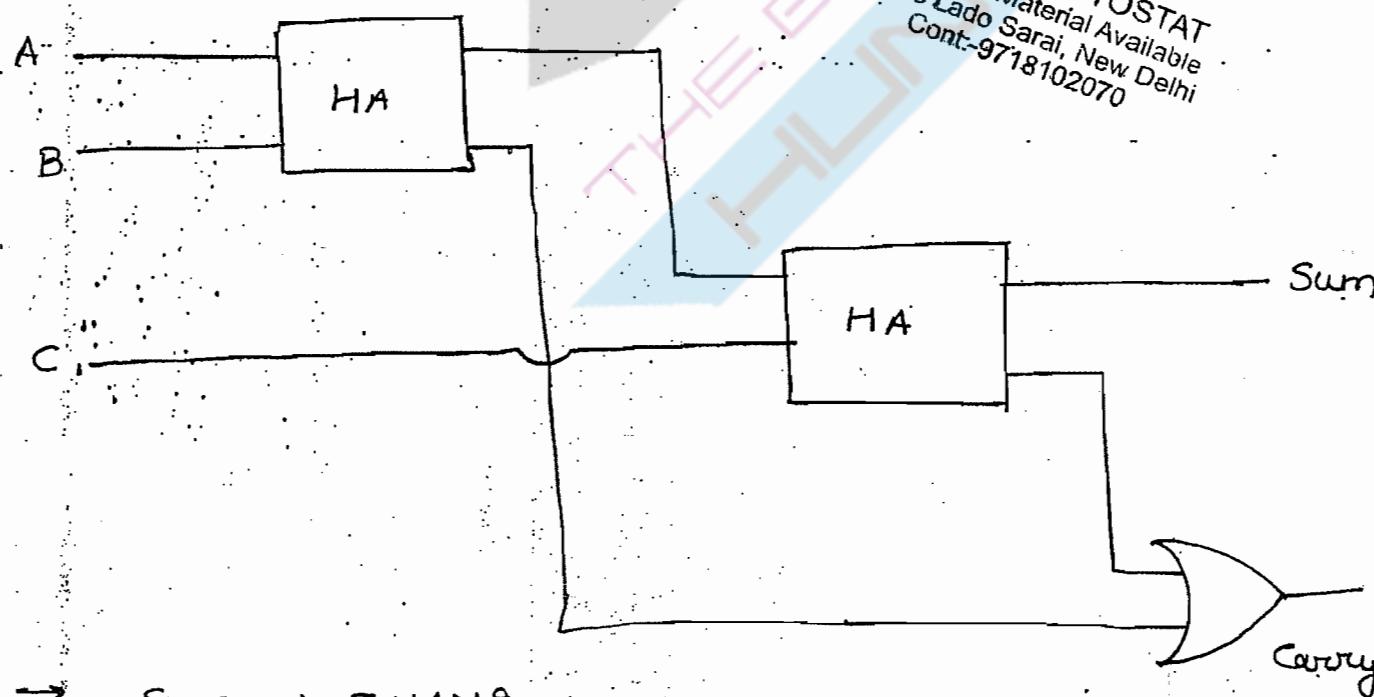
→ No. of HA and OR  $\Rightarrow 2HA + 1OR$

→ Min. no. of NANDS  $\Rightarrow 9$

→ " " " NOR  $\Rightarrow 9$

→ No. of MUX  $\Rightarrow -$

→ No. of Decoder  $\Rightarrow -$

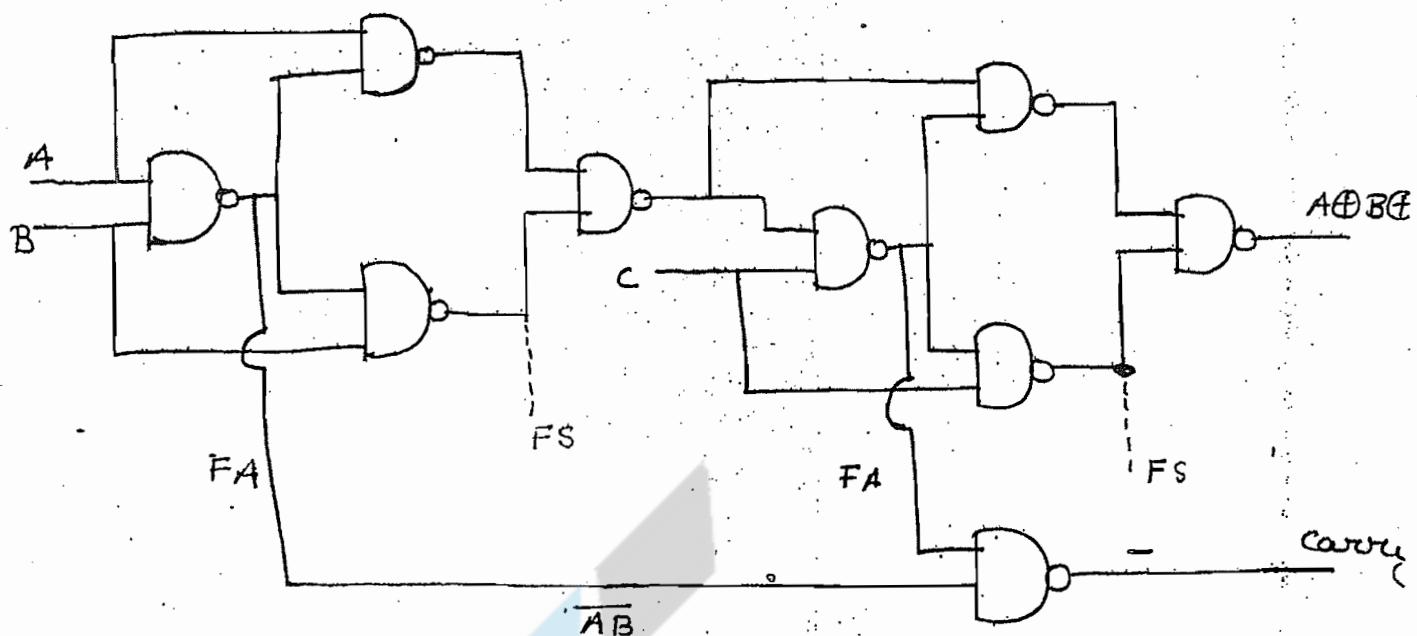


→ Sum  $\Rightarrow 8$  NANDS

→ Carry  $\Rightarrow 6$  NANDS

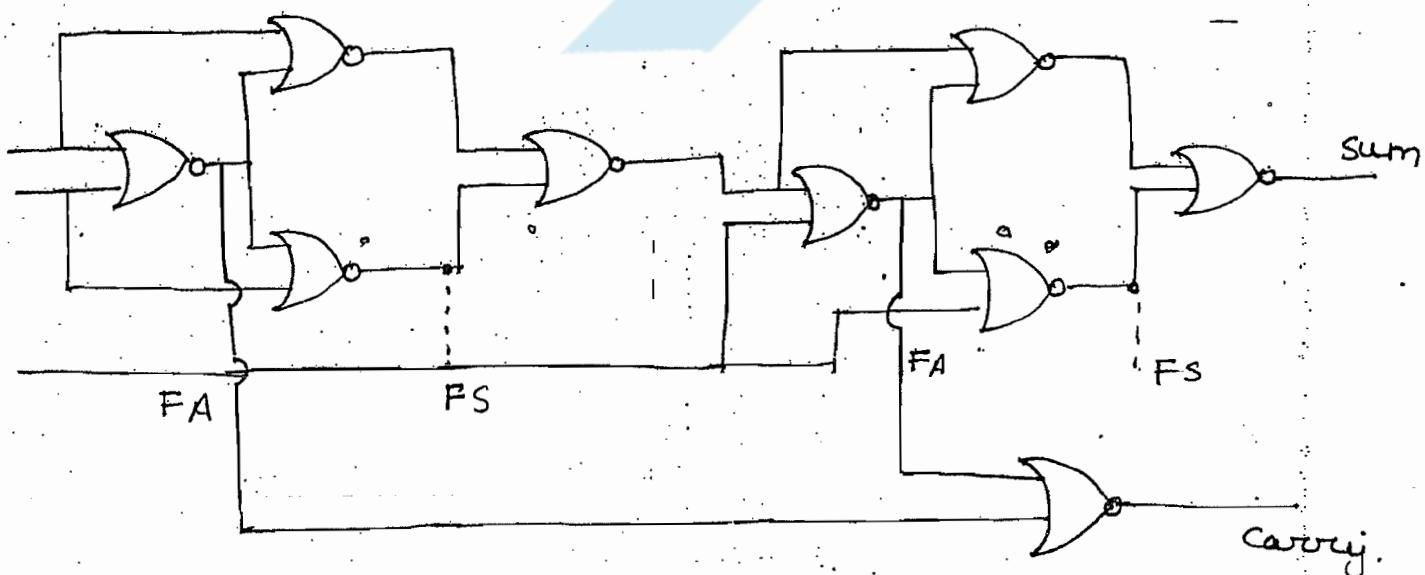
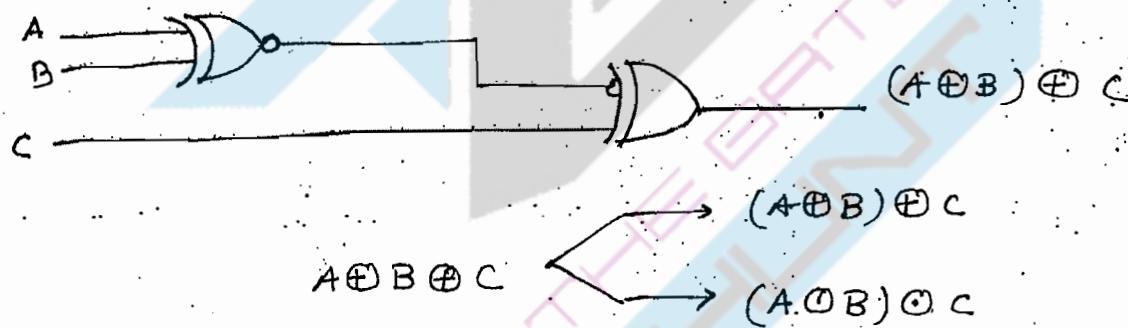
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• FA using NANDs :-

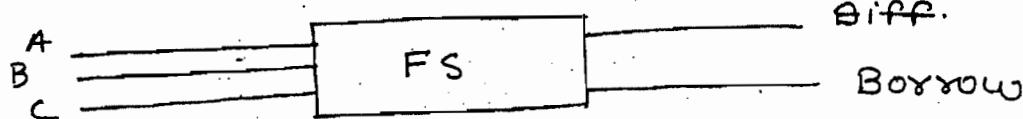


$$= \overline{AB} \overline{(A \oplus B)C} = AB + (A \oplus B)C$$

• FA Using NOR :-



## Full subtractor:-



Truth Table :-

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$\text{Difference} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \dots$$

$$= A \oplus B \oplus C = \Sigma m(1, 2, 4, 7)$$

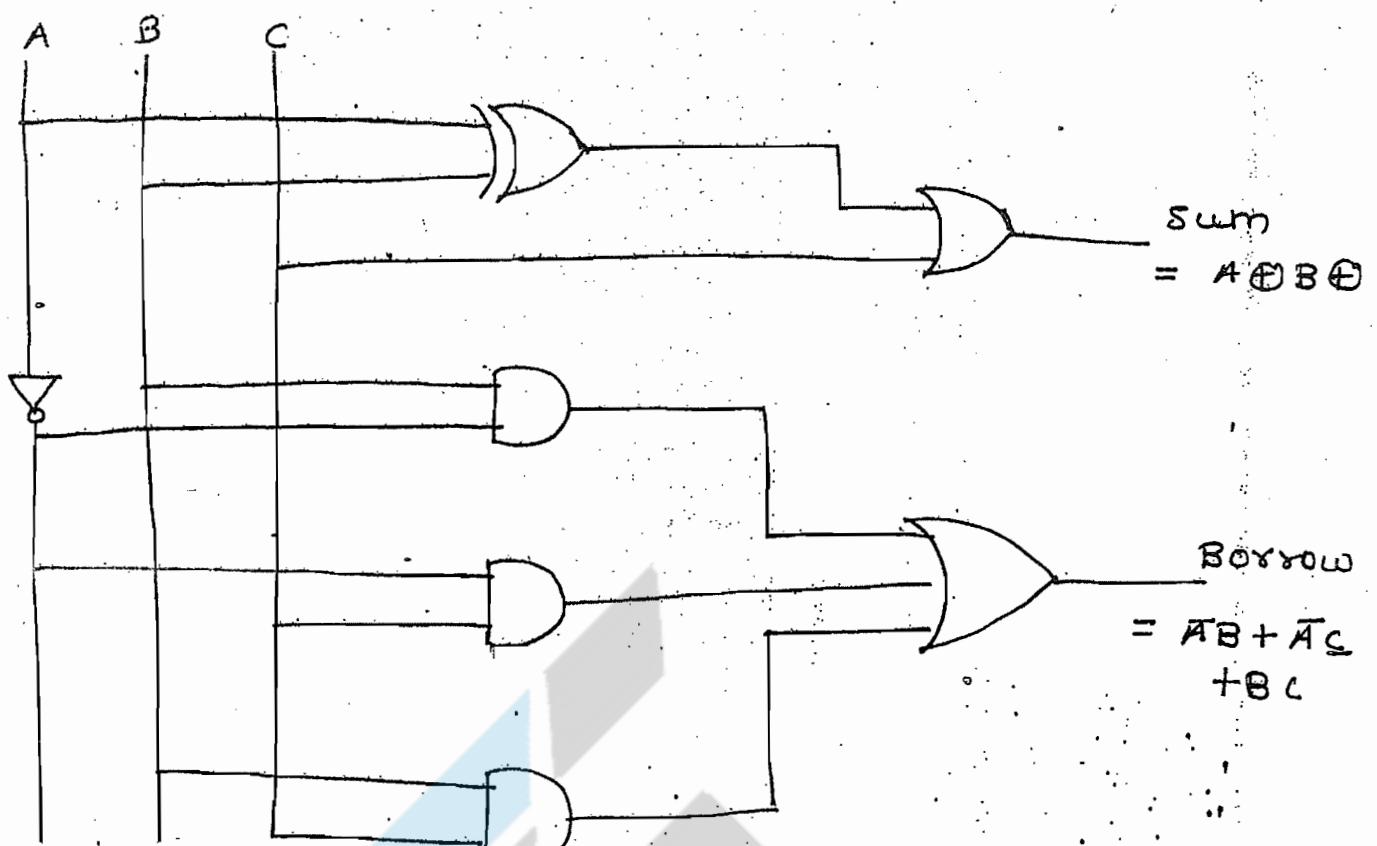
$$\text{Carry} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC = \Sigma m(1, 2, 3, 7)$$

$$= \bar{A}C + \bar{A}B + BC - 01$$

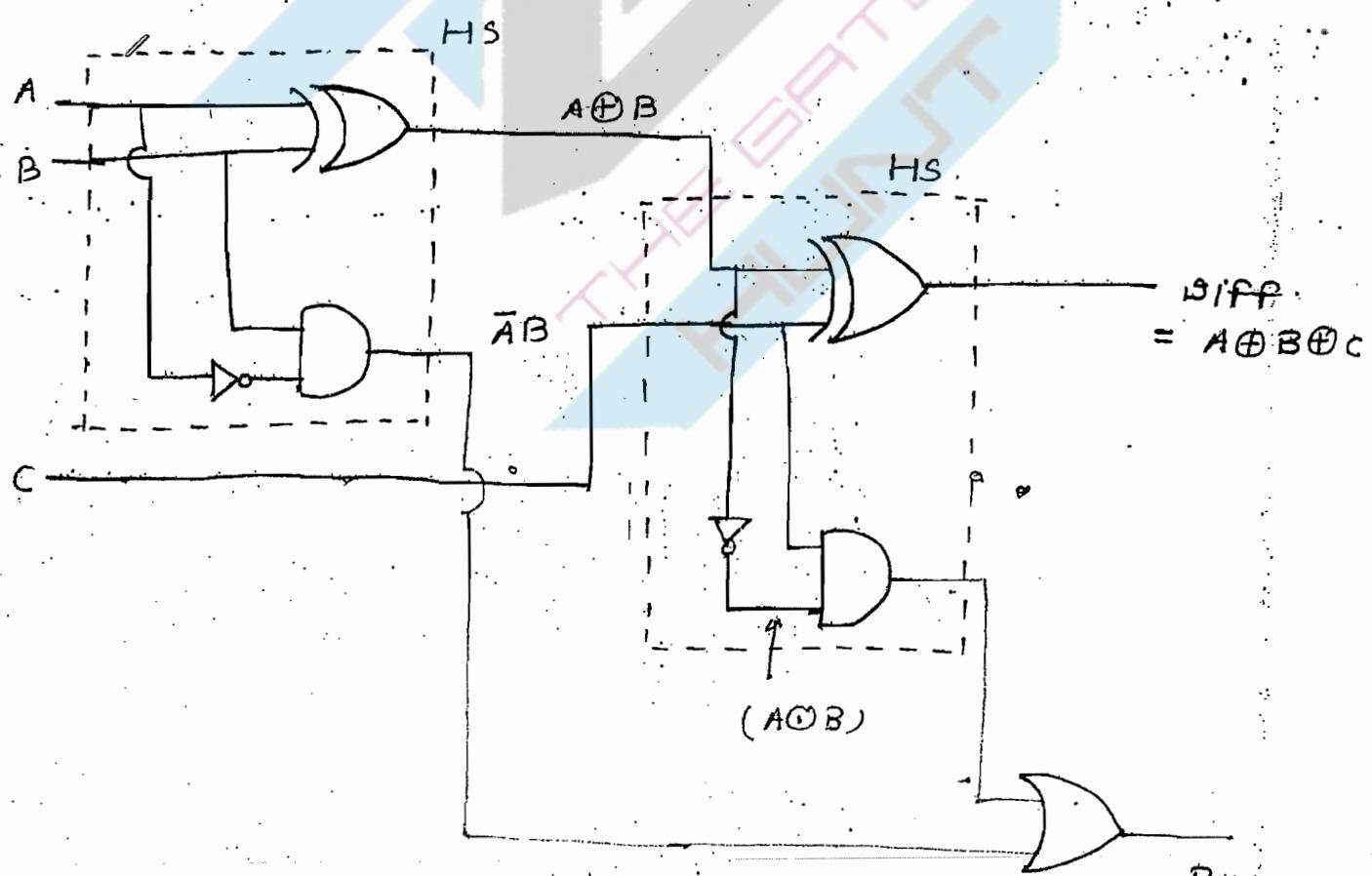
OR

$$= (\bar{A}\bar{B} + AB)C + \bar{A}B(C\bar{C} + C)$$

$$= (A \oplus B)C + \bar{A}B$$



OR



Question :-

- Logical expression for difference  $\rightarrow \Sigma m(1,2,4,7)$   
 $A \oplus B \oplus C$
- Logical expression for Borrow  $\rightarrow \Sigma m(1,2,3,7)$   
 $\bar{A}B + BC + \bar{A}C$   
 $\bar{A}B + (A \oplus B)C$

→ Min. no. of NANDS  $\Rightarrow 9$

→ " " " NOR  $\Rightarrow 9$

→ No. of HS & OR  $\Rightarrow 2HS + 1OR$

Comparator:-



Truth Table:-

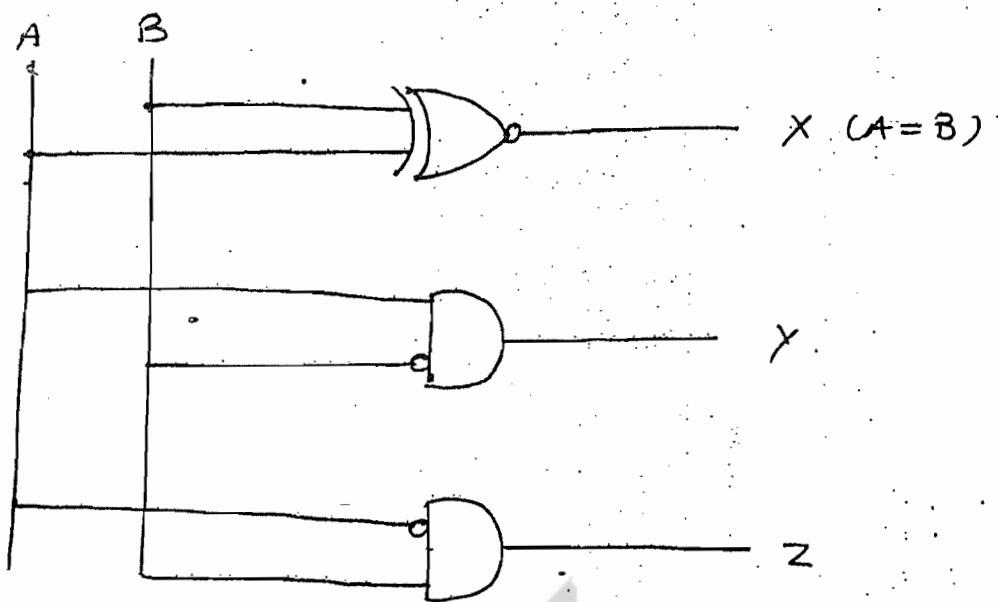
A	B	$A = B$ (X)	$A > B$ (Y)	$A < B$ (Z)
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

Logical Expressions:-

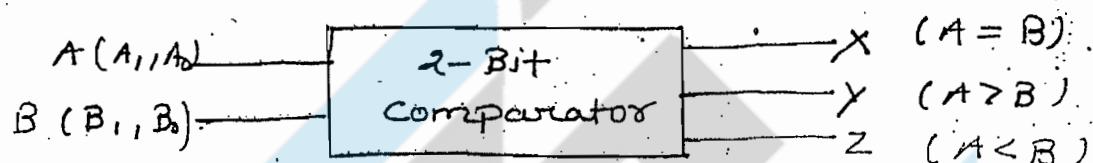
$$X = \bar{A}\bar{B} + AB = A \oplus B$$

$$Y = A\bar{B}$$

$$Z = \bar{A}B$$



2-Bit Comparator:-



A		B		A=B	A>B	A<B
A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>	X	Y	Z
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0			
0	1	1	1			

$$\rightarrow A = B = (A_1 = B_1) \cdot (A_0 = B_0)$$

$$= (A_1 \oplus B_1) \cdot (A_0 \oplus B_0)$$

$$\rightarrow A > B = (A_1 > B_1) \text{ or } (A_1 = B_1) \cdot (A_0 > B_0)$$

$$= (A_1 \cdot \overline{B}_1) + (A_1 \oplus B_1) \cdot A_0 \overline{B}_0$$

$$\rightarrow A < B = \overline{A}_1 \cdot B_1 + (A_1 \oplus B_1) \cdot \overline{A}_0 \cdot B_0$$

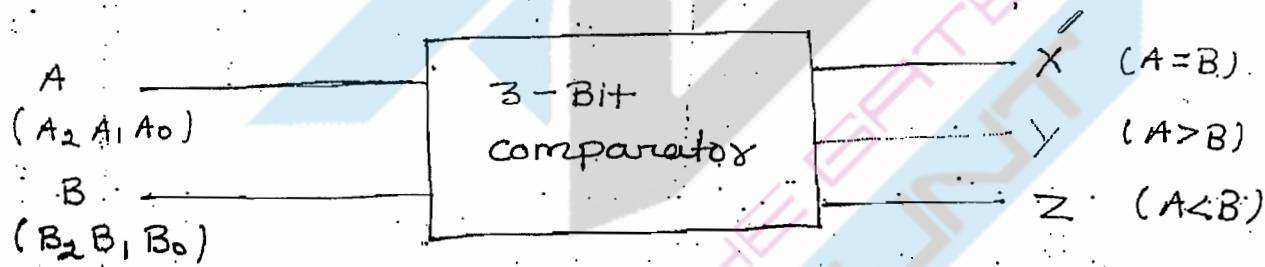
Note :-

→ In n-bit comparator total no. of combination

→ In n-bit comparator, no. of equal condition =  $2^n$

→ In n-bit comparator, no. of greater/lesser condition present =  ~~$2^n - 2^n$~~   $\frac{2^n - 2^n}{2}$

3-Bit Comparator :-



$$\rightarrow X = (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0)$$

$$\rightarrow Y = A_2 \overline{B}_2 + (A_2 \oplus B_2) A_1 \overline{B}_1 + (A_2 \oplus B_2) (A_1 \oplus B_1) A_0 \overline{B}_0$$

$$\rightarrow Z = \overline{A}_2 \cdot B_2 + (A_2 \oplus B_2) \cdot \overline{A}_1 B_1 + (A_2 \oplus B_2) (A_1 \oplus B_1) \cdot \overline{A}_0 B_0$$

Note :-

$$\rightarrow X_i = A_i \oplus B_i \quad | \quad X_0 = A_0 \oplus B_0$$

$$X_1 = A_1 \oplus B_1$$

$$X_2 = A_2 \oplus B_2$$

$$\rightarrow \text{For } A = B, \quad X = X_2 \cdot X_1 \cdot X_0$$

$$\rightarrow \text{For } A > B, \quad Y = A_2 \overline{B}_2 + X_2 \cdot A_1 \overline{B}_1 + X_2 X_1 A_0 \overline{B}_0$$

$$\rightarrow \text{For } A < B, \quad Z = \overline{A}_2 B_2 + X_2 \cdot \overline{A}_1 B_1 + X_2 X_1 \overline{A}_0 B_0$$

Note:-

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

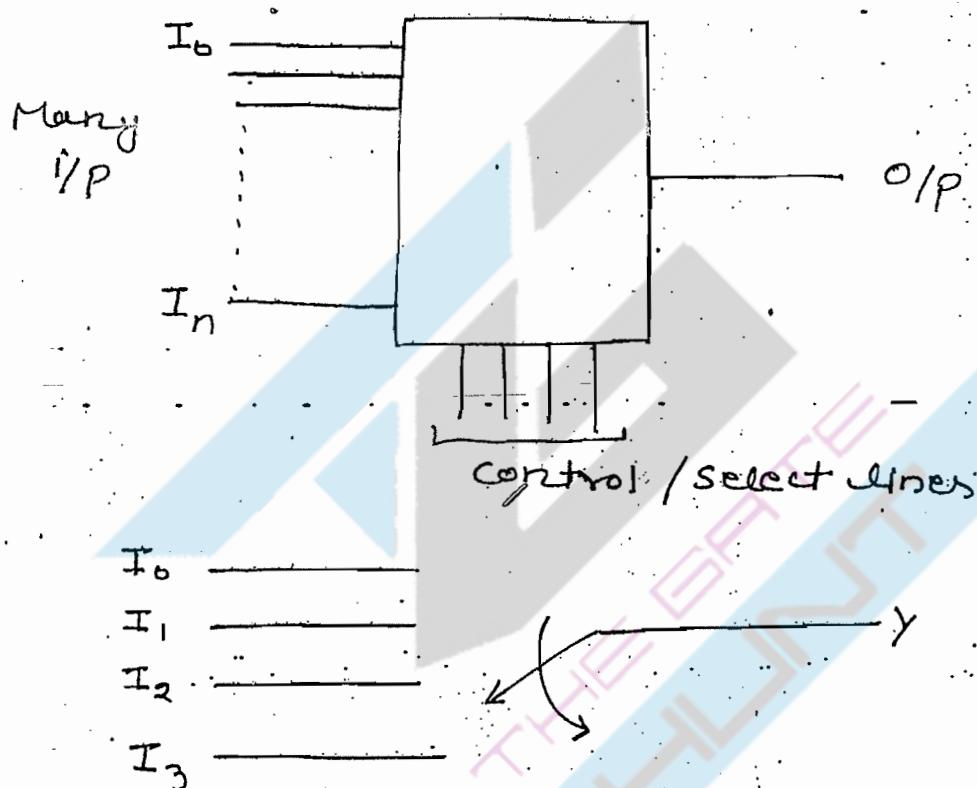
SOP Expression:-

$$Y = \bar{A}\bar{B} \cdot 1 + \bar{A}B \cdot 0 + A\bar{B} \cdot 1 + AB \cdot 0$$

POS Expression:-

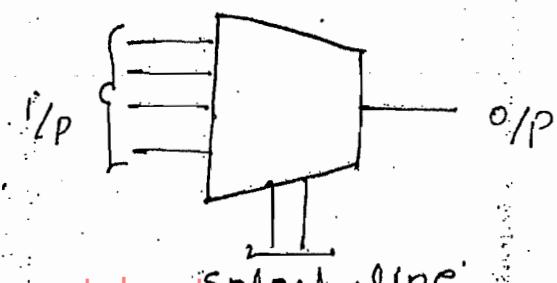
$$Y = (A+B+1)(A+\bar{B}+0)(\bar{A}+B+1)(\bar{A}+\bar{B}+0)$$

Multiplexer:-

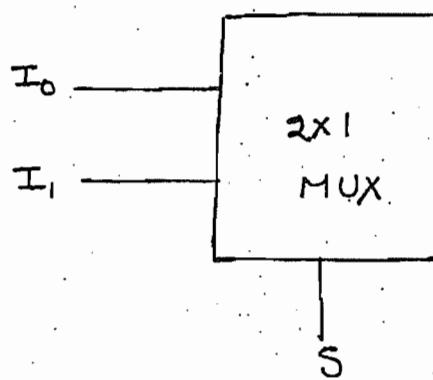


- It is a combinational circuit which have many data i/p's and single o/p
- Depending on select, one of the data is transferred to the o/p
- Hence MUX is known as Many to one circuit
- Data selector
- Universal logic circuit
- Parallel to serial data converter

Symbol:-

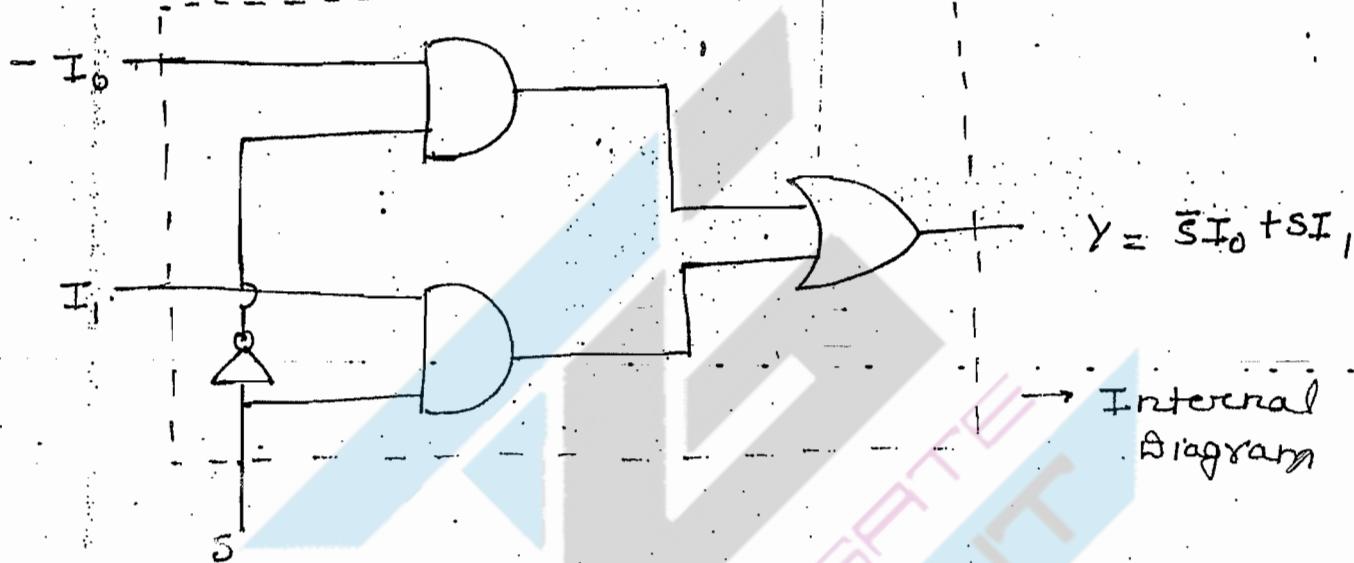


## 2:1 MUX:-



$$Y = \bar{S}_0 I_0 + S I_1$$

S	Y
0	$I_0$
1	$I_1$



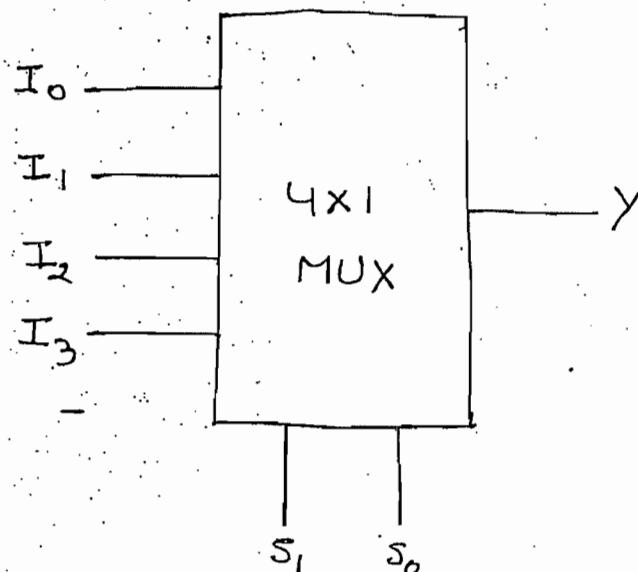
$$Y = \bar{S} I_0 + S I_1$$

→ Internal Diagram

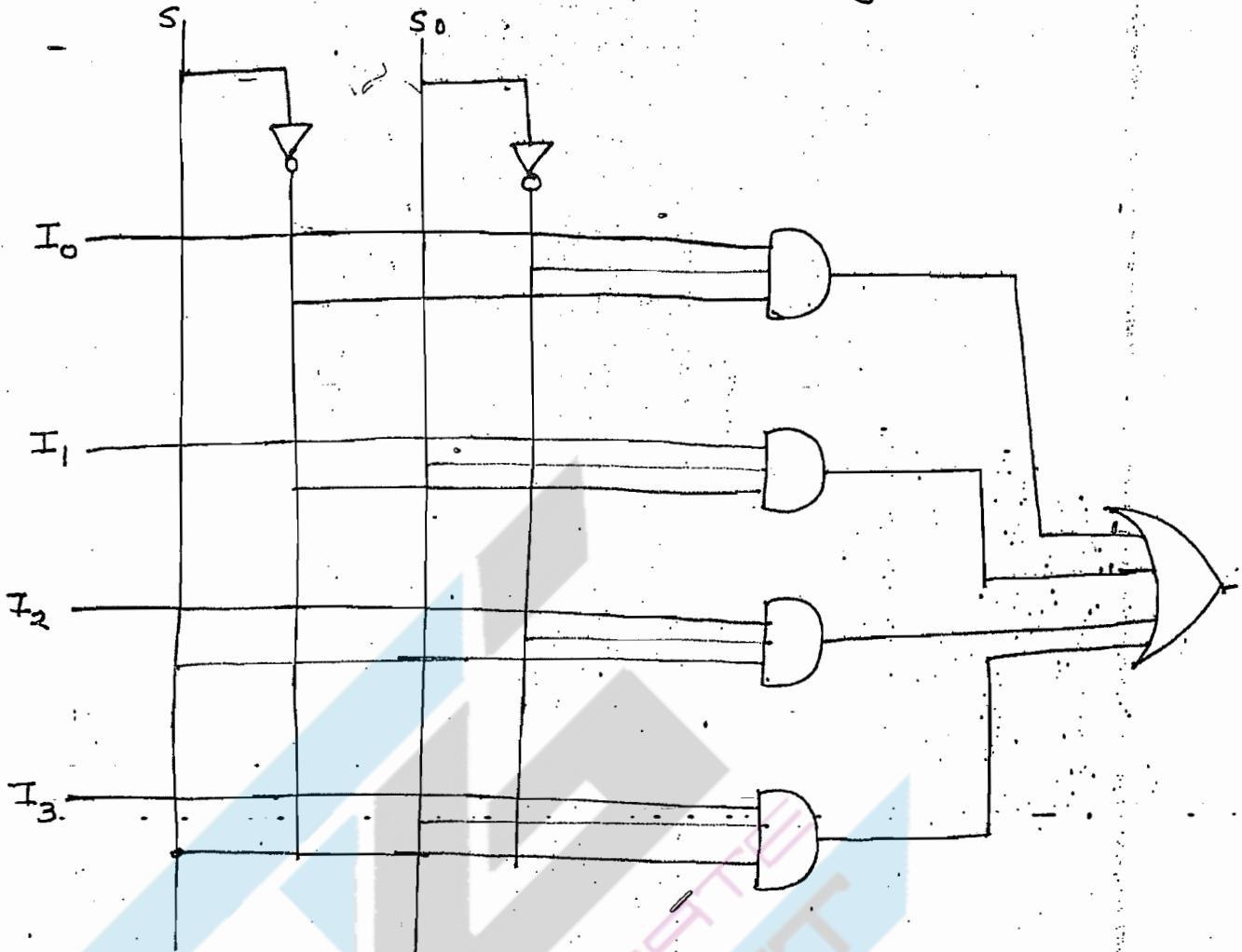
→ Two level AND-OR because data is not going through NOT gate.

## 4:1 MUX:-

$S_1$	$S_0$	Y
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$



$$Y = \bar{s}_1 \bar{s}_0 I_0 + \bar{s}_1 s_0 I_1 + s_1 \bar{s}_0 I_2 + s_1 s_0 I_3$$



For 8:1 MUX :-

$$Y = \bar{s}_2 \bar{s}_1 \bar{s}_0 I_0 + \bar{s}_2 \bar{s}_1 s_0 I_1 + \dots + s_2 s_1 s_0 I_7$$

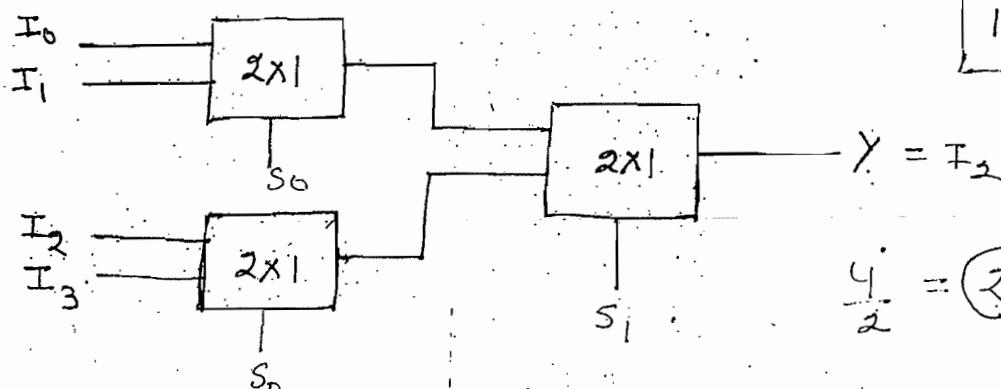
Types of questions in MUX :-

(1) Implementation of Higher order MUX using Lower order MUX :-

$$(a) \quad 4 \times 1 \xrightarrow{s_1 \quad s_0} 2 \times 1 \text{ MUX}$$

Operation:-

$s_1$	$s_0$	$Y$
1	0	$I_2$

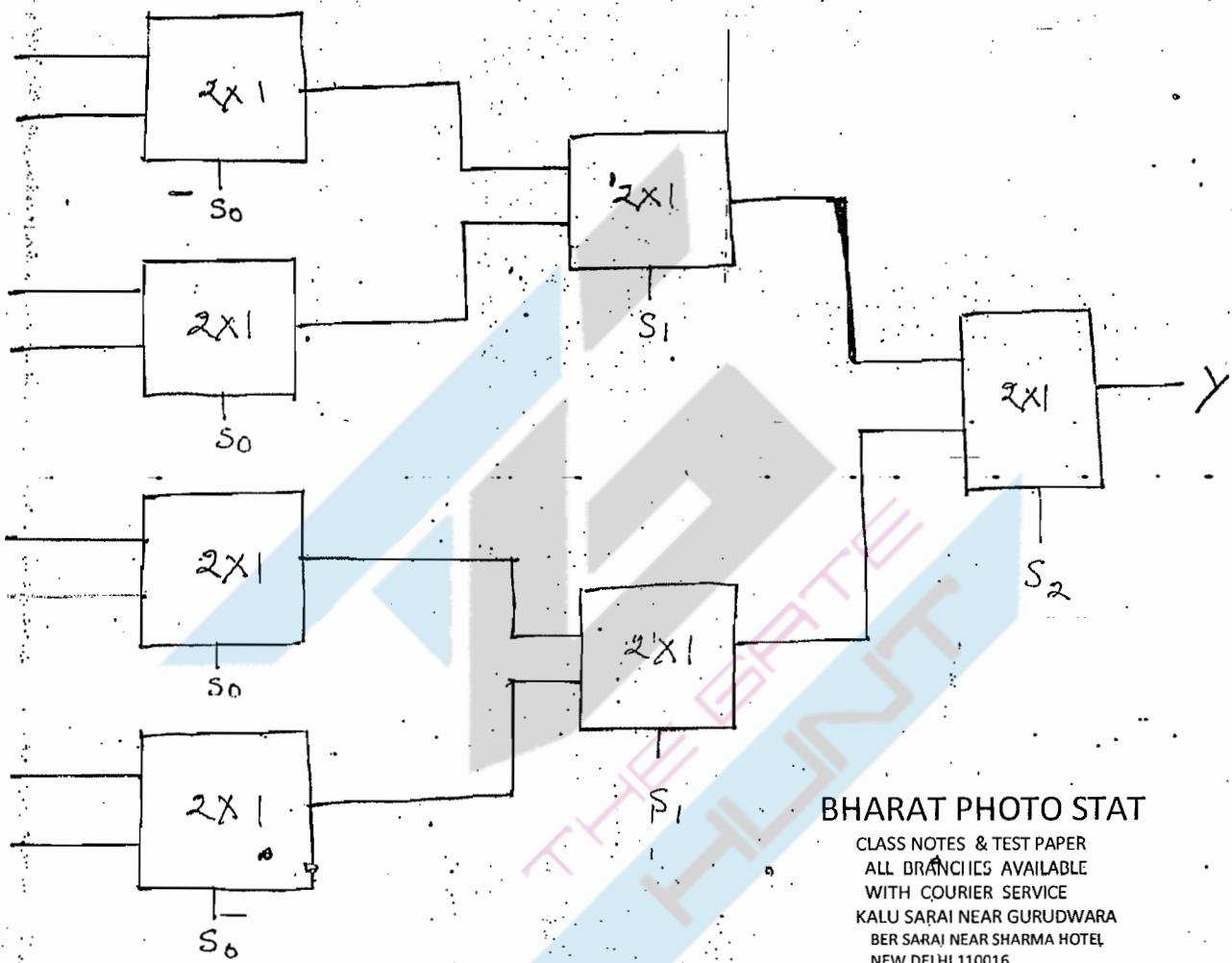


(b) 8x1 MUX Using 2x1 MUX:-

$8 \times 1 \longrightarrow 2 \times 1 \text{ MUX}$

$$\frac{8}{2} = 4, \frac{4}{2} = 2, \frac{2}{2} = 1$$

$$\text{No. of MUX required} = 4 + 2 + 1 = 7$$



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(c) 16x1 MUX using 2x1 MUX:-

$16 \times 1 \longrightarrow 2 \times 1$

$$\frac{16}{2} = 8, \frac{8}{2} = 4, \frac{4}{2} = 2, \frac{2}{2} = 1$$

$$\text{No. of MUX req.} = 8 + 4 + 2 + 1 = 15$$

Note:-

No. of MUX req.

$$\Rightarrow 64 \times 1 \xrightarrow{63} 2 \times 1$$

$$\Rightarrow 256 \times 1 \xrightarrow{255} 2 \times 1$$

$$\Rightarrow 2^n \times 1 \xrightarrow{2^n-1} 2 \times 1$$

$n = \text{select i/p}$

$2^D = \text{i/p's}$

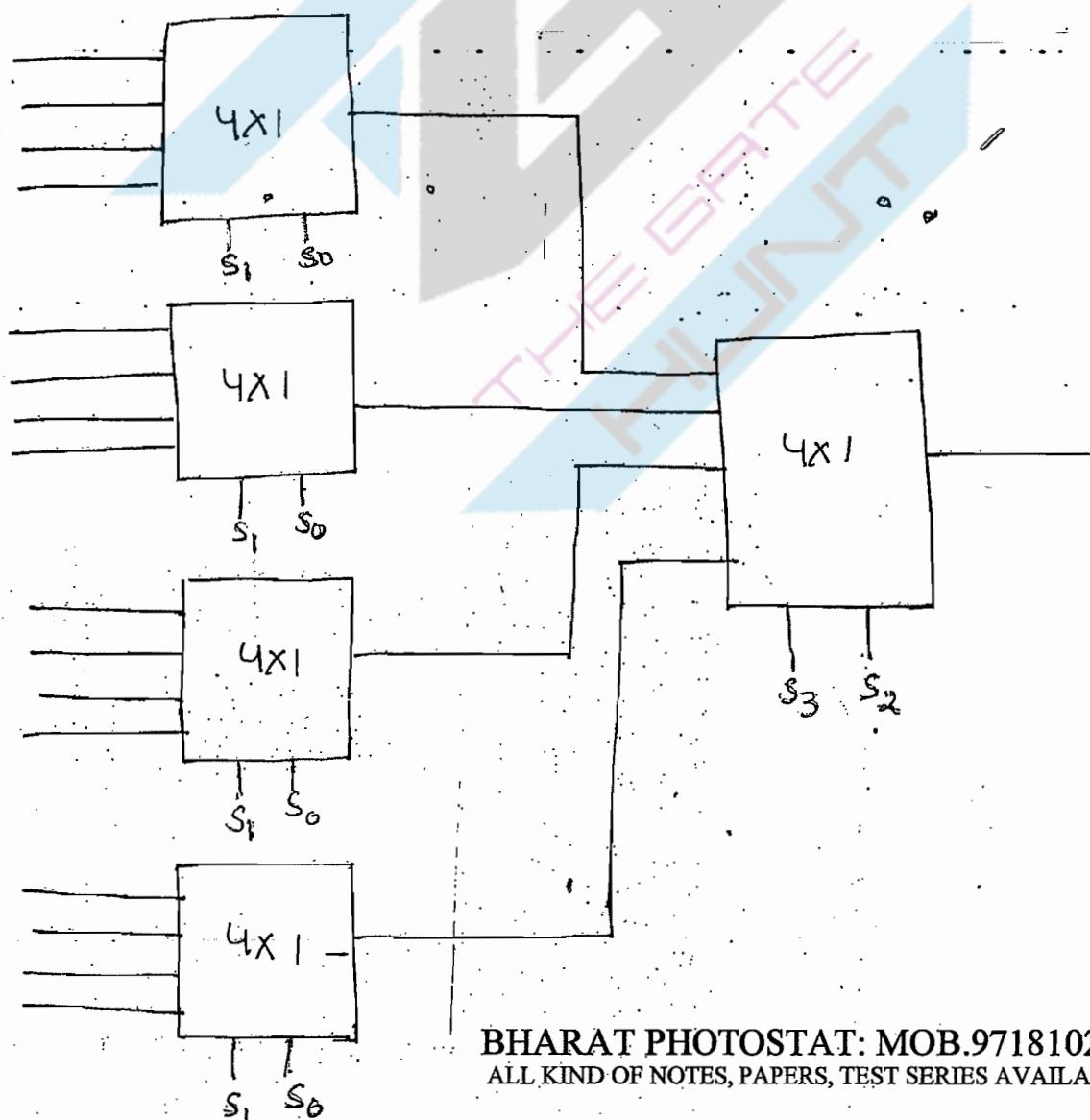
(d) 16x1 MUX Using 4x1 MUX :-

$$16 \times 1 \longrightarrow 4 \times 1$$

$s_3 \ s_2 \ s_1 \ s_0$

$$\frac{16}{4} = 4, \quad \frac{4}{4} = 1$$

No. of MUX Req =  $4+1 = 5$



Note:-

No. of MUX

Required

⇒

64 x 1

21

4 x 1

⇒

64 x 1

9

8 x 1

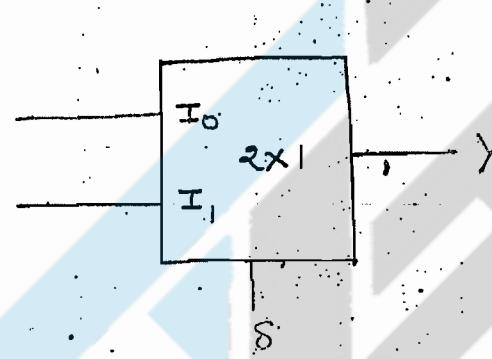
⇒

256 x 1

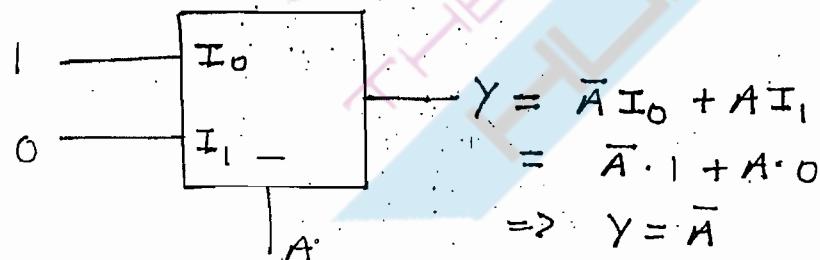
17

16 x 1

## (2) MUX as Universal Logic Circuit :-

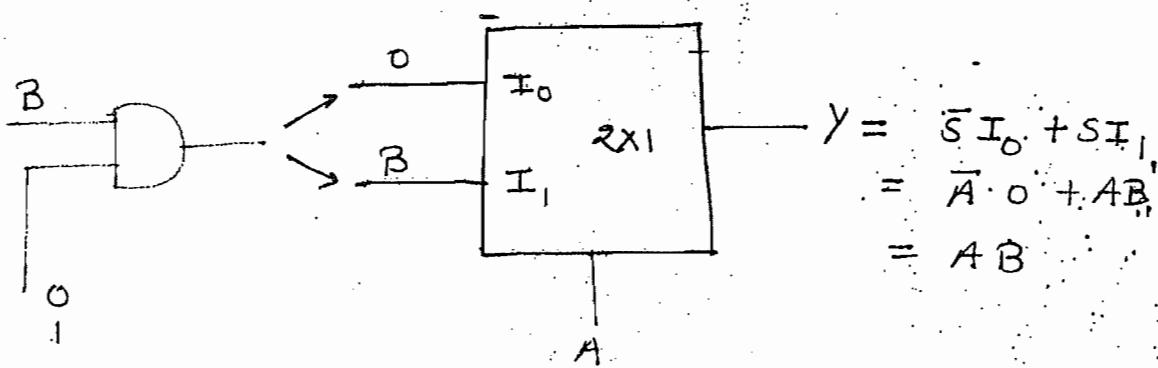


### (a) NOT Gate :-



A	Y
0	1
1	0

(b) AND Gate:-



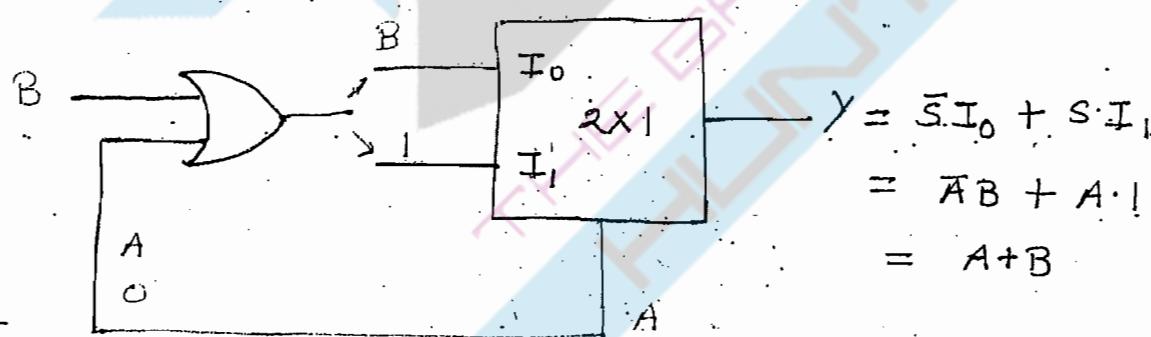
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	Y
0	0
1	B

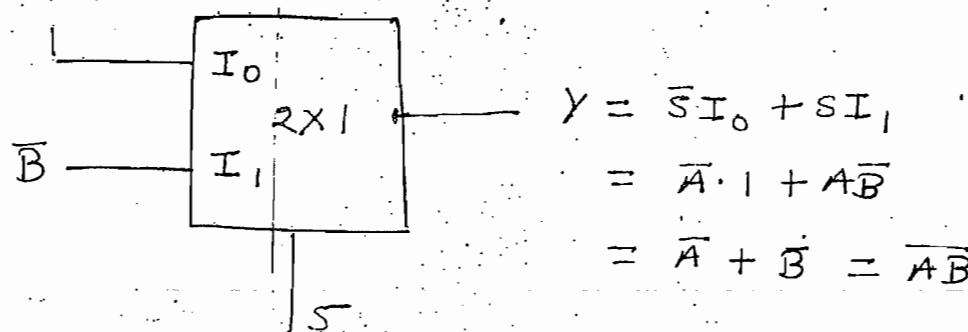
$\rightarrow I_0$   
 $\rightarrow I_1$

$$Y = \bar{A} \cdot \bar{B} + AB = AB$$

(c) OR Gate:-

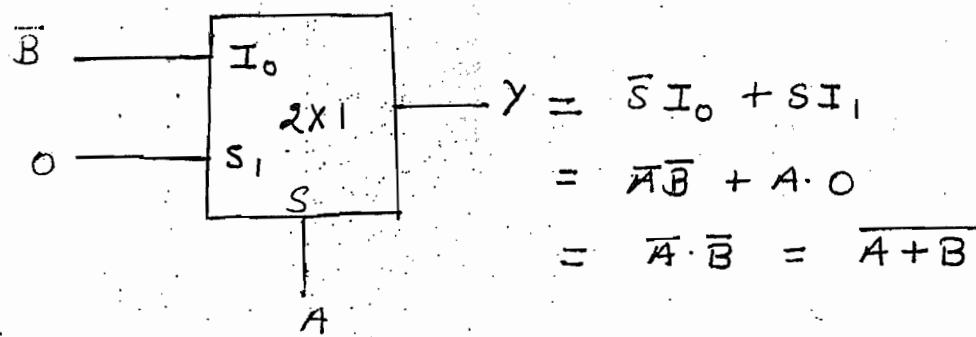


(d) NAND Gate:-



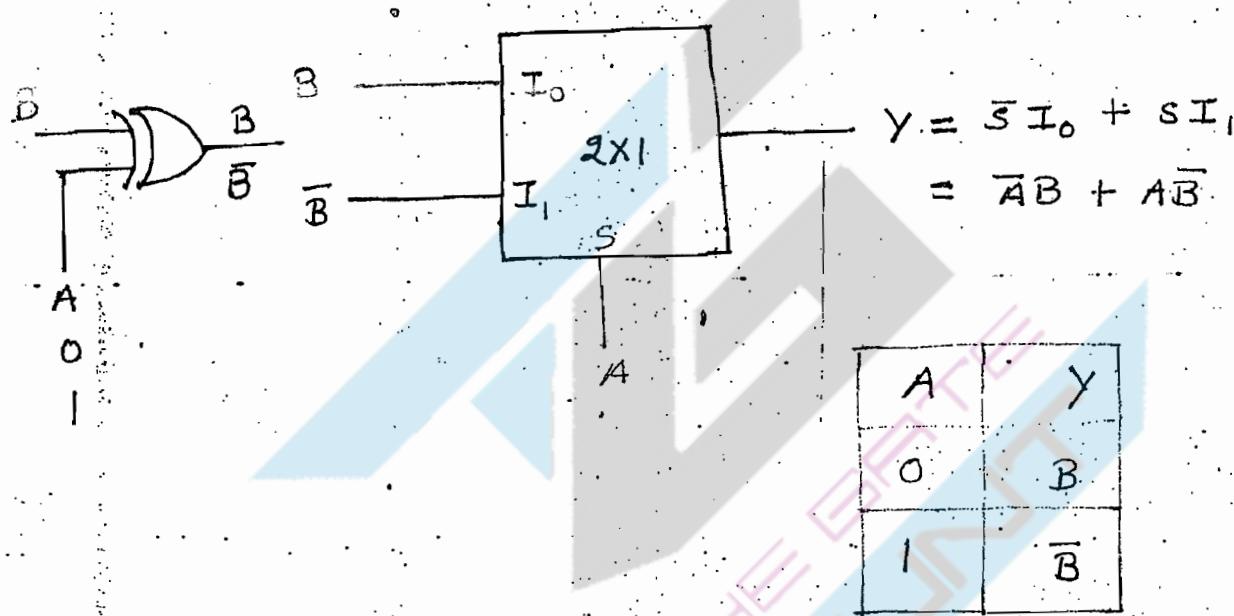
No. of 2x1 MUX implement NAND is 2

(c) NOR Gate :-

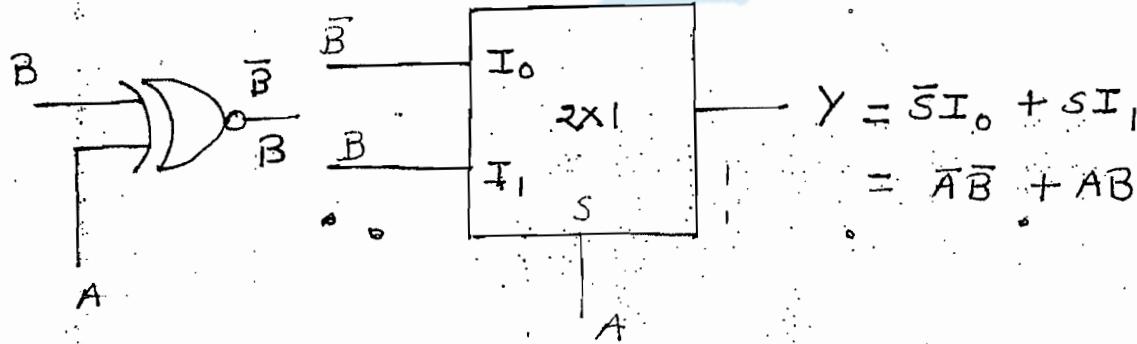


No. of MUX 2x1 MUX to implement NOR is 2.

(f) EXOR Gate :-



(g) EX-NOR Gate :-



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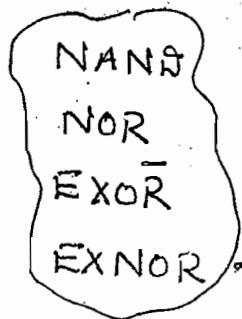
Ques:- To implement 2 i/p. exclusive OR gate & AND gate min. no. of 2x1 MUX required

Ans:- 2, 1

Note:-



→ Required ① → 2x1 MUX



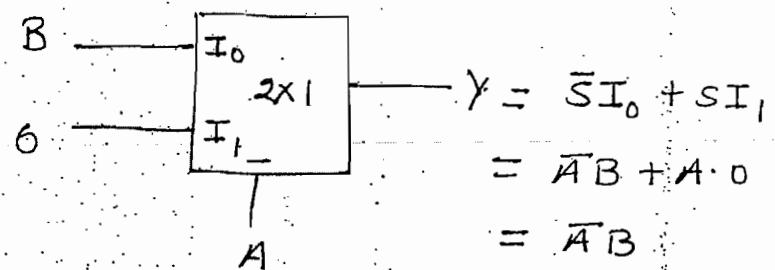
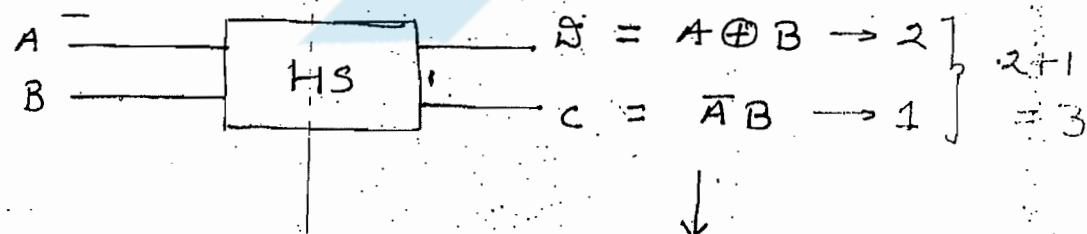
→ Required ② → 2x1 MUX

→ To implement half adder, No. of 2x1 MUX

(I) HA  $\xrightarrow{3}$  2x1 MUX

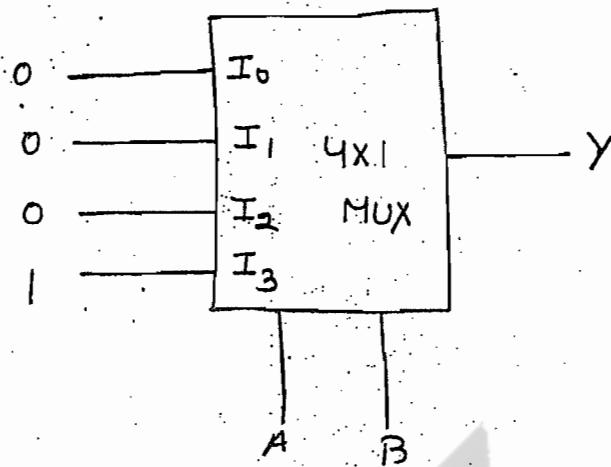


(II) HS  $\xrightarrow{3}$  2x1 MUX



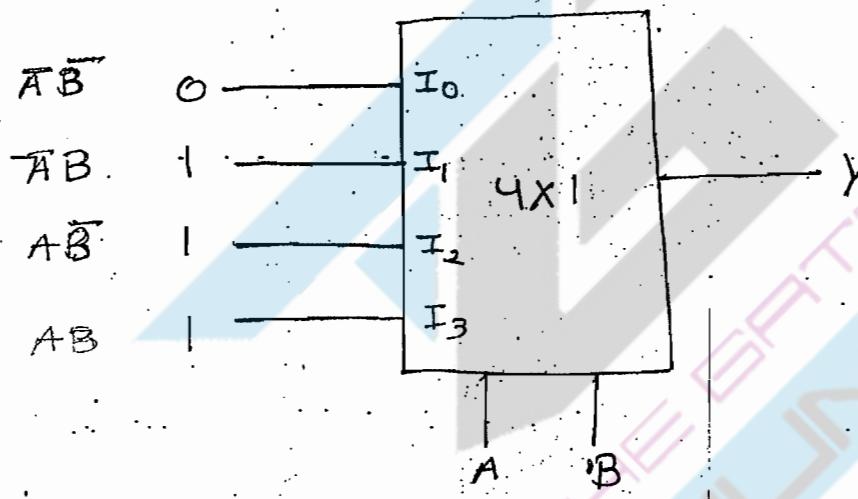
# 4x1 MUX as Universal circuit:-

(i) AND :-



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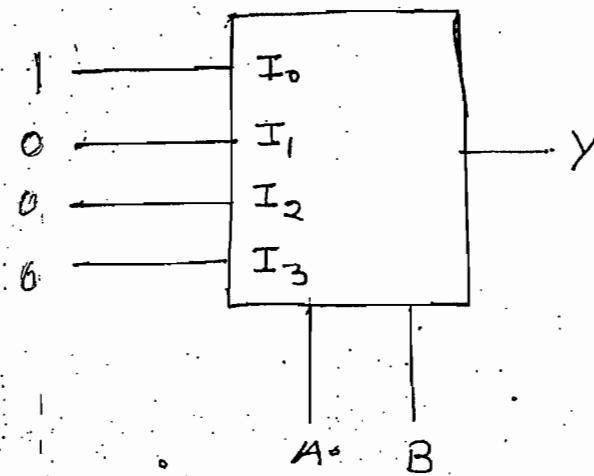
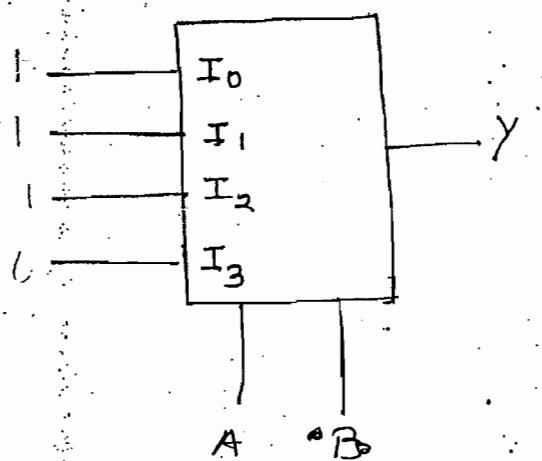
(ii) OR :-



(iii) NAND :-

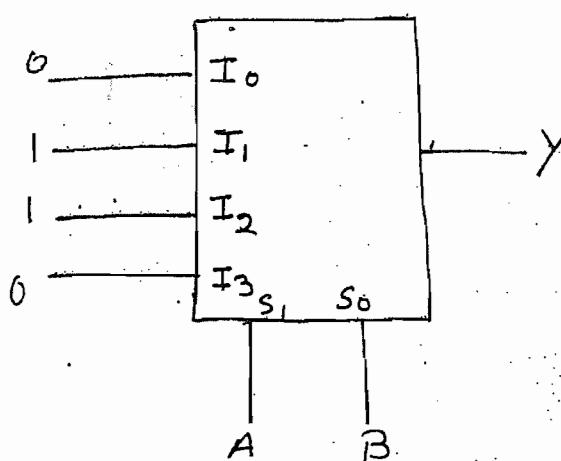
(iv)

NOR :-



e. (v) EXOR :-

NOTE :-



$$\Rightarrow HA \xrightarrow{2} -4 \times 1$$

$$\Rightarrow HS \xrightarrow{2} 4 \times 1$$

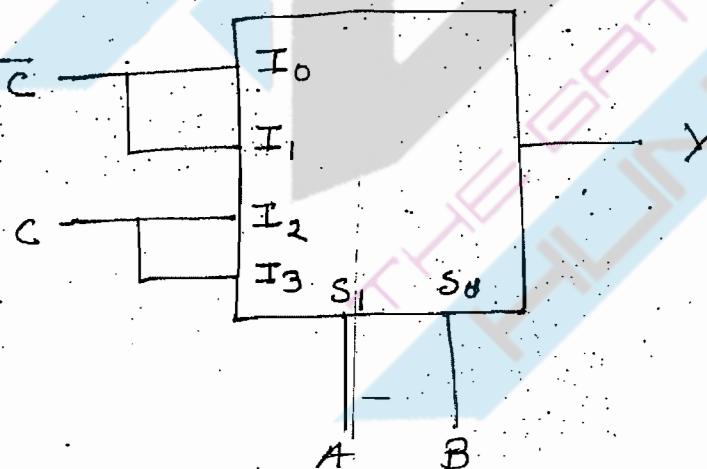
$\begin{array}{l} HA \\ HS \end{array} \Big] \ 5 \rightarrow NAND/NOR$

$\begin{array}{l} HA \\ HS \end{array} \Big] \ 3 \rightarrow (2 \times 1) MUX$

$\begin{array}{l} HA \\ HS \end{array} \Big] \ 2 \rightarrow (4 \times 1) MUX$

3. Determine minimised logical expression for given MUX circuit:-

Ans:-



(a)  $A \oplus B$

(b)  $A \odot B$

(c)  $A \oplus C$

(d)  $A \odot C$

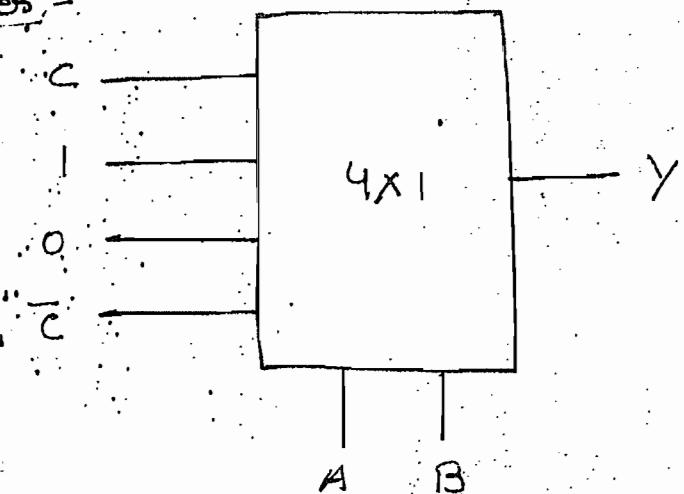
Soln:-  $y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$

$$= \cancel{\bar{A}\bar{C}} + \cancel{A\bar{C}} = \cancel{\bar{A}\bar{C}} + \cancel{ABC}$$

$$= \bar{A}\bar{C} + AC$$

$$= A \odot C$$

Ques:-



$$\text{Sol'n!- } Y = \bar{A}\bar{B}C + \bar{A}B + O$$

$$+ AB\bar{C}$$

$$\Rightarrow Y = \bar{A}\bar{B}C + B(\bar{A} + AC)$$

$$= \bar{A}\bar{B}C + B(\bar{A} + \bar{C})$$

$$= \bar{A}\bar{B}C + \bar{A}B + BC$$

$$= \bar{A}(\bar{B}C + B) + BC$$

$$= \bar{A}(B + C) + BC$$

$$= \bar{A}B + \bar{A}C + BC$$

$$= \bar{A}C + BC$$



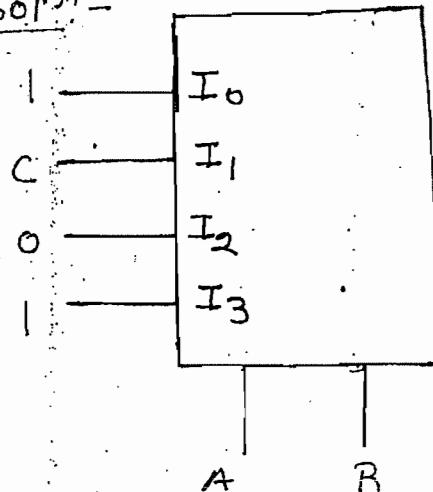
(4.) Implementation of given logical expression

using MUX:-

Ques:- Implement f(A, B, C) =  $\sum m(0, 1, 3, 6, 7)$

Using 4x1 MUX with AB as select line

Sol'n!-



A	B	$\bar{C}$	
0	0	0	0 $\rightarrow$ C
0	0	1	1 $\rightarrow$ C
1	0	0	0 $\rightarrow$ C
1	0	1	1 $\rightarrow$ C
2	0	0	0 $\rightarrow$ C
2	0	1	1 $\rightarrow$ C
3	0	0	1 $\rightarrow$ C
3	0	1	1 $\rightarrow$ C
4	1	0	0 $\rightarrow$ C
4	1	1	1 $\rightarrow$ C
5	1	0	1 $\rightarrow$ C
5	1	1	1 $\rightarrow$ C
6	1	1	0 $\rightarrow$ C
6	1	1	1 $\rightarrow$ C
7	1	1	1 $\rightarrow$ C
7	1	1	1 $\rightarrow$ C

## Implementation Table :-

	$I_0$	$I_1$	$I_2$	$I_3$
$\bar{C}$	⑥	2	4	⑥
$C$	①	③	5	⑦

↓      ↓      ↓      ↓

1      C      0      1

Ques:- Implement  $f(A, B, C) = \sum m(1, 2, 4, 5, 7)$  using  
 4:1 MUX with  
 (i) AB as select line  
 (ii) AC as select line  
 (iii) BC as select line

Note:-

- ⇒ Using one 4x1 MUX
  - any 2 variables
  - some of 3 variable
- ⇒ Using one 4x1 MUX
  - any 2 variables
  - any 3 variable
- ⇒ Using one 8x1 MUX
  - any 3 variable
  - some of 4 variables
- ⇒  $n \rightarrow 2^n \times 1$  ⇒  $n$  variable  $\rightarrow 2^{n-1} \times 1$   
 one No

questions:-

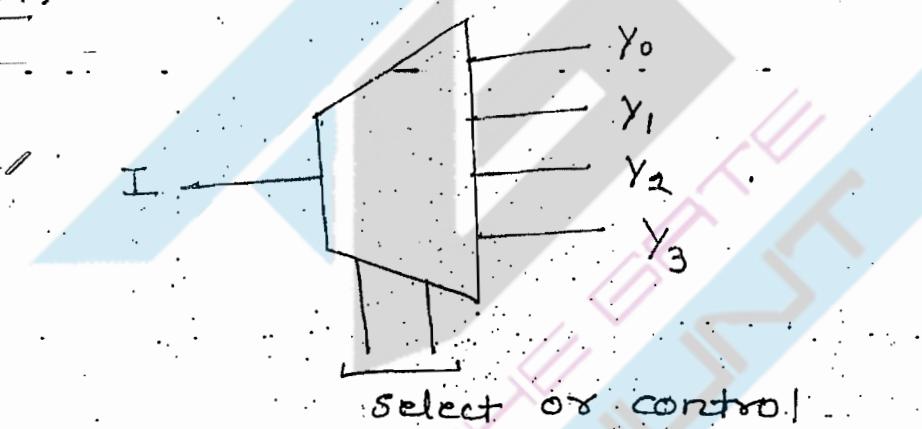
- Sum of FA
- FA using 4x1 MUX
- FA using 8x1 MUX
- $f(A, B, C) = A + \bar{B}C$
- $f(A, B, C) = \prod M(0, 1, 2, 5)$

## DEMUX:-

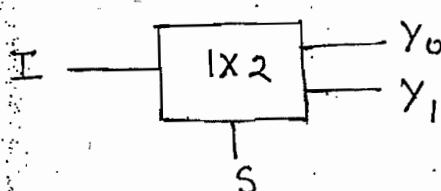
- It is a combinational circuit having many o/p and one i/p depending on the select control.
- I/P is transferred to one of the o/p line. Hence, it is known as 1 to many circuit. It is also called data distributor.
- It is serial to parallel converter.



## Symbol:-



## 1:2 DEMUX:-

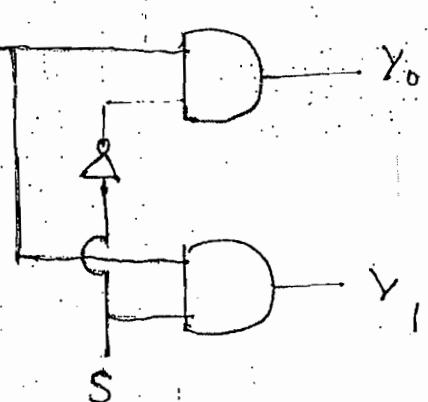


S	$Y_1$	$Y_0$
0	0	I
1	I	0

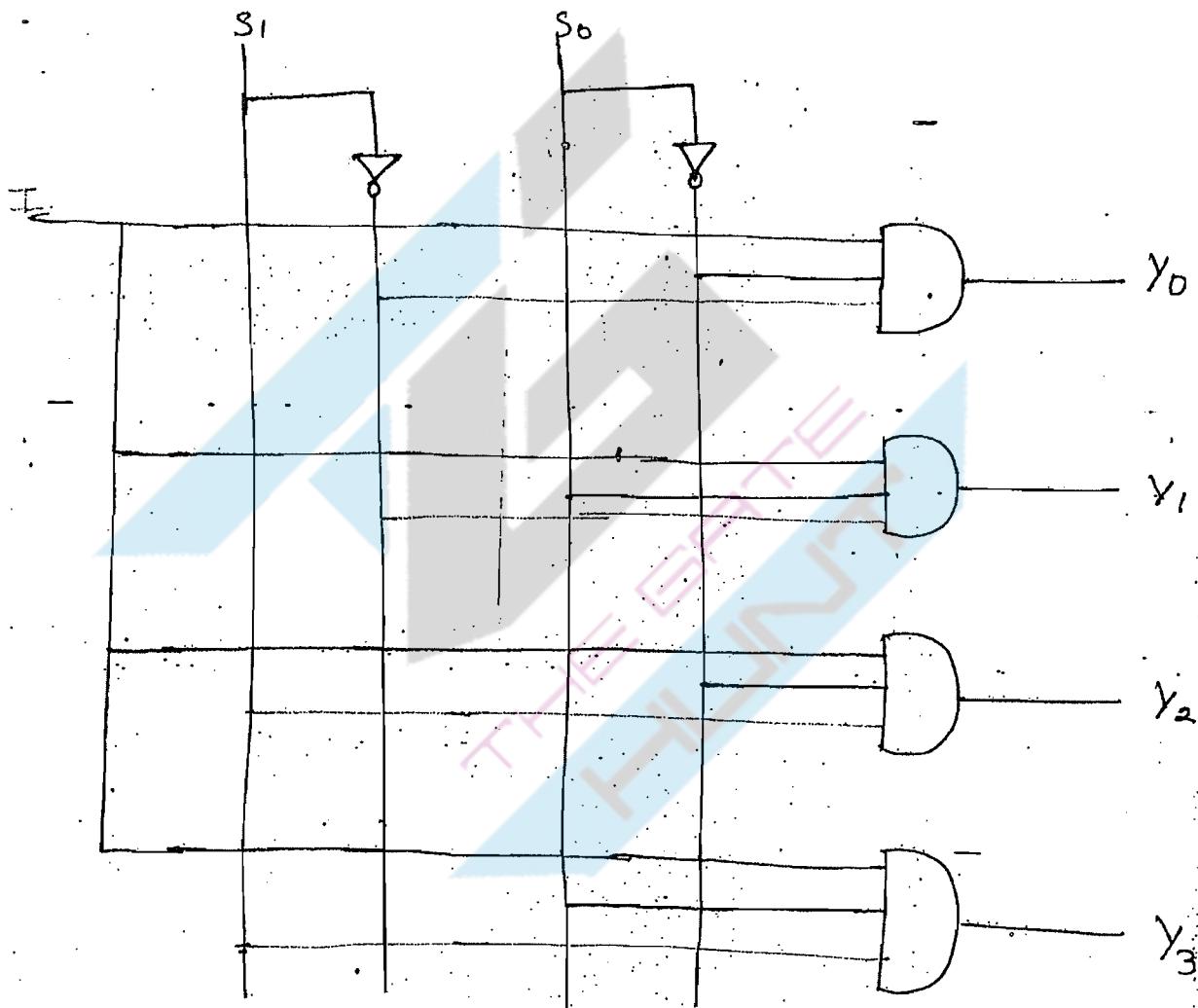
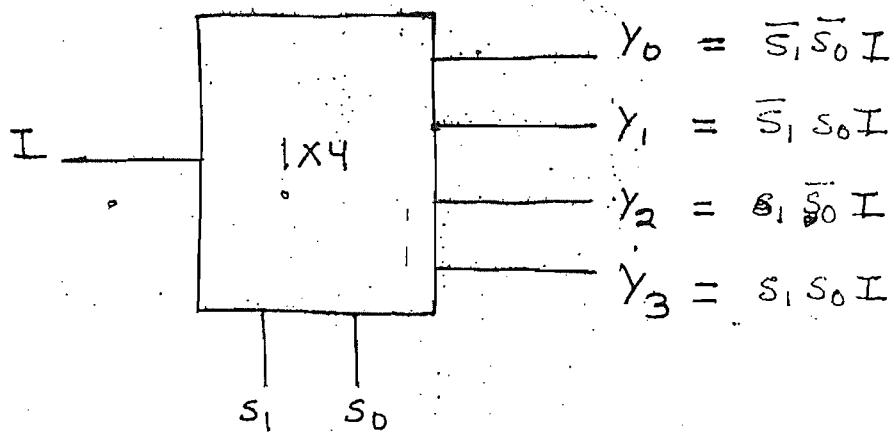
$$Y_0 = \bar{S}I$$

$$Y_1 = S I$$

- DEMUX contain AND gate N/W only.



1x4 DEMUX :-



Higher Order MUX DEMUX using Lower Order:

$$1 \times 4 \text{ DEMUX} \xrightarrow{1+2=3} 1 \times 2$$

$$4 \times 1 \text{ DEMUX} \xleftarrow[2+1]{3} 2 \times 1$$

$$1 \times 8 \text{ DEMUX} \xrightarrow{7} 1 \times 2$$

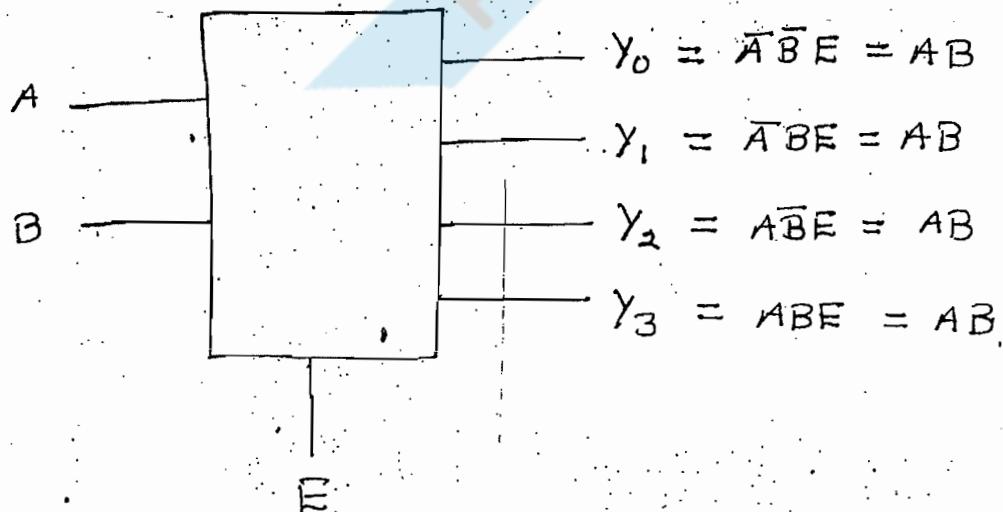
$$8 \times 1 \xrightarrow{7} 2 \times 1$$

$$\begin{array}{r}
 \Rightarrow 1 \times 16 \quad \frac{5}{1+4} \quad 1 \times 4 \\
 \Rightarrow 1 \times 64 \quad \frac{21}{1+4+16} \quad 1 \times 4 \\
 \Rightarrow 1 \times 64 \quad \frac{9}{1+8} \quad 1 \times 8 \\
 \Rightarrow 1 \times 256 \quad \frac{17}{1+16} \quad 1 \times 16
 \end{array}$$

### Decoder:-

- Decoder is a combinational circuit which has many data i/p's & many o/p's.
- Decoder is used to convert binary to other codes such as → Binary to octal ( $3 \times 8$ )  
→ BCD to decimal  
→ Binary to hexadecimal
- Decoder can be used to decode adder and will generate chip select signal.

$\overline{CS}$ , CS  
 Active low      Active high



E	A	B	$y_3$	$y_2$	$y_1$	$y_0$
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$$y_0 = \bar{A}\bar{B}E$$

$$y_1 = \bar{A}BE$$

$$y_2 = A\bar{B}E$$

$$y_3 = ABE$$

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→ Decoder and Demux internal circuit remain same

⇒ 2x4 DEMUX → 2x4 Decoder → 1x4 DEMUX

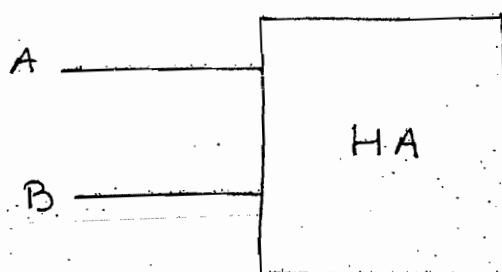
⇒ 3x8 → 1x8 DEMUX

⇒ 4x16 → 1x16

⇒ 8x256 → 1x256

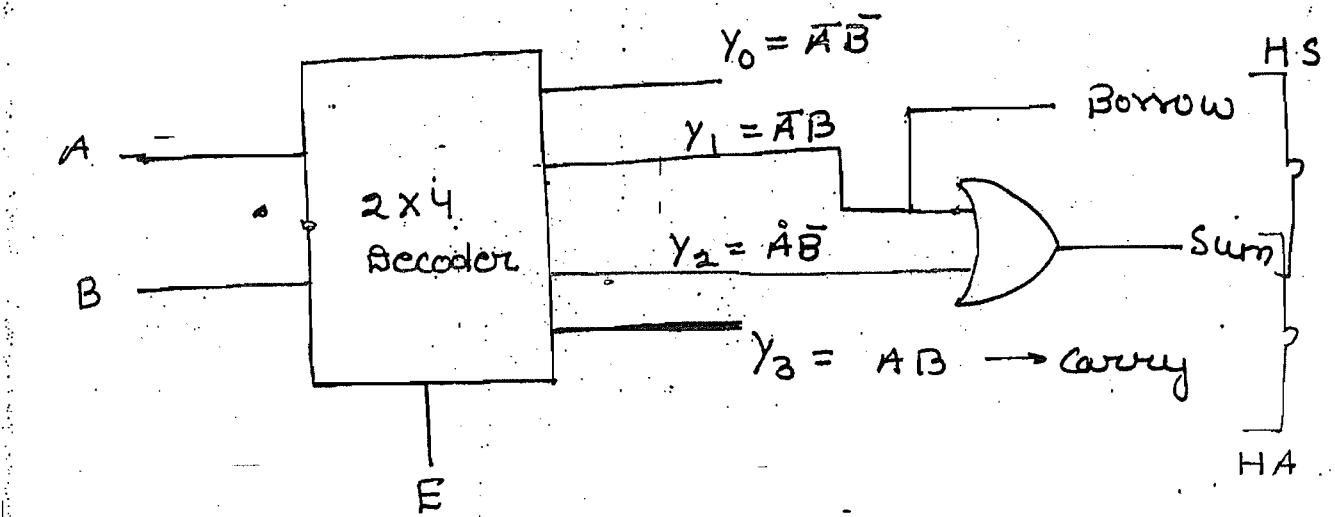
↓  
 select line → 8

Implement HA using 2x4 decoder circuit! -



$$\text{Sum} = \bar{A}\bar{B} + \bar{A}B + AB$$

$$\text{Carry} = AB$$



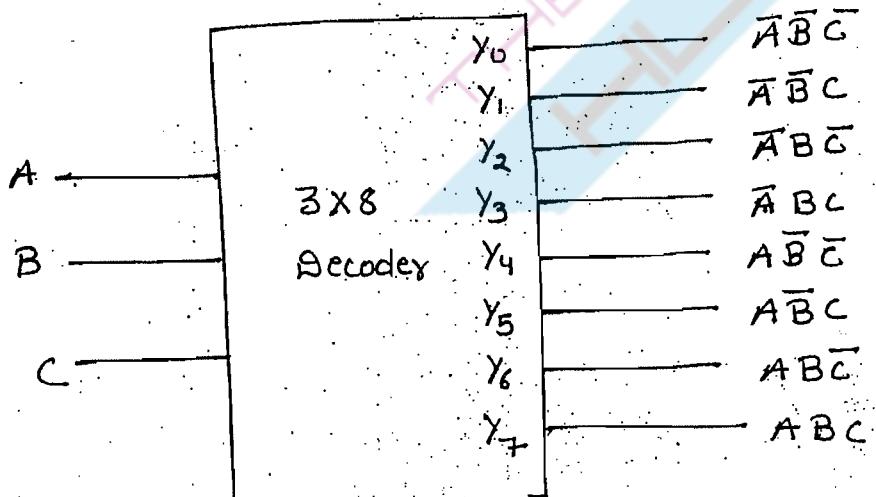
Implement HS! —



→ To implement HA one 2x4 and 1 OR gate is required.

→ To implement Both Subtract/Adder only 1 circuit with 2x4 decoder and 1 OR gate.

3x8 Decoder! —

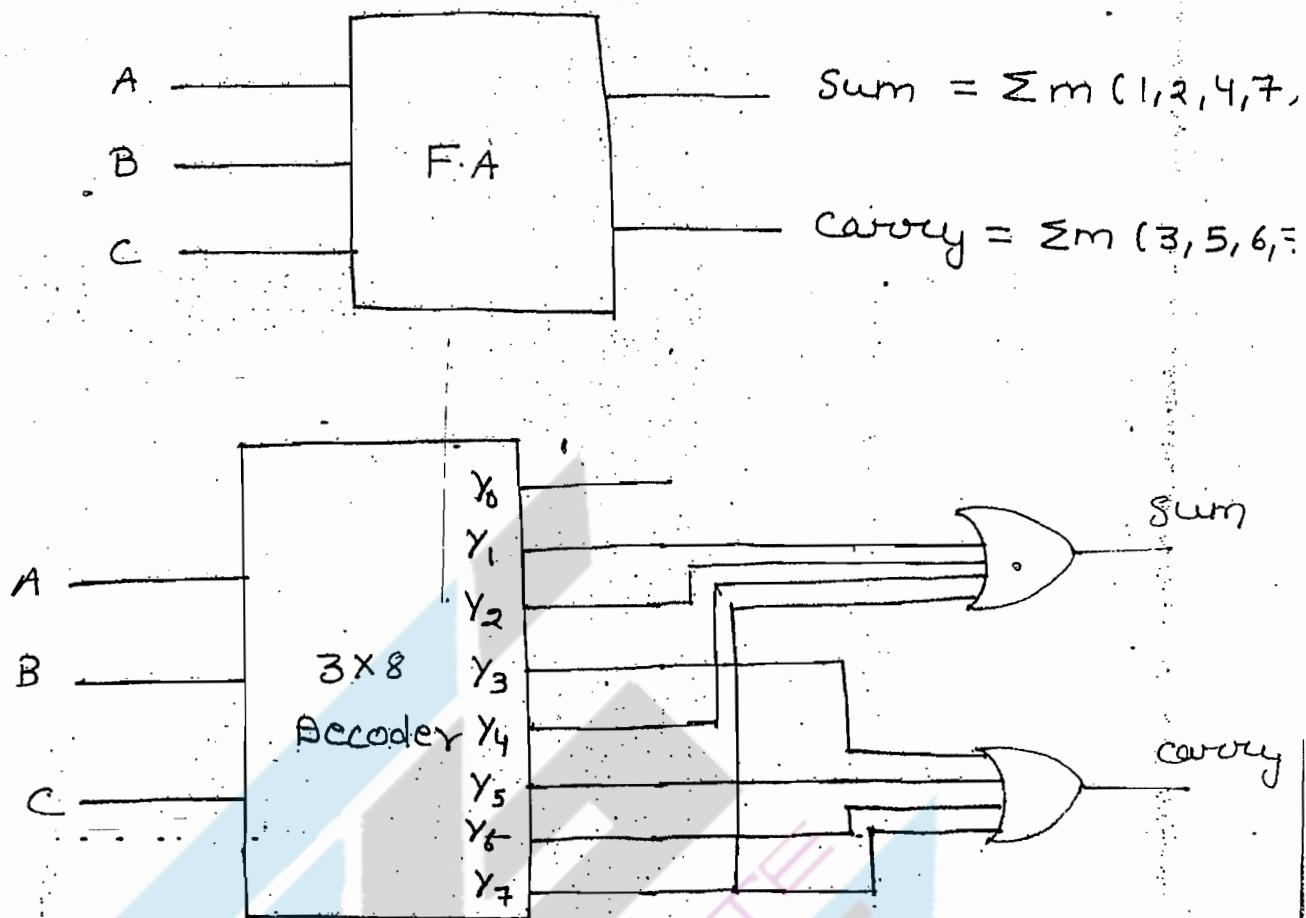


Binary to Octal! —

A	B	C	X
0	0	0	0
0	0	1	1
1	1	1	7

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- Implement FA circuit using 3x8 Decoder:-



Questions:-

Implement

(I) FS using 3x8 decoder

(II)  $f(A, B, C) = \sum m(1, 2, 4, 5, 7)$

(III)  $f(A, B, C) = \bar{A} + BC$

Ques:- 4x16 decoder any code conversion.

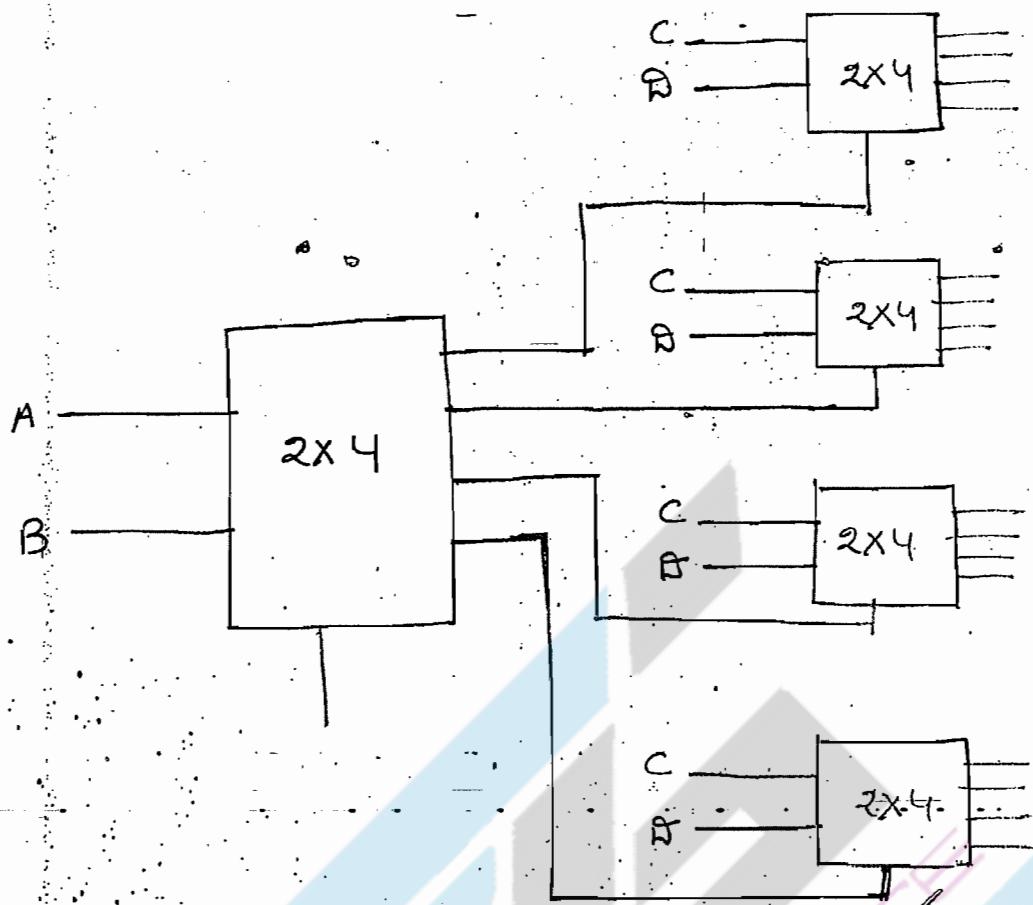
Implementation of Higher order decoders using lower order decoders:-

$$4 \times 16 \downarrow \xrightarrow{5(1+4)} 2 \times 4 \downarrow$$

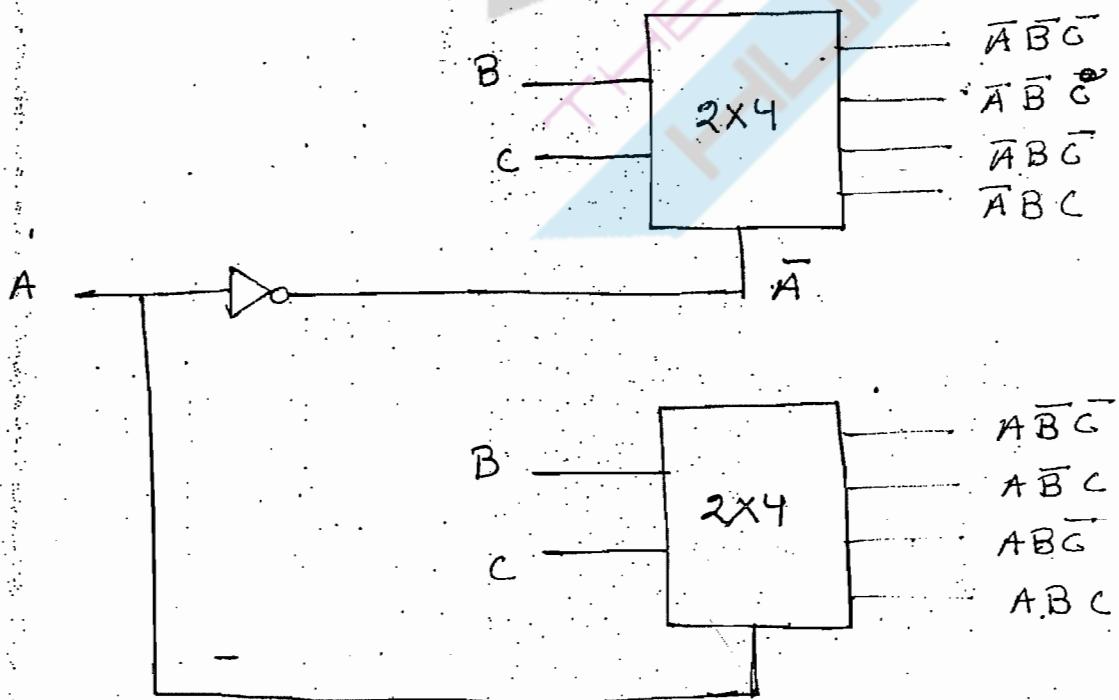
$$1 \times 16 \xrightarrow{5(1+4)} 1 \times 4$$

$$16 \times 1 \xrightarrow{5(4+1)} 4 \times 1$$

→  $4 \times 16$  using  $2 \times 4$  :-



⇒  $3 \times 8$  Using  $2 \times 4$  :-



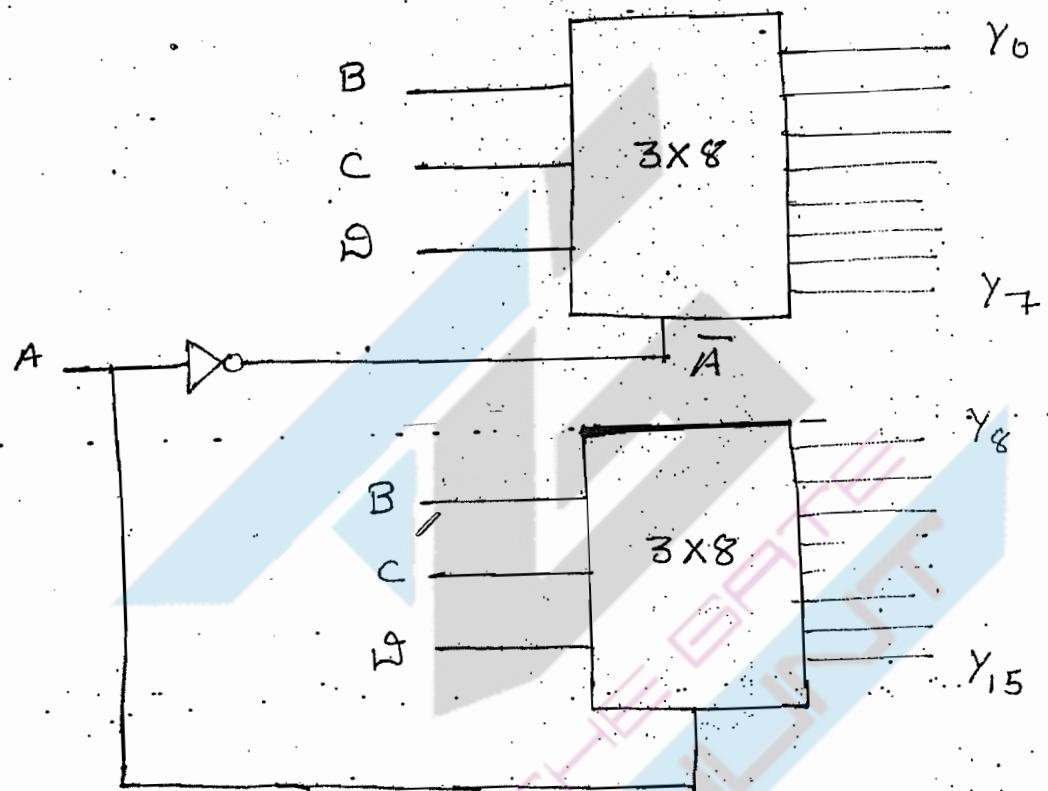
$$\Rightarrow 16 \times 64 \xrightarrow{21(1+4+16)} 2 \times 4 \downarrow$$

$$1 \times 64 \xrightarrow{21} 1 \times 4$$

$$\Rightarrow 8 \times 256 \xrightarrow{17(1+16)} 4 \times 16$$

→ Decoder / DEMUX → IC same

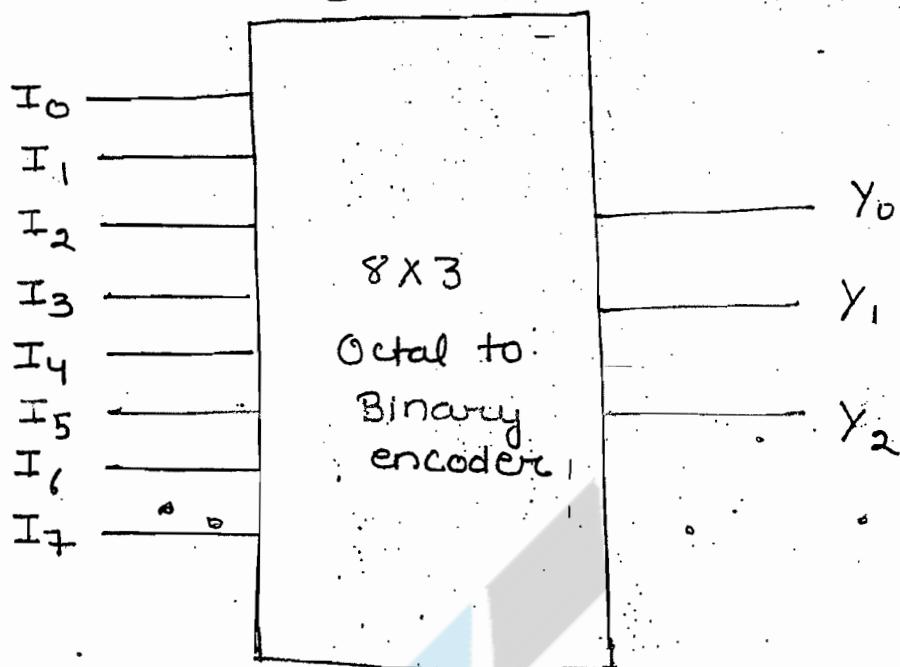
4x16 Using 3x8:



### ENCODER:-

- It is a combinational circuit which have many I/P & many O/P.
- It is used to convert other codes to binary such as
  - Octal to binary ( $8 \times 3$ )
  - Decimal to BCD ( $10 \times 4$ )
  - Hex to Binary ( $16 \times 4$ )

# Octal to Binary Encoder :- / 8x3 Encoder :-



→ In encoder one of the I/p line is high and corresponding binary is available at the O/p

I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

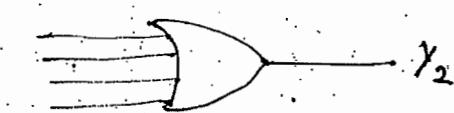
$$Y_0 = I_1 + I_3 + I_5 + I_7$$



$$Y_1 = I_2 + I_3 + I_6 + I_7$$



$$Y_2 = I_4 + I_5 + I_6 + I_7$$

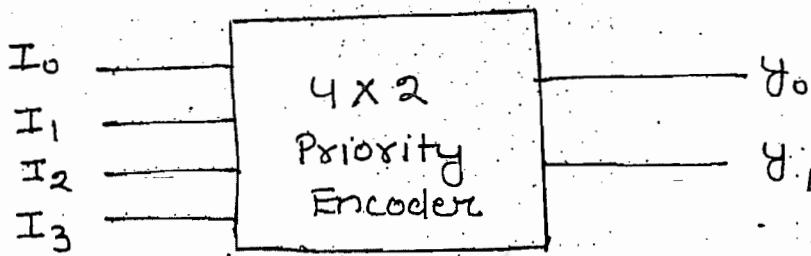


→ Encoder basic circuit is OR-gate.

Encoder

## Priority Encoder :-

- In priority encoder, any no. of i/p can be logic 1 but binary is available corresponding to highest priority i/p line at o/p

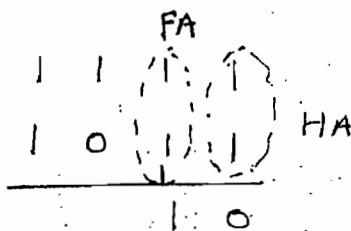


$I_3$	$I_2$	$I_1$	$I_0$	$Y_1$	$Y_0$
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

$$Y_1 = I_3 + \bar{I}_3 I_2 = I_3 + I_2$$

$$Y_0 = I_3 + \bar{I}_3 \bar{I}_2 I_1 = \bar{I}_3 + \bar{I}_2 I_1$$

## Adder :-



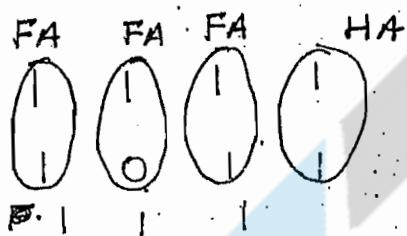
In order to add gp. of bits following adders are used.

- Serial adder
- Parallel adder
- Look ahead adder

### (i) Serial Adder:-

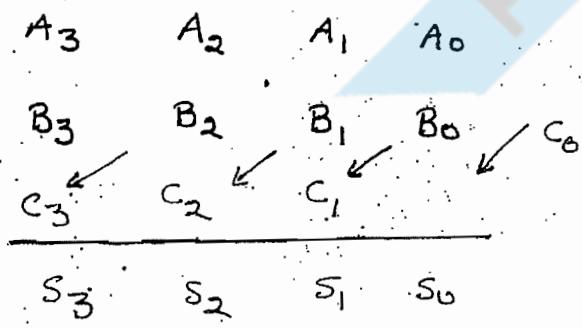
- In serial adder only 1 full adder is used to add any no of bits
- In this shift registers are used to provide data to full adder
- In serial adder to provide n-bit addition it requires min. n clock pulse
- serial adder is slowest adder

### (ii) Parallel Adders:-

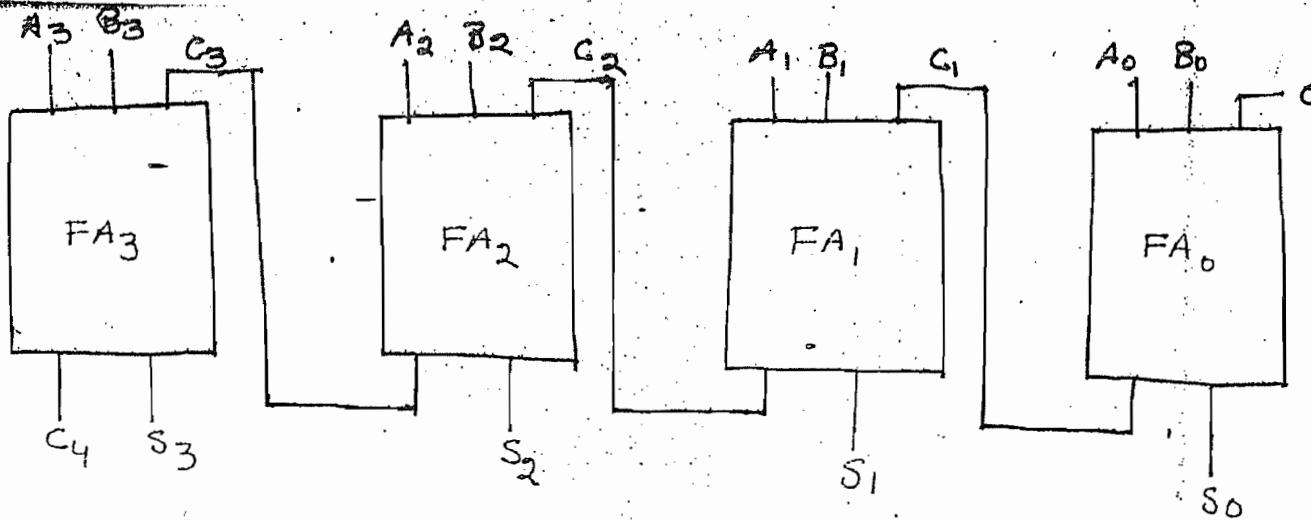


- In parallel adder each bit require separate adder circuits to provide n-bit addition in parallel adder , it requires  $(n-1)$  FA and 1 HA OR  $n$  FA  $(2n-1)$  HA and  $(n-1)$ . OR gates

### 4-bit Parallel adder circuit / Ripple carry Adders:-



$$\begin{array}{r}
 & 1 & 1 & 0 & 1 \\
 & 1 & 0 & 1 & 0 \\
 \hline
 & 1 & 1 & 1 & 0
 \end{array}$$



$C_4 \ S_3 \ S_2 \ S_1 \ S_0$

- In parallel adder each full adder will provide  $2t_{pd}$  delay to provide sum or carry o/p.
- In n-bit parallel adder to provide result, it require  $2N t_{pd}$  delay.
- In this carry propagation delay is present from i/p to o/p.
- As no. of bits are increase, carry propagation delay's increase. Hence it is known as ripple carry adder circuit.
- Its disadvantage is, as no. of bits are increase, speed of operation decrease.

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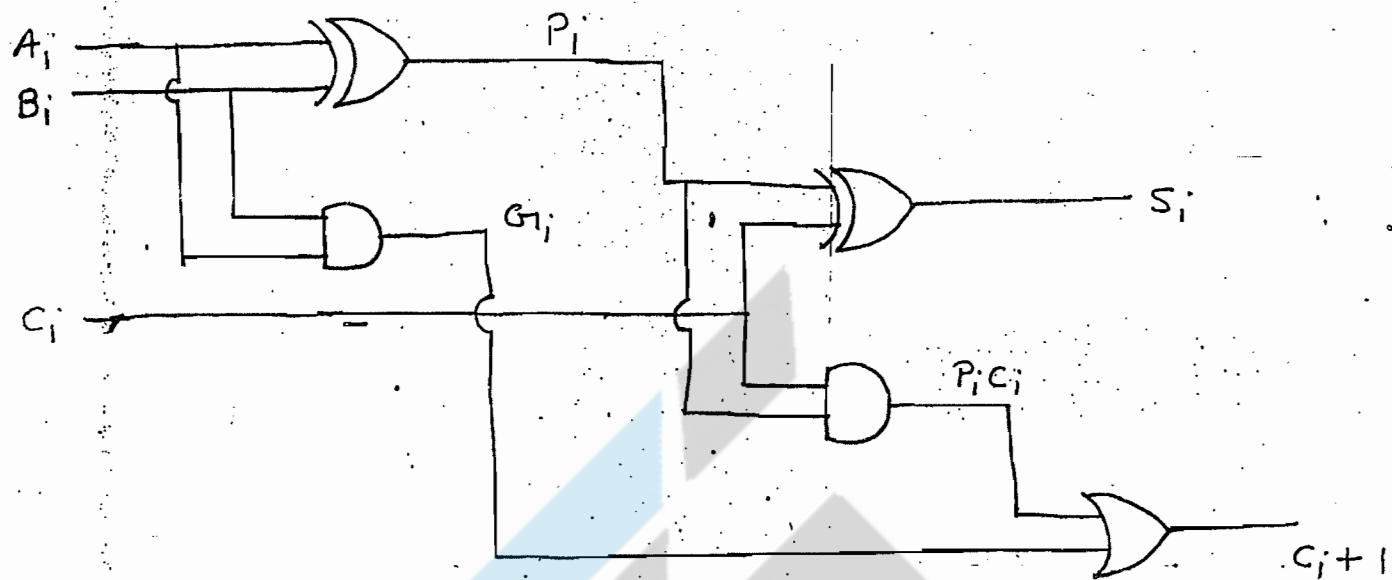
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## Look ahead carry circuit:-

→ To remove the disadvantage of parallel adder, look ahead carry circuit is designed.

## 4-Bit Look ahead carry adder circuit:-



$G_i$  = carry generator term     $P_i \rightarrow$  carry propagation term

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = P_i C_i + G_i$$

$P_0 = A_0 \oplus B_0$	$G_0 = A_0 \cdot B_0$	$S_0 = P_0 \oplus C_0$
$P_1 = A_1 \oplus B_1$	$G_1 = A_1 \cdot B_1$	$S_1 = P_1 \oplus C_1$
$P_2 = A_2 \oplus B_2$	$G_2 = A_2 \cdot B_2$	$S_2 = P_2 \oplus C_2$
$P_3 = A_3 \oplus B_3$	$G_3 = A_3 \cdot B_3$	$S_3 = P_3 \oplus C_3$

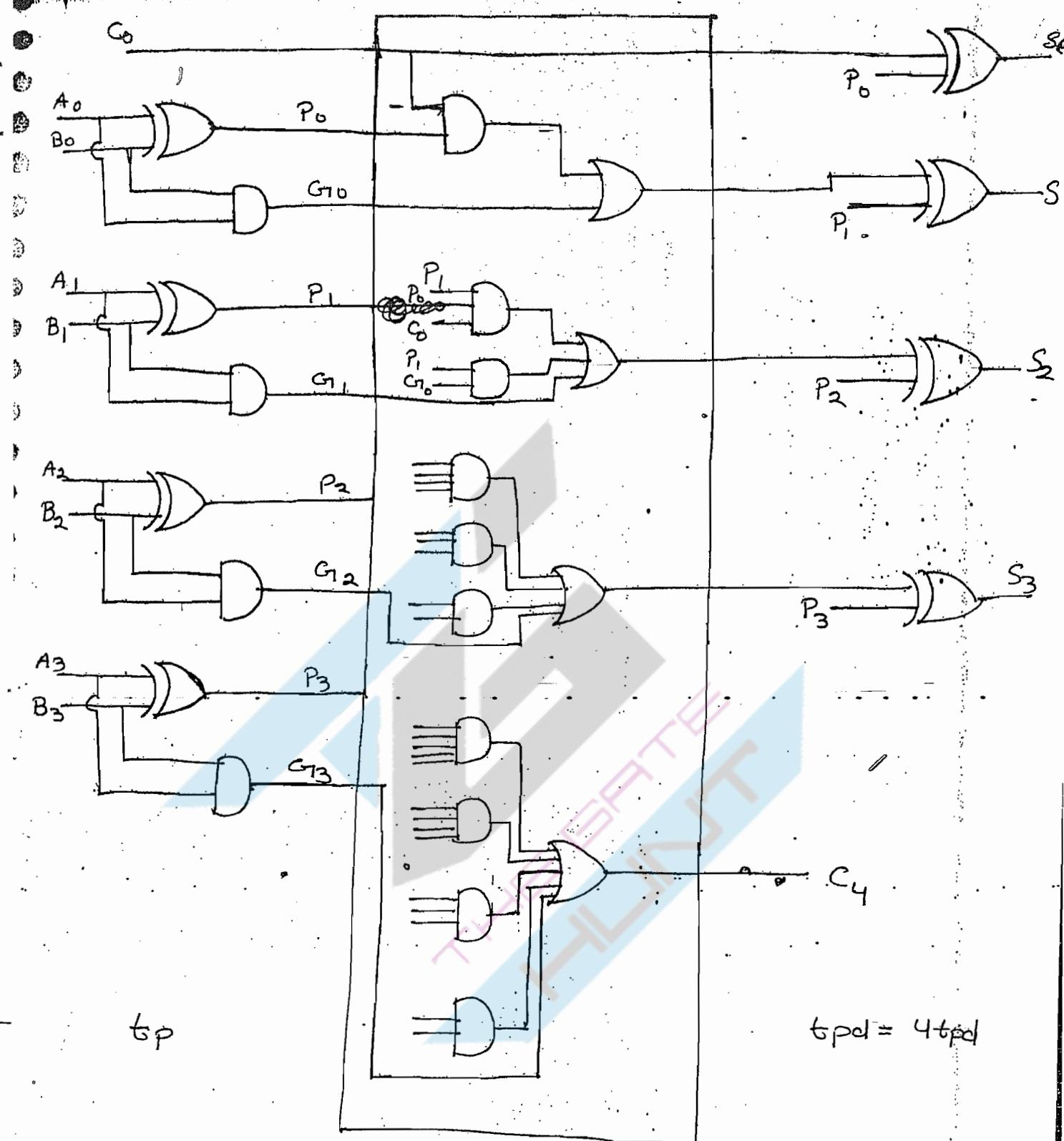
$C_0 \rightarrow$  input carry

$$C_1 = P_0 C_0 + G_0$$

$$C_2 = P_1 C_1 + G_1 = P_1 (P_0 C_0 + G_0) + G_1 = P_1 P_0 C_0 + P_1 G_0 + G_1$$

$$C_3 = P_2 C_2 + G_2 = P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$

$$C_4 = P_3 C_3 + G_3 = P_3 P_2 P_1 P_0 C_0 + P_3 P_2 P_1 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$$



2 - Logic levels

- In look ahead carry adder, carry generated by 2-level AND-OR N/W.
- In look ahead carry N/W, no. of AND-gate used  
=  $\frac{n(n+1)}{2}$
- No. of OR gate = n

- If all logic gates have same tpd (AND, OR, EXOR), then to provide carry, delay =  $3 \text{tpd}$
- to provide sum, delay =  $4 \text{tpd}$
- Propagation is independent of No. of bits and depends on no. of level
- LAC is fastest adder
- In this O/P is generated directly from i/p bits

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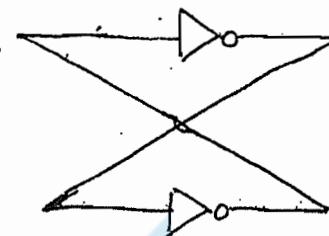
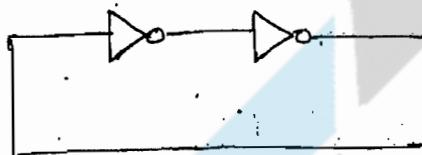
## Sequential circuits

### Flip Flops :-

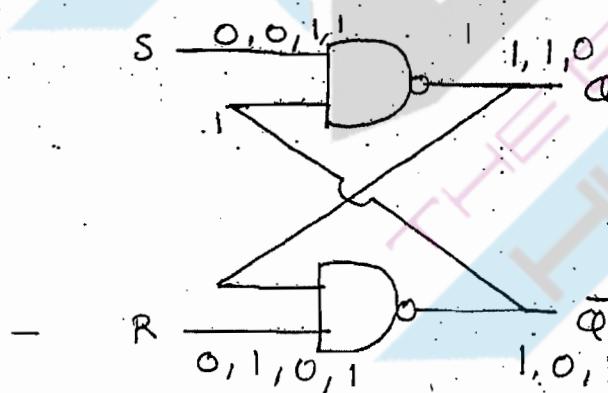
- Basic memory element
- stores 1 bit
- Having two stable state. Hence it is known as bistable multivibrator
- Having two outputs which are complementary to each other

### SR Latch :-

#### (I) Using NOT Gate :-



#### (II) Using NAND Gate :-



S	R	Q
0	0	Invalid
0	1	1
1	0	0
1	1	Previous State

→ Previous state ( $Q = 0, \bar{Q} = 1$  OR  $Q = 1, \bar{Q} = 0$ )

Note :-

$\equiv$

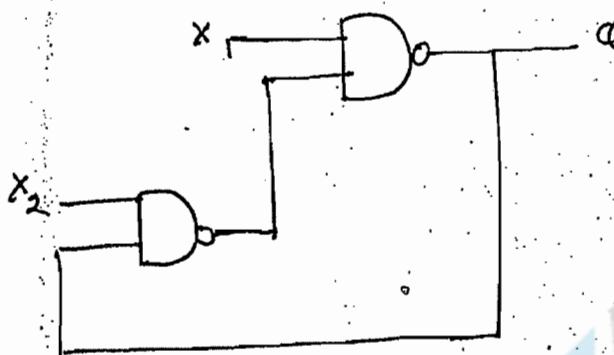
Invalid  
 $Q = 1, \bar{Q} = 1$

NAND

- Prev In SR latch if both gates are disable then O/P is in invalid state
- If both gates are enable then O/P remains in previous state, if previous state is valid state.

- If both gates are enable, o/p of SR latch is in  
 $Q=0, \bar{Q}=1$   
 OR  
 $Q=1, \bar{Q}=0$

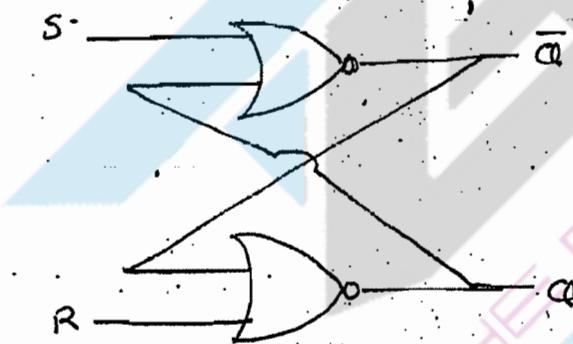
Cause:- The circuit shown in figure is NAND latch if i/p  
 $X_1=0, X_2=1$  applied then o/p Q will be



- (a) logic 0  
 (b) logic '1'  
 (c) Invalid  
 (d) Previous state

Ans - b.

(iii) Using NOR :-



S	R	Q
0	0	Prev. State
0	1	0
1	0	1
1	1	Invalid

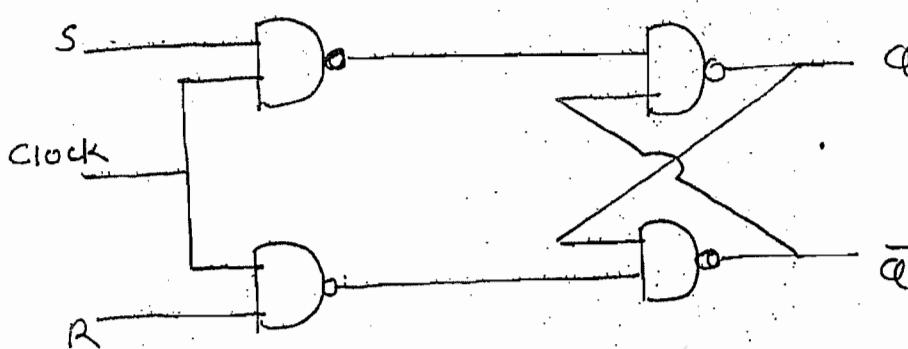
→ Invalid ( $Q=0, \bar{Q}=0$ ) → For NOR

Application of SR Latch :-

- SR latch is mainly used as memory element in digital circuit.
- To eliminate bounce in switches or keyboard SR latch is used.

## SR FF :-

### (i) Using NAND :-



Before  
Clock

$Q$   
 $Q_{in}$

After  
Clock

$Q+$   
 $Q_{in+1}$

Clock	S	R	$Q_{in+1}$
0	X	X	$Q_{in}$
1	0	0	$Q_{in}$
1	0	1	0
1	1	0	1
1	1	1	Invalid

Note:-

→ The purpose of two NAND gate (first) is to

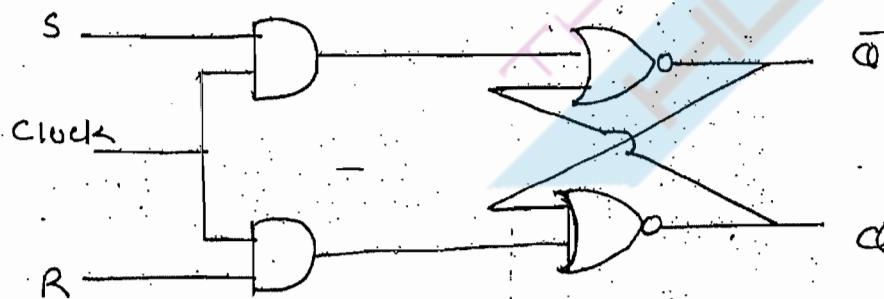
Memory → How to invert the (1)

→ Reset

→ Set

→ Unused state

### (ii) Using NOR Latch :-



Clock	S	R	$Q_{in+1}$
0	X	X	$Q_{in}$
1	0	0	$Q_{in}$
1	0	1	0
1	1	0	1
1	1	1	Invalid

→ Memory

→ How

→ Reset

→ Set

→ Unused state

### Characteristic Table :-

S	R	$Q_n$	$Q_{n+1}$	
0	0	0	0	HOLD ( $Q_n$ )
0	0	1	1	
0	1	0	0	
0	1	1	0	Reset
1	0	0	1	
1	0	1	1	Set
1	1	0	X	
1	1	1	X	

### Characteristic Equation :- (For O/P finding)

$$Q_{n+1} = \sum m(1, 4, 5) + \sum d(6, 7)$$

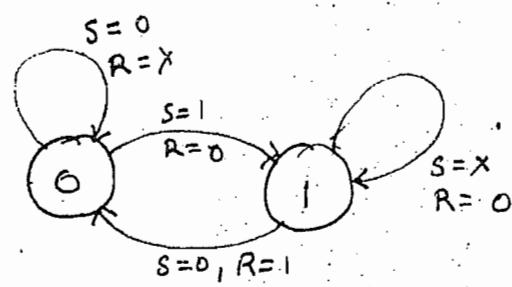
S	$R Q_n$	$\bar{R} Q_n$	$R Q_n$	$\bar{R} Q_n$
0		11		
1	11	X	X	

$$Q_{n+1} = S + \bar{R} Q_n \rightarrow S \cdot R \neq 1$$

### Excitation Table :- (For I/P finding)

$Q_n$	$Q_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

## State Diagram:-



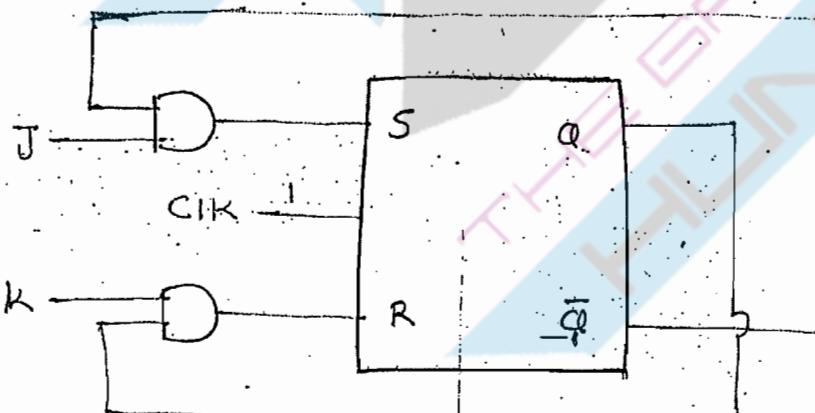
## Disadvantage :-

- Invalid state is present when S and R i/p is logical 1.
- To avoid this JK ff is used.

## JK FF :-

J	K	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q_n}$

→ Toggle



## SR to JK :-

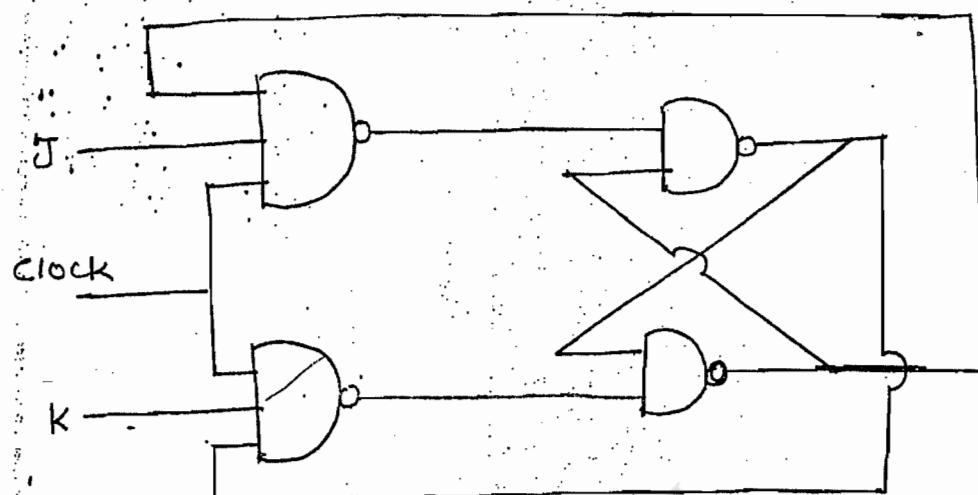
$$S = J\bar{Q}$$

$$R = KQ$$

Clock	J	K	$Q_{n+1}$
0	X	X	$Q_n$
1	0	0	$Q_n$
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

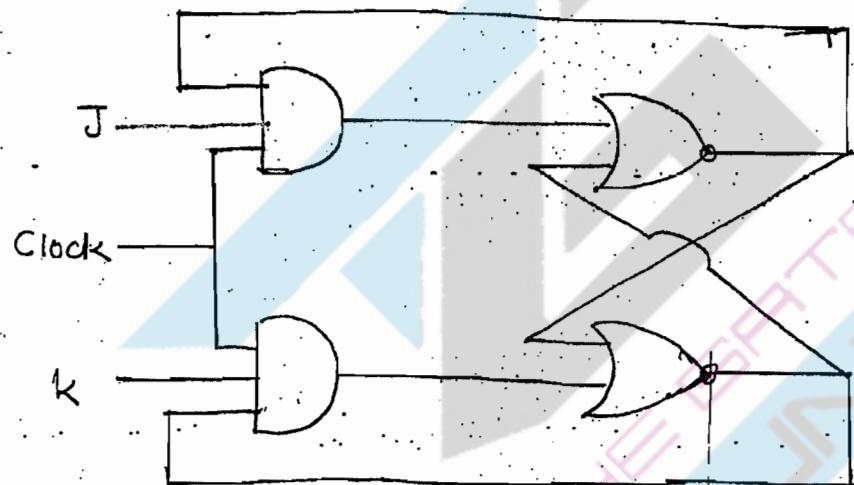
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### JK FF Using NAND Gate:-



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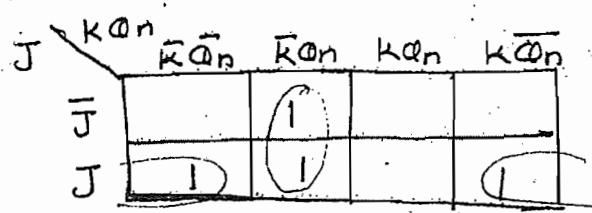
### JK FF Using NOR Gate:-



### Characteristic Table:-

J	K	$Q_n$	$Q_{n+1}$	
0	0	0	0	
0	0	1	1	H
0	1	0	0	R
0	1	1	0	S
1	0	0	1	
1	0	1	1	
1	1	0	1	Toggle.
1	1	1	0	

## Characteristic Equation :-

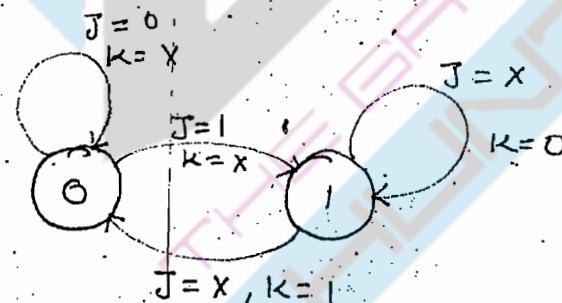


$$Q_{n+1} = \bar{J}Q_n + \bar{K}Q_n$$

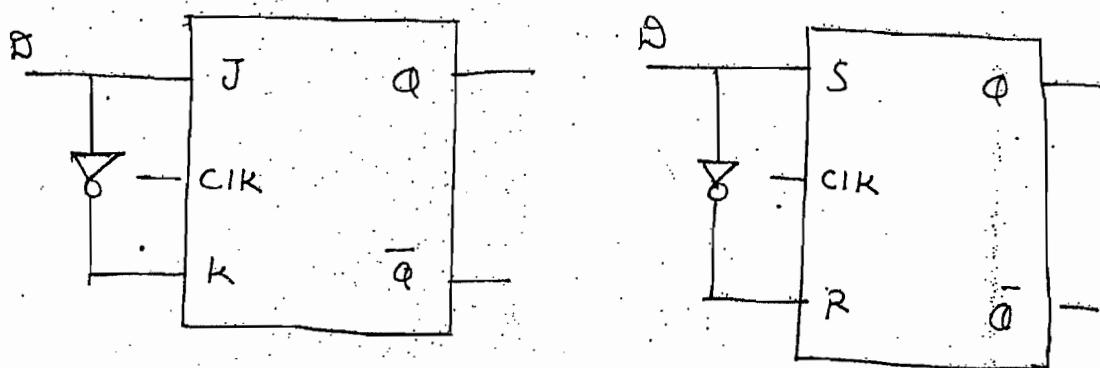
## Excitation Table :-

$Q_n$	$Q_{n+1}$	$J$	$K$
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

## State Diagram :-



## D FF :-



Clock	$\bar{D}$	$Q_{n+1}$
0	X	$Q_n$
1	0	0

$R$	$Q_{n+1}$
0	0
1	1

Characteristic Table :-

$R$	$Q_n$	$Q_{n+1}$
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1} = R$$

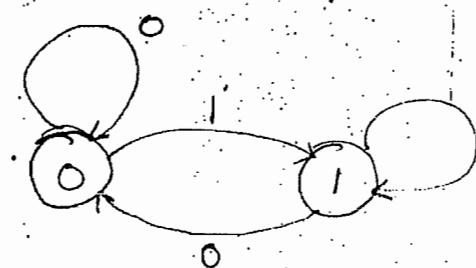
→ Delay FF (or) Data

→ Transparent latch

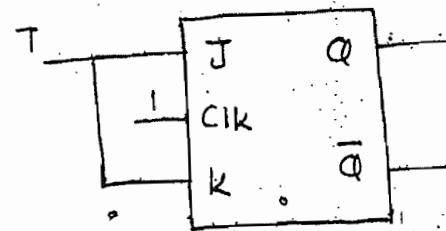
Excitation Table :-

$Q_n$	$a_{n+1}$	$R$
0	0	0
0	1	1
1	0	0
1	1	1

State Diagram :-



T FF! —



$$J = K = T$$

Clock	T	$Q_{n+1}$
0	X	$Q_n$
1	0	$Q_n$
1	1	$\bar{Q}_n$

T	$Q_{n+1}$
0	$Q_n$
1	$\bar{Q}_n$

Characteristic Table! —

T	$Q_n$	$Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

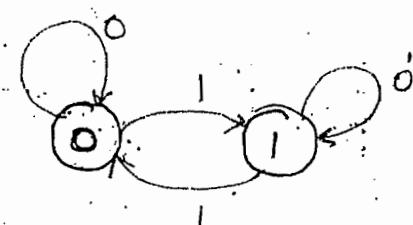
Characteristic Equation! —

$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

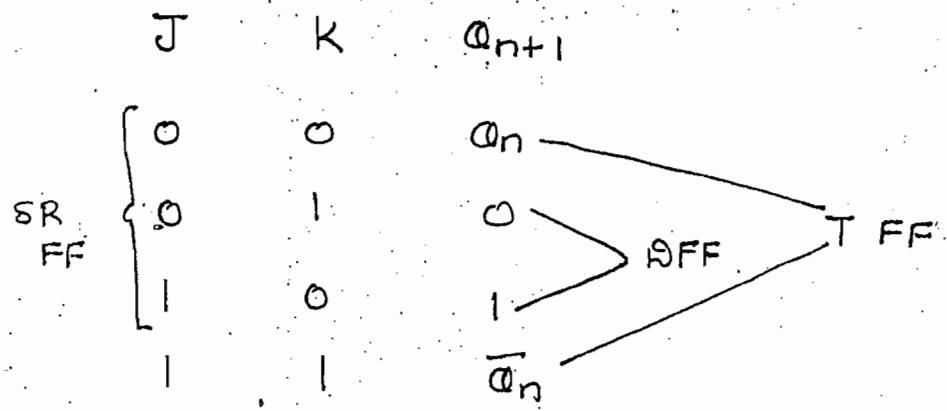
Excitation Table! —

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

State Diagram! —



Note:-



$$Q_{n+1} = S + \bar{R} Q_n$$

$$\therefore Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

$$Q_{n+1} = T$$

$$Q_{n+1} = T \oplus Q_n$$

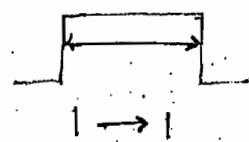
$Q_n$	$Q_{n+1}$	S	R	J	K	P	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

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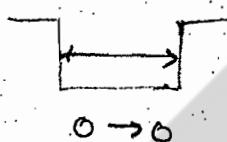
Clock :

Level Trigger

+ve level

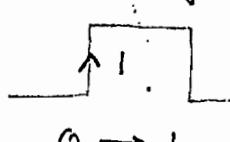


-ve level

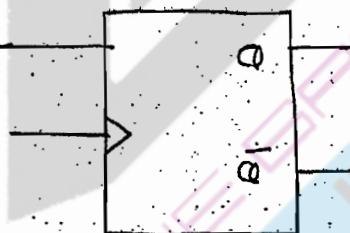
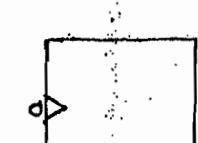
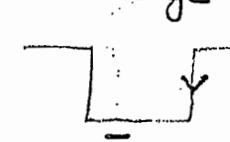


Edge Trigger

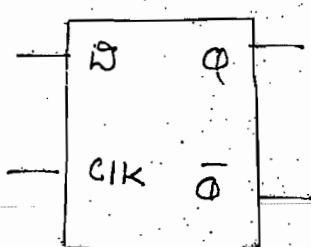
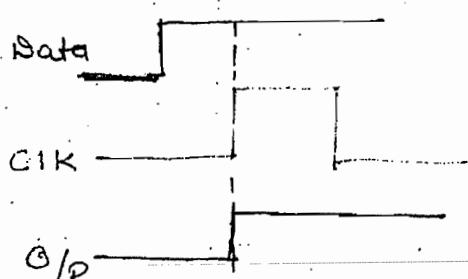
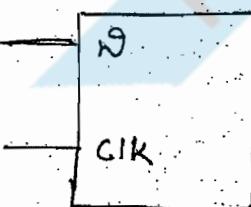
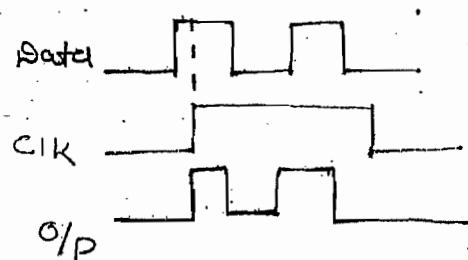
+ve edge



-ve edge

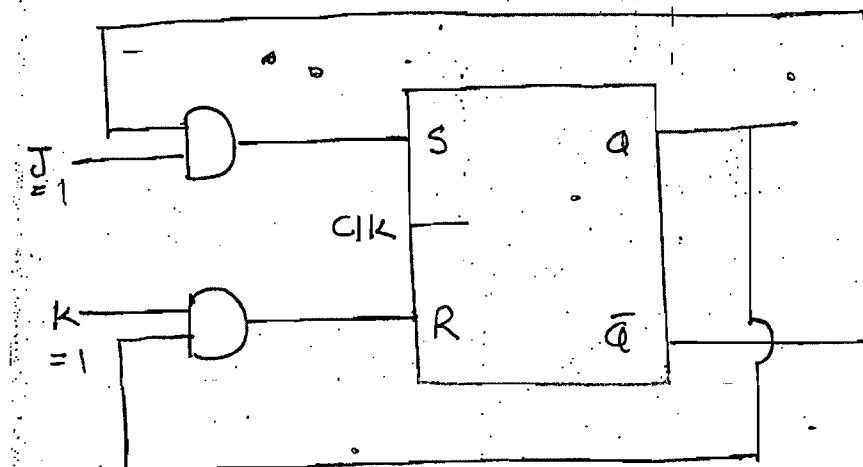


Level Triggering:-

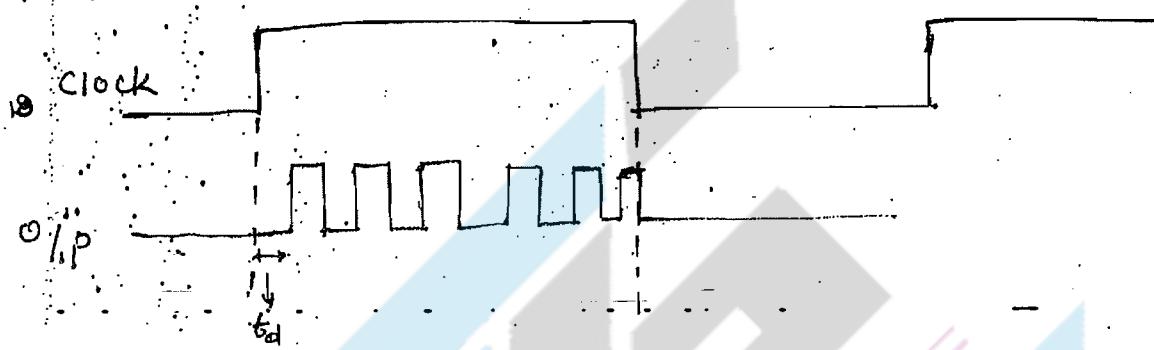


seen by FF

## Race Around Condition :-



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- Disadvantage of JK FF is race-around
- Race around occurs when
  - (i)  $J = K = 1$
  - (ii)  $t_{pd} \text{ FF} < t_{pw}$  (Pulse width delay)
- During race around, O/P will changes many times in single clock

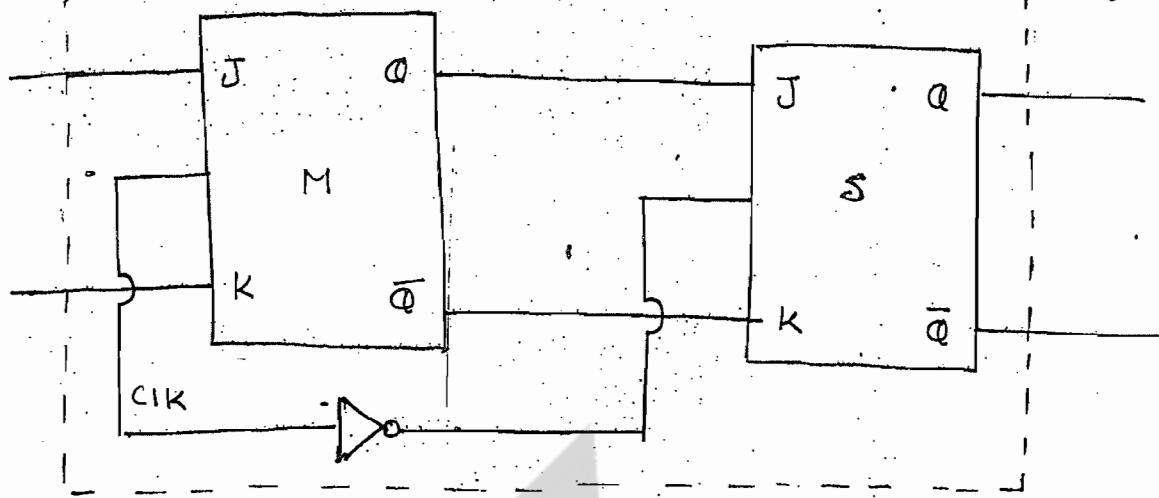
## Condition to avoid Race Around :-

$$t_{pw} < t_{pd \text{ FF}} < T_{CLK}$$



- To avoid race around condition Master-Slave FF is used

## Master Slave FF :-



- In MS FF shown in figure, Master is applied with i/p clock and slave is applied with inverted clock. Due to this Master and slave will not change at a time.
- O/p of MS FF change when slave o/p is changing
- As for operation master is level triggered and slave is edge triggered (if M is +ve level, slave → -ve edge  
M → -ve , slave → +ve edge)
- At the o/p of master & slave there is no race around condition.

## Conversion from one FF to another FF :-

→ Convert JK FF to D FF

Procedure :-

- (I) Construct required FF characteristic table
- (II) Fill available flip flop excitation table
- (III) Write excitation equation
- (IV) Minimize logical exp.
- (V) Implement circuit

$\bar{Q}_n$	$Q_n$	$Q_{n+1}$	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

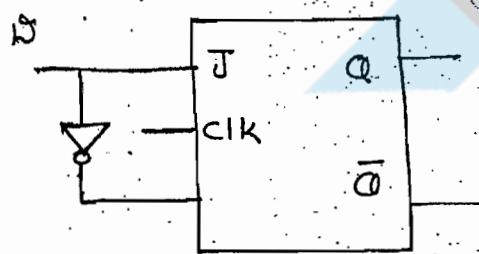
$$J = \sum m(2) + \sum d(1,3)$$

$$K = \sum m(1) + \sum d(0,2)$$

$\bar{Q}_n$	$\bar{Q}_n$	$Q_n$
0	0	X
0	1	X

$$J = \bar{D}$$

$\bar{Q}_n$	$\bar{Q}_n$	$Q_n$
0	0	X
0	1	X



WB (Q35)

$JK \rightarrow AB$  (Conv.)

A	B	$Q_{n+1}$
0	0	$\bar{Q}_n$
0	1	1
1	0	$Q_n$
1	1	0

A	B	$Q_n$	$Q_{n+1}$	J	K
0	0	0	1	1	X
0	0	1	0	X	1
0	1	0	1	1	X
0	1	1	1	X	0
1	0	0	0	0	X
1	0	1	1	X	0
1	1	0	0	0	X
1	1	1	0	X	1

$$J = \sum m(0,2) + \sum d(1,3,5,7)$$

A	$\bar{B}Q_n$	$\bar{B}\bar{Q}_n$	$BQ_n$	$B\bar{Q}_n$	$\bar{B}\bar{Q}_n$
$\bar{A}$	[ ]	X	X	X	
A		X	X	-	

$J = \bar{A}$

$\rightarrow \underline{JK \text{ to } S} :-$

$$J = S$$

$$K = \bar{S}$$

$\rightarrow \underline{JK \text{ to } SR} :-$

$$J \Leftarrow S$$

$$K \Leftarrow R$$

$\rightarrow \underline{SR \text{ to } S} :-$

$$S = A, R = \bar{A}$$

$\rightarrow \underline{S \text{ to } SR} :-$

$$Q_{n+1} = S$$

$$Q_{n+1} = S + \bar{R} Q_n$$

$$D = S + \bar{R} Q$$

$\rightarrow \underline{JK \text{ to } T} :-$

$$J = K = T$$

$\rightarrow \underline{SR \text{ to } JK} :-$

$$S = J\bar{Q}$$

$$R = KQ$$

$\rightarrow \underline{SR \text{ to } T} :-$

$$S = T\bar{Q}, R = TQ$$

$\rightarrow \underline{D \text{ to } JK} :-$

$$D = J\bar{Q} + KQ$$

$\rightarrow \underline{D \text{ to } T} :-$

$$D = T \oplus Q$$

→ T to JK :-

$$T = J\bar{Q} + KQ$$

→ T to SR :-

$$T = S\bar{Q} + RQ$$

→ T to D :-

$$T = D \oplus Q$$

Latch	FF
→ Level trigger	edge trigger
→ Asynchronous	Synchronous

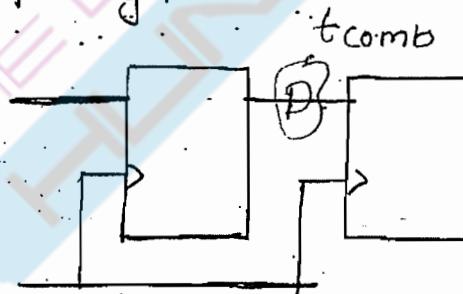
• Setup time :- ( $t_{SU}$ )

→ Min. time required to keep i/p at proper level before applying clock

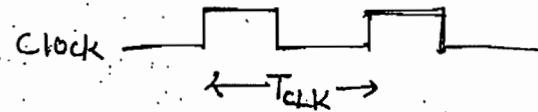
• Hold time :- ( $t_H$ )

→ Min. time to keep same data after applying clock to restore data properly.

$$t_{SU} > t_H$$



$$T_{CLK} \geq t_{pd\ FF} + t_{SU}$$



$$T_{CLK} \geq t_{pd\ FF} + t_{SU} + t_{comb}$$

## Registers:-

## Registers:-

- Registers are used to store group of bits
  - Registers are cascading of FF
  - For n-bits storage, n registers are required
  - Depending on i/p and o/p, registers are of four types

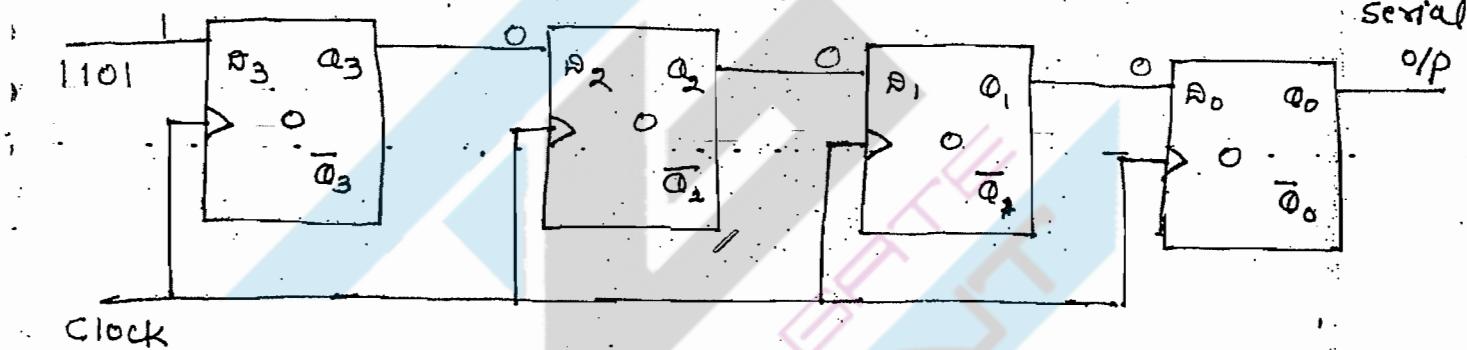
(I) SISO      (II) SIPO      (III) PISO      (IV) PIPO

→ In registers, FFF is used

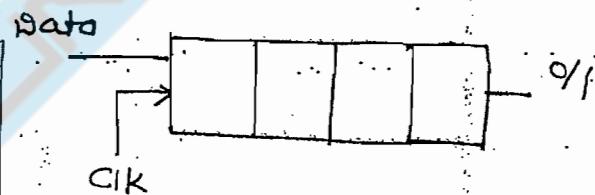
→ In shift registers - JK FF  
- S FF

SISO 1—

1. Serial in



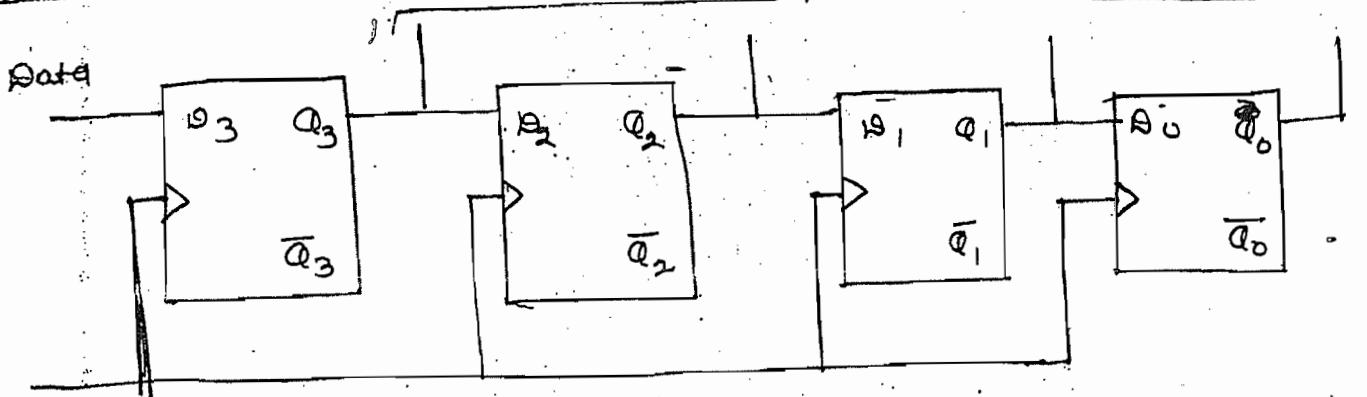
Clock	Data	$Q_3\ Q_2\ Q_1\ Q_0$
0	1101	0 0 0 0
1		1 0 0 0
2		0 1 0 0
3		1 0 1 0
4		1 1 0 1



- In n-bit SISO register to store n-bit data serial, minimum n-clock pulse are used.
  - SISO register is used to provide delay to the i/p data.
  - In n-bit SISO register, it provides  $n \times T_{CLK}$  delay to the i/p data.
  - In n-bit SISO register to provide serial out min  $(n-1)$  clock pulses are used.

SIPO :-

Parallel o/p



→ In SIPO registers, to provide serial i/p, min. n clock pulses are required.

→ To provide parallel out data, no clock pulse is required

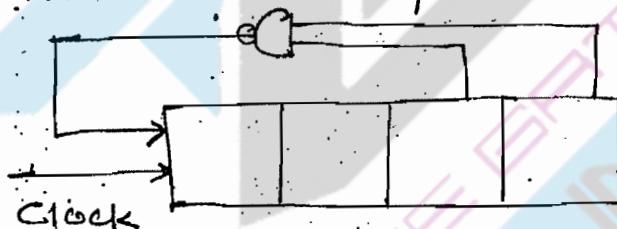
serial  $\rightarrow$  temporal code

Parallel  $\rightarrow$  Spacial code

→ Convert temporal code into spacial code

Ques:-

The circuit shown in figure 1 is SIPO register loaded with 1010. After 3-clock pulse data present is



Ans:-

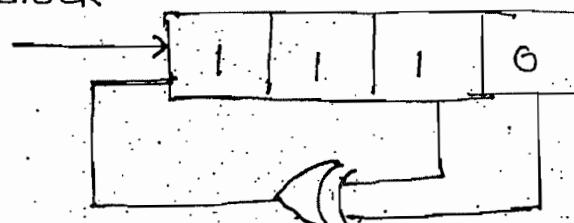
Clock

0	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1

Ques:- After 3-clock pulse data present in register

is

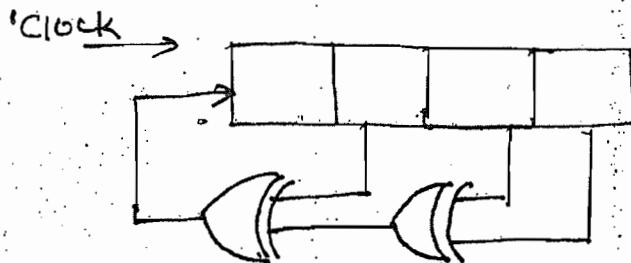
CLOCK



Ans:-

0 0 1 1

Ques:- 4-bit SIPO loaded with 1011 : If clock pulse are applied continuously then after how many clock pulses - data will become 1011 again

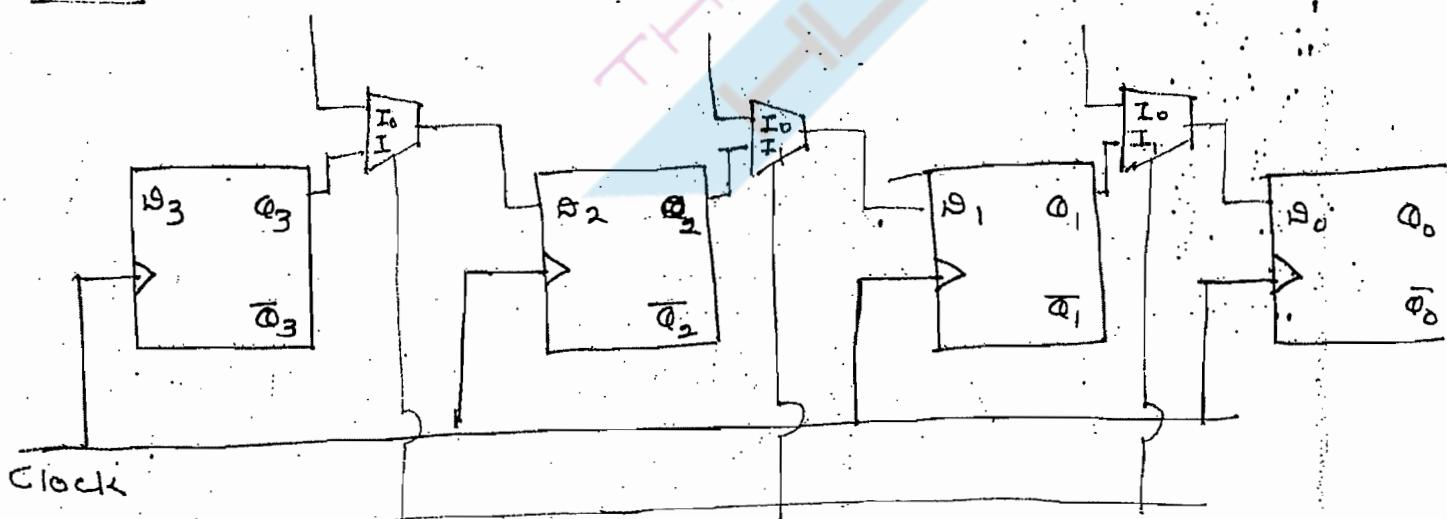


Soln:-

Clock	Data
0	1 0 1 1
1	0 1 0 1
2	0 0 1 0
3	1 0 0 1
4	1 1 0 0
5	1 1 1 0
6	0 1 1 1
7	1 0 1 1

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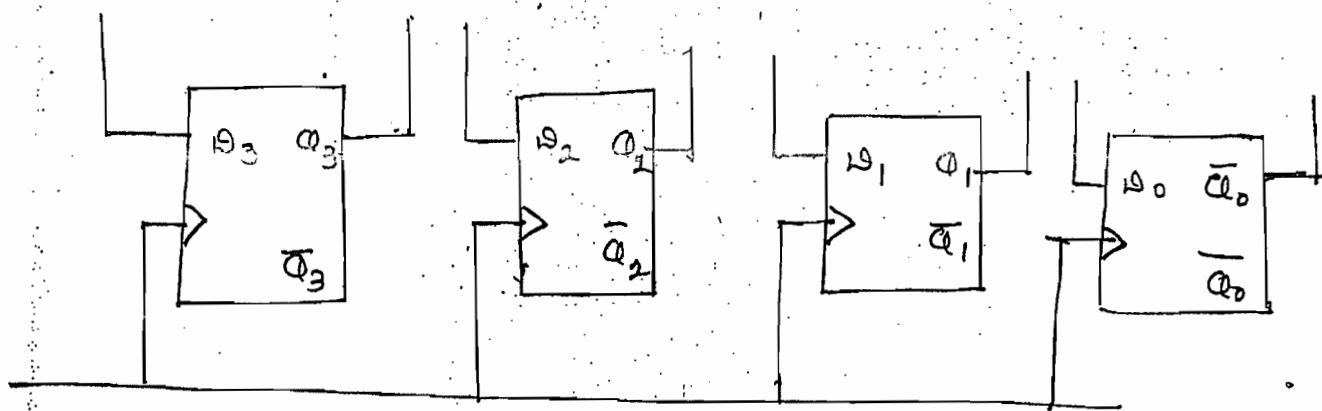
PISO :-



- control = 0 , parallel in
- control 1 → serial o/p
- PI ( $\frac{1}{2} \text{ clock}$ ) →  $\frac{1}{2} \text{ serial o/p} = n-1$

→ convert spatial code into temporal code.

PIPO:-



Note:-

S.T.SO	I/P	O/P
SIPO	n	n-1
PISO	n	0
PIPO	1	n-1

→ PIPO is fastest

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BCD Code :-

- 4 bit code
- Each decimal digit is represented with 4 bit binary form
- Weighted code
- 8421 code
- In 4-bit BCD code there are 6 invalid BCD code  
i.e. 1010, 1011, 1100, 1101, 1110, 1111

Note:-

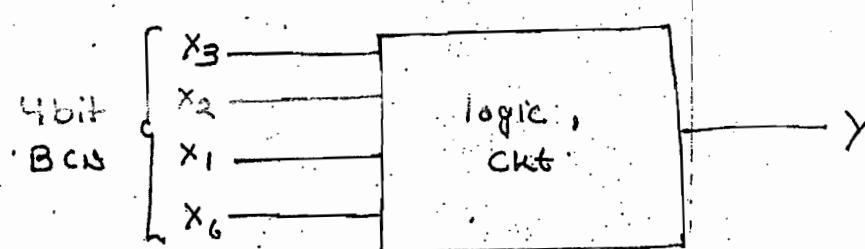
- In logic circuit design, consider invalid BCD code as don't care
- During addition if invalid BCD code is present then add 0110 to get correct result

<u>Decimal</u>	<u>BCD Code</u>	<u>Excess 3 Code</u>	<u>2421</u>
0	0 0 0 0	0 0 1 1	0 0 0 0
1	0 0 0 1	0 1 0 0	0 0 0 1
2	0 0 1 0	0 1 0 1	0 0 1 0
3	0 0 1 1	0 1 1 0	0 0 1 1
4	0 1 0 0	0 1 1 1	0 1 0 0
5	0 1 0 1	1 0 0 0	1 0 1 1
6	0 1 1 0	1 0 0 1	1 1 0 0
7	0 1 1 1	1 0 1 0	1 1 0 1
8	1 0 0 0	1 0 1 1	1 1 1 0
9	1 0 0 1	1 1 0 0	1 1 1 1

Compliment

Ques - The circuit shown in figure is a 4-bit logic circuit which has I/P as BCD code and O/P Y.

Y is logic '1' when I/P BCD is divisible by 3 then minimised expression for O/P Y



Soln:-

Decimal	BCD Code	Y
0	0 0 0 0	1
1	0 0 0 1	0
2	0 0 1 0	0
3	0 0 1 1	1
4	0 1 0 0	0
5	0 1 0 1	0
6	0 1 1 0	1
7	0 1 1 1	0
8	1 0 0 0	0
9	1 0 0 1	1

$x_3x_2$	$x_1x_0$	1	U	1
X	$\bar{x}$	$\bar{x}$	X	1
X	$\bar{x}$	$\bar{x}$	X	X
1	X	X	X	X

$$= x_3x_0 + \bar{x}_2x_1x_0 + x_2\bar{x}_1x_0 + \\ \bar{x}_3\bar{x}_2\bar{x}_1x_0$$

Note:-

For 8-bit BCD code

$$\text{Valid: } 00 \text{ to } 99 = 100$$

$$\text{Invalid: } 256 - 100 = 156$$

### Excess 3 code :-

- BCD code + 0011
- Excess 3 BCD code
- Unweighted code
- Self Complimentary code

### Note :-

$$9 = 2+4+2+1 \rightarrow 2\ 4\ 2\ 1$$

$$9 = 3+3+2+1 \rightarrow 3\ 3\ 2\ 1$$

Self Compliment

$$9 = 5+2+1+1 \rightarrow 5\ 2\ 1\ 1$$

Weighted

( If sum of digit  
comes q )

→ ASCII → 7 bit code

→ EBCDIC → 8 bit (data transmission) (Punching code)

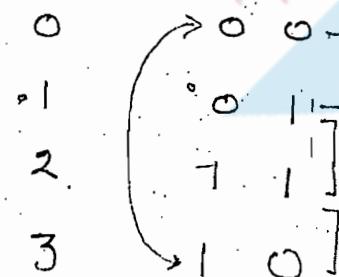
→ Hollerath → 12 bit

### Gray Code :-

→ In this, successive no. will differ by only 1 bit

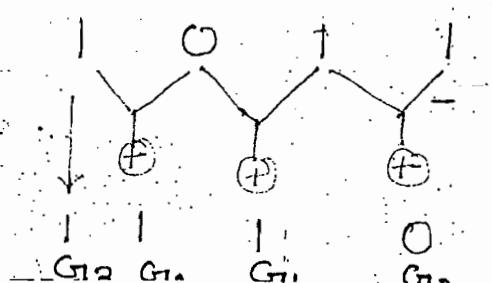
→ Also known as Unit distance code (UDC)

→ Reflective code or cyclic code

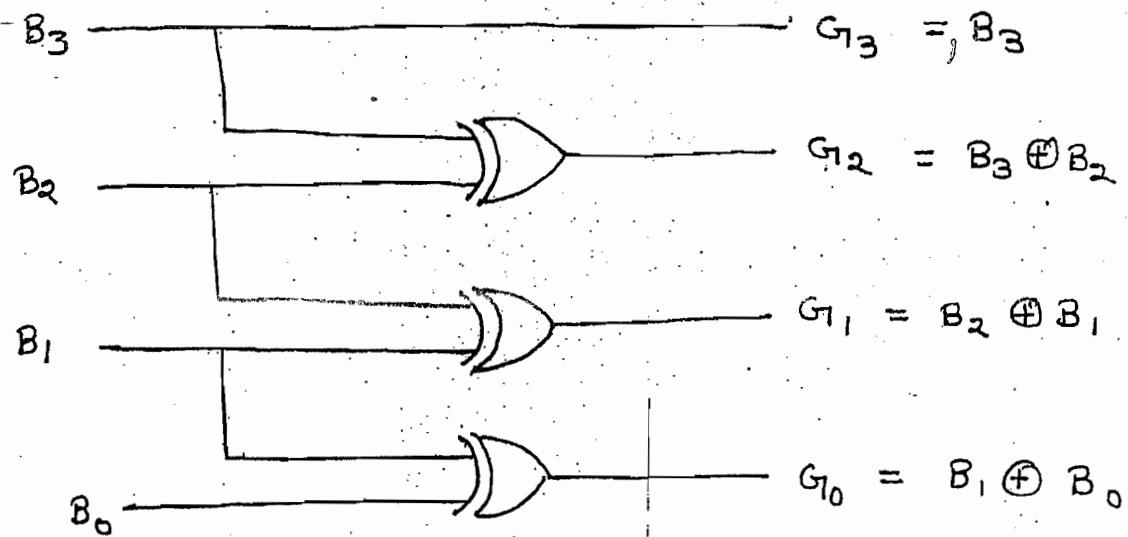


→ Minimum error code

→ Unweighted code

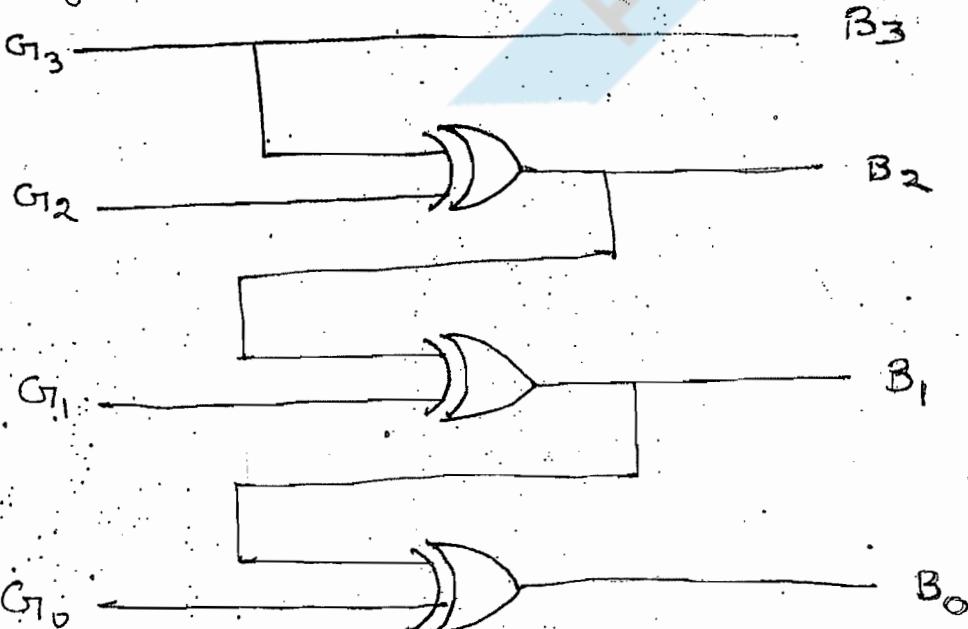
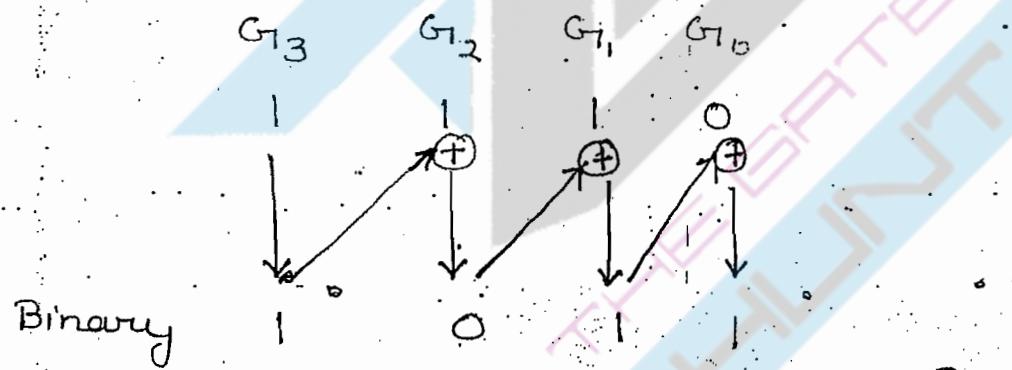


→ Binary  
(Binary to Gray)



Gray to Binary :-

$$\begin{array}{c}
 B_3 \longrightarrow B_3 \\
 B_3 \oplus B_2 \longrightarrow B_2 = B_3 \\
 B_2 \oplus B_1 \longrightarrow B_1 = B_2 \oplus G_{11} \\
 G_{10} = B_1 \oplus B_0 \longrightarrow B_0 = B_1 \oplus G_{10}
 \end{array}$$



## COUNTERS

### Counters:-

→ Counters can be used

- (I) To count no. of clock pulses
- (II) Frequency dividers
- (III) Timers
- (IV) To generate waveforms
- (V) To provide frequency measurements
- (VI) Pulse width measurements

→ In counters with  $n$  FF's max. possible states are

$$2^n$$

$n \rightarrow$  no. of FF

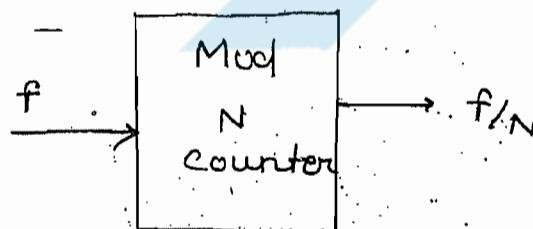
$N \rightarrow$  No. of states

$$N \leq 2^n$$

$$n \geq \log_2 N$$

→ No. of states used in counter is called as moduli count Mod. no.

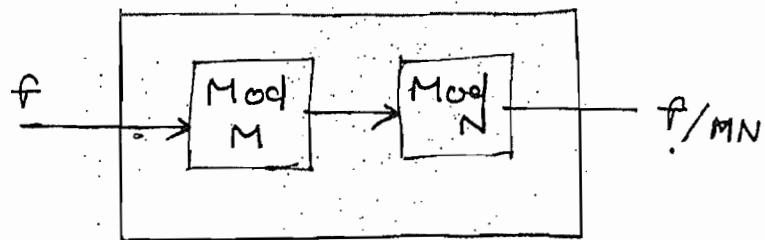
Mod 10 → Decade counter



Ques:- A decade counter is applied with clock frequency of 10 MHz then o/p of frequency is .

Ans:- 1 MHz.

→ If mod M and mod N counters are cascaded then it will acts as Mod MN counters.



Ques:- Mod 3, Mod 4 and Mod 5 counters are cascaded then no. of states are -

Soln:- No. of states =  $3 \times 4 \times 5 = 60$  states

→ Depending clock pulse applied counter are of two types

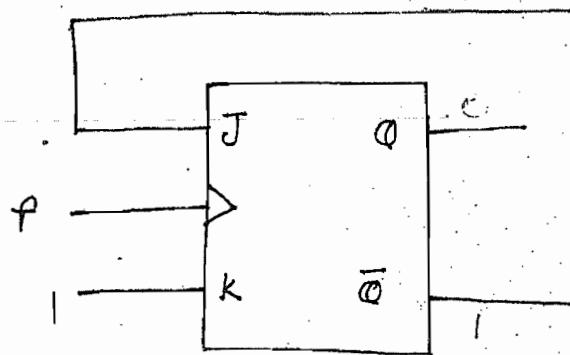
(i) Synchronous counter

(ii) Asynchronous counter

Clock

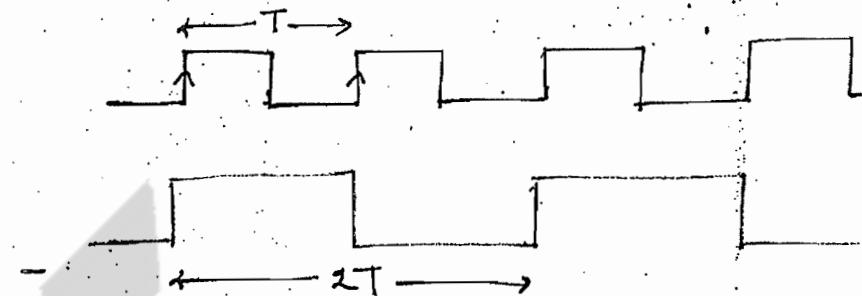
	Synchronous counter	Asynchronous counter
1.	All FF's are applied with same clock	Different FF's are applied with applied different clock
2.	Faster	Slower
3.	Any count sequence can be design	Fixed count sequence is possible i.e. Up & Down
4.	No decoding errors	Decoding errors will be present
5.	e.g:- Ring counter, Johnson counter	e.g:- Ripple counter

Ques:-



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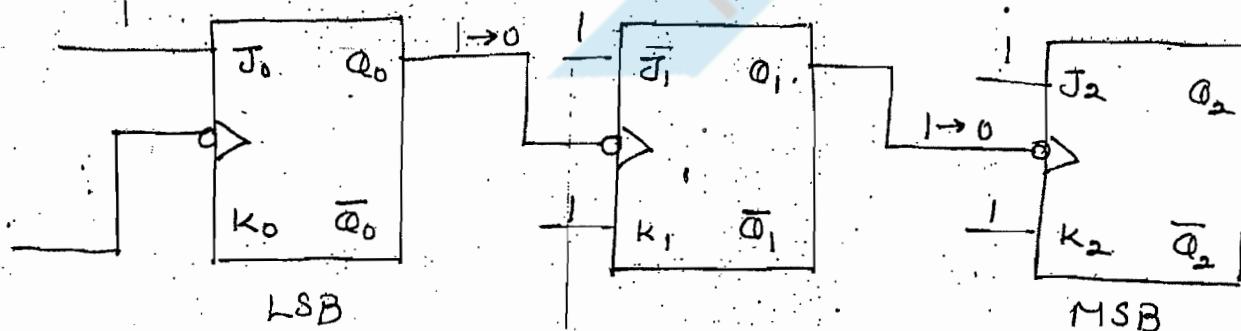
Clock	Q
0	0
1	1
2	0
3	1
4	0
5	1



### Ripple Counter :-

- Asynchronous counter
- Different flip flops are applied with different clock pulse
- Toggle Mode

### 3-Bit Ripple Counter :-



- In ripple counter shown in figure,  $Q_0$  toggles for every clock pulse -ve edge.
- $Q_1$  toggles,  $Q_0$  changes from  $1 \rightarrow 0$ .
- $Q_2$  toggles,  $Q_1$  changes from  $1 \rightarrow 0$ .
- $Q_0$  toggles for every clock pulse -ve edge.

### Truth Table:-

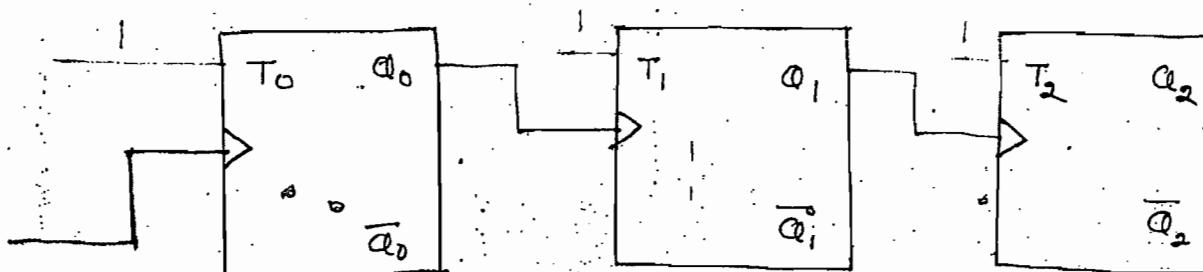
Clock	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

→ Mod 8 ripple up counter (above).

### Note:-

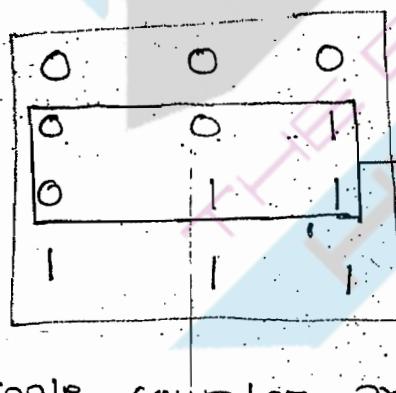
- (I) -ve edge trigger - Q as clock → Upcounter
- (II) +ve edge trigger -  $\bar{Q}$  as clock → Upcounter
- (III) +ve edge trigger - Q as clock → downcounter
- (IV) -ve edge trigger -  $\bar{Q}$  as clock → downcounter

### 3 Bit Ripple Down counter (Mod 8 ripple down counter):-



## Truth Table :-

Clock	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0



→ unwanted state  
transition state  
(due to propagation delay)  
↓  
Decoding error

In n-bit ripple counter propagation delay of each  
ff is  $t_{pd\text{ FF}}$  then  $T_{CLK} \geq n t_{pd\text{ FF}}$

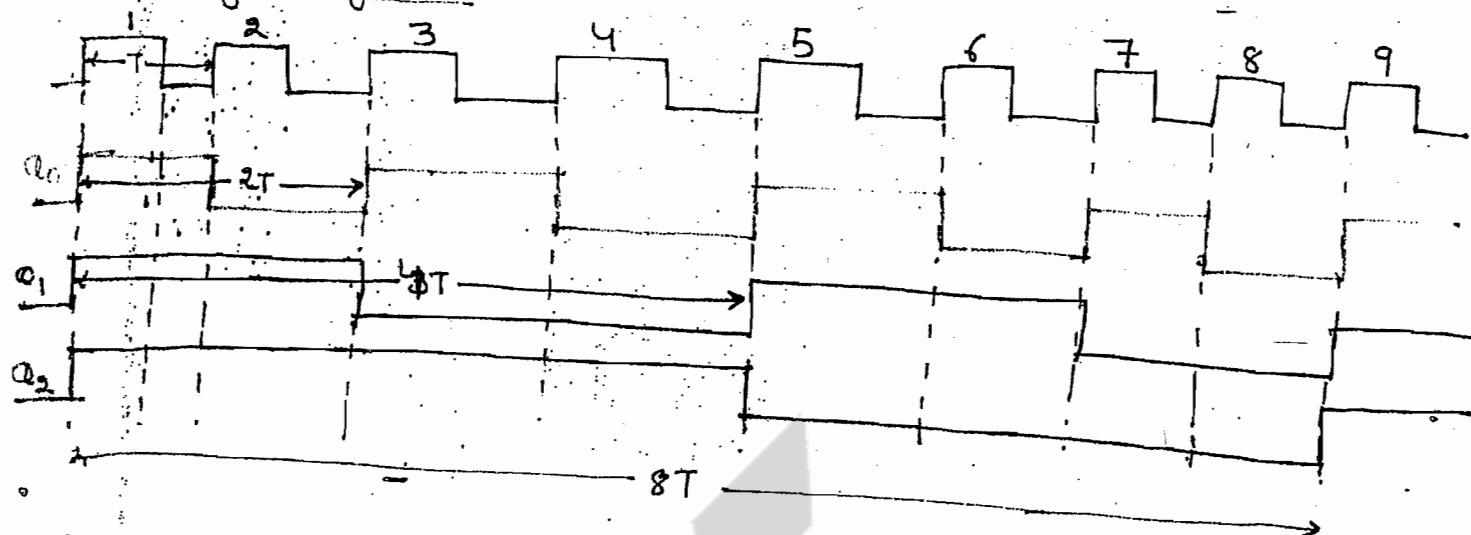
$$f_{CLK} \leq \frac{1}{n t_{pd\text{ FF}}}$$

$$f_{max} = \frac{1}{n t_{pd\text{ FF}}}$$

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→ Decoding error is present in ripple counter. It can be avoided by using strobe/control.

Timing diagram:-

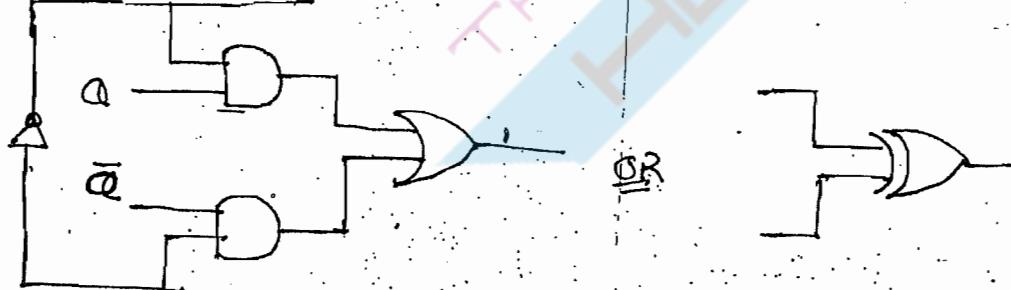


Note:-

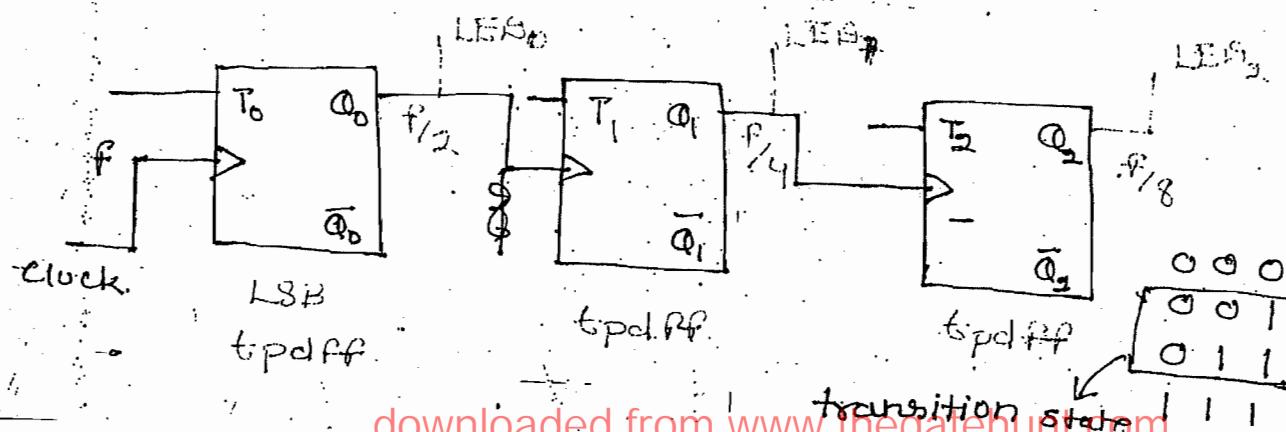
13 Bit Ripple up-down counter using the edge triggering

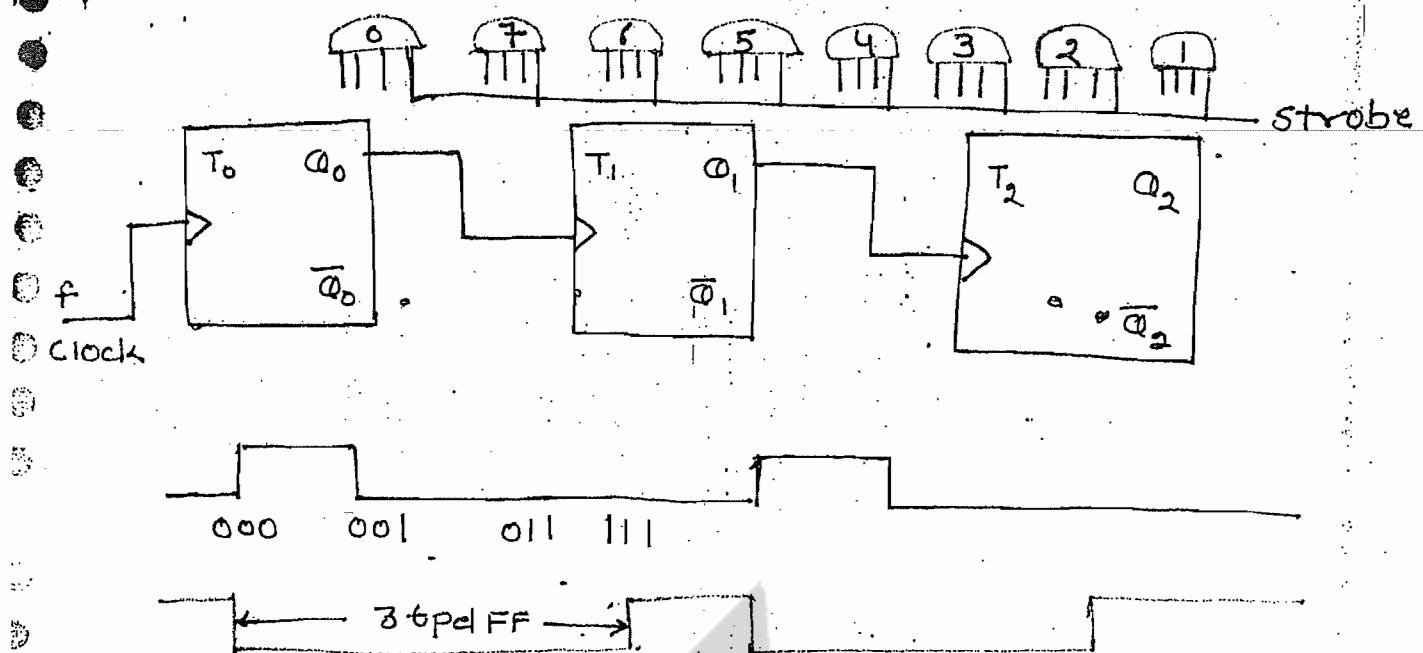


Control = 0 → Down counter      Control = 1 → Upcounter



Decoding in 3-Bit Ripple down counter:-



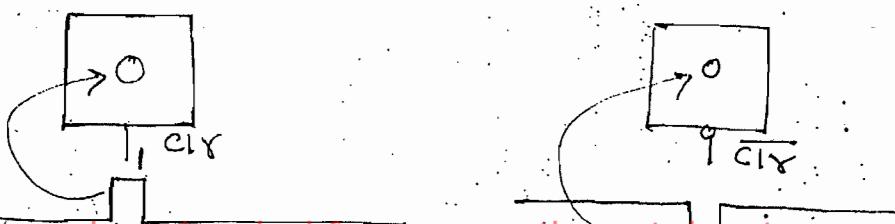
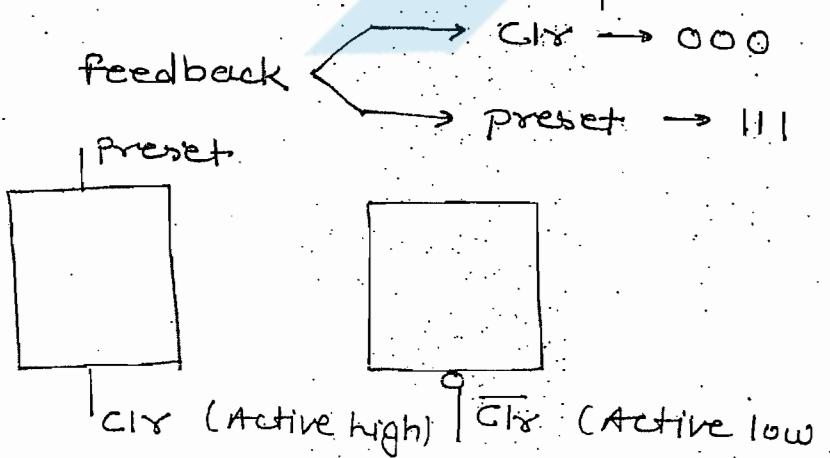


$$T_{CLK} \geq n \cdot t_{pd\text{FF}} + T_S$$

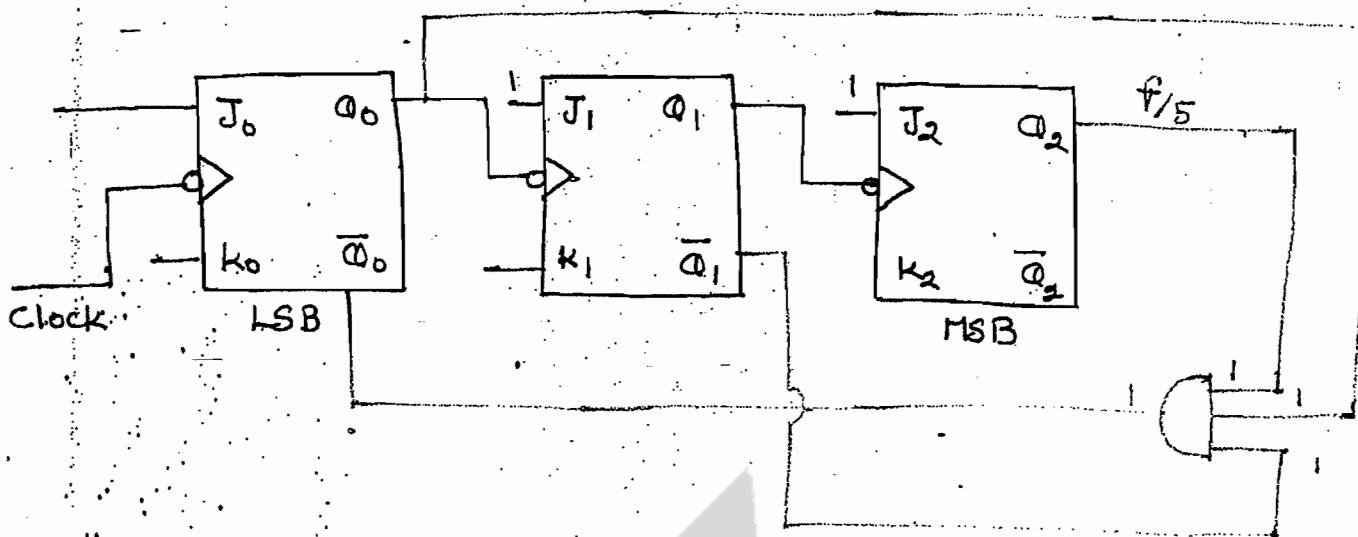
$$f_{CLK} \leq \frac{1}{n \cdot t_{pd\text{FF}} + T_S}$$

$$f_{max} = \frac{1}{n \cdot t_{pd\text{FF}} + T_S}$$

→ In counter to reduce no. of states or to eliminate some of the states feedback is applied in the count through clear or Reset the i/p



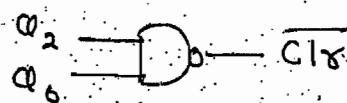
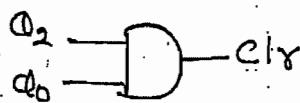
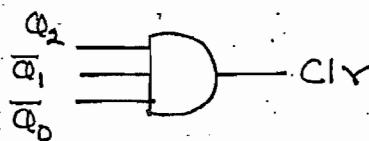
## Mod 5 Ripple Counter :-



Clock	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

→ If the edge trigger then it is MOD 3  
↳ Ripple down counter

→ In Ripple counter  
Max. possible states =  $2^n$



→ Types of Ripple Counter :-

(i) Trigger → the edge  
- re edge

(iii) Clock  $\rightarrow Q$   
 $\rightarrow \bar{Q}$

(ii) Clock  $\rightarrow Q$   
 $\rightarrow \bar{Q}$

(iii) Counter  $\rightarrow$  up  
 $\rightarrow$  down  
(iv) feedback  $\rightarrow$  CLR (000)  
 $\rightarrow$  Preset (111)

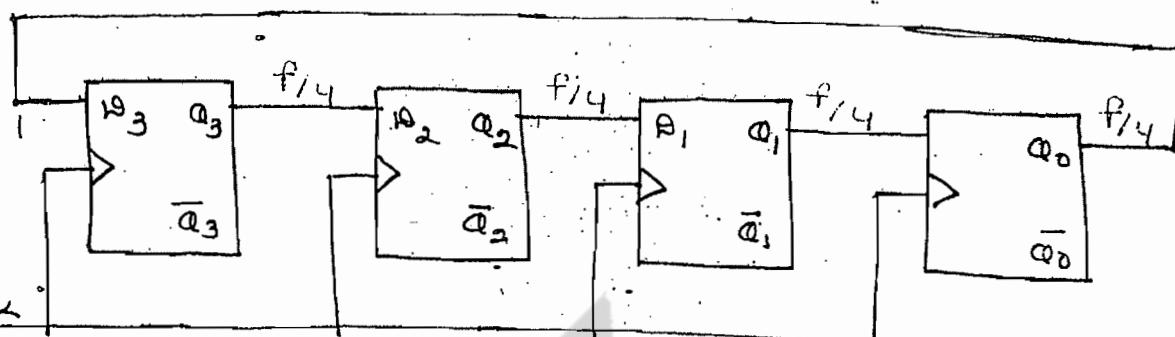
(v) Terminating logic/count  
→ CLR - 000  
→ Preset - 111

● Synchronous counter:-

● Ring Counter:-

● → Synchronous counter

● → Shift register with feedback



→ In ring counter only one FF o/p. is logic '1' and it will rotates among all FF's with clock.

Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1
9	1	0	0	0

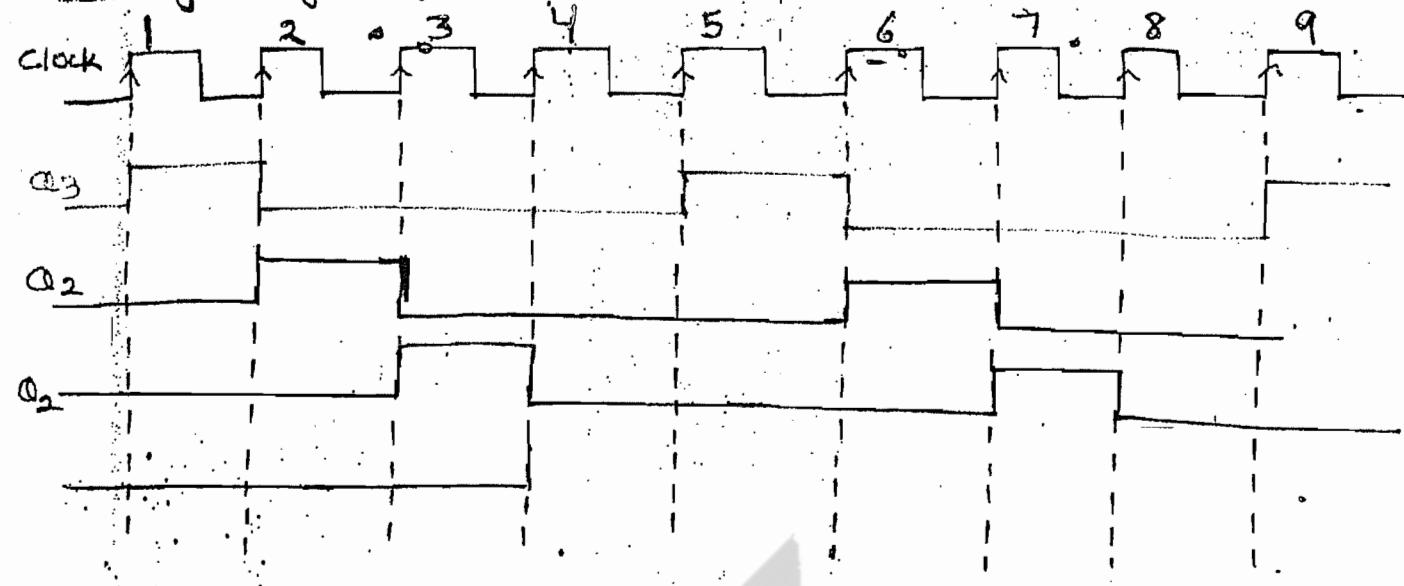
→ In ring counter

No. of states =  $n$

No. of unused states =  $2^n - n$

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## Timing Diagram :-



- In n-bit ring counter output frequency at any ff is  $f = \frac{f}{n}$
- In ring counter time period of clock

$$T_{CLK} \geq t_{pd\ FF} + t_{su}$$

$$f_{CLK} \leq \frac{1}{t_{pd\ FF} + t_{su}}$$

- Ring counter is fastest among all
- Ring counter will generate phase shift of  $\frac{360}{n}$

## Application:-

- Stepper Motor control
- SAR
- Waveform generators

## Decoding:-

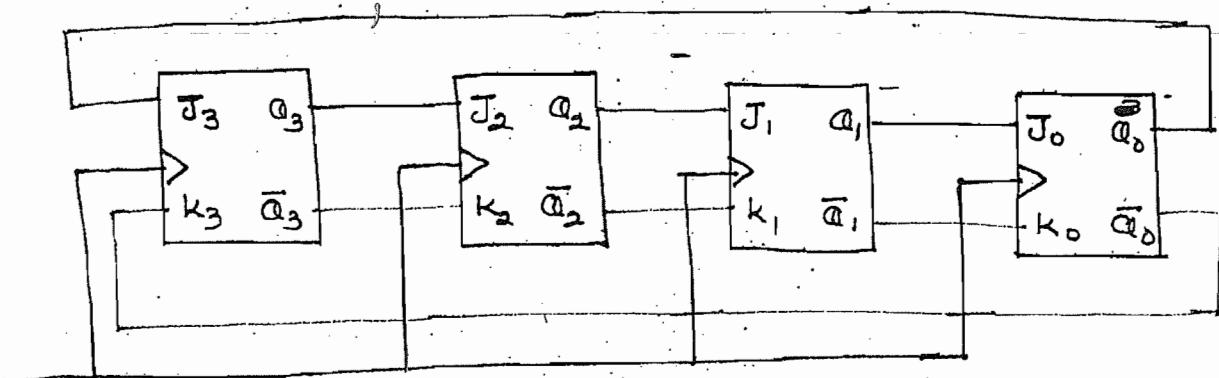
- Main advantage of Ring counter is decoding logic is very simple and no hardware is used

$Q_3 \quad Q_2 \quad Q_1 \quad Q_0$       Decoding  
 1 0 0 0 -  $Q_3$   
 0 1 0 0 -  $Q_2$

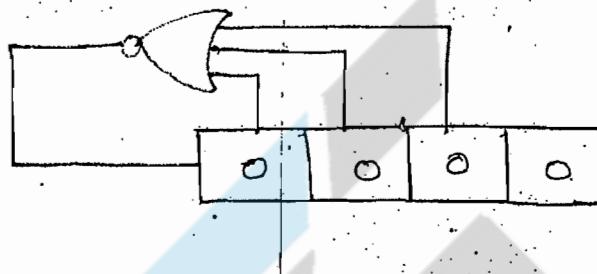
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## Ring Counter Using JK FF

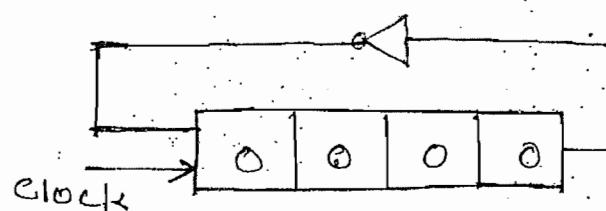
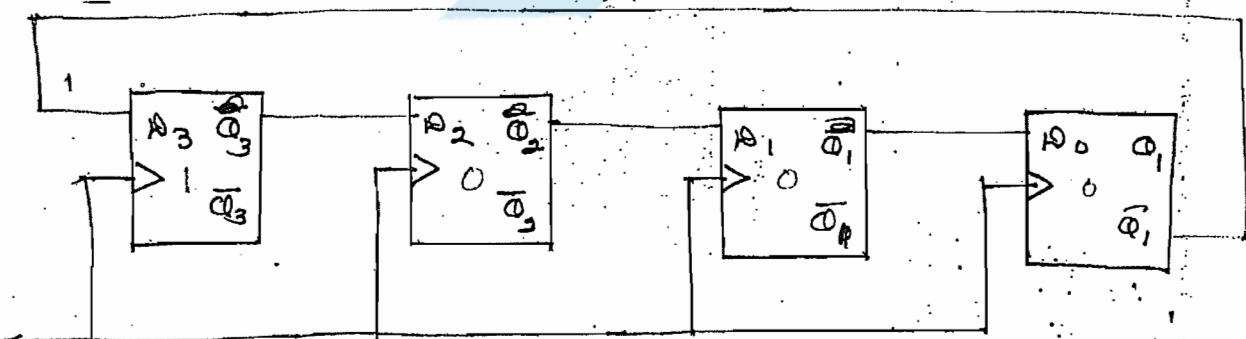
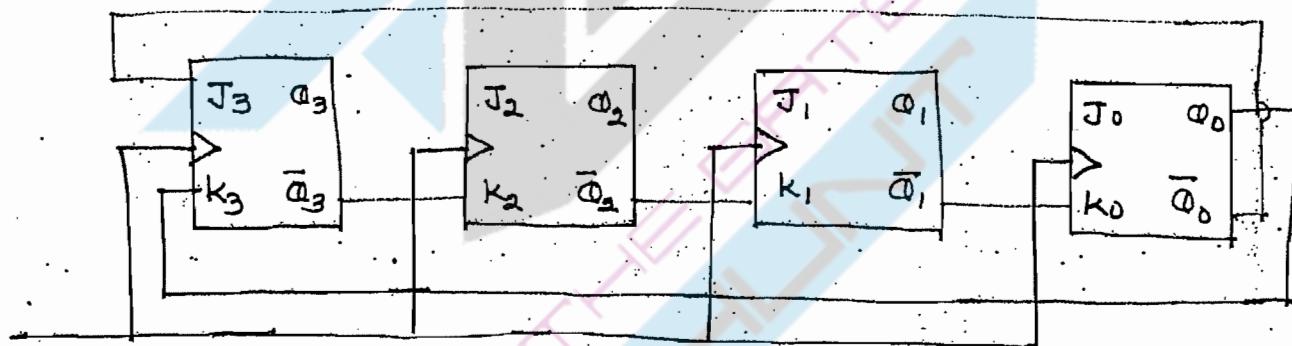


## Self starting Ring Counter



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## Johnson Counter



Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0
10	1	1	0	0

- No. of states used =  $2^n$
- No. of unused states =  $(2^n - 2^n)$
- If Johnson counter is operated in used state then O/P frequency at any flip flop is  $\frac{f}{2^n}$
- Disadvantage:-
- Lockout may occur when counter is operated in unused state

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$$T_{CLK} \geq t_{pdFF} + t_{su}$$

Decoding:-

Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$	Decoding
0	0	0	0	0	$\overline{Q}_3 \overline{Q}_0$
1	1	0	0	0	$\overline{Q}_3 \overline{Q}_2$

Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$	Decoding
0	0	0	0	0	$\bar{Q}_3 \bar{Q}_0$
1	1	0	0	0	$Q_3 \bar{Q}_2$
2	1	1	0	0	$Q_2 \bar{Q}_1$
3	1	1	1	0	$Q_1 \bar{Q}_0$
4	1	1	1	1	$Q_3 Q_0$
5	0	1	1	1	$\bar{Q}_3 Q_2$
6	0	0	1	1	$\bar{Q}_2 Q_4$
7	0	0	0	1	$\bar{Q}_1 Q_0$

→ To decode Johnson counter one 2 i/p AND gate or NOR gate is used for each state.

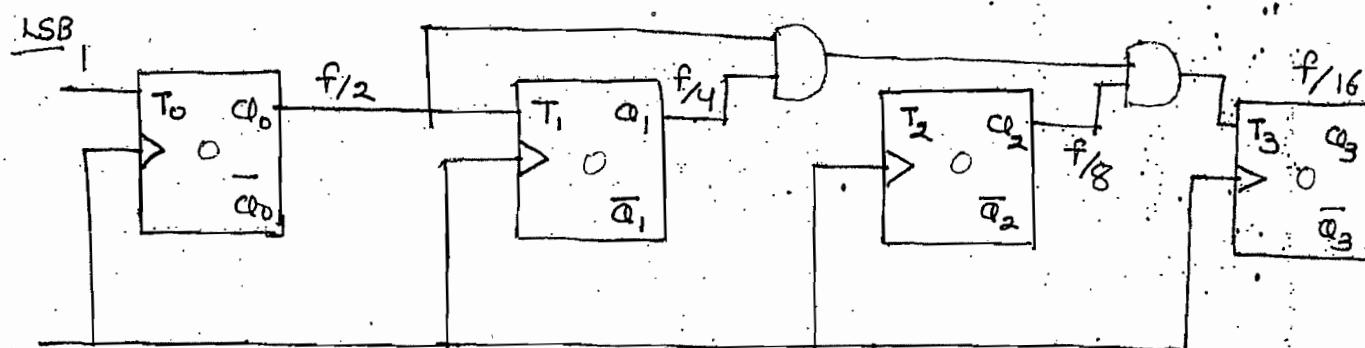
→ Johnson counter is also known as

- (I) Twisted Ring counter
- (II) switch tail counter
- (III) Walking counter
- (IV) creeping counter
- (V) Mobien counter

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#### Synchronous Series Counting Counter :-

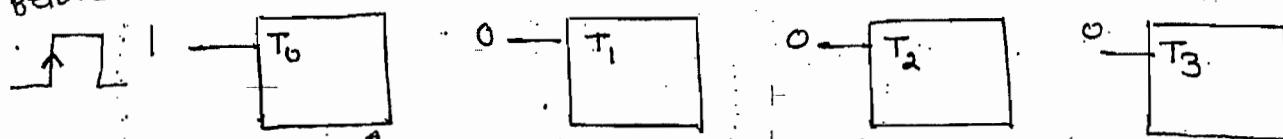


→ The circuit shown in figure is synchronous series counting upcounter.

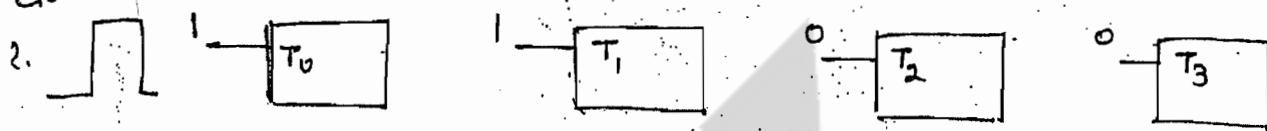
→ If  $\bar{Q}$  is connected then it is down counter.

- $Q_0$  toggles for every clock pulse the edge of clock
- $Q_1$  toggles when  $Q_0 = 1$  and the edge of clock
- $Q_2$  toggles when  $Q_1 \times Q_0 = 1$  and the edge of clock
- $Q_3$  toggles when  $Q_2 Q_1 Q_0 = 1$  and -ve edge of clock

before



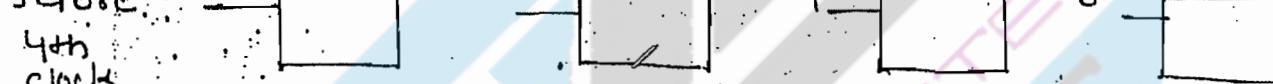
before



before



before



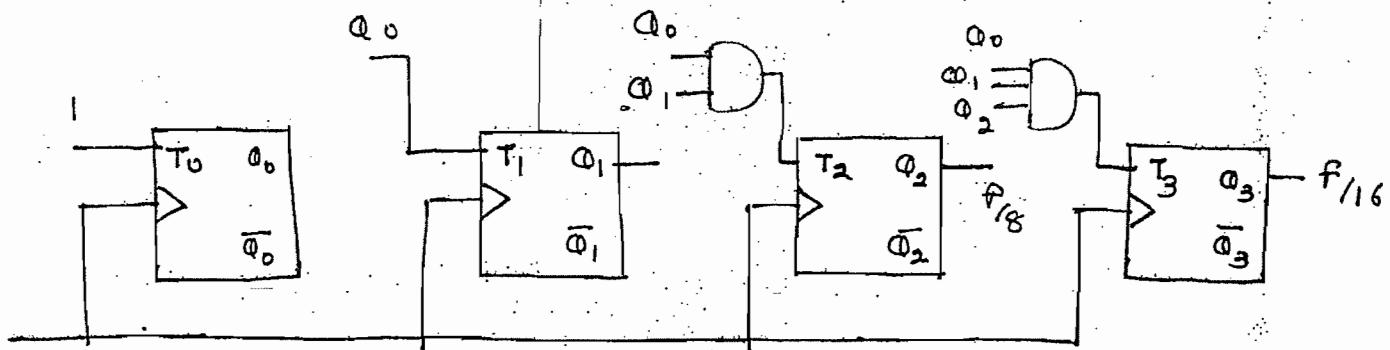
before  
4th clock

Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
...	...	...	...	...
15	1	1	1	1
16	0	0	0	0

Time period,

$$T_{CLK} \geq t_{pdFF} + (n-2)t_{pdAND} + t_{SU}$$

Synchronous Parallel carry counter :-



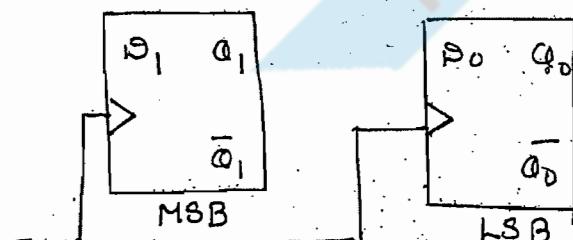
$$T_{CLK} > t_{pdFF} + t_{pdAND} + t_{SU}$$

Synchronous Counter Design :-

Design a synchronous counter with count sequence

$$\dots 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$$

- Identify no. of states and no. of FF
- construct state Table
- Write Excitation equation
- Minimize
- Implement



State Table :-

Present State		Next State		Excitation
Q1	Q0	Q1+	Q0+	Q1 . Q0
0	0	1	0	1 0
1	0	0	1	0 1
0	1	1	1	1 1
1	1	0	0	0 0

$$B_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1$$

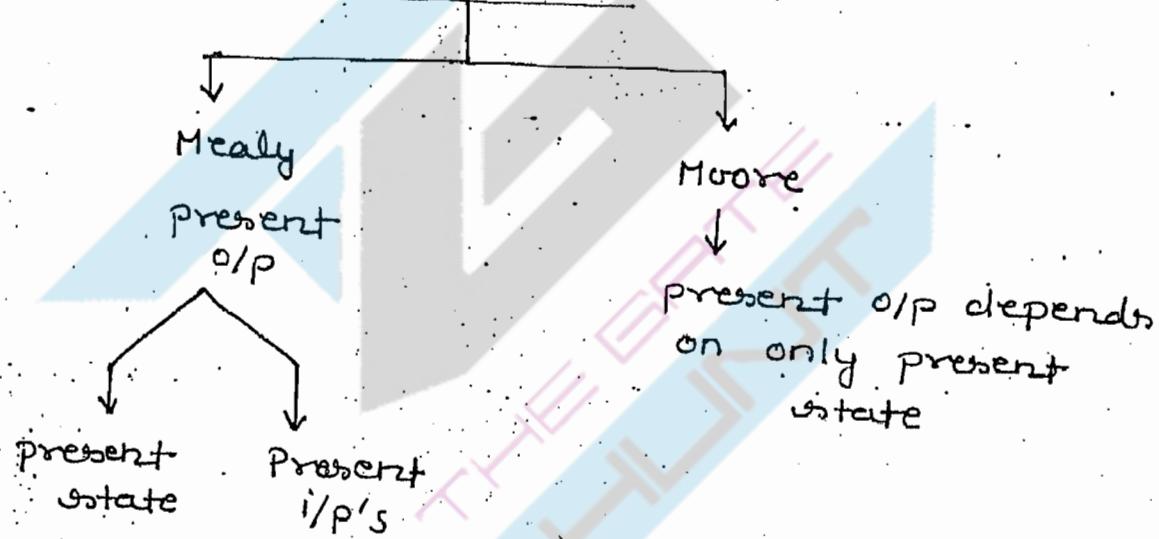
$$B_0 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 = Q_1 \oplus Q_0$$

Clock	$Q_1$	$Q_0$
0	0	0
1	1	0

Note:-

- In counter design, consider unused states as don't care.
- To design lock out avoiding counter, consider unused state corresponding next state, one of the used state

### State Machines



- According to Moore's law, transistor density will be double in every 18 months.

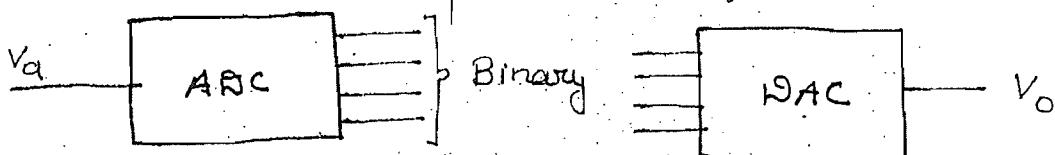
Ques! - In a 4-bit ripple counter propagation delay of each flip flop is 10 nsec then maximum clock frequency that can be applied to the counter is?

Soln:-

$$f_{\max} = \frac{1}{n t_{pd}} = \frac{1}{4 \times 10 \times 10^{-9}} = \frac{10^8}{4} = 25 \text{ MHz}$$

Ans

## A/D / D/A



- (I) Counter type
- (II) SAR type
- (III) Flash type
- (IV) Dual slope

- (I) Weighted Resistor
- (II) R-2R ladder

### DAC :-

- (I) Resolution
- (II) Analog o/p Voltage
- (III)  $V_{FS}$
- (IV) % Resolution
- (V) Error/ Accuracy

#### (I) Resolution :-

→ change in analog voltage corresponding 1 LSB bit increment at the i/p

$$\text{Resolution} = \frac{V_R}{2^n - 1}$$

where  $n$  = no. of bits

$V_R$  = reference voltage corresponding to logic '1' i/p

#### (II) Analog o/p Voltage :-

$$V_o = \text{Resolution} \times \text{Decimal}$$

Ques:- In a 4-bit DAC ref voltage is 10V. If binary data 1001 is applied then analog o/p voltage is

80%:-

$$\begin{aligned}
 V_o &= \frac{10}{2^4 - 1} \times 9 \\
 &= \frac{10}{15} \times 9 = 6V
 \end{aligned}$$

(III)  $V_{FS}$  :- (Full scale o/p voltage)

$$\begin{aligned}V_{FS} &= \text{Max. analog o/p voltage} \\&= R \times \text{max } \theta \\&= \frac{V_r}{2^n - 1} \times (2^n - 1)\end{aligned}$$

$$V_{FS} = V_r$$

(IV)  $\checkmark$  Resolution :-

$$\checkmark \text{ Resolution} = \frac{\text{Resolution}}{V_{FS}} \times 100$$

$$= \frac{V_r}{2^n - 1} \times 100$$

$$\checkmark \text{ Resolution} = \frac{1}{2^n - 1} \times 100$$

(V) Error / Accuracy :-

→ In ADC/DAC max. error acceptable is 1 LSB bit

$$\text{error} \leq 1 \text{ LSB}$$

$$\text{error} \leq \text{Resolution}$$

Note :-

→ Resolution of R-2-R ladder N/W is

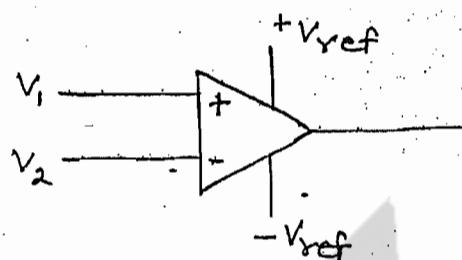
$$R = \frac{V_r}{2^n}$$

$$\text{Resolution of ADC} = \frac{V_r}{2^n - 1}$$

$$\% \text{ Resolution of ADC} = \frac{1}{2^n - 1} \times 100$$

error < Resolution

DAC



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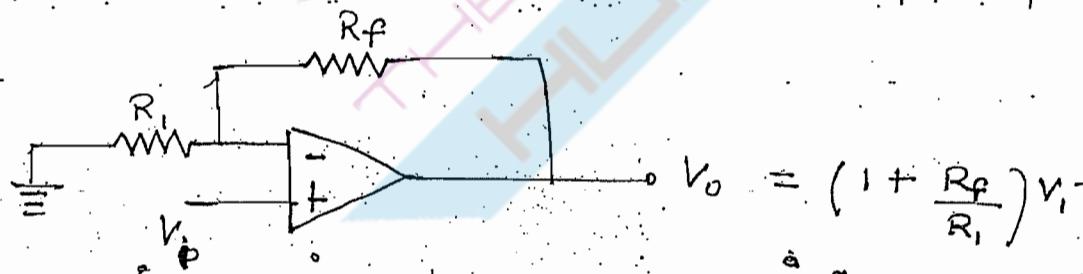
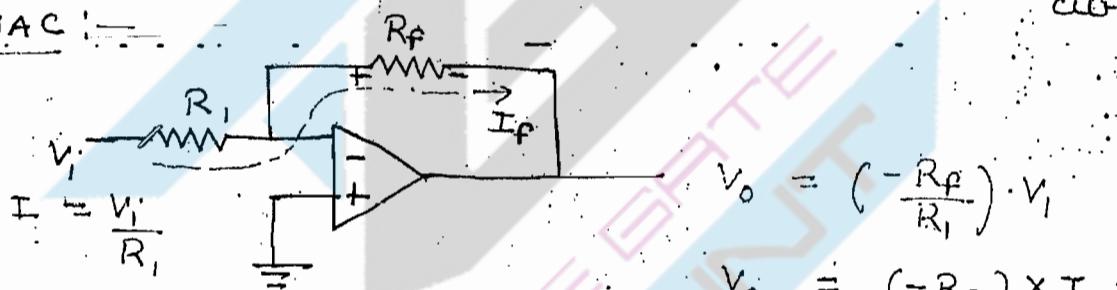
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- For ADC's
- $V_1 > V_2 \rightarrow +V_{ref} \rightarrow \text{logic 1}$
  - $V_1 < V_2 \rightarrow -V_{ref} \rightarrow \text{logic 0}$
  - If  $V_1 = V_2 \rightarrow \pm V_{ref}$  (based on internal bias current)

For DAC :-

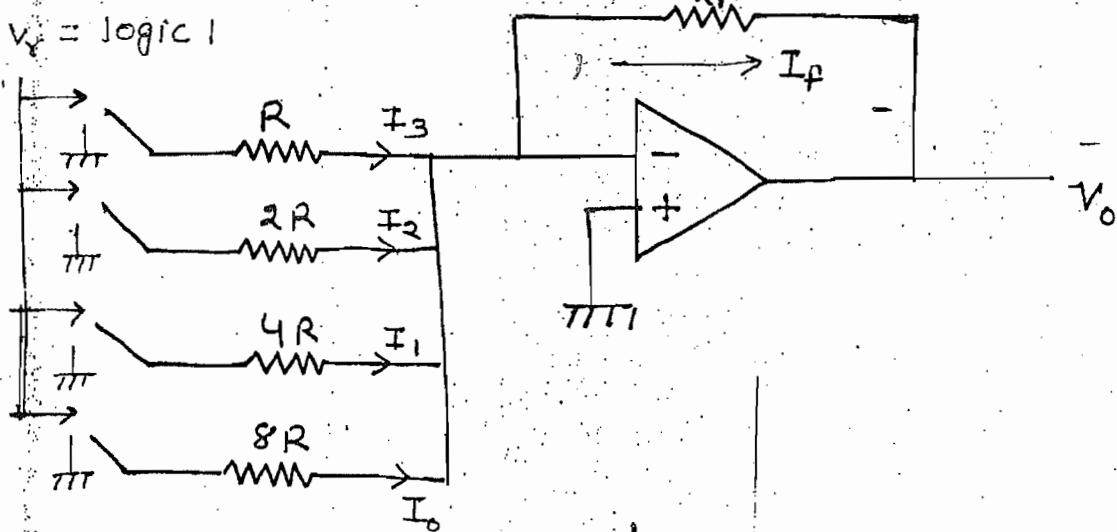


4-bit Weighted Resistor DAC ckt :-

- Accuracy is less due to different resistor
- Assuming 4 bit to

$b_3$	$b_2$	$b_1$	$b_0$
↓		↓	
MSB			LSB

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$$I_3 = \frac{V_x}{R} \times b_3$$

$$I_2 = \frac{V_x}{2R} \times b_2$$

$$I_1 = \frac{V_x}{4R} \times b_1$$

$$I_0 = \frac{V_x}{8R} \times b_0$$

$$I_f = I_3 + I_2 + I_1 + I_0.$$

$$\Rightarrow V_o = (-R_f) I_f$$

**LSB resistance =  $2^{n-1} \times \text{MSB Resistance}$**

### Disadvantage of Weighted Resistor :-

- Accuracy is less due to skiff use of different resistors
- To overcome this R-2R ladder network is used.

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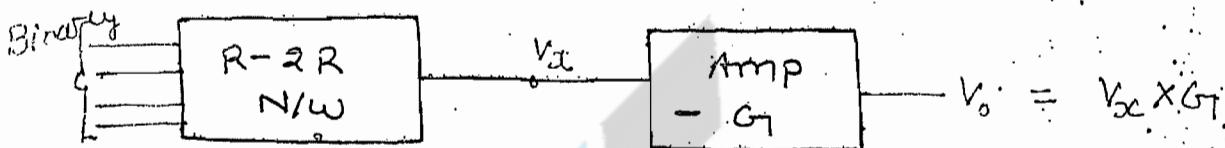
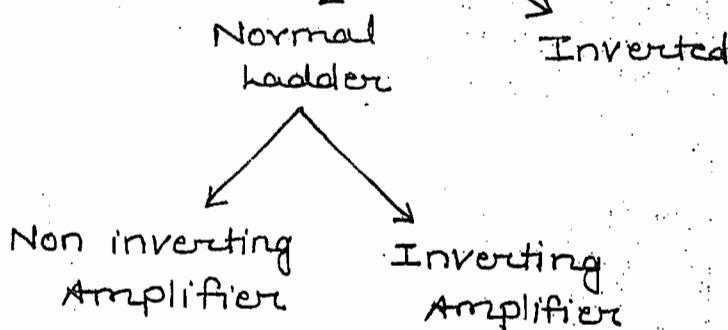
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### R-2R ladder

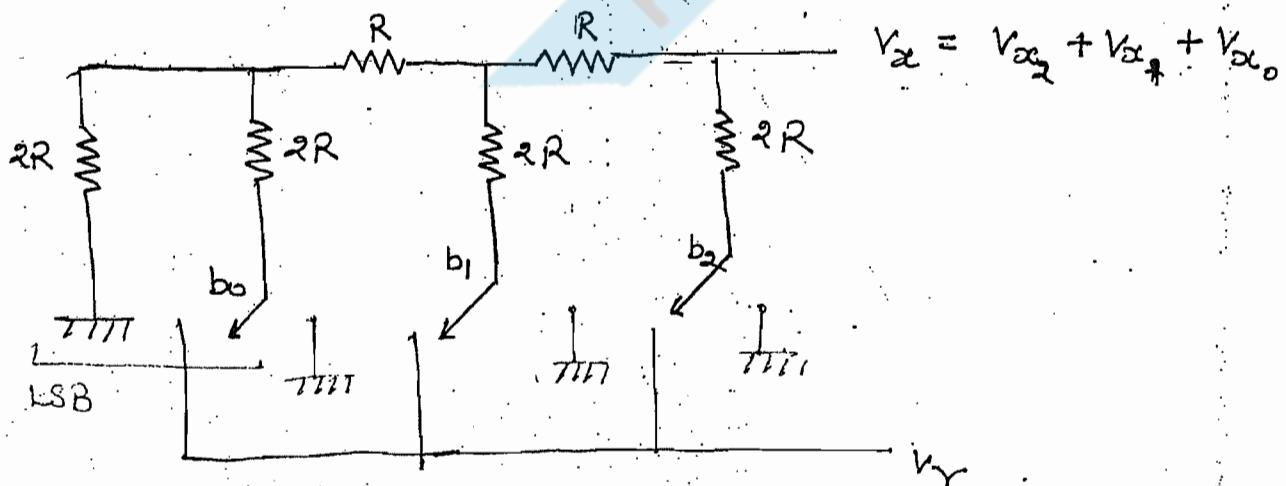


$$V_{xc} = R \times \beta \\ = \frac{V_r}{2^n} \left( \sum_{i=0}^{n-1} 2^i b_i \right)$$

$$V_0 = \frac{V_r}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right) \times G_t$$

$$V_0 = R \times \beta \times G_t$$

### 3-bit R-2-R ladder N/W :-



### Calculation of $V_{x_0}$ :-

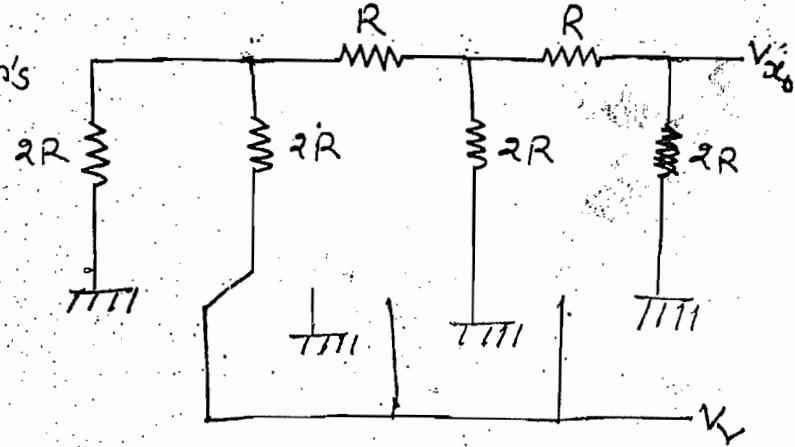
- By using S.T & therenin's theorem

$$V_x = V_{x_2} + V_{x_1} + V_{x_0}$$

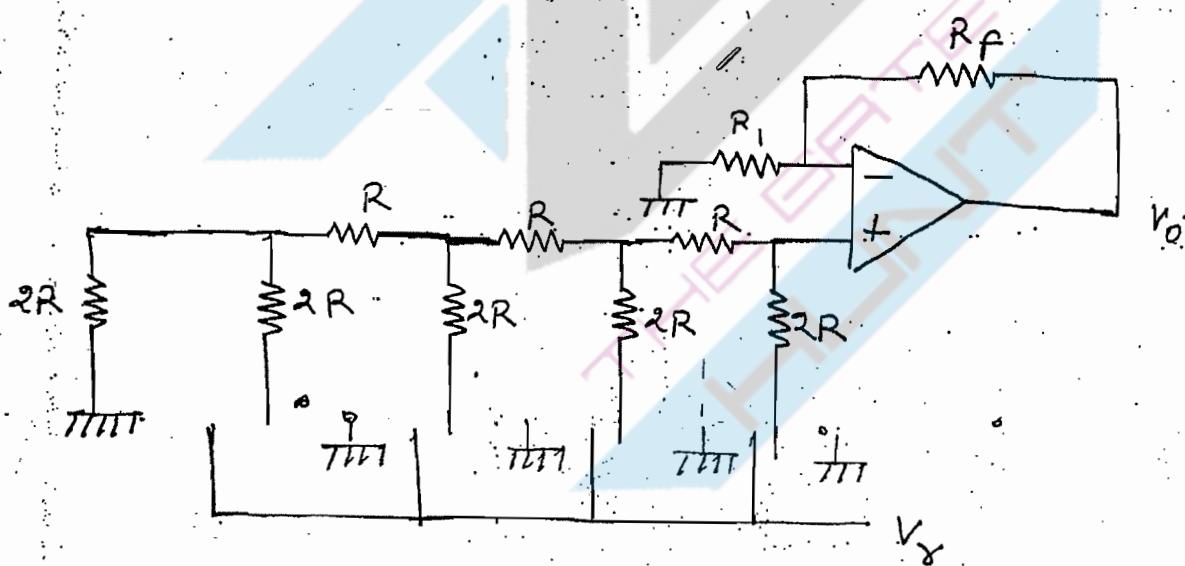
$$= \frac{V_r}{2} \times b_2 + \frac{V_r}{4} \times b_1 + \frac{V_r}{8} \times b_0$$

$$= \frac{V_r}{8} [4 \times b_2 + 2 \times b_1 + b_0]$$

$$V_x = \frac{V_r}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right)$$

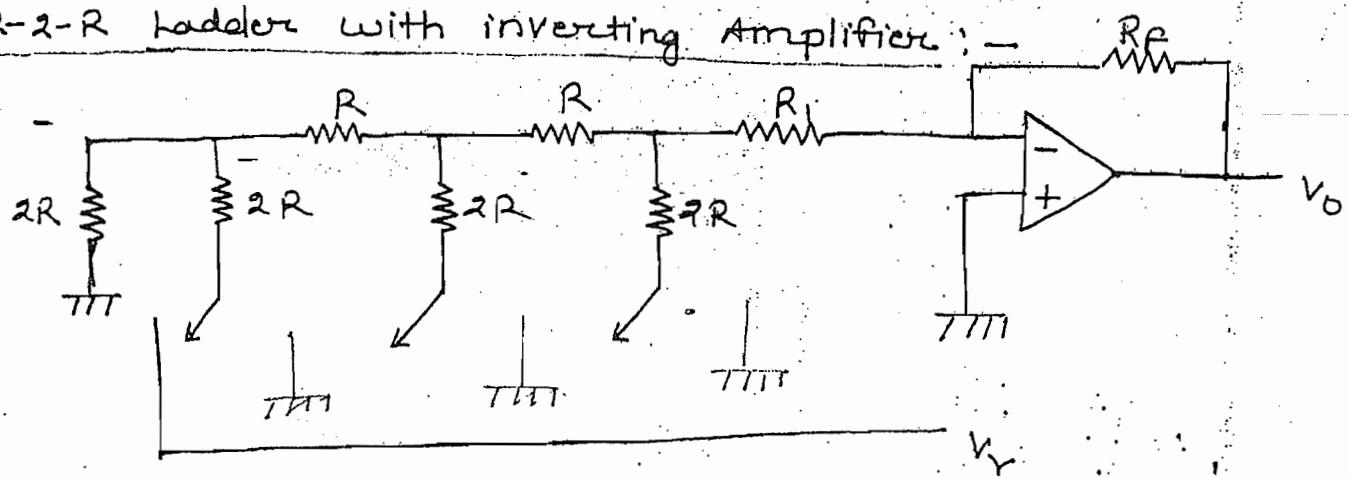


### 4-bit R-2-R ladder DAC (With non-inverting Amp.) :-



$$V_o = \frac{V_r}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right) \times \left( 1 + \frac{R_F}{R_1} \right)$$

## R-2-R ladder with inverting Amplifier :-

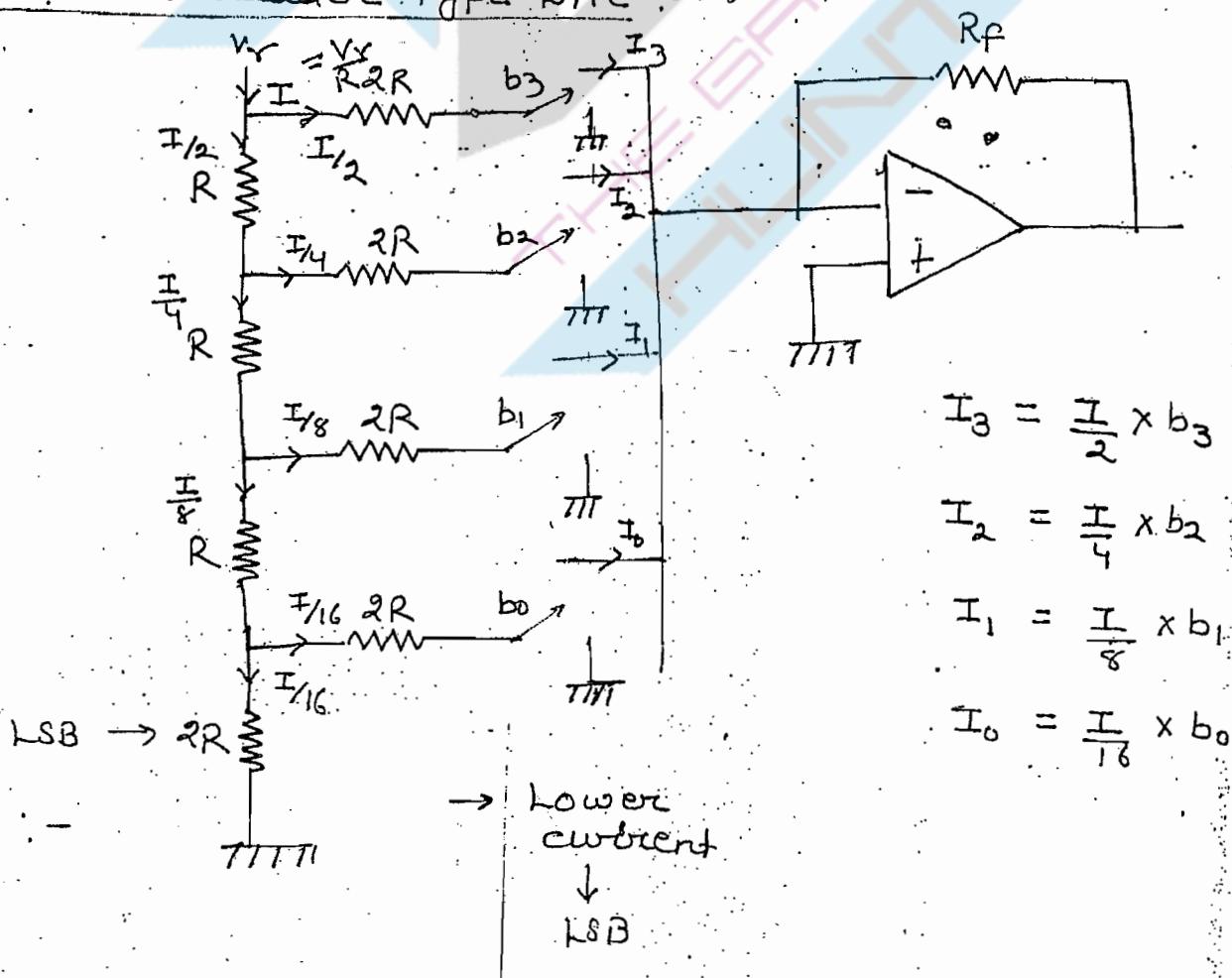


$$V_O = \frac{V_Y}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right) \times \left( -\frac{R_F}{R_1 + R} \right)$$

$$V_O = (-R_F) I_F$$

$$I_F = \frac{V_Y}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right) \left( \frac{1}{R_1 + R} \right)$$

## Inverted ladder type DAC :-



$$\begin{aligned}
 I_f &= I_3 + I_2 + I_1 + I_0 \\
 &= \frac{I}{2} \times b_3 + \frac{I}{4} \times b_2 + \frac{I}{8} \times b_1 + \frac{I}{16} \times b_0 \\
 &= \frac{I}{16} [8 \times b_3 + 4 \times b_2 + 2 \times b_1 + b_0]
 \end{aligned}$$

$$I_f = \frac{V_r}{2^n} \left( \sum_{i=0}^{n-1} 2^i b_i \right) \times \frac{1}{R}$$

$$V_o = (-R_f) \times I_f$$

$$V_o = \frac{V_r}{2^n} \times \left( \sum_{i=0}^{n-1} 2^i b_i \right) \times \left( -\frac{R_f}{R} \right)$$

$$= R \times f \times G$$

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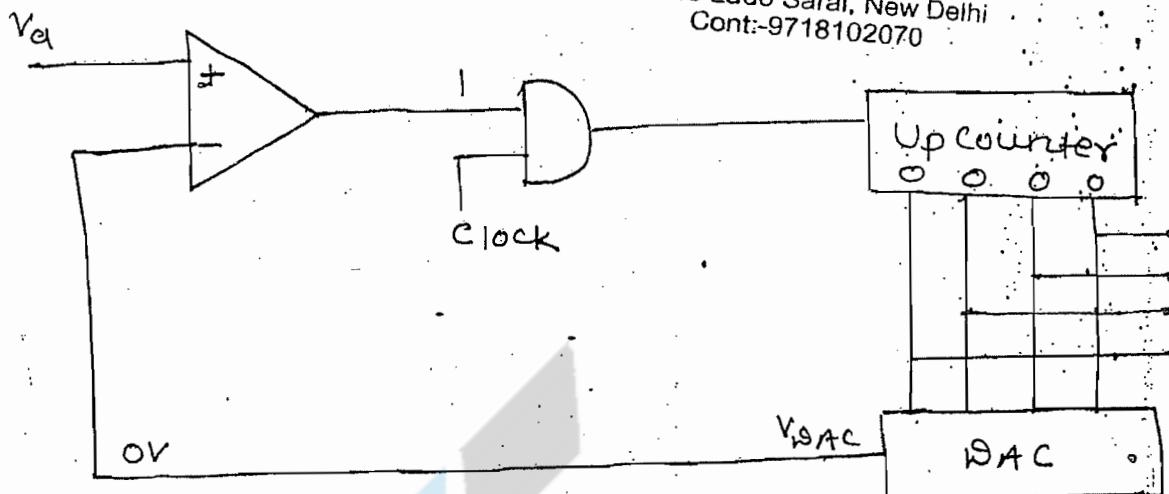
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## ADC :-

### Counter type ADC :-

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Resolution

- In counter type ADC shown in figure, a comparator is used in i/p to compare i/p analog voltage  $V_A$  with feedback reference voltage provided by DAC.
- An Upcounter is used to convert no. of clock pulse applied through AND gate.

### Operation :-

- When analog voltage is greater than feedback voltage, the o/p of comparator is logic 1 and the counter will continuously increment.
- When analog voltage is less than feedback voltage, o/p of comparator is zero and counter will stop at this time and o/p of counter will provide binary value corresponding to input analog voltage.

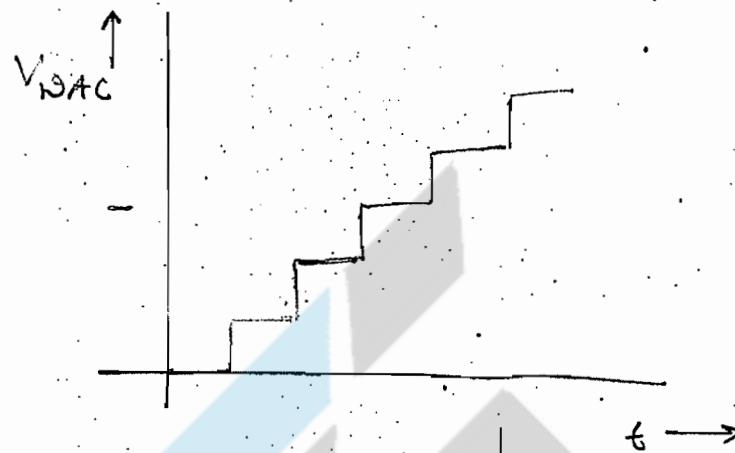
$$\text{eg:- Resolution} = 1V \quad \text{i/p} = V_A = 4.7V$$

o comparing with  $4.7V \Rightarrow V_A > V_{WAC}$   
 counter increment & count = 0001

Process is continue and atlast if  $V_{WAC} = 5V$   
 then  $V_A < V_{WAC}$  & i/p to AND gate = 0 & counter stop.

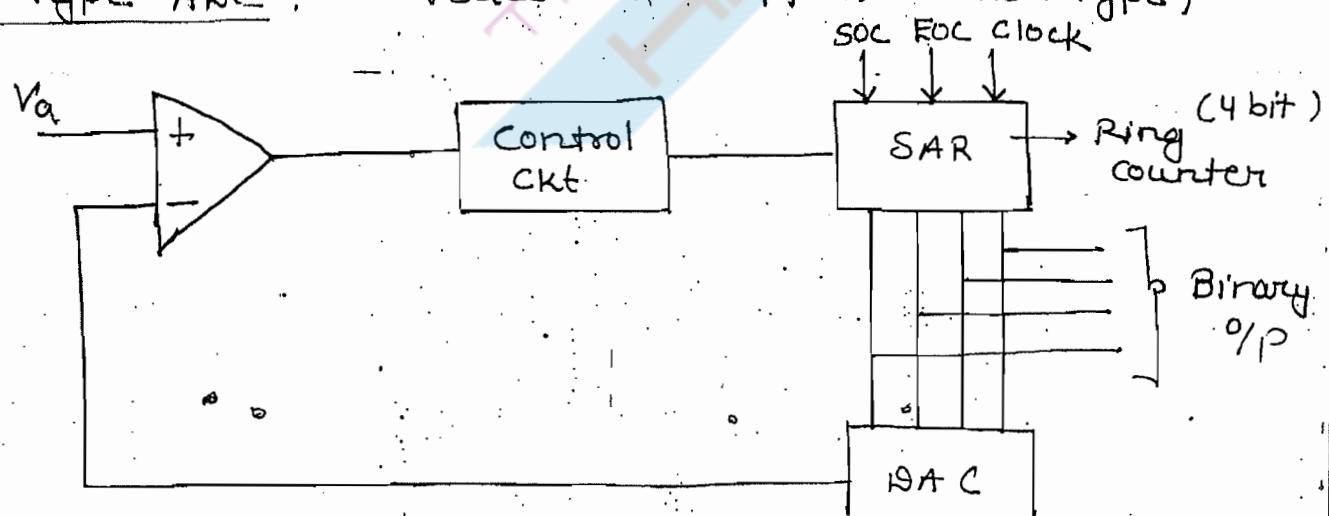
$$\text{Error} = 5 - 4.7 = 0.3V \leq \text{Resolution}(1V)$$

- In counter type ADC for n-bit conversion max. no. of clock pulses used is  $2^n - 1$
- Max. conversion time =  $(2^n - 1) T_{CLK}$
- Min " " = 1
- Avg. " " =  $\frac{2^n - 1 + 1}{2} = 2^{n-1}$



- Counter type ADC is also known as Ramp type ADC
- If up/down Counter is used in counter type ADC then it is known as Tracking type ADC
- In this conversion time depends on i/p analog Voltage

SAR type ADC :— (Successive Approximation type)



## 4-bit Ring counter

- 1. 1000
- 2. 0100
- 3. 0010
- 4. 0001

→ In SAR type ADC shown in fig, comparators used at i/p to compare i/p analog voltage with feedback voltage provided by DAC.

→ In SAR register ring counter is used to set successively one by one bit from MSB to LSB with clock.

→ Control ckt is used to reset current or present set bit in SAR when analog voltage is less than feedback voltage.

5.1V → SOC → 1000 → 0110 → 0101 → 0101 → EOC.

12.3V → SOC → 1000 → 1100 → 1110 → 1101 → 1100 → EOC

→ In SAR type ADC, for n-bit conversion max. no. of clock pulses used is  $2^n$ .

→ Max. conversion time =  $n \times T_{CLK}$

→ In this conversion time is independent of i/p analog voltage.

→ SAR type is faster than counter type ADC.

## Flash type ADC :-

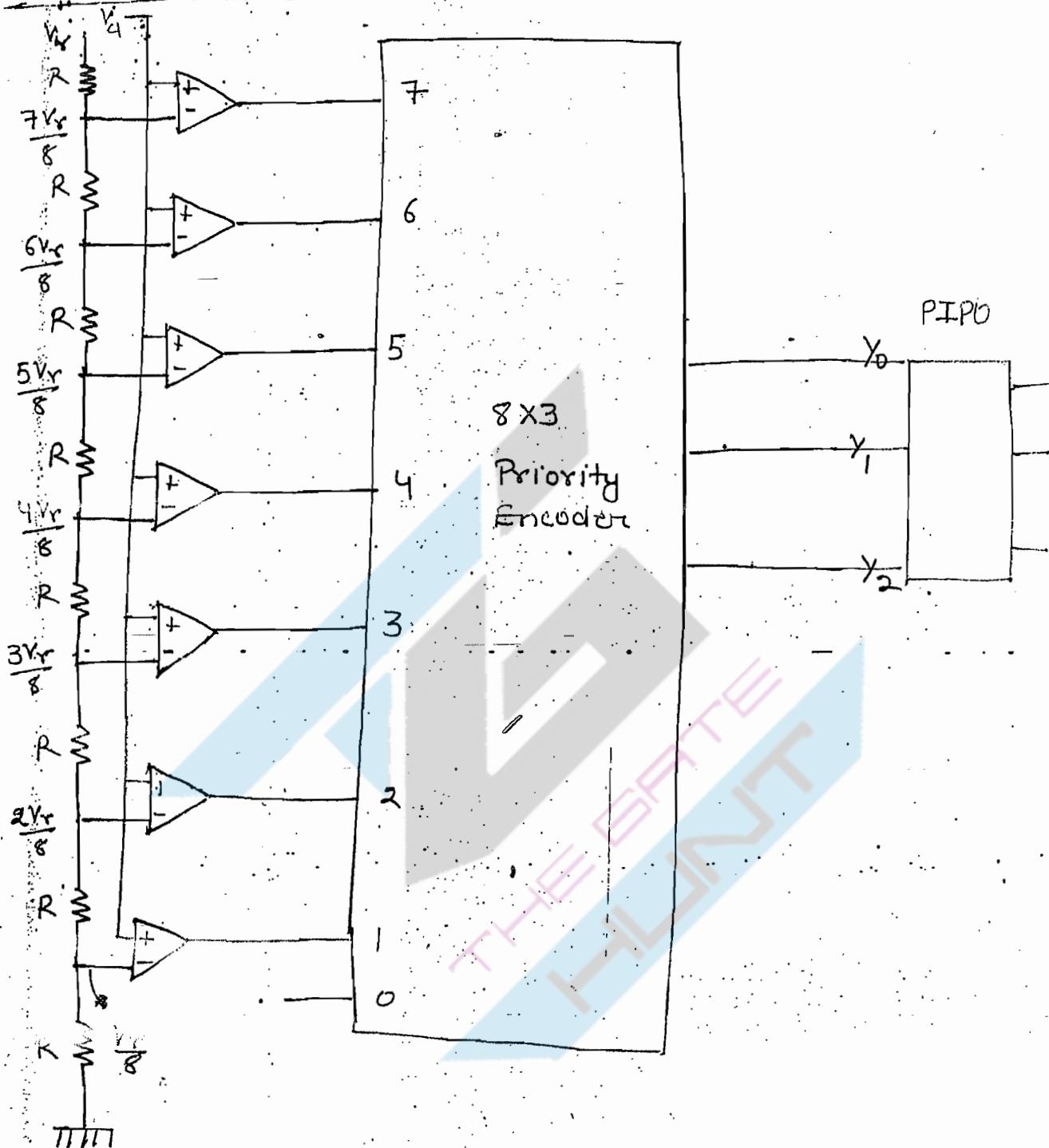
→ No. of comparators are connected in parallel to increase speed of operation. Hence it is known as parallel compare type ADC.

→ In this for n-bit conversion min. no. of comparators required =  $2^n - 1$

→ No. of resistor =  $2^n$  to provide reference voltage.

→  $2^n \times n$  priority encoder

- 3-bit flash type ADC :-



- Max. no. of clock pulses required for flash type → 1
- Fastest type ADC among all
- Range of analog

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Range of analog  
Voltage

$$V_a < \frac{V_r}{8}$$

Binary o/p

$y_2 \ y_1 \ y_0$

0 0 0

$$\frac{V_r}{8} < V_a < \frac{2V_r}{8}$$

0 0 1

$$\frac{2V_r}{8} < V_a < \frac{3V_r}{8}$$

0 1 0

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$$\frac{6V_r}{8} < V_a < \frac{7V_r}{8}$$

1 1 0

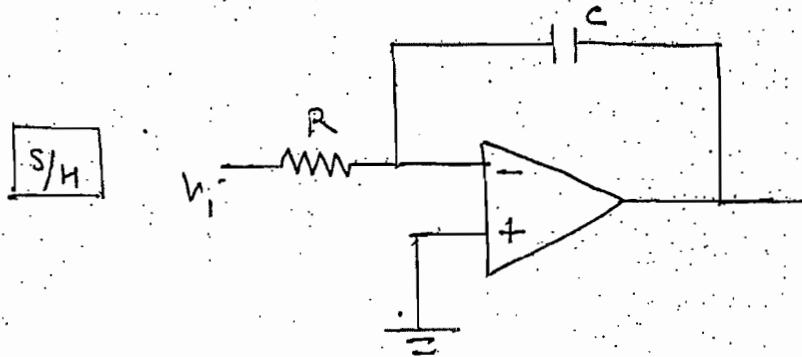
$$V_a > \frac{7V_r}{8}$$

1 1 1

Disadvantage :-

→ Large hardware is required.

Dual slope Integrating type ADC :-

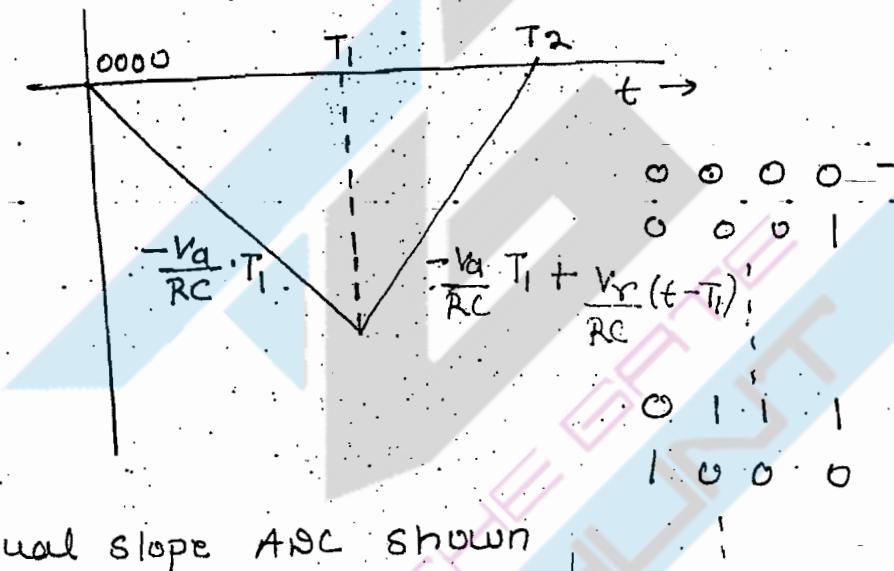
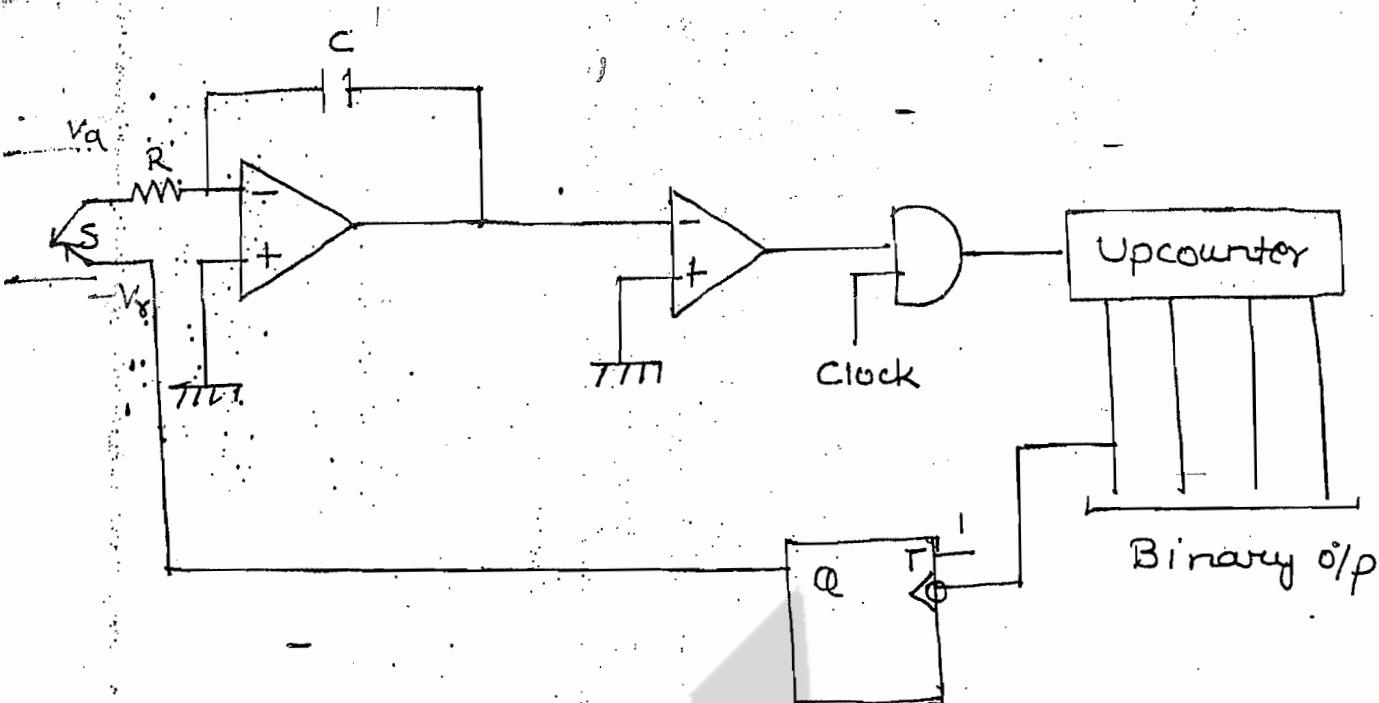


$$V_o = -\frac{1}{RC} \int V_i dt$$

$$= -\frac{V_i}{RC} \cdot \int dt$$

$$= \left( -\frac{V_i}{RC} \right) t$$

Ramp



- In Dual slope ADC shown in figure, an integrator is used to integrate analog voltage  $V_A$  and ref. voltage  $-V_R$  ( $|V_R| > V_A$ )
- When conversion is started counter & t-FF are reset to zero and the switch is connected to analog voltage  $V_A$
- During analog voltage integration o/p of the integrator is -ve voltage have

- After  $2^n$  clock pulse counter will reach count 0 again
- At this time ( $T_1 = 2^n \text{ CLK}$ ), TFF toggles to logic 1 (0 →) and switch 1 is connected to reference voltage
- During reference voltage integration, counter will continue clock pulses upto time  $T_2$
- At  $T = T_2$  integrator o/p is the voltage and count will stop
- Let 'N' is the count when counter has stopped

$$T_2 - T_1 = N \times T_{\text{CLK}}$$

$$V_o = -\frac{V_a}{RC} T_1 + \frac{V_r}{RC} (t - T_1)$$

$$\text{At } t = T_2 ; V_o = 0$$

$$0 = -\frac{V_a}{RC} T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

$$\frac{V_a}{RC} T_1 = \frac{V_r}{RC} (T_2 - T_1)$$

$$V_a \times 2^n T_{\text{CLK}} = V_r N T_{\text{CLK}}$$

$$\Rightarrow V_a = \left( \frac{V_r}{2^n} \right) N$$

$N \rightarrow \text{Count}$

$$V_a \propto N$$

- Most accurate ADC among all
- Ripple will not present
- Mostly used in digital voltmeter
- Slowest ADC among all
- No. of clock pulses =  $2^n + N$
- Max. no. of clock pulse =  $2^n + (2^n - 1)$   
 $\approx 2^{n+1}$

	Clock Time	
Counter type	$\rightarrow (2^n - 1) T_{CLK}$	= $T_S$
SAR type	$\rightarrow (n) T_{CLK}$	= $T_S$
Flash type	$\rightarrow 1 T_{CLK}$	= $T_S$
Stair slope	$\rightarrow (2^{n+1}) T_{CLK}$	= $T_S$

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## Logic families:-

### Transistor

JFB      JcB

RB            RB → Cutoff → OFF

FB            FB → saturation → ON

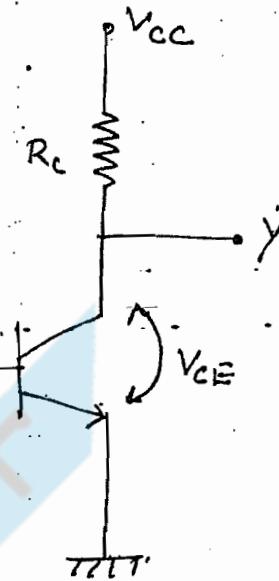
FB            RB → Active

RB            FB → Rev. active

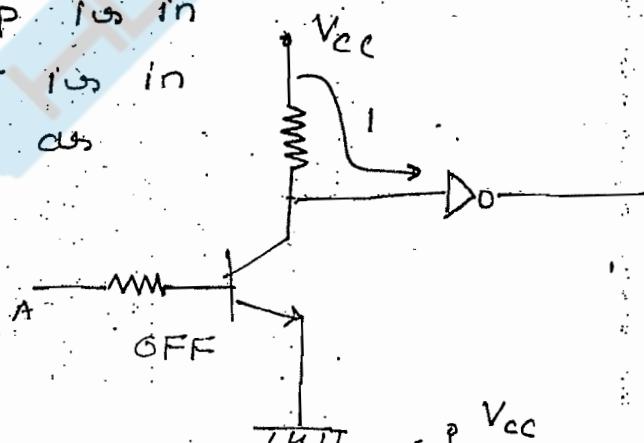
$$\rightarrow V_{cc} = I_c R_c + V_{CE}$$

$$\rightarrow V_{CE} = V_{cc} - I_c R_c$$

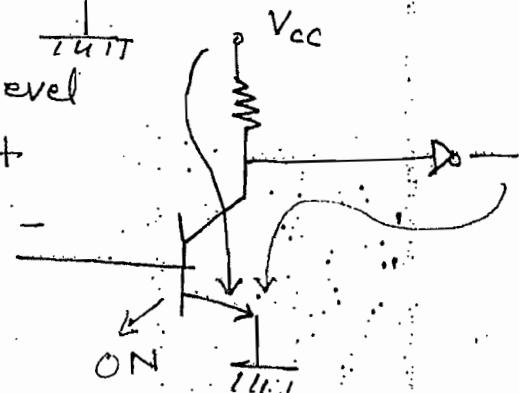
A	T <sub>1</sub>	O/P Voltage	Y
0	OFF	$\approx V_{cc}$	1
1	ON	$V_{CE\text{ sat}}$	0



→ When a logic gate o/p is in logic '1' level (transistor is in OFF state) then it act as current source.



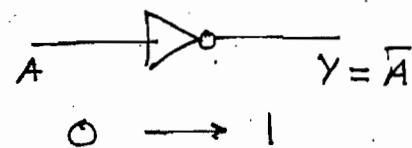
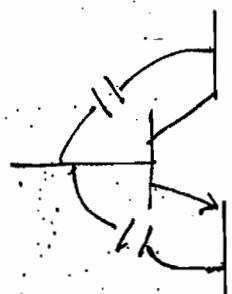
→ When logic gate o/p is zero level (transistor is in ON state) then it will act as current sink.



## Characteristics of logic families:-

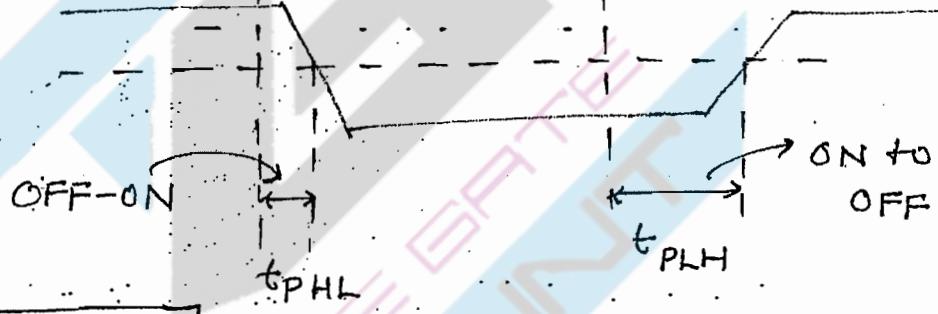
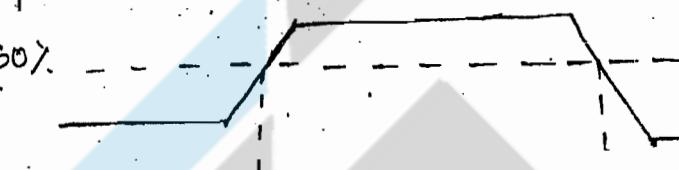
- (i)  $t_{pd}$
- (ii)  $P_{diss}$
- (iii) Figure of Merit
- (iv) fanout
- (v) Noise Margin
- (vi) Wired logic
- (v) fan in.

### (1) Propagation Delay ( $t_{pd}$ ) :-



$t_{pd} \rightarrow ns$

50%



$$t_{PLH} > t_{PHL}$$

→ In transistor  $t_{PLH} > t_{PHL}$  or  $t_{ON-OFF} > t_{OFF-ON}$   
 due to storage time or saturation delay

$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$$

Given:-

$$\text{TTL}, t_{PHL} = 9 \text{ ns}$$

$$t_{PLH} = 11 \text{ ns}, t_{pd} = ?$$

Soln:-

$$t_{pd} = \frac{9+11}{2} = 10 \text{ ns.}$$

### (III) Power dissipation:-

→ indicates power dissipation by 1 logic gate

→ mW

→

$$P_{diss} = V_{cc} I_{cavg}$$

Power diss. in bipolar

$$I_{cavg.} = \frac{I_{CON} + I_{COFF}}{2}$$

→

$$P_{diss} = V_{BB} I_{Bavg.}$$

Power diss in unipolar

### (III) Figure of Merit:-

$$FOM = t_{pd} \times P_{diss}$$

$$\text{ns} \times \text{mW} = \mu\text{J}$$

→ Speed power product

### Level of integration:-

SSI → 1-12 gates } Bipolar

MSI → 13 - 99 gates }

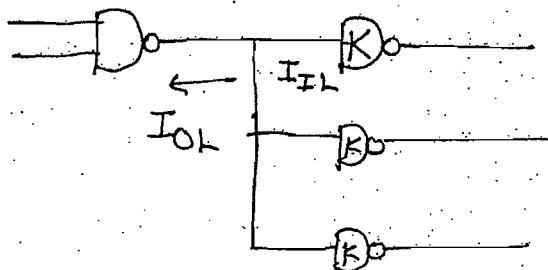
LSI → 100 - 1000 gates } MOS

VLSI → > 1000 gates

### (IV) Fanout:-

→ Max. no. of logic gate that can be driven by a logic gate output without effecting its operation.

→ Fanout depend on current source & current sink property of logic gate



$$\text{fanout}_H = \frac{I_{OH}}{I_{IH}}$$

$$\text{fanout}_L = \frac{I_{OL}}{I_{IL}}$$

$$\text{fanout} = (\text{fanout}_H, \text{fanout}_L) \min$$

Ques:- In TTL logic families,  $I_{OH} = 400 \mu A$

$$I_{IH} = 40 \mu A$$

$$I_{OL} = 16 mA \quad I_{IL} = 1.6 mA$$

$$\text{Fanout} = ?$$

Soln:-  $\text{Fanout}_H = \frac{400}{40} = 10$

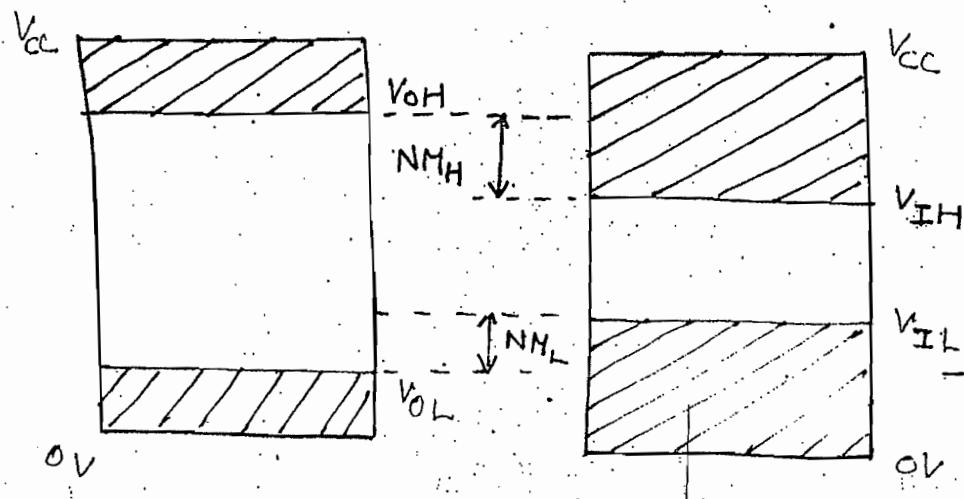
$$\text{Fanout}_L = \frac{16}{1.6} = 10$$

$$\text{Fanout} = 10$$

Noise Margin:-



→ Noise Margin is the max. noise voltage that can be added to a logic gate input which will not effect output

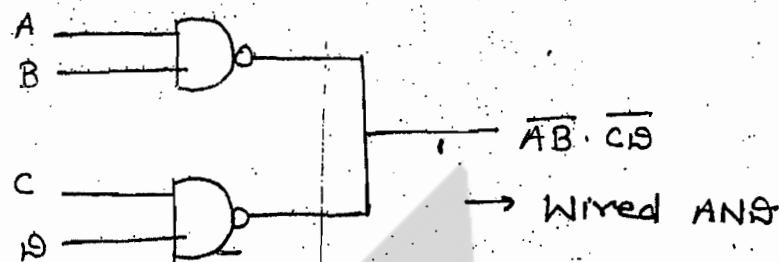


$$NM_H = V_{OH} - V_{IH}$$

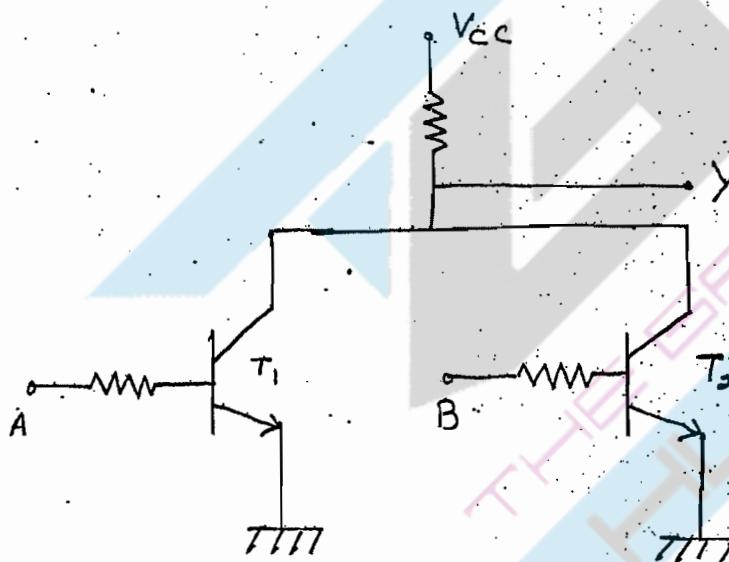
$$NM_L = V_{IL} - V_{OL}$$

$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$

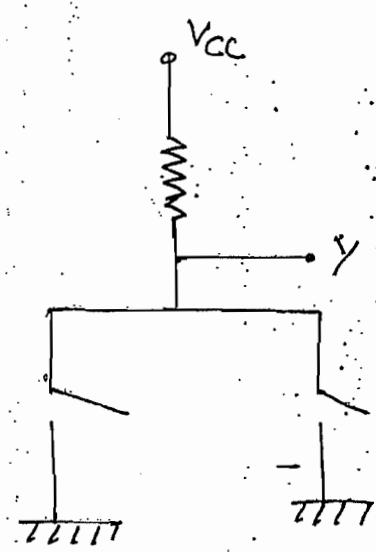
### (VII) Wired Logic :-



### Resistor Transistor Logic (RTL) :-



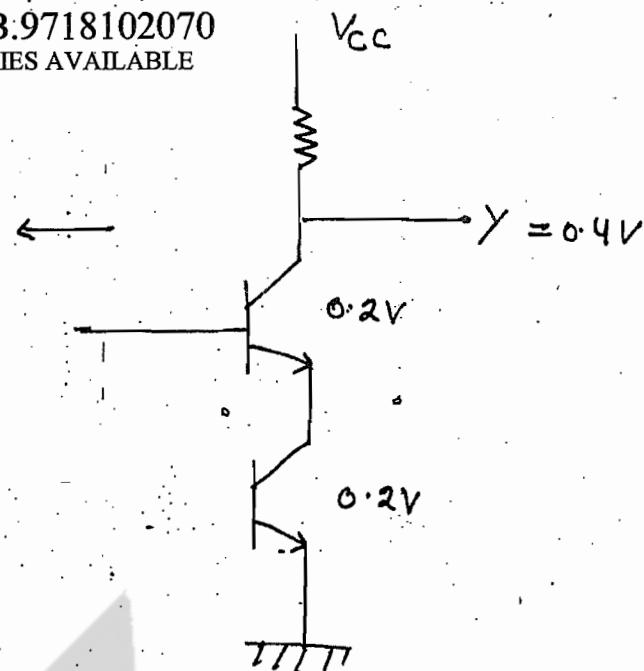
A	B	T <sub>1</sub>	T <sub>2</sub>	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0



$$\text{Logic 0} = 0.2V$$

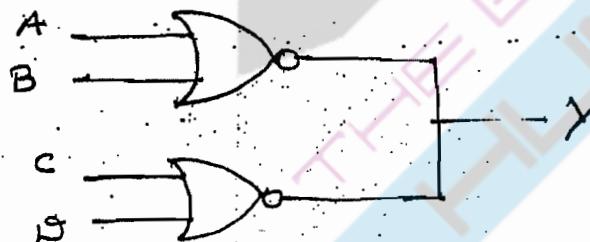
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It is not used  
because  $Y = 0.4V$

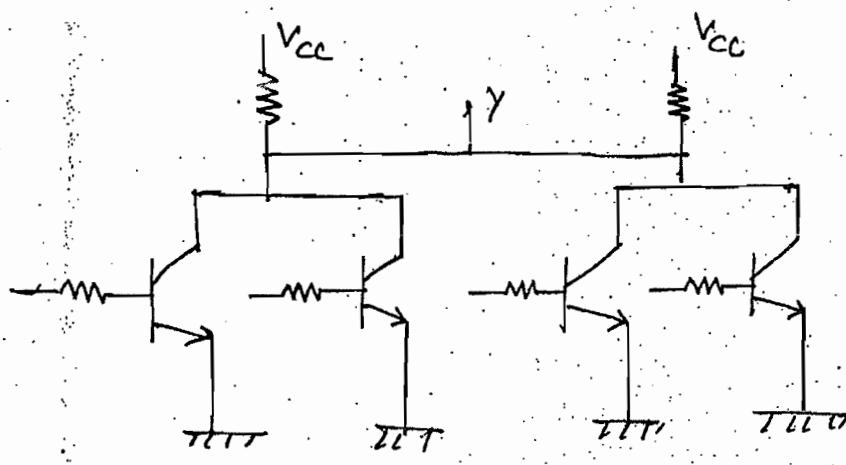


- Basic gate  $\Rightarrow$  NOR
- $t_{pd} = 50\text{ ns}$
- $P_{diss} = 10\text{ mW}$
- $FOM = 500 \text{ pJ}$
- Noise Margin  $= 0.2V$
- fanout  $= 3$
- Wired AND operation.

Ques:- The circuit shown in figure contains 2 RTL NOR gate then for given i/p ; output Y is



SOLN:- 
$$Y = (\overline{A+B}) \cdot (\overline{C+D})$$



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A	B	C	D		Y
0	0	0	0	.	1
0	0	0	1	.	0
1	0	0	1	.	0
1	1	0	1	.	0
1	0	1	1	.	1
0	1	1	1	.	1
1	1	1	1	.	0

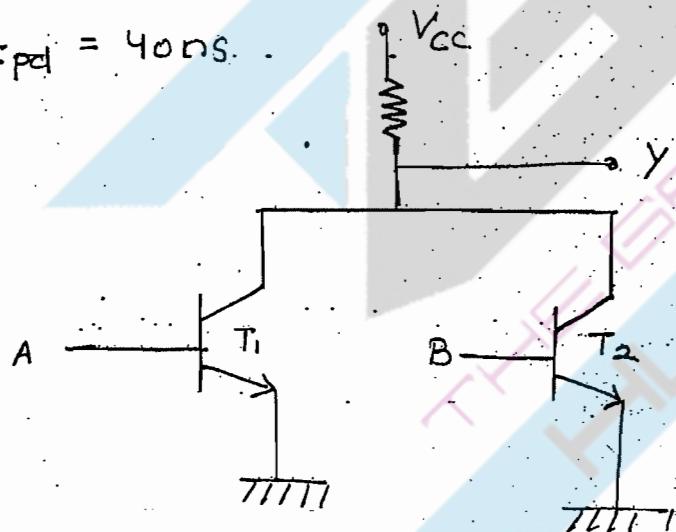
$$\Rightarrow Y = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} = (\bar{A} + B) \cdot (\bar{C} + D)$$

Disadvantage:-

- Speed of operation less
- Noise Margin less
- Fanout very less

Direct Coupled Transistor Logic (DCTL):-

$$\rightarrow t_{pd} = 40\text{ns.}$$



Speed of operation depends on

- (i) RC Time constant
- (ii) Storage time / saturated delay

→ In DCTL logic family base resistance is removed due to this RC time constant dec and speed of operation of gate will improves when compared with RTL logic gate.

Disadvantage:-

Current Hoggling:-

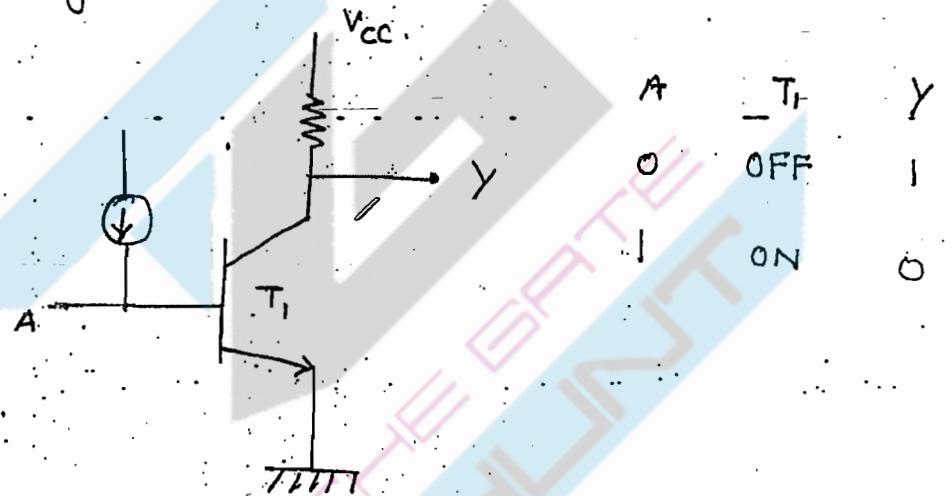
A	B	T <sub>1</sub>	T <sub>2</sub>	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	0

Current Hoggling

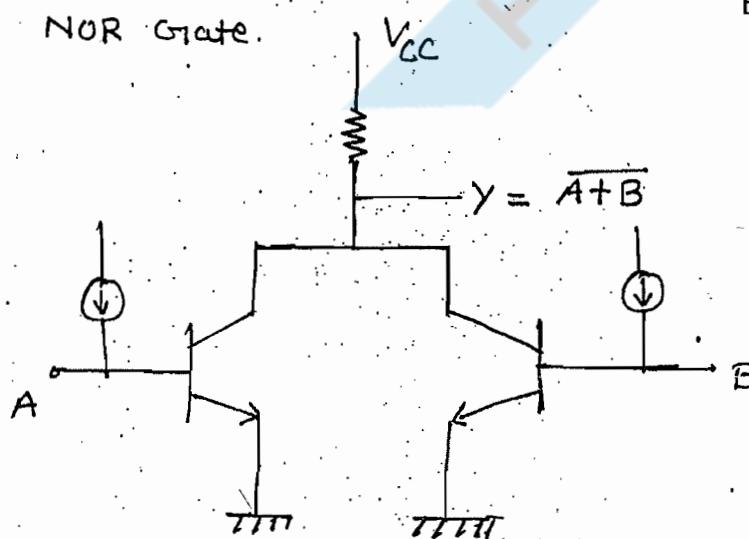
To avoid current hoggling I<sup>2</sup>L logic family is used

I<sup>2</sup>L (Integrated Injection logic) :-

→ I<sup>2</sup>L NOT gate

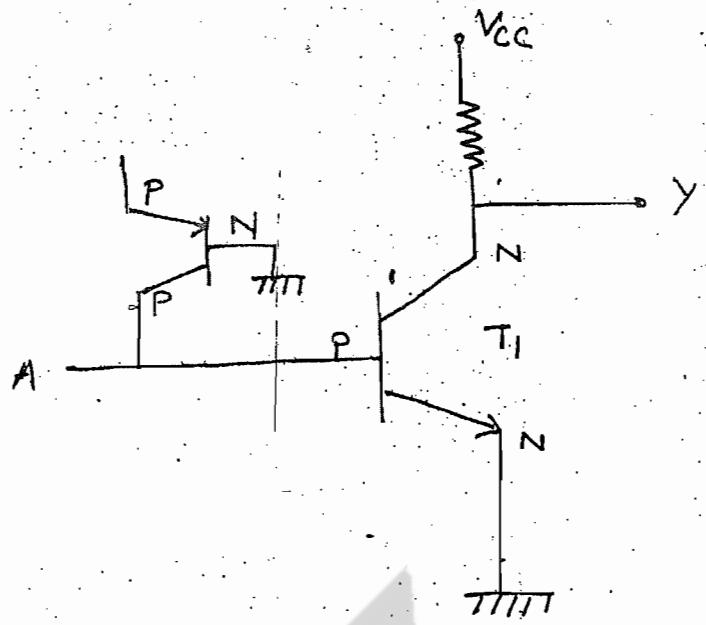


→ I<sup>2</sup>L NOR Gate.



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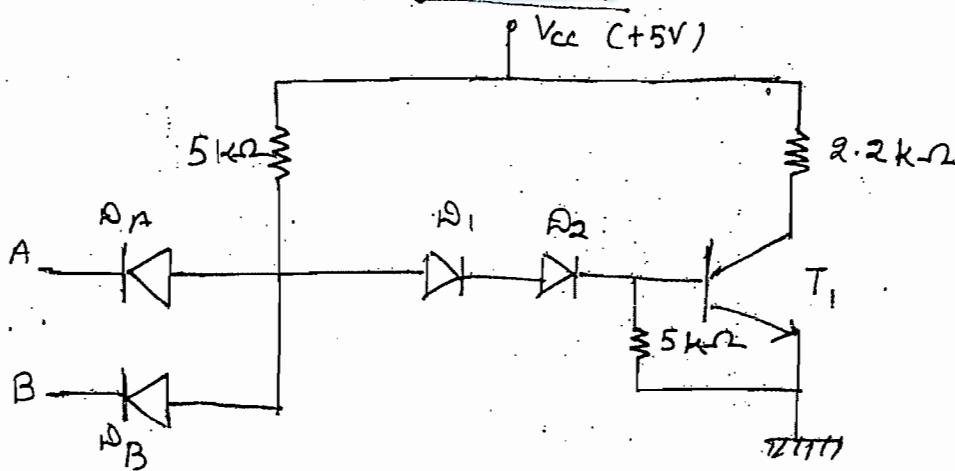
High level of integration

- In I<sup>2</sup>L logic family, PNP, NPN transistors are integrated together during IC fabrication. due to this transistor occupies less area (small geometry, low gain)
- I<sup>2</sup>L is also called as MTL logic family
- Merged-transistor logic
- I<sup>2</sup>L is mostly used in MSI and LSI circuit due to its higher level of integration
- I<sup>2</sup>L main advantage is having best FOM among all logic families.

$$FOM = 0.1PJ - 0.7PJ$$

- I<sup>2</sup>L is available with multicollector o/p.

### Diode Transistor Logic (DTL)



$A_1$	$B$	$D_A$	$D_B$	$R_1$	$D_2$	$T_1$	$Y$
0	0	ON	ON	OFF	OFF	OFF	1
0	1	ON	OFF	OFF	OFF	OFF	1
1	0	OFF	ON	OFF	OFF	OFF	1
1	1	OFF	OFF	ON	ON	ON	0

- Diode  $D_2$  is used to improve Noise Margin
- If one more diode  $D_3$  is connected in series with  $D_2$  then noise margin will improves whereas fanout will decreases.

→  $t_{pd} = 30\text{ns}$  → Basic gate is NAND

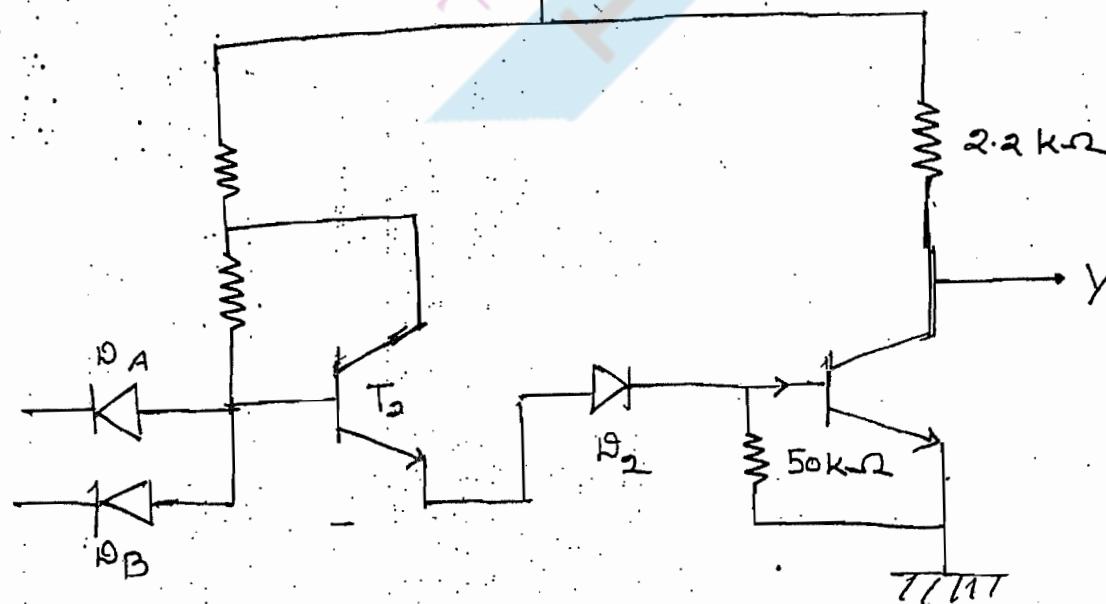
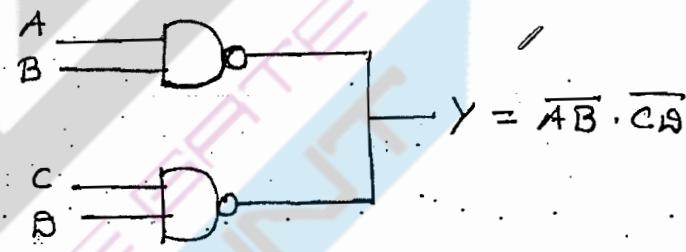
→  $P_{diss} = 8\text{mW}$  → fanout 3

→  $FOM = 24\text{PJ}$  → Wired AND

→  $NM = 0.75V$

→ Basic TTL

Standard TTL:-

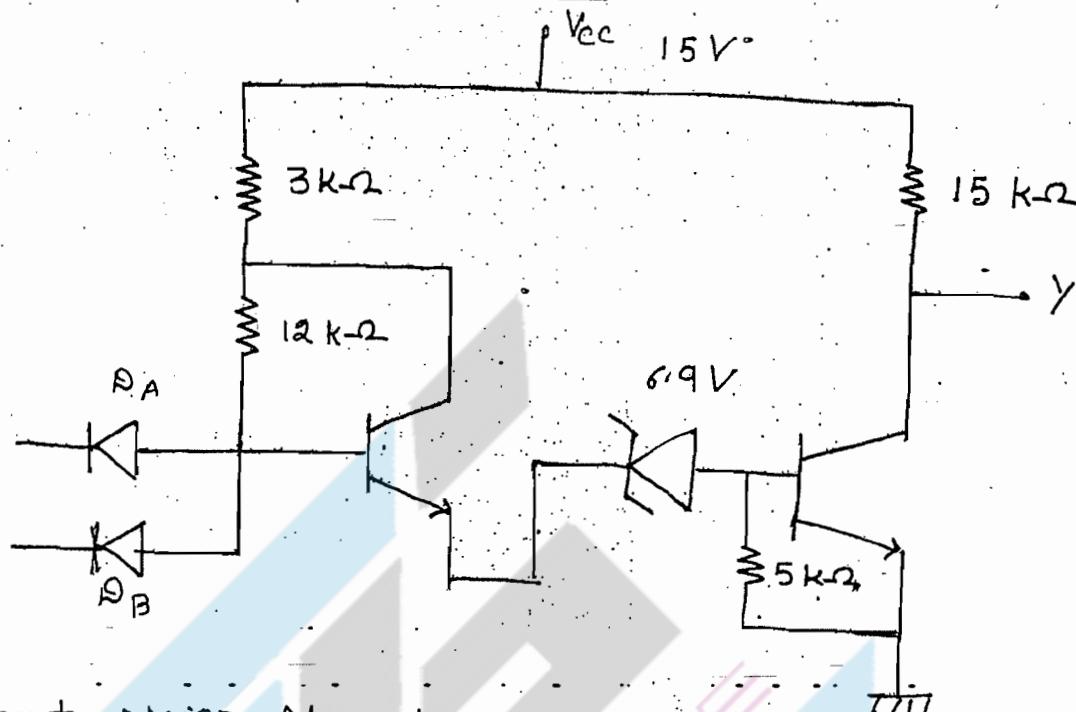


- In TTL logic family to improve fanout diode  $D_1$  is replaced with transistor  $T_2$  and resultant family

is known as standard TTL

→ TTL logic family is mostly used in monolithic IC fabrication

### High Threshold Logic family (HTL)



→ Highest Noise Margin

$$NM \Rightarrow 4V - 5V$$

High noise immunity

→ logic 0  $\rightarrow 2V$   
logic 1  $\rightarrow 14V$  ] Higher voltage swing

→ fanout - 10

→ Wired AND operation

→  $t_{pd} = 90\text{ ns}$

→  $P_{diss} = 55\text{ mW}$

→ FOM  $\approx 5000\text{ PJ}$

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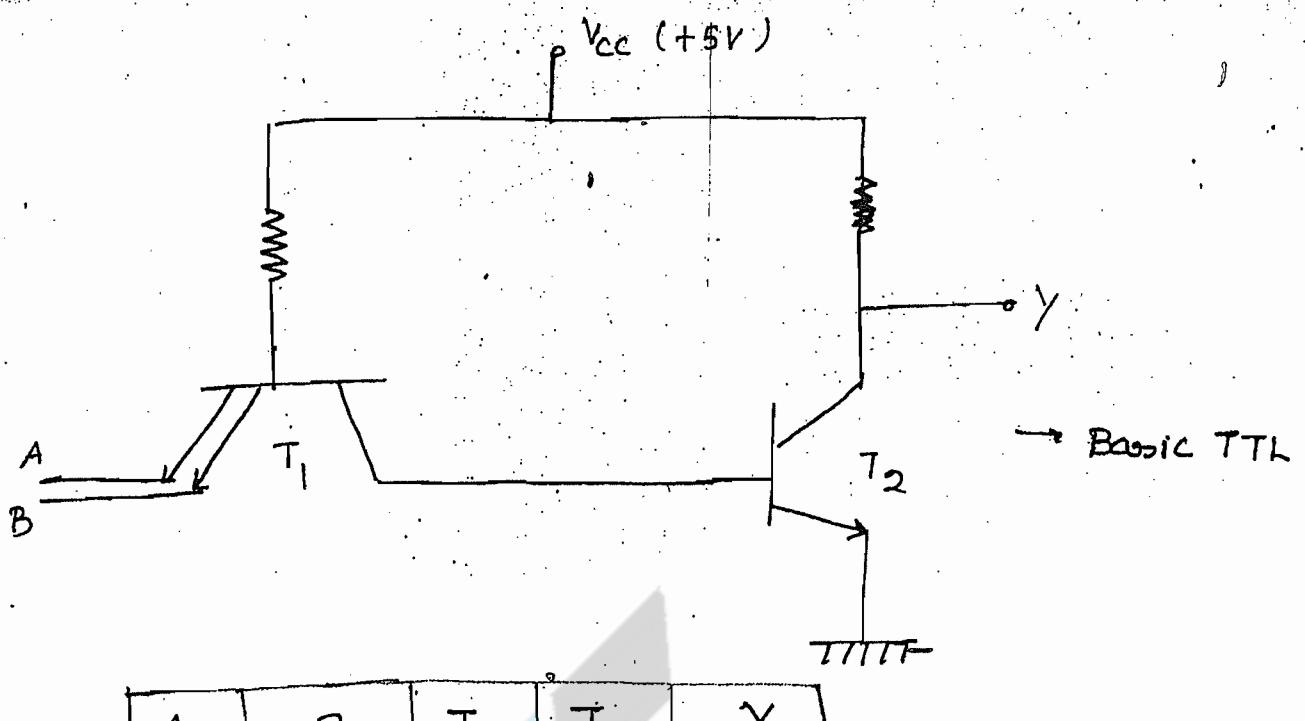
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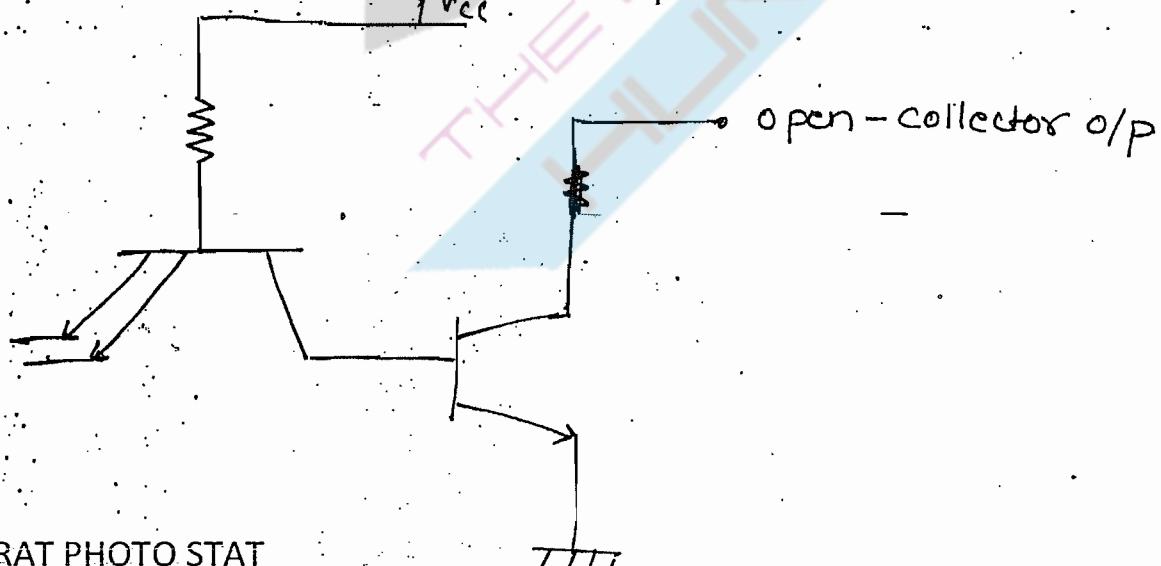
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A	B	T <sub>1</sub>	T <sub>2</sub>	Y
0	0	A	C	1
0	1	A	C	1
1	0	A	C	1
1	1	RA	S	0

→ In TTL logic family open collector outputs are used to provide wired AND operation.



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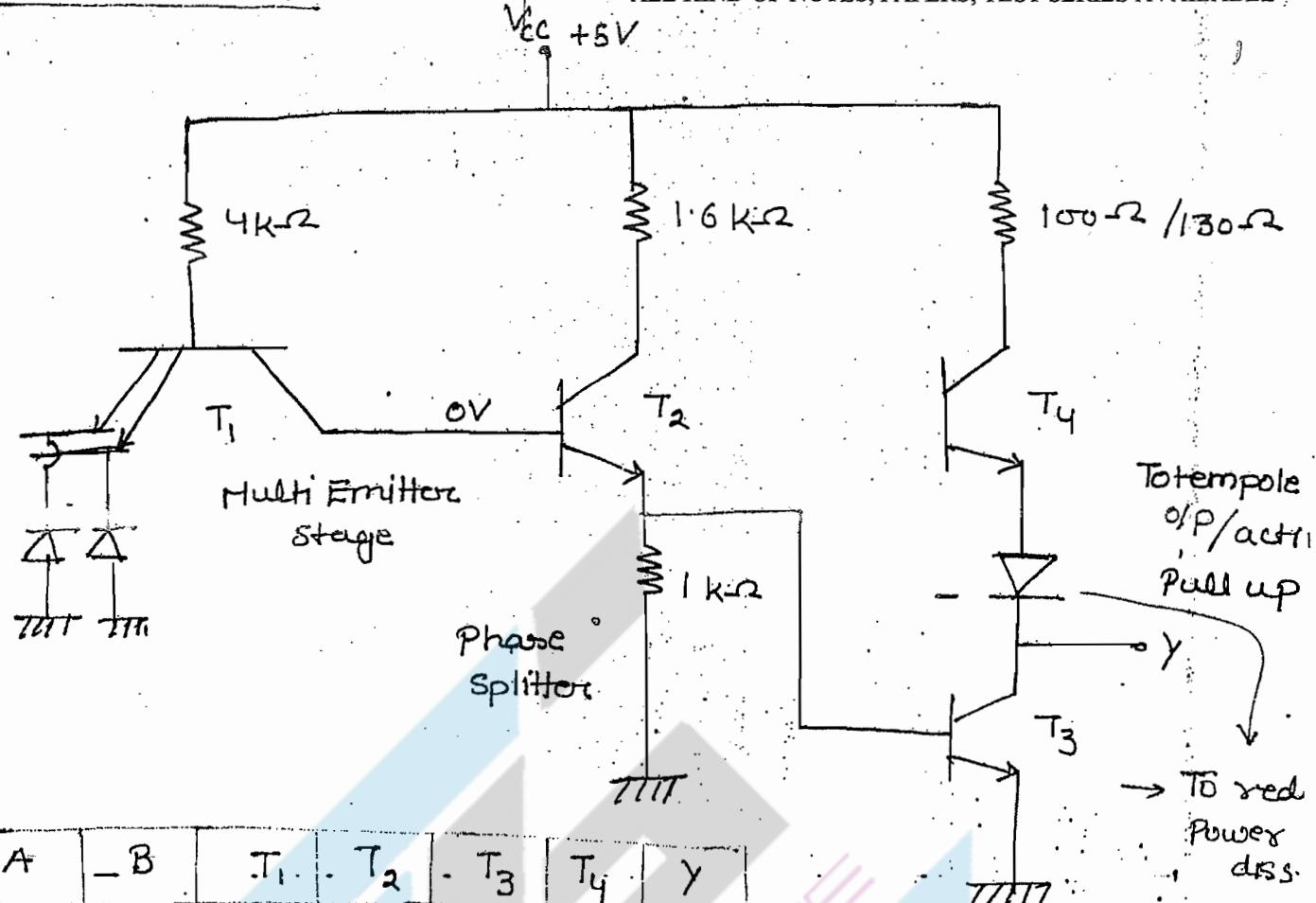
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Standard TTL :-

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A	-B	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	Y
0	0	A	C	C	S	I
0	1	A	C	C	S	I
1	0	A	C	C	S	I
1	1	RA	S	S	C	O

→ NANs

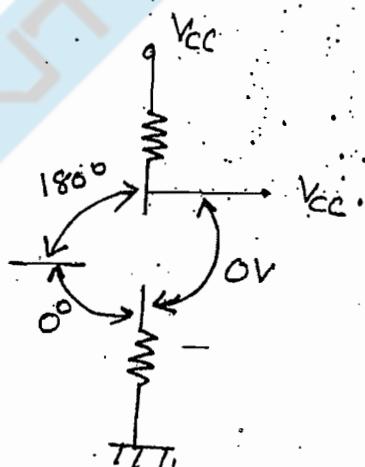
→ tpd - 10ns

→ Pdiss - 10mW

→ fanout - 10

→ FOM - 100PJ

→ NM - 0.4V

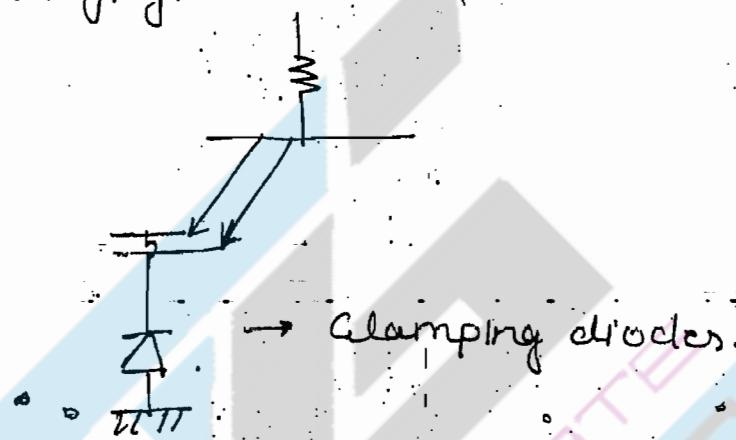


(Phase splitter)

V <sub>OH</sub> = 2.4V
V <sub>IH</sub> = 2V
V <sub>IL</sub> = 0.8V
V <sub>OL</sub> = 0.4V

## Advantage of totem pole o/p:-

- Higher speed of operation
- Low power dissipation
- Higher fanout
- Totem pole o/p or active pull up o/p is not used for wired operation.
- Diode is used in totem pole stage to cut-off transistor  $T_4$  when  $T_3$  is ON
- Clamping diodes are used in i/p stages/voltages to protect Transistor  $T_1$  during high freq transition or spikes or Ringing.



## TTL:-

10ns  $\rightarrow$  7400

$\rightarrow$  74H

(i) Standard TTL  $\rightarrow$  74L (ii) High speed TTL  $\rightarrow$  6ns / High power diss.

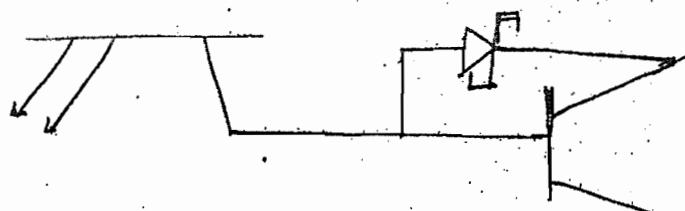
(iii) Low power TTL  $\rightarrow$  22ns (iv) Schottky TTL  $\rightarrow$  74S  $\rightarrow$  2ns

→ In TTL logic family if external resistors values are reduce then RC value will decrease and speed of operation increase & resultant logic family known as high speed TTL

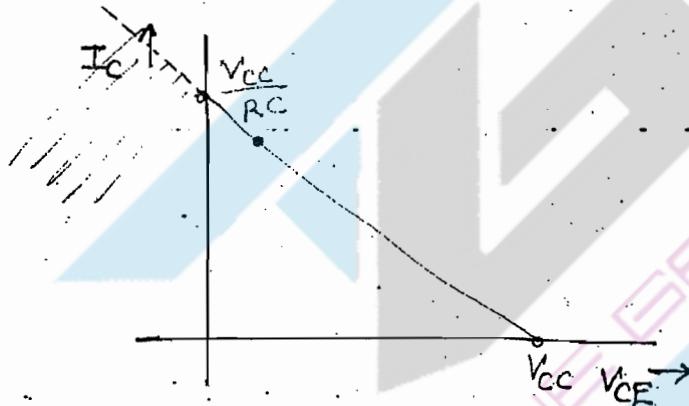
→ In low power TTL, resistor values are increased to reduce power dissipation.

→ If schottky diode is placed b/w base and collector terminal of each transistor in TTL then it remove storage time or saturation delay. Due to this speed of operation will increase and resultant logic family known as schottky TTL.

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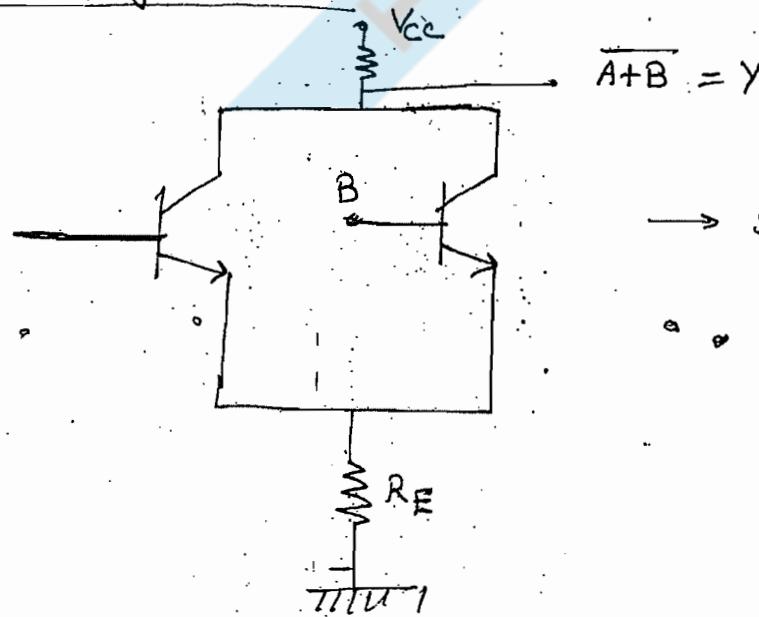
- ALS (Advanced low power schottky)
- LS (Low power schottky)



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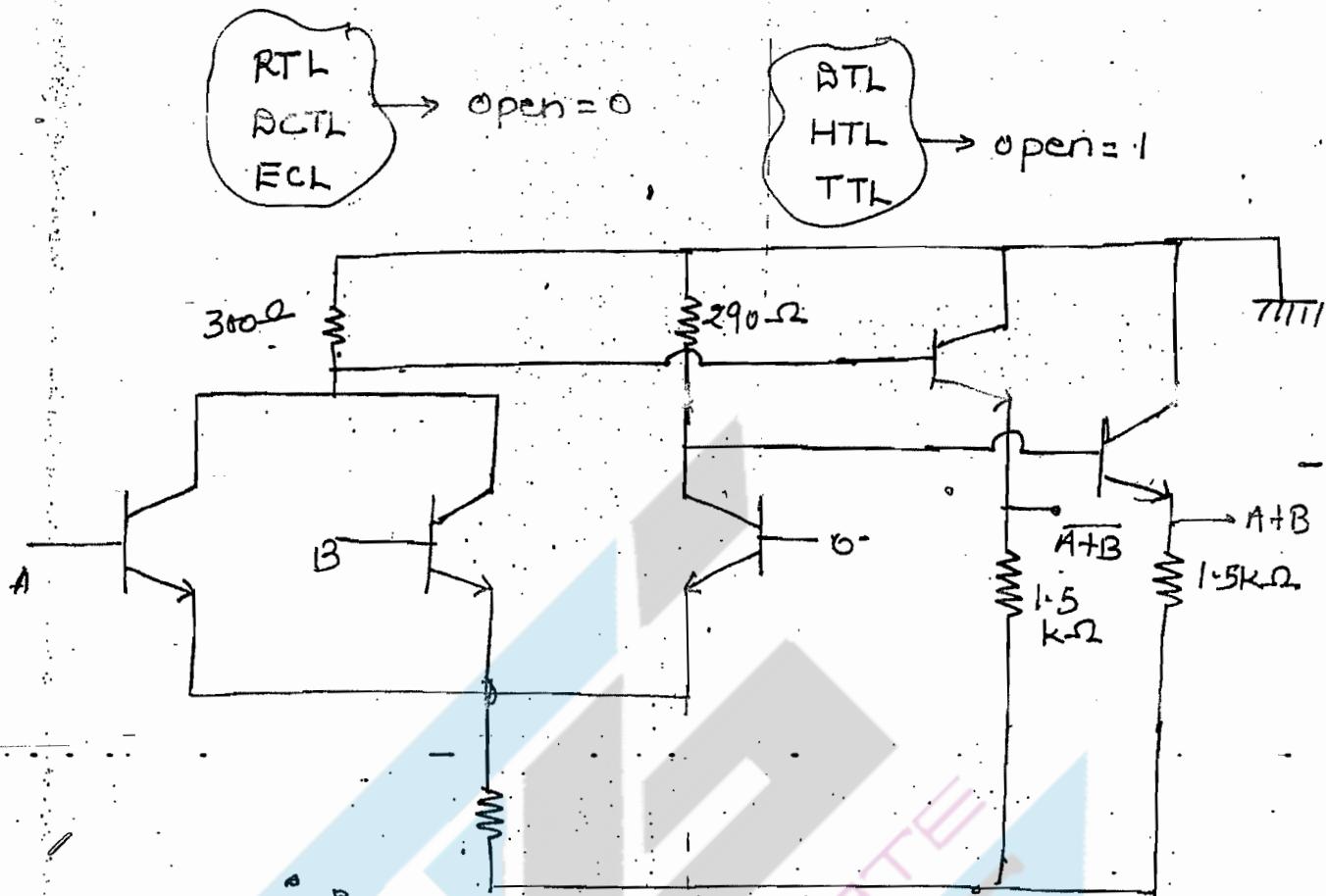
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### Emitter Coupled Logic (ECL)



→ Simple ECL

- In ECL logic family transistors are operated cut-off and active mode.
- Fastest logic family because is non-saturated

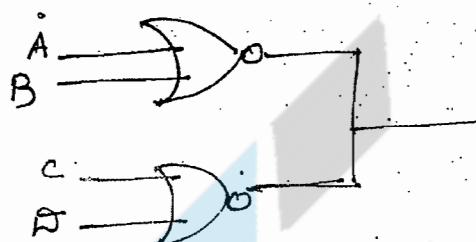


- ECL basically contains two stages! -
- (i) Differential Amplifier stage
- (ii) CC (or) Emitter follower
- To use differential amplifier, component complement o/p are available in ECL
- NOR/OR Gate  $\rightarrow P_{ds} = 55 \text{ pJ}$   $P_{diss} = 55 \text{ mW}$
- $t_{pd} = 1 \text{ ns}$   $\rightarrow \text{FOM} \rightarrow 55 \text{ pJ}$
- fanout = 25
- ECL uses (-ve) power supply. Due to this power supply ripple / noise / spikes / glitches will not effect operation of logic gate.
- logic 0 =  $-1.7V$   
logic 1 =  $-0.8V$  } true logic

$V_{OL} = -1.7V$
$V_{IL} = -1.4V$
$V_{IH} = -1.1V$
$V_{OH} = -0.8V$

→ ECL will provide wired OR operation.

Ques:- The ckt shown in figure use ECL, O/P Y is



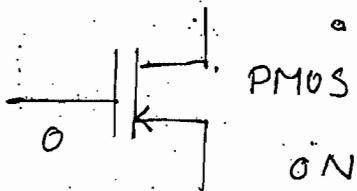
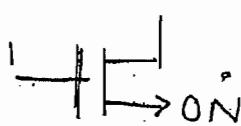
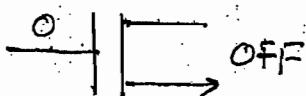
Ans:-  $Y = \overline{A+B} + \overline{C+D}$

→ ECL is also known as current mode logic family (CML).

Disadvantage:-

→ High power dissipation.

NMOS:-



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PMOS  
 logic 0 → ON

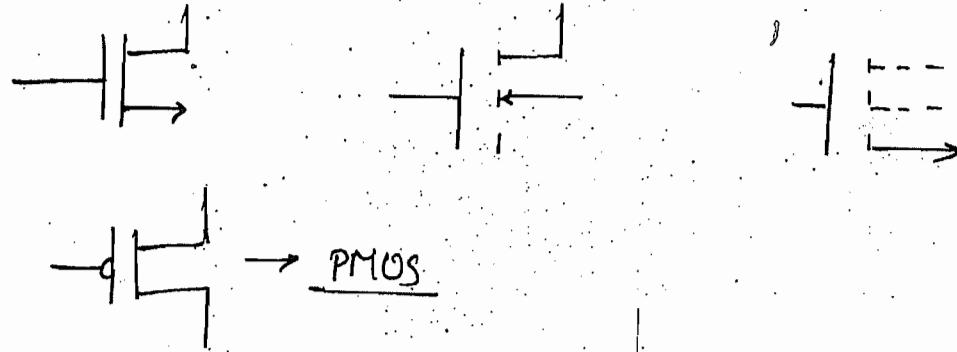
1 → OFF

N-MOS

0 → OFF

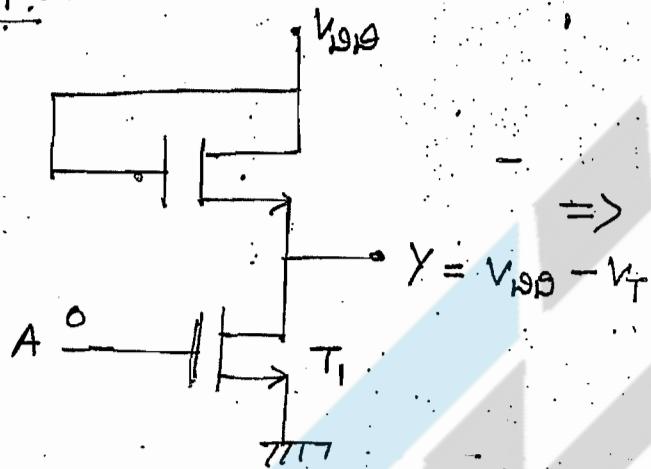
1 → ON

NMOS :-

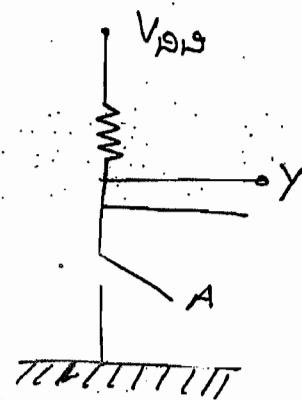


→ PMOS

NOT :-

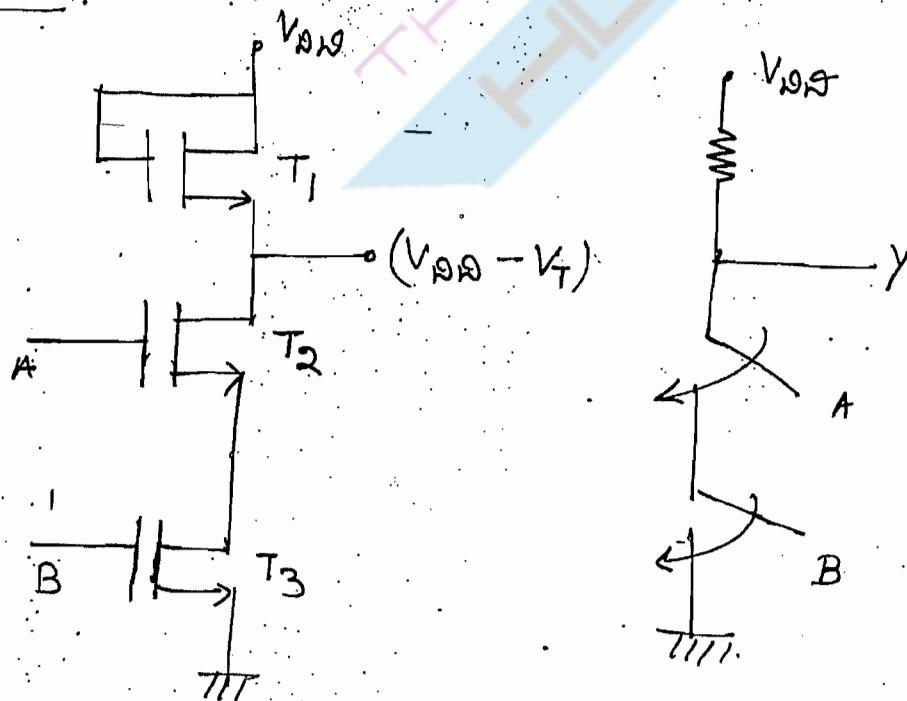


$$Y = V_{DD} - V_T$$

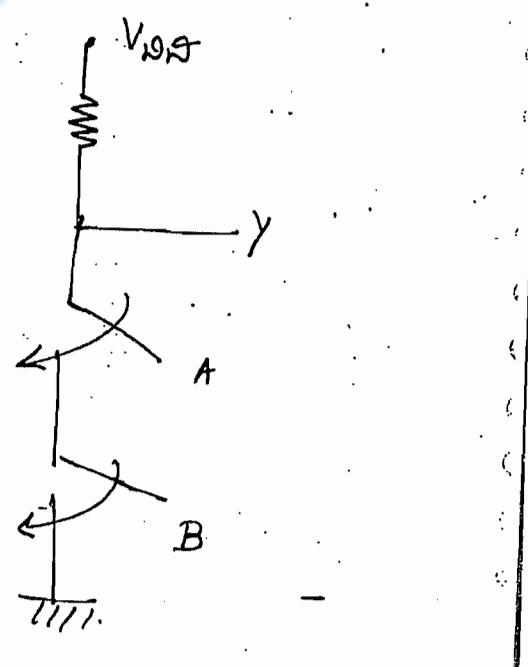


A	T <sub>1</sub>	Y
0	OFF	1 → $V_{DD} - V_T$
1	ON	0 → (0V)

NAND Gate :-

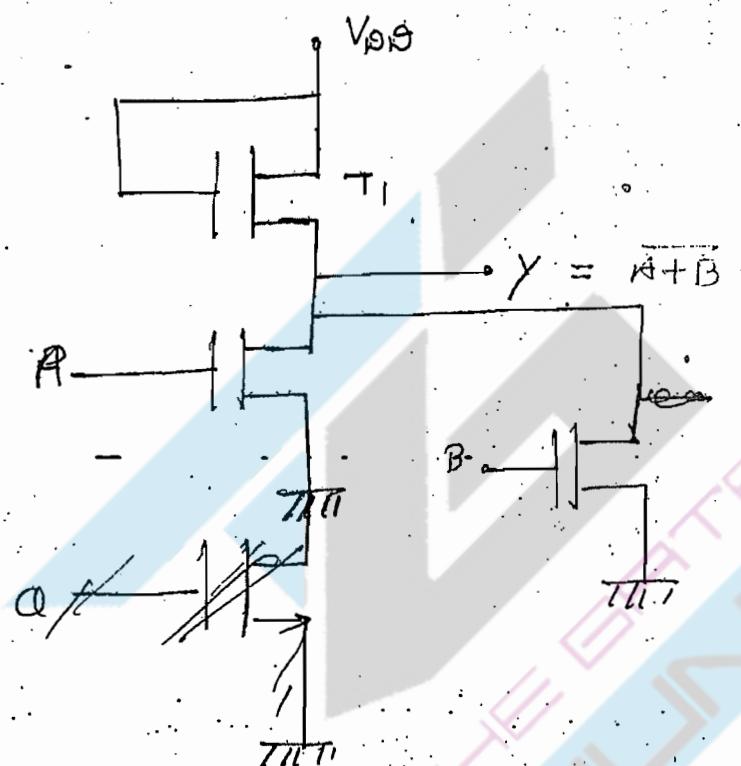


$$(V_{DD} - V_T)$$



A	B	$T_2$	$T_3$	Y
0	0.	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

NOR:-

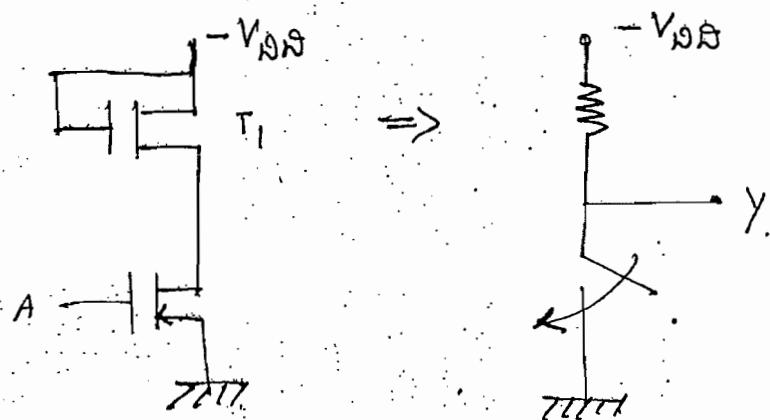


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NMOS:-

- $t_{pd} \Rightarrow 250\text{ ns}$  →  $P_{diss} = 1\text{ mW}$
- FOM  $\Rightarrow 250$  → fanout  $\rightarrow 5$
- NM  $= 1.5V$

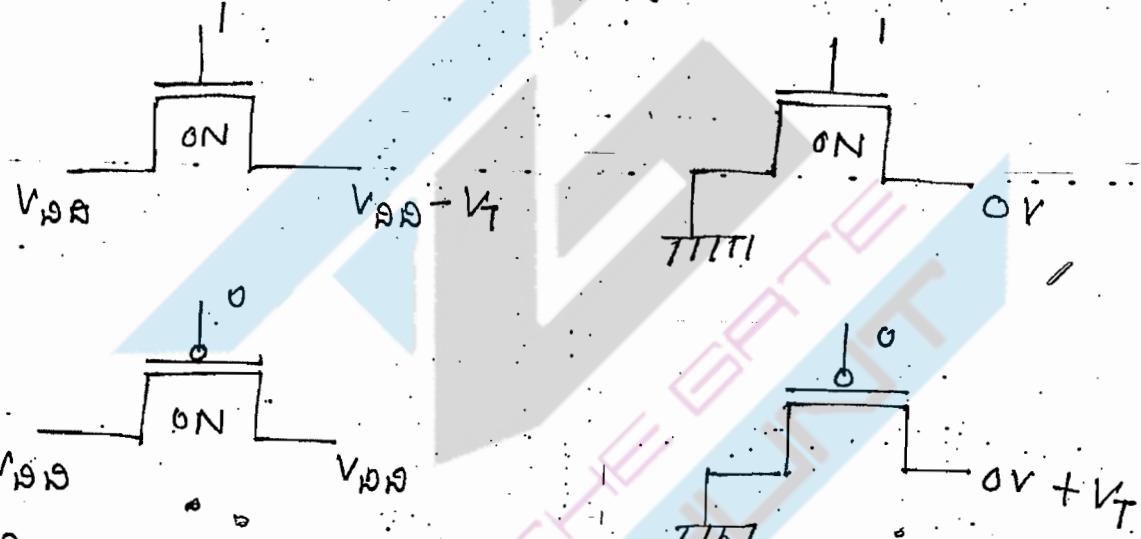
PMOS :-



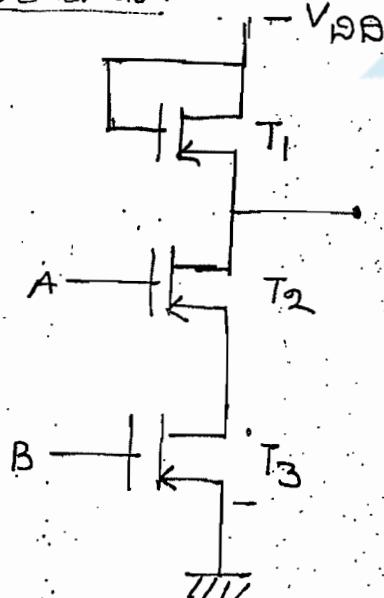
A	T <sub>2</sub>	O/P Voltage	Y
0	- ON	$GND (V_T)$	1
1	OFF	$-V_{DD}$	0

NMOS → Strong '0'  
Weak '1'

PMOS → Strong '1'  
Weak '0'



NOR  
NAND (CMOS) :-

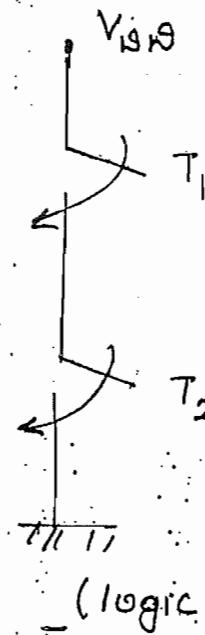
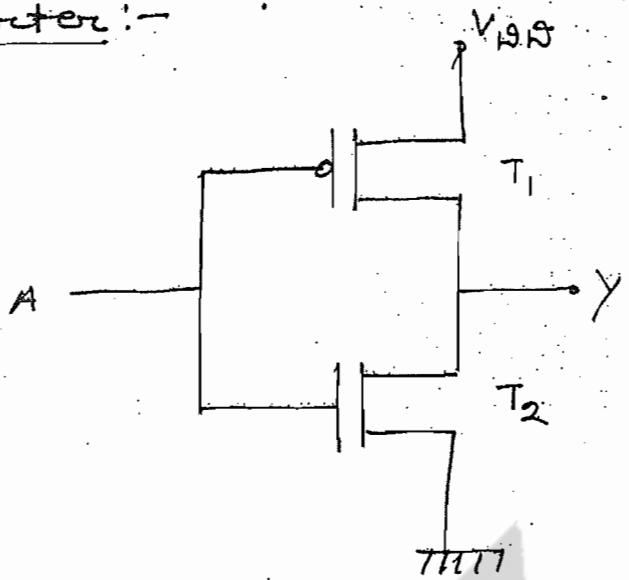


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

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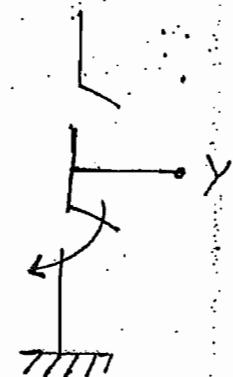
## CMOS :-

### Inverter :-



A	T <sub>1</sub>	T <sub>2</sub>	Y
0	ON	OFF	1 ( $V_{DD}$ )
1	OFF	ON	0 (0V)

Logic 1,



→ Lowest Power dissipation

$$P_{diss} = 0.01 \text{ mW}$$

→  $t_{pd} = 70 \text{ ns}$

→  $FOM = 0.7 \text{ PJ}$

→ fanout = 50

$$\rightarrow NM \approx \frac{V_{DD}}{2}$$

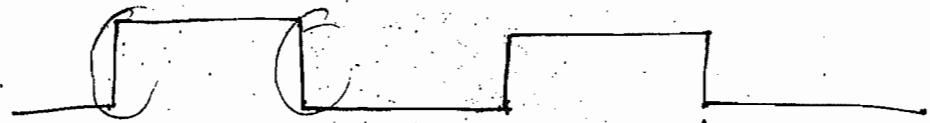
→ In CMOS there are two types of power dissipation (i) Static Power dissipation:-

↓

is present during logic 0 or logic 1 input

→ Dynamic Power dissipation:-

is present during 0 to 1 / 1 to 0 transition.

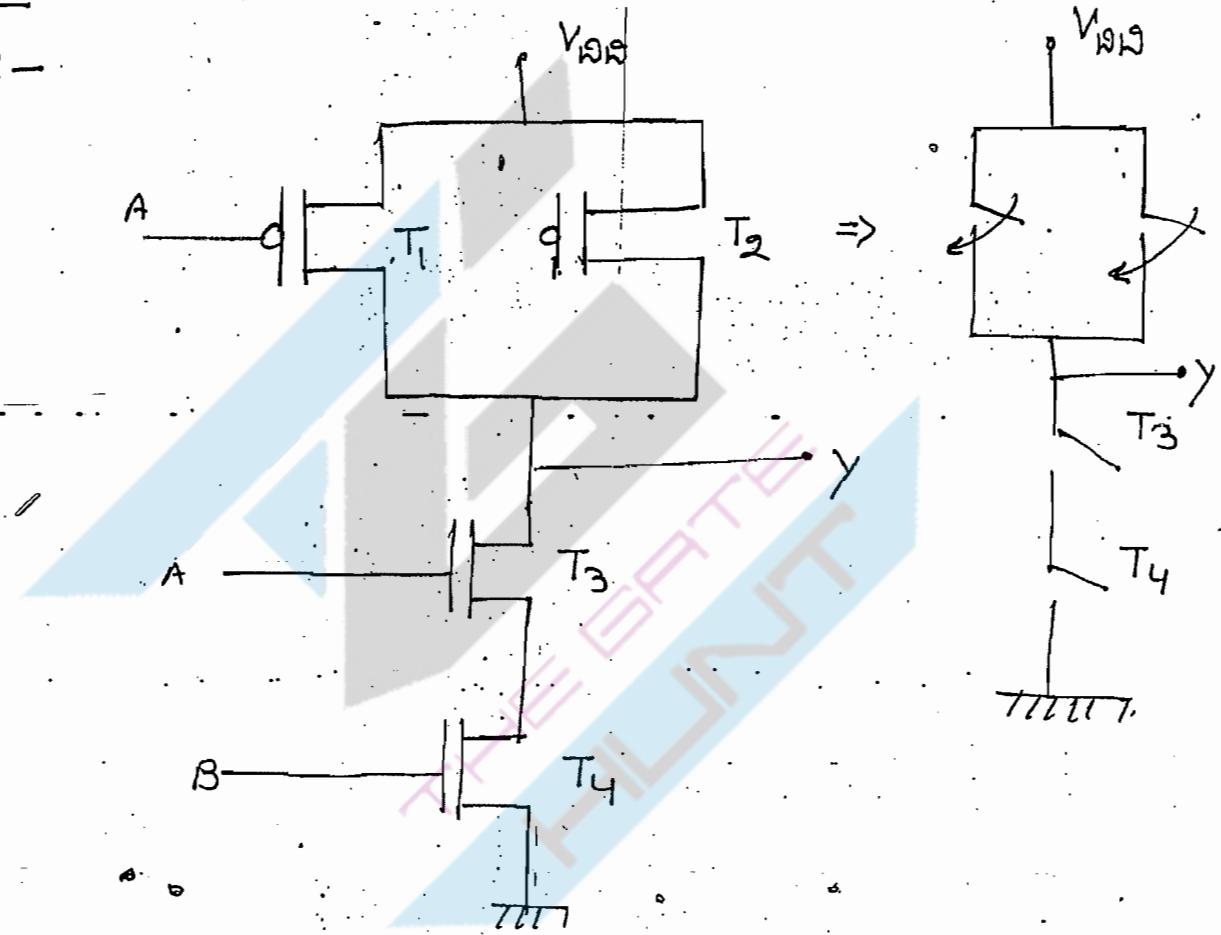


Dynamic Power diss

$$\text{Dynamic Power dissipation} = \frac{1}{2} C f V_{DD}^2$$

CMOS :-

NAND :-



A	B	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

CMOS :-

NAND

4

NOR

4

ANB

6

OR

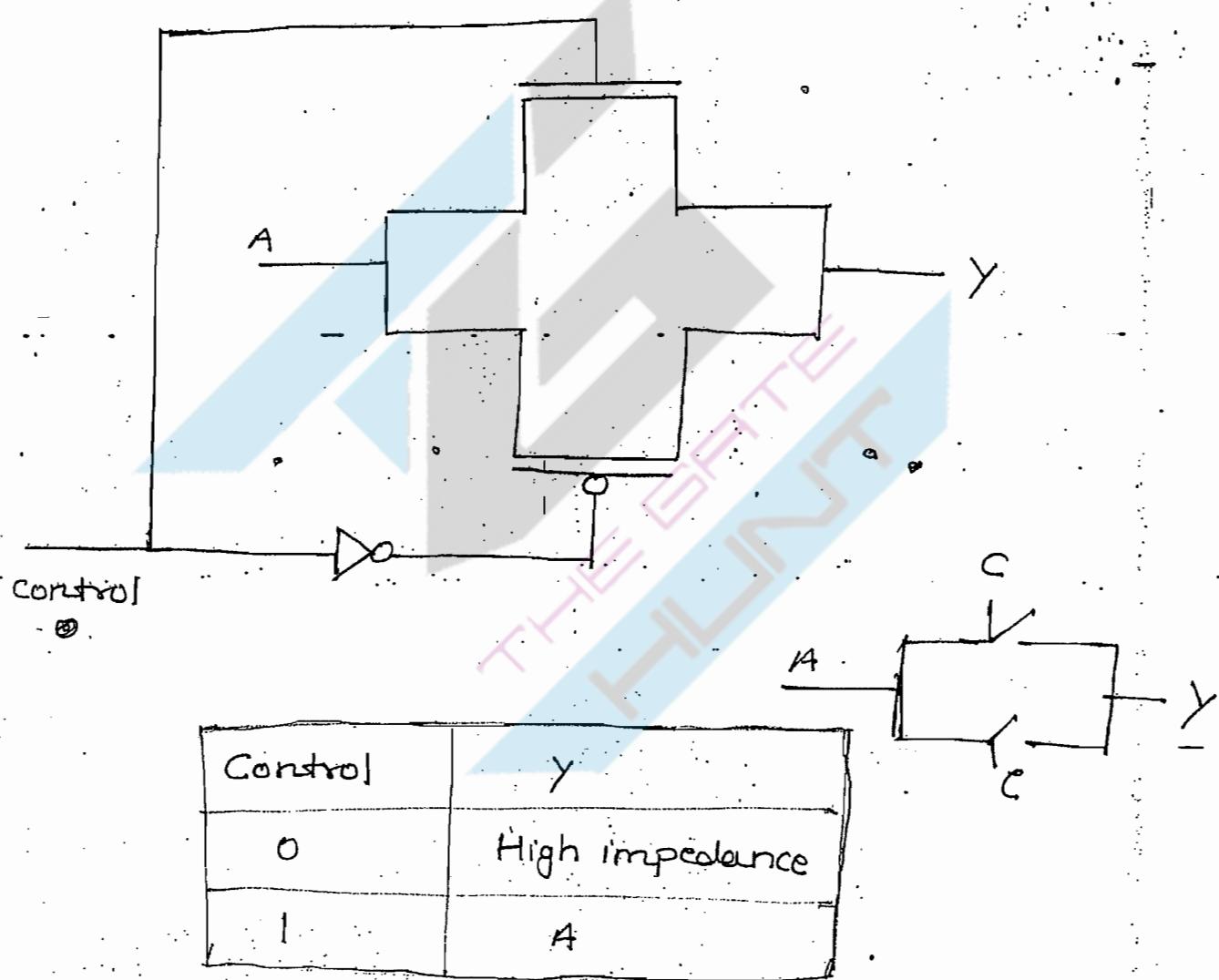
6

NOT

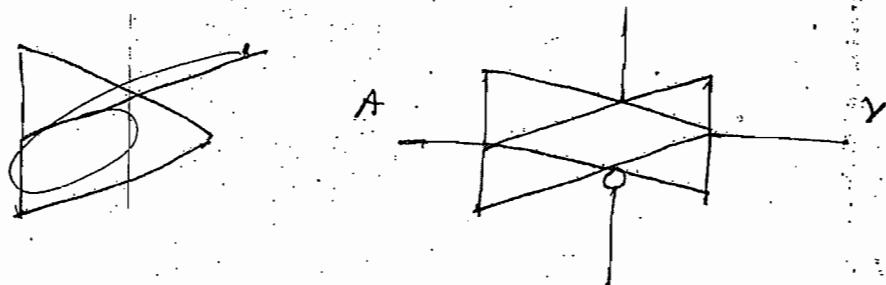
2

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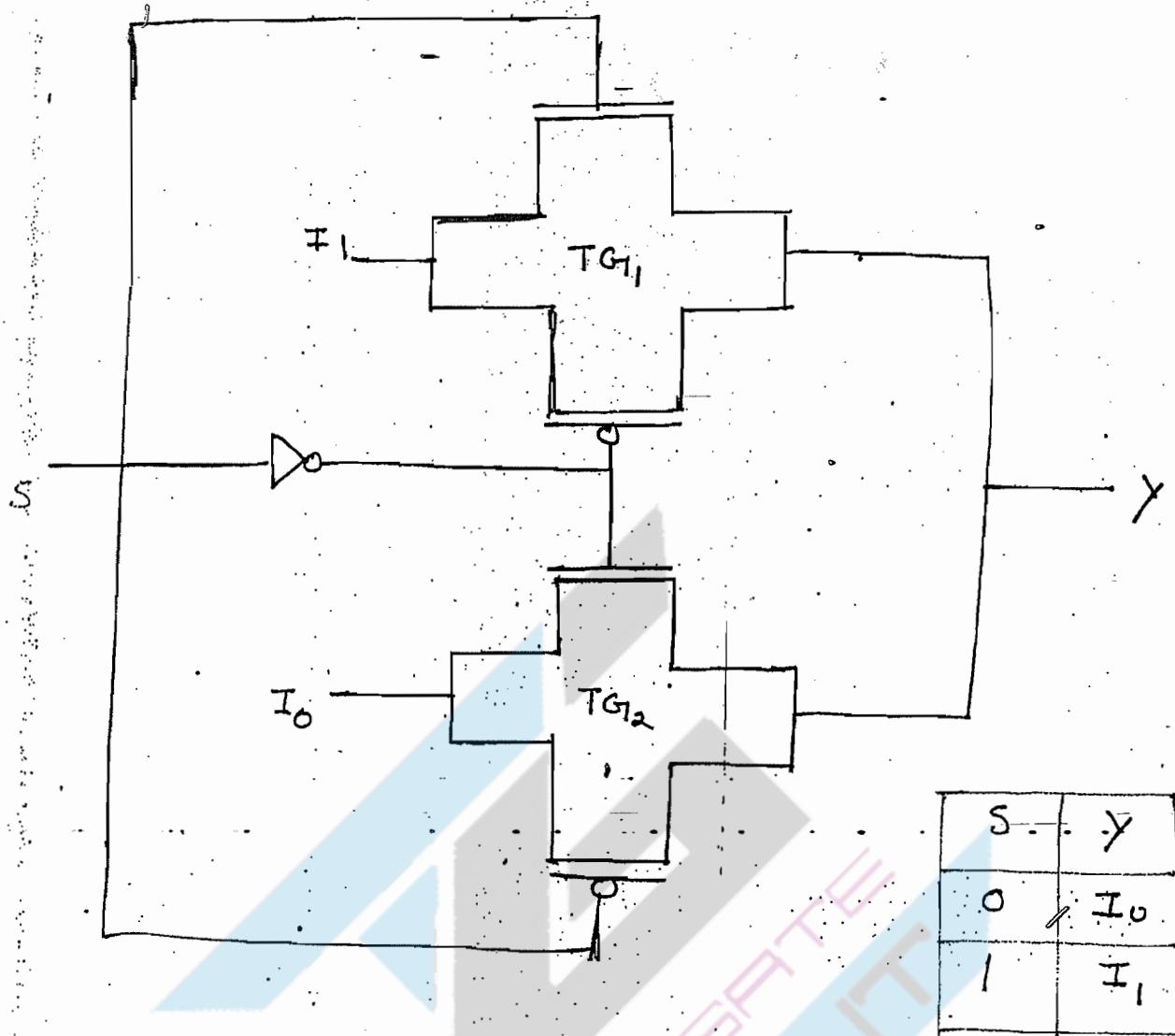
Transmission Gate :-



Symbol :-



Implement 2x1 MUX using Transmission Gate! -



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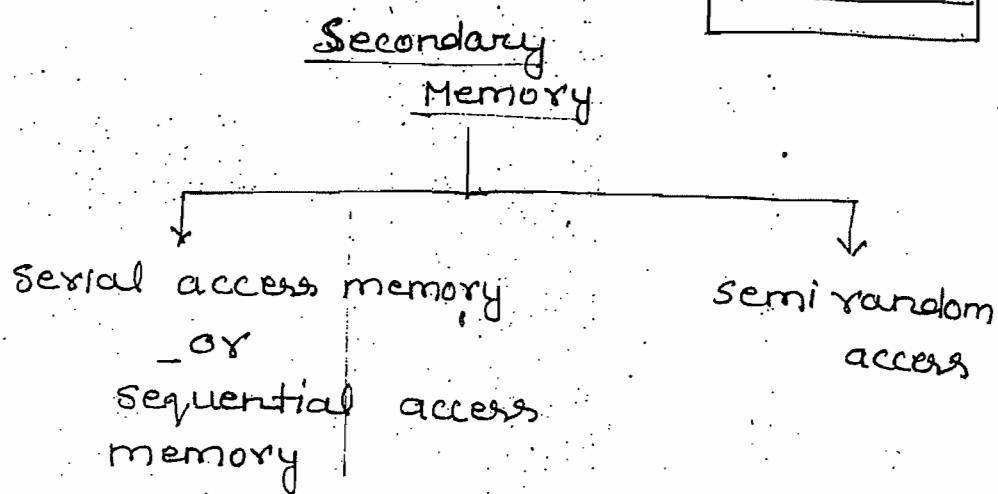
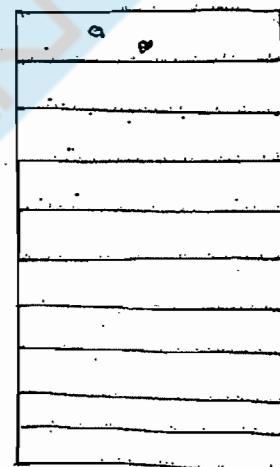
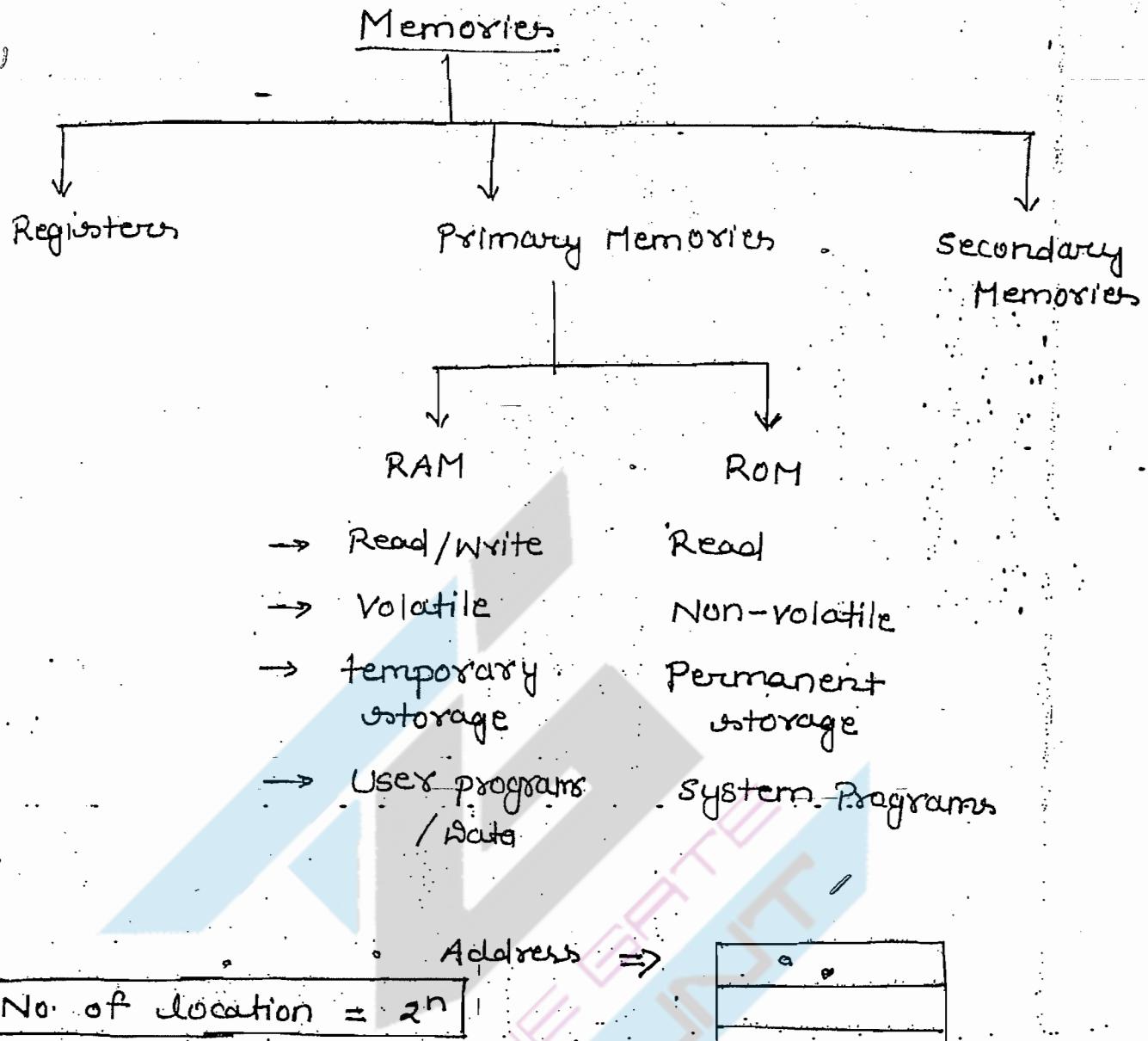
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## Serial Access Memory

eg:- Magnetic tape

→ Magnetic bubble

→ Ferrite core memory



Distributive Read out

## Semi Random Access

eg:- All disk memories

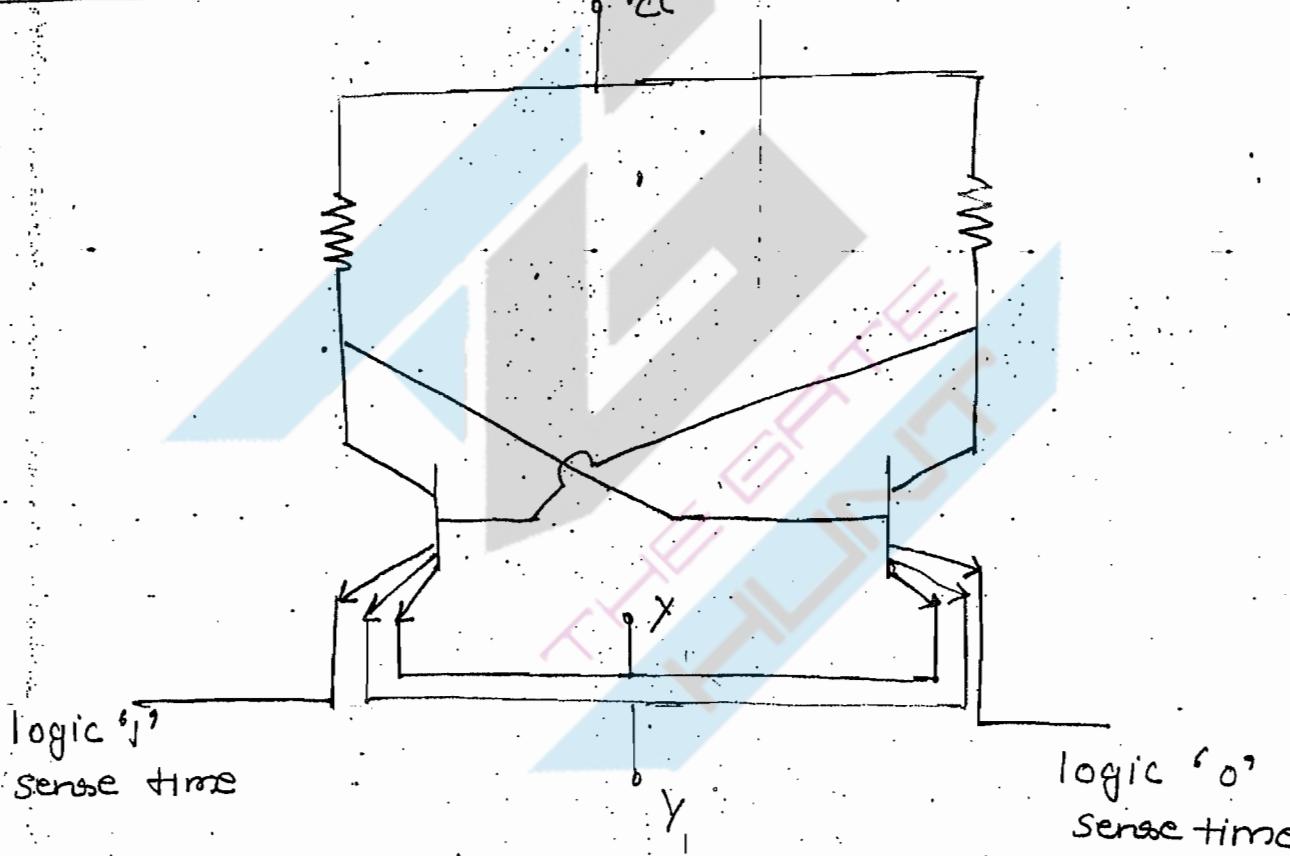


CD, DVD, HD

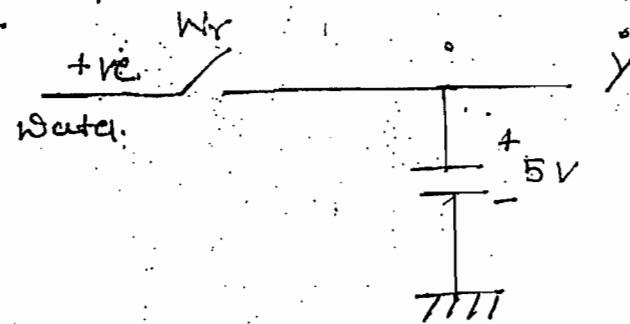
## RAM:-

### (I) Static RAM.

#### Static RAM:-



#### Dynamic RAM:-

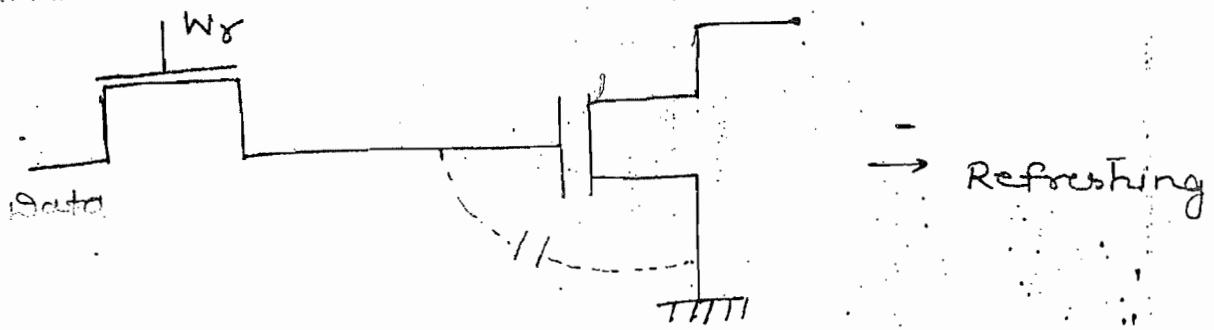


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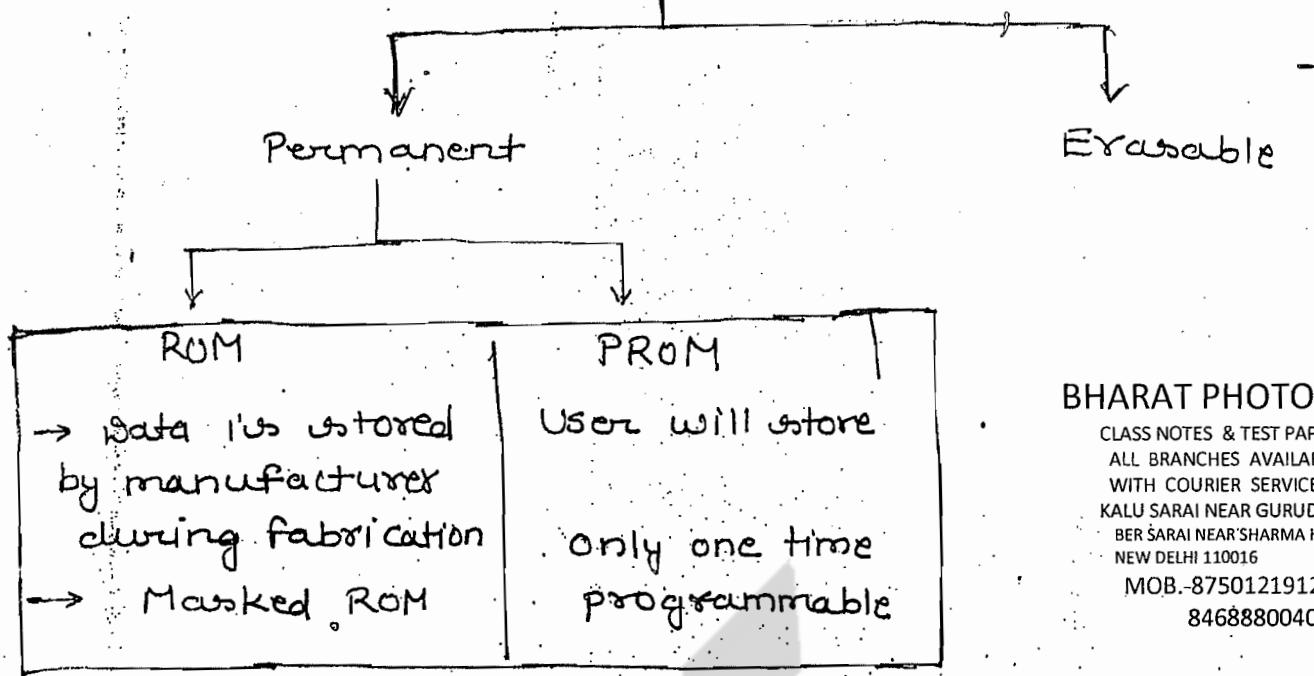
Static RAM	Dynamic RAM
1. Data is stored in cross coupled structure	Data is stored in MOS capacitor
2. BJT, MOSFET	MOSFET
3. Faster	Slower
4. Not dissipate more power	Dissipate less power
5. For storage of 1-bit, 6 transistors are required	1-bit $\Rightarrow$ 2 transistors
6. Memory capacity is less	Memory capacity is more
7. It is used as a cache memory	Used as a primary memory
8. No refreshing is req.	Refreshing is required (every 2ns)
9. Volatile	Volatile

### ROM:

- combinational circuit
- Decoder - Encoder
- AND  $\rightarrow$  OR
- Permanent programs

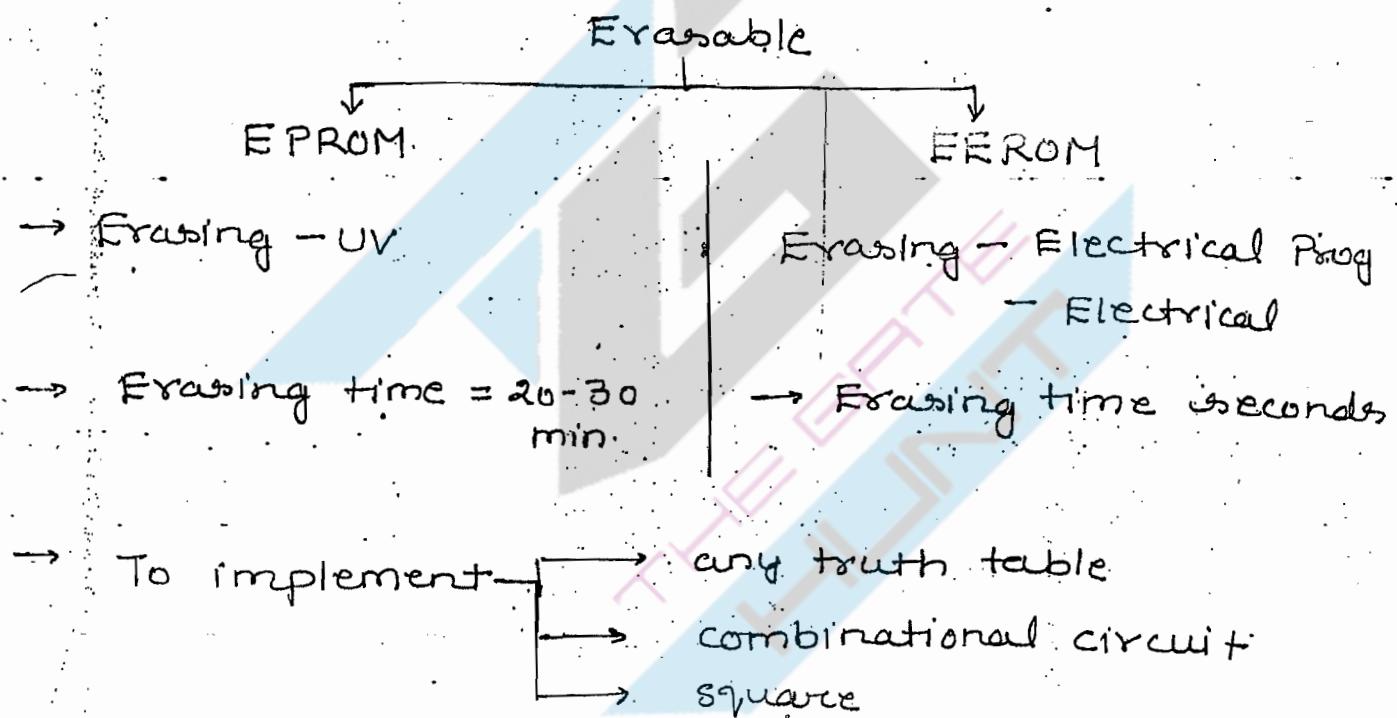
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# ROM



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Ques:- Implement following logic expression using ROM circuit.

$$Y_3(A, B, C) = \sum m(1, 3, 4, 7)$$

$$Y_2(A, B, C) = \sum m(0, 1, 4, 5)$$

$$Y_1(A, B, C) = \sum m(1, 3, 5, 6)$$

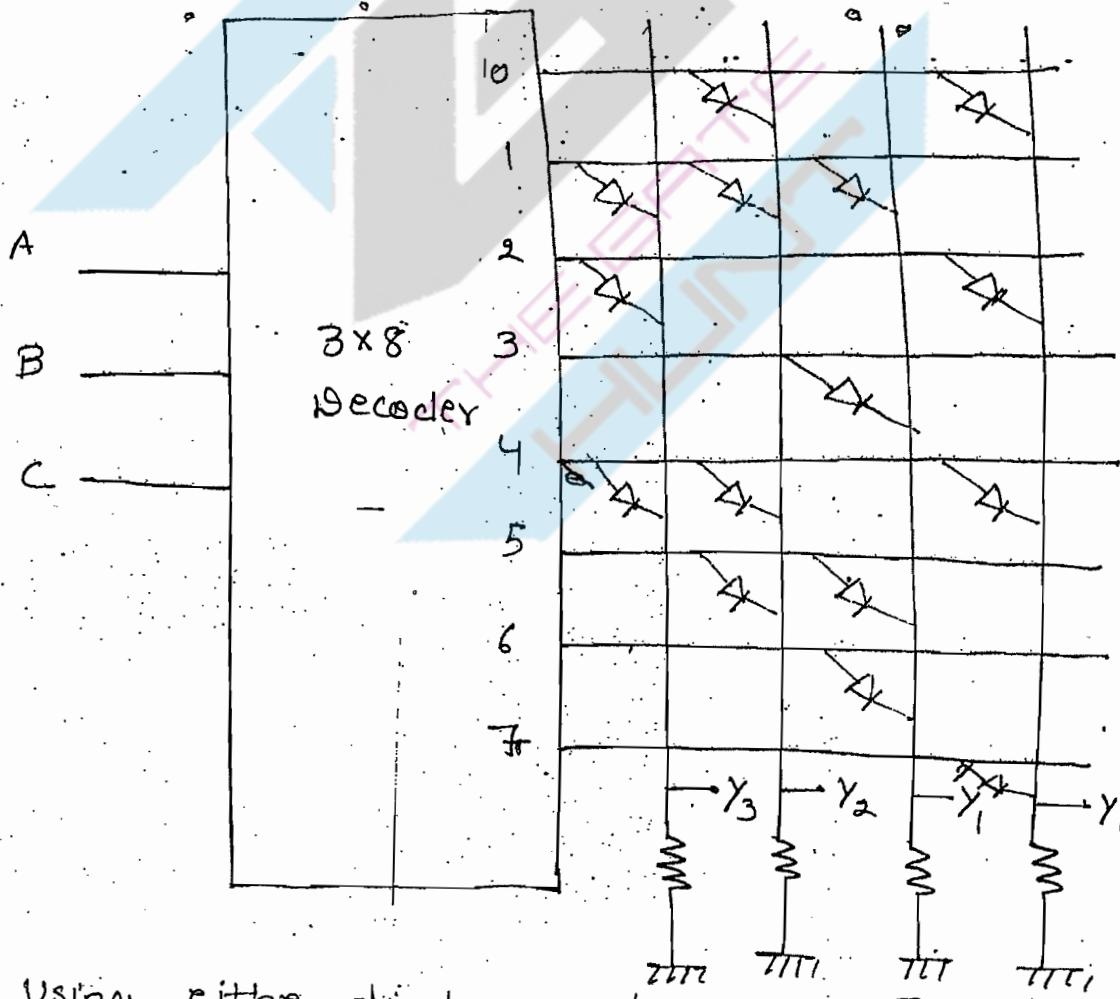
$$Y_0(A, B, C) = \sum m(0, 2, 4, 7)$$

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Truth Table

Data Bus

A	B	C		$y_3$	$y_2$	$y_1$	$y_0$
0	0	0		0	1	0	1
0	0	1		1	1	1	0
0	1	0		1	0	0	1
0	1	1		0	0	1	0
1	0	0		1	1	0	1
1	0	1	-	0	1	1	0
1	1	0		0	0	1	0
1	1	1		1	0	0	1



→ Using either diode  
or cross marks

Encoding

→ ROM	Fixed AND	Fixed OR
→ PROM	Fixed AND	Prog. OR
→ PAL	Prog. AND	Fixed OR
→ PLA	Prog. AND	Prog. OR

ques:- To implement 2-bits squaring function no. of address line and data lines used in ROM?

Soln:-

A	B	Add.	Data	Data
0	0	0	→ 0000	
0	1	1	→ 0001	
1	0	4	→ 0100	
1	1	9	→ 1001	

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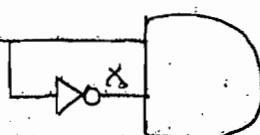
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Hazards :-

- Hazards are unwanted change in o/p due to propagation delay.

A



$$Y = A \cdot \bar{A} = 0$$

Sometimes it is 1  
due to propagation delay.

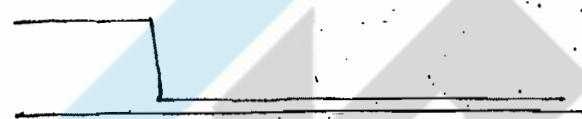
ques:- Draw o/p waveform for given i/p with no delay in logic gate

SOLN:- (i)

A



X



Y



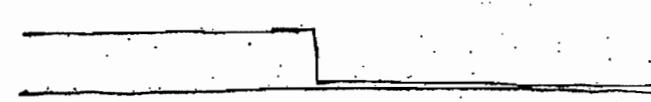
→ static '0'

(ii) Consider  $t_{pd\text{ Not}} = 1\text{ ns}$     $t_{pd\text{ AND}} = 0\text{ ns}$ 

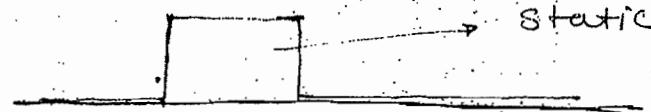
A



X



Y

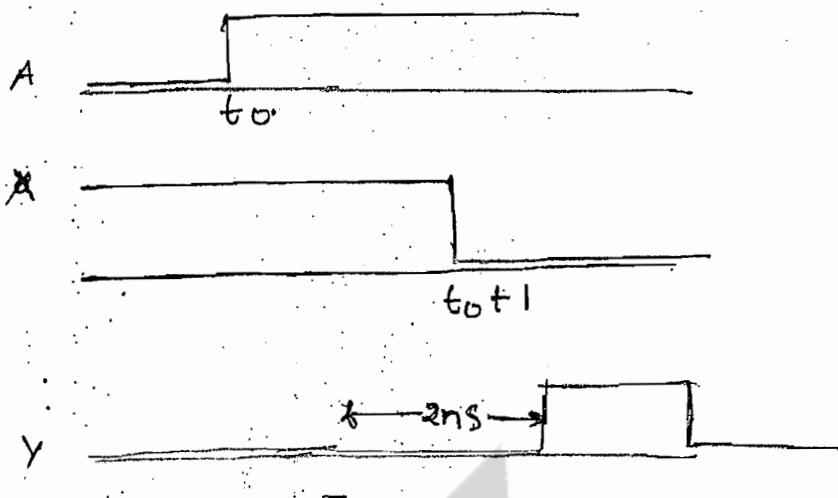


→ static '0' Hazard

(iii)  $t_{pd\ NUT} = 1\text{ ns}$

$t_{pd\ AND} = 2\text{ ns}$

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Hazard

Static  
↓  
occurs in  
two level  
combination

Static  
Hazard  
↓  
two level

AND - OR  
SOP

SOP

Dynamic  
↓  
Multi level  
comb

Static  
O

two level  
OR- AND

SOP

Essential  
↓  
Essential Hazard  
occurs in  
asynchronous,  
sequential

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→ Static and dynamic hazards can be avoided by

END OF DIGITAL CIRCUITS