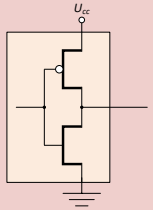
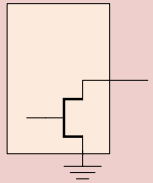
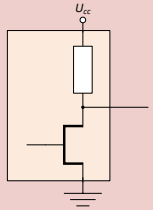
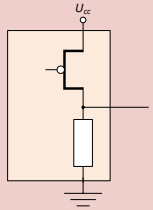
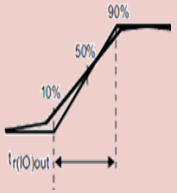
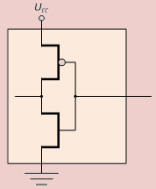
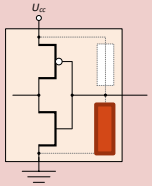
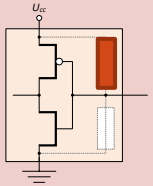
Osnove mikroprocesorske elektronike

Marko Jankovec

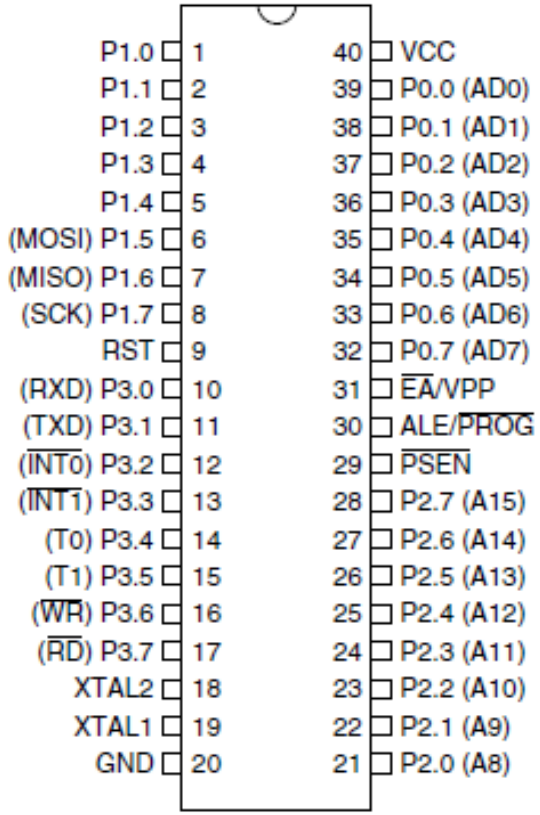
Vhodno-izhodne (I/O) linije

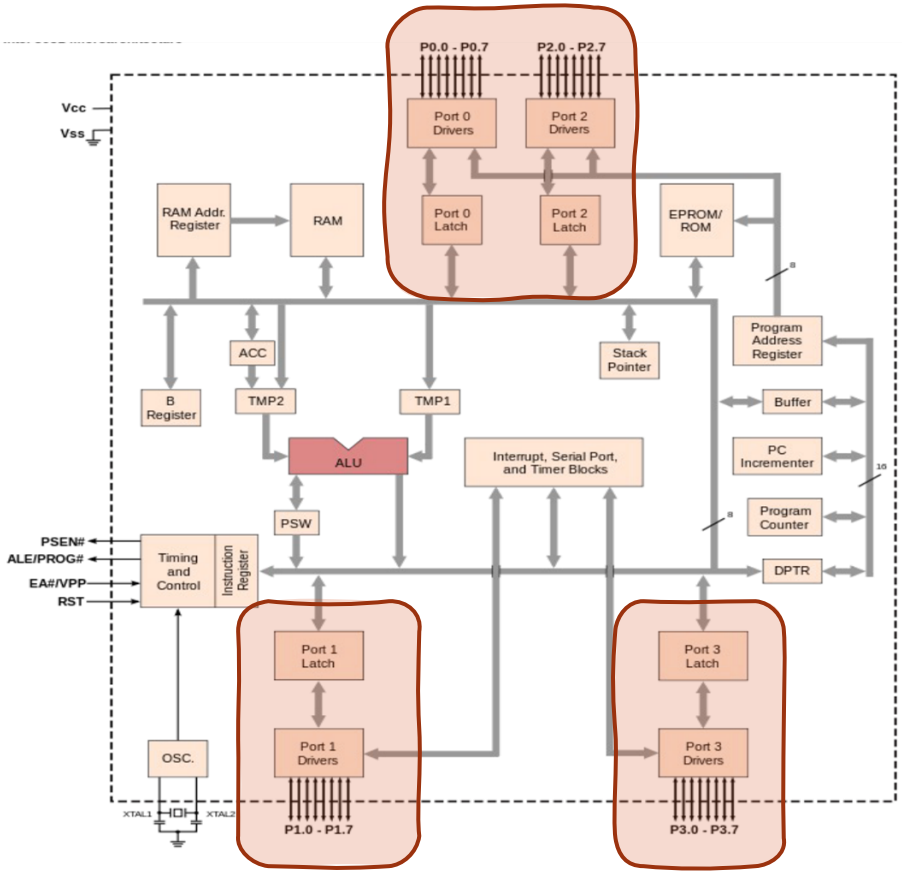
Primeri

Arhitekture I/O linij nekatrih mikrokrmilnikov

Družina	Izhod					Vhod		
	Simetrični 	Odprti ponor 	Zgornji upor 	Spodnji upor 	Dvižni čas 	HiZ 	Spodnji upor 	Zgornji upor 
Intel 8051			✓					✓
Atmel AVR	✓					✓		✓
Microchip PIC	✓	✓	✓		✓	✓		✓
Ti MSP430	✓					✓	✓	✓
ARM STM32	✓	✓	✓	✓	✓	✓	✓	✓

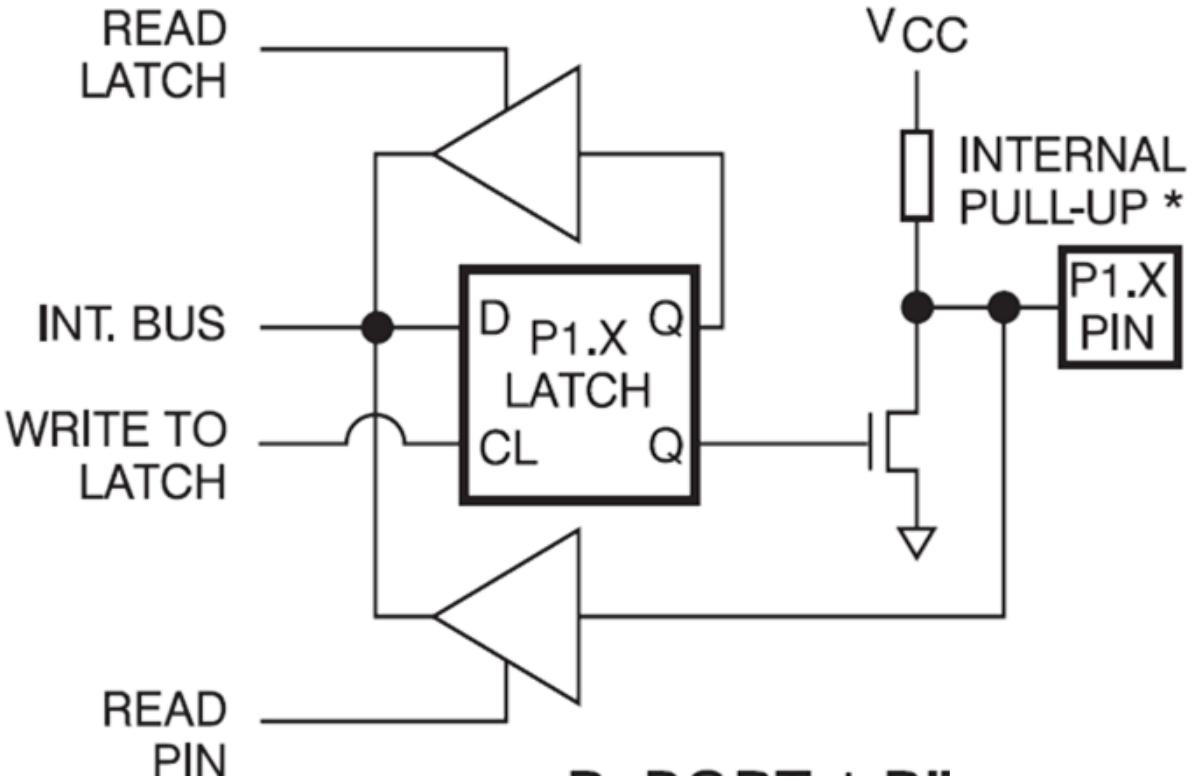
Intel 8051


P1.0 1
P1.1 2
P1.2 3
P1.3 4
P1.4 5
(MOSI) P1.5 6
(MISO) P1.6 7
(SCK) P1.7 8
RST 9
(RXD) P3.0 10
(TXD) P3.1 11
(INT0) P3.2 12
(INT1) P3.3 13
(T0) P3.4 14
(T1) P3.5 15
(WR) P3.6 16
(RD) P3.7 17
XTAL2 18
XTAL1 19
GND 20
40 VCC
39 P0.0 (AD0)
38 P0.1 (AD1)
37 P0.2 (AD2)
36 P0.3 (AD3)
35 P0.4 (AD4)
34 P0.5 (AD5)
33 P0.6 (AD6)
32 P0.7 (AD7)
31 EA/VPP
30 ALE/PROG
29 PSEN
28 P2.7 (A15)
27 P2.6 (A14)
26 P2.5 (A13)
25 P2.4 (A12)
24 P2.3 (A11)
23 P2.2 (A10)
22 P2.1 (A9)
21 P2.0 (A8)

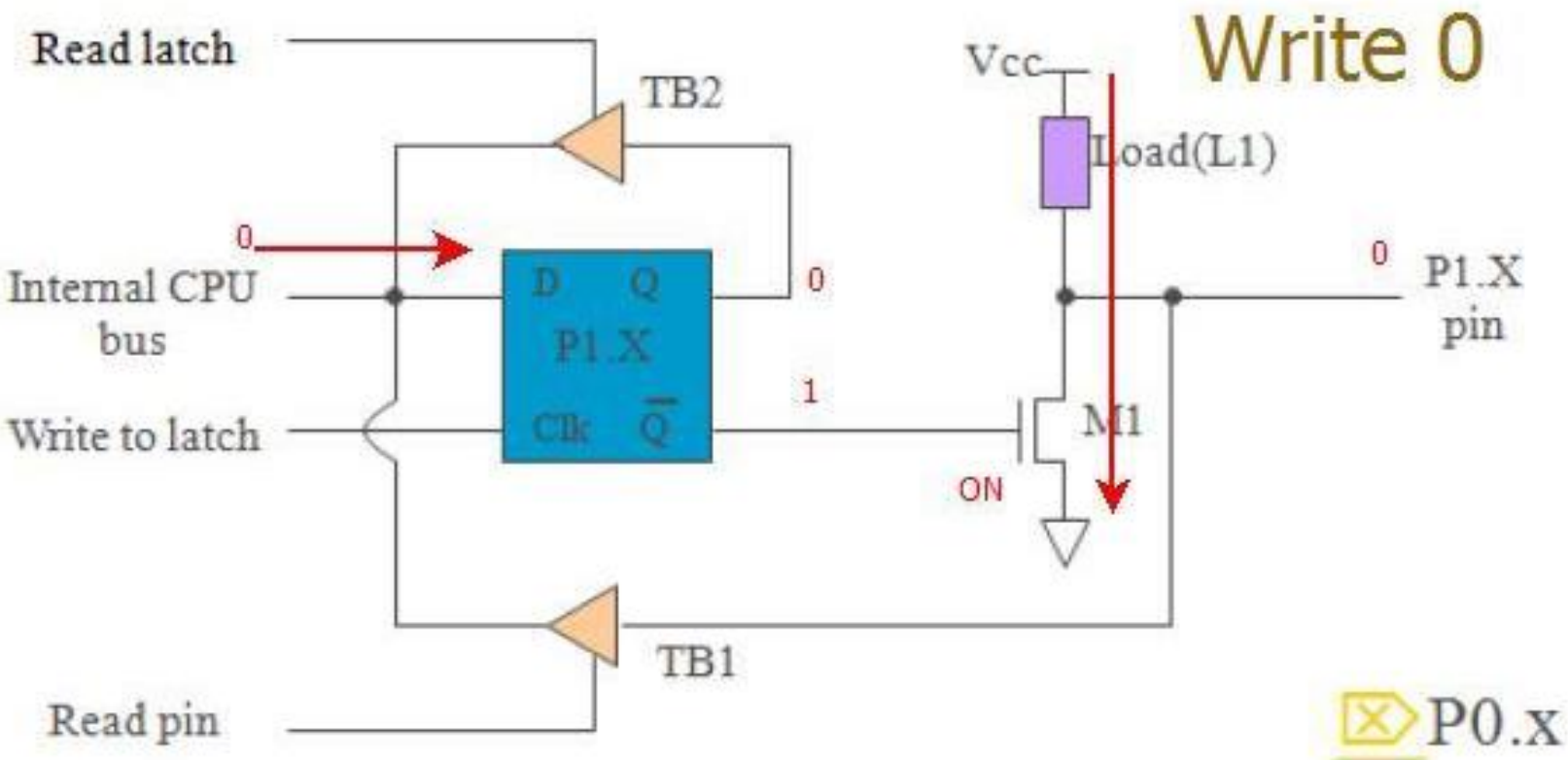

P0.0 - P0.7
P2.0 - P2.7
Vcc
Vss
Port 0 Drivers
Port 2 Drivers
RAM Addr. Register
RAM
Port 0 Latch
Port 2 Latch
EPROM/ ROM
Program Address Register
ACC
Stack Pointer
B Register
TMP2
TMP1
Buffer
ALU
Interrupt, Serial Port, and Timer Blocks
PC Incrementer
PSW
Program Counter
PSEN#
ALE/PROG#
EA#/VPP
RST
Timing and Control
Instruction Register
DPTR
Port 1 Latch
Port 3 Latch
OSC.
Port 1 Drivers
Port 3 Drivers
XTAL1
XTAL2
P1.0 - P1.7
P3.0 - P3.7

Arhitektura splošnega I/O priključka pri Intel 8051

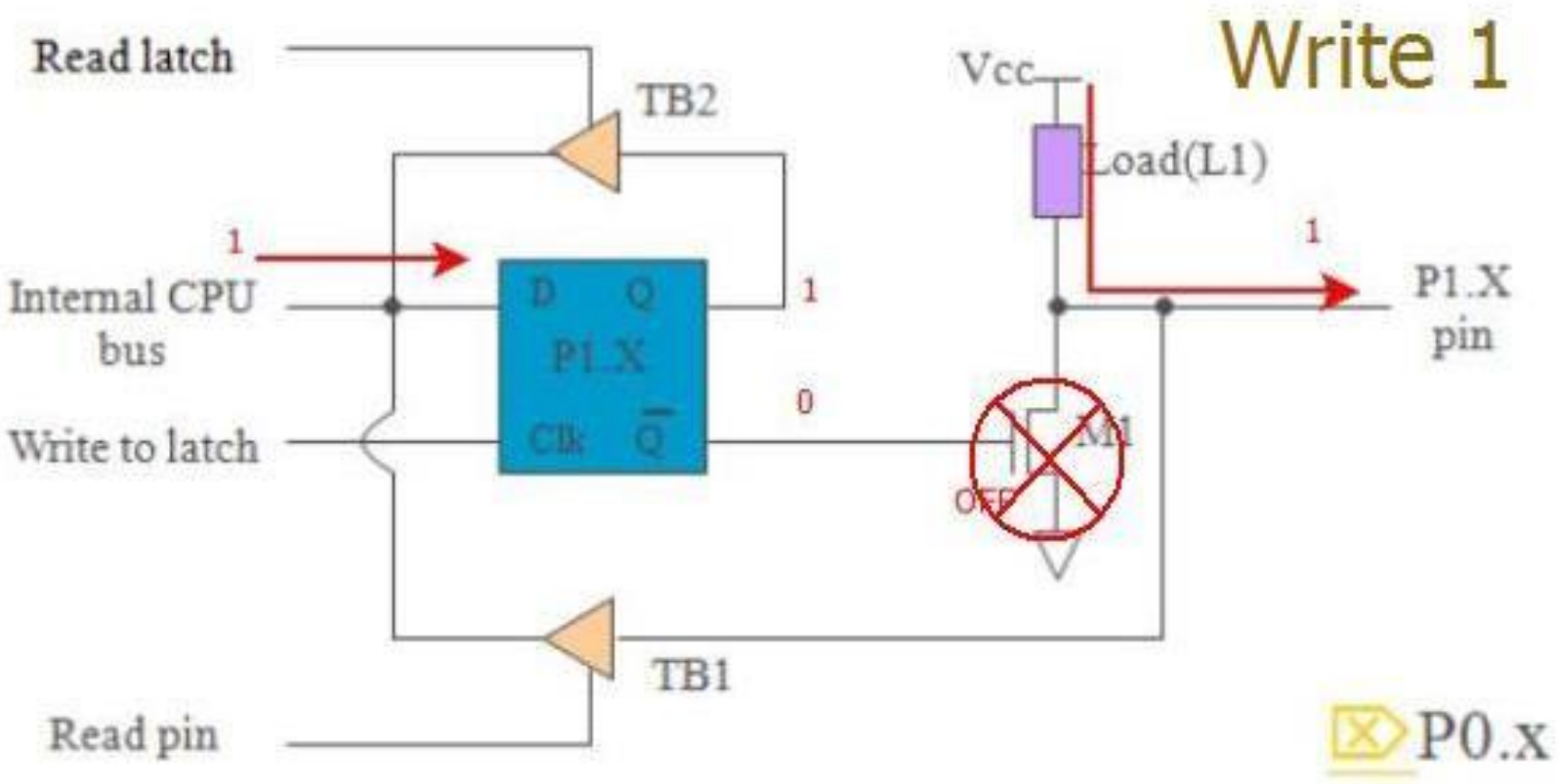
- Vsak vhod je hkrati tudi izhod
- Stalno vključen zgornji upor



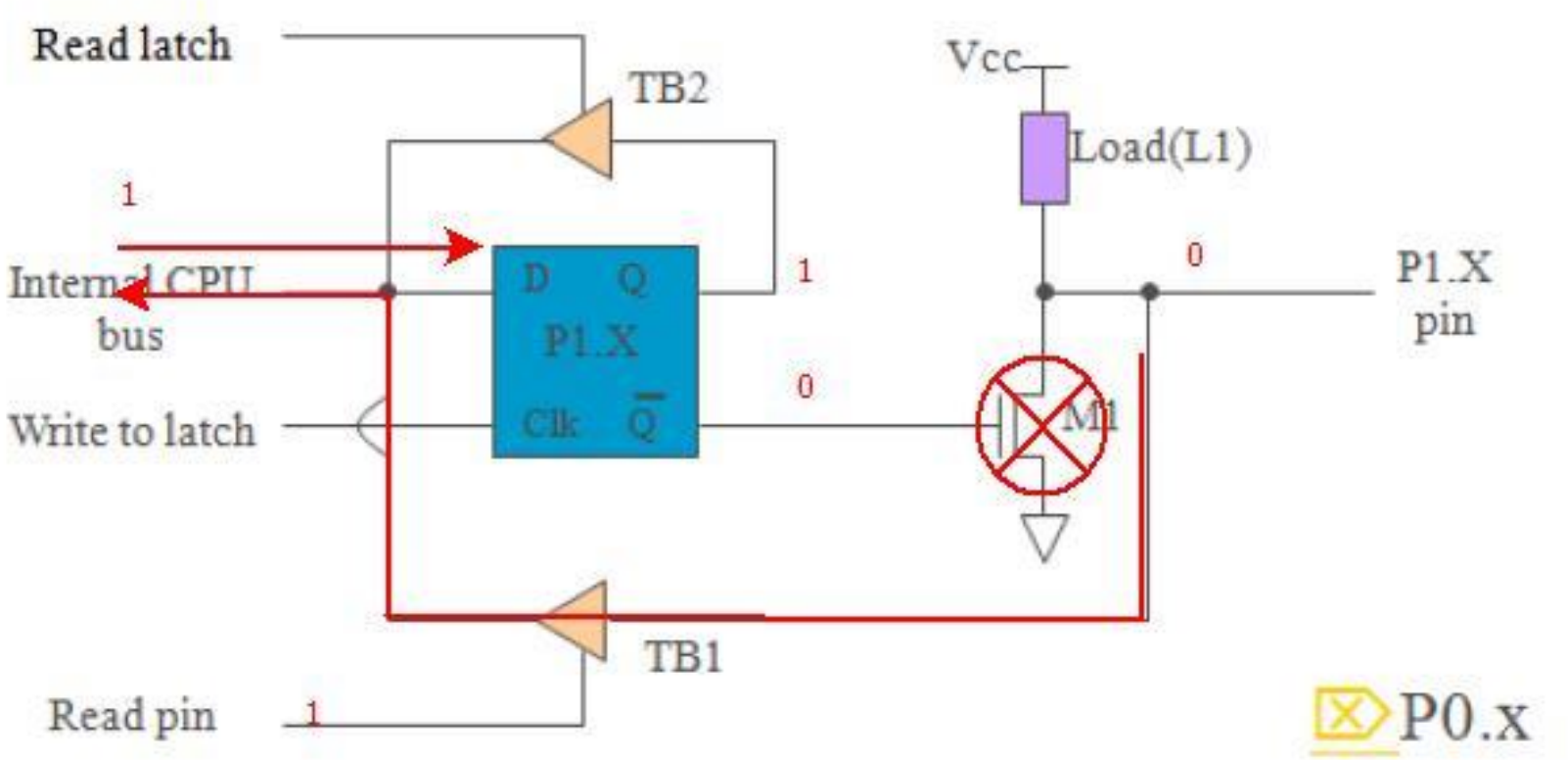
Pisanje “0”


Read latch
TB2
Vcc
Write 0
Load(L1)
0
Internal CPU bus
D
Q
P1.X
0
0
P1.X pin
1
Write to latch
Clk
Q
M1
ON
TB1
Read pin
P0.x

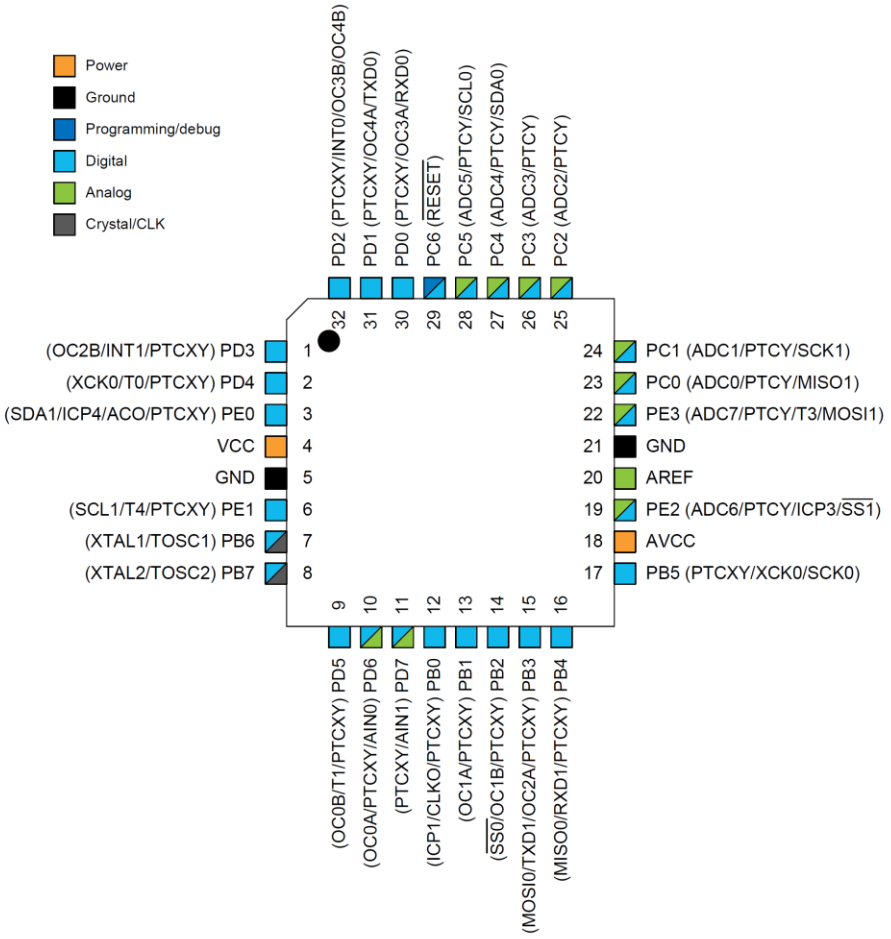
Pisanje “1”

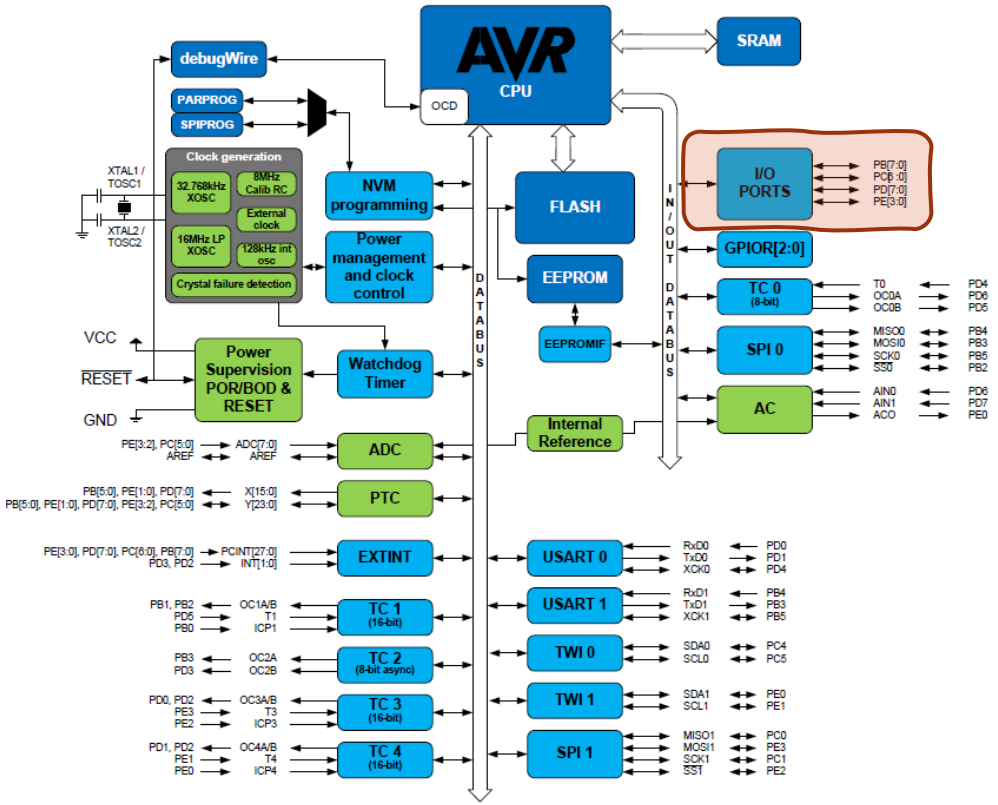

Write 1
Read latch
TB2
Vcc
Load(L1)
1
Internal CPU bus
D
Q
P1.X
1
0
Write to latch
Clk
Q
M1
OFF
P1.X pin
TB1
Read pin
P0.x

Branje

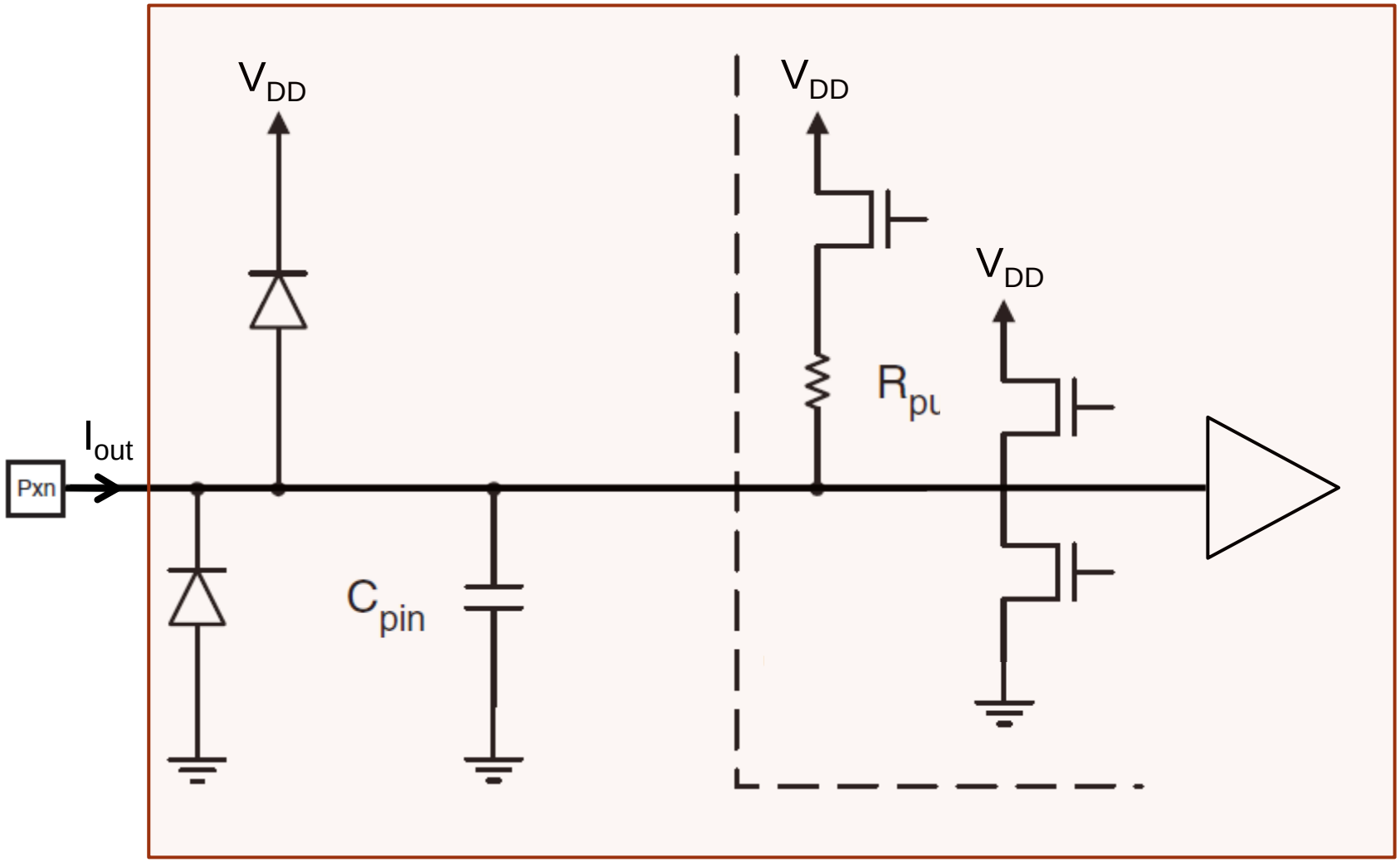

Read latch
TB2
Vcc
Load(L1)
1
Internal CPU bus
D
Q
P1.X
1
0
P1.X pin
Write to latch
Clk
Q
M1
TB1
Read pin
1
P0.x

Atmel AVR

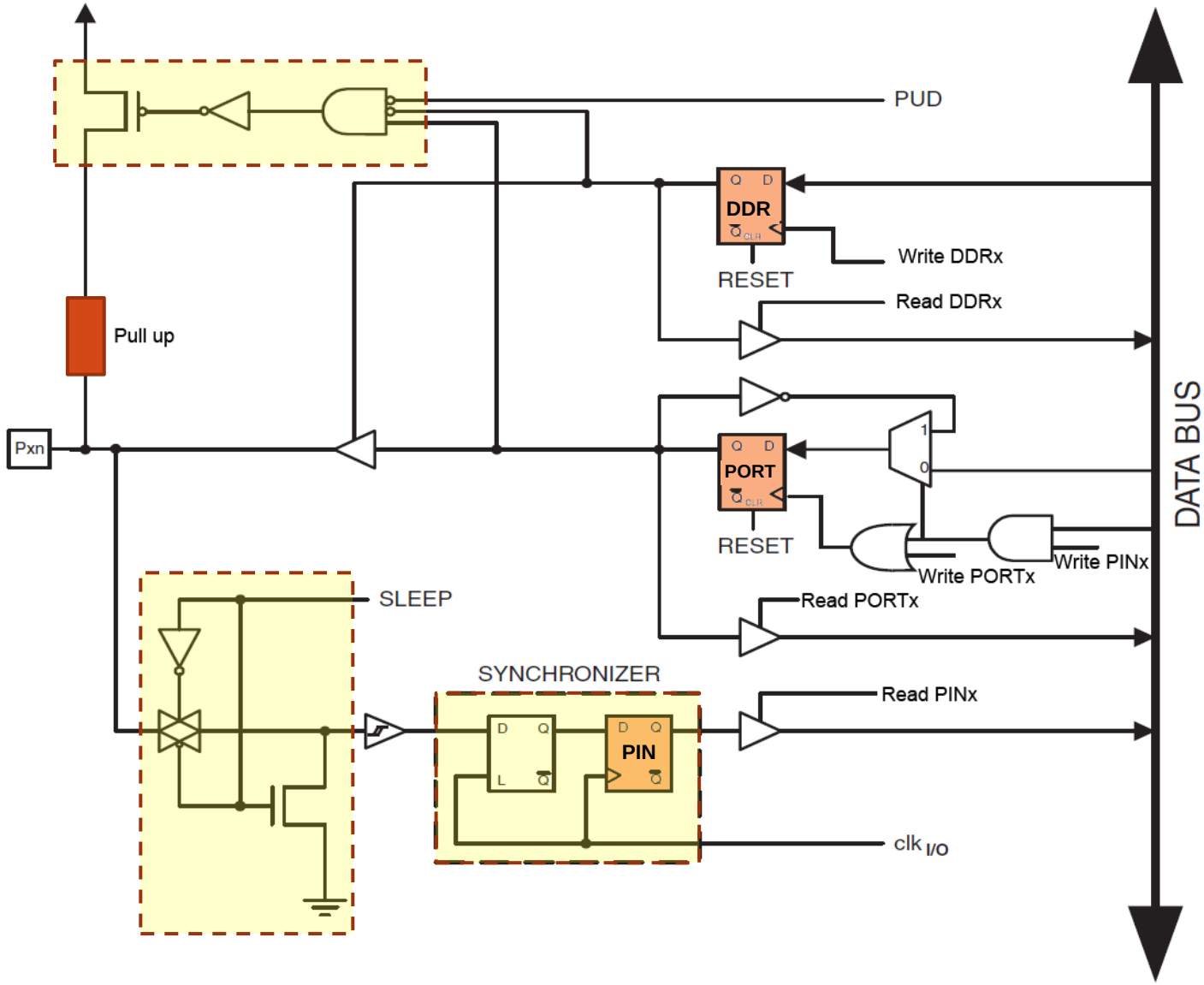

Power
Ground
Programming/debug
Digital
Analog
Crystal/CLK
PD2 (PTCXY/INT0/OC3B/OC4B)
PD1 (PTCXY/OC4A/TXD0)
PD0 (PTCXY/OC3A/RXD0)
PC6 (RESET)
PC5 (ADC5/PTCY/SCL0)
PC4 (ADC4/PTCY/SDA0)
PC3 (ADC3/PTCY)
PC2 (ADC2/PTCY)
32
31
30
29
28
27
26
25
(OC2B/INT1/PTCXY) PD3 1
(XCK0/T0/PTCXY) PD4 2
(SDA1/ICP4/ACO/PTCXY) PE0 3
VCC 4
GND 5
(SCL1/T4/PTCXY) PE1 6
(XTAL1/TOSC1) PB6 7
(XTAL2/TOSC2) PB7 8
24 PC1 (ADC1/PTCY/SCK1)
23 PC0 (ADC0/PTCY/MISO1)
22 PE3 (ADC7/PTCY/T3/MOSI1)
21 GND
20 AREF
19 PE2 (ADC6/PTCY/ICP3/SS1)
18 AVCC
17 PB5 (PTCXY/XCK0/SCK0)
9
10
11
12
13
14
15
16
(OC0B/T1/PTCXY) PD5
(OC0A/PTCXY/AIN0) PD6
(PTCXY/AIN1) PD7
(ICP1/CLKO/PTCXY) PB0
(OC1A/PTCXY) PB1
(SS0/OC1B/PTCXY) PB2
(MOSI0/TXD1/OC2A/PTCXY) PB3
(MISO0/RXD1/PTCXY) PB4


AVR
CPU
SRAM
debugWire
PARPROG
SPIPROG
OCD
Clock generation
32.768kHz XOSC
8MHz Calib RC
External clock
16MHz LP XOSC
128kHz int osc
Crystal failure detection
XTAL1 / TOSC1
XTAL2 / TOSC2
NVM programming
Power management and clock control
FLASH
EEPROM
EEPROMIF
Internal Reference
I/O PORTS
GPIOR[2:0]
TC 0 (8-bit)
SPI 0
AC
Power Supervision POR/BOD & RESET
Watchdog Timer
VCC
RESET
GND
ADC
PTC
EXTINT
TC 1 (16-bit)
TC 2 (8-bit async)
TC 3 (16-bit)
TC 4 (16-bit)
USART 0
USART 1
TWI 0
TWI 1
SPI 1
DATABUS
I/O DATABUS

Arhitektura splošnega I/O priključka pri AVR



Arhitektura splošnega I/O priključka pri AVR



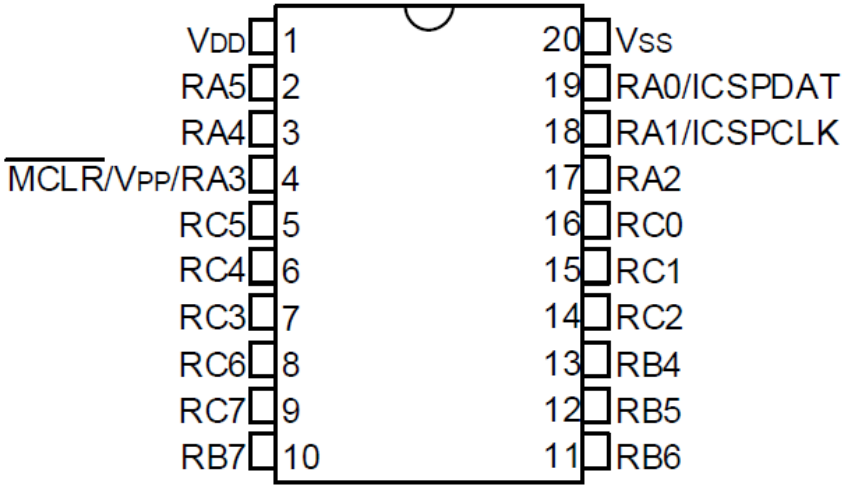
Logična tabela nastavitev I/O linije

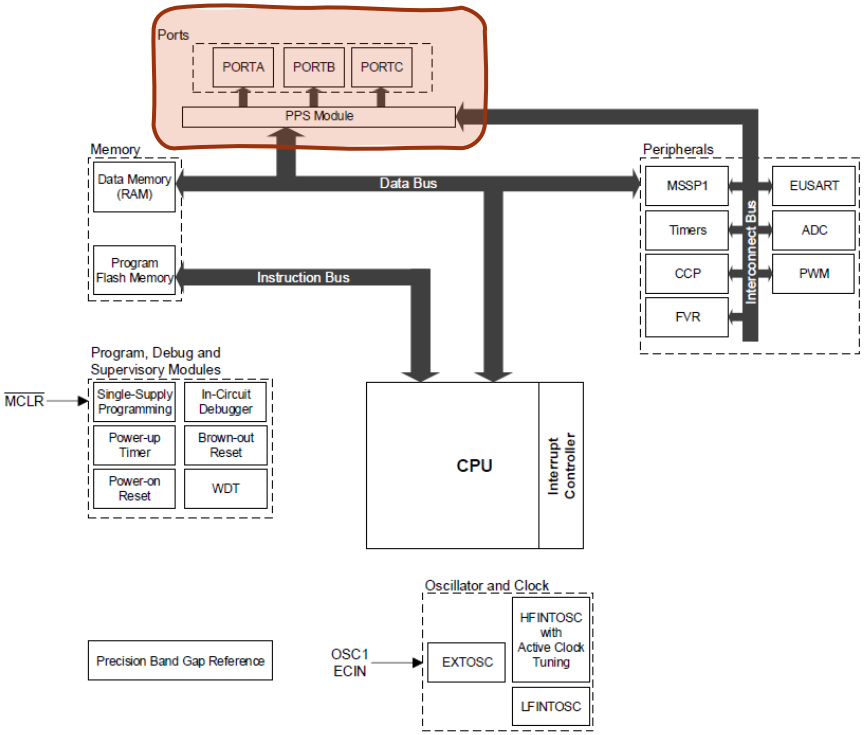
DDRxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

- x – se nanaša na port (A, B, C, …)
- n – se nanaša na linijo v portu (0,1,…,7)

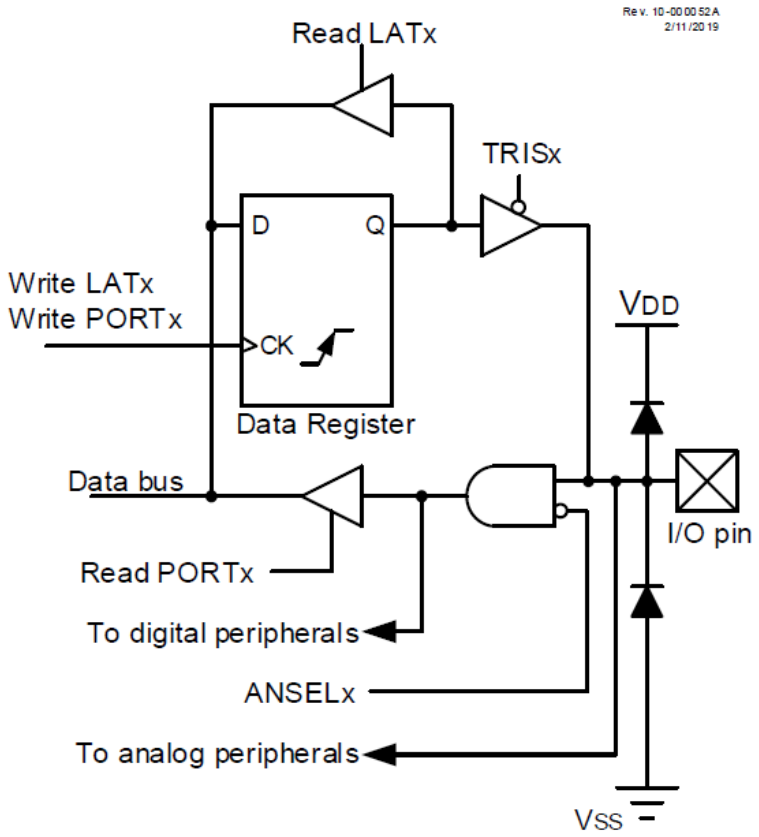
- Vpis logične „1“ v register PINxn negira vrednost registra PORTxn, ne glede na vrednost DDRxn

Microchip PIC



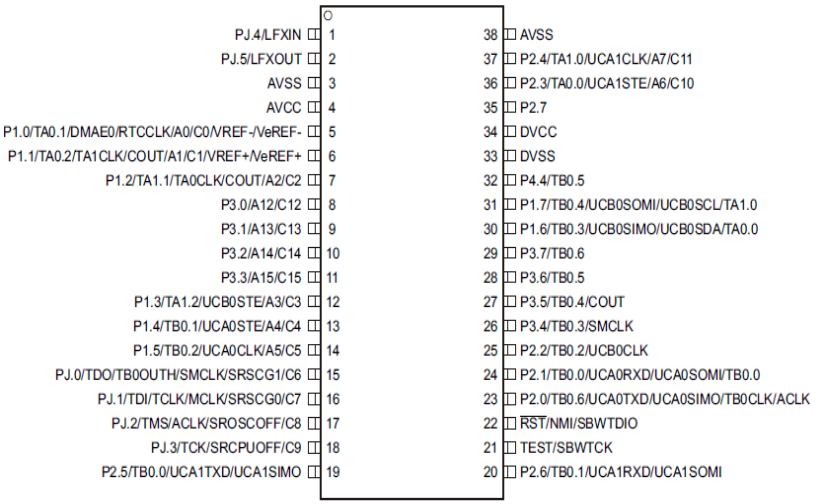


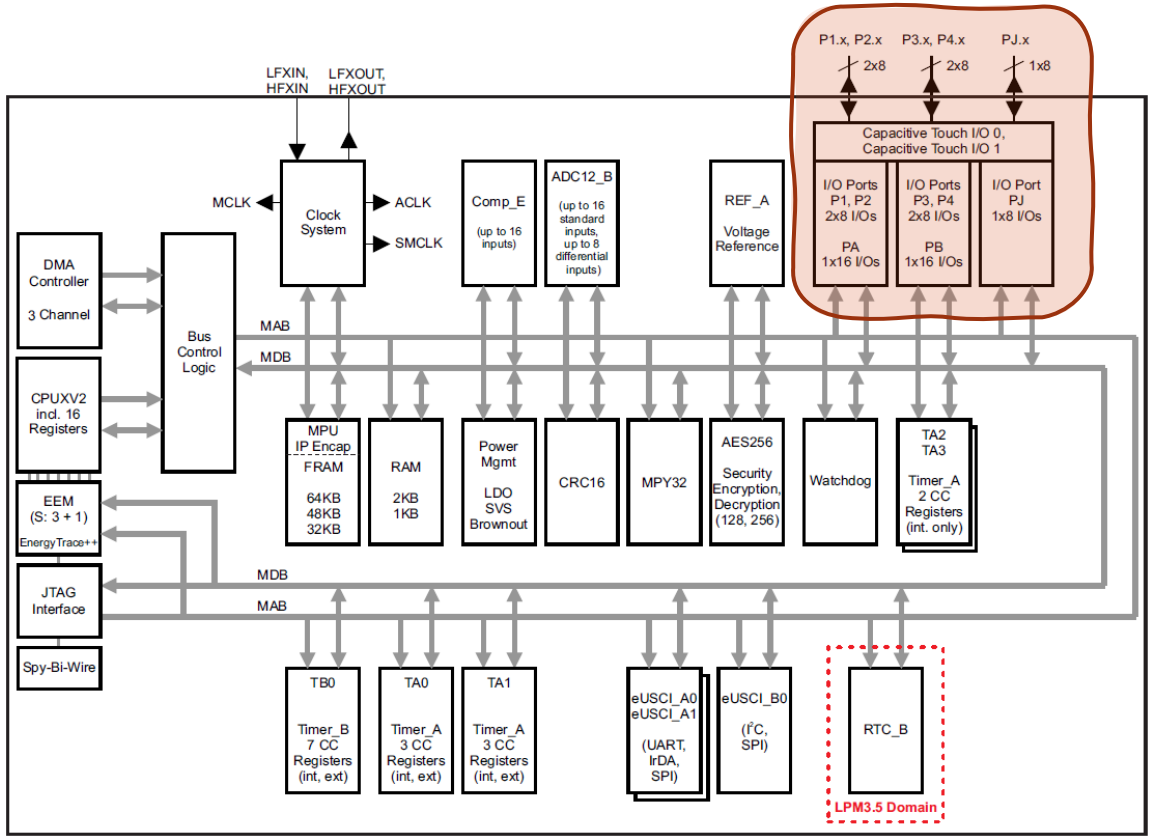
Arhitektura splošnega I/O priključka pri PIC



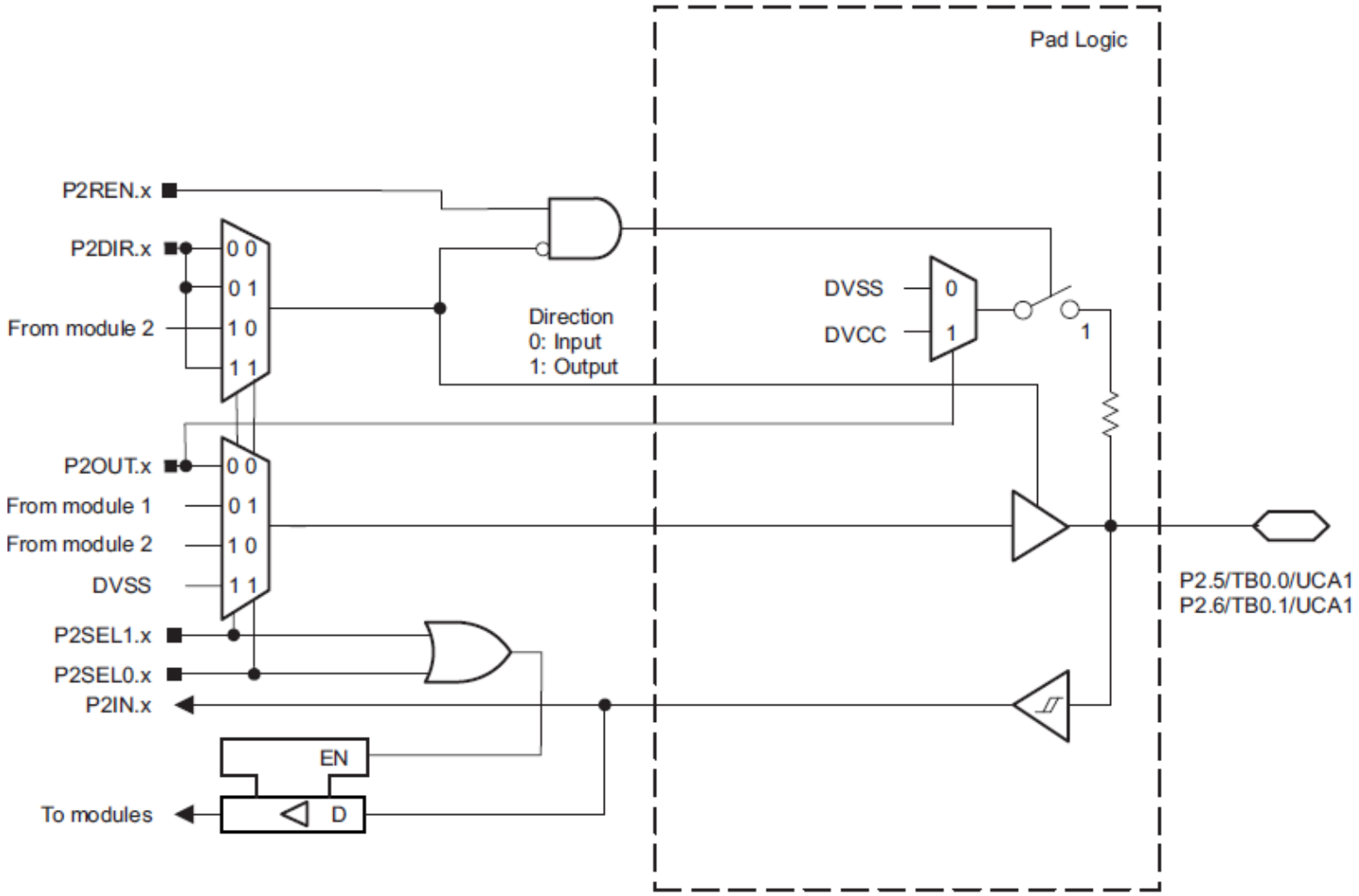
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUx registers (weak pull-up)
- INLVLx (input level control)
- SLRCONx registers (slew rate control)
- ODCONx registers (open-drain control)

TI MSP430

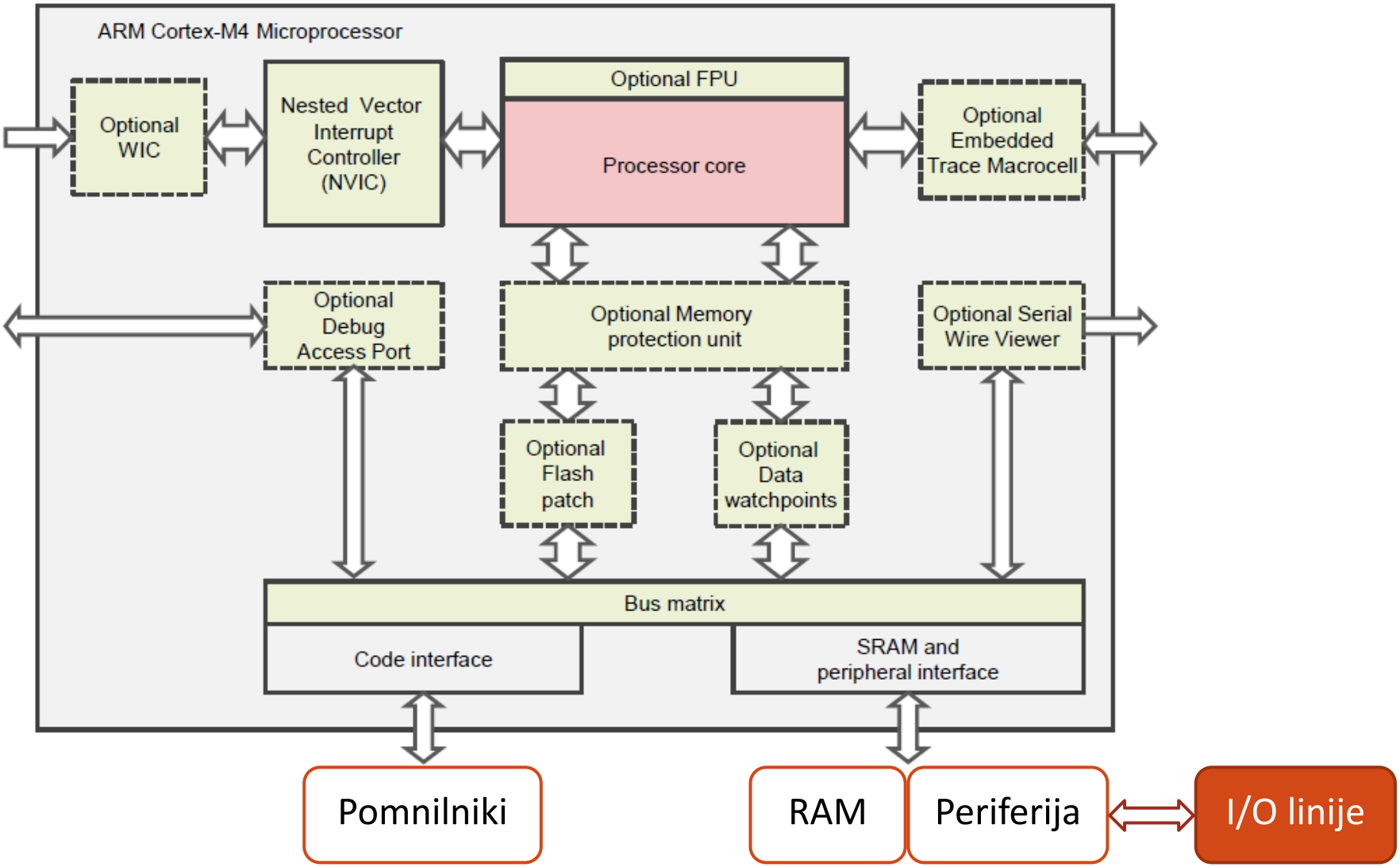

PJ.4/LFXIN 1
PJ.5/LFXOUT 2
AVSS 3
AVCC 4
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/VREF-/VeREF- 5
P1.1/TA0.2/TA1CLK/COUT/A1/C1/VREF+/VeREF+ 6
P1.2/TA1.1/TA0CLK/COUT/A2/C2 7
P3.0/A12/C12 8
P3.1/A13/C13 9
P3.2/A14/C14 10
P3.3/A15/C15 11
P1.3/TA1.2/UCB0STE/A3/C3 12
P1.4/TB0.1/UCA0STE/A4/C4 13
P1.5/TB0.2/UCA0CLK/A5/C5 14
PJ.0/TDO/TB0OUTH/SMCLK/SRSCG1/C6 15
PJ.1/TDI/TCLK/MCLK/SRSCG0/C7 16
PJ.2/TMS/ACLK/SROSCOFF/C8 17
PJ.3/TCK/SRCPUOFF/C9 18
P2.5/TB0.0/UCA1TXD/UCA1SIMO 19
38 AVSS
37 P2.4/TA1.0/UCA1CLK/A7/C11
36 P2.3/TA0.0/UCA1STE/A6/C10
35 P2.7
34 DVCC
33 DVSS
32 P4.4/TB0.5
31 P1.7/TB0.4/UCB0SOMI/UCB0SCL/TA1.0
30 P1.6/TB0.3/UCB0SIMO/UCB0SDA/TA0.0
29 P3.7/TB0.6
28 P3.6/TB0.5
27 P3.5/TB0.4/COUT
26 P3.4/TB0.3/SMCLK
25 P2.2/TB0.2/UCB0CLK
24 P2.1/TB0.0/UCA0RXD/UCA0SOMI/TB0.0
23 P2.0/TB0.6/UCA0TXD/UCA0SIMO/TB0CLK/ACLK
22 RST/NMI/SBWTDIO
21 TEST/SBWTCK
20 P2.6/TB0.1/UCA1RXD/UCA1SOMI


P1.x, P2.x
P3.x, P4.x
PJ.x
2x8
2x8
1x8
Capacitive Touch I/O 0,
Capacitive Touch I/O 1
I/O Ports P1, P2 2x8 I/Os
PA 1x16 I/Os
I/O Ports P3, P4 2x8 I/Os
PB 1x16 I/Os
I/O Port PJ 1x8 I/Os
LFXIN, HFXIN
LFXOUT, HFXOUT
MCLK
Clock System
ACLK
SMCLK
Comp_E (up to 16 inputs)
ADC12_B (up to 16 standard inputs, up to 8 differential inputs)
REF_A Voltage Reference
DMA Controller 3 Channel
CPUXV2 incl. 16 Registers
EEM (S: 3 + 1) EnergyTrace++
JTAG Interface
Spy-Bi-Wire
Bus Control Logic
MAB
MDB
MPU IP Encap FRAM 64KB 48KB 32KB
RAM 2KB 1KB
Power Mgmt LDO SVS Brownout
CRC16
MPY32
AES256 Security Encryption, Decryption (128, 256)
Watchdog
TA2 TA3 Timer_A 2 CC Registers (int. only)
TB0 Timer_B 7 CC Registers (int, ext)
TA0 Timer_A 3 CC Registers (int, ext)
TA1 Timer_A 3 CC Registers (int, ext)
eUSCI_A0 eUSCI_A1 (UART, IrDA, SPI)
eUSCI_B0 (I²C, SPI)
RTC_B
LPM3.5 Domain

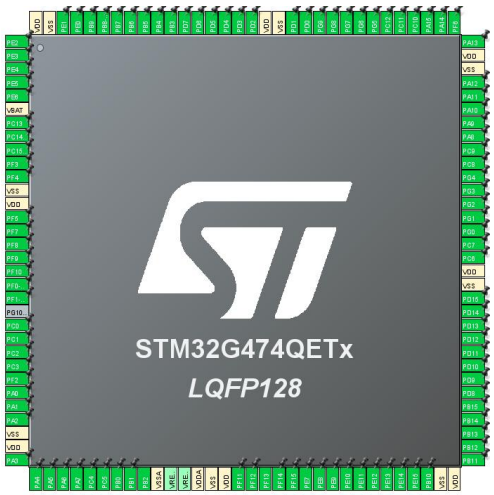
Arhitektura splošnega I/O priključka pri MSP430

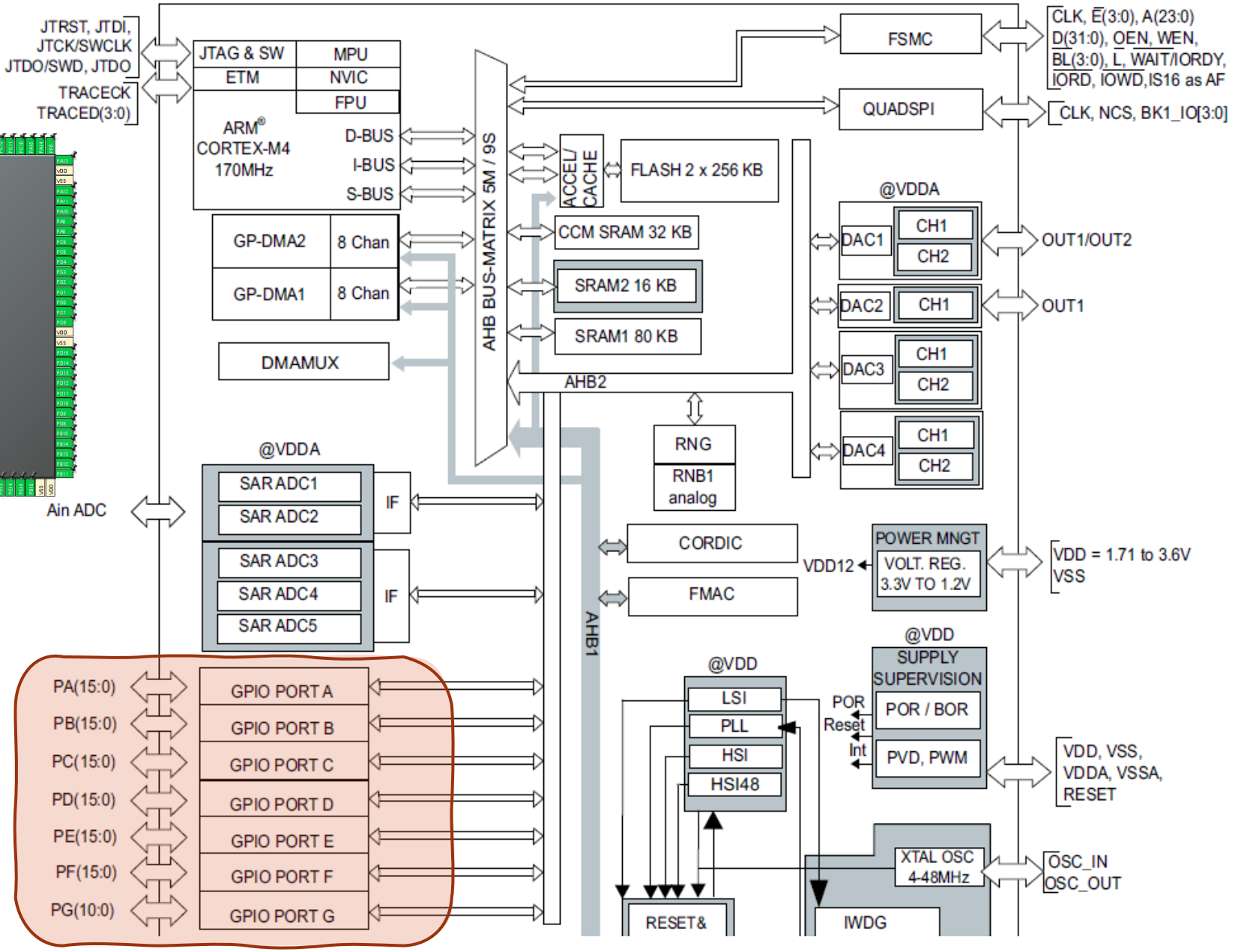


ARM STM32

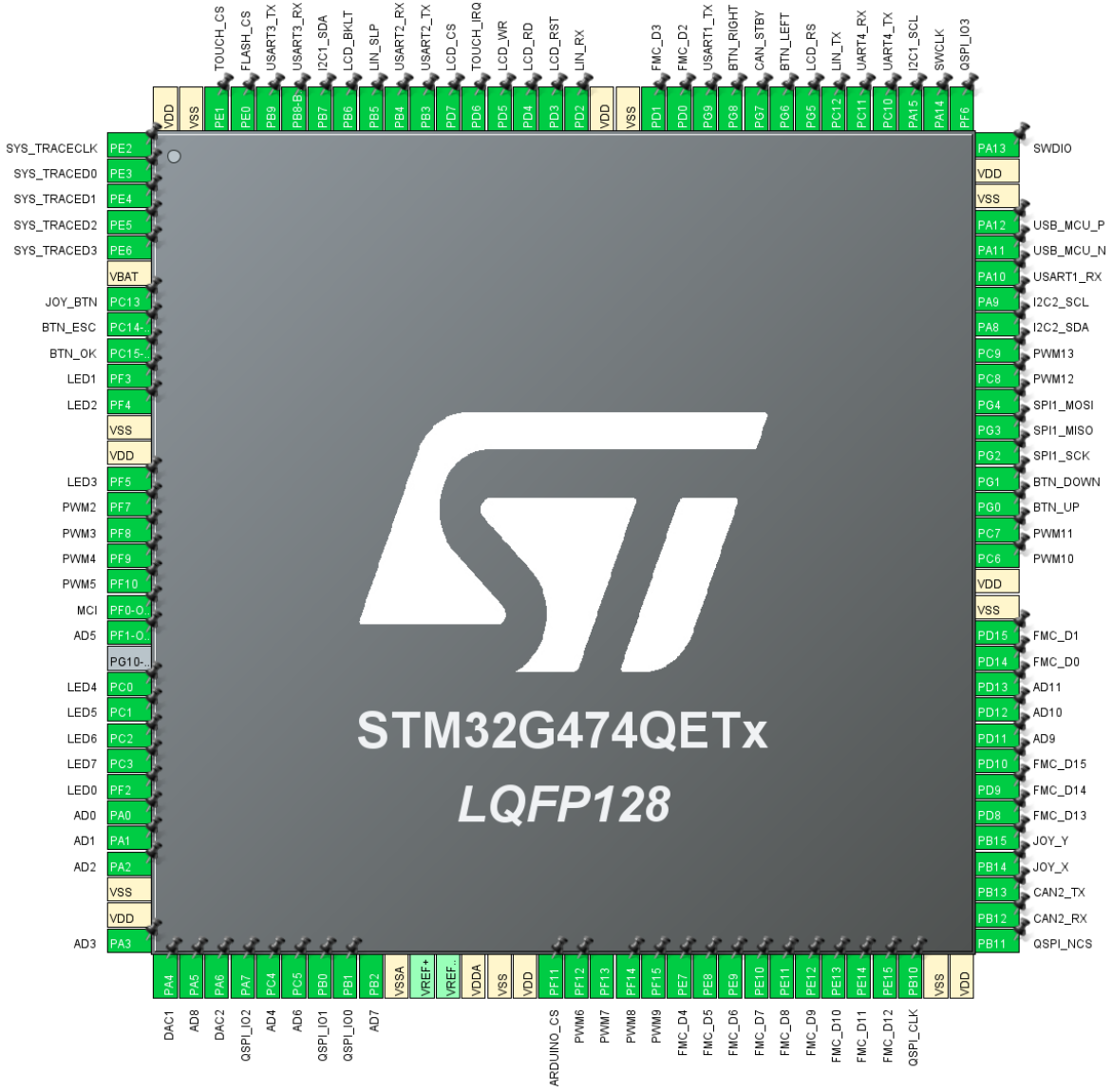

ARM Cortex-M4 Microprocessor
Optional WIC
Nested Vector Interrupt Controller (NVIC)
Optional FPU
Processor core
Optional Embedded Trace Macrocell
Optional Debug Access Port
Optional Memory protection unit
Optional Serial Wire Viewer
Optional Flash patch
Optional Data watchpoints
Bus matrix
Code interface
SRAM and peripheral interface
Pomnilniki
RAM
Periferija
I/O linije

STM32G474 QET

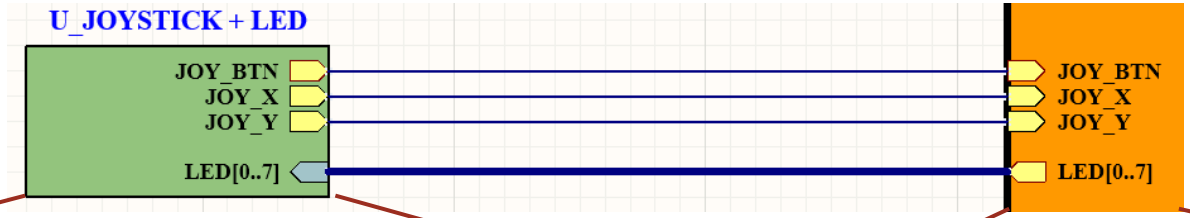


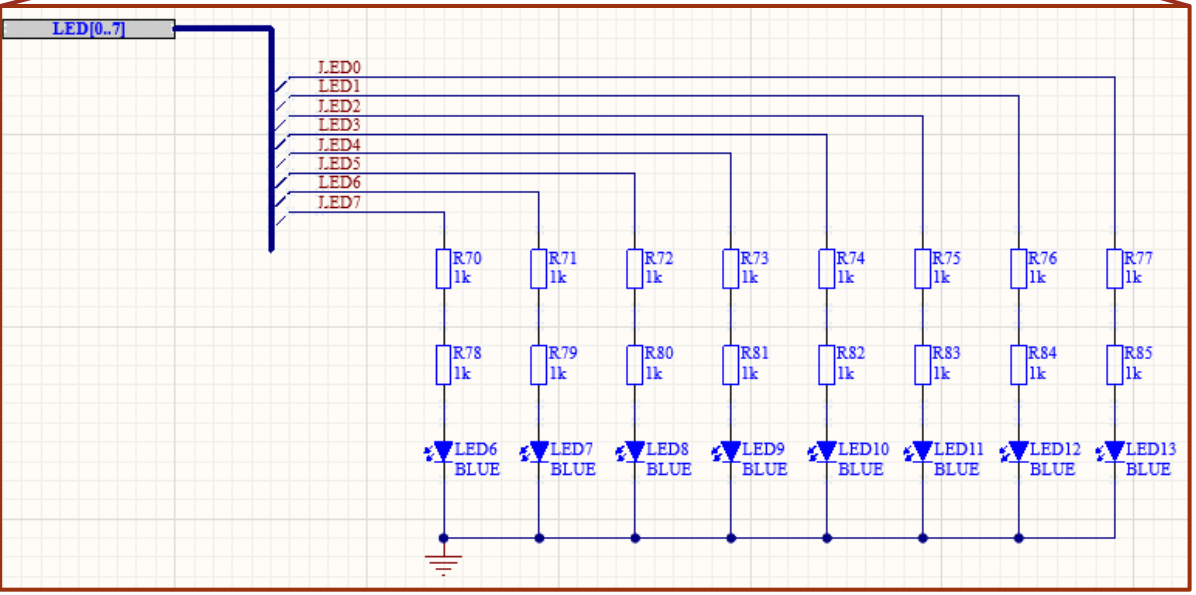


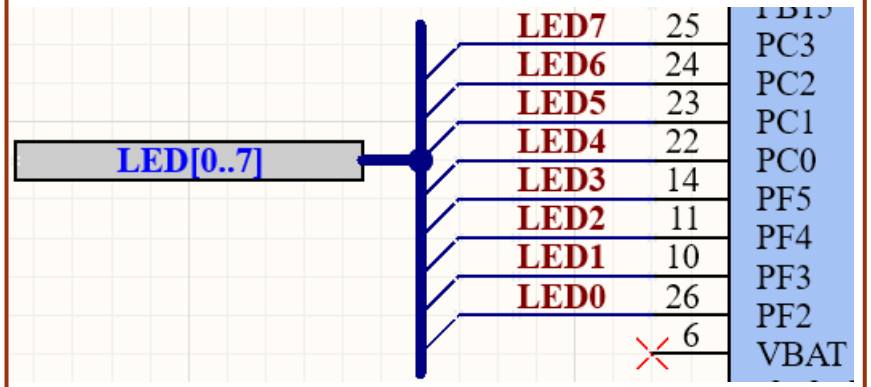
STM32G474QET



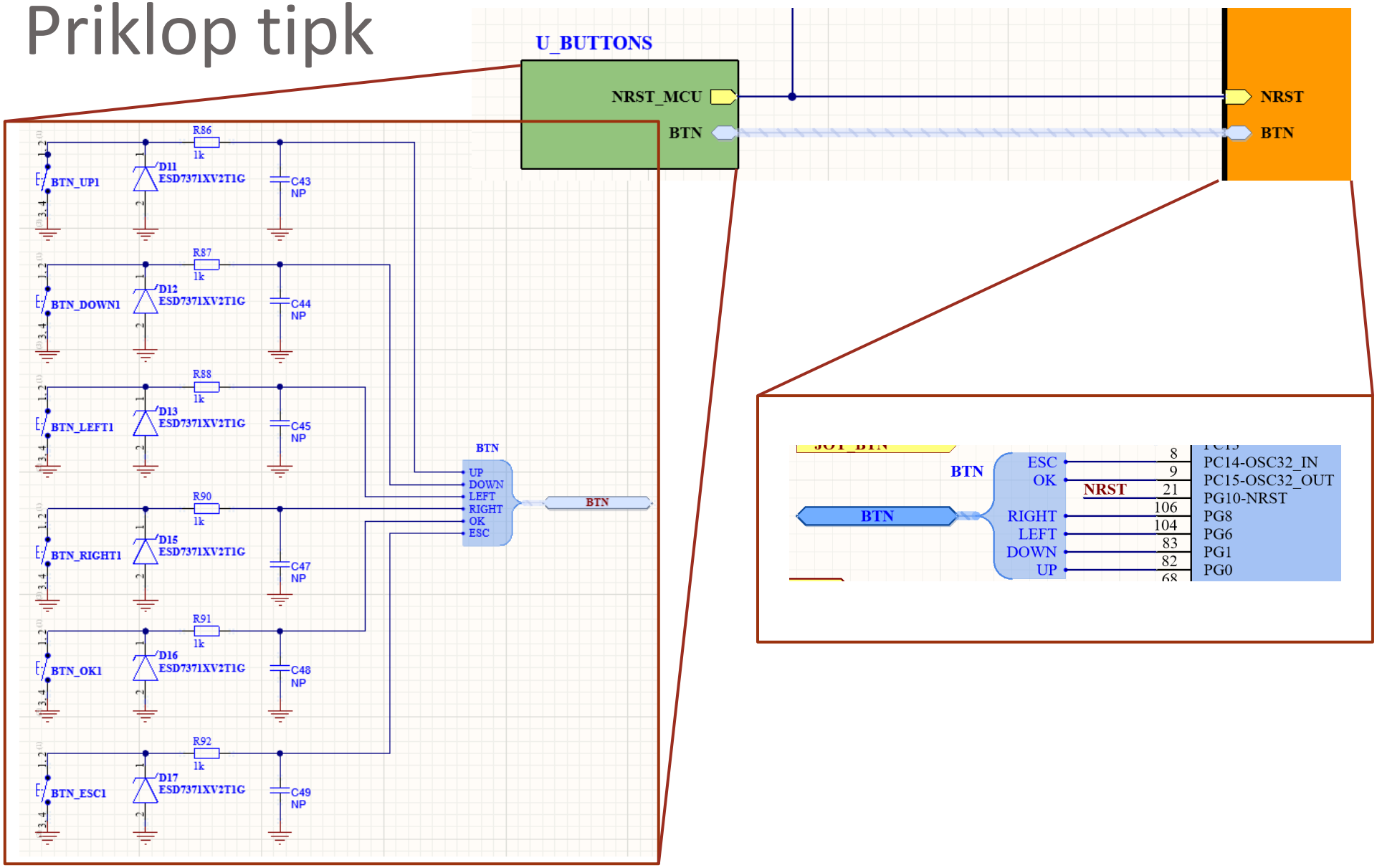
Priklop LED


U_JOYSTICK + LED
JOY_BTN
JOY_X
JOY_Y
LED[0..7]
JOY_BTN
JOY_X
JOY_Y
LED[0..7]

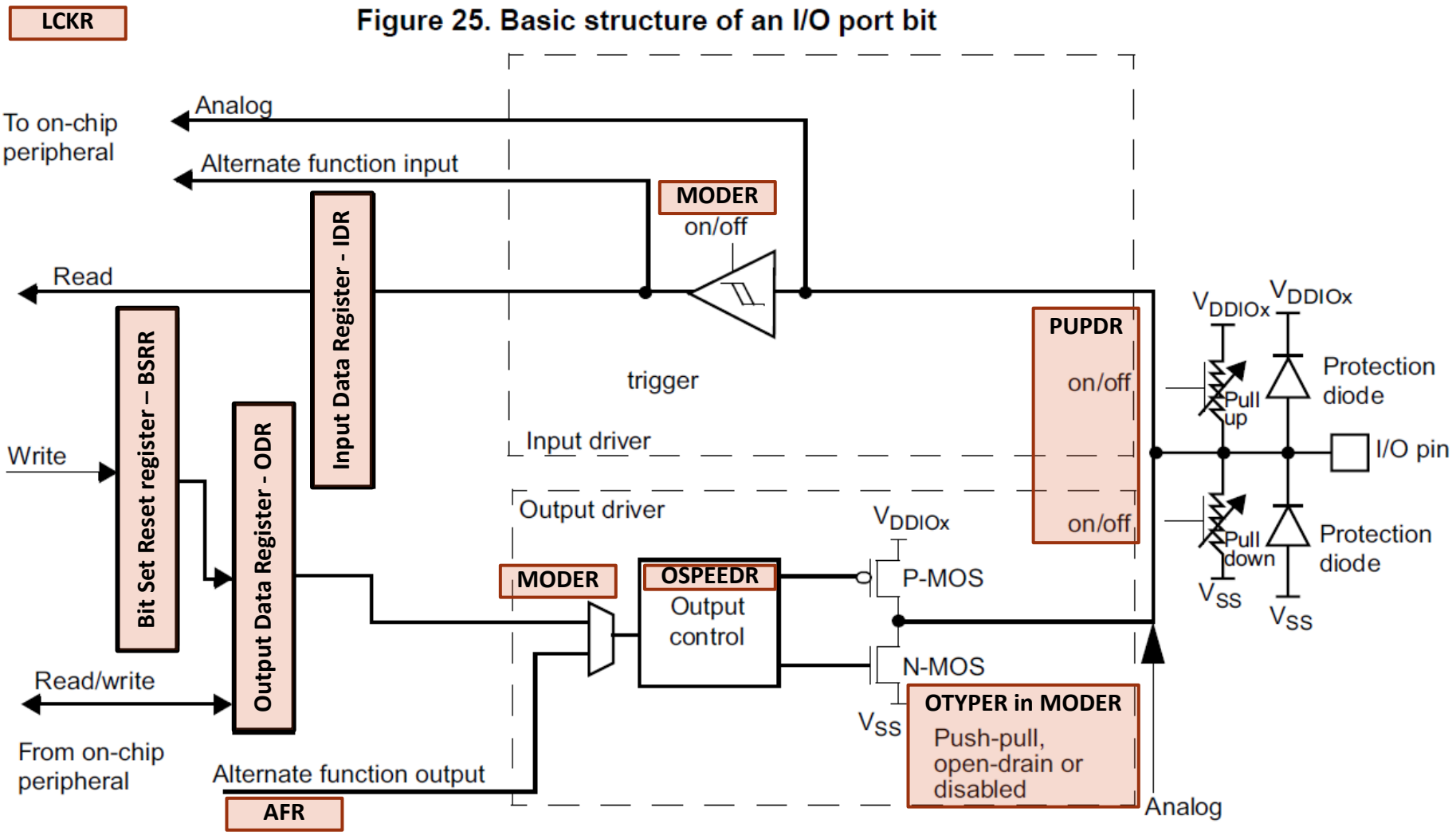

LED[0..7]
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
R70 1k
R71 1k
R72 1k
R73 1k
R74 1k
R75 1k
R76 1k
R77 1k
R78 1k
R79 1k
R80 1k
R81 1k
R82 1k
R83 1k
R84 1k
R85 1k
LED6 BLUE
LED7 BLUE
LED8 BLUE
LED9 BLUE
LED10 BLUE
LED11 BLUE
LED12 BLUE
LED13 BLUE


LED[0..7]
LED7 25 PC3
LED6 24 PC2
LED5 23 PC1
LED4 22 PC0
LED3 14 PF5
LED2 11 PF4
LED1 10 PF3
LED0 26 PF2
6 VBAT

Priklop tipk

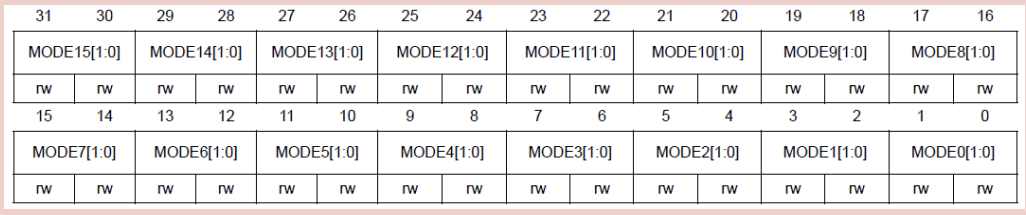
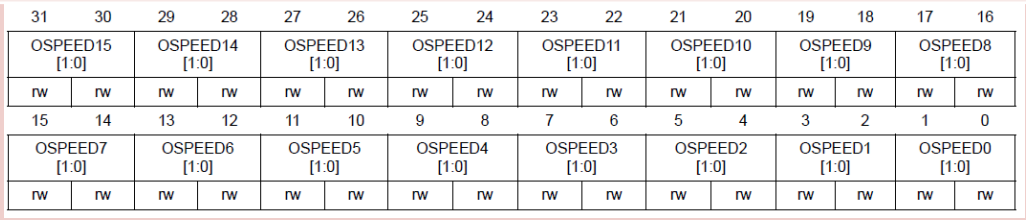
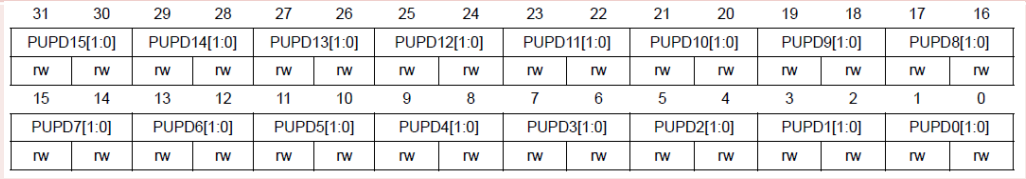
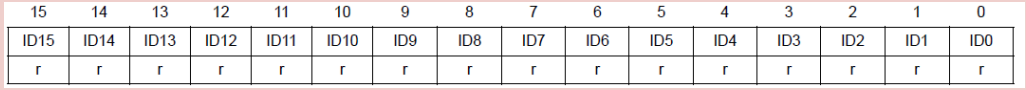
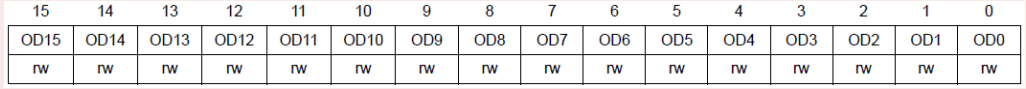


Arhitektura splošnega I/O priključka pri STM32



GPIOx registri

9.4 GPIO registers

Ime	Register	Funkcija
Mode R **MODER**		00: Input mode 01: General purpose output mode 10: Alternate function mode 11: Analog mode (reset state)
Output Type R **OTYPER**		0: Output push-pull (reset state) 1: Output open-drain
Output Speed R **OSPEEDR**		00: Low speed 01: Medium speed 10: High speed 11: Very high speed
Pull-Up/Down R **PUPDR**		00: No pull-up, pull-down 01: Pull-up 10: Pull-down 11: Reserved
Input Data R **IDR**		Port x input data I/O pin
Output Data R **ODR**		Port output data I/O pin

GPIOx registri

9.4 GPIO registers

Ime	Register	Funkcija
Bit Set/Reset R **BSRR**	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 BR15 BR14 BR13 BR12 BR11 BR10 BR9 BR8 BR7 BR6 BR5 BR4 BR3 BR2 BR1 BR0 w w w w w w w w w w w w w w w w 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BS15 BS14 BS13 BS12 BS11 BS10 BS9 BS8 BS7 BS6 BS5 BS4 BS3 BS2 BS1 BS0 w w w w w w w w w w w w w w w w	0: No action on the corresponding ODx bit 1: Resets the corresponding ODx bit 0: No action on the corresponding ODx bit 1: Sets the corresponding ODx bit
Lock R **LCKR**	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 Res Res Res Res Res Res Res Res Res Res Res Res Res Res Res LCKK rw 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 LCK15 LCK14 LCK13 LCK12 LCK11 LCK10 LCK9 LCK8 LCK7 LCK6 LCK5 LCK4 LCK3 LCK2 LCK1 LCK0 rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw	WR LCKR[16] = '1' + LCKR[15:0] WR LCKR[16] = '0' + LCKR[15:0] WR LCKR[16] = '1' + LCKR[15:0] RD LCKR RD LCKR[16] = 0: Port configuration not locked 1: Port configuration locked
Alternate function R Low **AFRL**	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 AFSEL7[3:0] AFSEL6[3:0] AFSEL5[3:0] AFSEL4[3:0] rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 AFSEL3[3:0] AFSEL2[3:0] AFSEL1[3:0] AFSEL0[3:0] rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw	Seznam vseh Alternate functions: STM32G474 datasheet poglavje 4.11
Alternate function R High **AFRH**	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 AFSEL15[3:0] AFSEL14[3:0] AFSEL13[3:0] AFSEL12[3:0] rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 AFSEL11[3:0] AFSEL10[3:0] AFSEL9[3:0] AFSEL8[3:0] rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw	
Bit Reset R **BRR**	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 BR15 BR14 BR13 BR12 BR11 BR10 BR9 BR8 BR7 BR6 BR5 BR4 BR3 BR2 BR1 BR0 w w w w w w w w w w w w w w w w	0: No action on the corresponding ODx bit 1: Reset the corresponding ODx bit

Alternate functions

4.11 Alternate functions

Table 13. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/ SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C1/3/ TIM1/2/3/4/5/8/ 20/15/ COMP1	QUADSPI1/ I2C3/4/SAI1/USB/HRTIM1/ TIM8/20/15/ COMP3	I2C1/2/3/ 4/TIM1/8/ 16/17	QUADSPI1 /SPI1/2/3/4/ I2S2/3/I2C4/ UART4/5/ TIM8/ Infrared	QUADSPI1/ SPI2/3/I2S2 /3/TIM1/5/8/ 20/Infrared	USART1/2/3 /FDCAN/CO MP7/5/6	I2C3/4/UAR T4/5/LPUA RT1/COMP 1/2/7/4/5/6/ 3	FDCAN/T IM1/8/15/ FDCAN1/ 2	QUADSPI1/ TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/F DCAN1/3	FMC/LPUART1 /SAI1/HRTIM1/ TIM1	SAI1SAI1/HR TIM1/OPAMP 2	UART4/5/ SAI1/TIM 2/15/ UCPD1	EVENT
Port A	PA0	-	TIM2_CH1	TIM5_CH1	-	-	-	-	USART2_ CTS	COMP1 _OUT	TIM8_ BKIN	TIM8_ETR	-	-	-	TIM2_ ETR	EVENT OUT
	PA1	RTC_ REFIN	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_ RTS_DE	-	TIM15_ CH1N	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_ TX	COMP2 _OUT	TIM15_ CH1	QUADSPI1_ BK1_NCS	-	LPUART1_TX	-	UCPD1_ FRSTX	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_ RX	-	TIM15_ CH2	QUADSPI1_ CLK	-	LPUART1_RX	SAI1_MCLK_ A	-	EVENT OUT
	PA4	-	-	TIM3_CH2	-	-	SPI1_NSS	SPI3_NSS/ I2S3_WS	USART2_ CK	-	-	-	-	-	SAI1_FS_B	-	EVENT OUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	UCPD1_ FRSTX	EVENT OUT
	PA6	-	TIM16_CH1	TIM3_CH1	-	TIM8_ BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1 _OUT	-	QUADSPI1_ BK1_IO3	-	LPUART1_ CTS	-	-	EVENT OUT
	PA7	-	TIM17_CH1	TIM3_CH2	-	TIM8_ CH1N	SPI1_MOSI	TIM1_ CH1N	-	COMP2_ OUT	-	QUADSPI1_ BK1_IO2	-	-	-	UCPD1_ FRSTX	EVENT OUT
	PA8	MCO	-	I2C3_SCL	-	I2C2_ SDA	I2S2_MCK	TIM1_CH1	USART1_ CK	COMP7 _OUT	-	TIM4_ETR	FDCAN3 _RX	SAI1_CK2	HRTIM1_ CHA1	SAI1_SC K_A	EVENT OUT
	PA9	-	-	I2C3_SMBA	-	I2C2_ SCL	I2S3_MCK	TIM1_CH2	USART1_ TX	COMP5 _OUT	TIM15_ BKIN	TIM2_CH3	-	-	HRTIM1_ CHA2	SAI1_FS _A	EVENT OUT
	PA10	-	TIM17_BKIN	-	USB_ CRS_SYNC	I2C2_ SMBA	SPI2_MISO	TIM1_CH3	USART1_ RX	COMP6 _OUT	-	TIM2_CH4	TIM8_ BKIN	SAI1_D1	HRTIM1_ CHB1	SAI1_SD _A	EVENT OUT
	PA11	-	-	-	-	-	SPI2_MOSI/ I2S2_SD	TIM1_ CH1N	USART1_ CTS	COMP1 _OUT	FDCAN1 _RX	TIM4_CH1	TIM1_ CH4	TIM1_BKIN2	HRTIM1_ CHB2	-	EVENT OUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_ CH2N	USART1_ RTS_DE	COMP2 _OUT	FDCAN1 _TX	TIM4_CH2	TIM1_ ETR	-	HRTIM1_ FLT1	-	EVENT OUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	I2C4_SCL	I2C1_ SCL	IR_OUT	-	USART3_ CTS	-	-	TIM4_CH3	-	-	SAI1_SD_B	-	EVENT OUT
	PA14	SWCLK-JTCK	LPTIM1_OUT	-	I2C4_SMBA	I2C1_ SDA	TIM8_CH2	TIM1_ BKIN	USART2_ TX	-	-	-	-	-	SAI1_FS_B	-	EVENT OUT
	PA15	JTDI	TIM2_CH1	TIM8_CH1	-	I2C1_ SCL	SPI1_NSS	SPI3_NSS/ I2S3_WS	USART2_ RX	UART4 _RTS_DE	TIM1_ BKIN	-	FDCAN3 _ TX	-	HRTIM1_ FLT2	TIM2_ ETR	EVENT OUT

I/O priključek kot izhod (MODE 01)

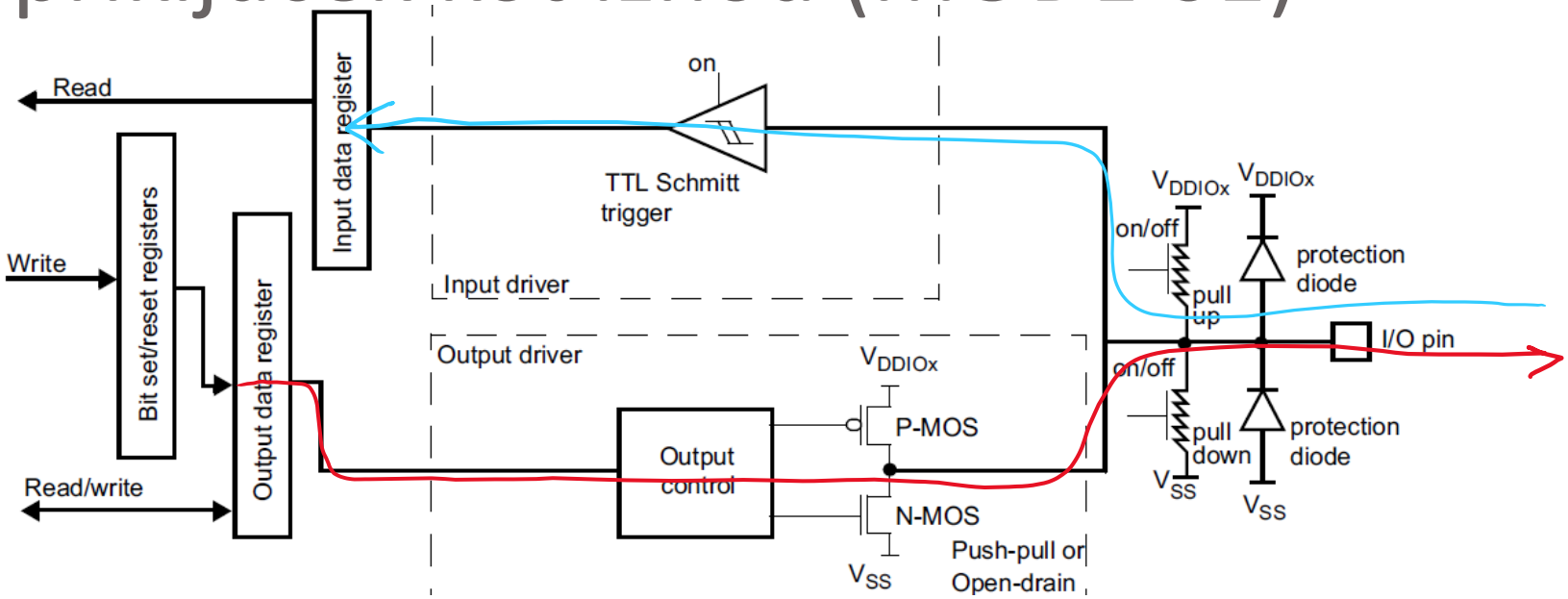


Table 56.

MODE(i) [1:0]	OTYPE(i)	OSPEED(i) [1:0]	PUPD(i) [1:0]		I/O configuration	
01	0	SPEED [1:0]	0	0	GP output	PP
	0		0	1	GP output	PP + PU
	0		1	0	GP output	PP + PD
	0		1	1	Reserved	
	1		0	0	GP output	OD
	1		0	1	GP output	OD + PU
	1		1	0	GP output	OD + PD
	1		1	1	Reserved (GP output OD)	

GP = general-purpose, PP = push-pull, PU = pull-up, PD = pull-down, OD = open-drain, AF = alternate function.

I/O priključek kot vhod (MODE 00)

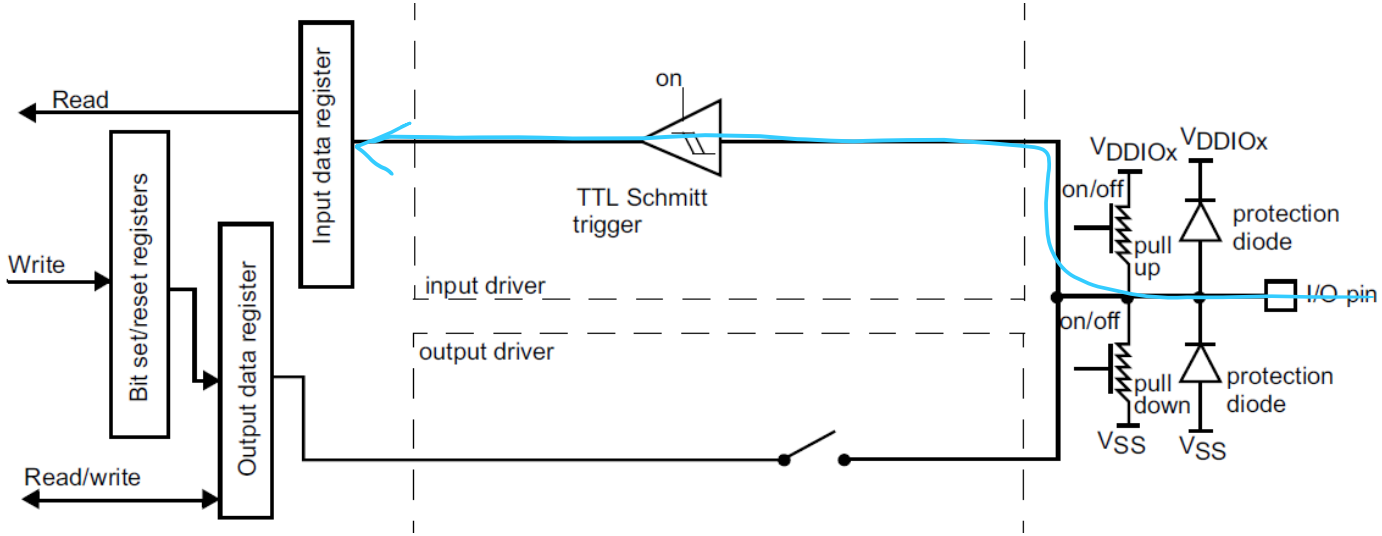


Table 56.

MODE(i) [1:0]	OTYPE(i)	OSPEED(i) [1:0]		PUPD(i) [1:0]		I/O configuration	
00	x	x	x	0	0	Input	Floating
	x	x	x	0	1	Input	PU
	x	x	x	1	0	Input	PD
	x	x	x	1	1	Reserved (input floating)	

GP = general-purpose, PP = push-pull, PU = pull-up, PD = pull-down, OD = open-drain, AF = alternate function.

Alternativne funkcije (MODE 10)

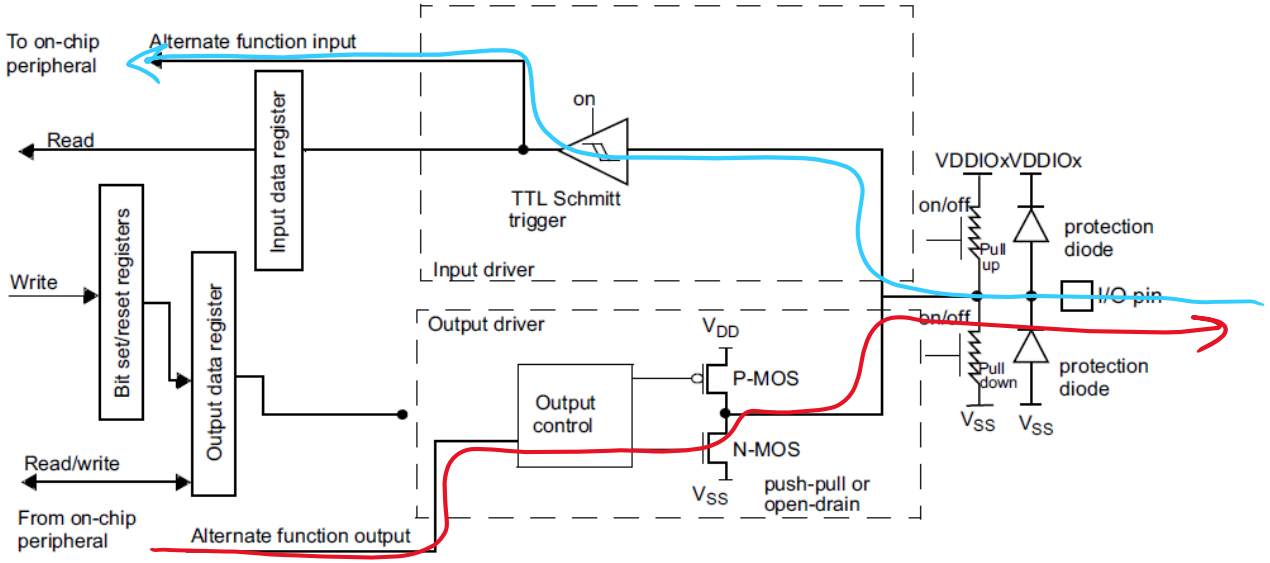


Table 56.

MODE(i) [1:0]	OTYPE(i)	OSPEED(i) [1:0]	PUPD(i) [1:0]		I/O configuration	
10	0	SPEED [1:0]	0	0	AF	PP
	0		0	1	AF	PP + PU
	0		1	0	AF	PP + PD
	0		1	1	Reserved	
	1		0	0	AF	OD
	1		0	1	AF	OD + PU
	1		1	0	AF	OD + PD
	1		1	1	Reserved	

GP = general-purpose, PP = push-pull, PU = pull-up, PD = pull-down, OD = open-drain, AF = alternate function.

Analogne funkcije (MODE 11)

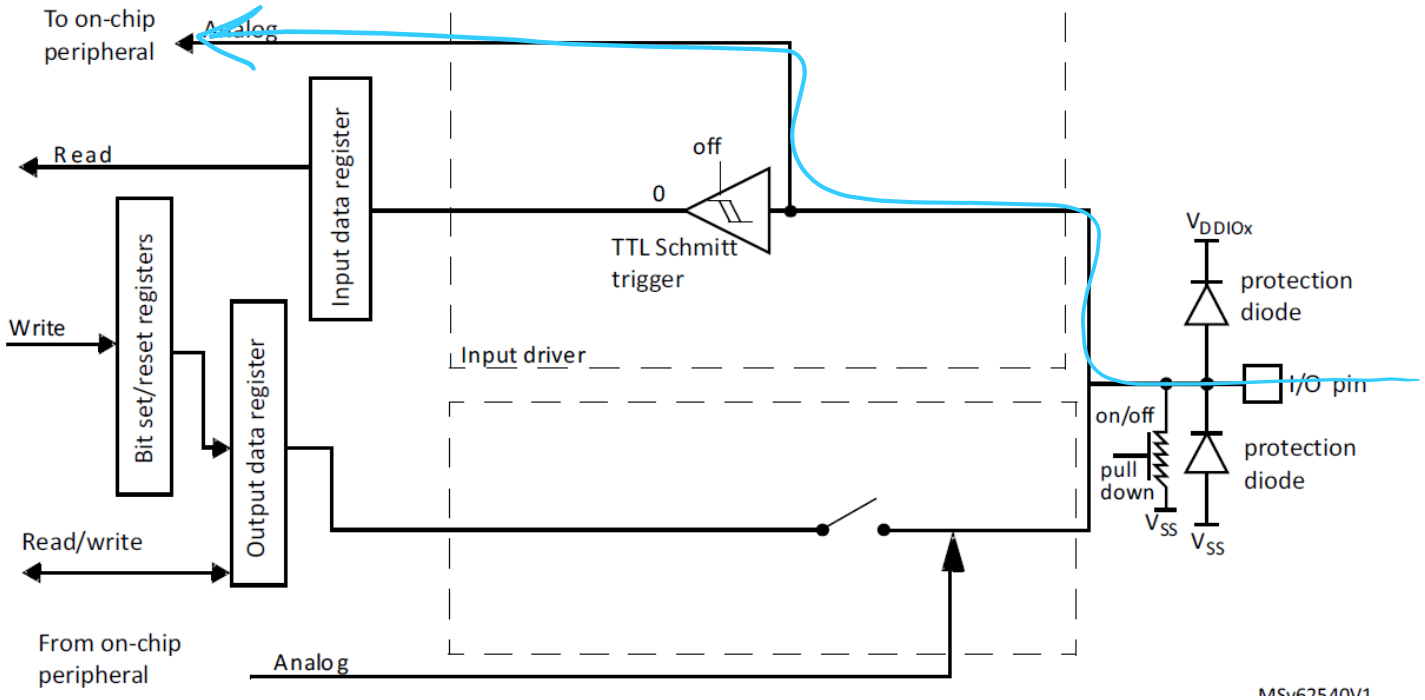
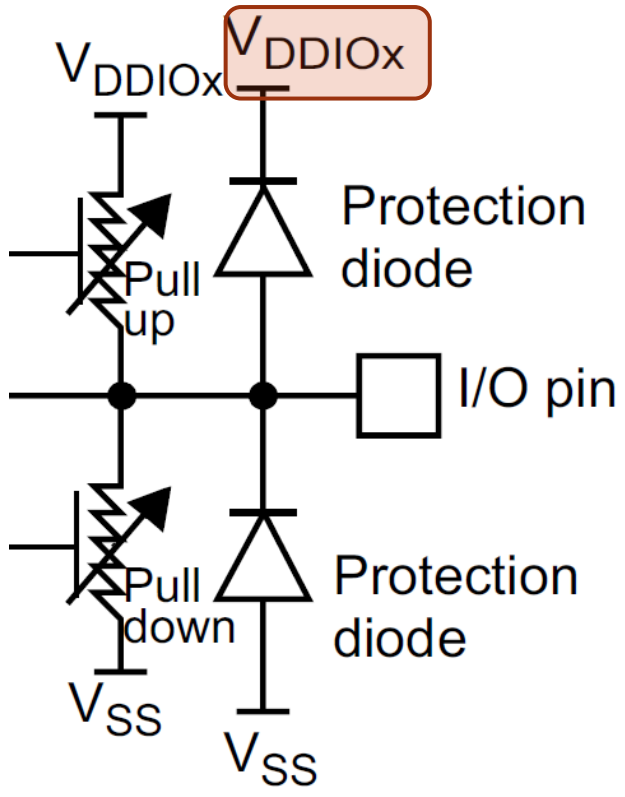


Table 56.

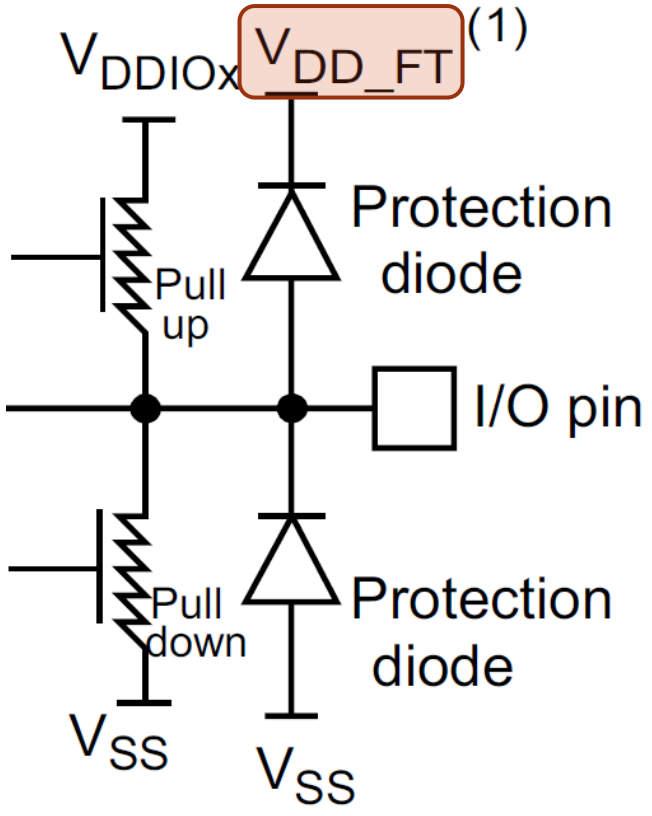
MODE(i) [1:0]	OTYPE(i)	OSPEED(i) [1:0]		PUPD(i) [1:0]		I/O configuration	
11	x	x	x	0	0	Input/output	Analog
	x	x	x	0	1	Reserved	
	x	x	x	1	0	Input/output	Analog, PD
	x	x	x	1	1	Reserved	

3.3 V in 5V tolerantni vhodi

3.3V tolerantni vhod **Figure 25.**

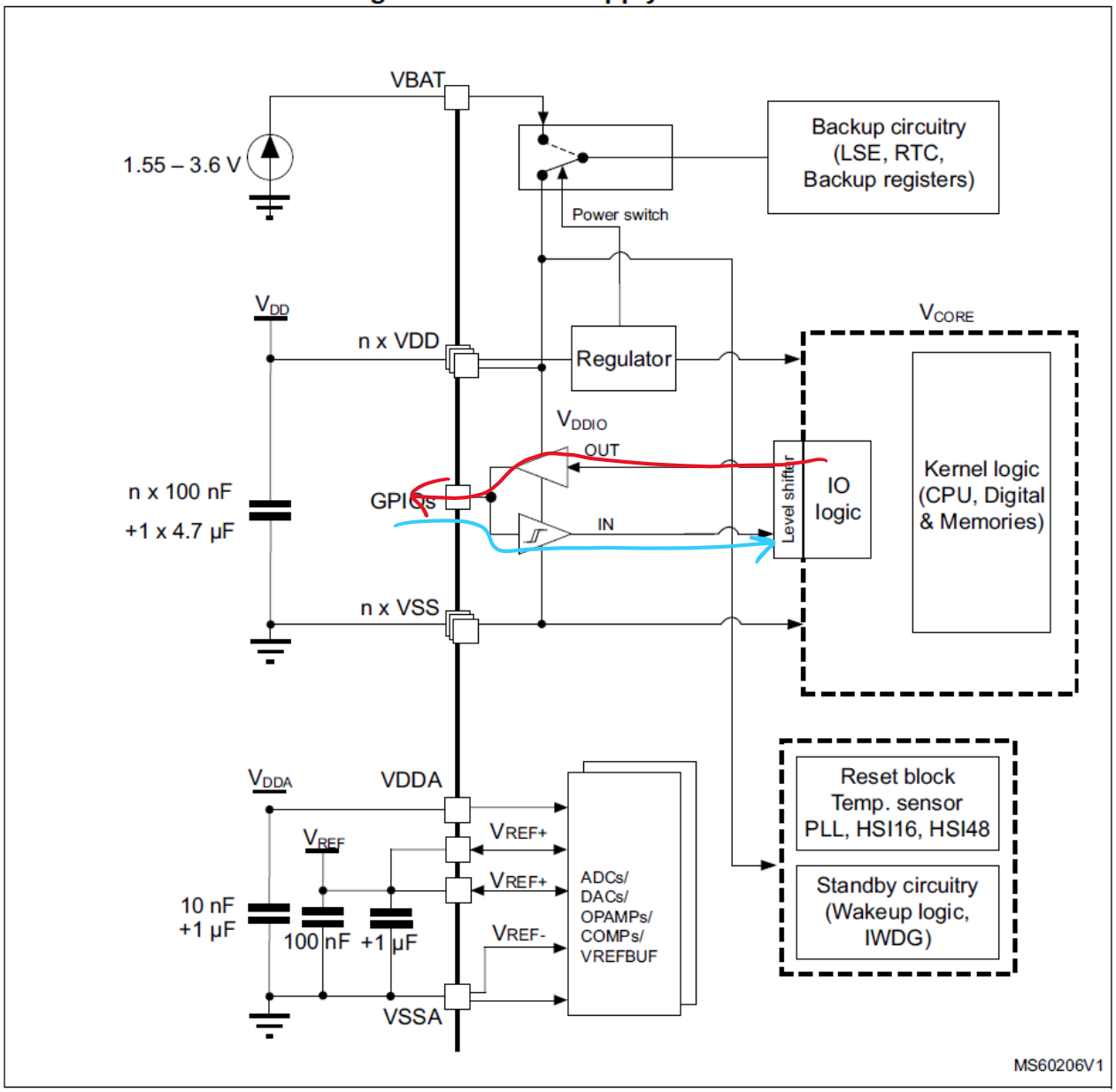


5V toleratni vhod **Figure 26.**



Napajanje

Figure 16. Power supply scheme



Tipi I/O linij

4.10 Pin definition

Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_a(1)	I/O, with Analog switch function supplied by V_{DDA}
	_c	I/O, USB Type-C PD capable
	_d	I/O, USB Type-C PD Dead Battery function
	_f(2)	I/O, Fm+ capable
	_u(3)	I/O, with USB function

Maksimalne napetosti

Table 14. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{BAT} and V_{REF+})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins except FT_c pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	
	Input voltage on FT_c pins	V_{SS}-0.3	5.5	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	
$V_{REF+}-V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 15: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Maksimalni tokovi

Table 15. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, NRST pins	-5/0(4)	
$\Sigma\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by VIN < VSS. IINJ(PIN) must never be exceeded. Refer also to *Table 14: Voltage characteristics* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Nominalni delovni pogoji

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	170	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	170	
f_{PCLK2}	Internal APB2 clock frequency	-	0	170	
V_{DD}	Standard operating voltage	-	1.71(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC	1.62	3.6	V
		DAC 1 MSPS or DAC 15 MSPS or OPAMP	1.8		
		COMP used	1.8	3.6	
		VREFBUF used	2.4	3.6	
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{IN}	I/O input voltage	TT_xx	-0.3	V_{DD}+0.3	V
		FT_c	-0.3	5	
		All I/O except TT_xx and FT_c	-0.3	MIN(MIN(V_{DD}, V_{DDA})+3.6 V, 5.5 V)(2)(3)	

Napetostni nivoji I/O linij

Table 54. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)(2)	I/O input low level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	-	-	$0.3xV_{DD}$	V
						$0.39xV_{DD}$-0.06(3)	
		FT_c	1.62 V<V_{DD}<3.6 V	-	-	$0.3xV_{DD}$	
						$0.25xV_{DD}$	
V_{IH}(1)(2)	I/O input high level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	$0.7xV_{DD}$	-	-	V
				$0.49xV_{DD}$ +0.26(3)	-	-	
		FT_c	1.62 V<V_{DD}<3.6 V	$0.7xV_{DD}$	-	-	
V_{HYS}(3)	Input hysteresis	TT_xx, FT_xxx, NRST	1.62 V<V_{DD}<3.6 V	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}		25	40	55	
C_{IO}	I/O pin capacitance	I/O pin capacitance	-	-	5	-	pF

Tokovna zmogljivost I/O linij

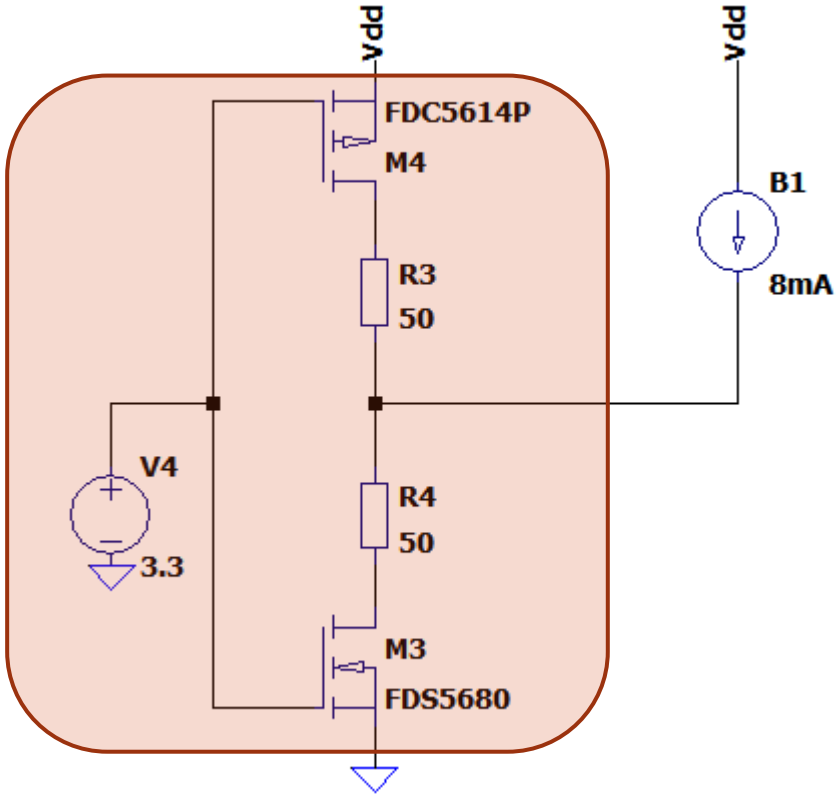
Table 55. Output voltage characteristics(1)(2)

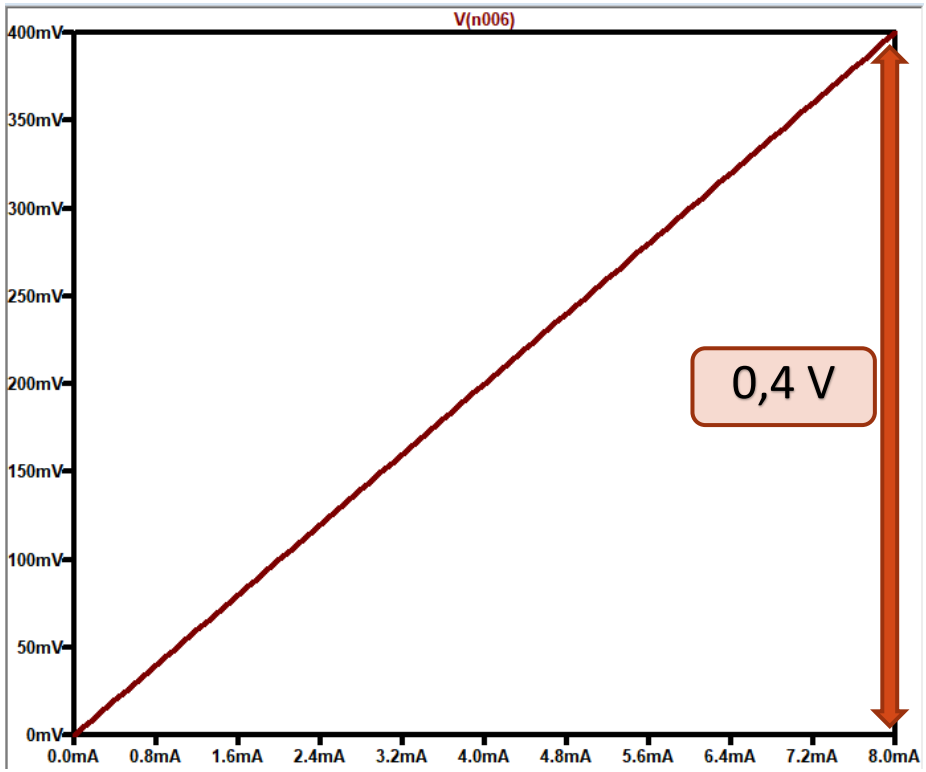
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(3)	Output low level voltage for an I/O pin	CMOS port $\|I_{IO}\|$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port $\|I_{IO}\|$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os except FT_c $\|I_{IO}\|$ = 20 mA V_{DD} ≥ 2.7 V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 1 mA for FT_c I/Os = 4 mA for other I/Os V_{DD} ≥ 1.62 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA V_{DD} ≥ 2.7 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA V_{DD} ≥ 1.62 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 14: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Zmogljivost tokovnega ponora pri -8 mA

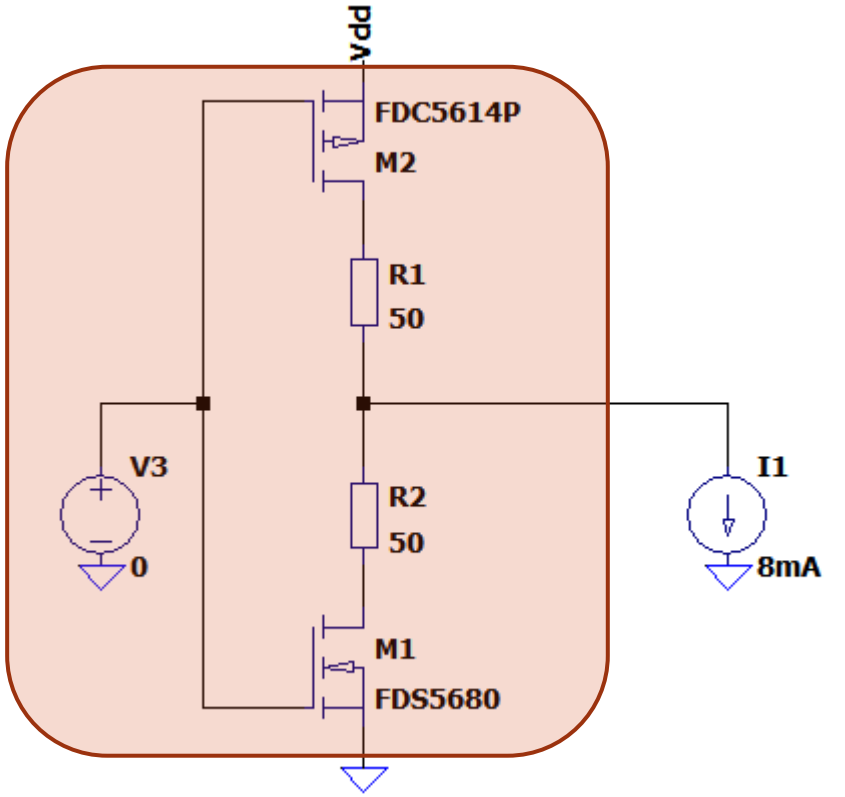
V_{OL} (3)	Output low level voltage for an I/O pin	CMOS port	-	0.4

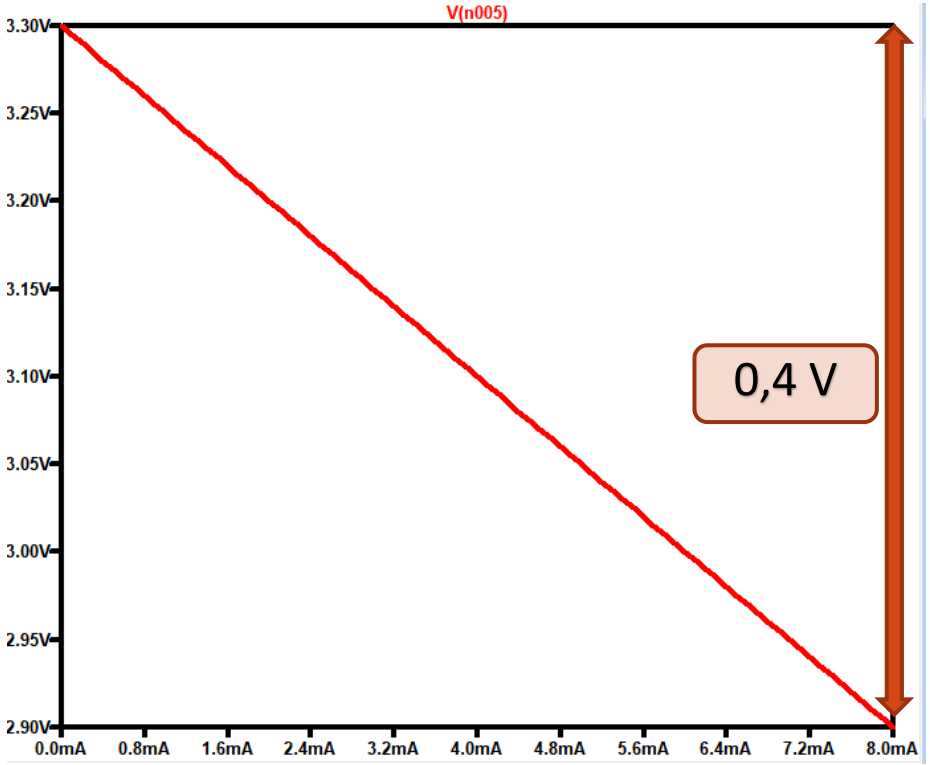




Zmogljivost tokovnega izvora pri 8 mA

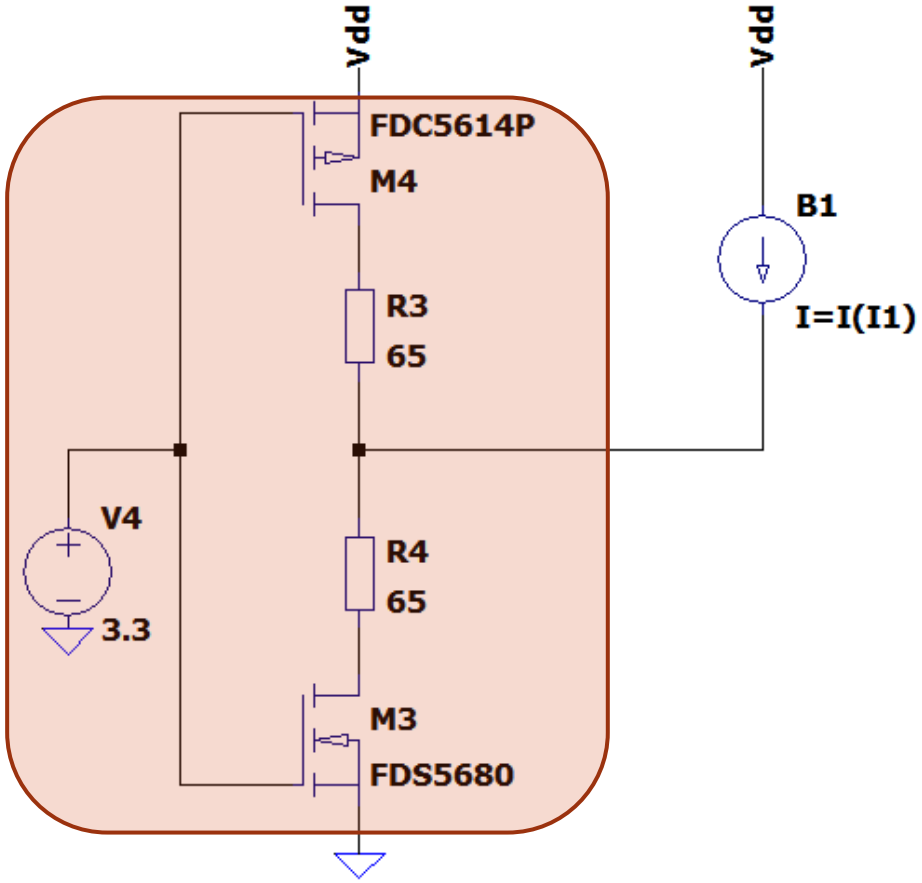
V_{OH}(3)	Output high level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	V_{DD}-0.4	-

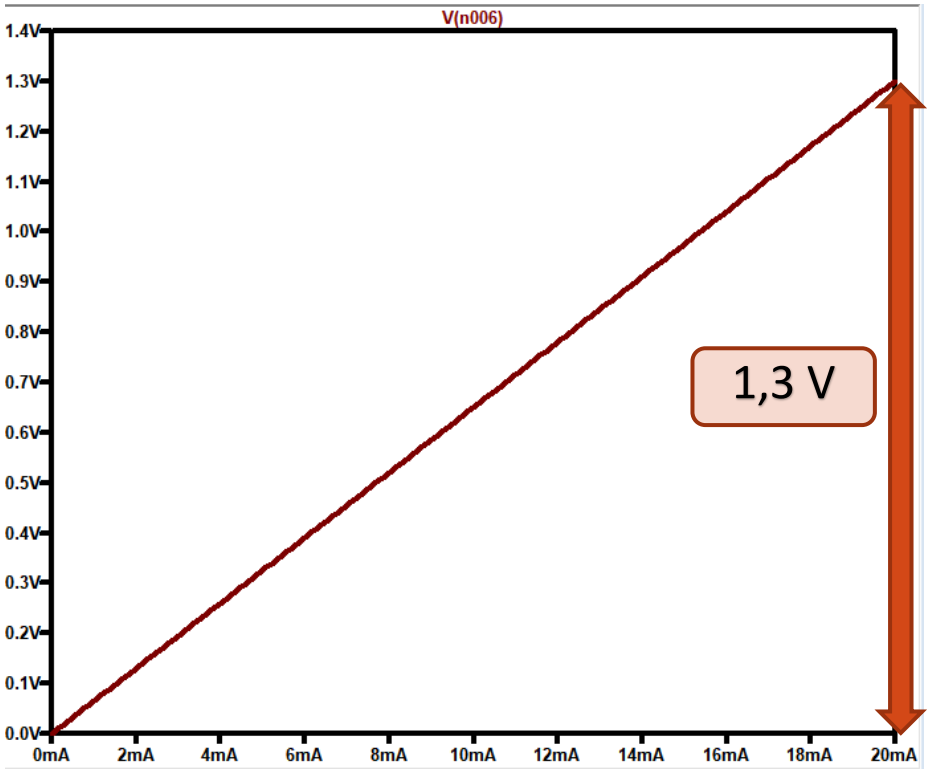




Zmogljivost tokovnega ponora pri -20 mA

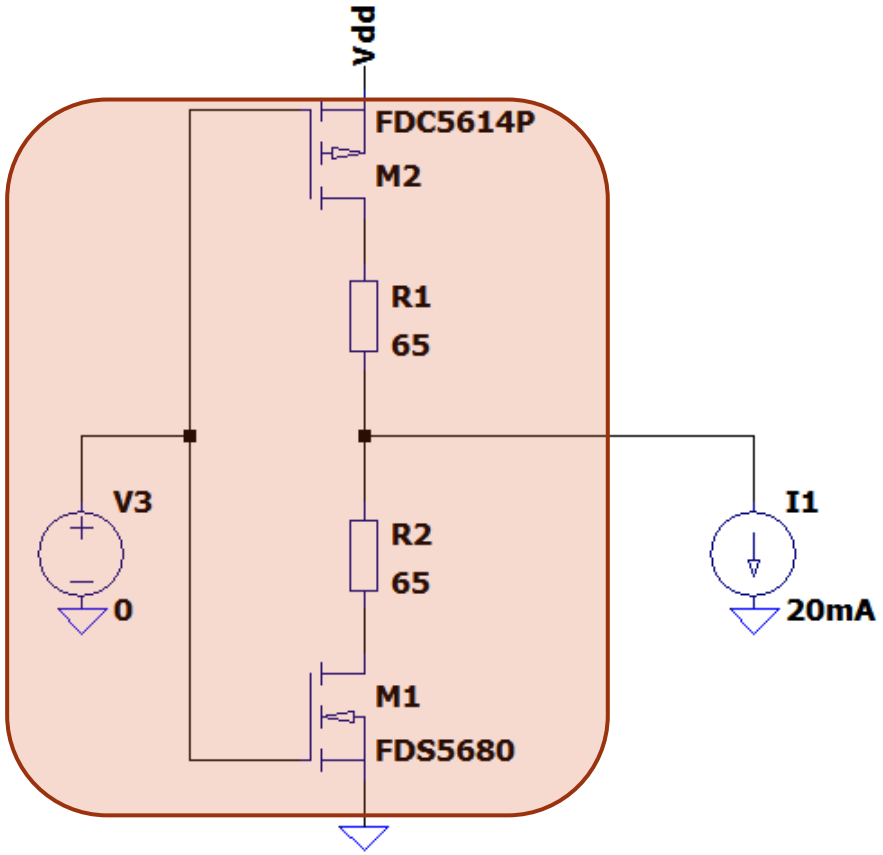
V_{OL} (3)	Output low level voltage for an I/O pin	All I/Os except FT_c I_{IO} I = 20 mA	-	1.3	V

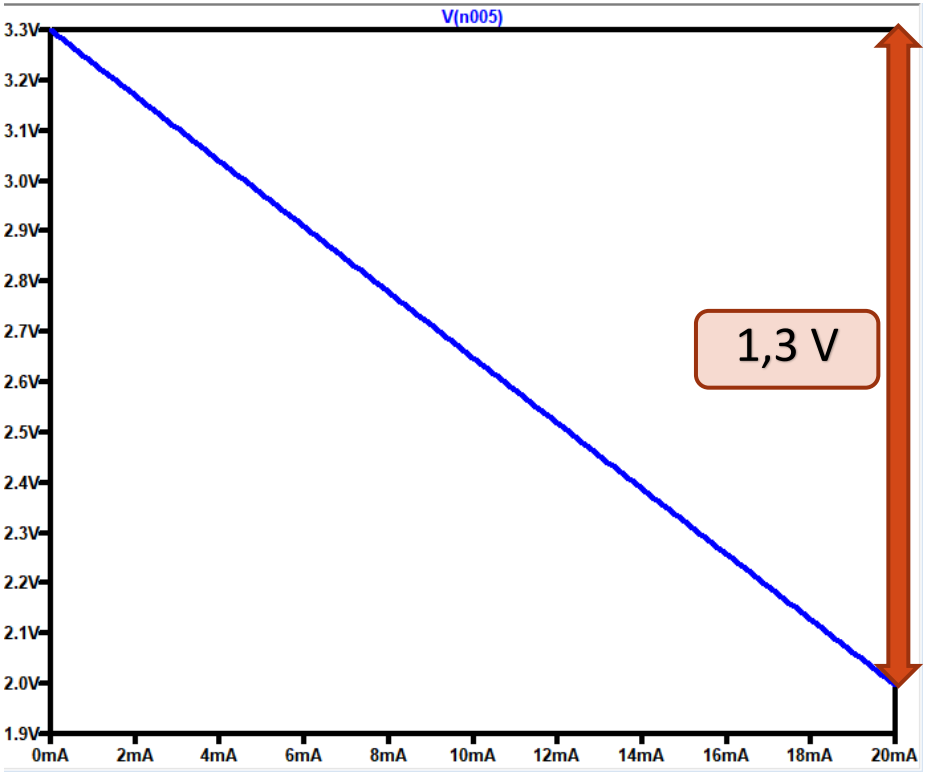




Zmogljivost tokovnega izvora pri 20 mA

V_{OH}(3)	Output high level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	V_{DD}-1.3	-





Hitrosti preklopov (**OPEEDR**)

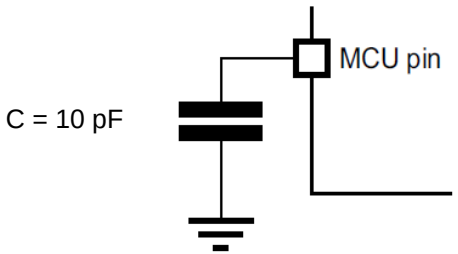
Vdd = 2,7 – 3.6 V

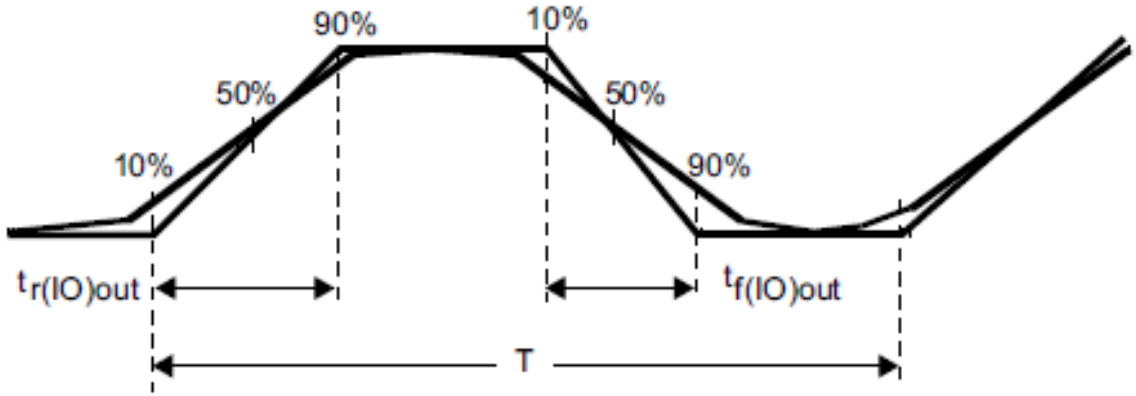
OSPEEDR	Dvnižni čas	Maks.frekvenca
00	17 ns	10 MHz
01	4,5 ns	50 MHz
10	2,5 ns	100 MHz
11	1,7 ns	180 MHz

Vdd = 1,6 – 2.7 V

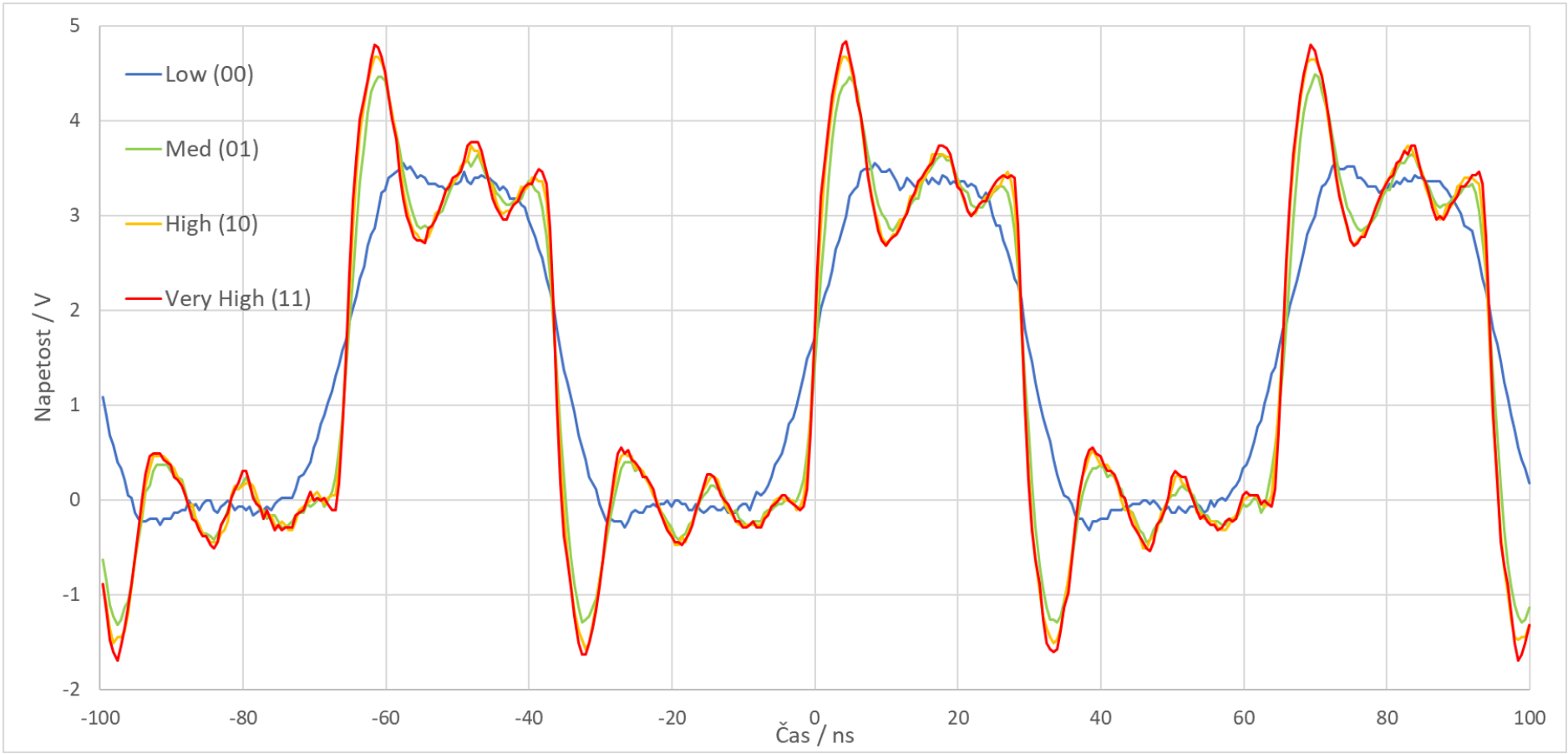
OSPEEDR	Dvnižni čas	Maks.frekvenca
00	37 ns	1,5 MHz
01	9 ns	15 MHz
10	5 ns	37,5 MHz
11	3.3 ns	75 MHz

Figure 14. Pin loading conditions





Izmerjen signal pri različnih **OSPEEDR**



Za konec

Datasheet

- Električni in logični podatki za specifični mikrokrmilnik

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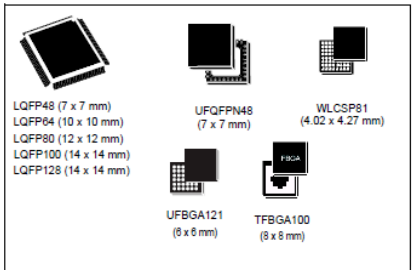
STM32G474xB STM32G474xC STM32G474xE

Arm® Cortex®-M4 32-bit MCU+FPU, 170 MHz / 213 DMIPS, 128 KB SRAM, rich analog, math acc, 184 ps 12 chan Hi-res timer

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 170 MHz with 213 DMIPS, MPU, DSP instructions
- Operating conditions:
  - V_{DD}, V_{DDA} voltage range: 1.71 V to 3.6 V
- Mathematical hardware accelerators



Reference manual

- Skupni podatki družine mikrokrmilnikov
  - Jedro, pomnilniki
  - Periferija in registri

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RM0440
Reference manual

STM32G4 Series
advanced Arm®-based 32-bit MCUs

Introduction

This reference manual targets application developers. It provides complete information on how to use the STM32G4 Series microcontroller memory and peripherals.

The STM32G4 Series is a family of microcontrollers with different memory sizes, packages and peripherals.

For ordering information, mechanical and electrical device characteristics refer to the corresponding datasheets.

For information on the Arm® Cortex®-M4 core, refer to the Cortex®-M4 *Technical Reference Manual*.

The STM32G4 Series microcontrollers include ST state-of-the-art patented technology.