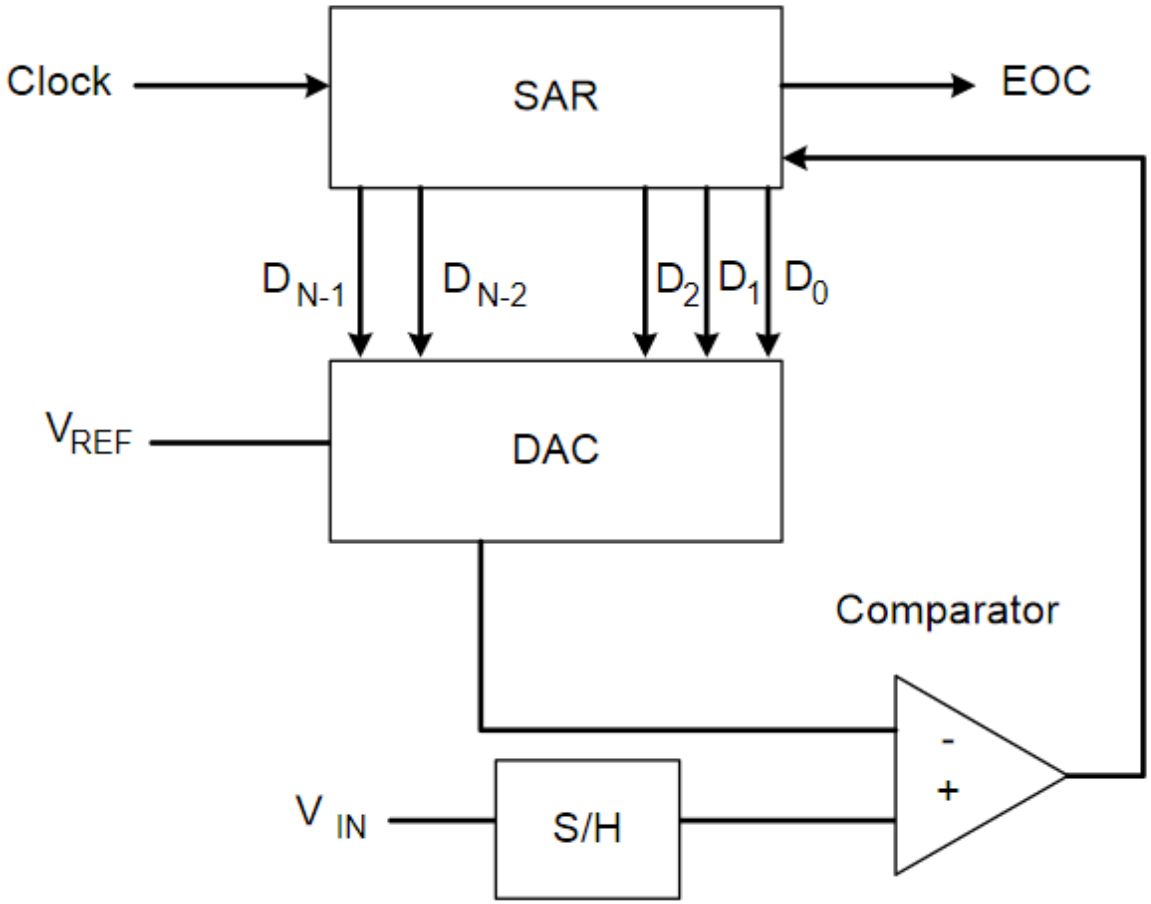
Osnove mikroprocesorske elektronike

Marko Jankovec

Primeri A/D pretvornikov

A/D pretvorniki pri mikrokrmilnikih

Figure 1. ADC operation based on successive approximation principle



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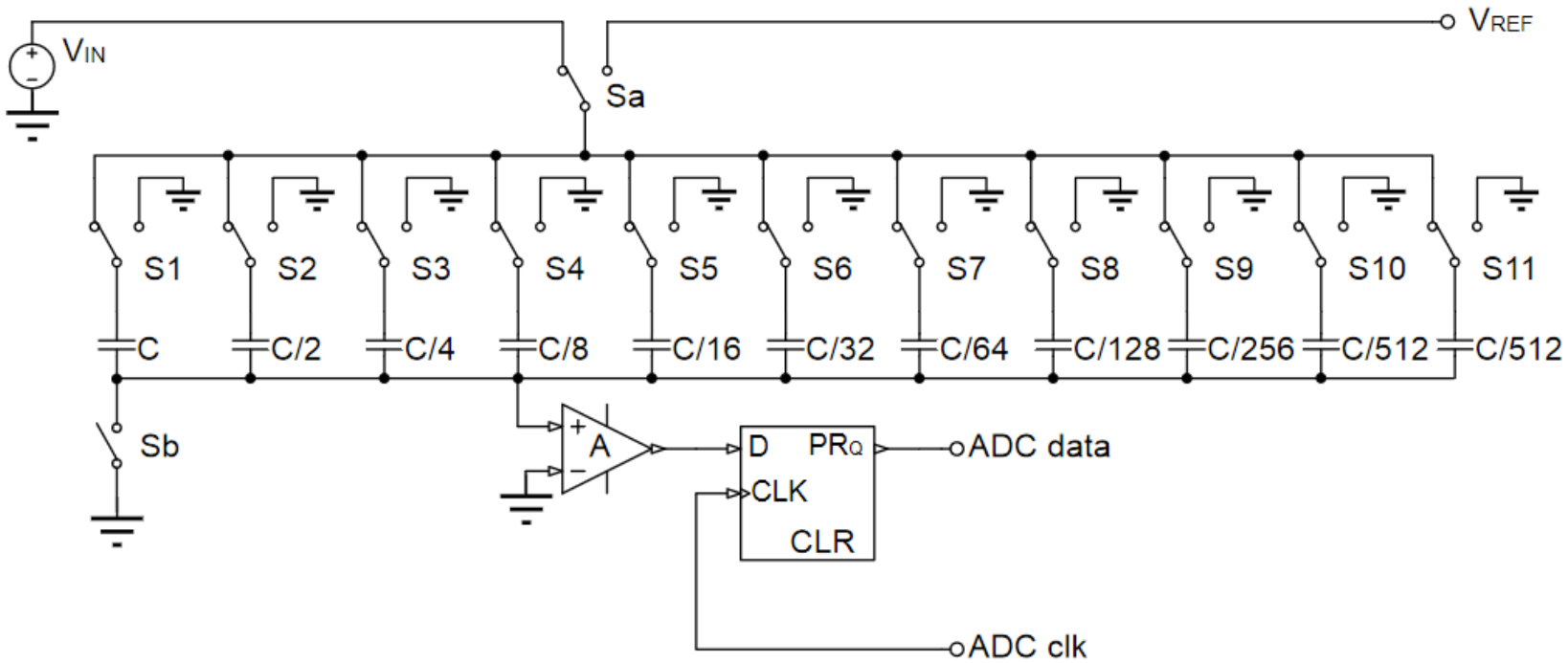
A/D pretvorniki pri mikrokrmilnikih

Figure 2. Basic schematic of SAR switched-capacitor ADC (10-bit ADC example)



Note: This is a schematic of an ADC with digital output.

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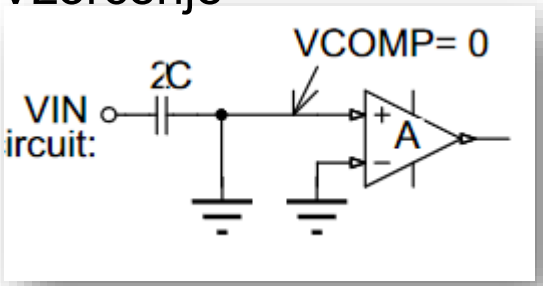
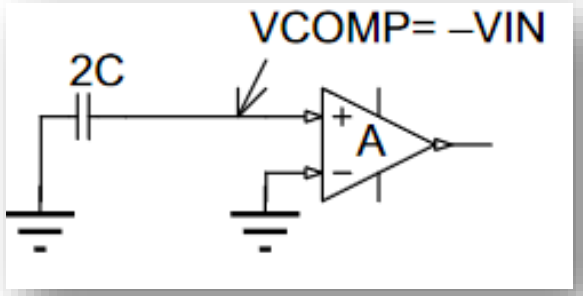
A/D pretvorniki pri mikrokrmilnikih

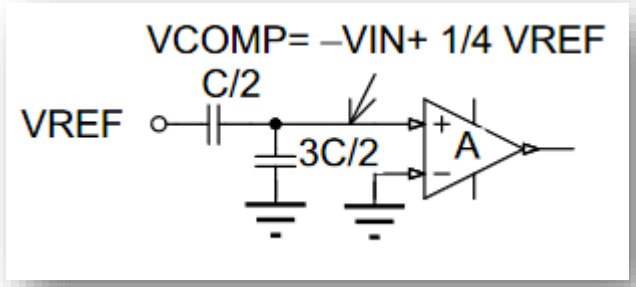
Vzorčenje



Zadrževanje

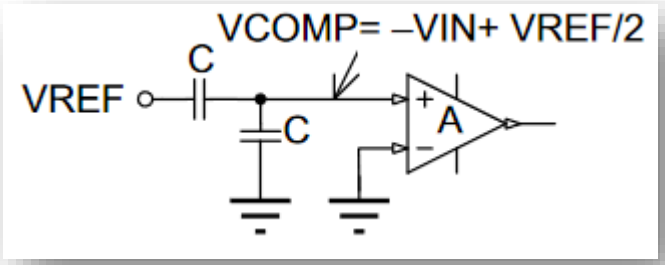


Primerjava z ¼ Vref



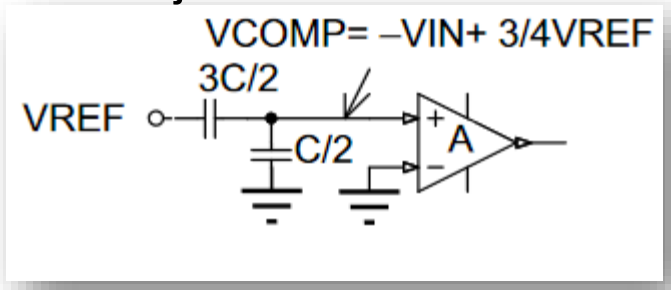
MSB = 0

Primerjava za MSB



MSB = 1

Primerjava z ¾ Vref



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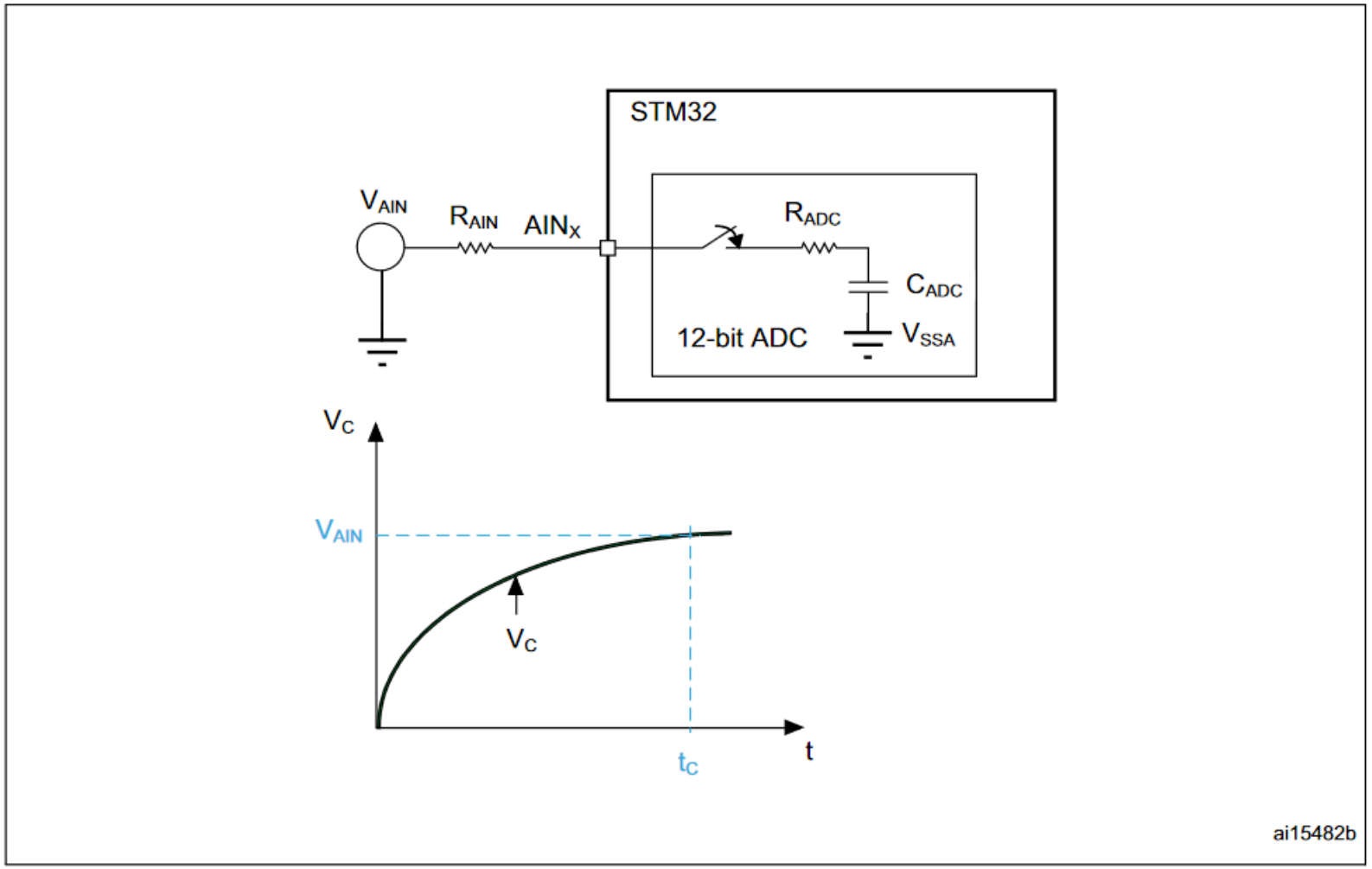
Analogno ekvivalentno vezje ADCD

Figure 15. Analog signal source resistance effect



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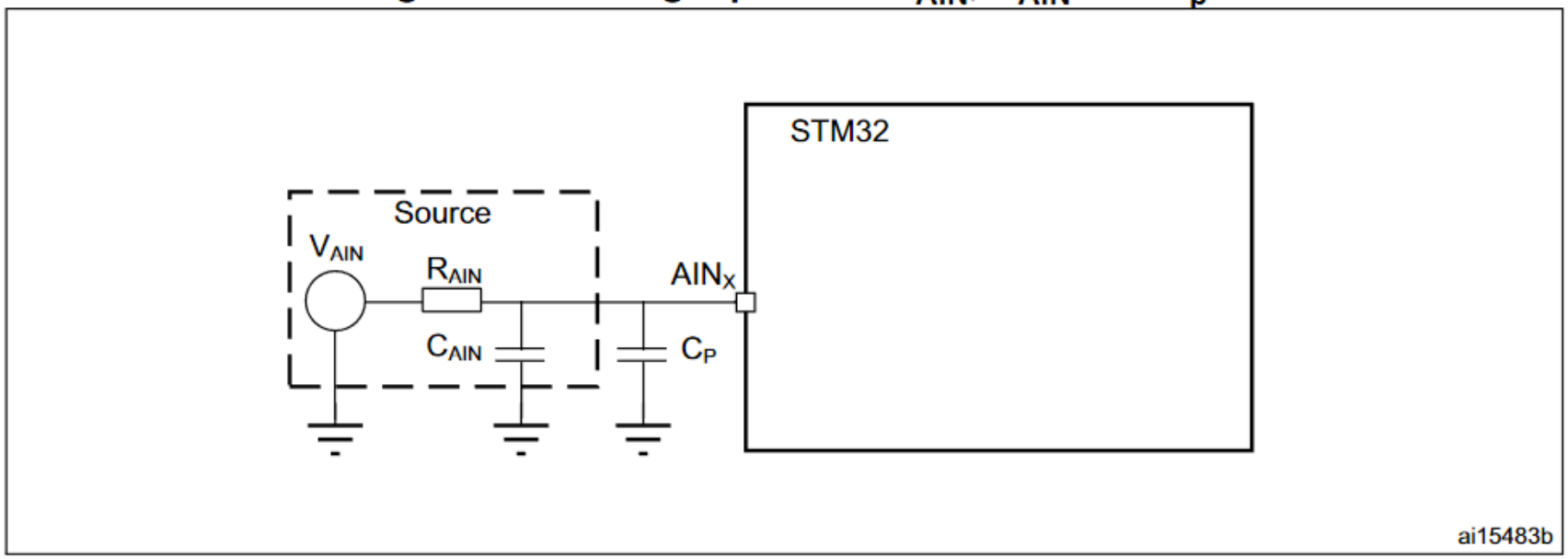
Vplivi dodatne ali parazitne zunanje kapacitivnosti

Figure 16. Analog input with R_{AIN}, C_{AIN} and C_p



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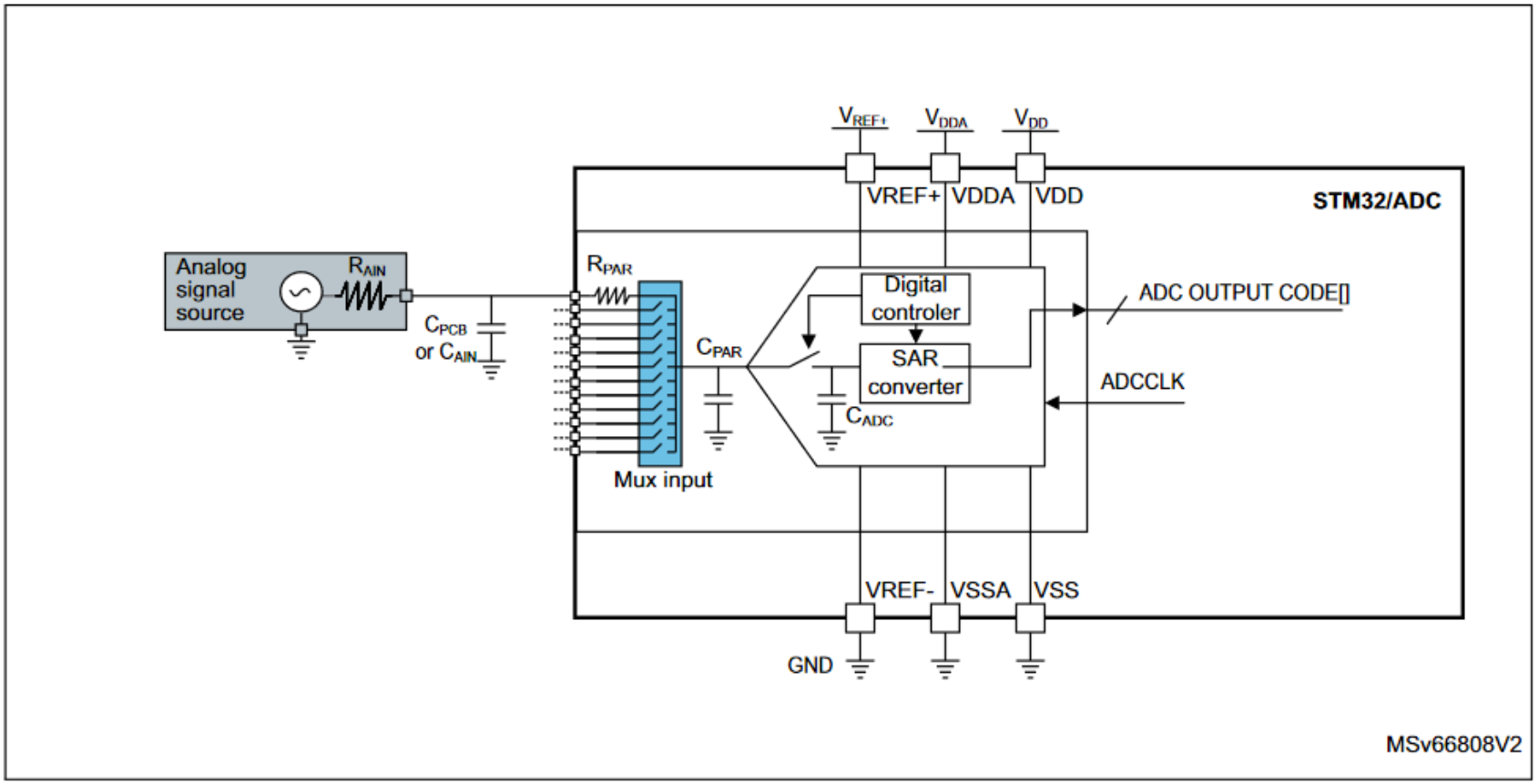
Določanje časa vzorčenja

Figure 26. Simplified external/internal SAR ADC sampling diagram



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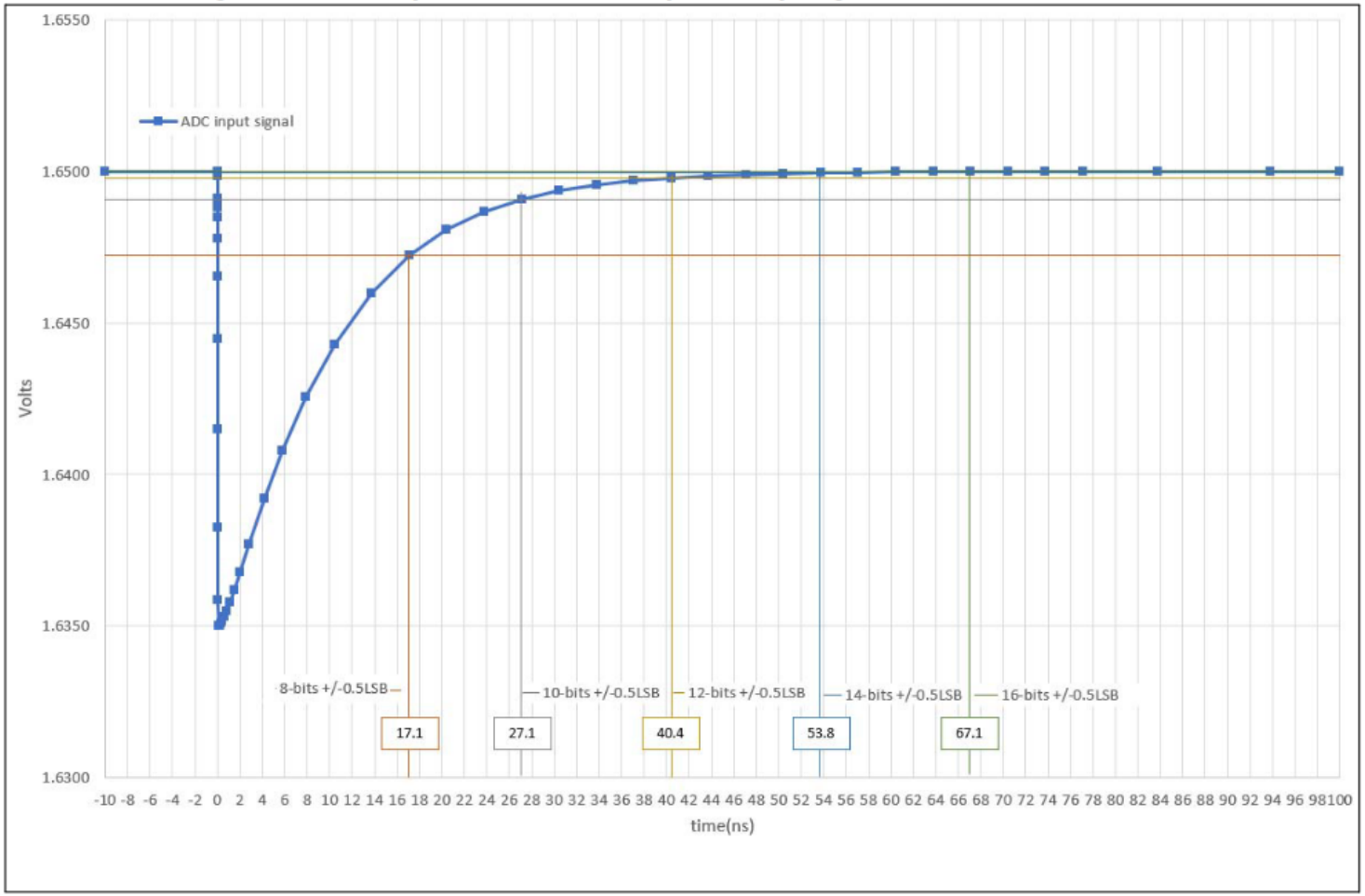
Določanje časa vzorčenja

Figure 27. Example of SAR ADC input sampling time vs ADC resolution



1. The above results are obtained in the following conditions:
   V_{REF+} = 2 V
   R_{AIN} = 1 kΩ
   C_{AIN}/C_{PCB} = 2 nF

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Določanje časa vzorčenja

Table 6. Minimum ADC conversion time (T_{SMPL} + T_{SAR}) vs resolution and maximum error (in ADC clock cycles)

Acquisition accuracy	8 bits	10 bits	12 bits	14 bits	16 bits
± 0.5 LSB	13	14	23	24	25
± 1 LSB	7	14	15	24	25
± 2 LSB	6	14	15	24	25
± 3 LSB	6	14	15	16	25

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Problem pri visokoimpedančnih virih

Figure 37. Typical voltage source connection to ADC input

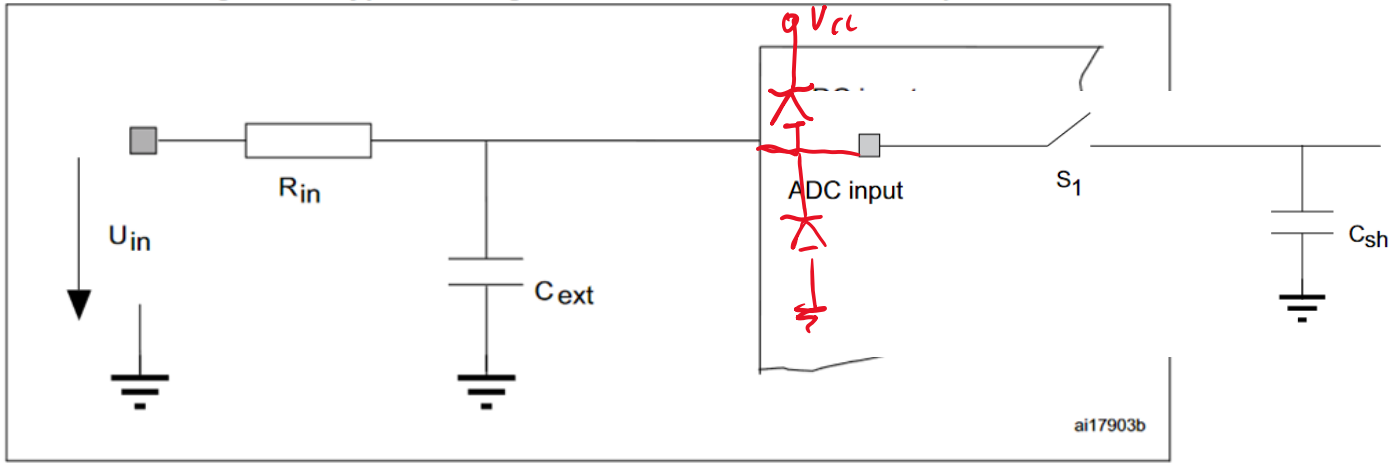
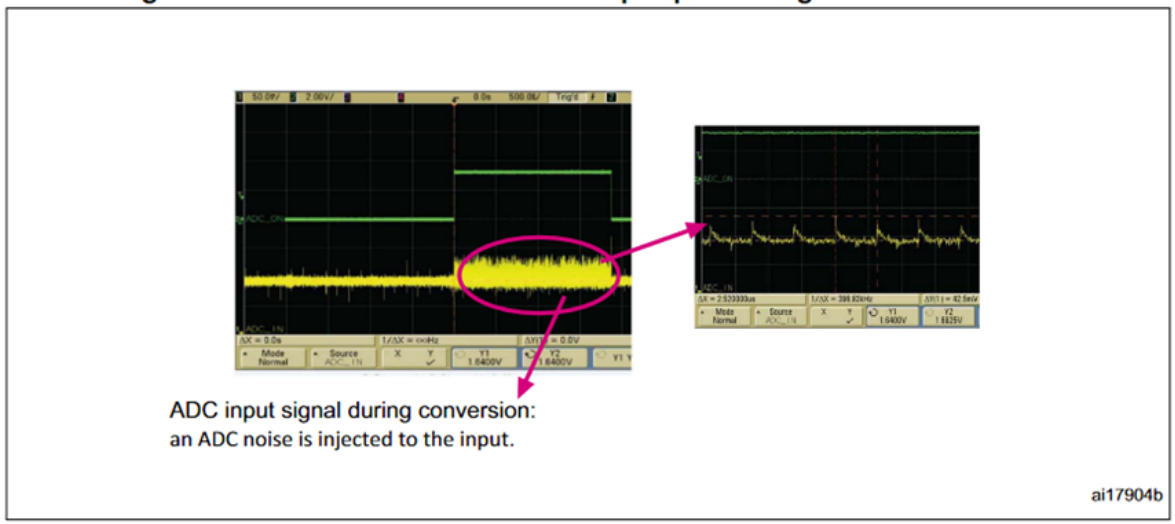


Figure 38. Noise observed on ADC input pin during ADC conversions



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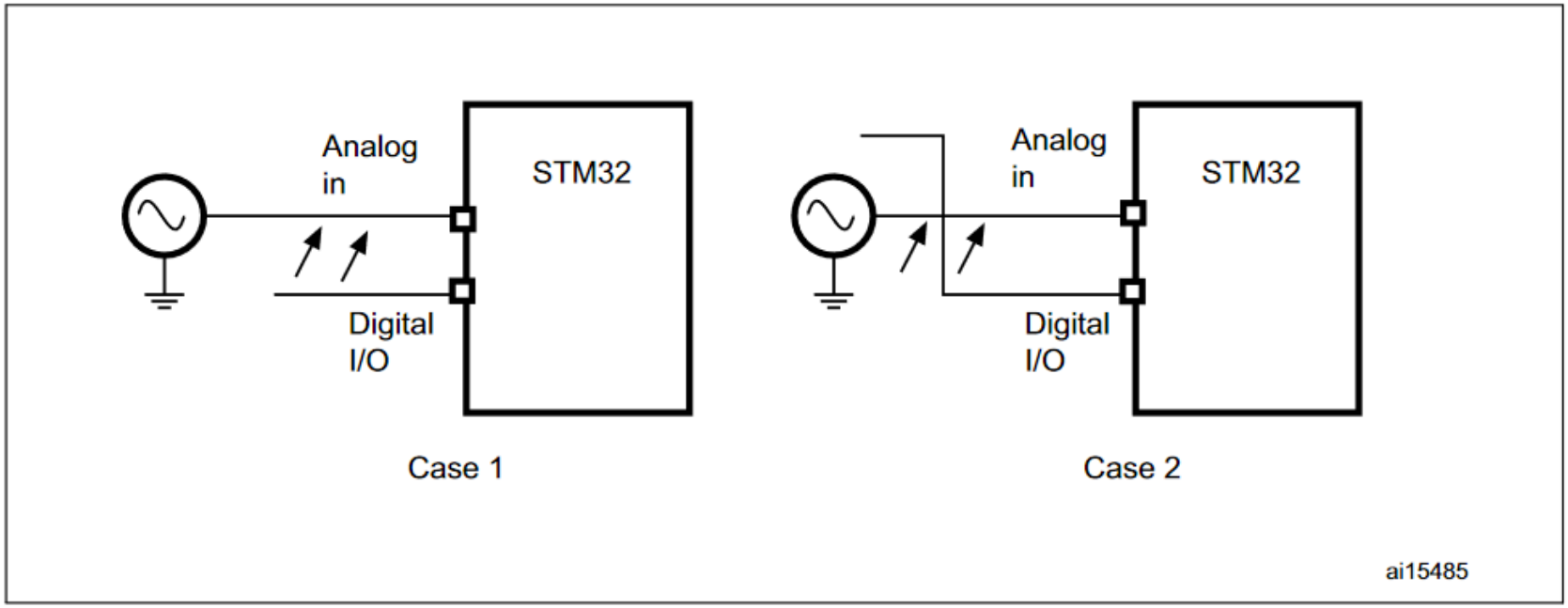
Presluhi med vhodi (analognimi/digitalnimi)

Figure 18. Crosstalk between I/O pins



1. Case 1: Digital and analog signal tracks that pass close to each other.
2. Case 2: Digital and analog signal tracks that cross each other on a different PCB side.

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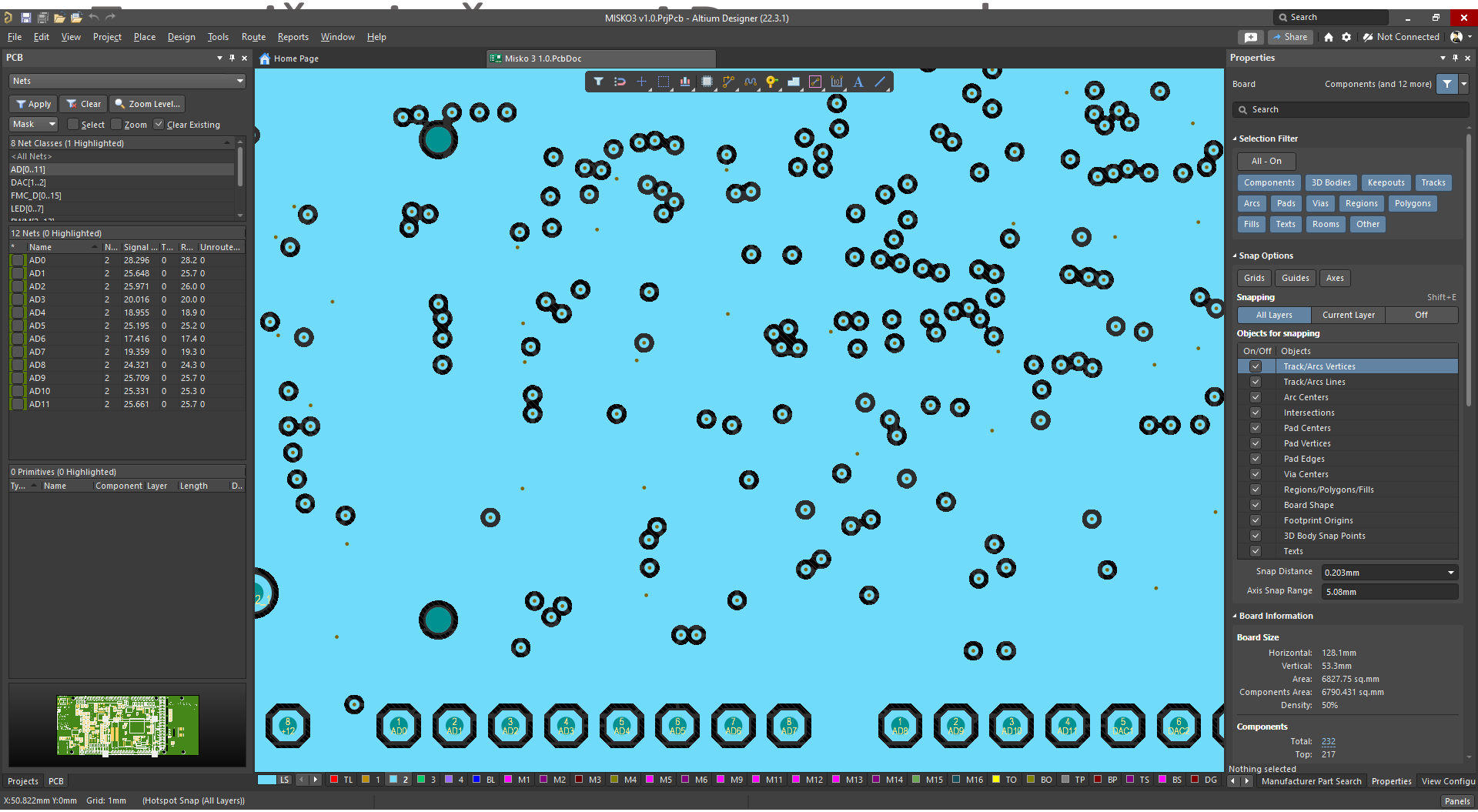
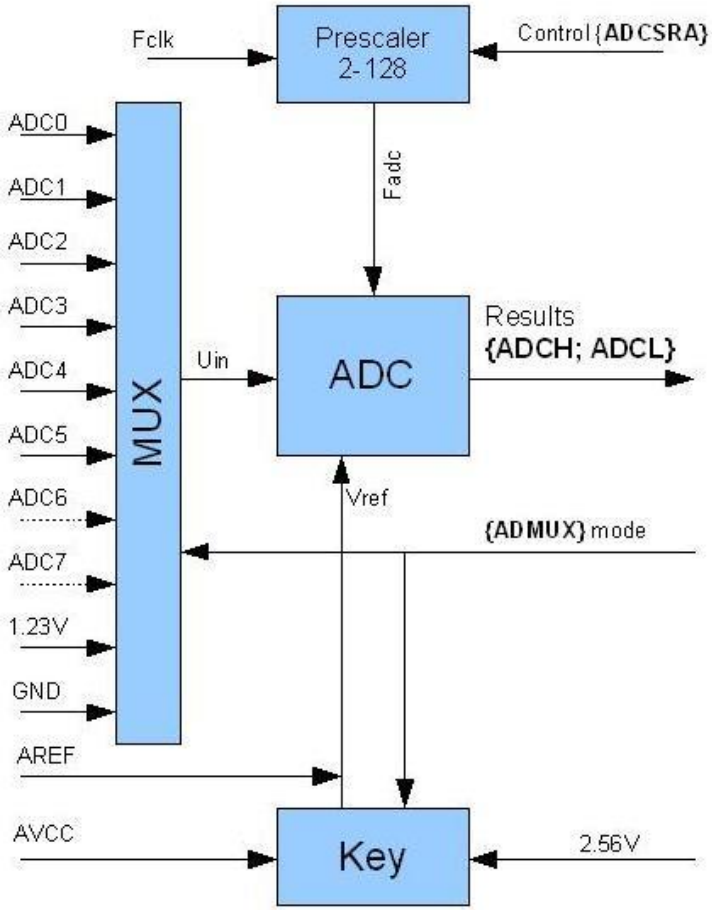
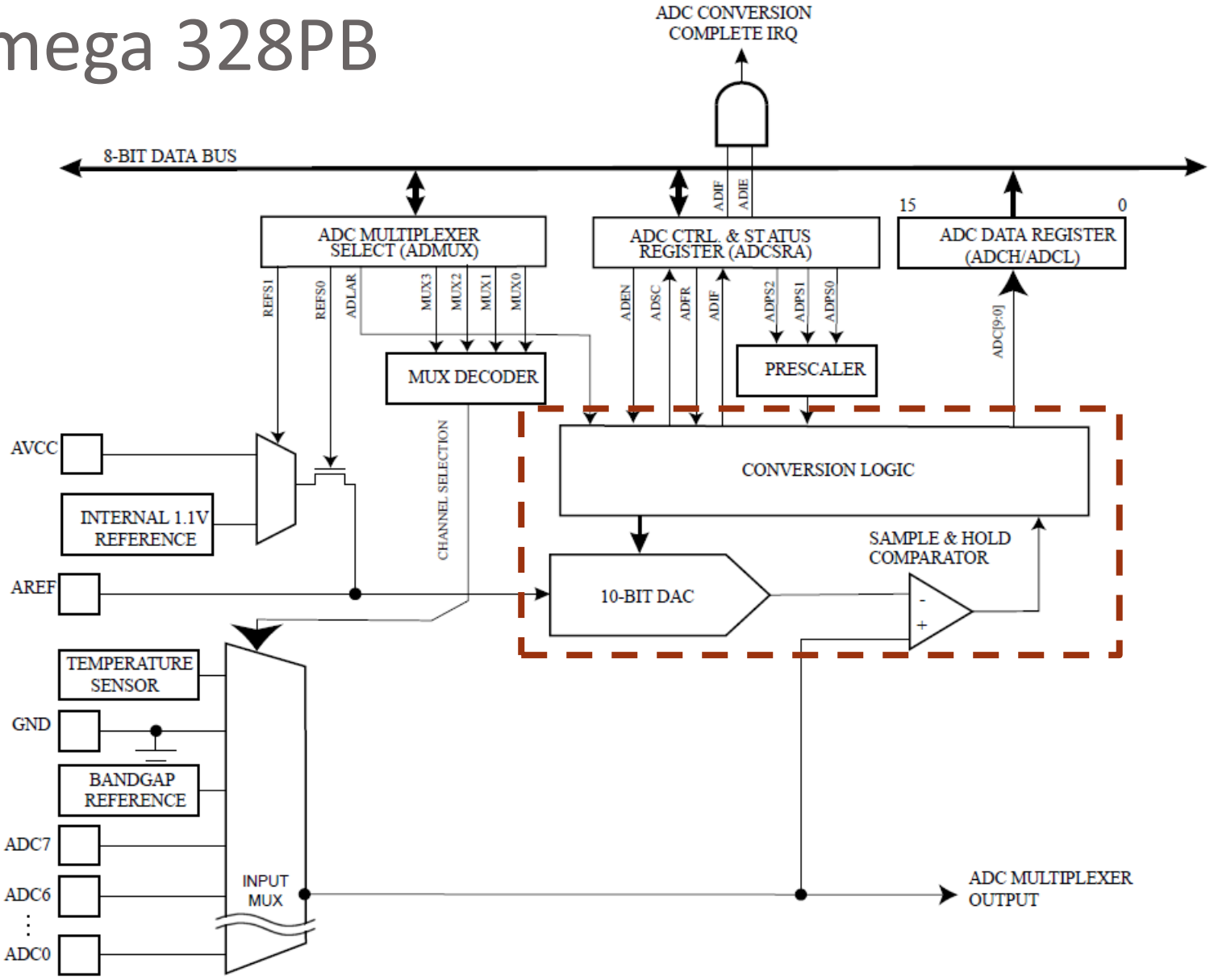

MISKO3 v1.0.PrjPcb - Altium Designer (22.3.1)
File Edit View Project Place Design Tools Route Reports Window Help
Home Page
Misko 3 1.0.PcbDoc
PCB
Nets
Apply Clear Zoom Level...
Mask Select Zoom Clear Existing
8 Net Classes (1 Highlighted)
<All Nets>
AD[0..11]
DAC[1..2]
FMC_D[0..15]
LED[0..7]
12 Nets (0 Highlighted)
Name N... Signal ... T... R... Unroute...
AD0 2 28.296 0 28.2 0
AD1 2 25.648 0 25.7 0
AD2 2 25.971 0 26.0 0
AD3 2 20.016 0 20.0 0
AD4 2 18.955 0 18.9 0
AD5 2 25.195 0 25.2 0
AD6 2 17.416 0 17.4 0
AD7 2 19.359 0 19.3 0
AD8 2 24.321 0 24.3 0
AD9 2 25.709 0 25.7 0
AD10 2 25.331 0 25.3 0
AD11 2 25.661 0 25.7 0
0 Primitives (0 Highlighted)
Ty... Name Component Layer Length D...
Properties
Board Components (and 12 more)
Search
Selection Filter
All - On
Components 3D Bodies Keepouts Tracks
Arcs Pads Vias Regions Polygons
Fills Texts Rooms Other
Snap Options
Grids Guides Axes
Snapping Shift+E
All Layers Current Layer Off
Objects for snapping
On/Off Objects
Track/Arcs Vertices
Track/Arcs Lines
Arc Centers
Intersections
Pad Centers
Pad Vertices
Pad Edges
Via Centers
Regions/Polygons/Fills
Board Shape
Footprint Origins
3D Body Snap Points
Texts
Snap Distance 0.203mm
Axis Snap Range 5.08mm
Board Information
Board Size
Horizontal: 128.1mm
Vertical: 53.3mm
Area: 6827.75 sq.mm
Components Area: 6790.431 sq.mm
Density: 50%
Components
Total: 232
Top: 217
Nothing selected
Projects PCB
Manufacturer Part Search Properties View Configu
X:50.822mm Y:0mm Grid: 1mm (Hotspot Snap (All Layers))
Panels

A/D pretvornik pri ATmega 328PB (ADC)

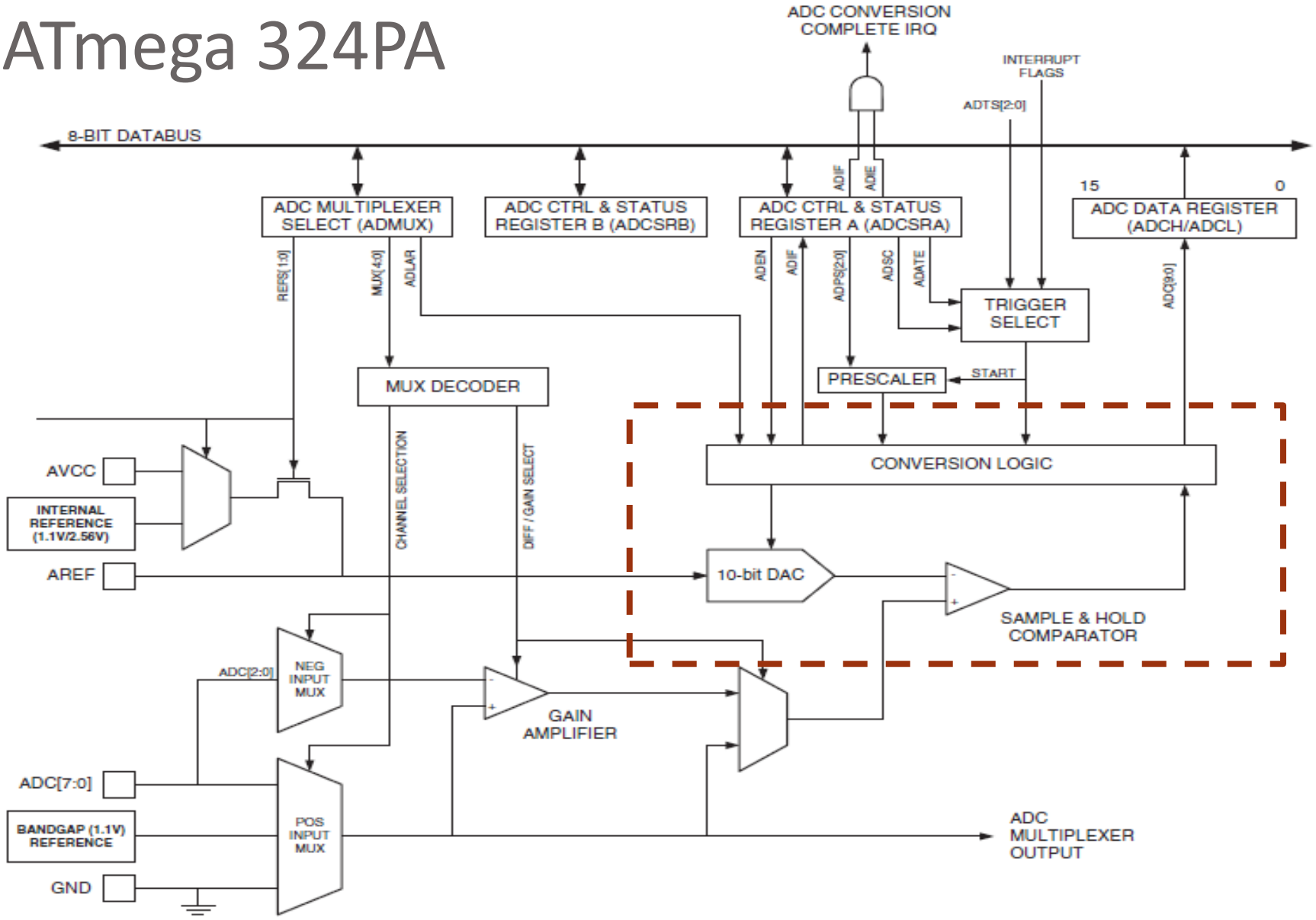
- Resolucija 10 bit
- Integralna nelinearnost 0,5 LSB
- Absolutna napaka ±2 LSB
- Čas pretvorbe 13 – 260 µs
- Hitrost pretvorbe do 15 000 vzorcev/s
- 6 multipleksiranih vhodov
- Senzor temperature
- Različni viri referenčne napetosti
  - Notranja referenca 1.1 V
  - Zunanji vir
  - Napajalna napetost AVcc
- Avtomatsko proženje iz različnih virov prekinitev



ATmega 328PB

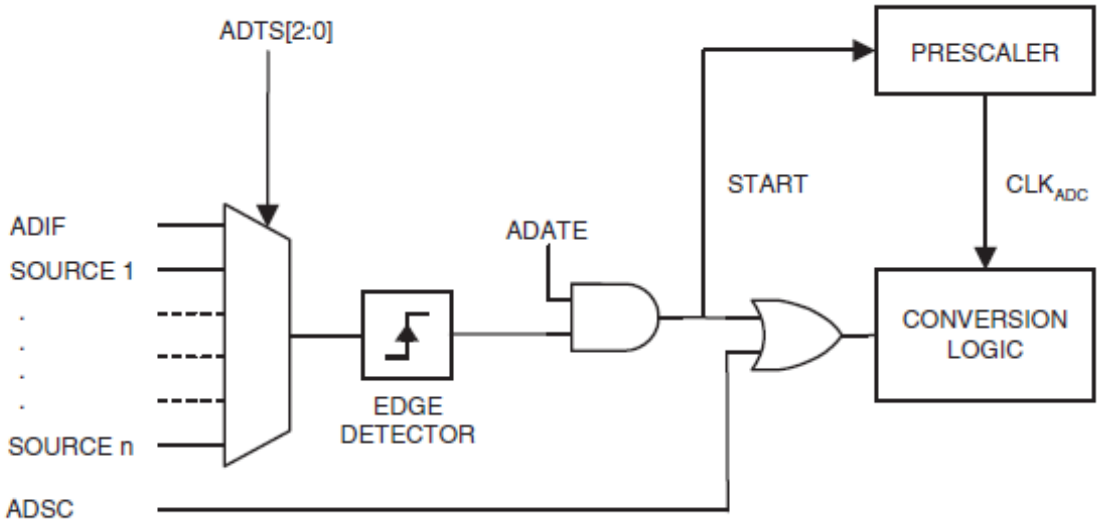


ATmega 324PA



Viri proženja pretvorbe

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free Running mode
0	0	1	Analog Comparator
0	1	0	External Interrupt Request 0
0	1	1	Timer/Counter0 Compare Match A
1	0	0	Timer/Counter0 Overflow
1	0	1	Timer/Counter1 Compare Match B
1	1	0	Timer/Counter1 Overflow
1	1	1	Timer/Counter1 Capture Event

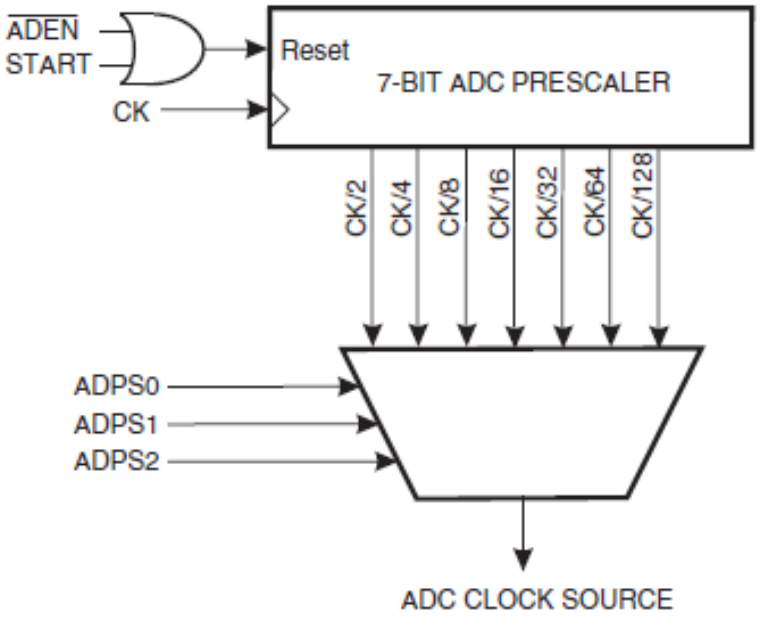


Bit	7	6	5	4	3	2	1	0	
(0x7A)	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
(0x7B)	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	ADCSRB
Read/Write	R	R/W	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Čas pretvorbe

- Frekvenca med 50 in 200 kHz za maksimalno 10-bit resolucijo
- Čas pretvorbe
  - za prvo pretvorbo – 25 cikov
    - S/H 14,5 ciklov
  - za vse nadaljne pretvorbe: 13-14 ciklov
    - S/H 1,5-2,5 cikla

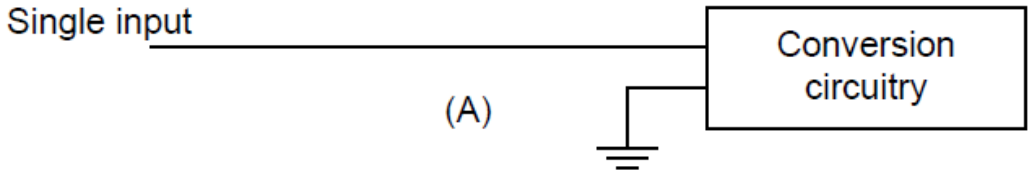


Bit	7	6	5	4	3	2	1	0	
(0x7A)	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Rezultat pretvorbe

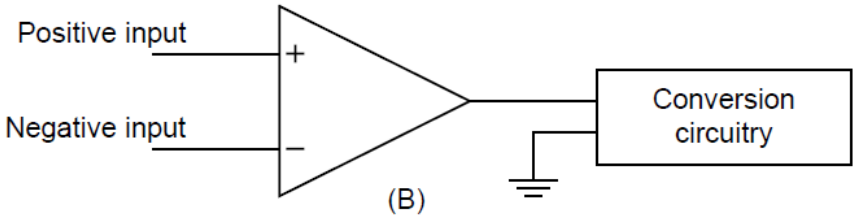
- Merjenje proti masi

$$ADC = \frac{U_{IN}}{U_{REF}} 1024$$



- Diferencialno merjenje

$$ADC = \frac{U_{INp} - U_{INn}}{U_{REF}} \; GAIN \; 512$$



Podatki ADC

33.9 ADC Characteristics

Table 33-10. ADC Characteristics

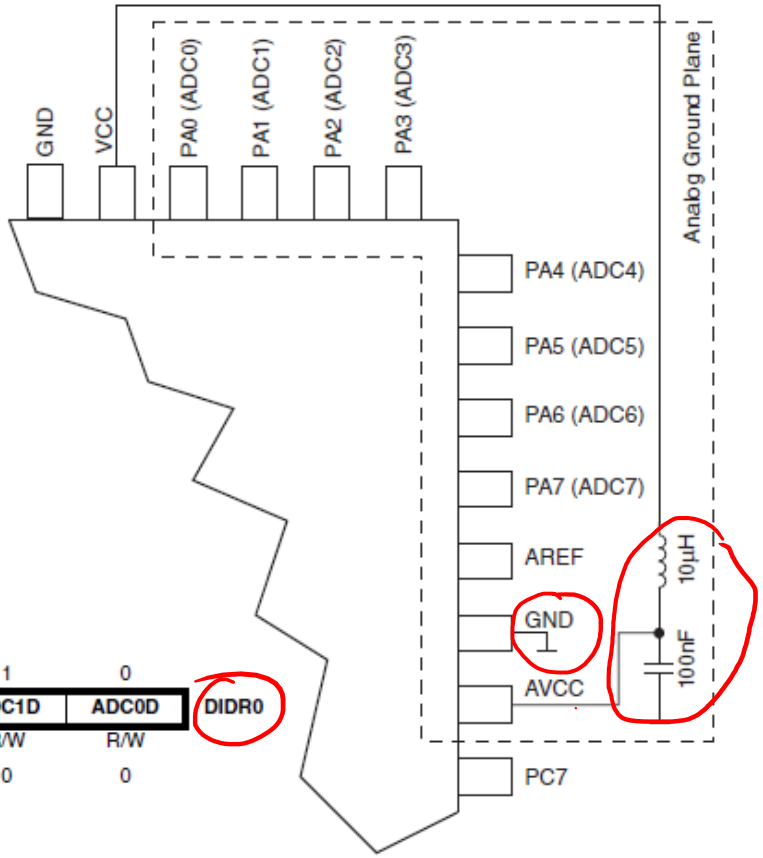
Symbol	Parameter	Condition	Min.	Typ	Max	Units
	Resolution		-	10	-	Bits
TUE	Absolute accuracy (Including INL, DNL, quantization error, gain and offset error)	V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz	-	2	-	LSB
		V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 1MHz	-	4	-	LSB
		V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz Noise Reduction Mode	-	2	-	LSB
		V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 1MHz Noise Reduction Mode	-	4	-	LSB
INL	Integral Non-Linearity	V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz	-	0.5	-	LSB
DNL	Differential Non-Linearity	V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz	-	0.25	-	LSB
	Gain Error	V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz	-	2	-	LSB
	Offset Error	V_{REF} = 4V, V_{CC} = 4V, clk_{ADC} = 200kHz	-	2	-	LSB
	Conversion Time	Free Running Conversion	13	-	260	µs
	Clock Frequency		50	-	1000	kHz
AV_{CC}(1)	Analog Supply Voltage		V_{CC} - 0.3	-	V_{CC} + 0.3	V
V_{REF}	Reference Voltage		1.0	-	AV_{CC}	V
V_{IN}	Input Voltage		GND	-	V_{REF}	V
	Input Bandwidth		-	38.5		kHz
V_{INT}	Internal Voltage Reference		1.0	1.1	1.2	V
R_{REF}	Reference Input Resistance		-	50	-	kΩ
R_{AIN}	Analog Input Resistance		-	100	-	MΩ

Zmanjšanje šuma ADC

- ADC noise reduction mode
- Pogoji
  - omogočen ADC noise reduction način (SM2..0 = 001)
  - ročno proženje pretvorbe (ADATE = 0)
  - omogočena prekinitev ob končani pretvorbi (ADIE = 1)
- Sprožitev AD pretvorbe
  - ADC mora biti omogočen (ADEN = 1)
  - pretvorbo sproži ASM ukaz „sleep“
  - procesor gre v stanje nizke porabe (koda se ne izvaja)
  - zbudi ga prekinitev ob končani pretvorbi

Zmanjšanje šuma ADC

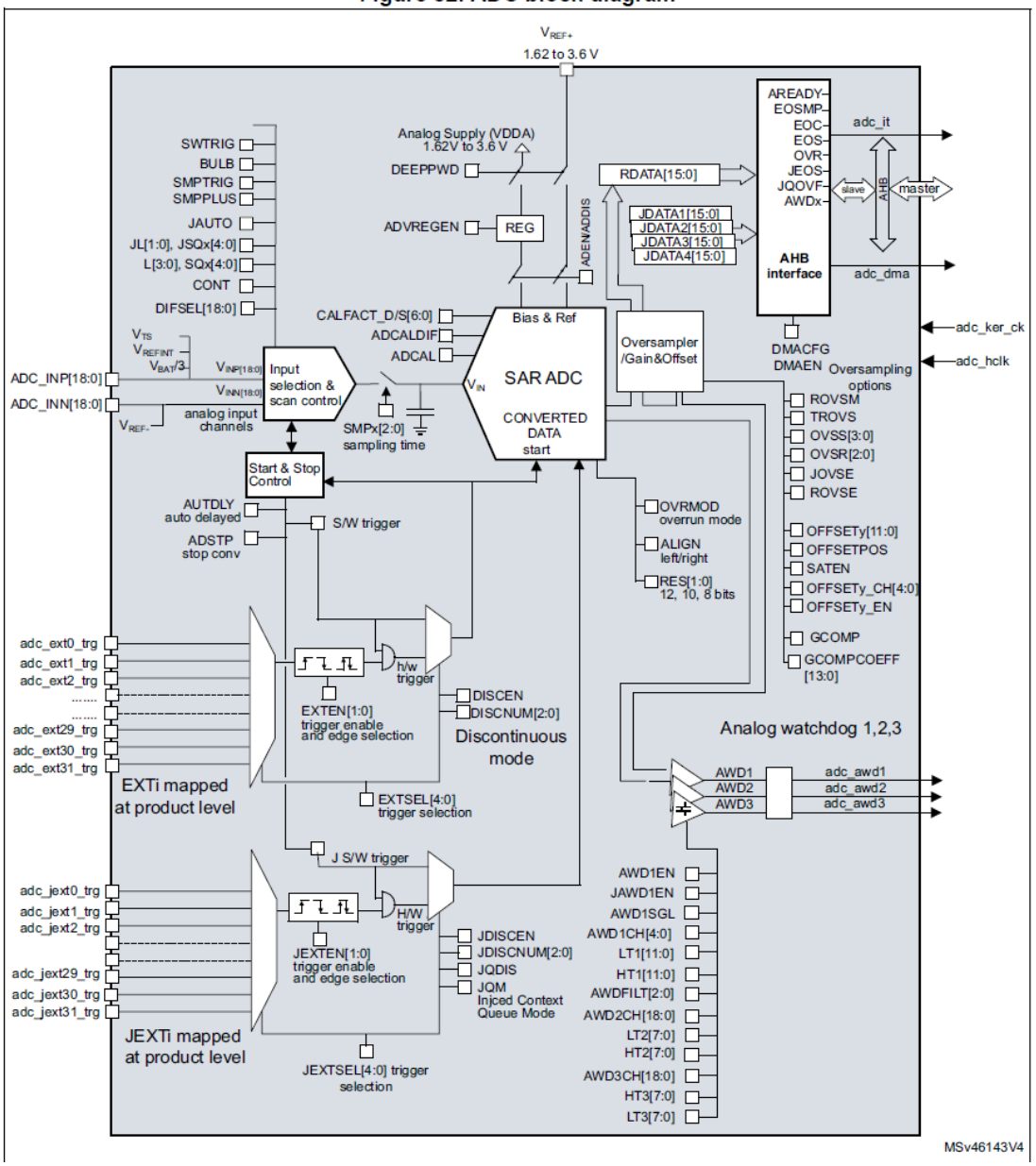
- Analogne povezave naj bodo čim krajše
- AVCC povezan na VCC preko LC filtra
- Uporaba ADC noise canceller načina
- Če so vhodi ADC uporabljeni hkrati kot I/O pini, jih ne preklapljati v času pretvorbe
- Onemogočitev vhodnih digitalnih ojačevalnikov I/O pinov



Bit	7	6	5	4	3	2	1	0	
(0x7E)	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	DIDR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

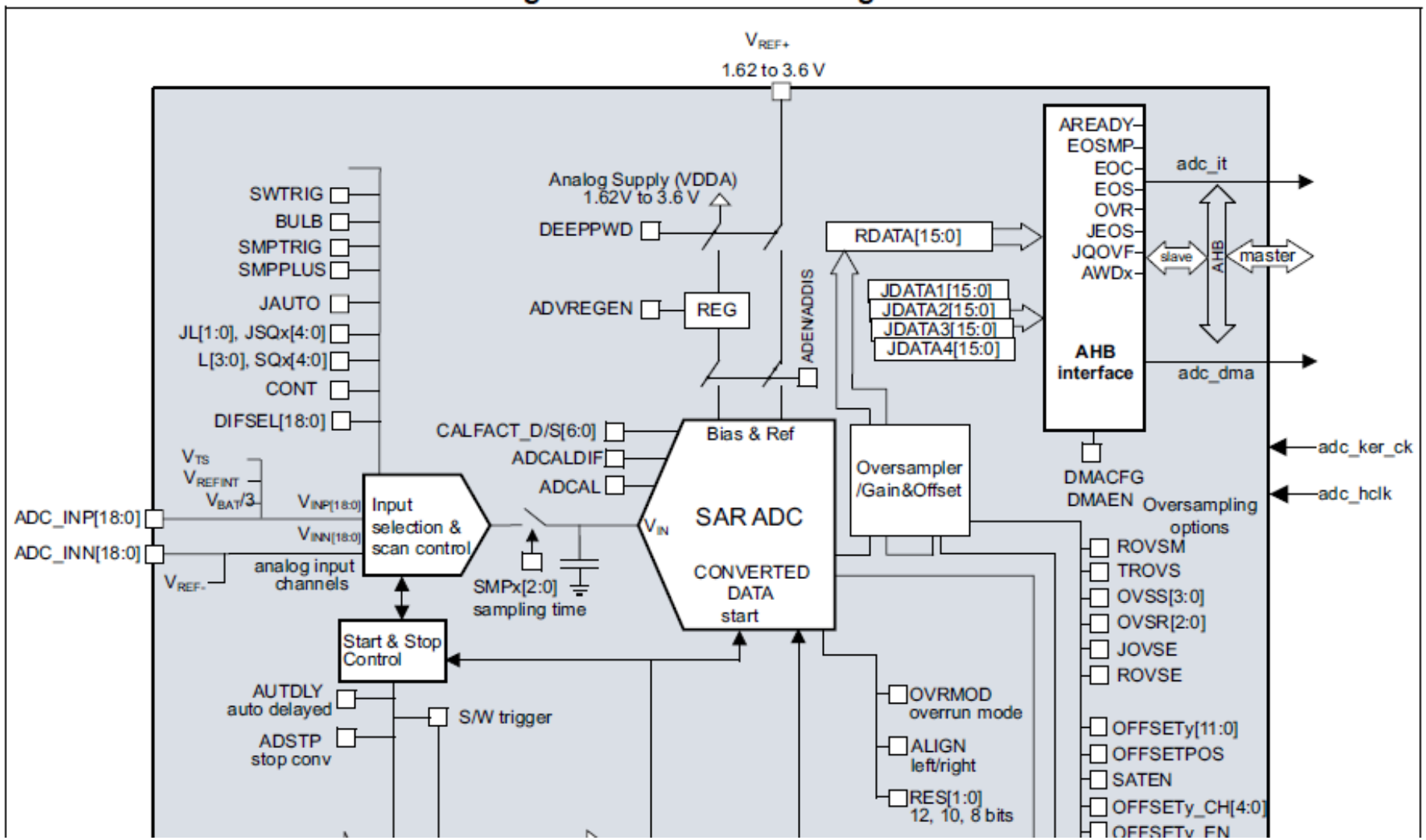
STM32G4 ADC

Figure 82. ADC block diagram

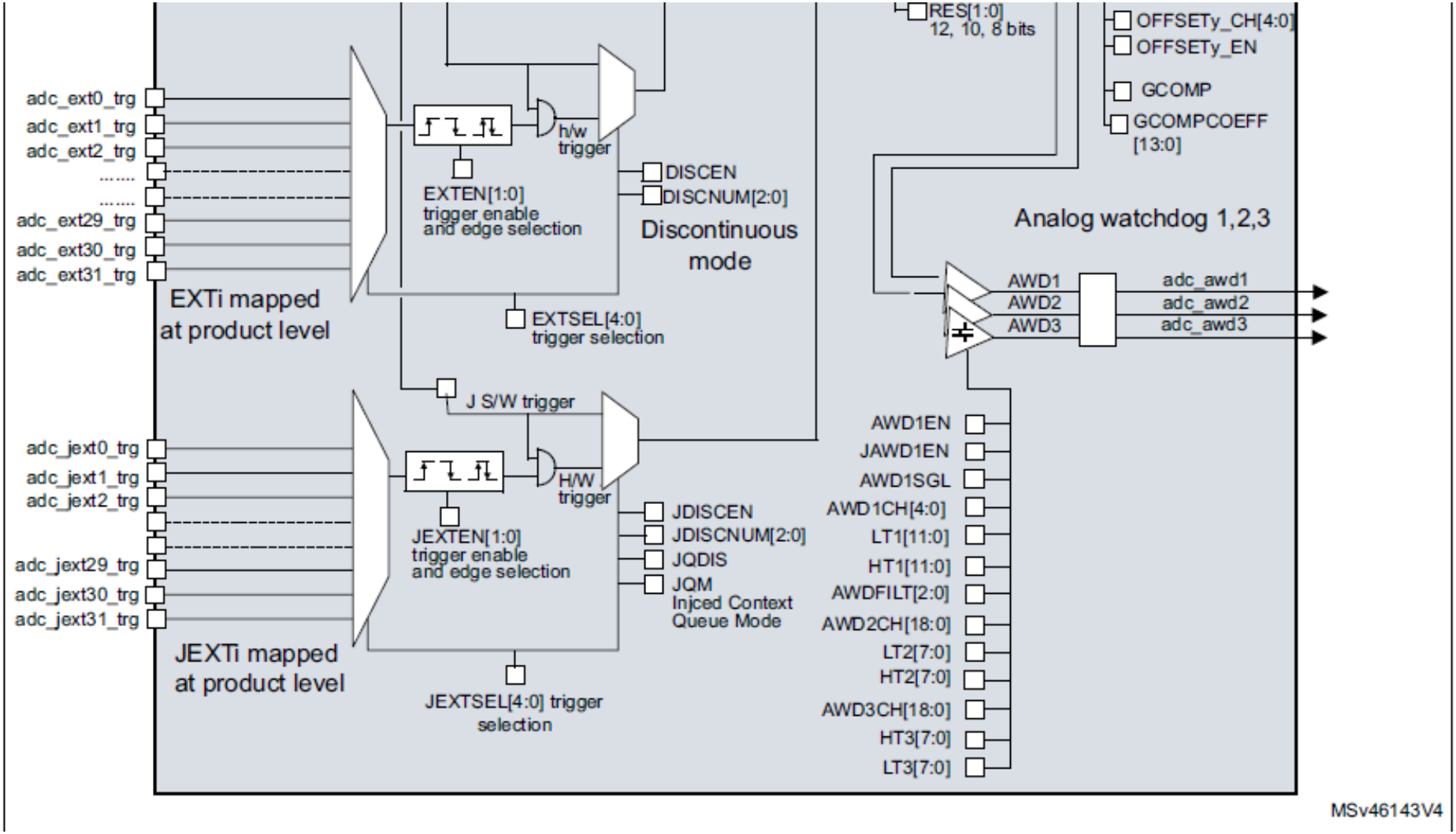


STM32G4 ADC (1)

Figure 82. ADC block diagram



STM32G4 ADC (2)



Osnovne lastnosti

- 12, 10, 8 in 6-bitna konverzija
- Enojni ali diferencialni vhodi
- Počasni in hitri kanali
- Zunanji in notranji kanali
- Notranja in zunanja napetostna referenca
- Nastavljiv čas vzorčenja
- Programsko in strojno proženje rpetvorbe
- Regularni in vstavljeni kanali
- Samokalibracija
- Prevzorčenje
- Načini delovanja z nizko porabo
- Analogni rotvajler (watchdog)
- Združevanje ADC

Osnovne lastnosti

Table 66. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
V_{CMIN}	Input common mode	Differential	$(V_{REF+}+V_{REF-})/2 - 0.18$	$(V_{REF+} + V_{REF-})/2$	$(V_{REF+} + V_{REF-})/2 + 0.18$	V
f_{ADC}	ADC clock frequency	Range 1, single ADC operation	0.14	-	60	MHz
		Range 2	-	-	26	
		Range 1, all ADCs operation, single ended mode $V_{DDA} \geq 2.7$ V	0.14	-	52	
		Range 1, all ADCs operation, single ended mode $V_{DDA} \geq 1.62$ V	0.14	-	42	
		Range 1, all ADCs operation, differential mode $V_{DDA} \geq 1.62$ V	0.14	-	56	

Hitrost pretvorbe

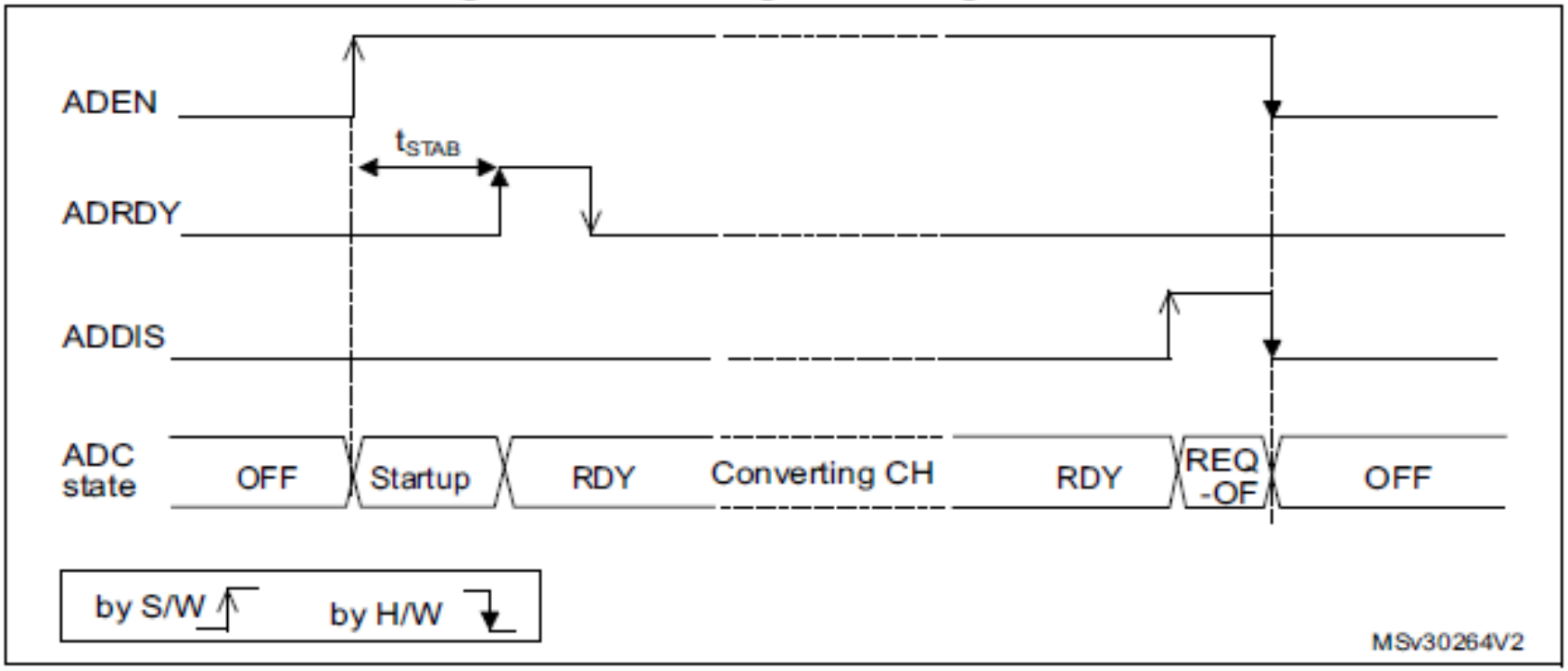
- Čas vzorčenja (sample time):

000: 2.5 ADC clock cycles
001: 6.5 ADC clock cycles
010: 12.5 ADC clock cycles
011: 24.5 ADC clock cycles
100: 47.5 ADC clock cycles
101: 92.5 ADC clock cycles
110: 247.5 ADC clock cycles
111: 640.5 ADC clock cycles

- Frekvenca ure AD:
  - $f_{AD_{maks}} = 60\ MHz \rightarrow 1\ cikel = 16{,}6\ ns$
- Čas pretvorbe
  - $t_{conv} = t_{samp} + Q + 0{,}5$
  - $t_{conv_{min}@12-bit} = 2{,}5 + 12 + 0{,}5 = 15\ ciklov \rightarrow 250\ \text{ns}$
- Vzorčna frekvenca
  - $f_{samp} = \frac{1}{t_{conv}}, \quad f_{samp_{maks}@12-bit} = 4\ \text{MHz}$

Vklop/izklop ADC

Figure 92. Enabling / disabling the ADC



Rezultat pretvorbe

- Rezultat (enojni vhod)
  - $U_{in} = ADC \cdot \frac{U_{ref}}{2^Q}$

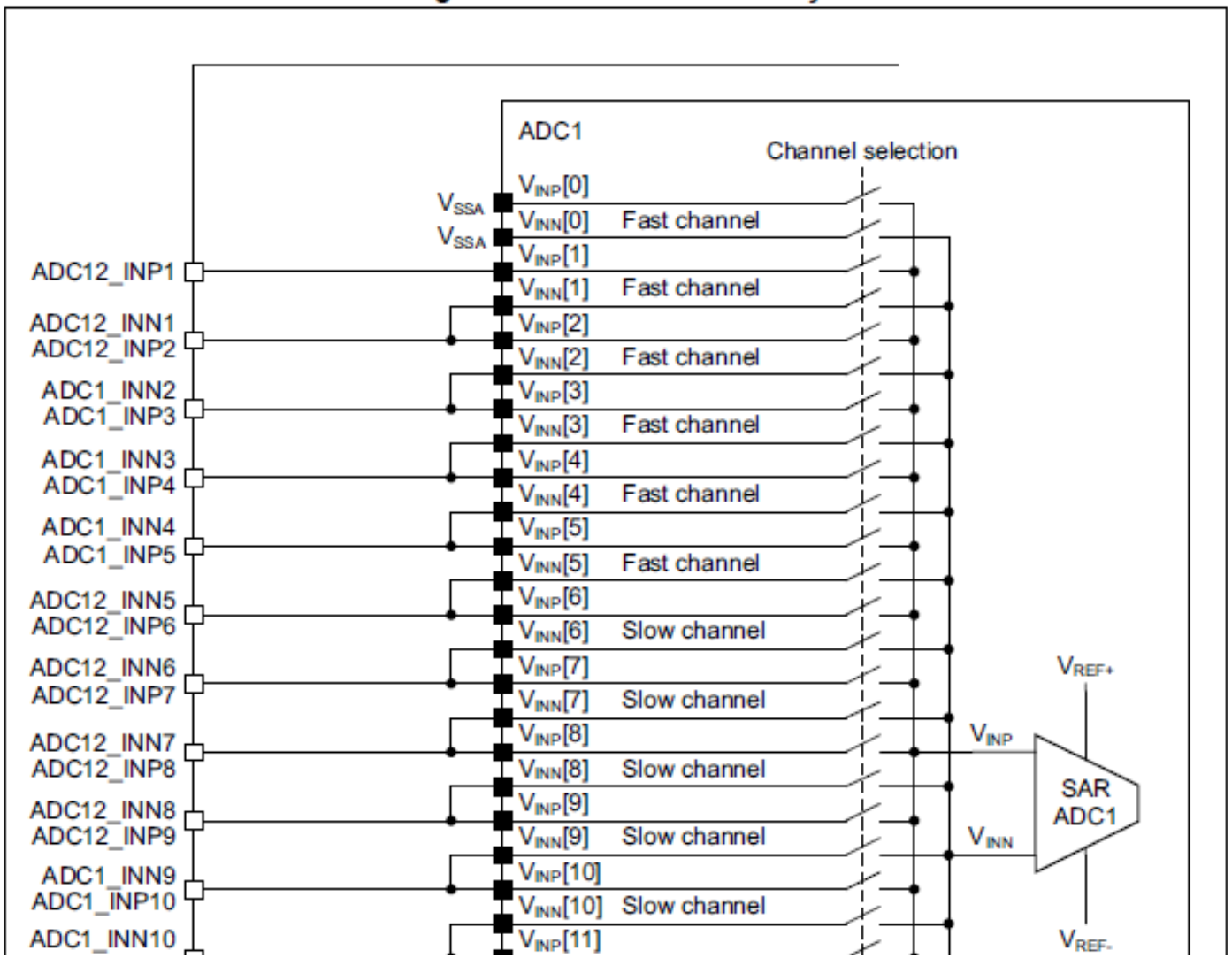
ADC	Uin
0x000	0
0xFFF	U_{ref}

- Rezultat (diferencialni vhod)
  - $U_{in} = (ADC - 2^{Q-1}) \cdot \frac{2 \cdot U_{ref}}{2^{Q-1}}$

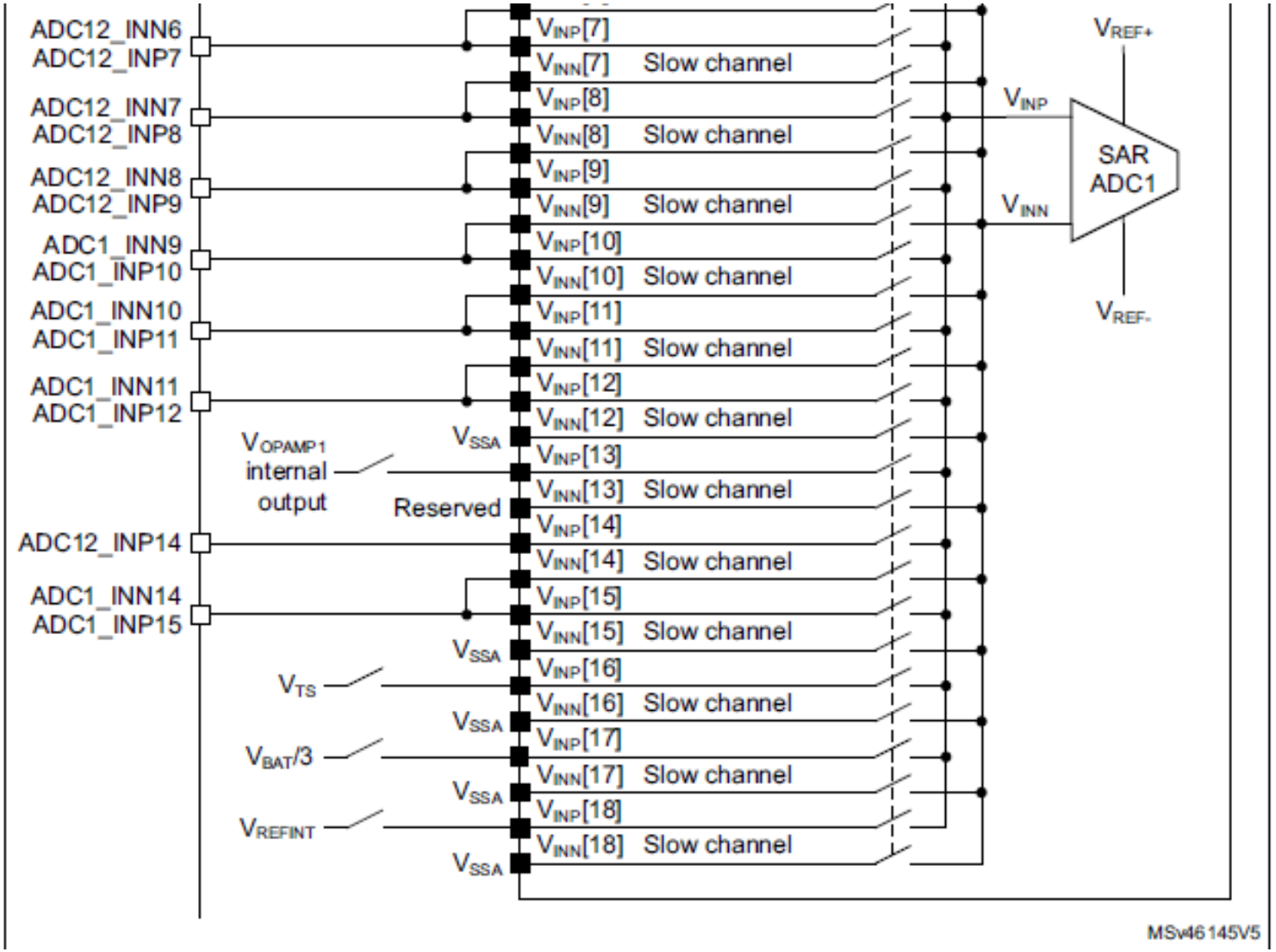
ADC	Uin
0x000	$-2 \cdot U_{ref}$
0x800	0
0xFFF	$2 \cdot U_{ref}$

Izbira vhodov

Figure 84. ADC1 connectivity



Izbira vhodov



Hitri in počasni kanali – fast and slow channels

Figure 84. ADC1 connectivity

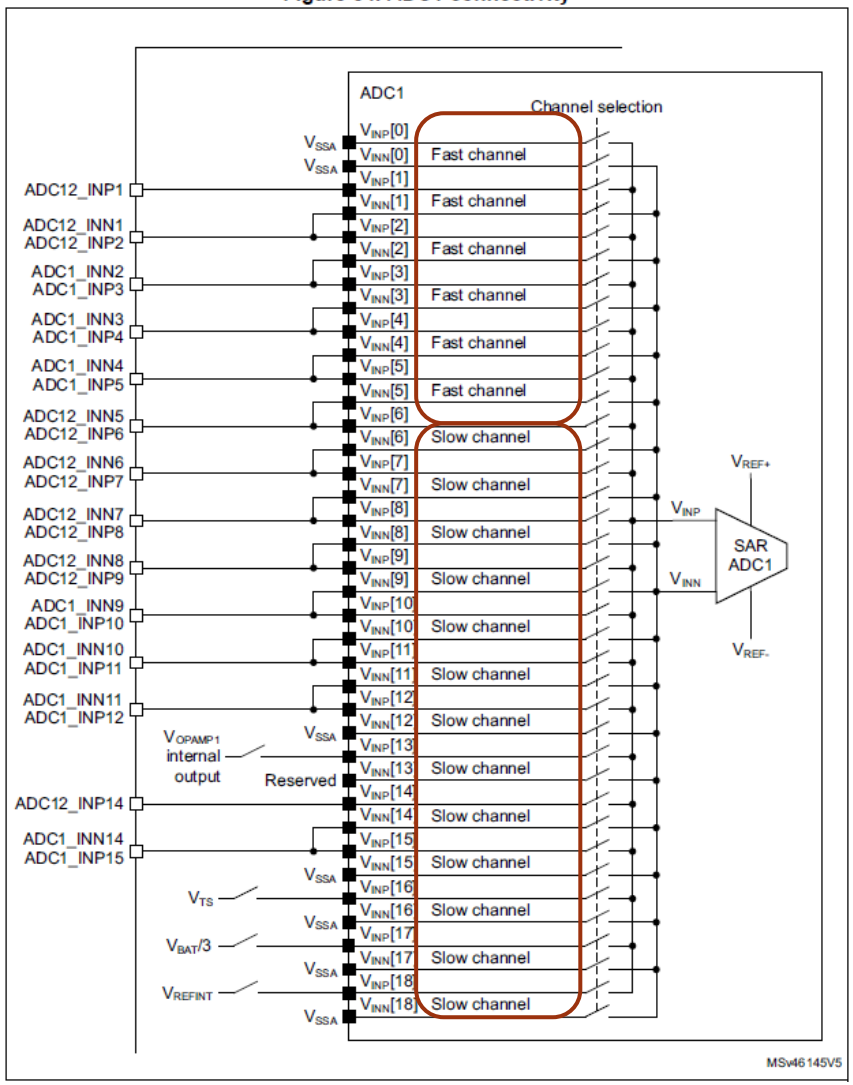
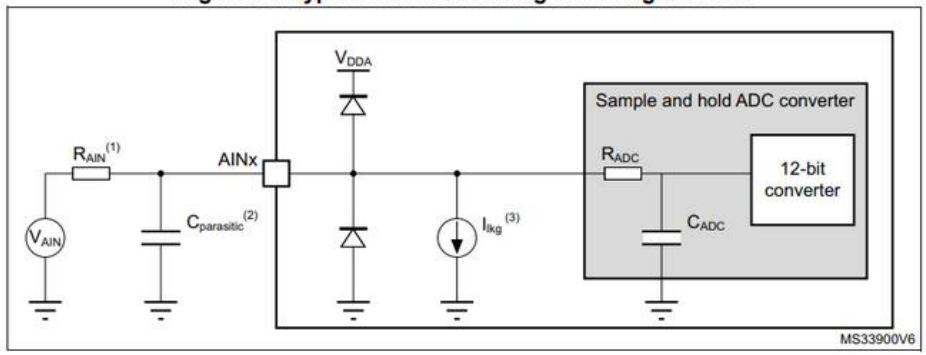


Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 66: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 54: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Page 142 gives R_{AIN} for different resolutions. 12-bit being:

Table 67. Maximum ADC R_{AIN} (1)(2)

Resolution	Sampling cycle @60 MHz	Sampling time [ns]	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	41.67	100	N/A
	6.5	108.33	330	100
	12.5	208.33	680	470
	24.5	408.33	1500	1200
	47.5	791.67	2200	1800
	92.5	1541.67	4700	3900
	247.5	4125	12000	10000
	640.5	10675	39000	33000

Skupine kanalov

Regularni (regular group)

- Do 16 pretvorb v skupina
- Poljuben vrstni red kanalov
- Med skeniranjem jih ne moreš spreminjat

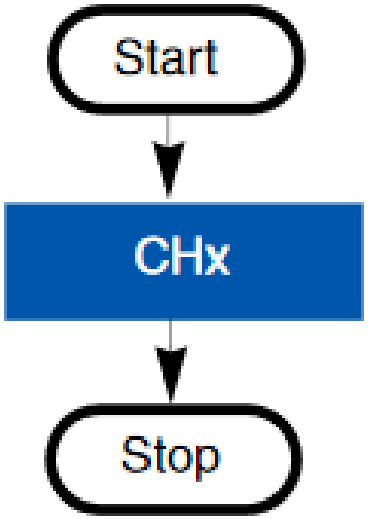
Vstavljeni (Injected group)

- Do 4 pretvorbe
- Proženi z dogodki (events)
- Lahko se spreminjajo med skeniranjem

Načini AD pretvorbe

- Diskretni način (single conversion mode)
  - Enkrat pretvori sekvenco kanalov
  - Programsko ali zunanje proženje
- Kontiunirani način (continuous conversion mode)
  - Samo za regularne kanale
  - Po pretvorbi sekvence začne takoj od začetka
- Prekinjeni način skeniranja (discontinuous mode)
  - Za regularne ali vstavljene kanale
  - Po zunanjem proženju pretvori del sekvence kanalov (n<8)
- Dvojni način delovanja (dual mode)

Single conversion mode



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Single conversion scan mode

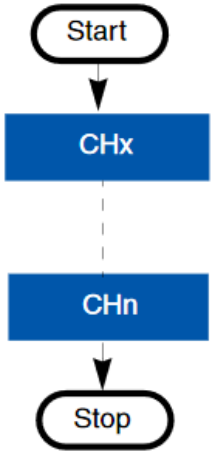
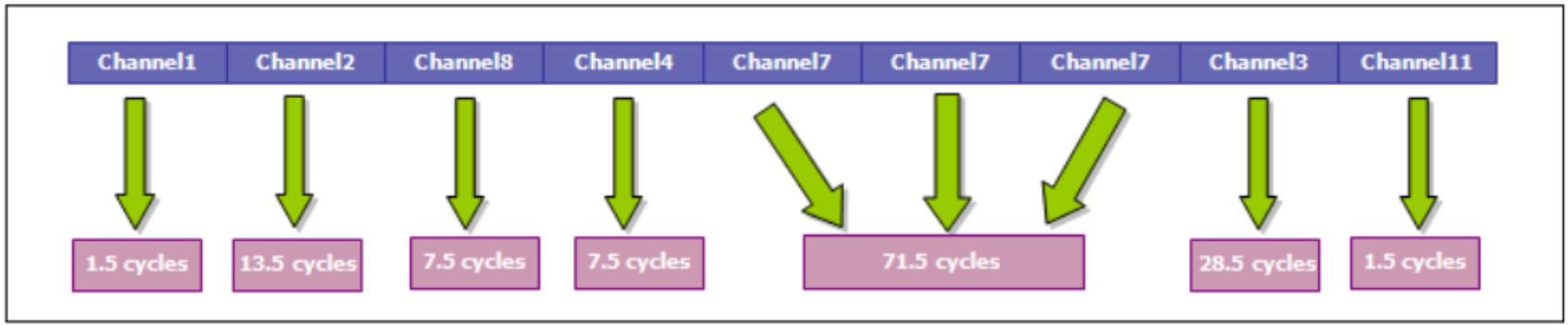


Figure 2. ADC sequencer converting 7 channels with different configured sampling times



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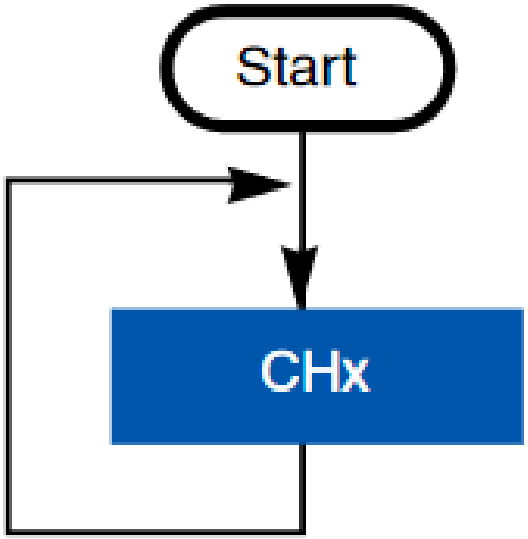
Single conversion continuous mode



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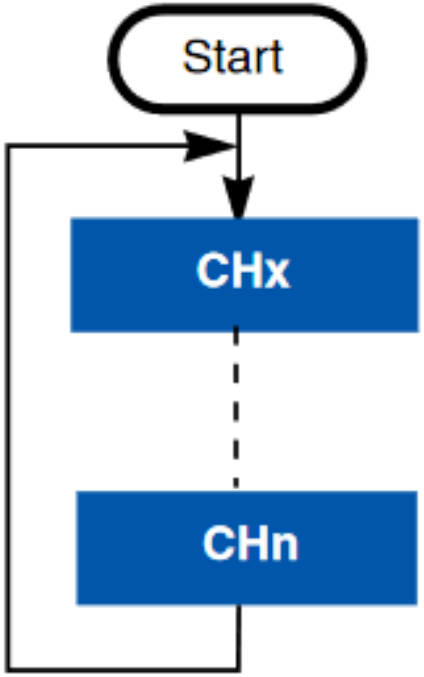
Multichannel conversion continuous mode



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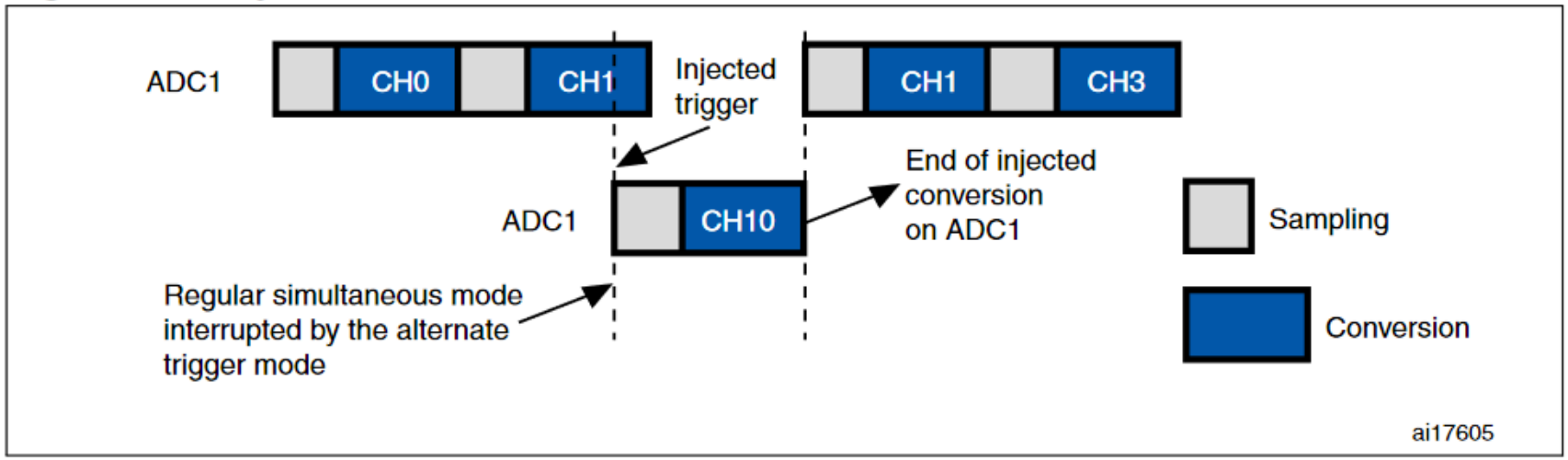
Injected conversion mode

Figure 6. Injected conversion mode



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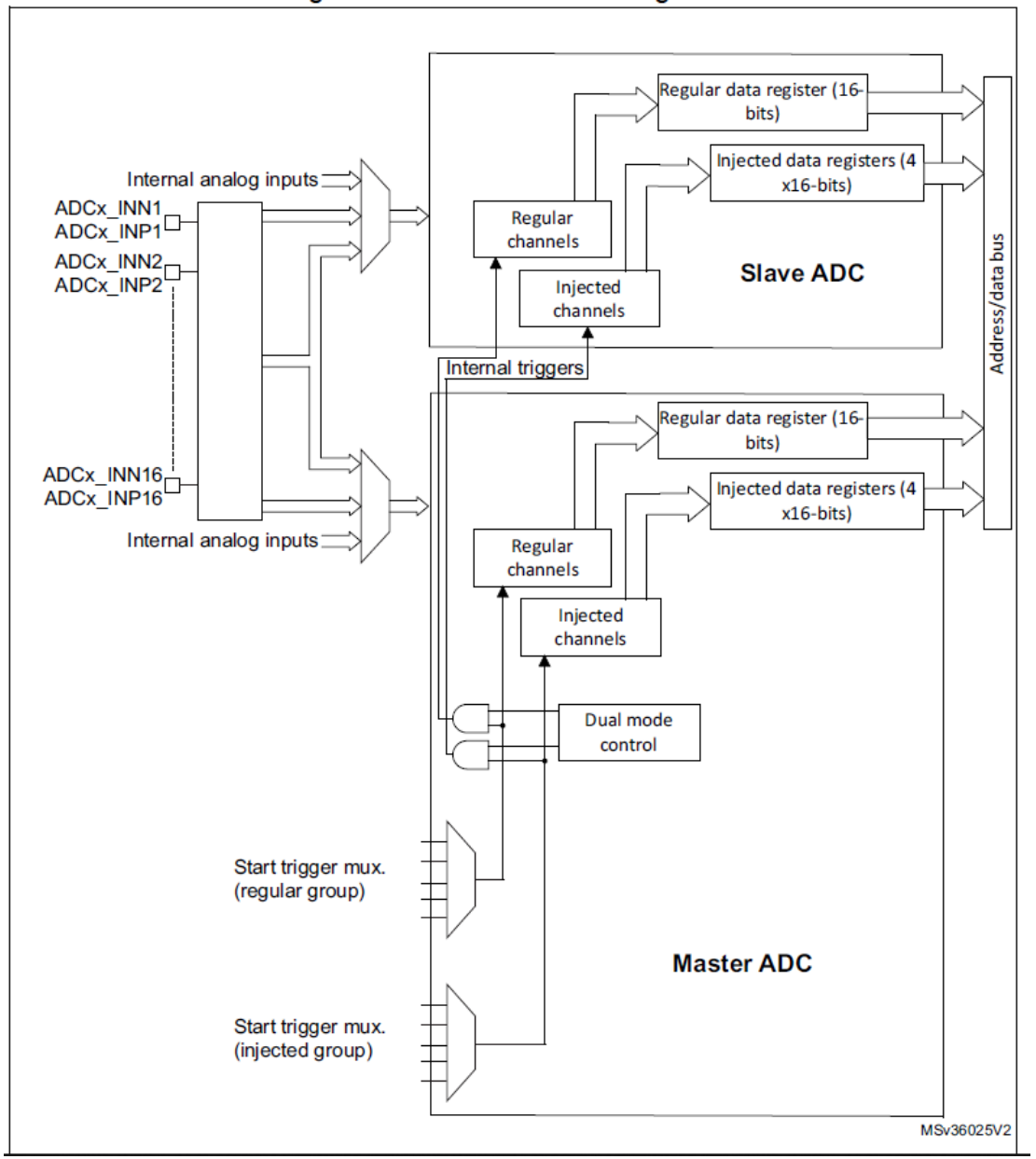
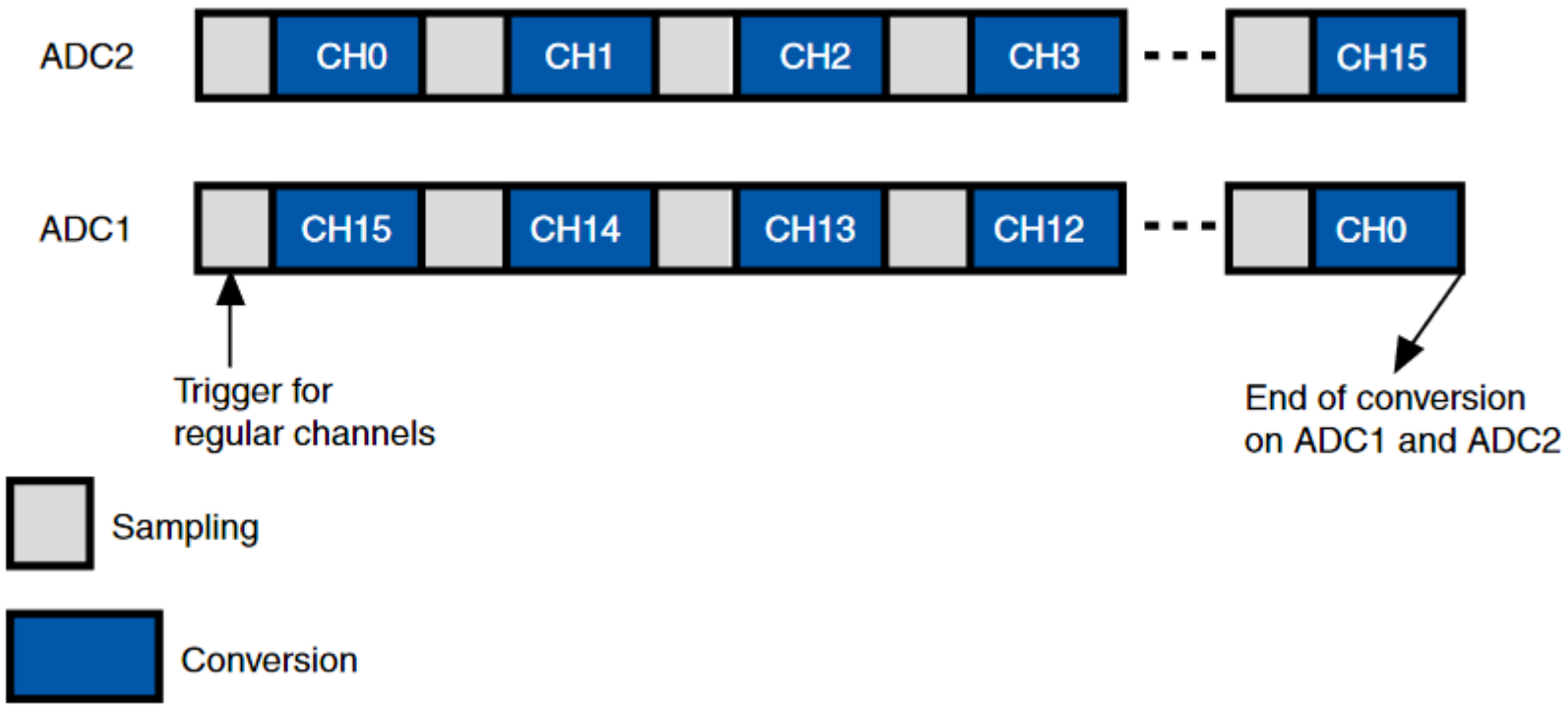
Dvojni ADC

Figure 137. Dual ADC block diagram(1)



Dual regular simultanoues mode



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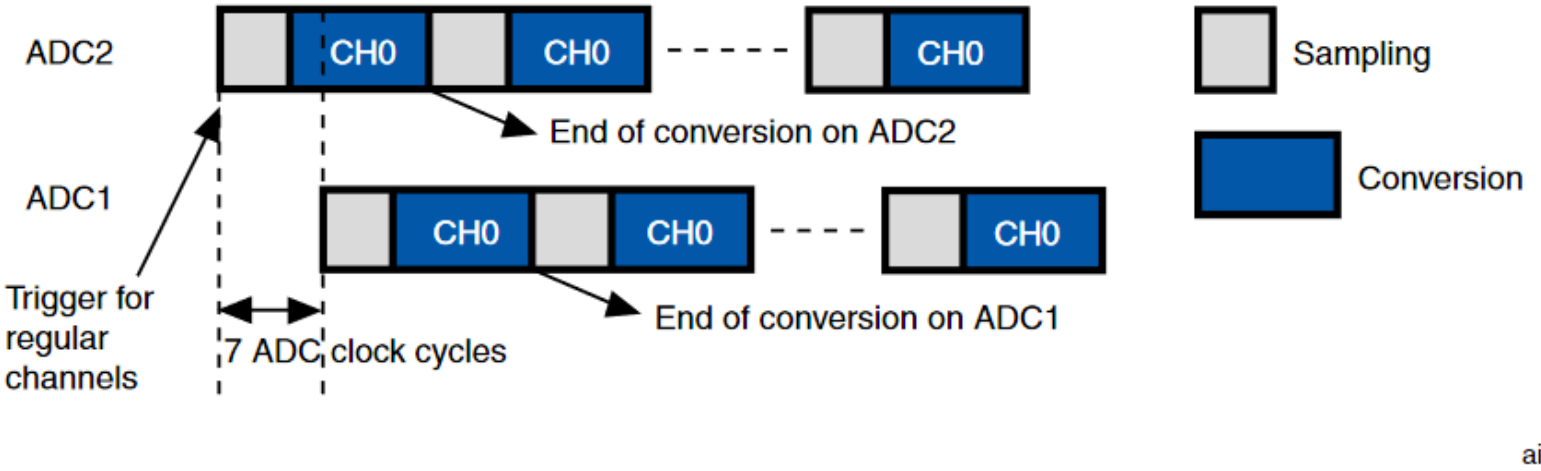
Dual interleaved mode



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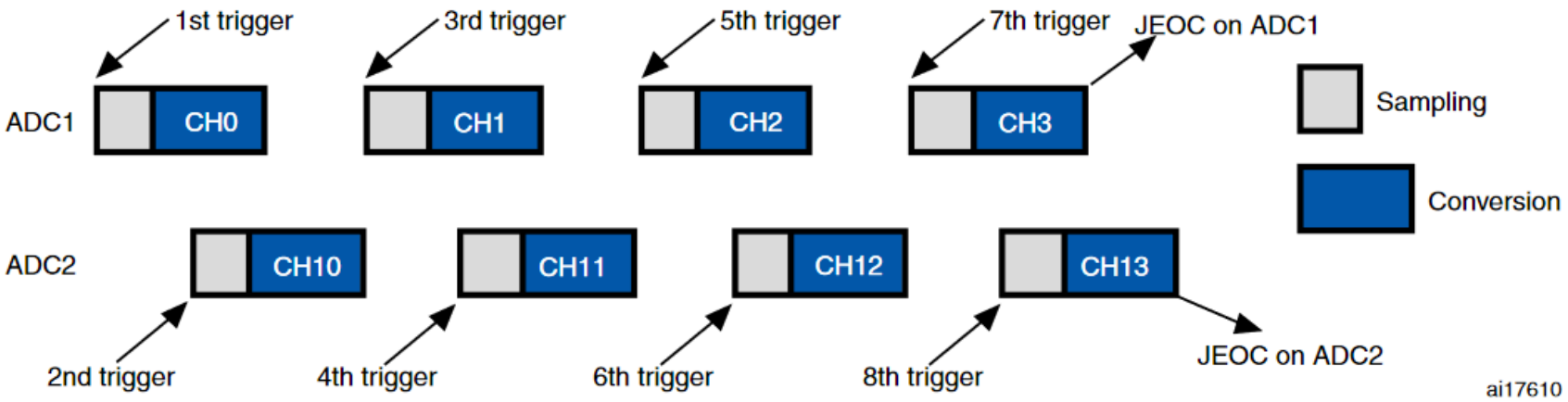
Dual alternate trigger mode



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