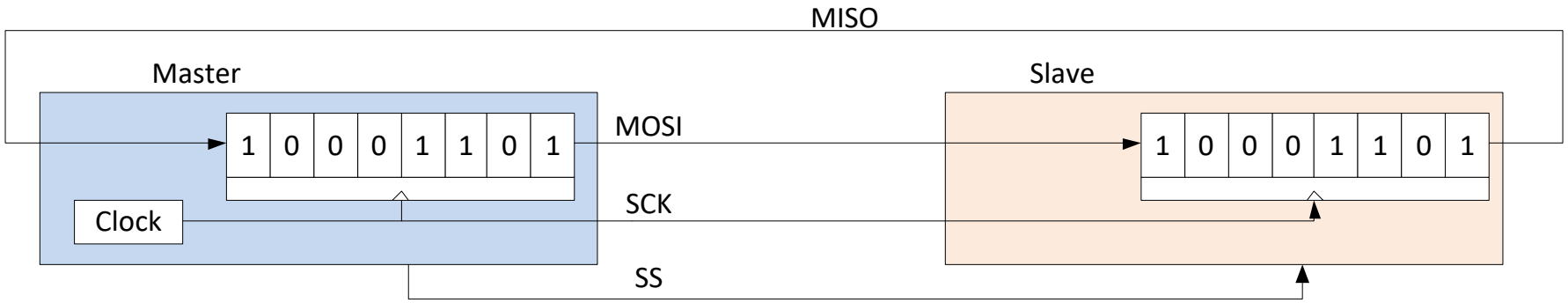
Osnove mikroprocesorske elektronike

Marko Jankovec

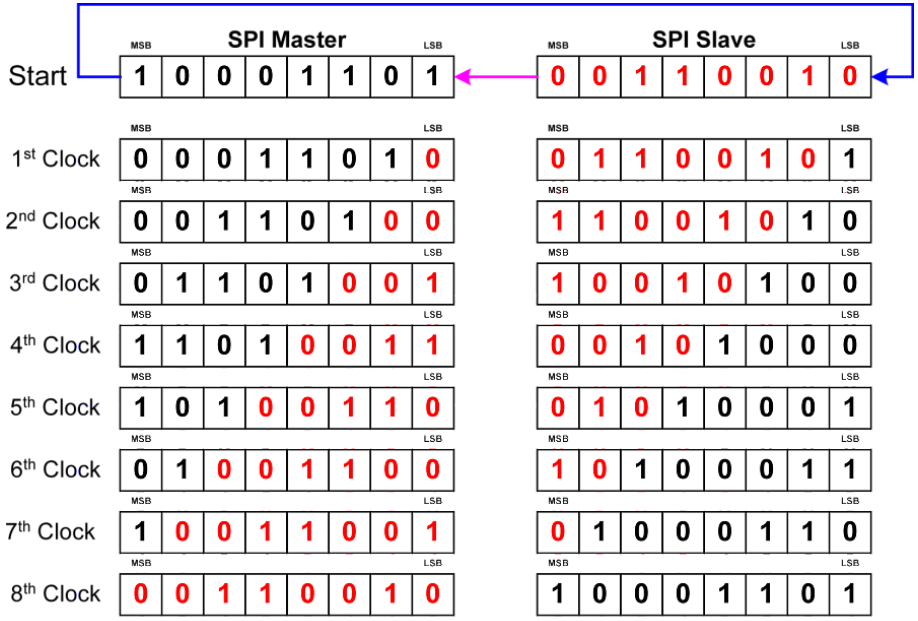
Sinhrona komunikacijska vodila

SPI

Vodilo SPI



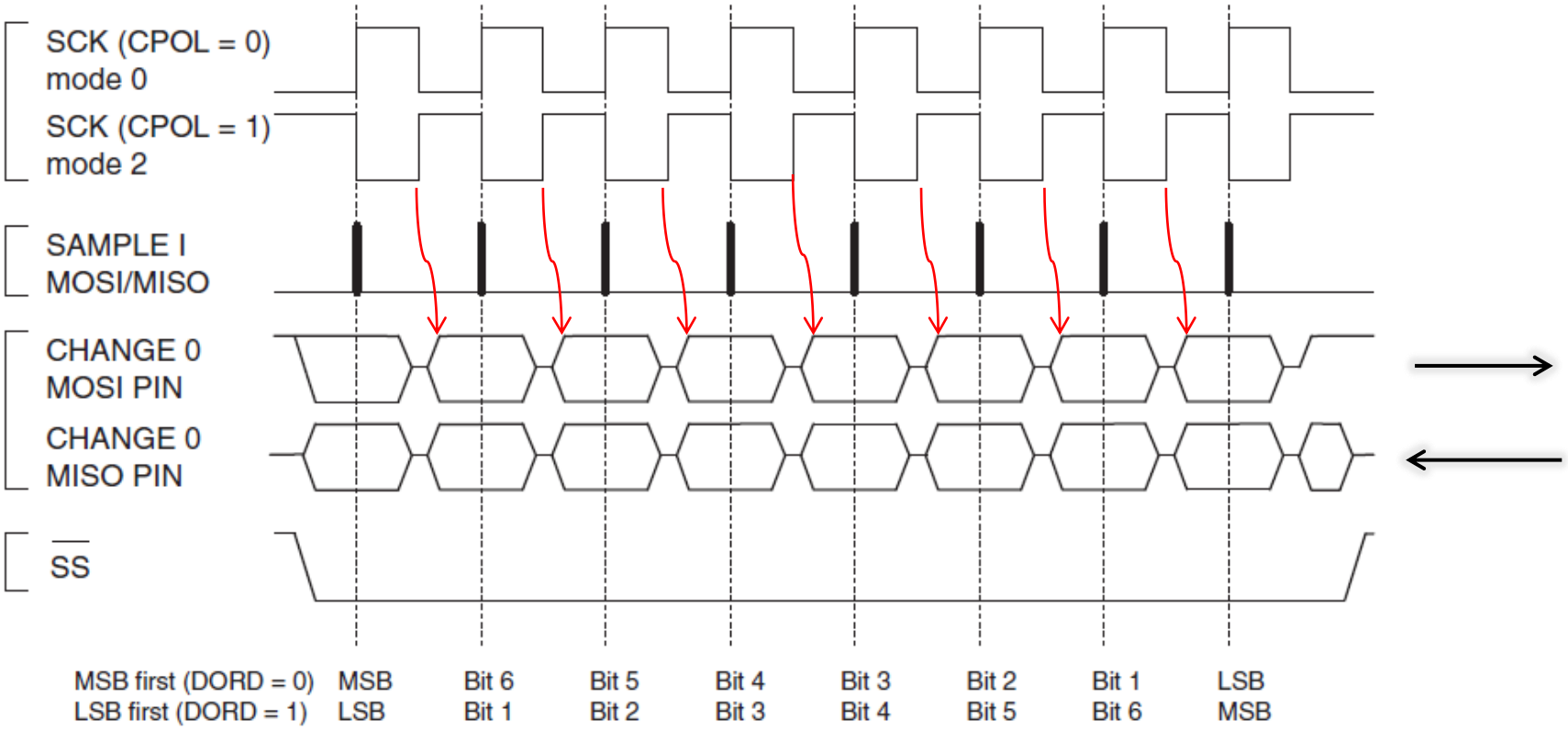
- Sinhrono vodilo
  - MOSI – Master Out Slave In
  - MISO – Master In Slave Out
  - SCK – System Clock
  - SS – Slave Select



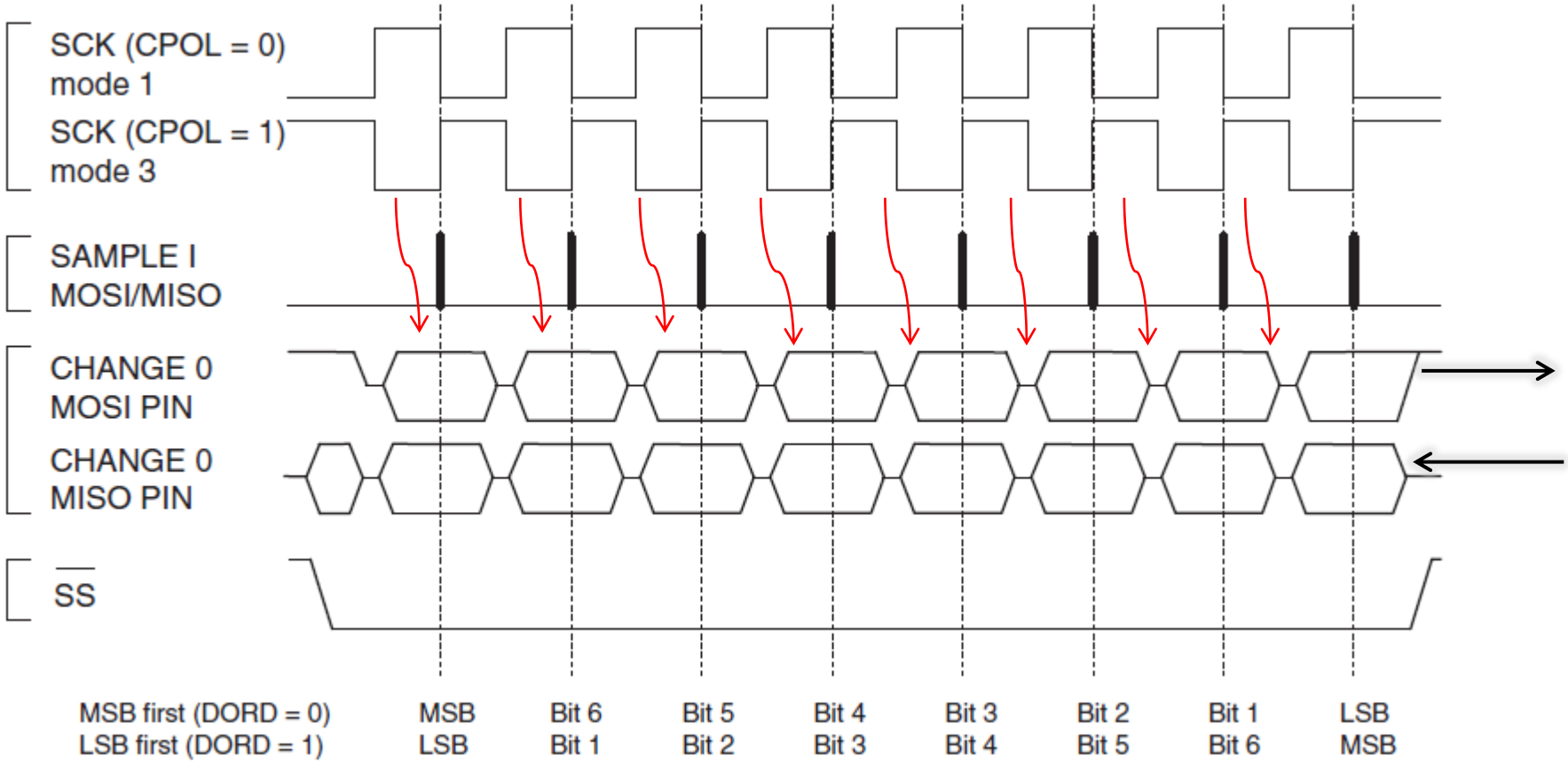
Možnost vodila SPI

- Clock polarity (CPOL)
- Clock phase (CPHA)
  - Mode 0 (CPOL = 0, CPHA = 0)
  - Mode 1 (CPOL = 0, CPHA = 1)
  - Mode 2 (CPOL = 1, CPHA = 0)
  - Mode 3 (CPOL = 1, CPHA = 1)
- Data order (DORD)

Možnost vodila SPI (CPHA = 0)

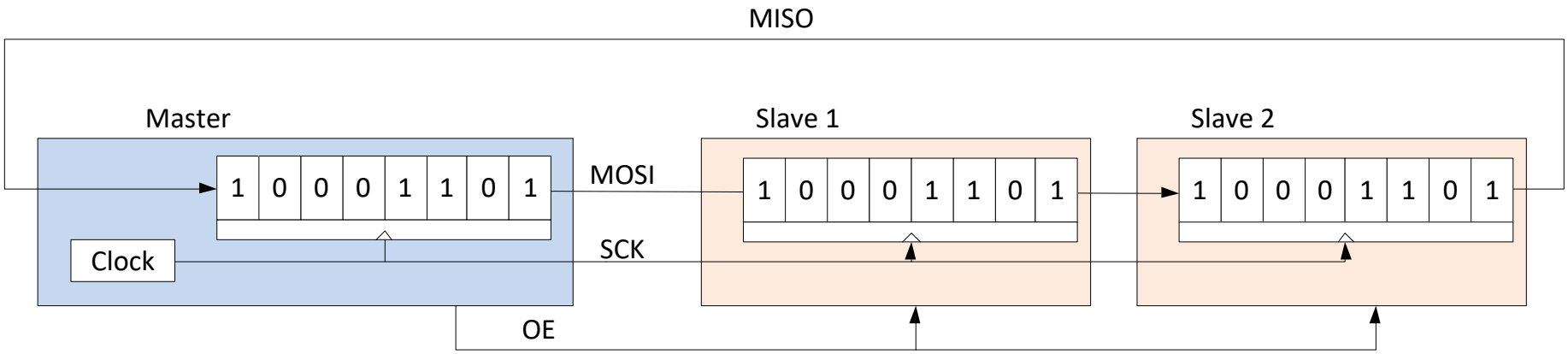


Možnost vodila SPI (CPHA = 1)



Več naprav na vodilu SPI

- Zaporedna vezava - Daisy chain



Več naprav na vodilu SPI

- Vzporedna vezava