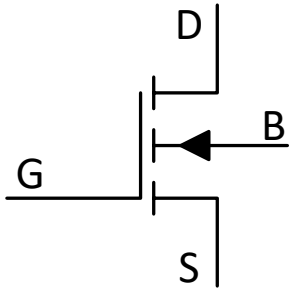
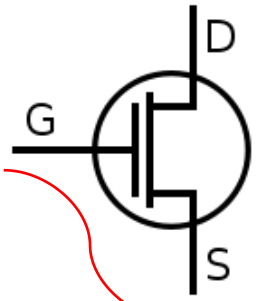
Osnove mikroprocesorske elektronike

Marko Jankovec

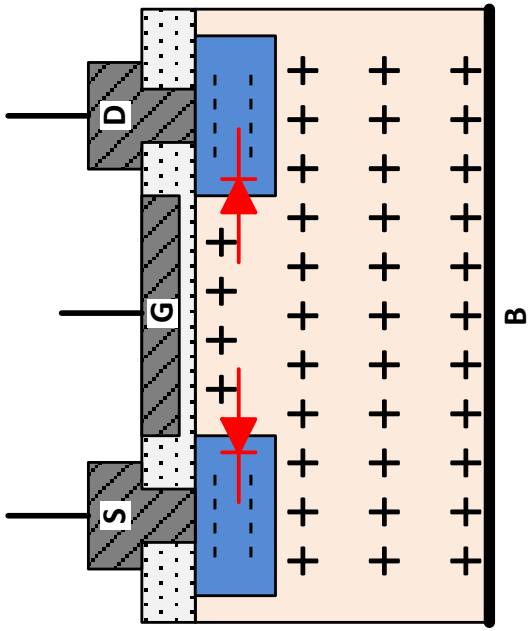
MOS transistor – osnovni gradnik mikroprocesorjev

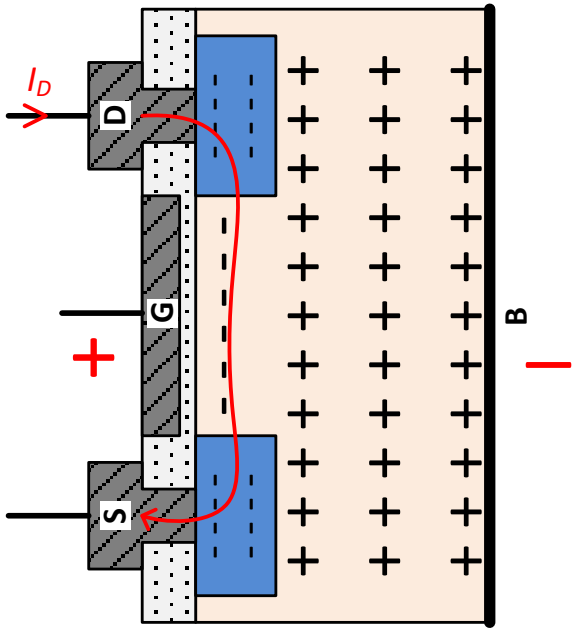
Osnovni element – nMOS tranzistor



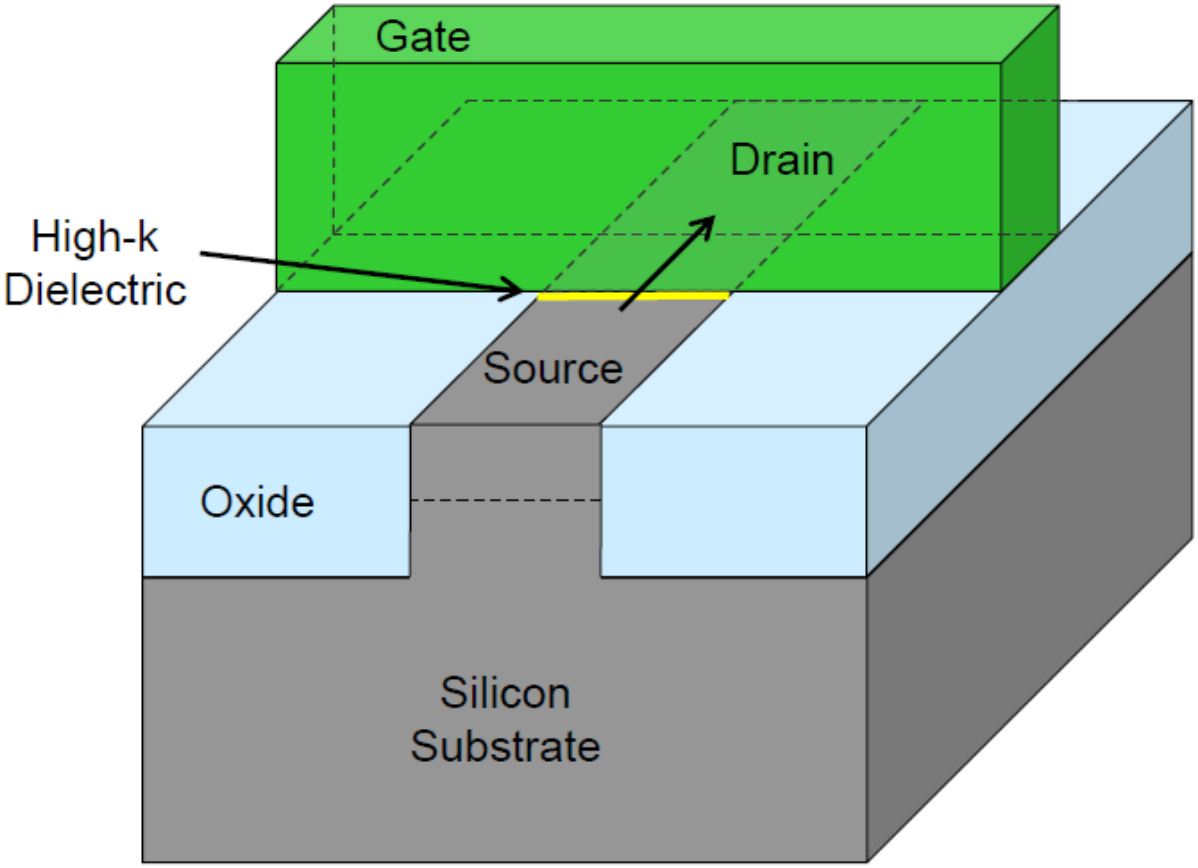


$U_{gs} > 0$



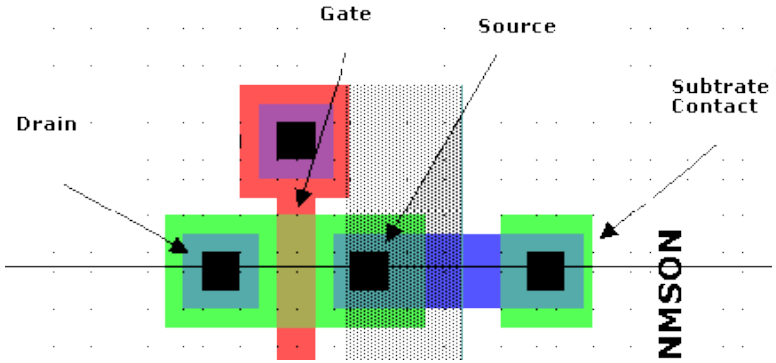


MOS tranzistor

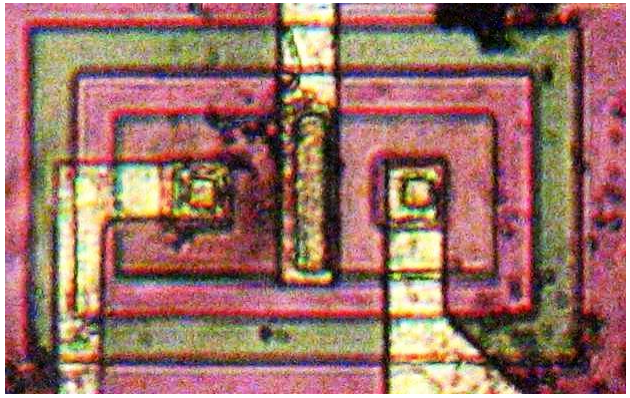


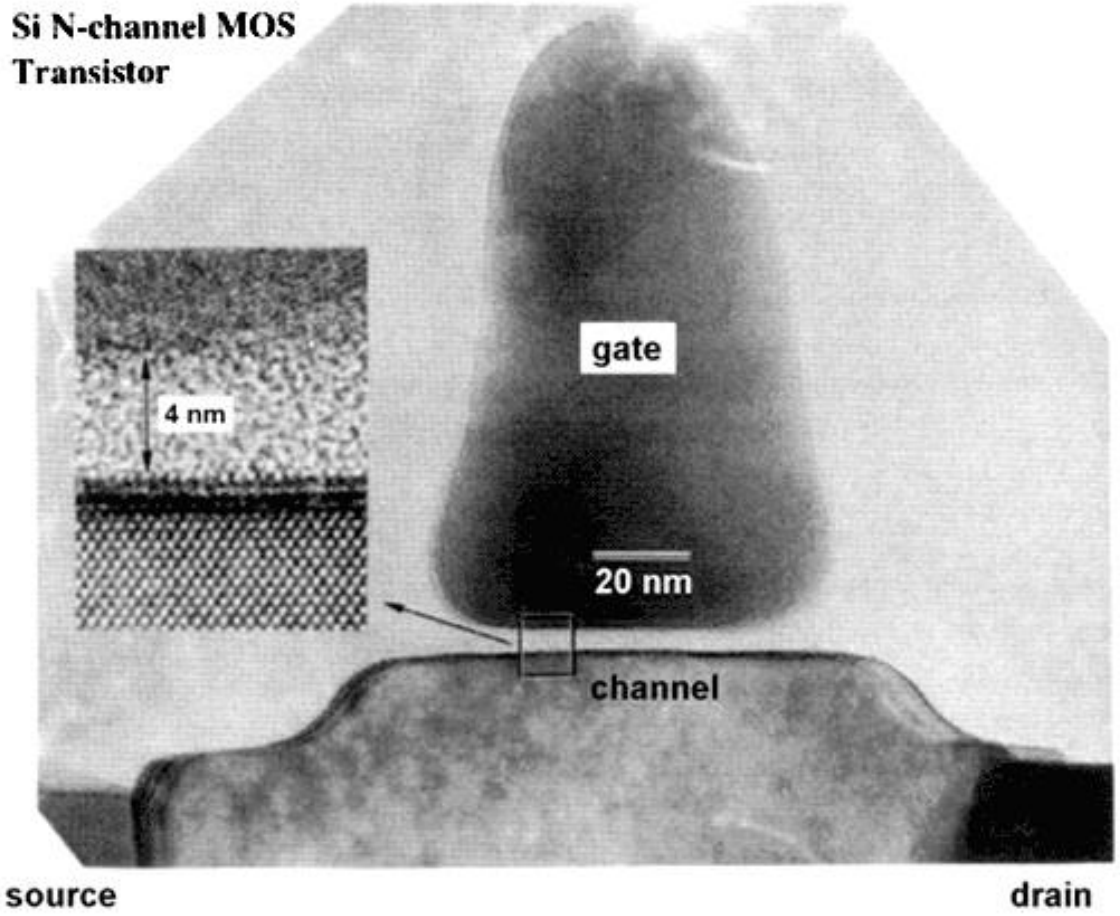
MOS tranzistor

http://www.youtube.com/watch?v=v7J_snw0Eng



http://www.ami.ac.uk

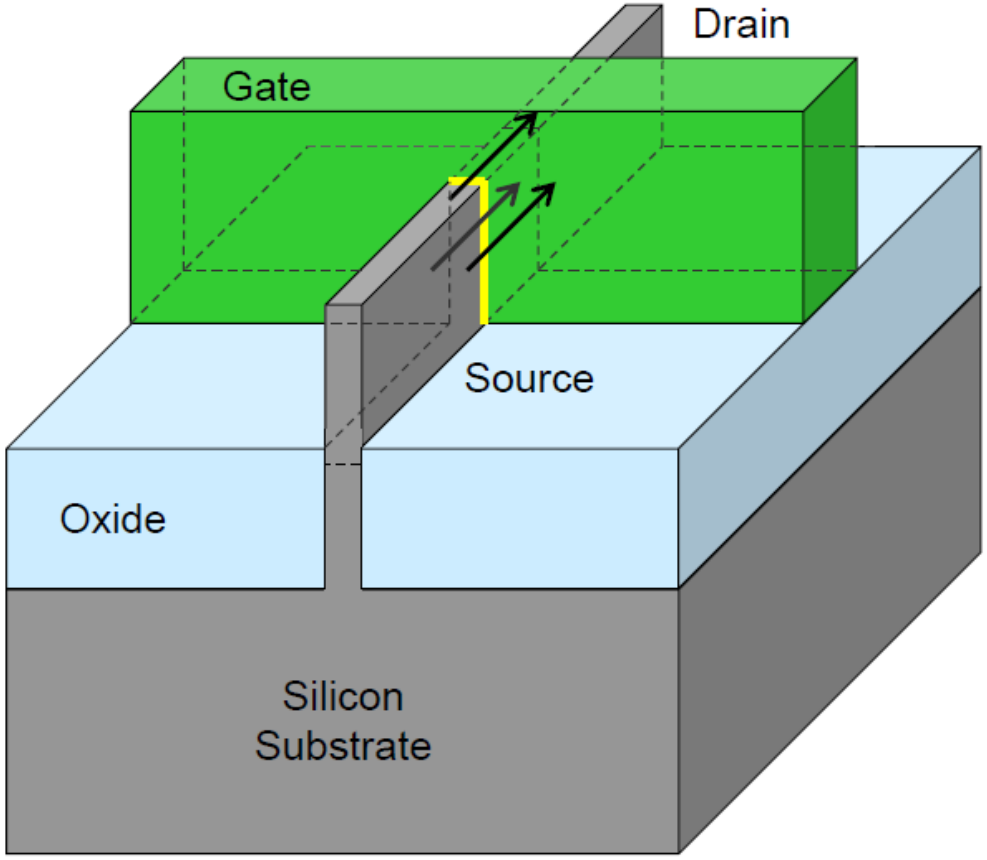




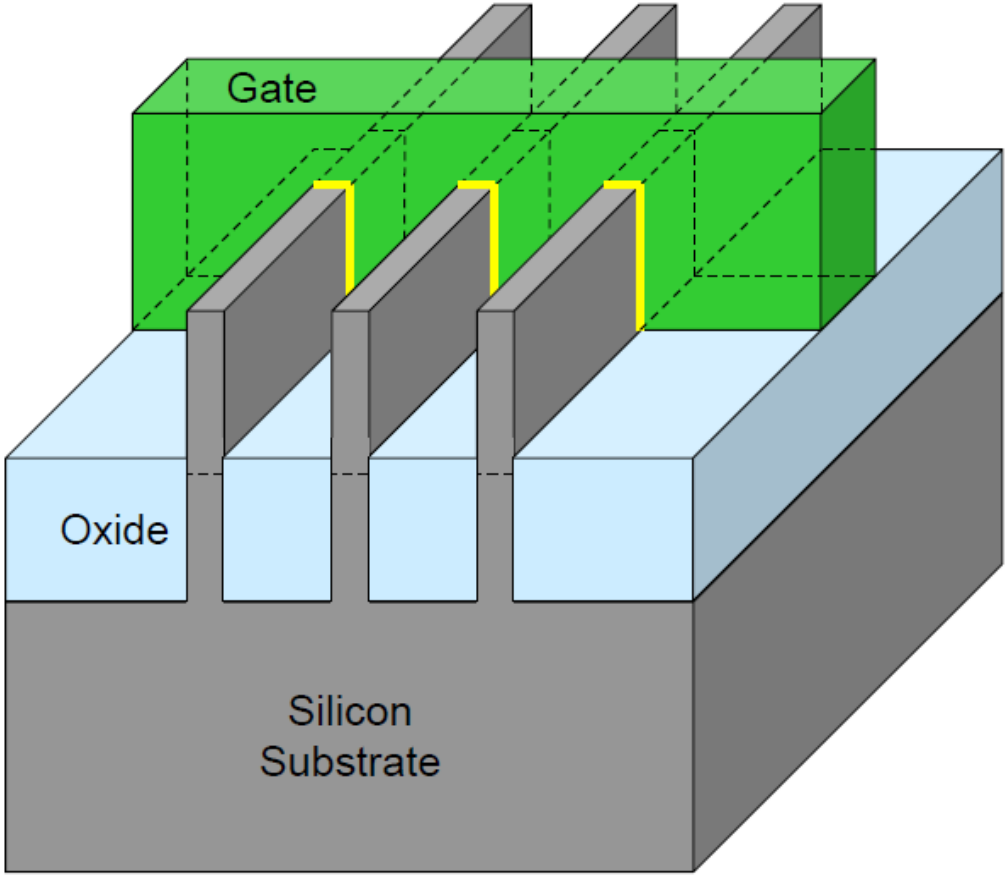
http://uvicrec.blogspot.com/2011_09_01_archive.html

www.chem.wisc.edu

3D Tri-Gate MOS tranzistor

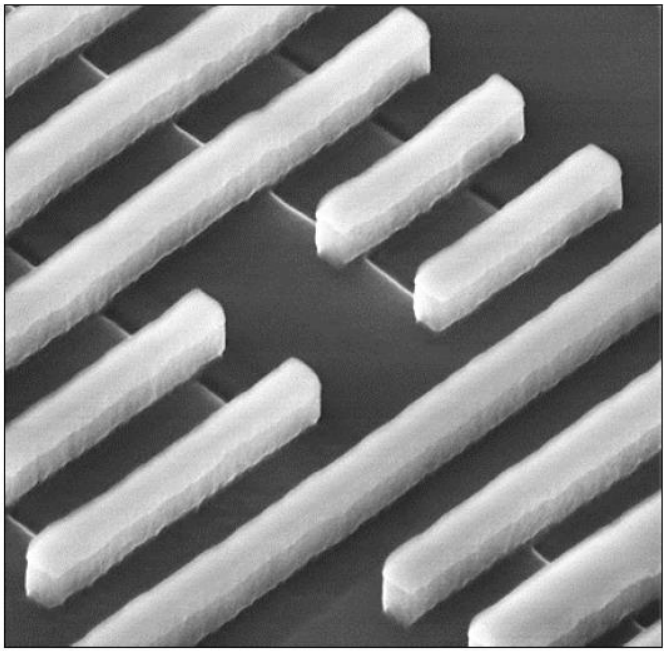


3D Tri-Gate MOS tranzistor

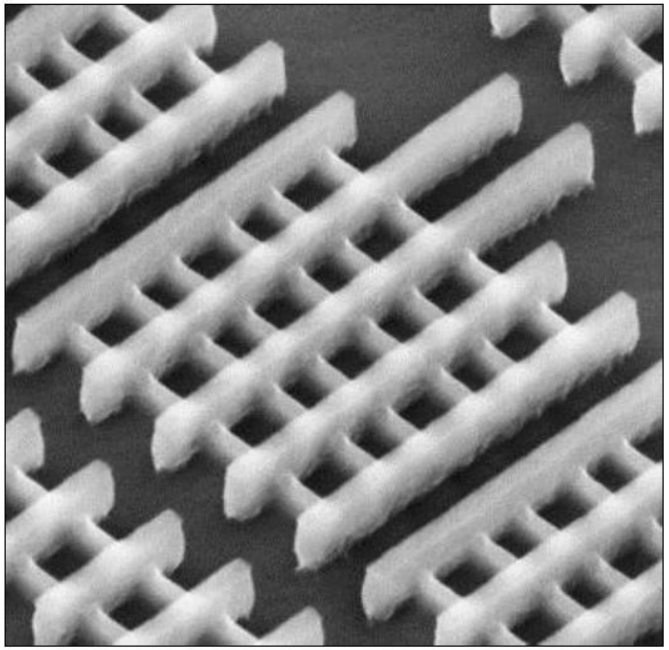


Primerjava

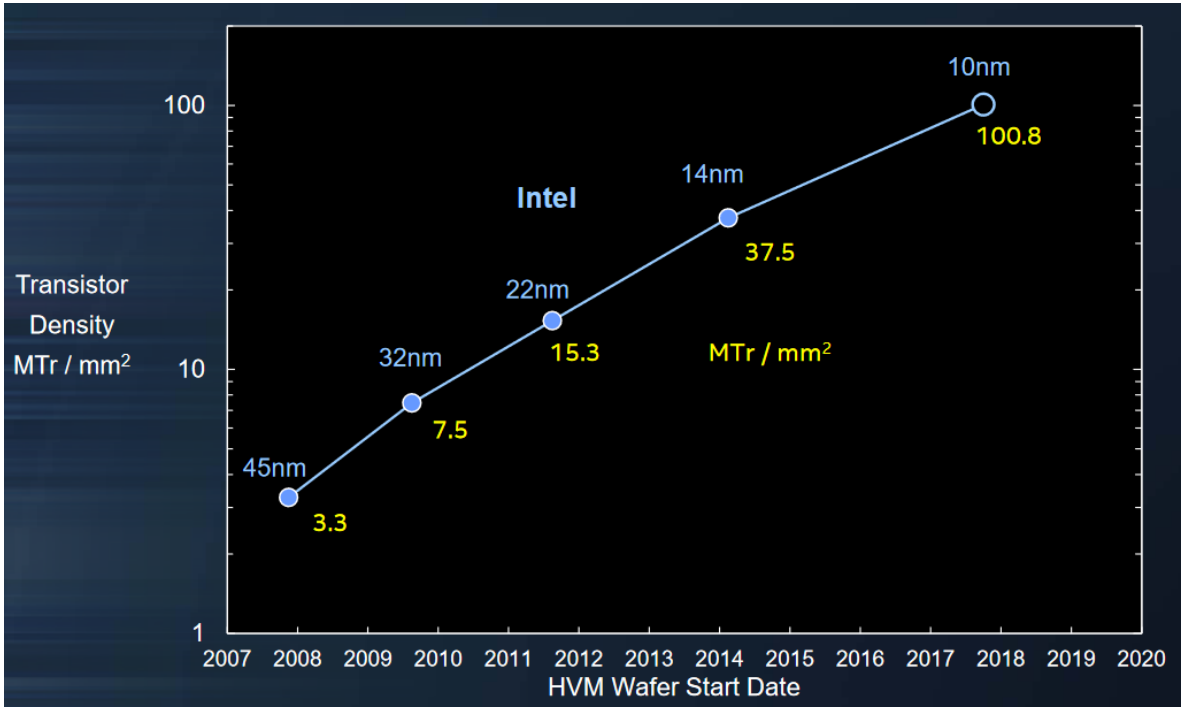
32 nm planarni MOS tranzistor

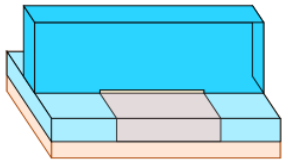


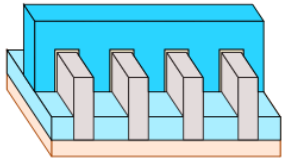
22 nm Tri-Gate MOS tranzistor

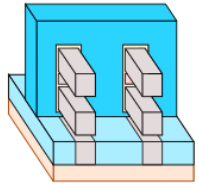


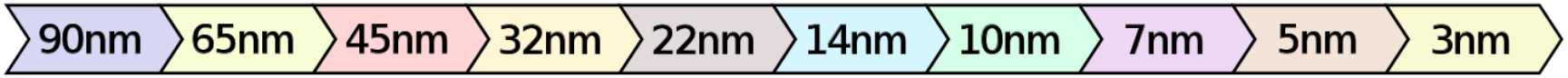
Moorov zakon za gostoto tranzistorjev



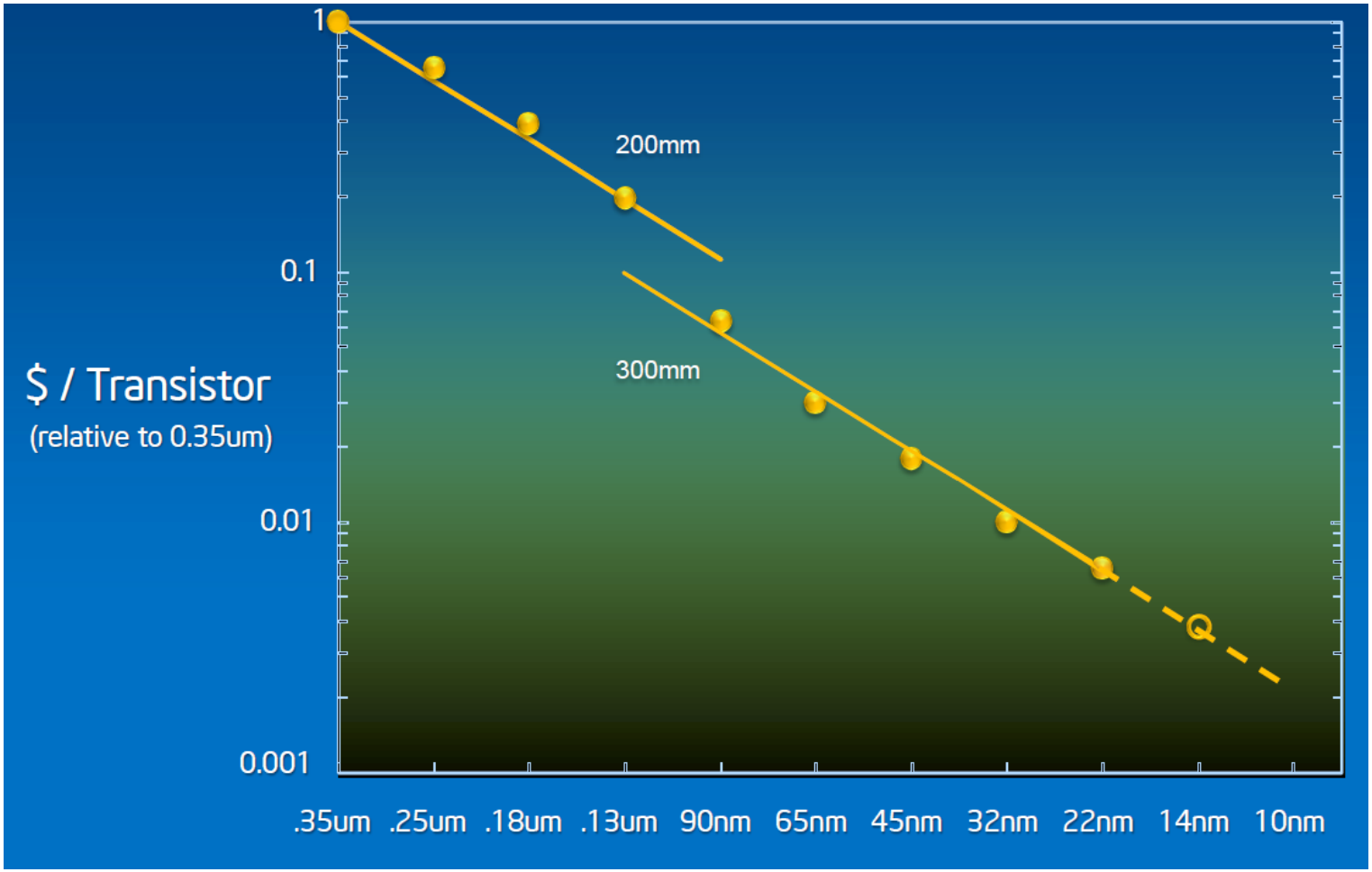








Moorov zakon za ceno tranzistorjev



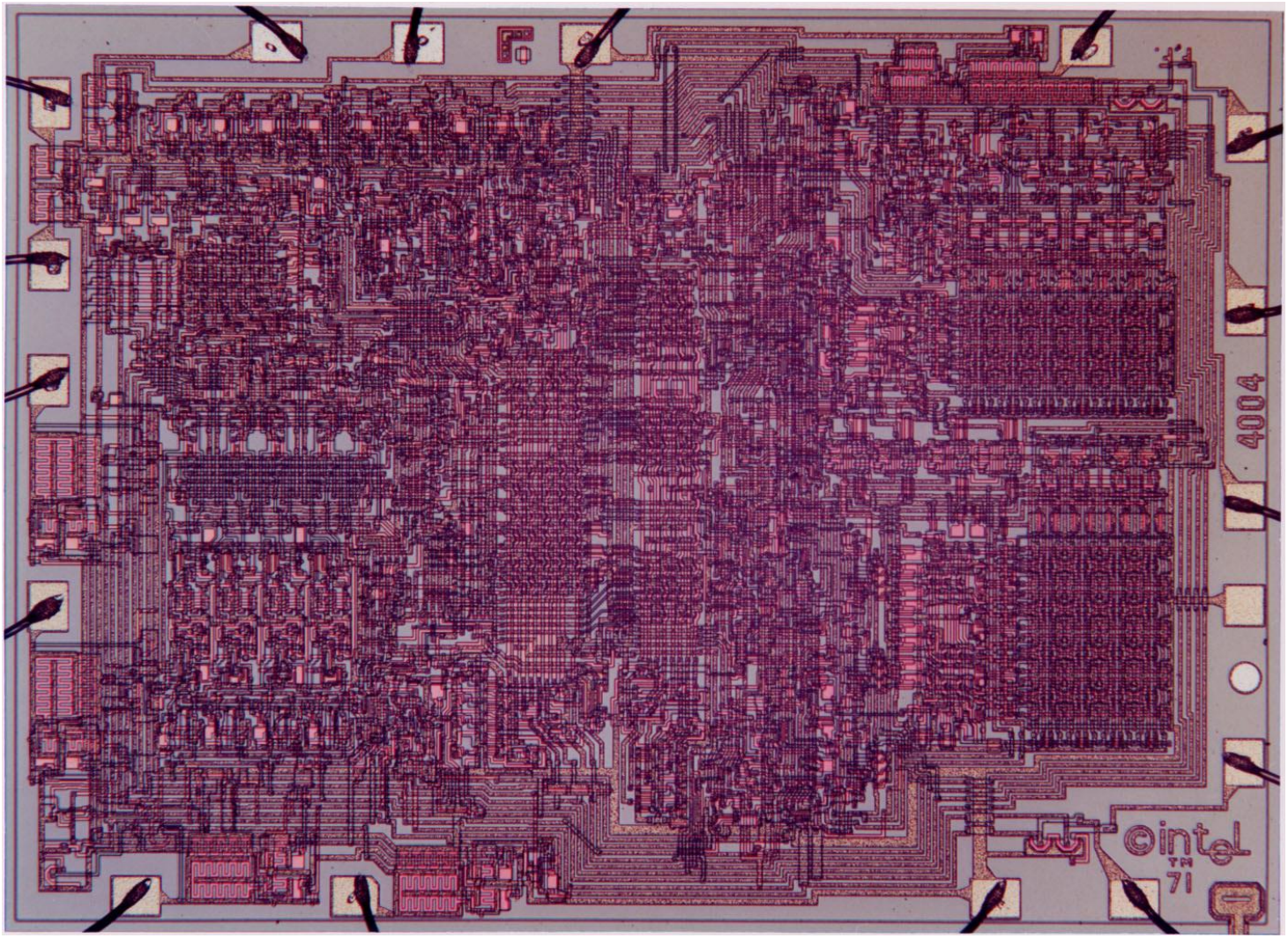
http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Announcement_Presentation.pdf

Osnove mikroprocesorske elektronike

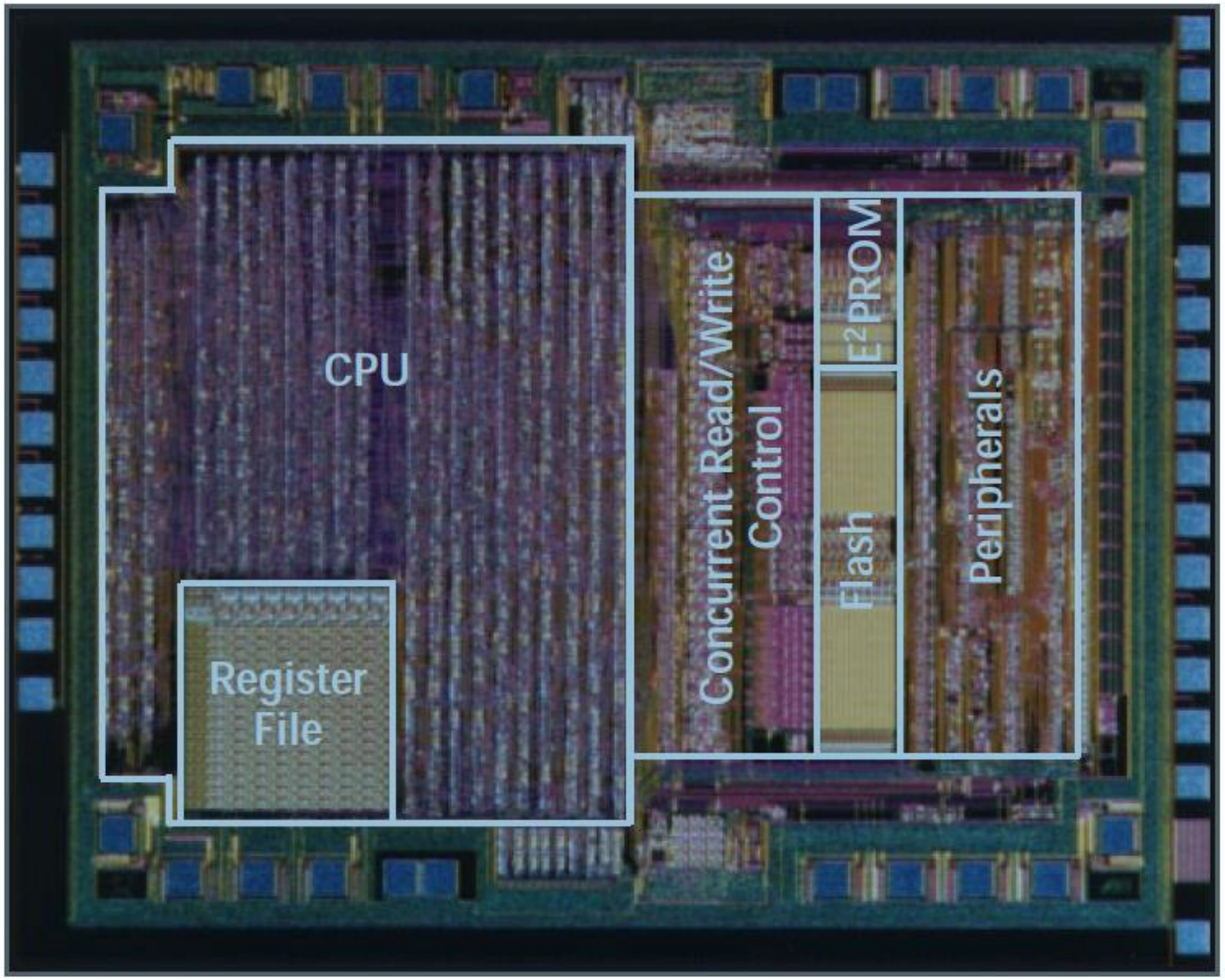
Marko Jankovec

Pomnilniki v mikrokrmilniku

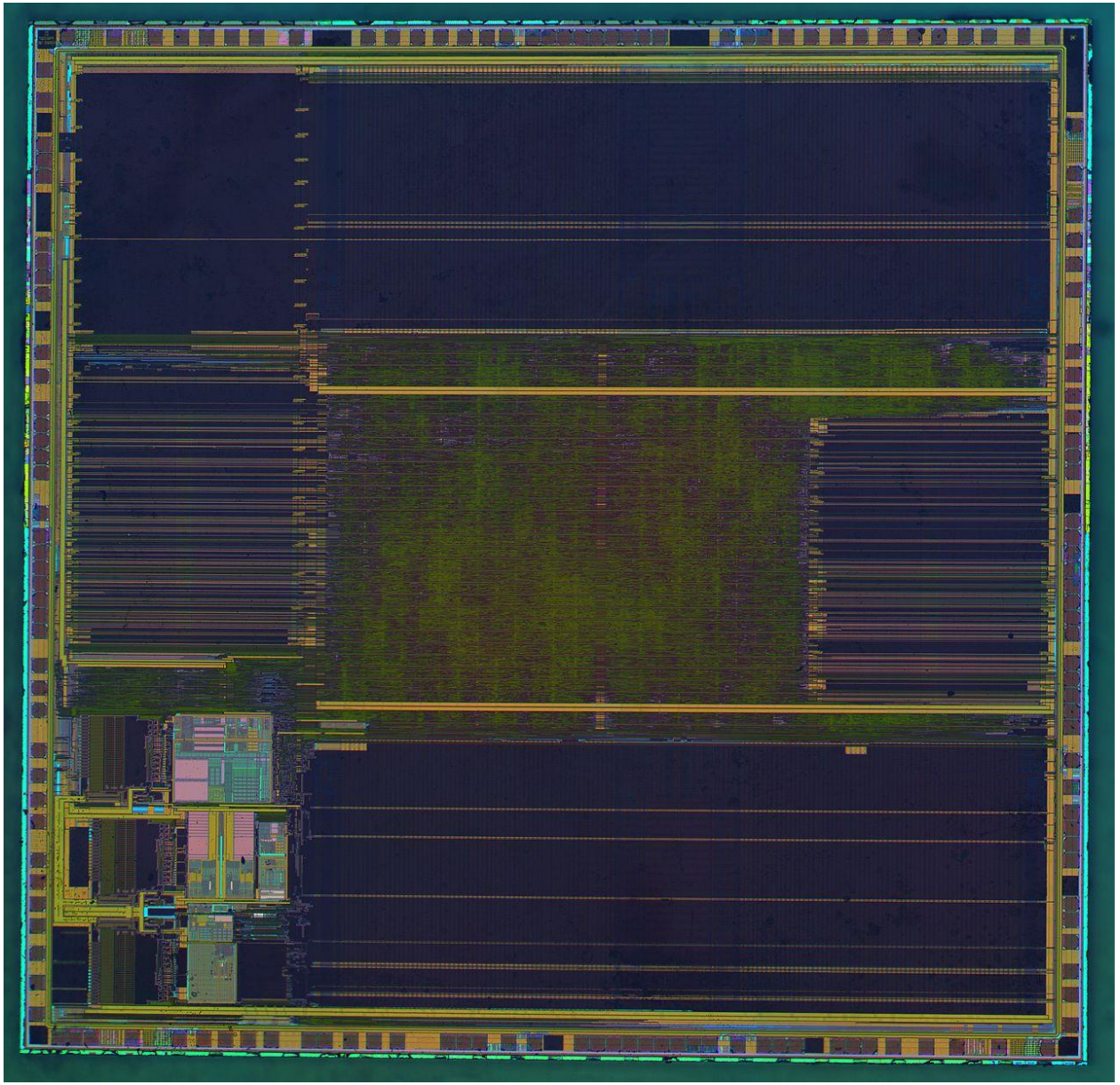
Intel 4004



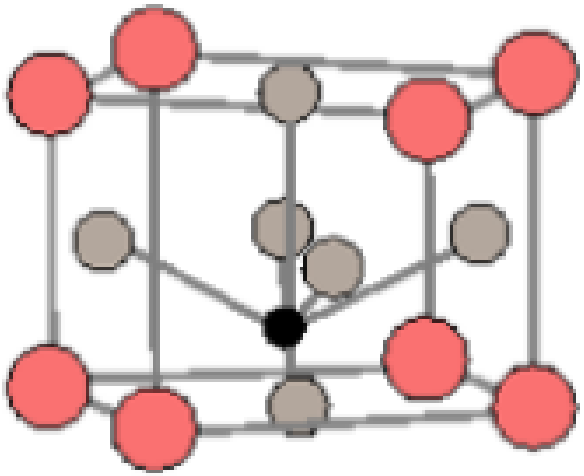
AT90S1200

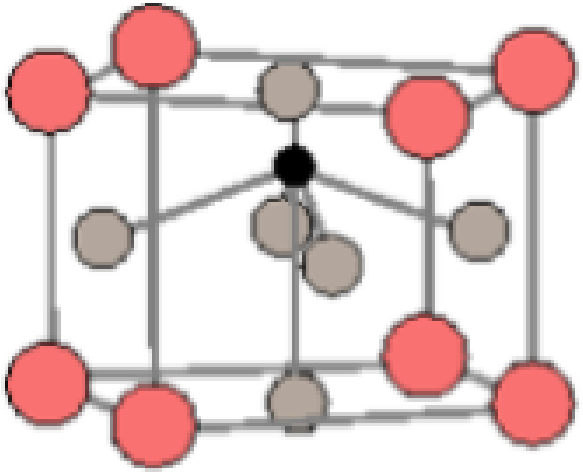

CPU
Register File
Concurrent Read/Write Control
Flash
E2PROM
Peripherals

STM32F100

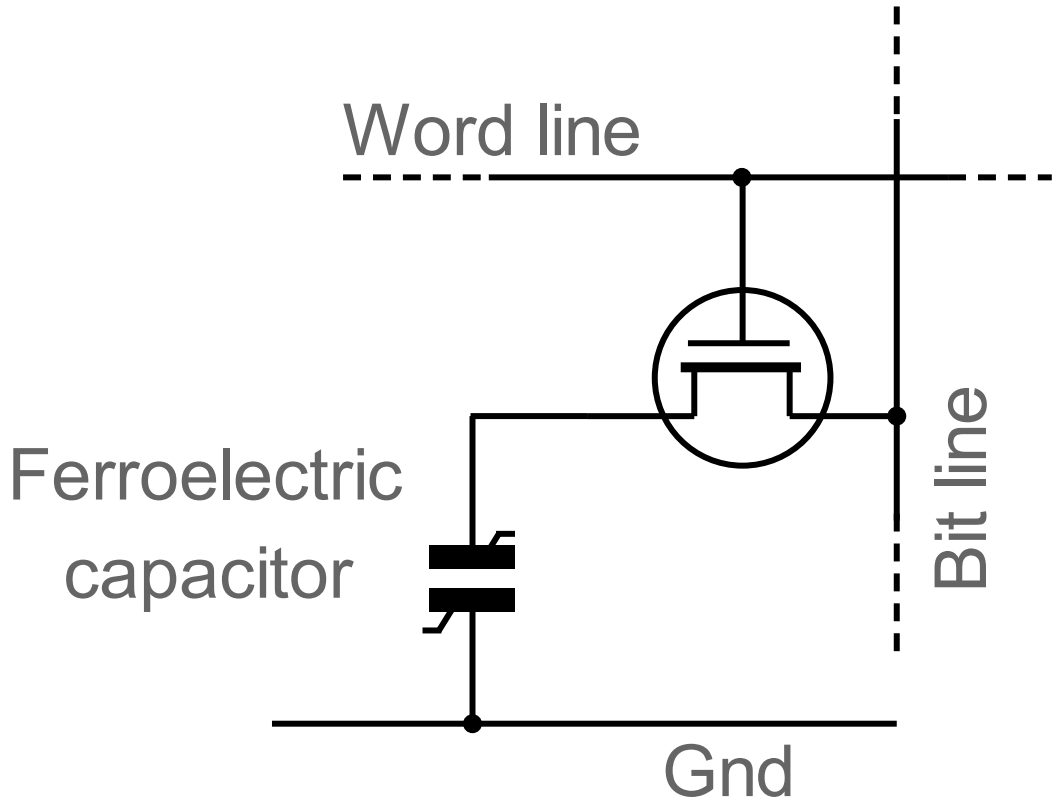


FRAM – Feroelektrični materiali





FRAM – variabilni kondenzator



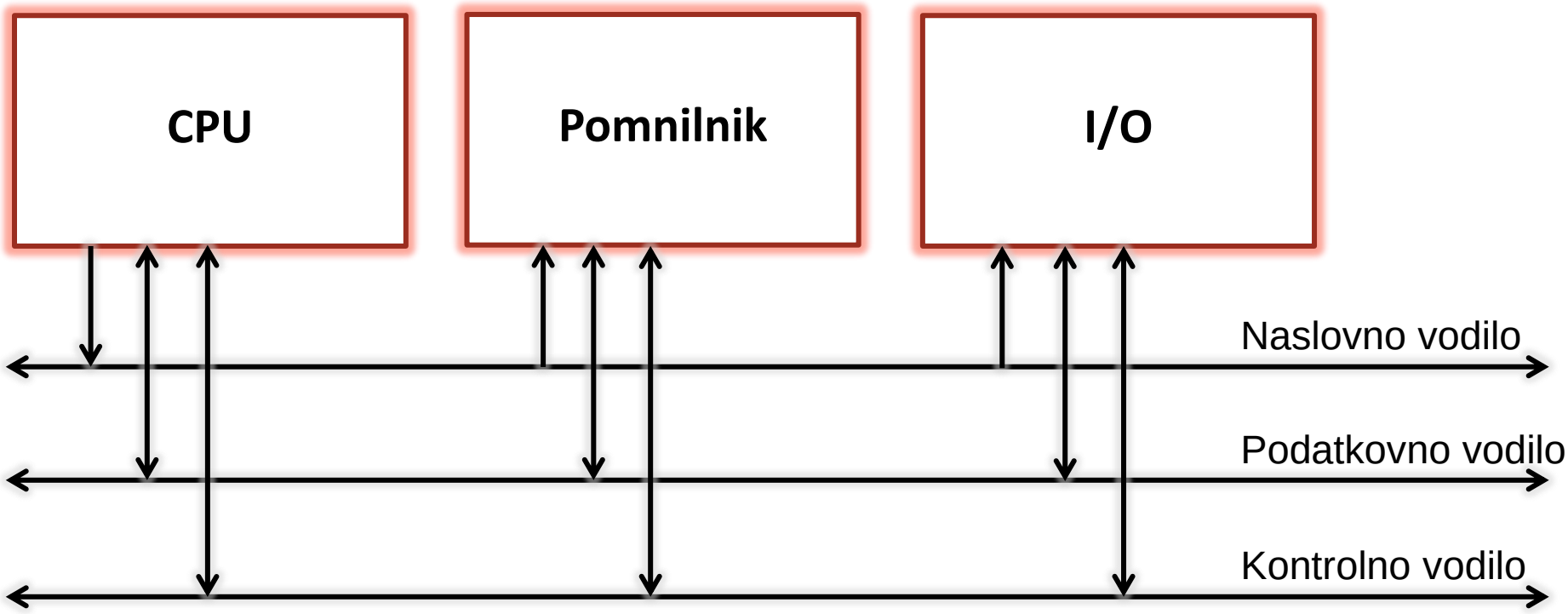
Primerjava

	FRAM	SRAM	Flash	EEPROM
Non-Volatile Retains data without power	Yes	No	Yes	Yes
Avg Active Power (µA/MHz)	100	< 60	230	50,000+
Write Power for 12KB/s	9 µA	N/A	2200 µA	N/A
Write Speeds (13KB)	10 ms	< 10 ms	1 sec	2 secs
Write Endurance	10^{15}	Unlimited	10^5	10^5
Bit-wise Programmable	Yes	Yes	No	No
Data Erase Required	No	No	Segment	Page
Unified: Code and Data	Yes	No	No	No
Read Speeds	8 MHz	up to 25MHz (on some devices)		N/A

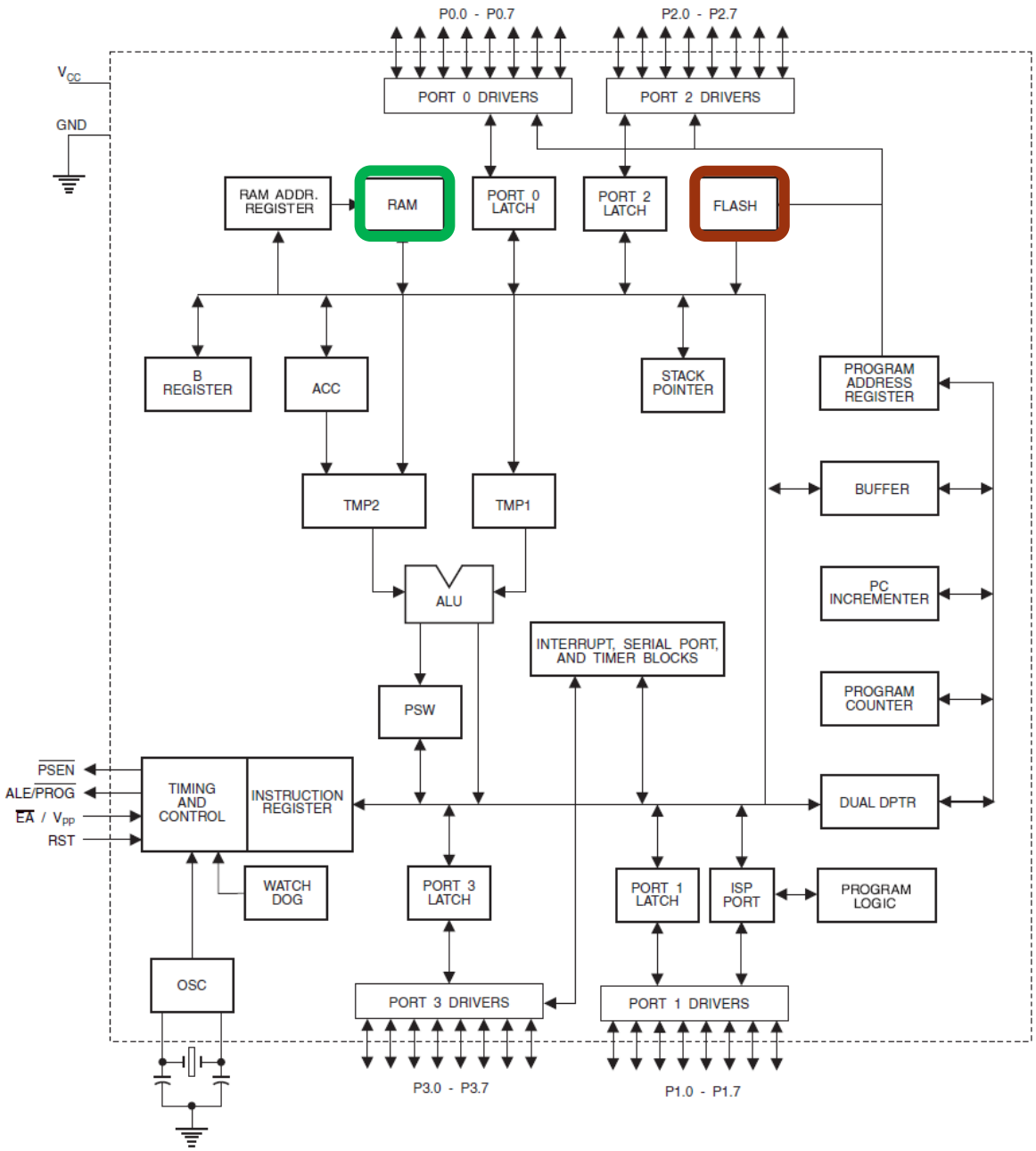
- Similar to SRAM, FRAM has virtually unlimited write endurance with no signs of degradation. FRAM does not require a pre-erase in which every write to FRAM is non-volatile. However, there are some minor trade-offs in using FRAM instead of RAM that may apply to a subset of use cases. One of the differences on the MSP430 platform is the FRAM access speed, which is limited to 8 MHz, whereas, SRAM can be accessed at the maximum device operating frequency. Wait-states are required if the CPU accesses the FRAM at speeds faster than 8 MHz. Another trade-off is that FRAM access results in a somewhat higher power consumption compared with SRAM.

- Variables are allocated in SRAM by the default linker command files. FRAM-based MSP430 devices would typically have 2KB of SRAM. For the exact specification, see the device-specific data sheet. If the variable size is too large to fit in SRAM, the linker command file can be modified or C-language `#pragma` directives can be used to allocate specific variables or structures in FRAM memory. Section 3.4 showcases how you would modify the linker command file to move variables from SRAM to FRAM. Aside from SRAM memory constraint, another reason you would use FRAM for variables is to decrease start-up time as outlined in Section 4.

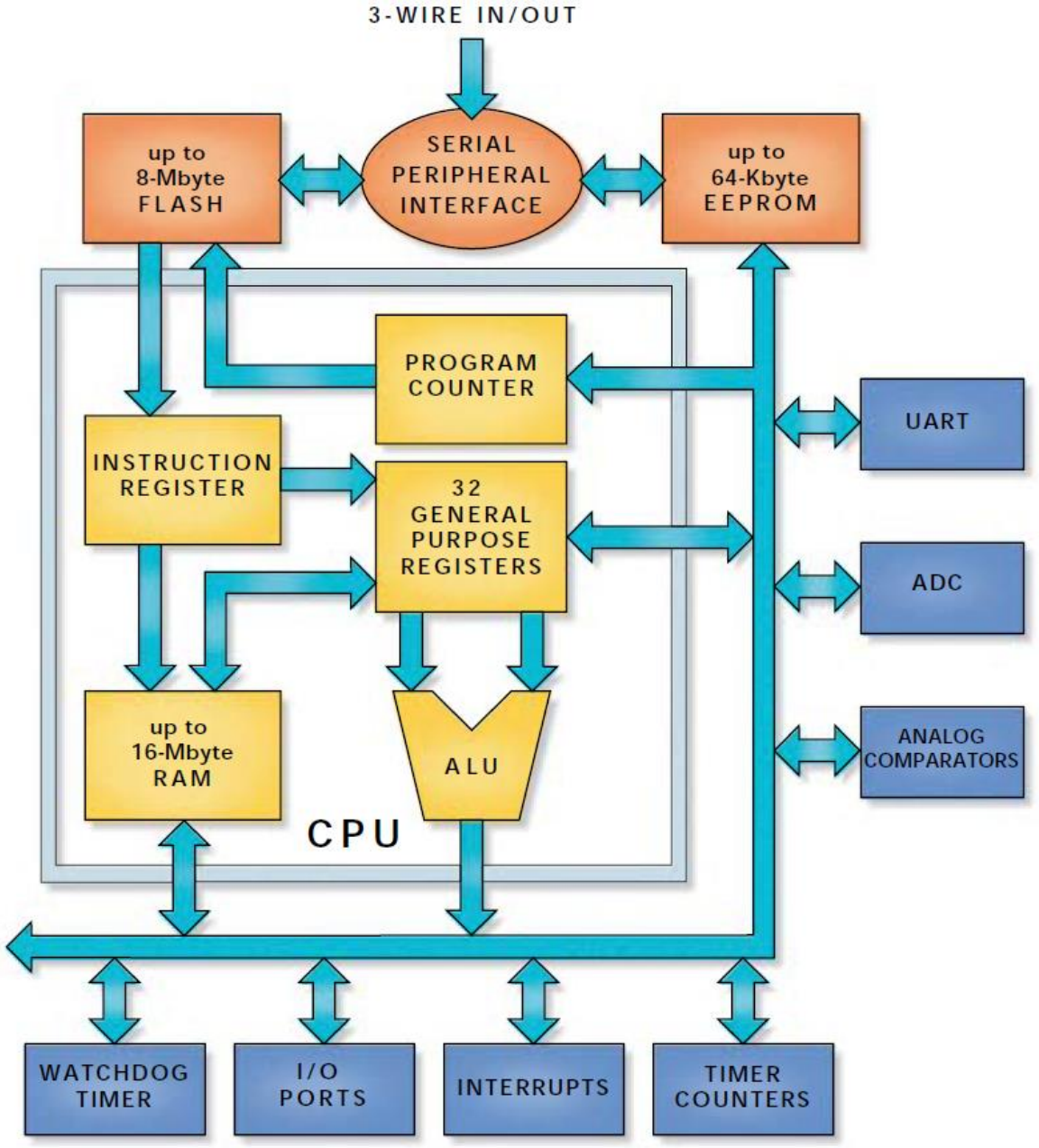
Mikroračunalnik (MCU)



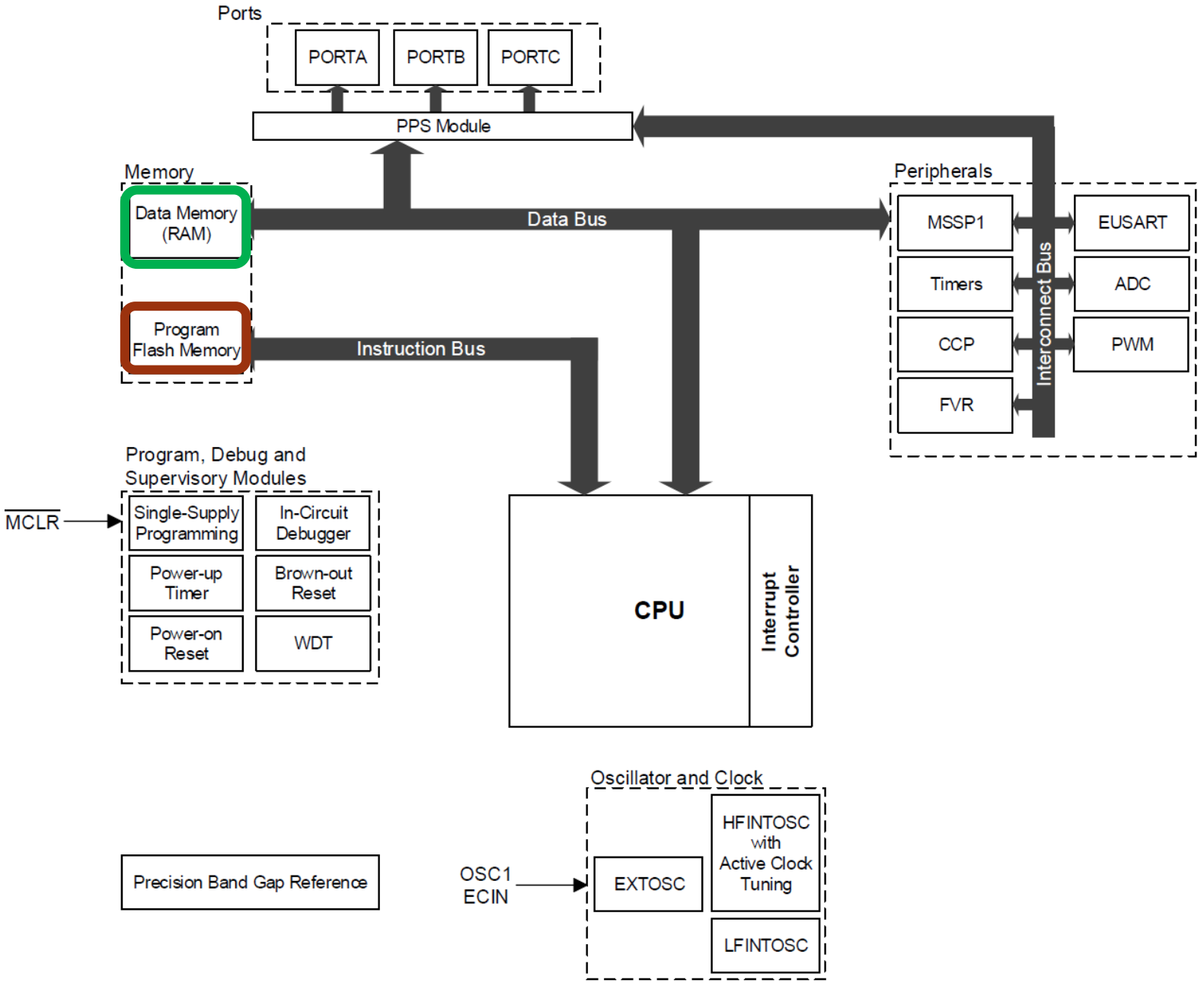
8051


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
ALE/PROG
EA / V_{pp}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

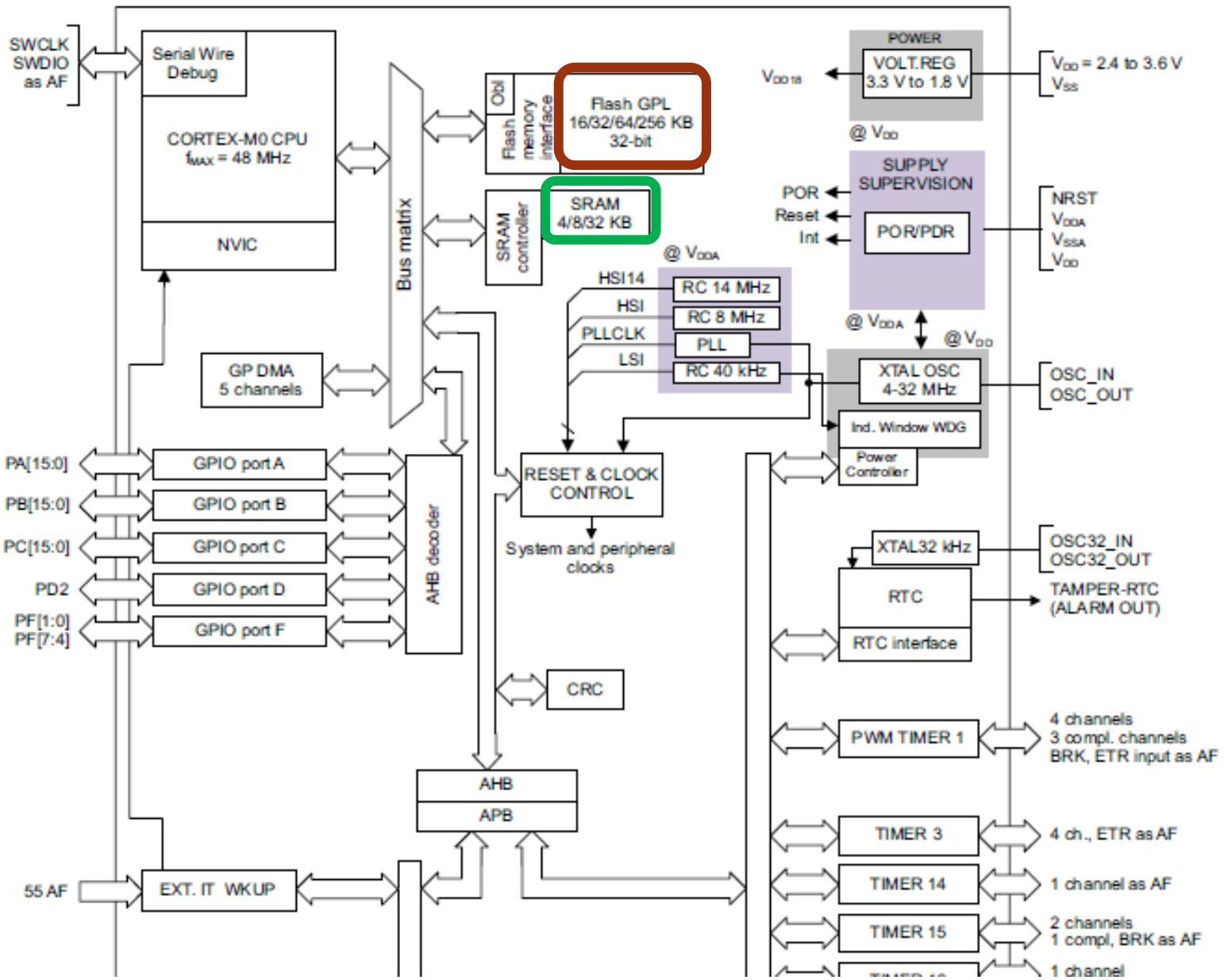
AVR


3-WIRE IN/OUT
up to 8-Mbyte FLASH
SERIAL PERIPHERAL INTERFACE
up to 64-Kbyte EEPROM
PROGRAM COUNTER
INSTRUCTION REGISTER
32 GENERAL PURPOSE REGISTERS
UART
ADC
ANALOG COMPARATORS
up to 16-Mbyte RAM
ALU
CPU
WATCHDOG TIMER
I/O PORTS
INTERRUPTS
TIMER COUNTERS

PIC


Ports
PORTA
PORTB
PORTC
PPS Module
Memory
Data Memory (RAM)
Program Flash Memory
Data Bus
Instruction Bus
Peripherals
MSSP1
Timers
CCP
FVR
EUSART
ADC
PWM
Interconnect Bus
Program, Debug and Supervisory Modules
MCLR
Single-Supply Programming
In-Circuit Debugger
Power-up Timer
Brown-out Reset
Power-on Reset
WDT
CPU
Interrupt Controller
Oscillator and Clock
HFINTOSC with Active Clock Tuning
OSC1
ECIN
EXTOSC
LFINTOSC
Precision Band Gap Reference

STM


SWCLK
SWDIO
as AF
Serial Wire Debug
CORTEX-M0 CPU
fMAX = 48 MHz
NVIC
Bus matrix
Obl
Flash memory interface
Flash GPL
16/32/64/256 KB
32-bit
SRAM controller
SRAM
4/8/32 KB
POWER
VOLT.REG
3.3 V to 1.8 V
VDD18
@ VDD
VDD = 2.4 to 3.6 V
VSS
SUPPLY SUPERVISION
POR
Reset
Int
POR/PDR
NRST
VDDA
VSSA
VDD
@ VDDA
HSI14
HSI
PLLCLK
LSI
RC 14 MHz
RC 8 MHz
PLL
RC 40 kHz
@ VDDA
@ VDD
XTAL OSC
4-32 MHz
OSC_IN
OSC_OUT
Ind. Window WDG
Power Controller
GP DMA
5 channels
PA[15:0]
PB[15:0]
PC[15:0]
PD2
PF[1:0]
PF[7:4]
GPIO port A
GPIO port B
GPIO port C
GPIO port D
GPIO port F
AHB decoder
RESET & CLOCK CONTROL
System and peripheral clocks
XTAL32 kHz
OSC32_IN
OSC32_OUT
RTC
TAMPER-RTC
(ALARM OUT)
RTC interface
CRC
PWM TIMER 1
4 channels
3 compl. channels
BRK, ETR input as AF
AHB
APB
TIMER 3
4 ch., ETR as AF
TIMER 14
1 channel as AF
TIMER 15
2 channels
1 compl, BRK as AF
55 AF
EXT. IT WKUP
1 channel