Osnove mikroprocesorske elektronike

Marko Jankovec

Asinhrone serijske komunikacije - Primeri

... STM32 G4

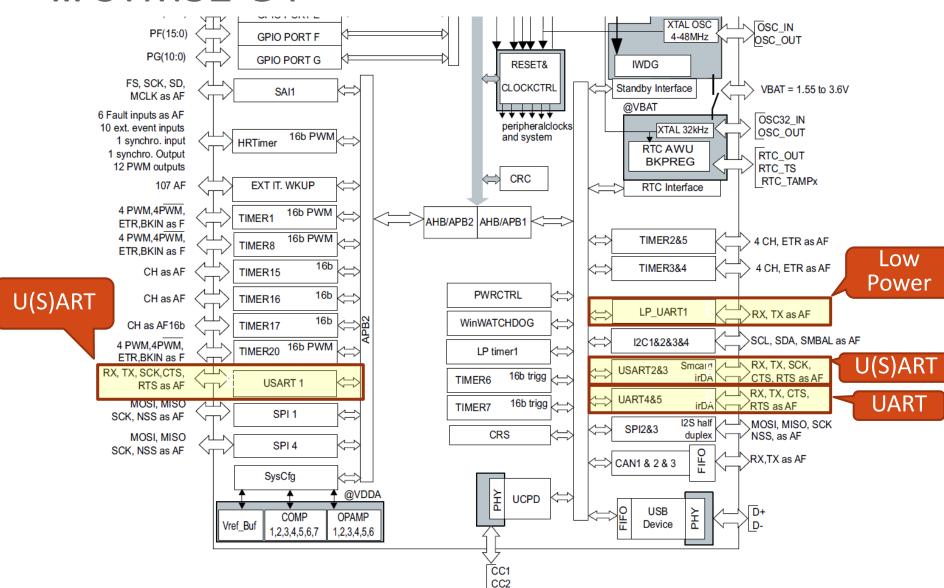


Figure 530. USART block diagram

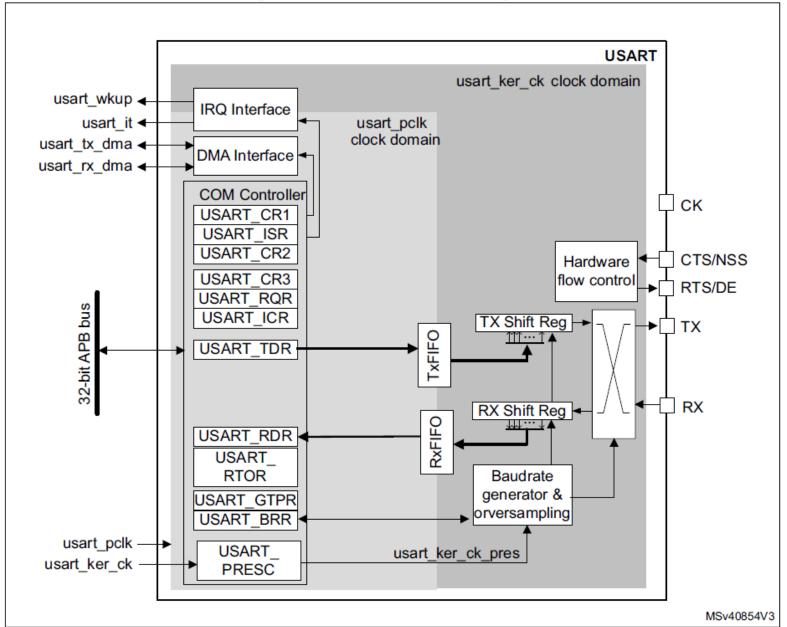
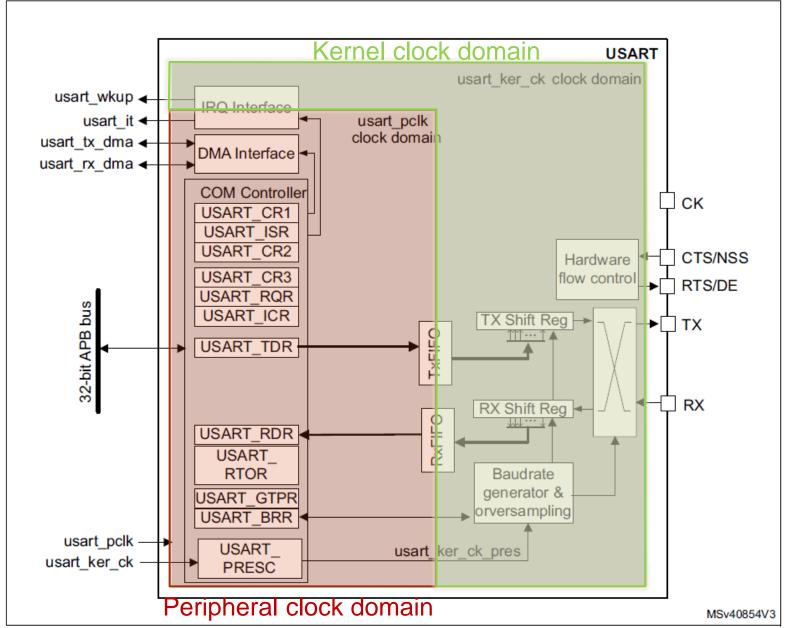


Table 9 USART/UART/I PUART features

Table 9. C	ISARI/UARI	LPUARI	reatures			
USART modes/features ⁽¹⁾	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	Х	Х	X	Х	Х
Continuous communication using DMA	X	Х	Х	Х	Х	Х
Multiprocessor communication	X	Х	Х	X	Х	Х
Synchronous mode	X	Х	Х	-	-	-
Smartcard mode	X	Х	Х	-	-	-
Single-wire half-duplex communication	X	Х	Х	X	Х	Х
IrDA SIR ENDEC block	X	Х	Х	X	Х	-
LIN mode	X	Х	Х	X	X	-
Dual clock domain	Х	Х	Х	X	Х	Х
Wakeup from Stop mode	X	Х	Х	Х	Х	Х
Receiver timeout interrupt	X	Х	Х	X	Х	-
Modbus communication	X	Х	Х	X	Х	-
Auto baud rate detection		X (4 modes)				
Driver Enable	X	Х	Х	X	Х	Х
LPUART/USART data length		7, 8 and 9 bits				
Tx/Rx FIFO		X				
Tx/Rx FIFO size		8				

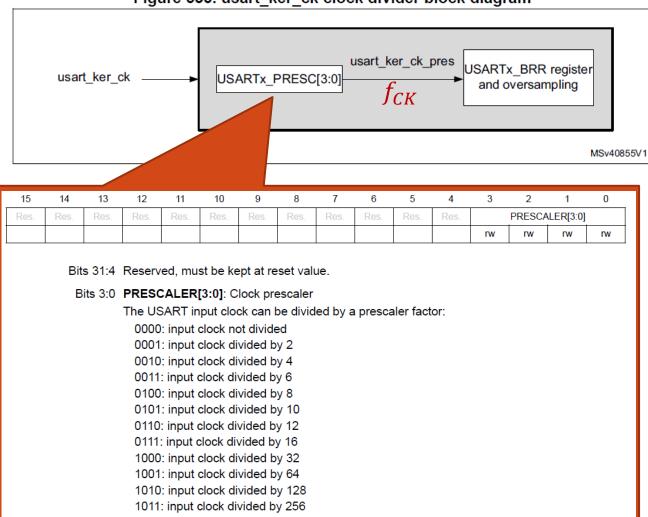
Figure 530. USART block diagram

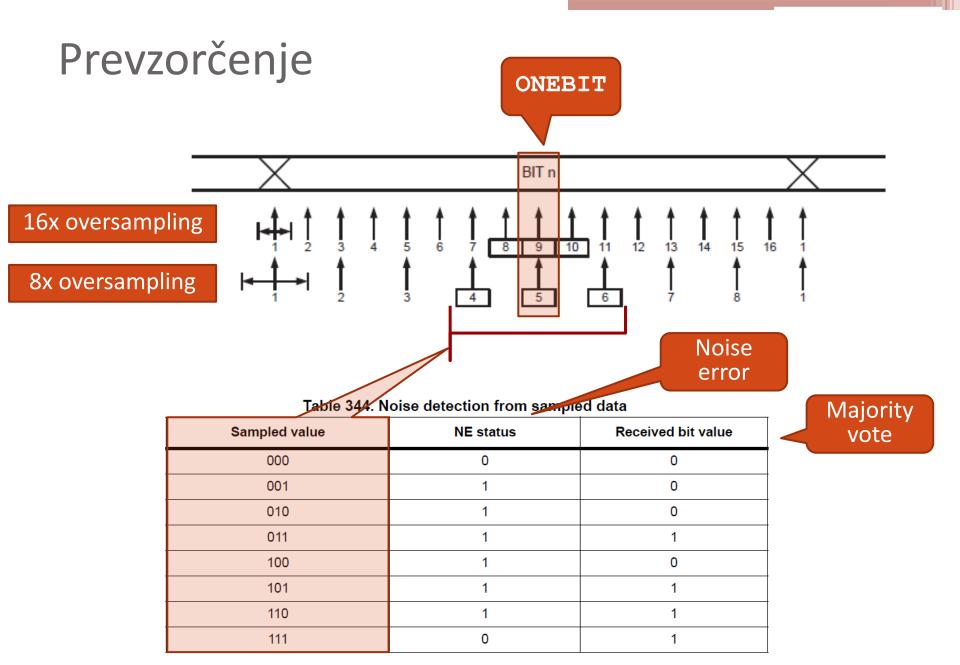


UART primeri 2021/2022 HSE_RTC / 32 Peripheral 144 32.768 LSE 32 To RTC (KHz) HCLK to AHB bus, core, 144 LSIRC clock domain 1-1000 KHz /1 V To Cortex System timer (MHz) Enable CSS 144 FCLK Cortex clock (MHz) To IWDG (KHz) System Clock Mux 170 MHz max PCLK1 144 APB1 peripheral clocks (MHz) SYSCLK (MHz) AHB Prescaler HCLK (MHz) APB1 Prescale HSE X 1 144 ▶ /1 ∨ PLLCLK 170 MHz max PCLK2 144 PLL Source Mux HSIRC APB2 Prescaler APB2 timer clocks (MHz) **→** /1 ∨ X 1 144 12 V X72 V /2 V USART1 Clock Mux HSE PLLQ Kernel /6 V 48 PCLK2 1-48 MHz /Q CK48 Clock Mux PLLP SYSCLK clock domain PLLQ 48 To USB (MHz) HSI ► C 144 To USART1 (MHz) LPUART1 Clock Mux HSI48 RC LSE 48 SYSCLK To RNG (MHz) MCO Source Mux 144 To LPUART1 (MHz) USART2 Clock Mux PCLK1 ADC12 Clock Mux SYSCLK LPTIM1 Clock Mux HSI ► ► 144 To USART2 (MHz) To ADC12 (MHz) HSI 16 LSE PLLCLK LSI ADC345 Clock Mux HSI O 144 To LPTIM1 (MHz) SYSCLK LSE 128 Clock Mux To ADC345 (MHz) SYSCLK PLLQ 12.288 HSI I2S_CKIN 144 To I28 (MHz) USART3 Clock Mux LSCO Source Mux PCLK1 I2C1 Clock Mux SYSCLK HSI 144 To USART3 (MHz) (MHz) LSCO 0.032 SYSCLK SAI Clock Mux To I2C1 (MHz) LSE 144 SYSCLK HSI 144 To SAI1 (MHz) I2C2 Clock Mux UART4 Clock Mux I2S_CKIN PCLK1 N PCLK1 SYSCLK HSI O SYSCLK 144 LSE O 144 To UART4 (MHz) HSI QSPI Clock Mux SYSCLK I2C3 Clock Mux PLLQ 144 To QSPI (MHz) **UARTS Clock Mux** HSI SYSCLK 144 To I2C3 (MHz) SYSCLK HSI HSI O 144 To UARTS (MHz) FDCAN Clock Mux PCLK1 I2C4 Clock Mux

Hitrost prenosa (baud rate)

Figure 535. usart_ker_ck clock divider block diagram





Hitrost prenosa (baud rate)

Figure 535. usart ker ck clock divider block diagram



OVER8=0

$$BAUD = \frac{f_{CK}}{16 \cdot IISARTDIV}$$

OVER8=1

$$BAUD = \frac{f_{CK}}{8 \cdot USARTDIV}$$

$$BRR[15:4] = USARTDIV$$

Primer izračuna

$$BAUD = 9600$$

$$usart_ker_ck = 144 MHz$$

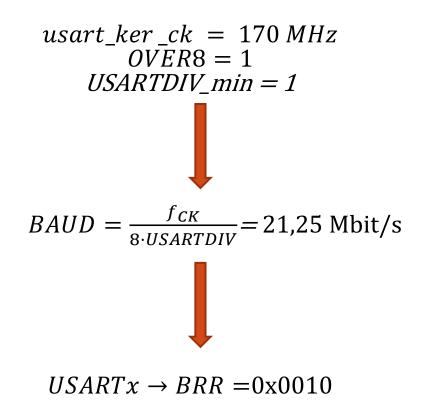
$$OVER8 = 0$$

$$USARTDIV = \frac{f_{CK}}{16 \cdot BAUD} = 937,5$$

$$USARTx \rightarrow BRR = 937 \cdot 16 + 0,5 \cdot 16 = 15000$$

Maksimalne hitrosti

Pri maksimalni frekvenci ure



Dopustne tolerance ure

16x oversampling

8x oversampling

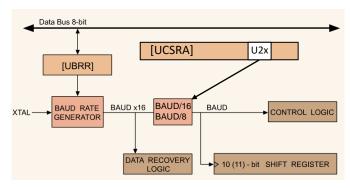
Table 345. Tolerance of the USART receiver when BRR [3:0] = 0000

M bits	OVER8	bit = 0	OVER8 bit = 1		
Wi Dits	ONEBIT = 0	ONEBIT = 0 ONEBIT = 1 ONEBIT = 0		ONEBIT = 1	
00	3.75%	4.375%	2.50%	3.75%	
01	3.41%	3.97%	2.27%	3.41%	
10	4.16%	4.86%	2.77%	4.16%	



Primer pri Atmel AVR

- Za 8 podatkovnih bitov brez paritete, 1 stop bit
 - ±2% napaka frekvence za normalen način
 - ± 1.5 % napaka za dvojno hitrost



		f _{osc} = 16.	0000 MHz		f _{osc} = 18.4320 l				f _{osc} = 20.0000 MHz			
Baud Rate	U2X	n = 0	U2X	n = 1	U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1	
(bps)	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error
2400	416	-0.1%	832	0.0%	479	0.0%	959	0.0%	520	0.0%	1041	0.0%
4800	207	0.2%	416	-0.1%	239	0.0%	479	0.0%	259	0.2%	520	0.0%
9600	103	0.2%	207	0.2%	119	0.0%	239	0.0%	129	0.2%	259	0.2%
14.4k	68	0.6%	138	-0.1%	79	0.0%	159	0.0%	86	-0.2%	173	-0.2%
19.2k	51	0.2%	103	0.2%	59	0.0%	119	0.0%	64	0.2%	129	0.2%
28.8k	34	-0.8%	68	0.6%	39	0.0%	79	0.0%	42	0.9%	86	-0.2%
38.4k	25	0.2%	51	0.2%	29	0.0%	59	0.0%	32	-1.4%	64	0.2%
57.6k	16	2.1%	34	-0.8%	19	0.0%	39	0.0%	21	-1.4%	42	0.9%
76.8k	12	0.2%	25	0.2%	14	0.0%	29	0.0%	15	1.7%	32	-1.4%
115.2k	8	-3.5%	16	2.1%	9	0.0%	19	0.0%	10	-1.4%	21	-1.4%
230.4k	3	8.5%	8	-3.5%	4	0.0%	9	0.0%	4	8.5%	10	-1.4%
250k	3	0.0%	7	0.0%	4	-7.8%	8	2.4%	4	0.0%	9	0.0%
0.5M	1	0.0%	3	0.0%	_	-	4	-7.8%	-	_	4	0.0%
1M	0	0.0%	1	0.0%	_	_	_	_	_	_	_	_
Max. (1)	1 M	bps	2 M	bps	1.152	Mbps	2.304	Mbps	1.25	Mbps	2.5	Mbps

Table 9. USART/UART/LPUART features

Table 9. C	JOAN I/OAN I	LFUARI	icaluics				
USART modes/features ⁽¹⁾	USART1	USART2	USART3	UART4	UART5	LPUART1	
Hardware flow control for modem	X	X	Х	X	X	Х	
Continuous communication using DMA	X	X	Х	X	X	Х	
Multiprocessor communication	X	X	Х	X	X	Х	
Synchronous mode	X	X	Х	-	-	-	
Smartcard mode	X	X	Х	-	-	-	
Single-wire half-duplex communication	X	X	Х	X	X	Х	
IrDA SIR ENDEC block	X	X	Х	X	X	-	
LIN mode	X	X	Х	X	X	-	
Dual clock domain	X	X	Х	X	X	Х	
Wakeup from Stop mode	X	X	Х	Х	X	Х	
Receiver timeout interrupt	Х	X	Х	X	X	-	
Modbus communication	Х	Х	Х	X	X	-	
Auto baud rate detection		X (4 modes)					
Driver Enable	Х	Х	Х	X	Х	Х	
LPUART/USART data length		•	7, 8 ar	nd 9 bits	•	•	
Tx/Rx FIFO		X					
Tx/Rx FIFO size				8			

Avtomatska detekcija hitrosti komunikacije (ABREN)

ABRMOD[1:0]	Vzorec	Meritev
00	1xxx xxxx	Dolžina START bita
01	10xx xxxx	Dolžina START bita + prva "1"podatka
10	OxFE	Dolžina START bita + dolžina do konca bita 6
11	0x55	Dolžina START bita + bit 0 + bit6

UART primeri 2021/2022

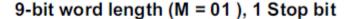
Table 9. USART/UART/LPUART features

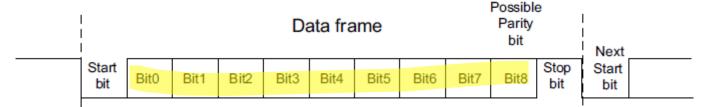
Table 9. C	JSAKI/UAKI	LPUARI	reatures				
USART modes/features ⁽¹⁾	USART1	USART2	USART3	UART4	UART5	LPUART1	
Hardware flow control for modem	X	Х	Х	X	X	Х	
Continuous communication using DMA	X	Х	Х	X	X	Х	
Multiprocessor communication	Х	Х	Х	Х	X	Х	
Synchronous mode	X	Х	Х	-	-	-	
Smartcard mode	Х	Х	Х	-	-	-	
Single-wire half-duplex communication	Х	Х	Х	X	X	X	
IrDA SIR ENDEC block	X	Х	Х	Х	X	-	
LIN mode	Х	Х	Х	X	Х	-	
Dual clock domain	Х	Х	X	X	Х	X	
Wakeup from Stop mode	Х	Х	X	X	Х	Х	
Receiver timeout interrupt	Х	Х	X	X	Х	-	
Modbus communication	Х	Х	Х	X	X	-	
Auto baud rate detection		X (4 modes)					
Driver Enable	Х	Х	Х	X	X	Х	
LPUART/USART data length		!	7, 8 ar	nd 9 bits		,	
Tx/Rx FIFO		X					
Tx/Rx FIFO size				8			

Možnosti podatkovnega okvirja

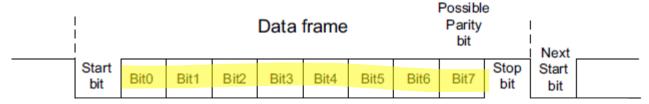
7,8 ali 9-bit dolžina podatka (M[1:0])

Figure 531. Word length programming

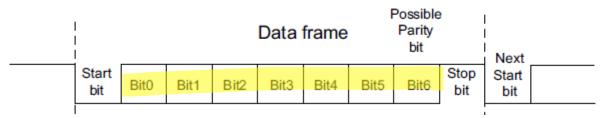




8-bit word length (M = 00), 1 Stop bit



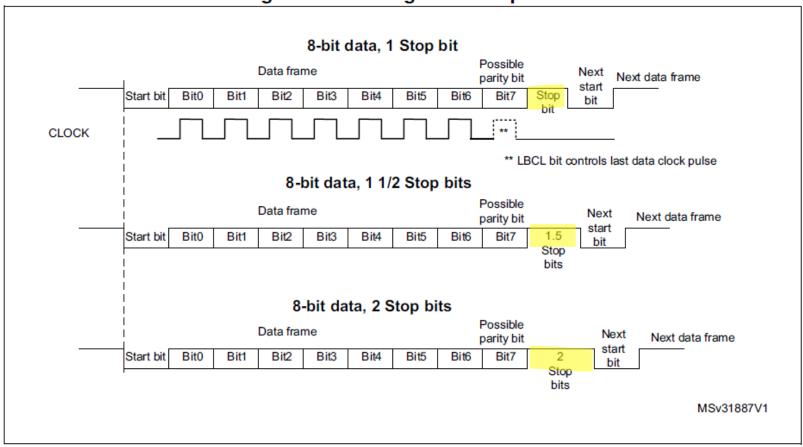
7-bit word length (M = 10), 1 Stop bit



Možnosti podatkovnega okvirja

1, 1.5 ali 2 stop bita (STOP[1:0])

Figure 532. Configurable stop bits



Možnosti podatkovnega okvirja

Liha ali soda pariteta (PS in PCE)

PS: Parity selection 0: Even parity 1: Odd parity

Table 347, USART frame formats

M bits	PCE bit	USART frame ⁽¹⁾
00	0	SB 8 bit data STB
00	1	SB 7-bit data PB STB
01	0	SB 9-bit data STB
01	1	SB 8-bit data PB STB
10	0	SB 7bit data STB
10	1	SB 6-bit data PB STB

^{1.} Legends: SB: start bit, STB: stop bit, PB: parity bit. In the data register, the PB is always taking the MSB position (8th or 7th, depending on the M bit value).

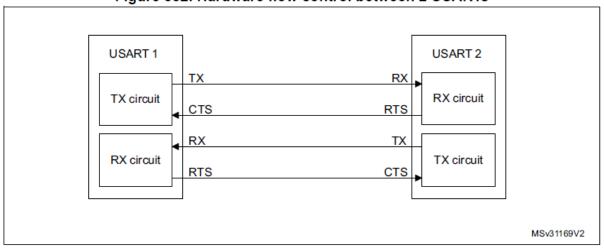
Nekatere ostale možnosti

- Zaporedje bitov: prvi MSB ali prvi LSB (MSBFIRST)
- Zamenjava Tx in Rx pinov (SWAP)
- Invertiranje Tx in Rx pinov (TXINV, RXINV)
- Invertiranje podatkov (DATAINV)
- Signali za rokovanje (CTSE, RTSE)
- RS485 signali (DEM, DEP, DAT, DEDT)
- Half-duplex način delovanja (HDSEL)

MSv31168V1

Rokovanje - handshaking

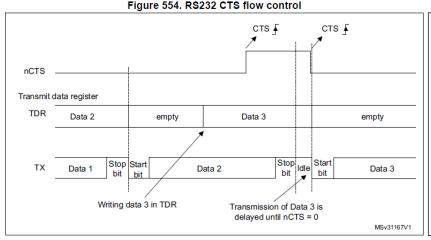
Figure 552. Hardware flow control between 2 USARTs

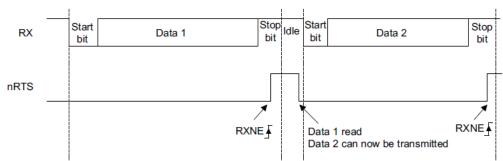


CTS - Vhod, visoko stanje ustavi oddajo (CTSE)

RTS - Izhod, nizko stanje pomeni pripravljenost za sprejem (RTSE)

Figure 553. RS232 RTS flow control





Pošiljanje podatka

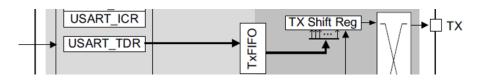
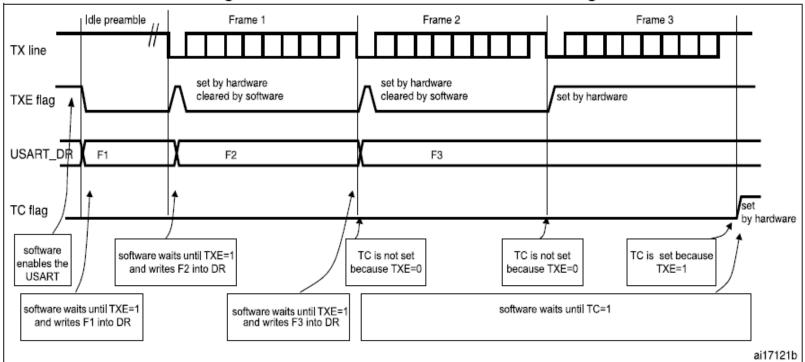


Figure 533. TC/TXE behavior when transmitting



- Omogoči oddajnik (TE = 1)
- Preveri, če je USART_TDR prazen (TXE==1?)
- Vpiši podatek v USART TDR
 - Avtomatsko postavi TXE = 0
 - Ko se podatek dejansko pošlje se postavi TC = 1

Poizvedovanje - polling

Sprejem podatka

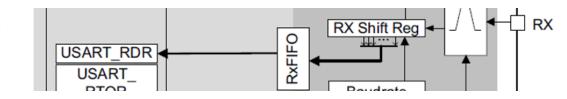
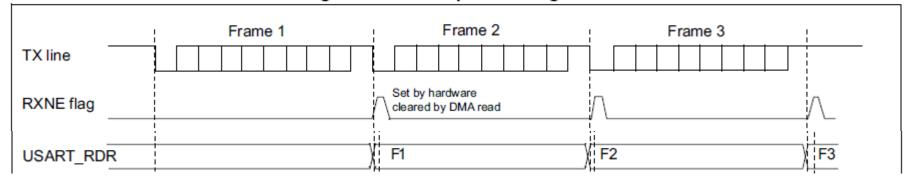


Figure 551. Reception using DMA



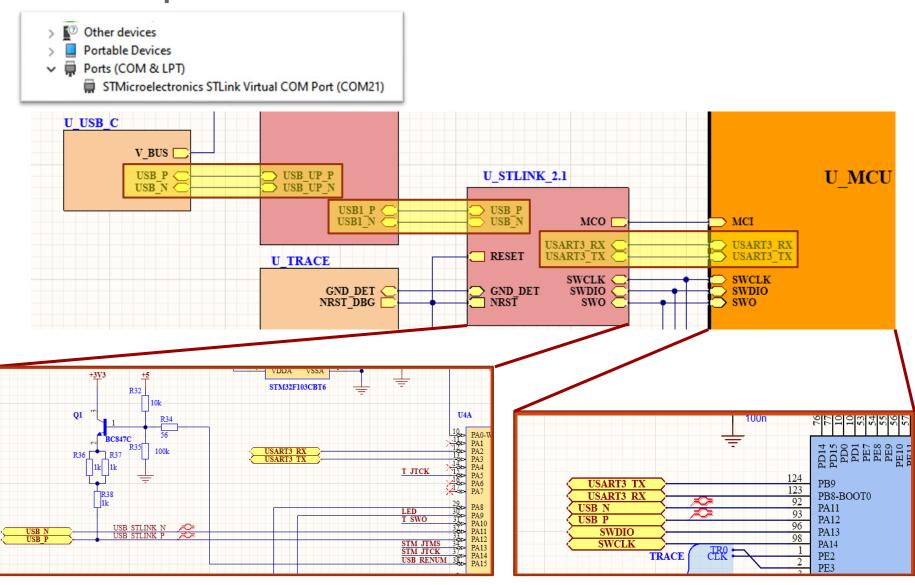
- Omogoči sprejemnik (RE=1)
- Preveri, če je v USART RDR nov podatek (RXNE==1?)
- Preberi podatek iz USART_RDR
 - Avtomatsko postavi RXNE=0

Poizvedovanje - polling

Detekcija napak pri sprejemu

- Overrun
 - Če je RXNE==1 in pride nov podatek
 - Postavi se ORE=1
 - Vsebina USART RDR se ohrani
- Noise error (NE)
 - Pri prevzorčenju trije sredinski biti niso bili enaki
- Framing error (FE)
 - Napaka pri okvirju (npr. ni zaznan stop bit)
- Parity error (PE)
 - Napaka pri preverjanju paritete sporočila

UART pri MiŠKo 3



Primer FT232R kot USB-UART vmesnika

7.4 USB to MCU UART Interface

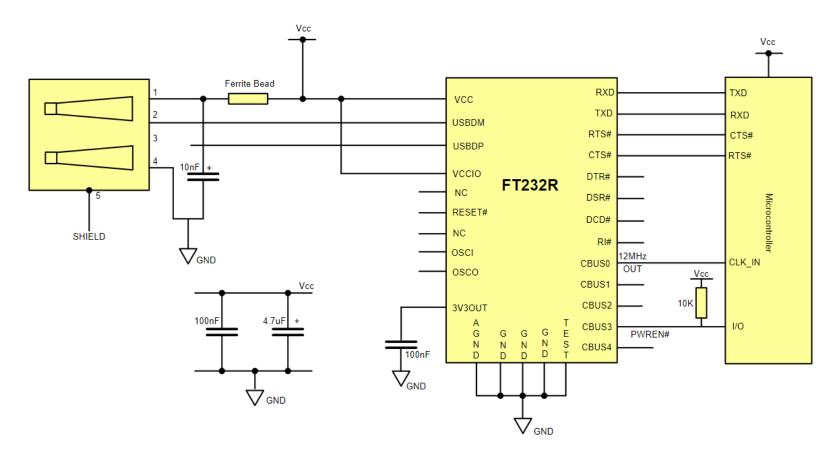
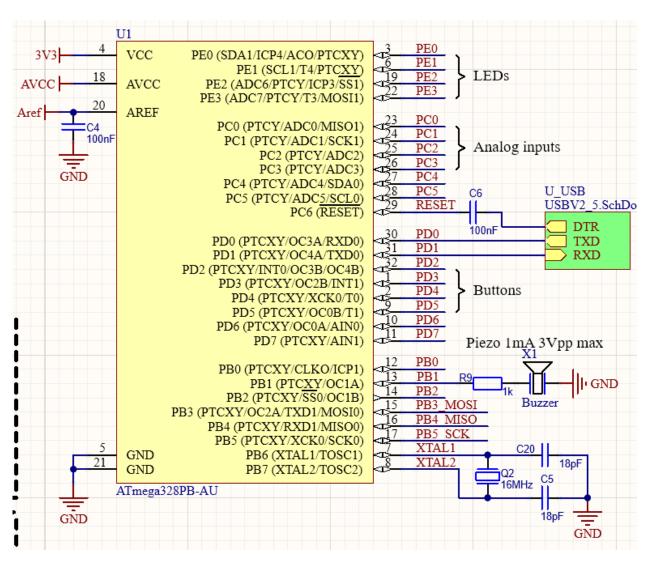


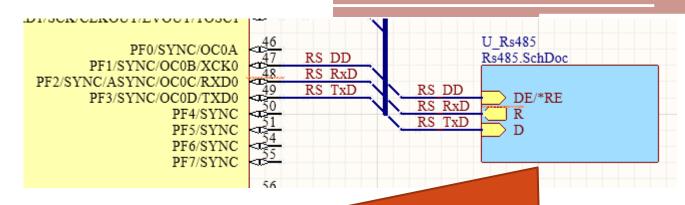
Figure 7.4 USB to MCU UART Interface

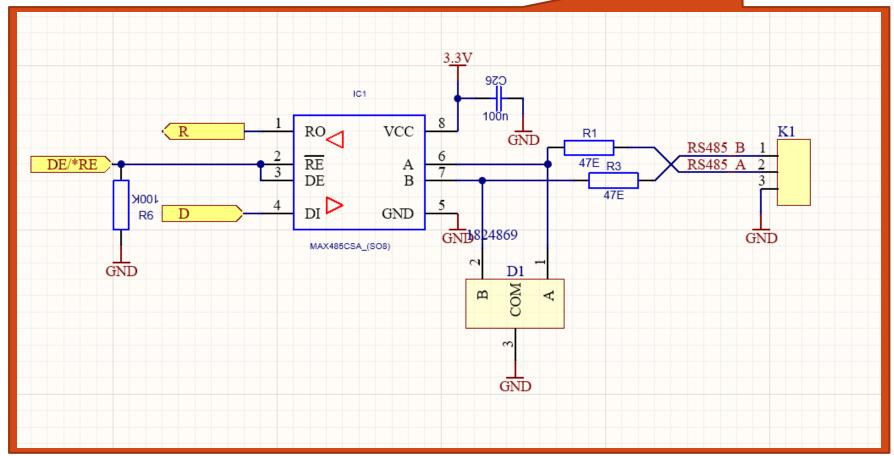
Primer FT232R pri MiŠKo 2 in Arduino



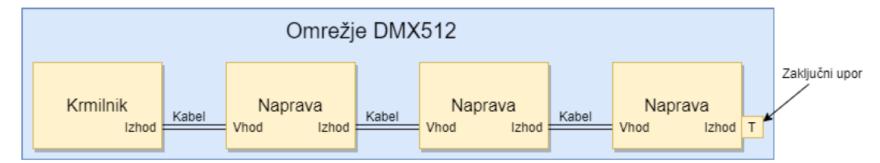
UART primeri 2021/2022

RS-485





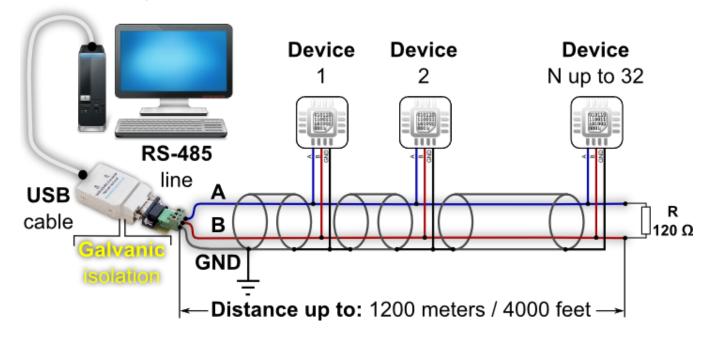
Primeri uporabe RS-485 – DMX512

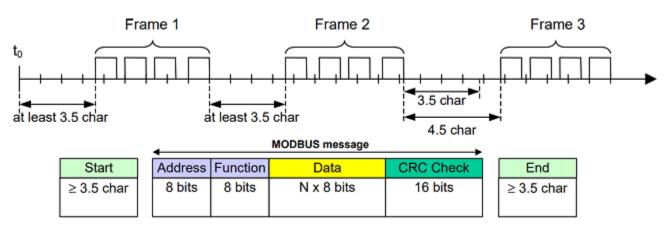






Primeri uporabe RS-485 – MODBUS





Primer



Vmesnik LIN

