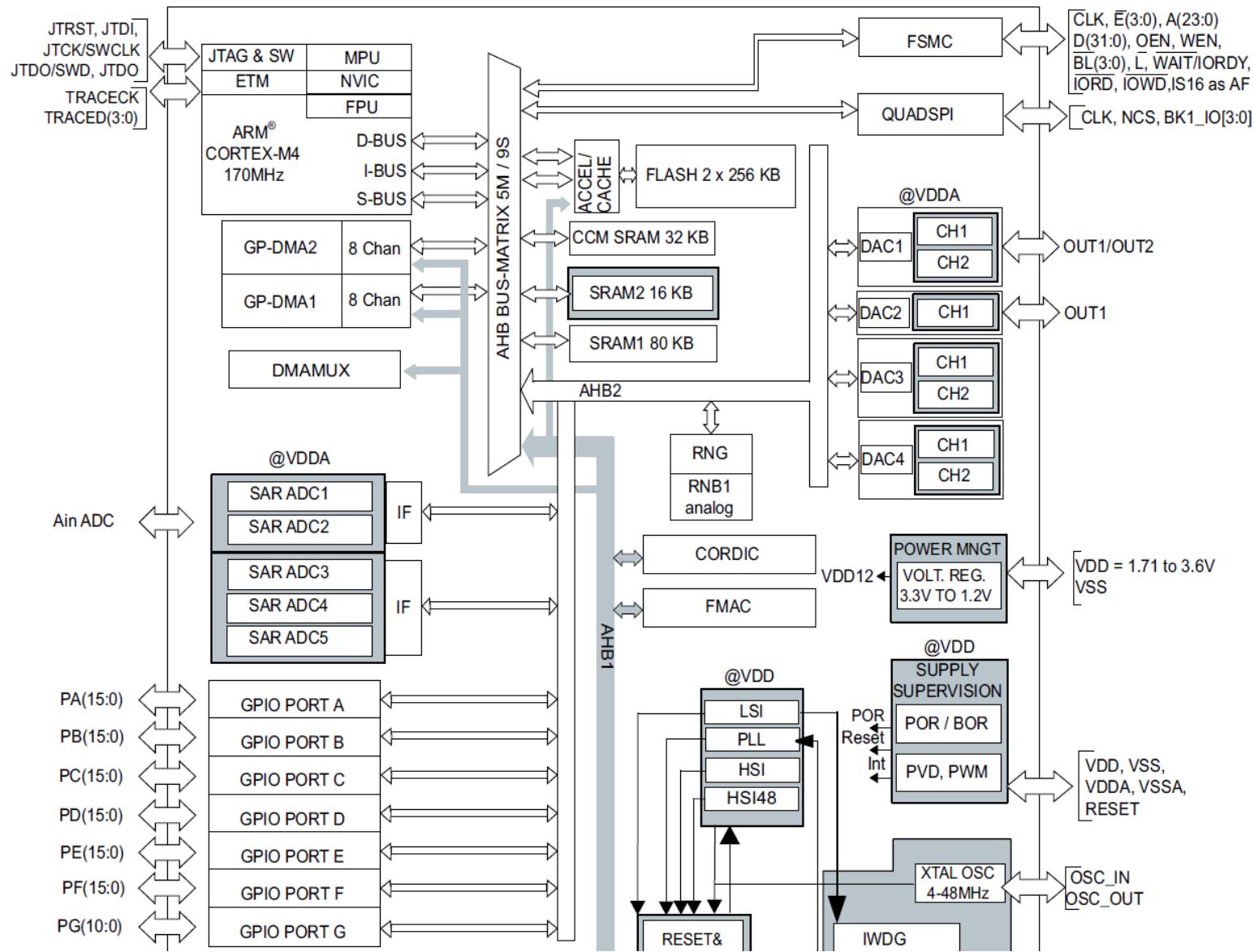


Osnove mikroprocesorske elektronike

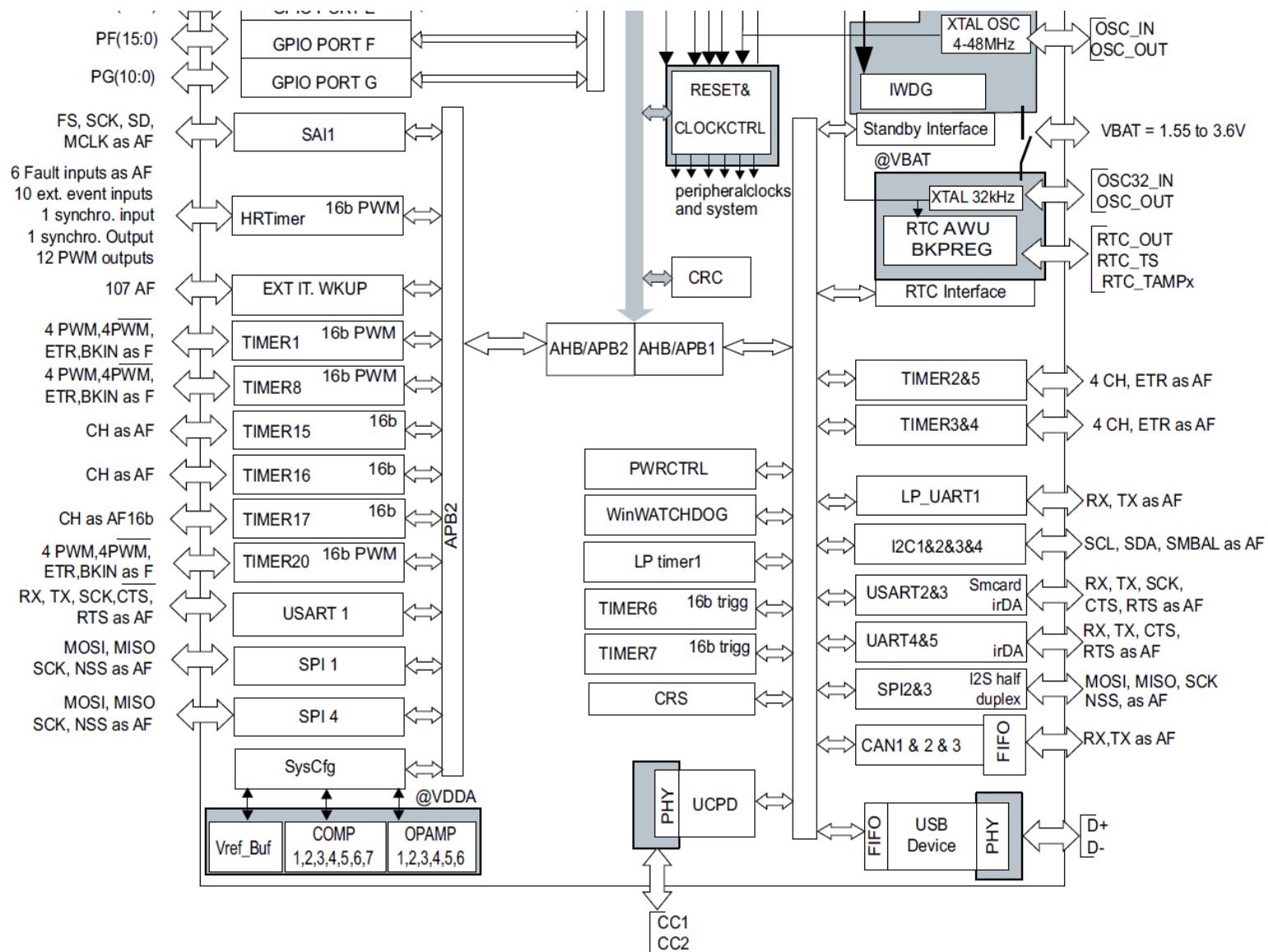
Marko Jankovec

Podporni sistemi mikrokrmilnikov

STM32 G4 ...

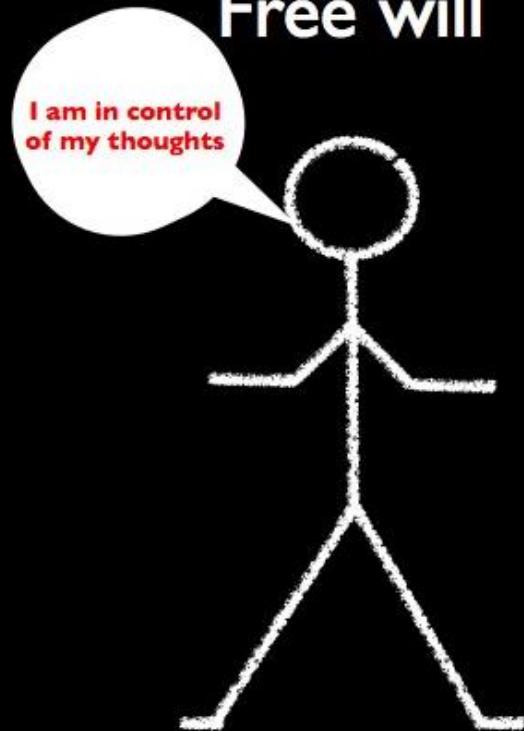


... STM32 G4

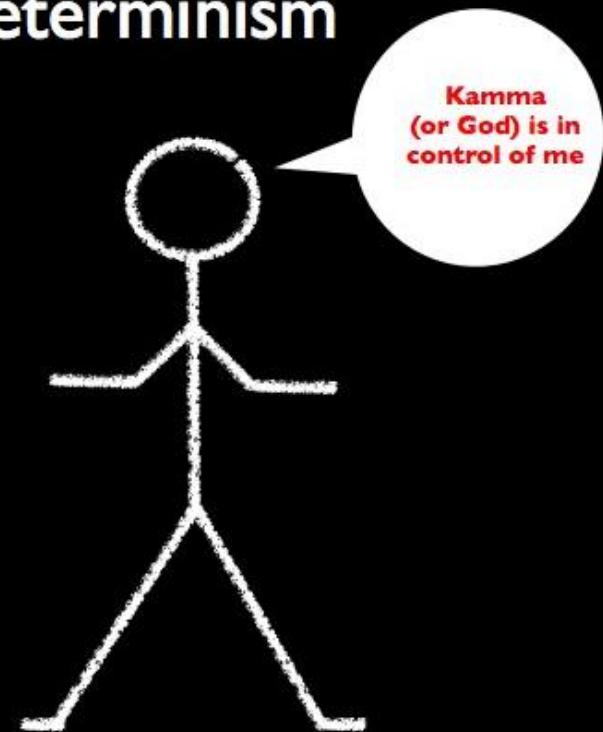


Svobodna volja ali determinizem?

Free will



Determinism

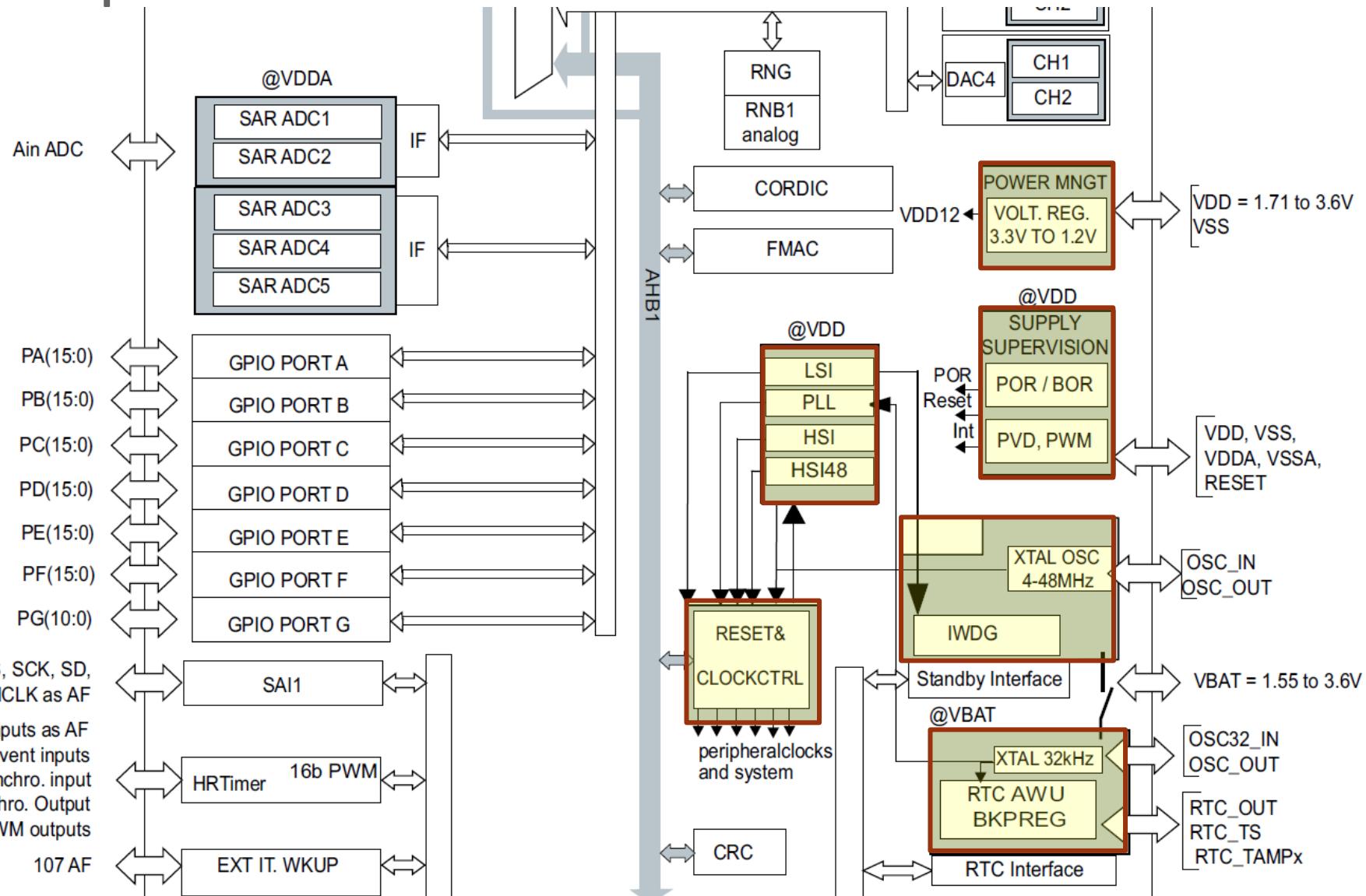


VS

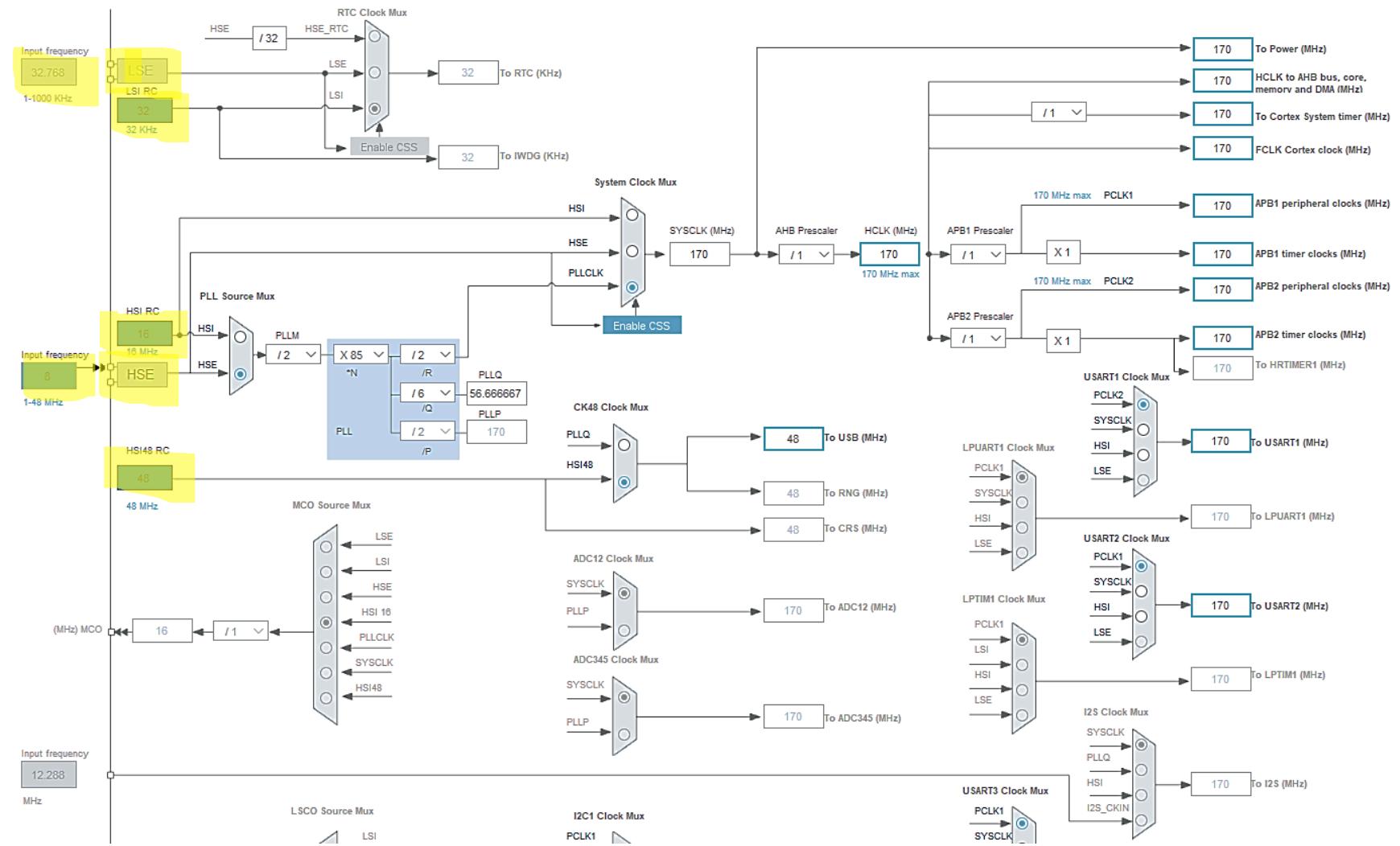
This is me, this is mine and this is myself

This is all my kamma
(or "Gods" wish)

Podporni sistemi v STM32G4

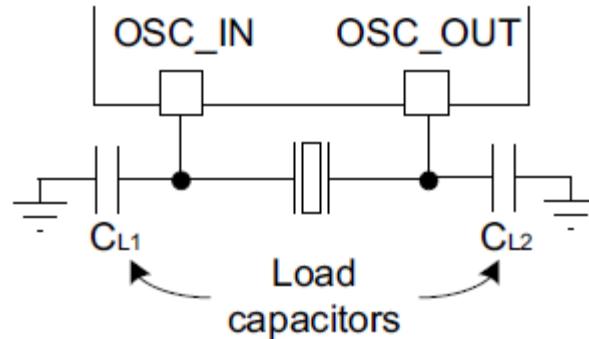


Distribucija ure



HSE – High-speed External Clock

Zunanji kristalni rezonator



Zunanji vir ure

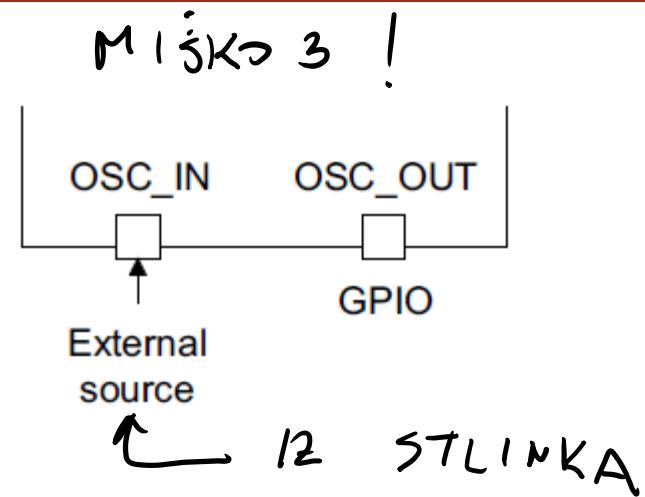


Table 39. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	

LSE – Low-speed External Clock

- Zunanji nizkofrekvenčni kristalni rezonator

$$32768 = 2^{15} = 2^h$$

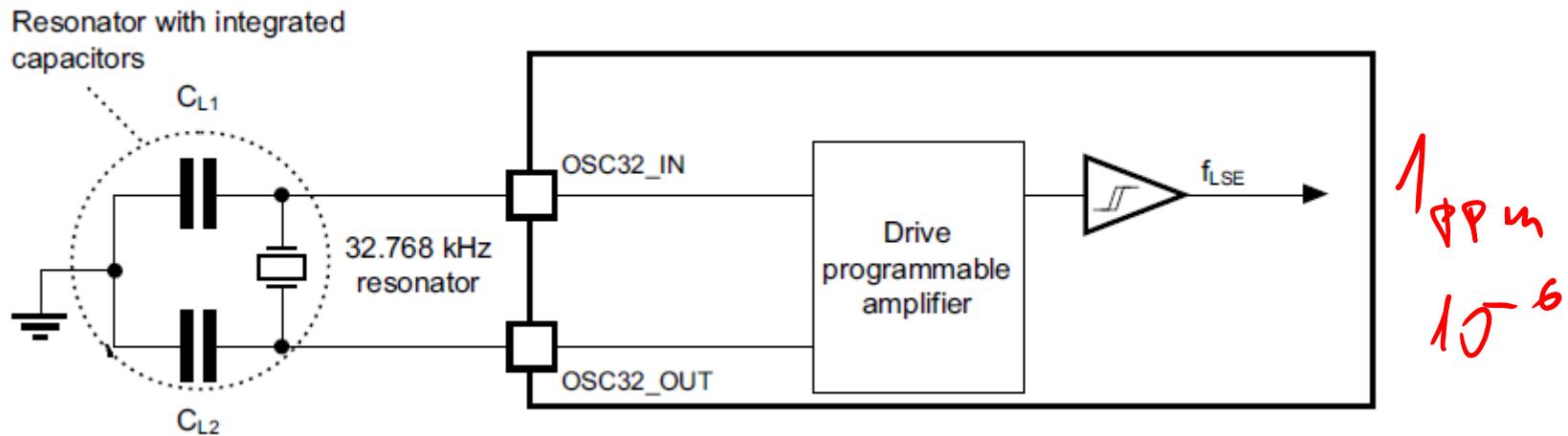


Table 40. Low-speed external user clock characteristics⁽¹⁾ URB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz

Notranji urini viri – HSI16 → TRIM 2
LSE

High-speed internal (HSI16) RC oscillator

Table 43. HSI16 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	$V_{DD}=3.0\text{ V}$, $T_A=30\text{ }^\circ\text{C}$	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16) ⁽²⁾	Duty Cycle	-	45	-	55	%
$\Delta_{Temp}(HSI16)$	HSI16 oscillator frequency drift over temperature	$T_A= 0 \text{ to } 85\text{ }^\circ\text{C}$	-1	-	1	%
		$T_A= -40 \text{ to } 125\text{ }^\circ\text{C}$	-2	-	1.5	%
$\Delta_{VDD}(HSI16)$	HSI16 oscillator frequency drift over V_{DD}	$V_{DD}=1.62\text{ V to } 3.6\text{ V}$	-0.1	-	0.05	%

Notranji urini viri – HSI48

OSB SINHR

High-speed internal 48 MHz (HSI48) RC oscillator

Table 44. HSI48 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	$V_{DD}=3.0V$, $T_A=30^\circ C$	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11 ⁽²⁾	0.18 ⁽²⁾	%
USER TRIM COVERAGE	HSI48 user trimming coverage	± 32 steps	$\pm 3^{(3)}$	$\pm 3.5^{(3)}$	-	%
DuCy(HSI48)	Duty Cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
ACC _{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	$V_{DD} = 3.0 V$ to $3.6 V$, $T_A = -15$ to $85^\circ C$	-	-	$\pm 3^{(3)}$	%
		$V_{DD} = 1.65 V$ to $3.6 V$, $T_A = -40$ to $125^\circ C$	-	-	$\pm 4.5^{(3)}$	
D _{VDD} (HSI48)	HSI48 oscillator frequency drift with V_{DD}	$V_{DD} = 3 V$ to $3.6 V$	-	0.025 ⁽³⁾	0.05 ⁽³⁾	%
		$V_{DD} = 1.65 V$ to $3.6 V$	-	0.05 ⁽³⁾	0.1 ⁽³⁾	

Notranji urini viri – LSI

← Uporaba za WDT

Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	$V_{DD} = 3.0 \text{ V}$, $T_A = 30 \text{ }^\circ\text{C}$	31.04	-	32.96	kHz
		$V_{DD} = 1.62 \text{ to } 3.6 \text{ V}$, $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$	29.5	-	34	
$t_{SU(LSI)}$ ⁽²⁾	LSI oscillator start-up time	-	-	80	130	μs

PLL – fazno sklenjena zanka

Table 46. PLL characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽²⁾	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1 Boost mode	2.0645	-	170	MHz
		Voltage scaling Range 1	2.0645	-	150	
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1 Boost mode	8	-	170	MHz
		Voltage scaling Range 1	8	-	150	
		Voltage scaling Range 2	8	-	26	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1 Boost mode	8	-	170	MHz
		Voltage scaling Range 1	8	-	150	
		Voltage scaling Range 2	8	-	26	

Clock out - MCO

Screenshot of the Miskos v1.0.ioc - Pinout & Configuration tool interface.

The left sidebar shows categories: System Core (DMA, GPIO, IWDG, NVIC, RCC, SYS, WWDG), Analog, Timers, Connectivity, Multimedia, Security, Computing, Middleware, Utilities.

The main tab is "Clock Configuration".

RCC Mode and Configuration

- High Speed Clock (HSE) : BYPASS Clock Source
- Low Speed Clock (LSE) : Disable
- Master Clock Output (highlighted with a red circle)
- LSCO Clock Output
- Audio Clock Input (I2S_CKIN)
- CRS SYNC : Disable

Configuration

Reset Configuration

User Constants, NVIC Settings, GPIO Settings, Parameter Settings (all checked)

Configure the below parameters :

VDD voltage (V) : 3.3 V
Instruction Cache : Enabled
Prefetch Buffer : Disabled
Data Cache : Enabled
Flash Latency(WS) : 4 WS (5 CPU cycle)

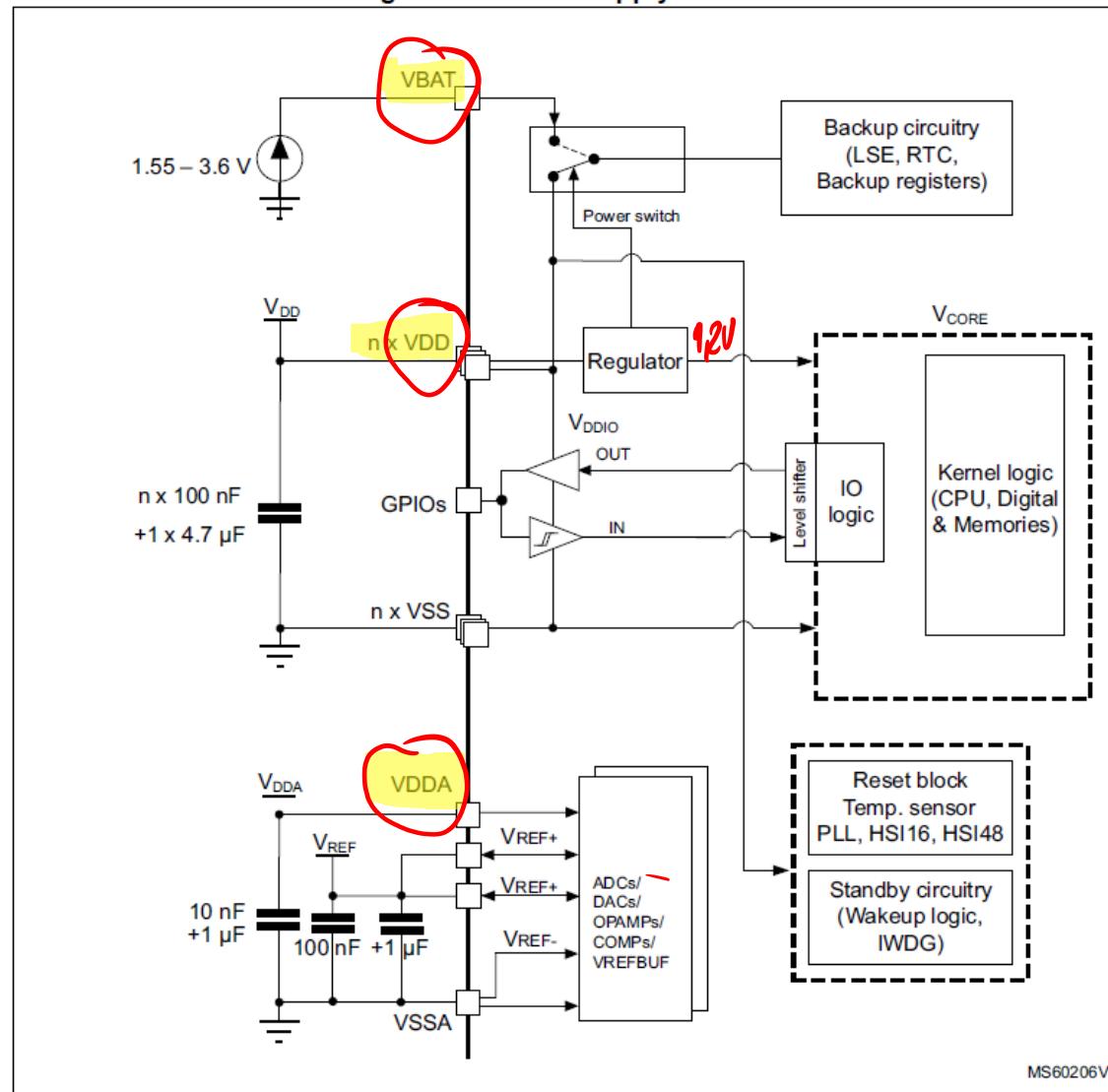
RCC Parameters

HSI Calibration Value : 64
HSE Startup Timeout Value (ms) : 100

On the right, there is a pinout diagram for the STM32G474QETx showing pins 1 through 108. A yellow oval highlights pins 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108. A red arrow points from the "Master Clock Output" setting to this pinout diagram.

Napajjalna shema STM32

Figure 16. Power supply scheme

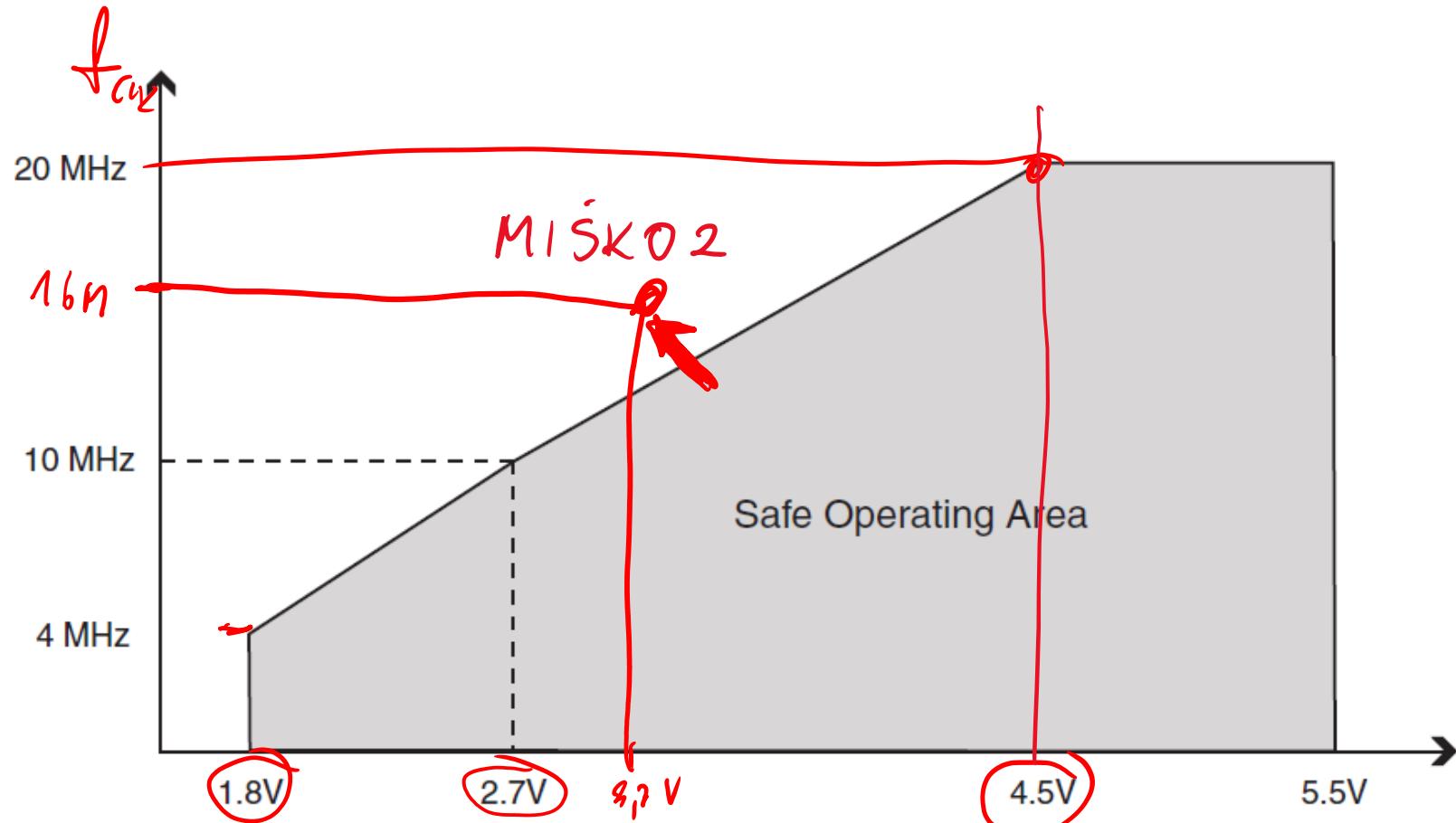


Območje napajalne napetosti STM32

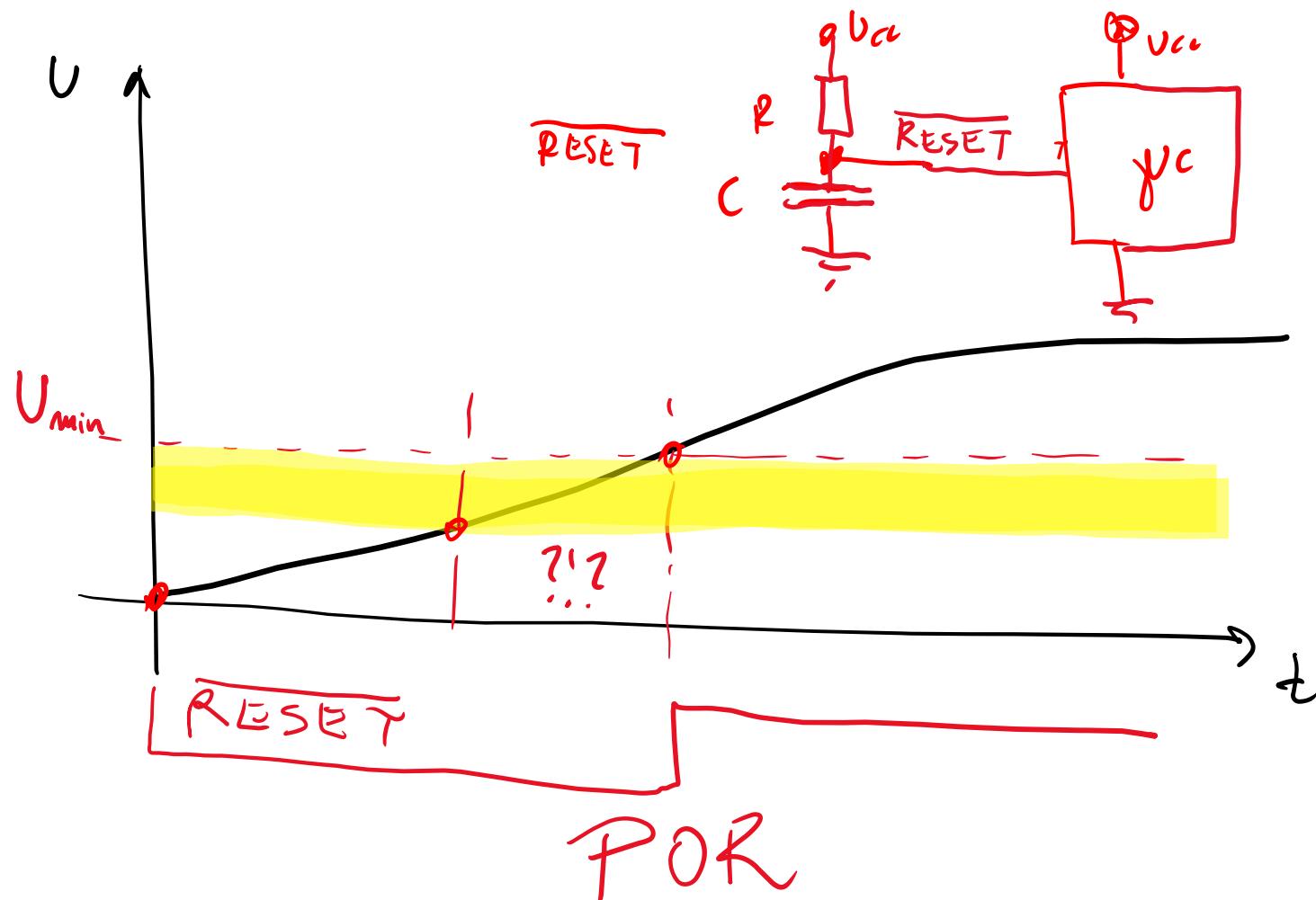
Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.71 ⁽¹⁾	3.6	V
V_{DDA}	Analog supply voltage	ADC	1.62		
		DAC 1 MSPS or DAC 15 MSPS or OPAMP	1.8	3.6	
		COMP used	1.8	3.6	
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0	3.6	
V_{BAT}	Backup operating voltage	-	1.55	3.6	V

Območje napajalnih napetosti in frekvenc za Atmel AVR mikrokrmilnike



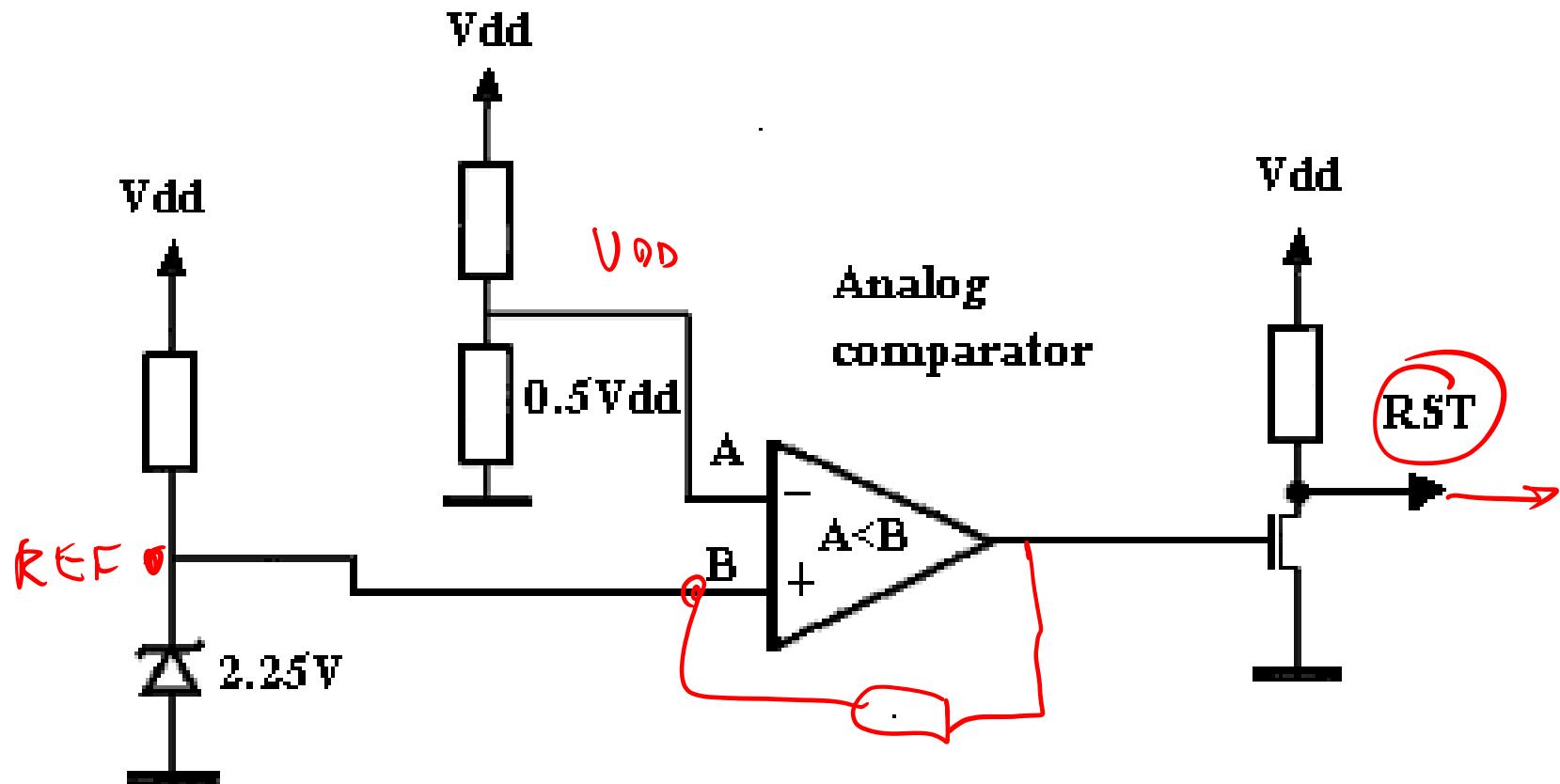
Počasno naraščanje napetosti ob vklopu



Prenihaj napajalne napetosti

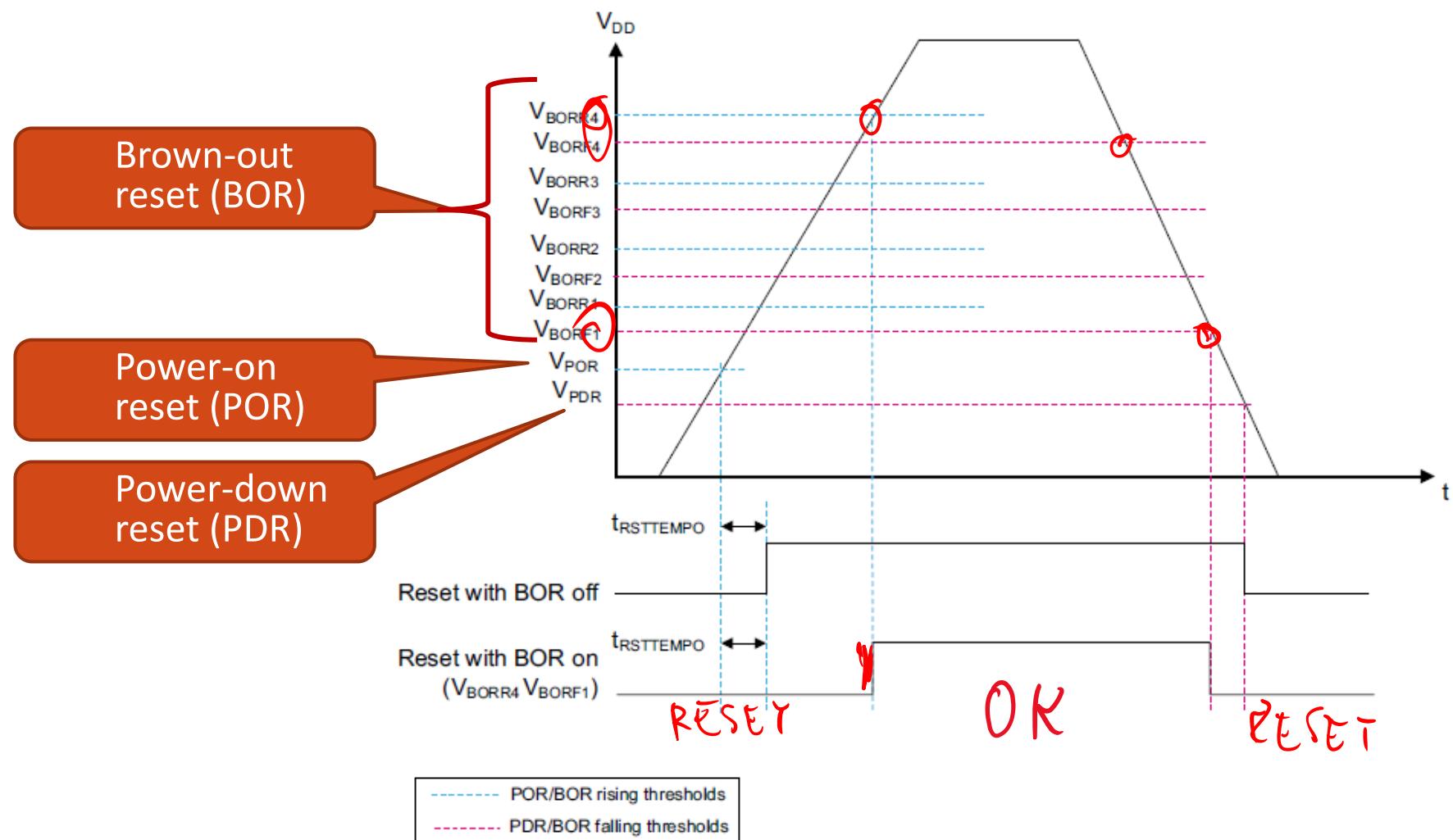


Nadzor napajanja

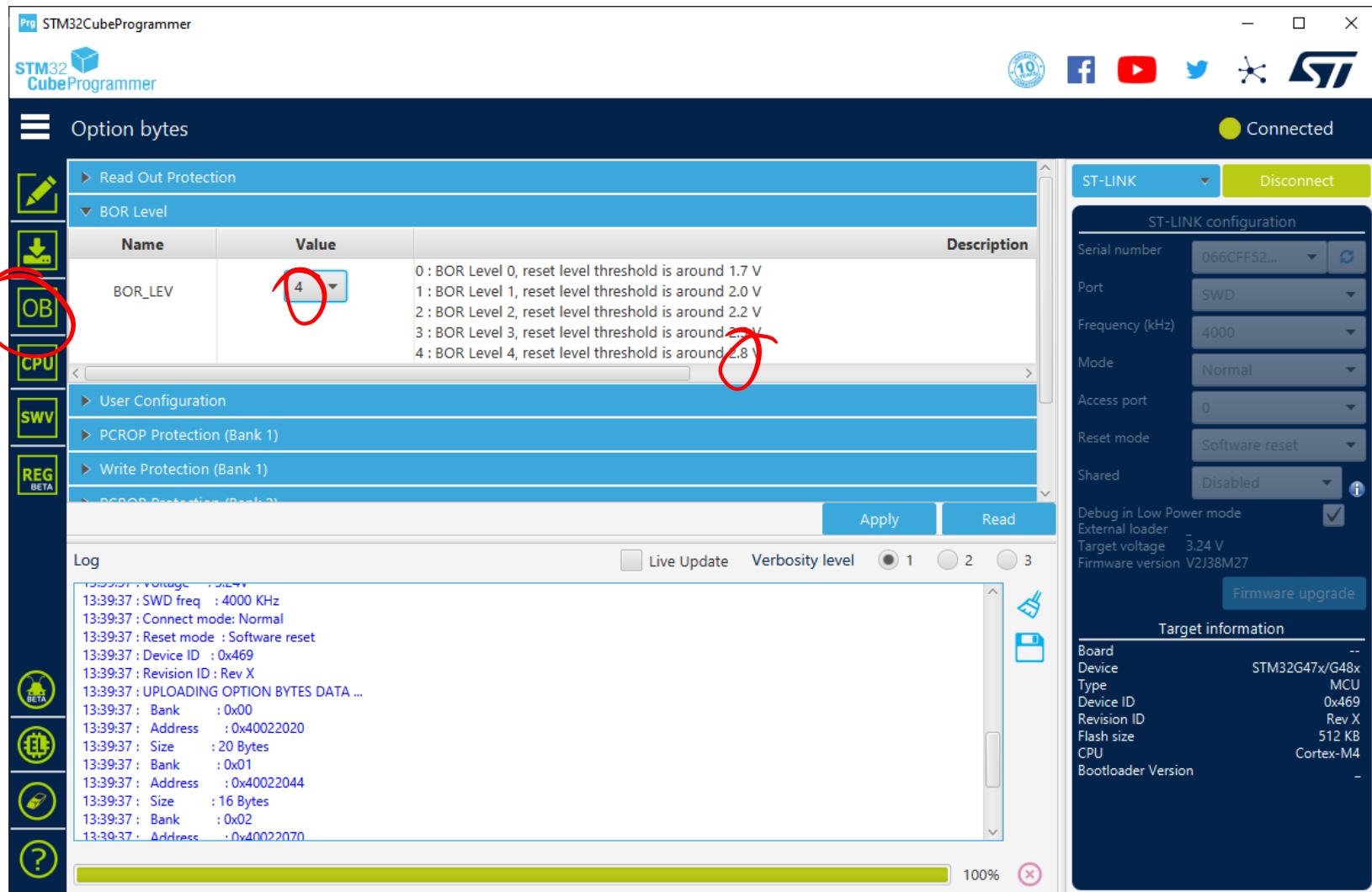


Nadzor napajanja (supply supervision) pri STM32

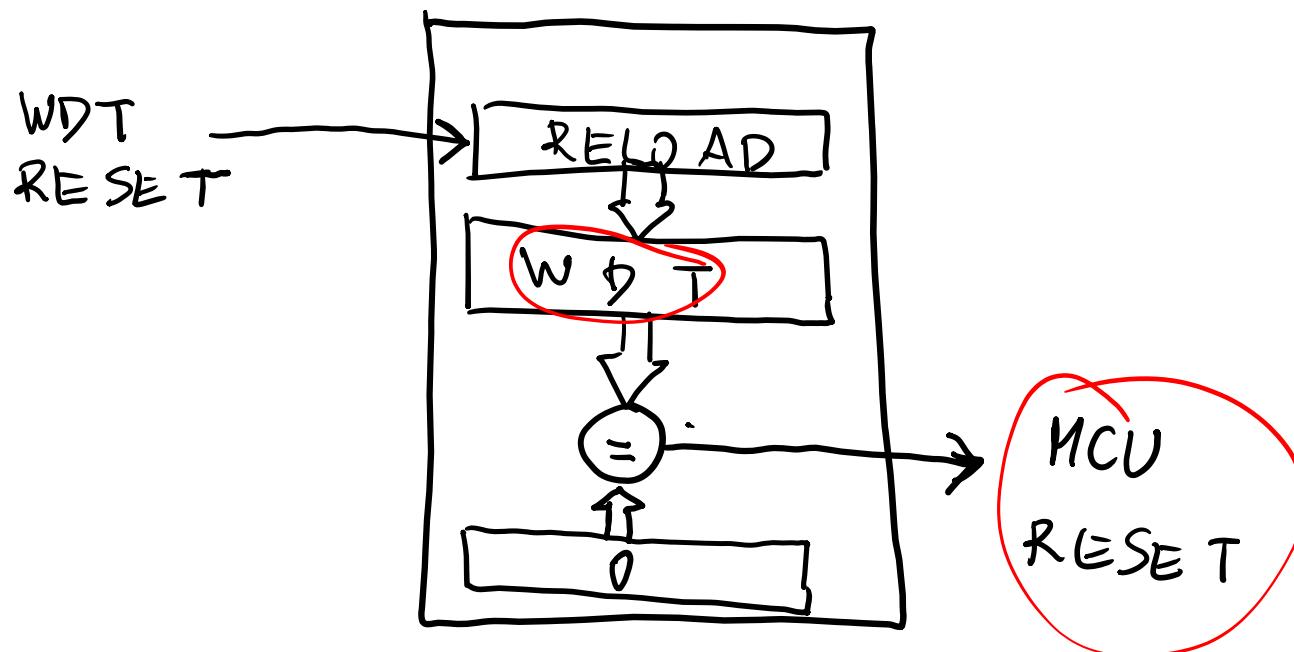
Figure 13. Brown-out reset waveform



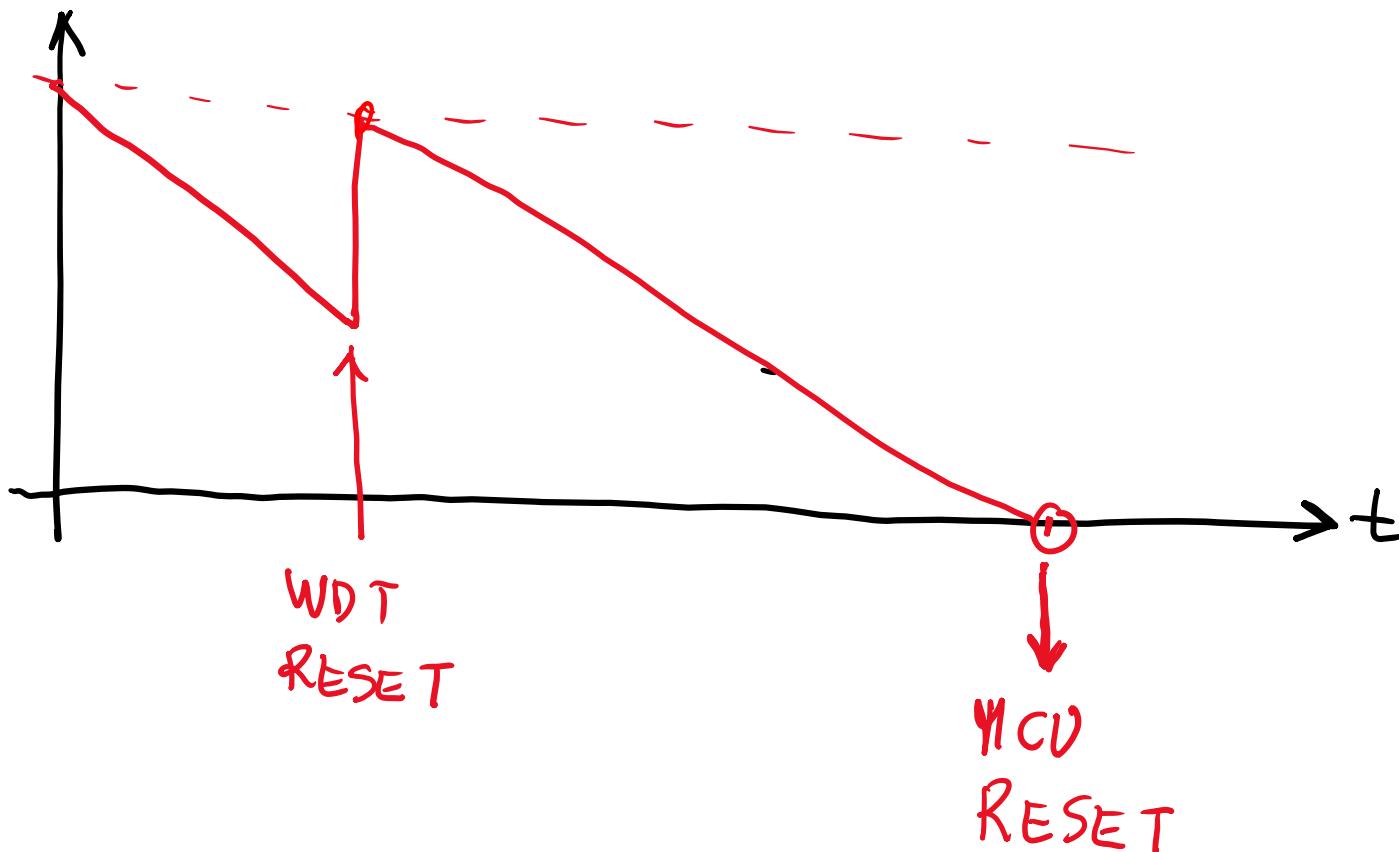
Nastavitev v STM32 Cube programmer



Watchdog - čuvaj, (pes čuvaj, kuža pazi, čivava na straži, rotvajler,...)



Časovni diagram enostavnega WDT

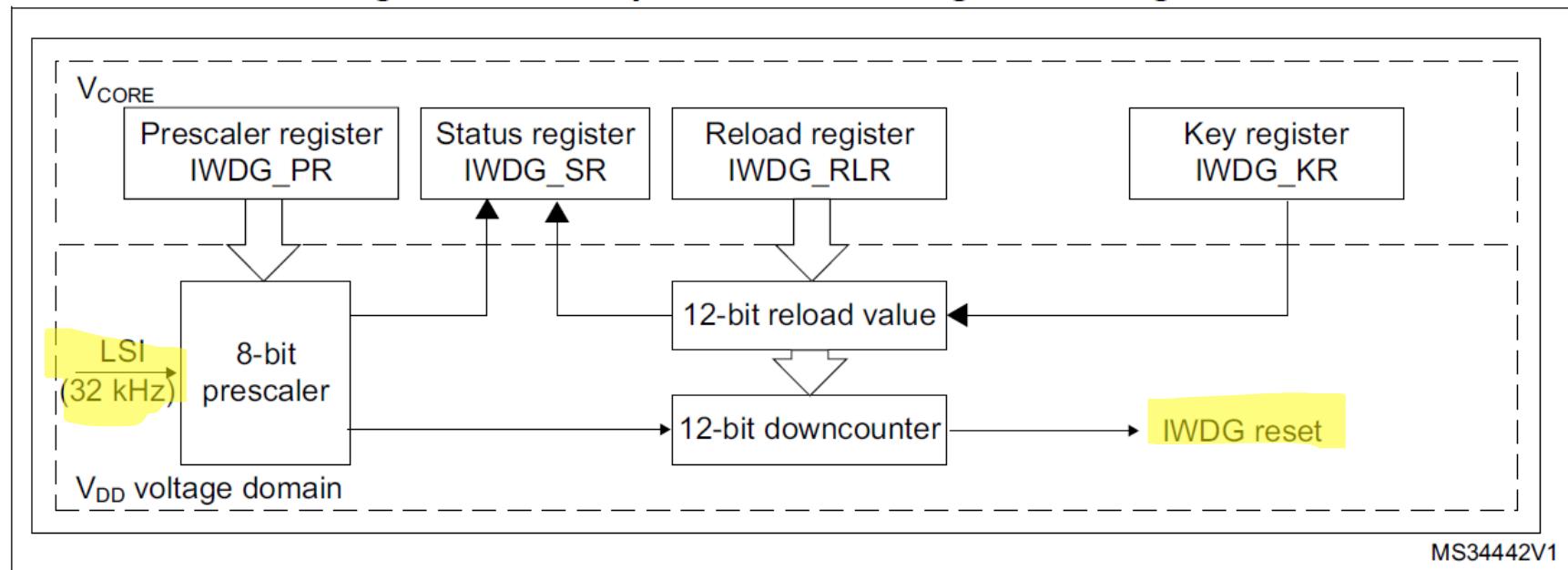


Časovni diagram okenskega WDT



IWDG – Independent Watchdog

Figure 659. Independent watchdog block diagram



MS34442V1

- Lahko je
 - navaden WDT
 - Okenski WDT, kjer je MIN = 0

Nastavitev v CubeMX

The screenshot shows the CubeMX software interface. The left side features a sidebar with categories like DMA, GPIO, IWDG, NVIC, RCC, SYS, and WWDG. The 'IWDG' item is selected and highlighted in blue. The main area has two tabs: 'Pinout & Configuration' (selected) and 'Clock Configuration'. The 'Clock Configuration' tab is currently active, showing the 'Software Packs' section. Under 'Software Packs', the 'IWDG Mode and Configuration' section is expanded, showing the 'Mode' tab with the 'Activated' checkbox checked. Below this is the 'Configuration' tab, which contains a 'Reset Configuration' button. At the bottom of the configuration section, there are tabs for 'Parameter Settings' and 'User Constants', with 'Parameter Settings' being the active tab. A search bar at the bottom allows for searching parameters by name.

Pinout & Configuration

Clock Configuration

Software Packs

IWDG Mode and Configuration

Mode

Activated

Configuration

Reset Configuration

Parameter Settings

User Constants

Configure the below parameters :

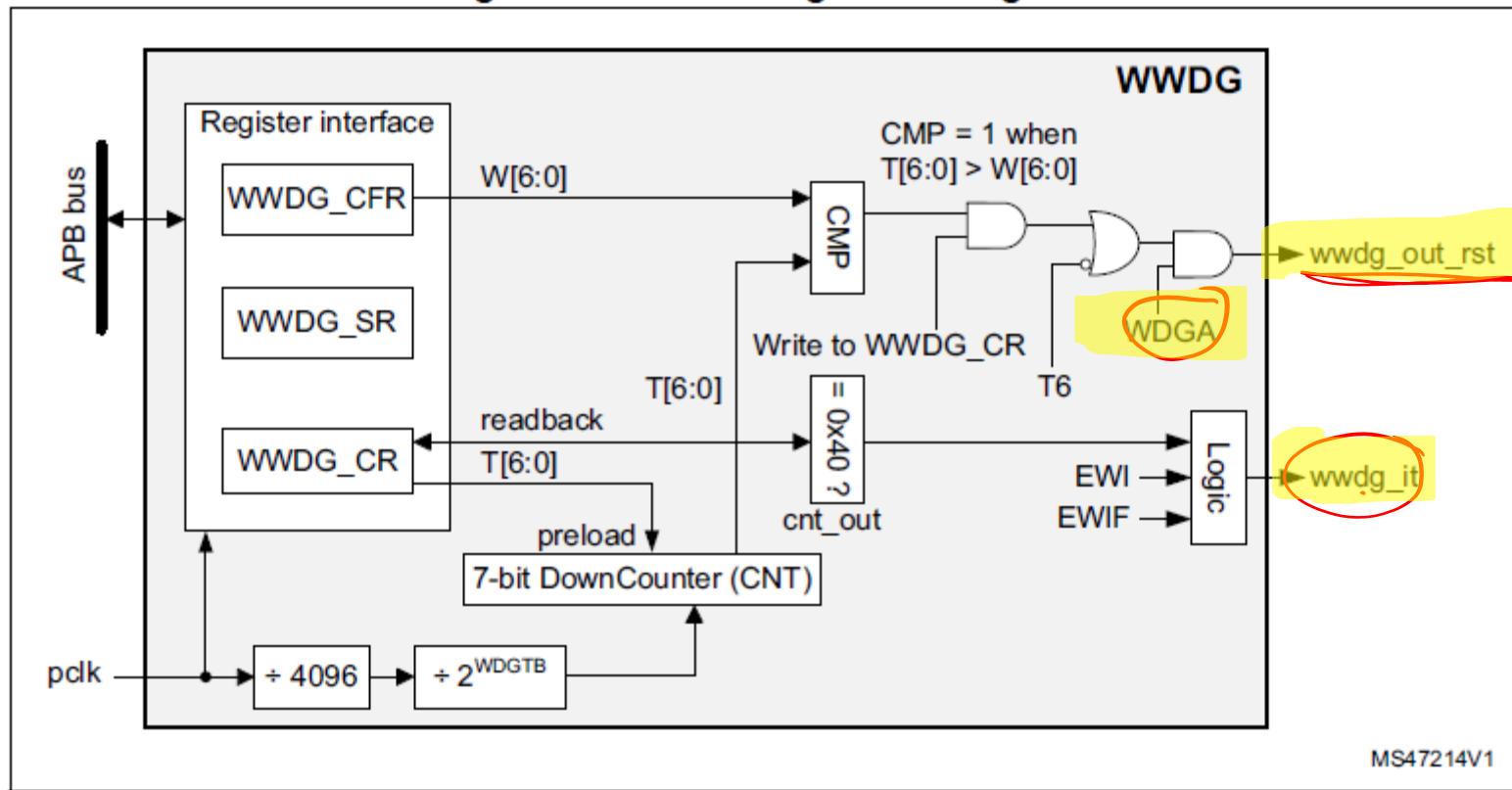
Search (Ctrl+F)

Watchdog Clocking

- IWDG counter clock prescaler 4
- IWDG window value 4095
- IWDG down-counter reload value 4095

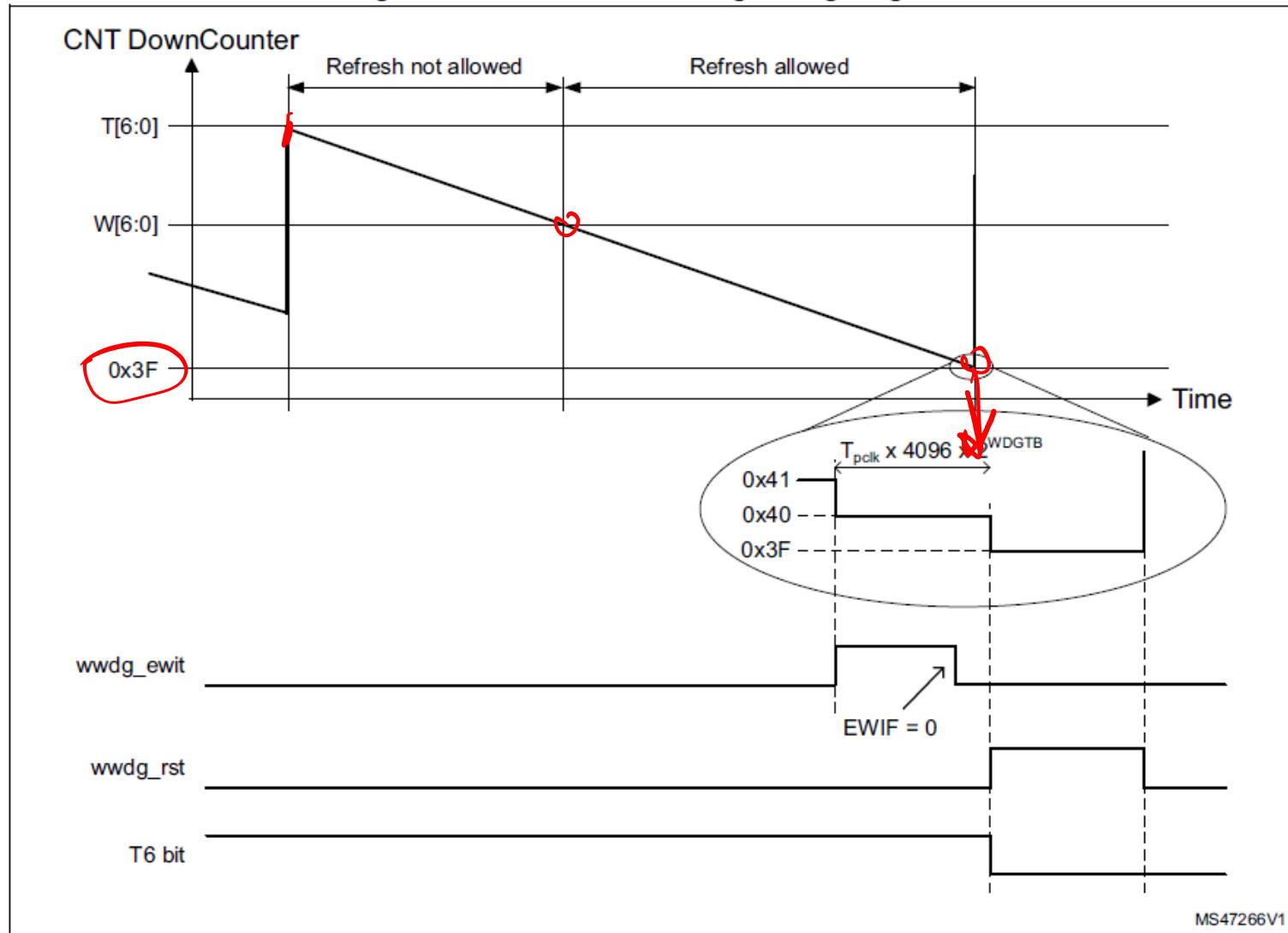
WWDG – Windowed Watchdog

Figure 660. Watchdog block diagram



WWDG – Windowed Watchdog

Figure 661. Window watchdog timing diagram



Nastavitev v CubeMX

The screenshot shows the CubeMX software interface for pinout and configuration. The left sidebar lists categories like System Core, Analog, Timers, Connectivity, and Multimedia, with WWDG selected. The main area is titled 'Clock Configuration' for the WWDG module. It includes sections for Mode (Activated), Configuration (Reset Configuration, Parameter Settings, User Constants, NVIC Settings), and parameters for Watchdog Clocking (prescaler 1, window value 64, free-running downcount 64) and Watchdog Interrupt (Early wakeup interrupt disabled).

Pinout & Configuration

Clock Configuration

WWDG Mode and Configuration

Mode

Activated

Configuration

Reset Configuration

Parameter Settings

User Constants

NVIC Settings

Configure the below parameters :

Search (Ctrl+F)

Watchdog Clocking

WWDG counter clock prescaler: 1

WWDG window value: 64

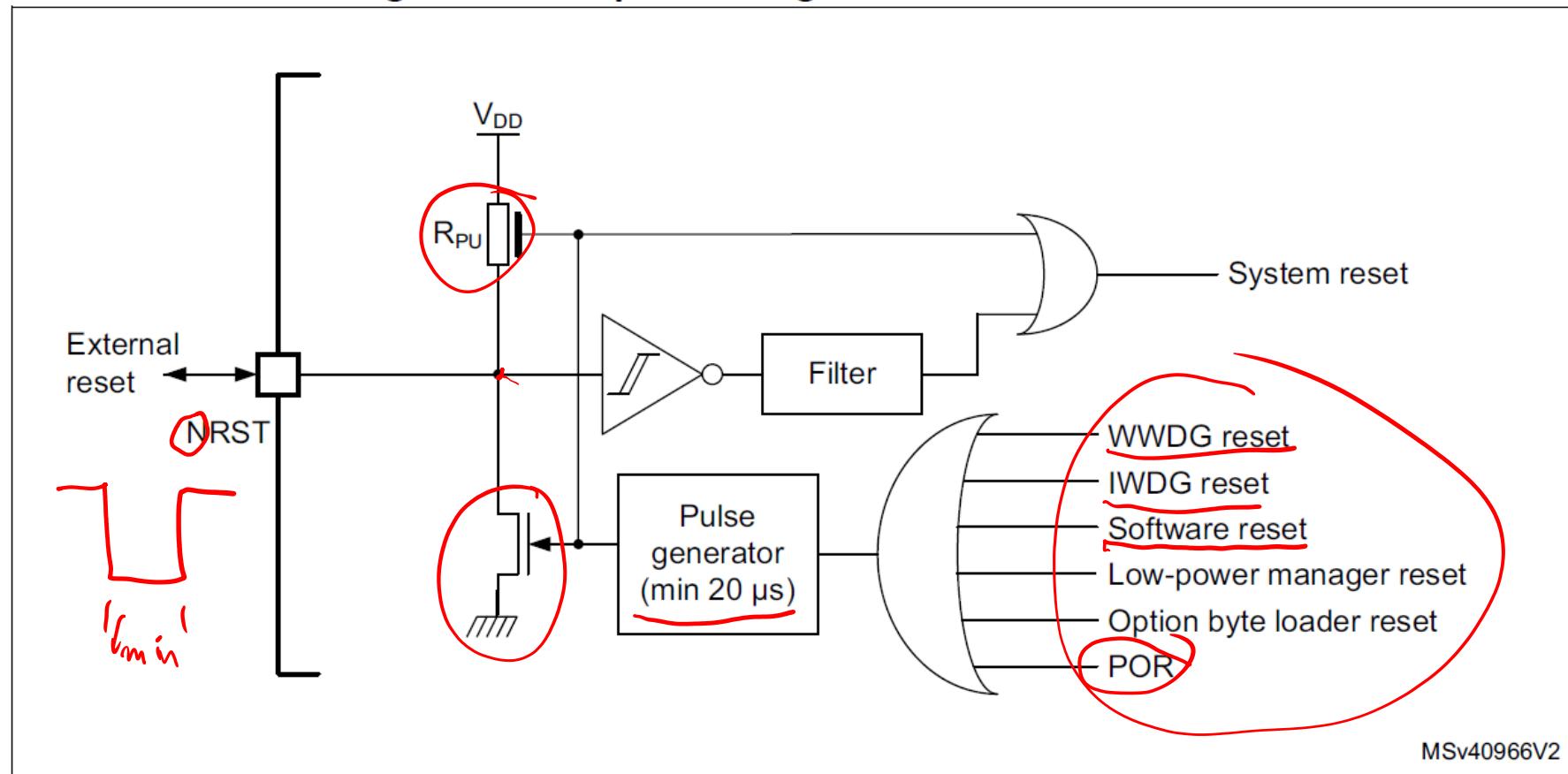
WWDG free-running downcount: 64

Watchdog Interrupt

Early wakeup interrupt: Disable

Reset logika pri STM32

Figure 16. Simplified diagram of the reset circuit



RCC_CSR – Register o informaciji reset vira

INFO O NACINU SNRTI V PREJŠNJEM
7.4.28 Control/status register (RCC_CSR) ČIVLJENJU:)
Address: 0x84

7.4.28 Control/status register (RCC_CSR)

Address: 0x94

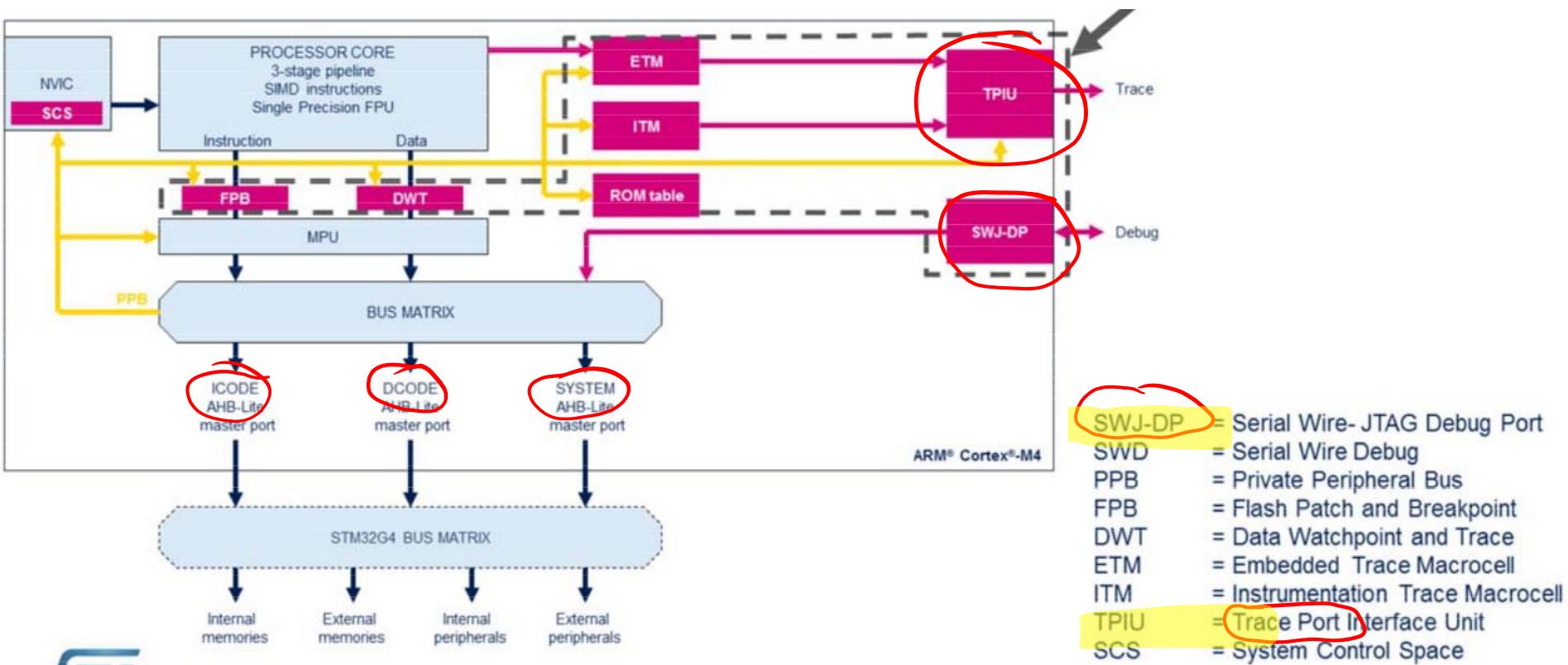
Reset value: 0x0C00 0000

Reset by system Reset, except reset flags by power Reset only.

Access: $0 \leq \text{wait state} \leq 3$, word, half-word and byte access

Wait states are inserted in case of successive accesses to this register.

Programiranje in razhroščevanje



SWJ-DP (Serial Wire-JTAG Debug Port)

2-wire SWD – Serial Wire Debug

- Invazivno razhroščevanje

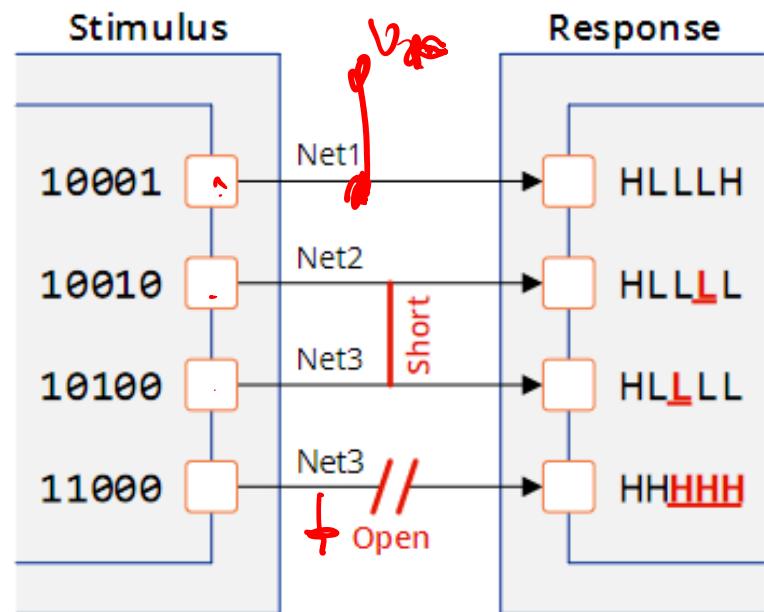
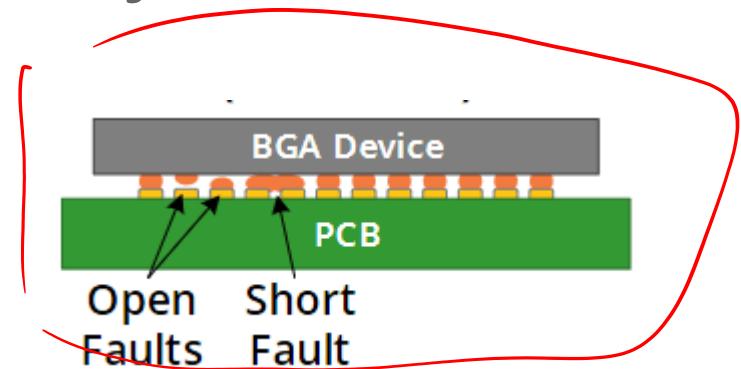
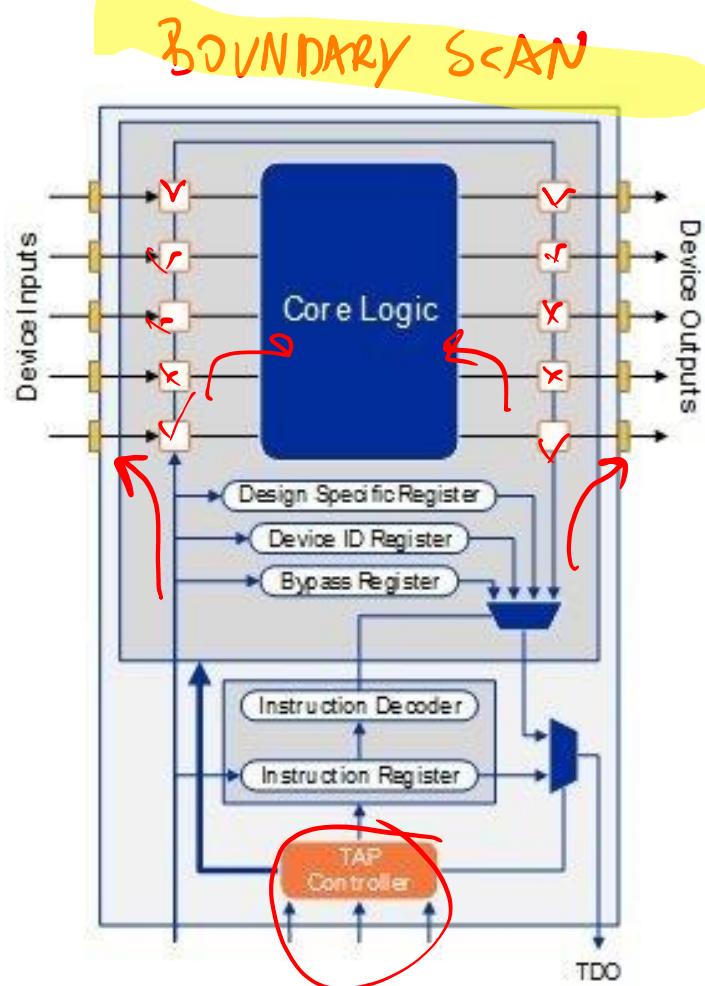
Rnout	PA13	PA14
SWD	SWDIO	SWCLK
JTAG	JTMS	JTCK
SWO		
TRACE PORT		

5-wire JTAG - Joint Test Action Group

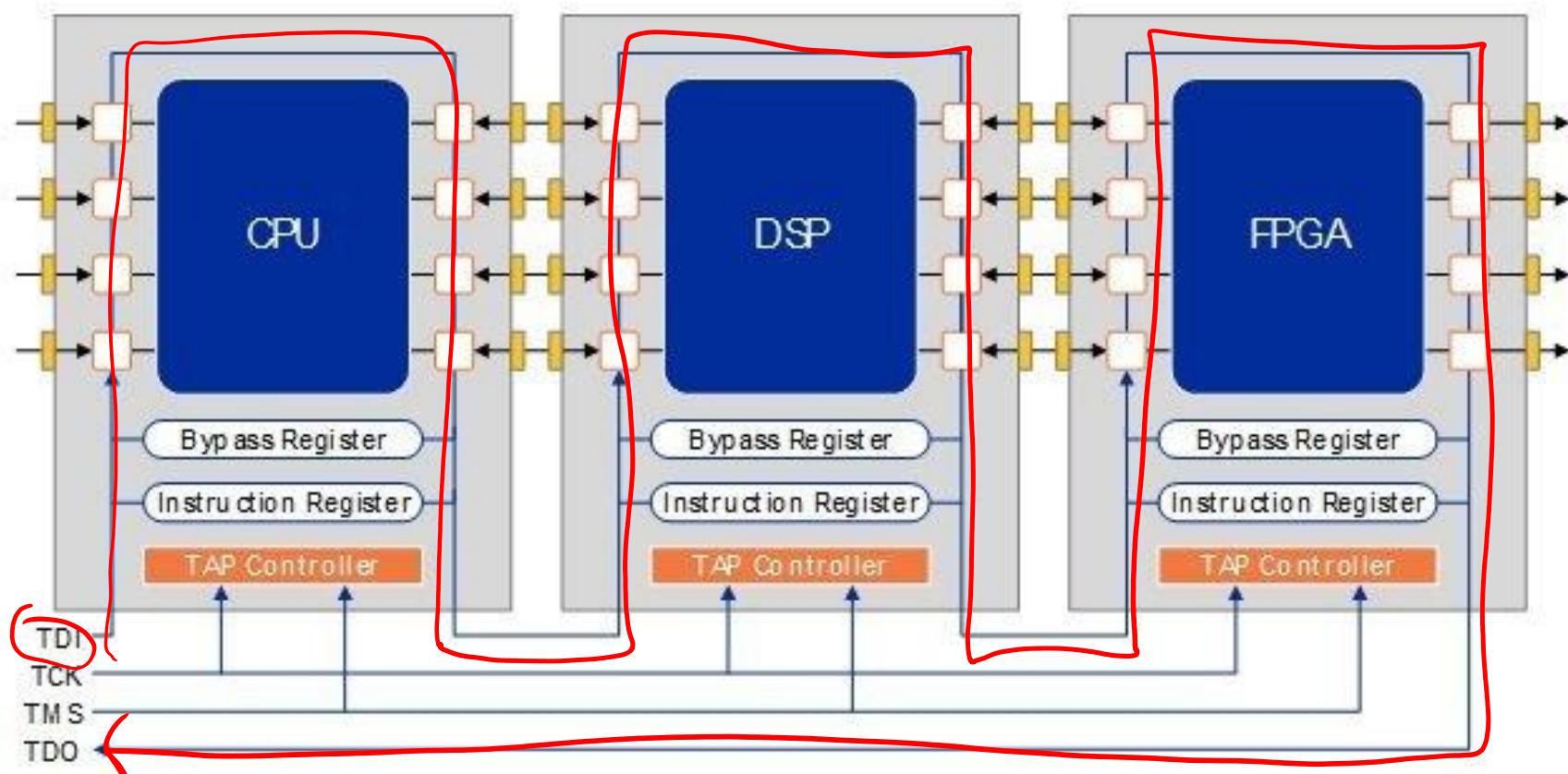
- Standard IEEE Std.-1149.1
- Invazivno razhroščevanje
- Preverjanje povezav

Rnout	PA13	PA14	PA15	FB3	FB4
SWD	SWDIO	SWCLK			
JTAG	JTMS	JTCK	JTDI	JTDO	JTRST
SWO				TRACESWO	
TRACE PORT					

Preverjanje povezav na vezju z JTAG



Zaporedna vezava JTAG v verigo - Daisy chain



TP – Trace Port

1-wire trace port

- Serial Wire Output (SWO)
- Neinvazivno razhroščevanje

Sinhroni 5-wire trace port

- clock + 1, 2 ali 4 podatkovne linije
- Neinvazivno razhroščevanje
- Najhitrejši prenos podatkov

Pinout	PA13	PA14	PA15	PB3	PB4	PE2	PE3	PE4	PE5	PE6
SWD	SWDIO	SWCLK								
JTAG	JTMS	JTCK	JTDI	JTDO	JTRST					
SWO				TRACESWO						
TRACE PORT						TRACECK	TRACED0	TRACED1	TRACED2	TRACED2

+

STLINK



Vmesniki

JTAG

SWD

USB naprave

ST-LINK

VCP

UDP

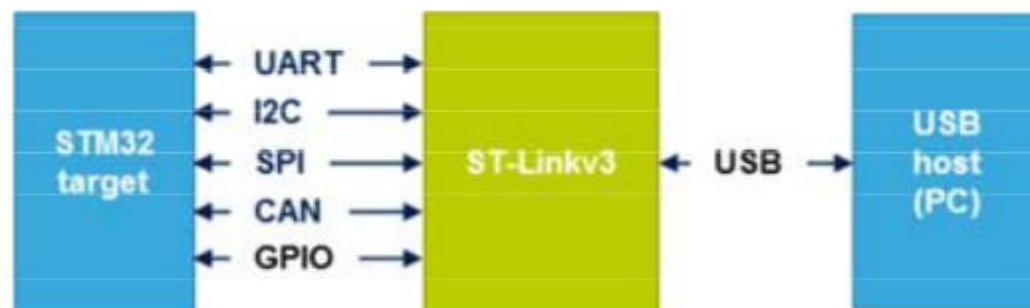
FLASH DRIVE

STLINK v3

- Performance enhancement

	ST-Link V2 (KHz)	ST-Link V3 (KHz)
SWD	4000	24000
JTAG	9000	21333

- Bridge feature overview

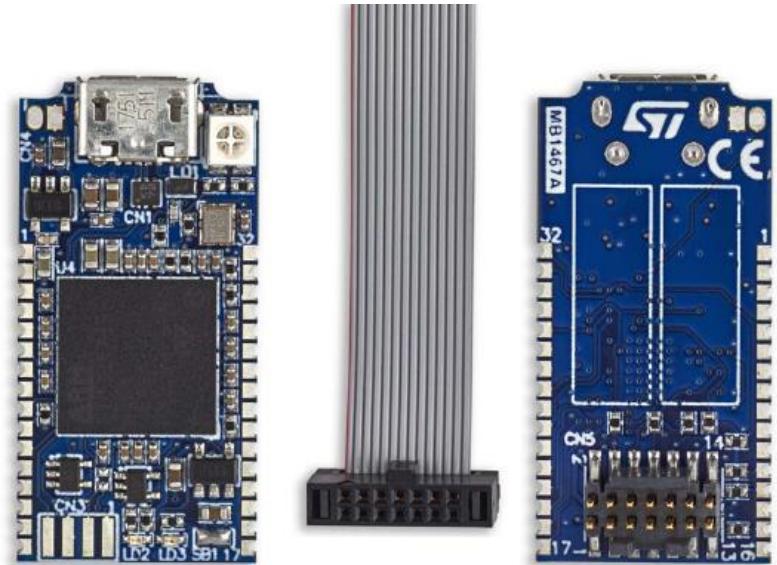


STLINK v3

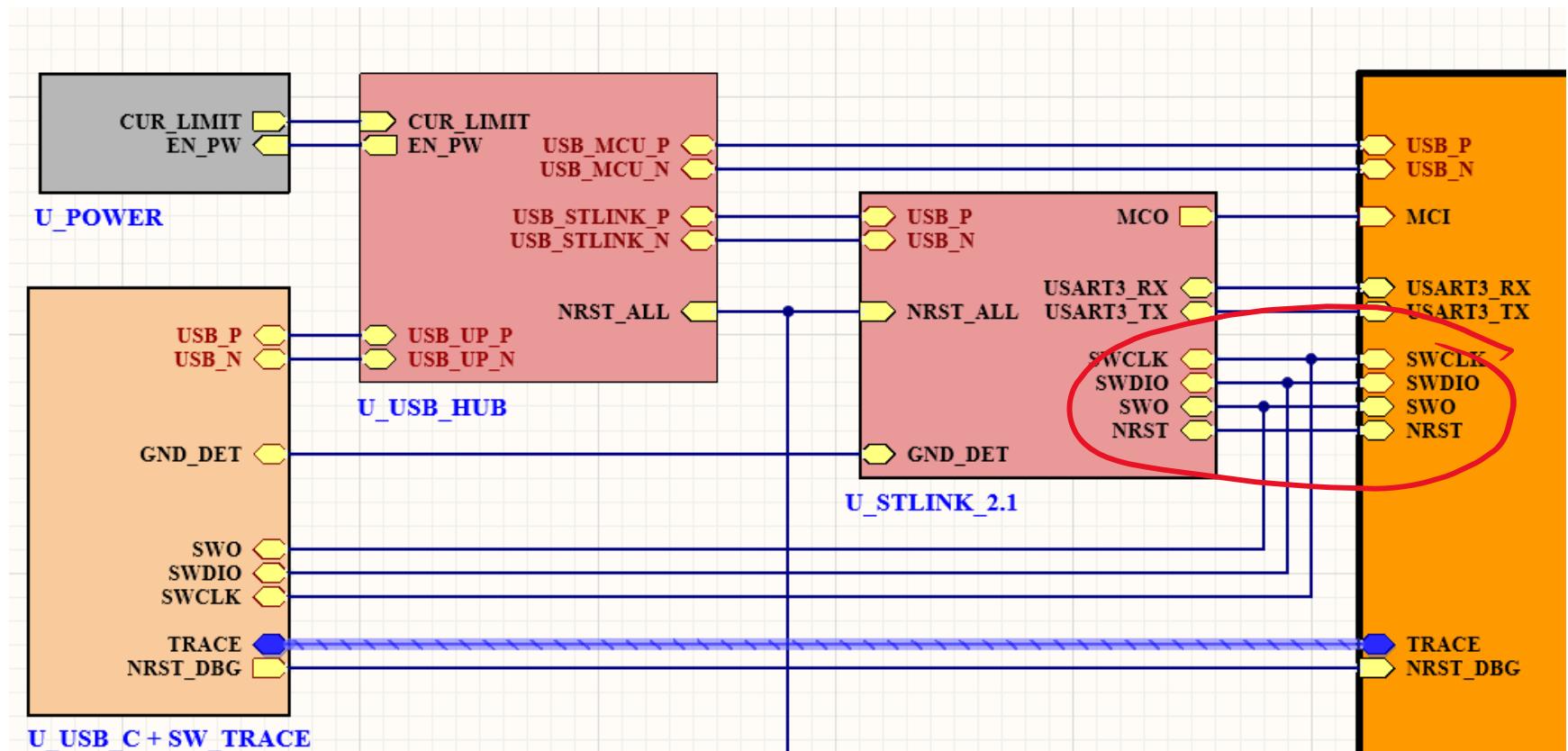
STLINK-V3SET



STLINK-V3MODS / V3MINI

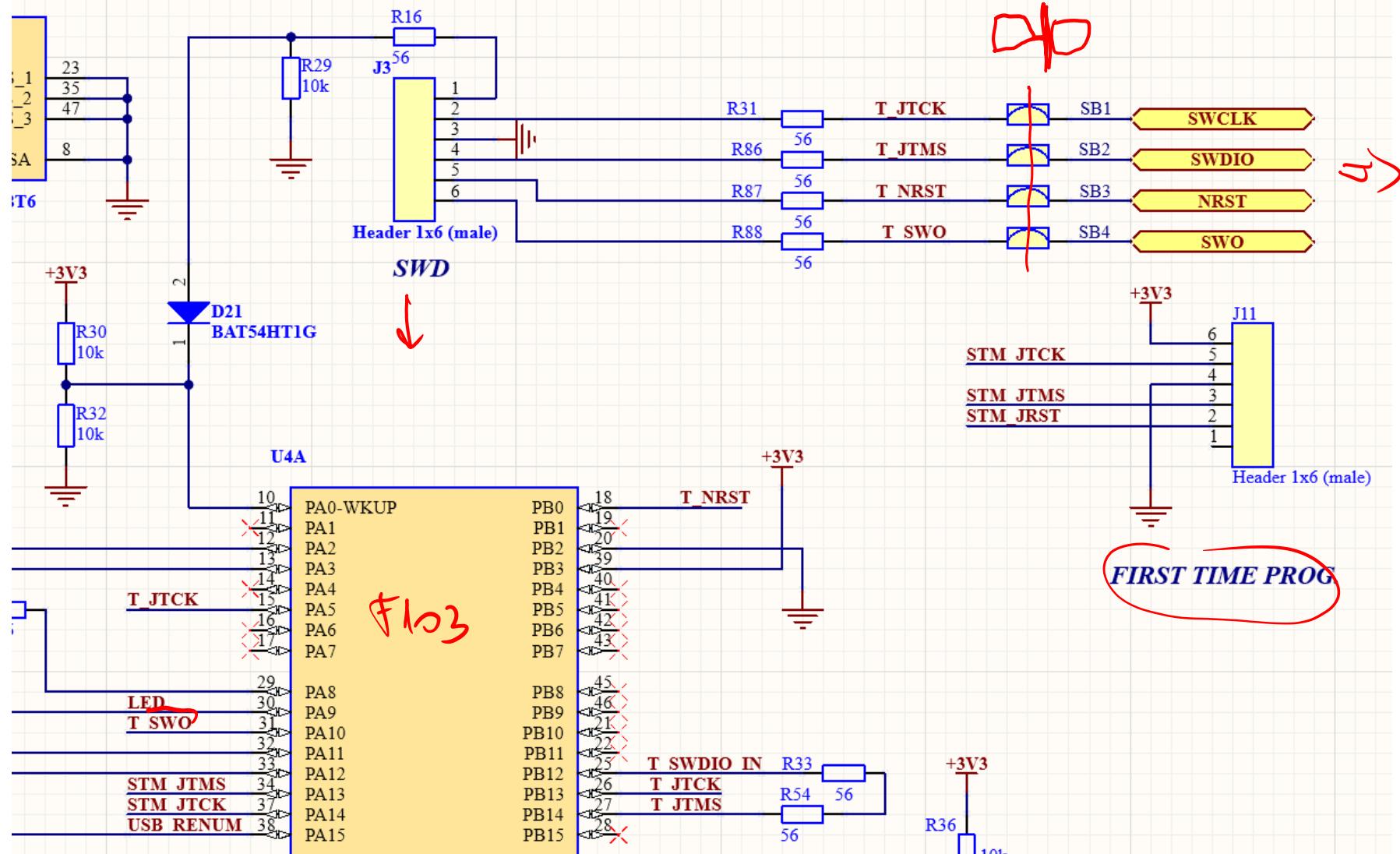


Miško 3



ST-LINK v2.1: SWD + SWO

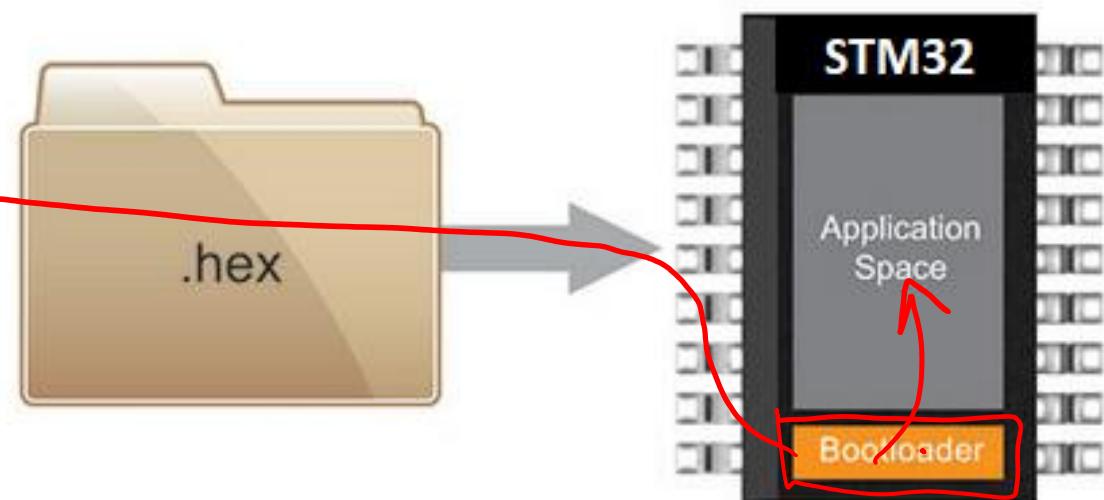
SOLD BR BLD 13



Zagonski nalagalnik - bootloader

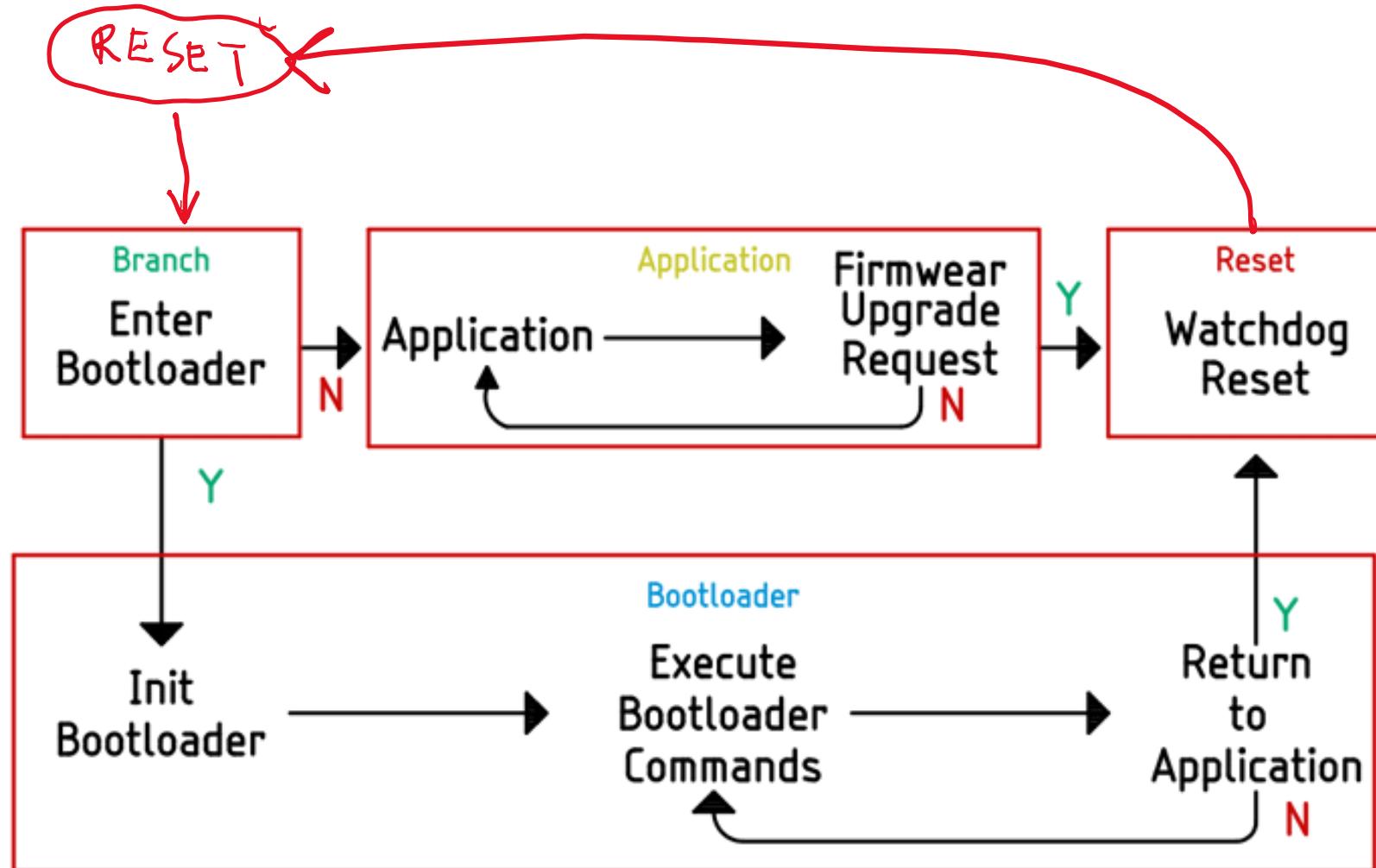
From:

Ethernet, CAN, USB, etc



Bootloader programmed
into Flash memory

Umetitev zagonskega nalagalnika



Tovarniško vgrajeni zagonski nalagalniki

Table 3. Embedded bootloaders

STM32 Series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
F1	STM32F10xxx	Low-density USART1	NA	NA	USART (V2.2)
		Medium-density USART1	NA	NA	USART (V2.2)
		High-density USART1	NA	NA	USART (V2.2)
		Medium-density value line USART1	0x10	0x1FFFF7D6	USART (V2.2)
		High-density value line USART1	0x10	0x1FFFF7D6	USART (V2.2)
G4	STM32G431xx/441xx	USART1/USART2/USART3 I2C2/I2C3 SPI1/SPI2 DFU (USB device FS)	0xD4	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2)
	STM32G47xxx/48xxx	USART1/USART2/USART3 I2C2/I2C3/I2C4 SPI1/SPI2 DFU (USB device FS)	0xD5	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2)
	STM32G491xx/4A1xx	USART1/USART2/USART3 I2C2/I2C3 SPI1/SPI2 DFU (USB device FS)	0xD2	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2)

Organizacija pomnilnika pri STM32G4

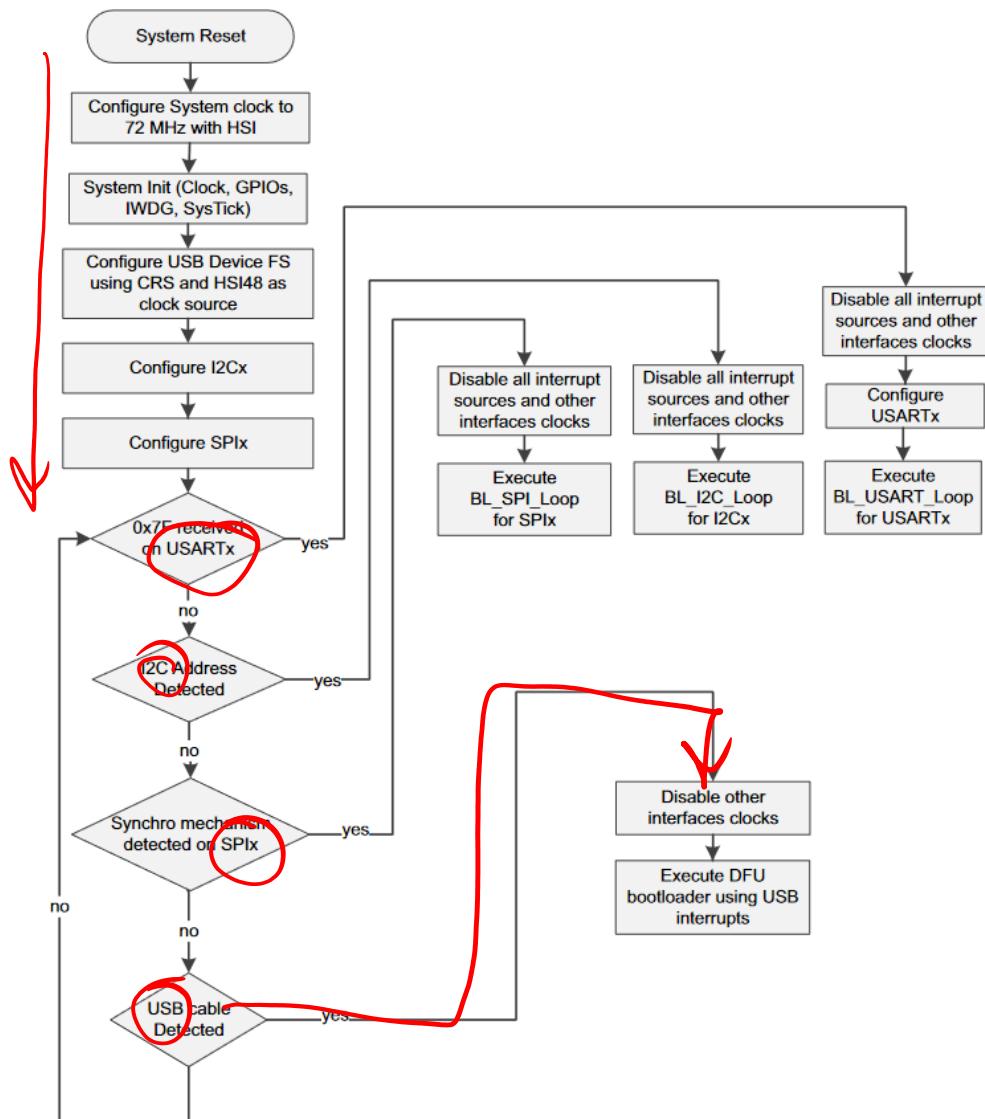
Table 8. Flash module - 512/256/128 KB single bank organization (128 bits read width)

Flash area	Flash memory addresses		Size (bytes)	Name
Main memory (512/256/128 KB)	0x0800 0000 - 0x0800 0FFF	4 K	Page 0	
	0x0800 1000 - 0x0800 1FFF	4 K	Page 1	
	0x0800 2000 - 0x0800 2FFF	4 K	Page 2	
	-	-	-	
	-	-	-	
	-	-	-	
	-	-	-	
	-	-	-	
	-	-	-	
	0x0807 F000 - 0x0807 FFFF	4 K	Page 127	
Information block	Bank 1	0x1FF 0000 - 0x1FF 6FFF	28 K	System memory
	Bank 2	0x1FF 8000 - 0x1FF EFFF	28 K	
	Bank 1	0x1FF 7000 - 0x1FF 73FF	1 K	
	Bank 1	0x1FF 7800 - 0x1FF 782F	48	Option bytes
	Bank 2	0x1FF F800 - 0x1FF F82F	48	

NASTAVITVE

BOOTLOADER

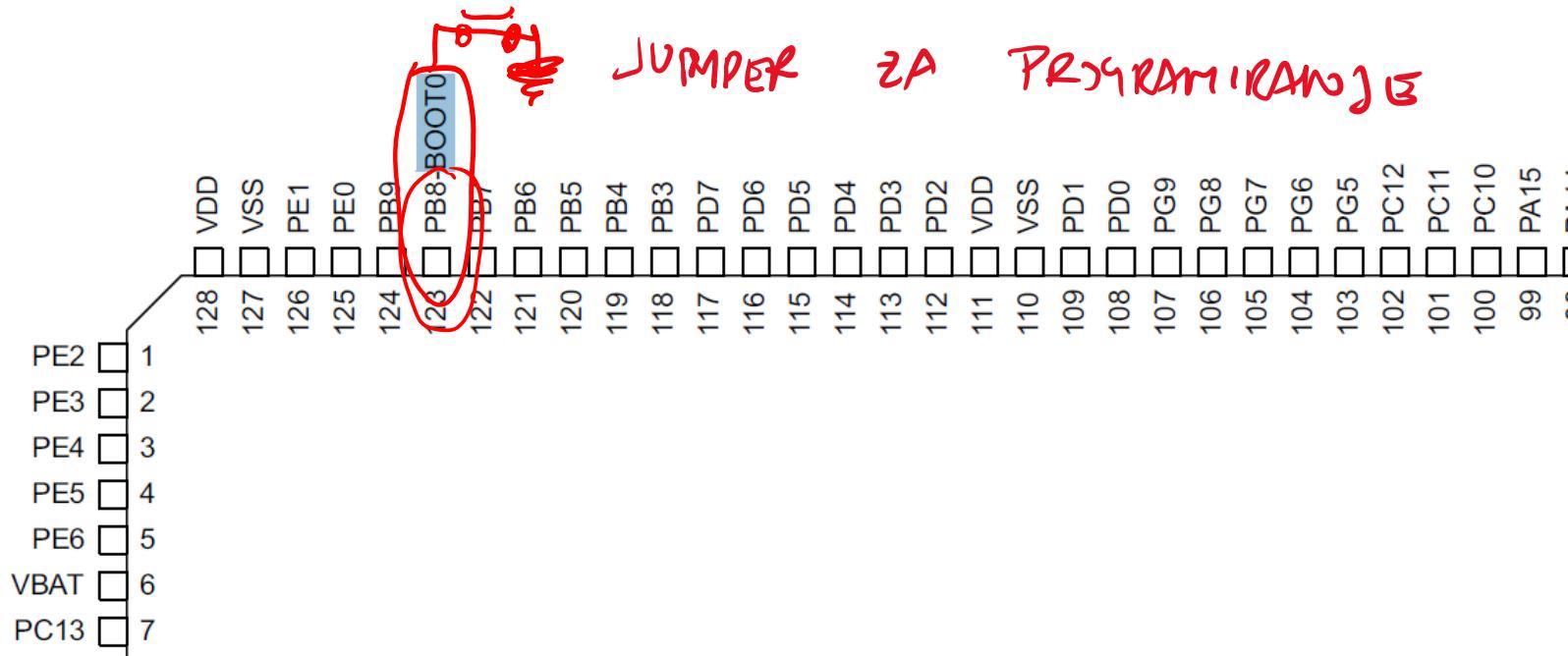
Algoritem zagosnkega nalagalnika pri STM32G4



Zunanji BOOT0 priključek

Pri MiŠKo 3 je onemogočen!

Figure 10. STM32G474xB/xC/xE LQFP128 pinout



Option bytes, fuses

- Opcijski byti, varovalke

Table 31. Option byte organization

Address	[63:56]	[55:48]	[47:40]	[39:32]	[31:24]	[23:16]	[15:8]	[7:0]
1FFF7800	USER OPT			RDP	USER OPT			RDP
1FFF7808	Unused		Unused and PCROP1_STRT[13:0]			Unused		Unused and PCROP1_STRT[13:0]
1FFF7810	PCROP_RDP and Unused		Unused and PCROP1_END[13:0]			PCROP_RDP and Unused		Unused and PCROP1_END[13:0]
1FFF7818	Unused	WRP1A _END [5:0]	Unused	WRP1A _STRT [5:0]	Unused	WRP1A_ END [5:0]	Unused	WRP1A _STRT [5:0]
1FFF7820	Unused	WRP2A _END [5:0]	Unused	WRP2A _STRT [5:0]	Unused	WRP2A_ END [5:0]	Unused	WRP2A _STRT [5:0]
1FFF7828	Unused	BOOT_ LOCK	Unused	SEC_ SIZE1	Unused	BOOT_ LOCK	Unused	SEC_ SIZE1

Zaščita pomnilnikov

Area	Protection level (RDP)	Access rights when Boot in User Flash memory	Access rights when Boot from RAM or from bootloader or Debug Access detected
Main Flash memory	1	R/W/E	No Access
	2	R/W/E	NA, only boot in user flash memory is allowed
System Flash memory (Boot loader)	1	R	R
	2	R	NA, only boot in user flash memory is allowed
Option bytes	1	R/W/E	R/W/E
	2	R	NA, only boot in user flash memory is allowed
Backup registers	1	R/W	No Access
	2	R/W	NA, only boot in user flash memory is allowed
CCM SRAM	1	R/W	No Access
	2	R/W	NA, only boot in user flash memory is allowed
OTP	1	R/W	No Access
	2	R/W	NA, only boot in user flash memory is allowed

Nastavite v STM32 Cube Programmer

Option bytes		
IWDG_STOP	<input checked="" type="checkbox"/>	Unchecked : Freeze IWDG counter in stop mode Checked : IWDG counter active in stop mode
IWDG_STDBY	<input checked="" type="checkbox"/>	Unchecked : Freeze IWDG counter in standby mode Checked : IWDG counter active in standby mode
WWDG_SW	<input checked="" type="checkbox"/>	Unchecked : Hardware window watchdog Checked : Software window watchdog
BFB2	<input type="checkbox"/>	Unchecked : Dual bank boot disable Checked : Dual-bank boot enable
DBANK	<input checked="" type="checkbox"/>	Unchecked : Single bank mode with 128 bits data read width Checked : Dual bank mode with 64 bits data
nBOOT1	<input checked="" type="checkbox"/>	Unchecked : Boot from Flash if BOOT0 = 0, otherwise Embedded SRAM1 Checked : Boot from Flash if BOOT0 = 0, otherwise system memory SRAM1 and CCM SRAM parity check enable
SRAM_PE	<input checked="" type="checkbox"/>	Unchecked : SRAM1 and CCM SRAM parity check enable Checked : SRAM1 and CCM SRAM parity check disable CCM SRAM Erase when system reset
CCMSRAM_RST	<input checked="" type="checkbox"/>	Unchecked : CCM SRAM erased when a system reset occurs Checked : CCM SRAM is not erased when a system reset occurs Software BOOT0
nSWBOOT0	<input type="checkbox"/>	Unchecked : BOOT0 taken from the option bit nBOOT0 Checked : BOOT0 taken from PBs BOOT0 pin This option bit sets the BOOT0 value only when nSWBOOT0=0
nBOOT0	<input checked="" type="checkbox"/>	Unchecked : nBOOT0 = 0 Checked : nBOOT0 = 1 0 : Reserved 1 : Reset Input only: a low level on the NRST pin generates system reset, internal RESET not propagated to the NSRT pin 2 : GPIO: standard GPIO pad functionality, only internal RESET possible 3 : Bidirectional reset: NRST pin configured in reset input/output mode (legacy mode) Internal reset holder enable bit
NRST_MODE	3 ▾	Unchecked : Internal resets are propagated as simple pulse on NRST pin Checked : Internal resets drives NRST pin low until it is seen as low level
IRHEN	<input checked="" type="checkbox"/>	