Osnove mikroprocesorske elektronike

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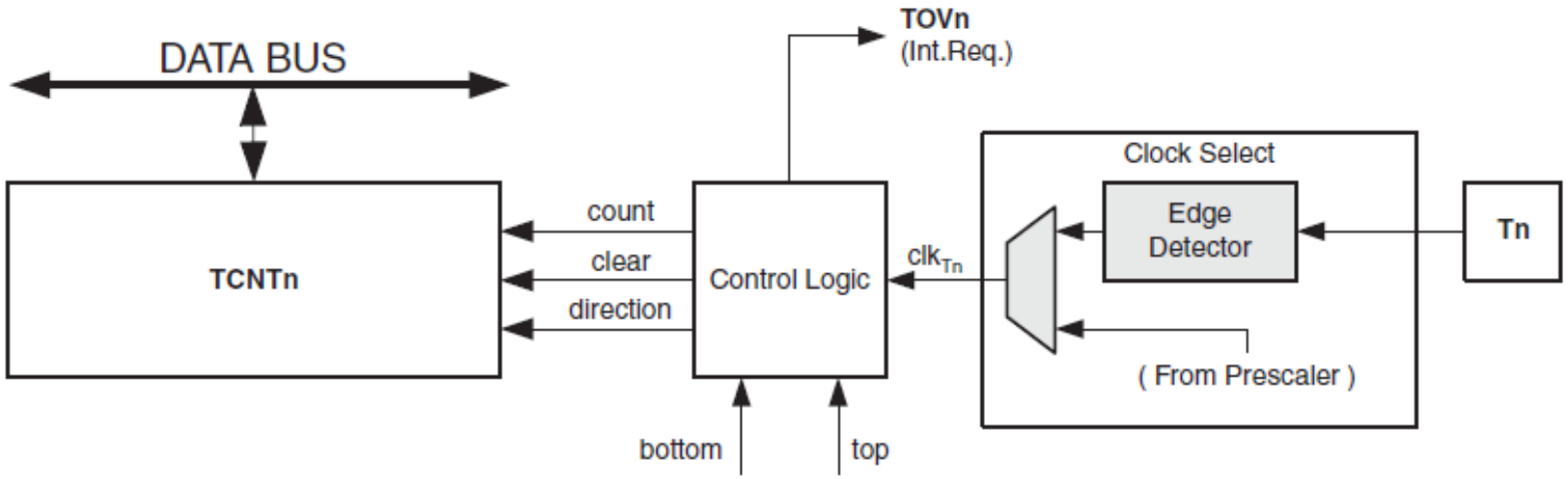
Primeri števcev in časovnikov

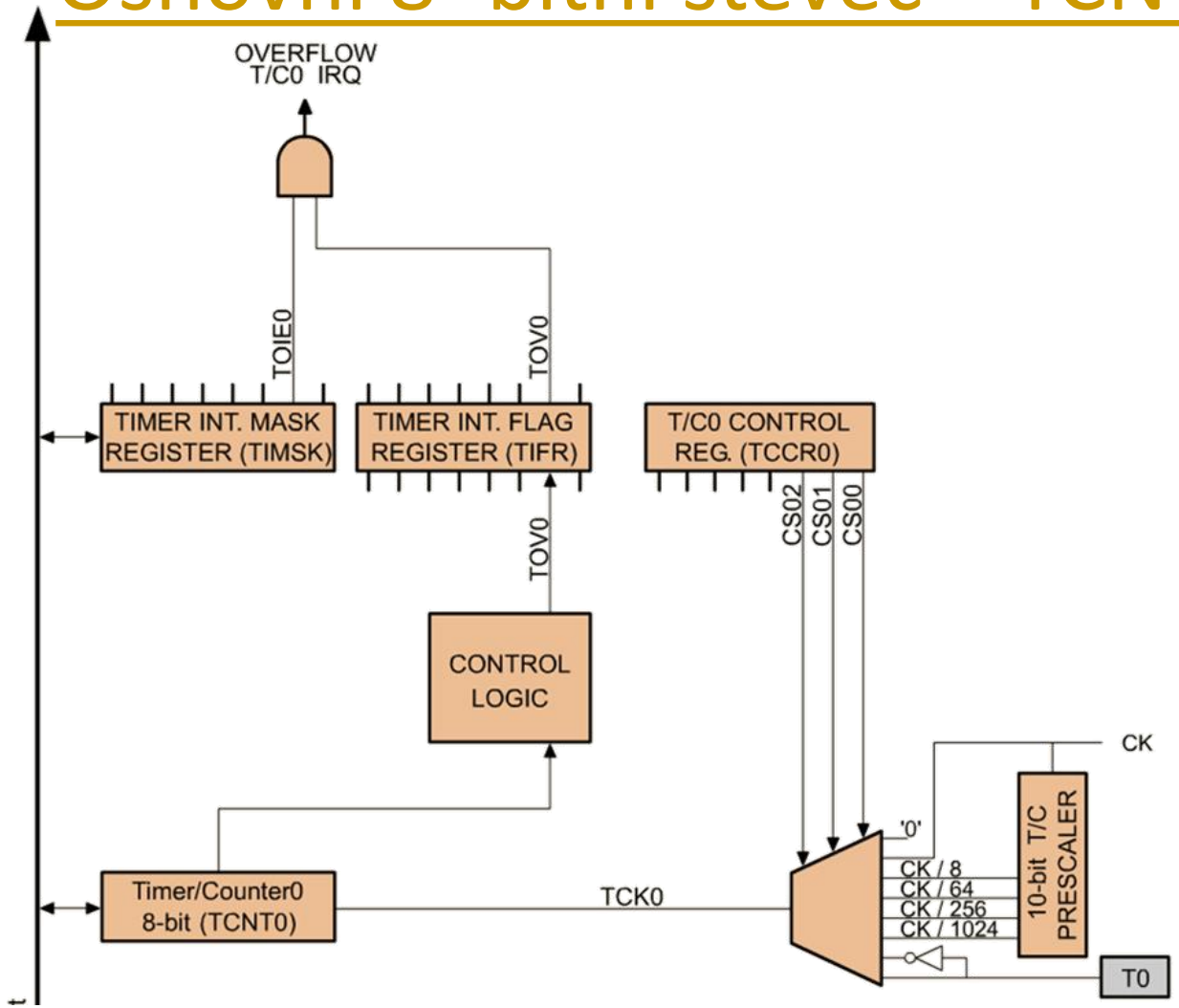
ATmega 328PB

- 8 bitni števec TCNT0
- 16 bitni števci TCNT1, 3 in 4
  - Zajemanje (CAPTURE)
- 8 bitni števec TCNT2
  - Poseben oscilator za vir ure
- Skupno vsem trem
  - 2xPrimerjalnik (COMPARE)
  - Nastavljiva TOP vrednost
  - Ločeni delilniki ure (PRESCALER)
    - Neodvisna nastavitev frekvence štetja
  - Zunanji viri štetja

Osnovni 8- bitni števec – TCNT0



Osnovni 8- bitni števec – TCNT0

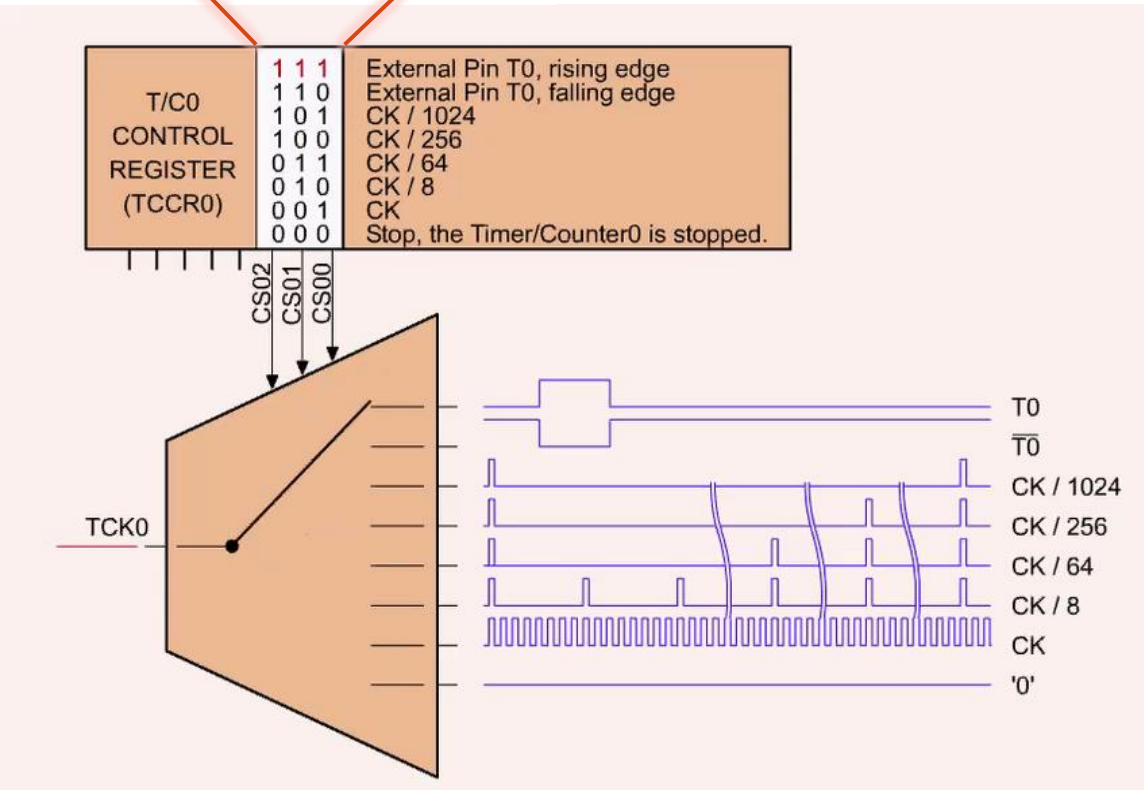


http://paris.fe.uni-lj.si/fileadmin/files/Izobrazevanje/OME/microschematics/ztc.html

Viri ure

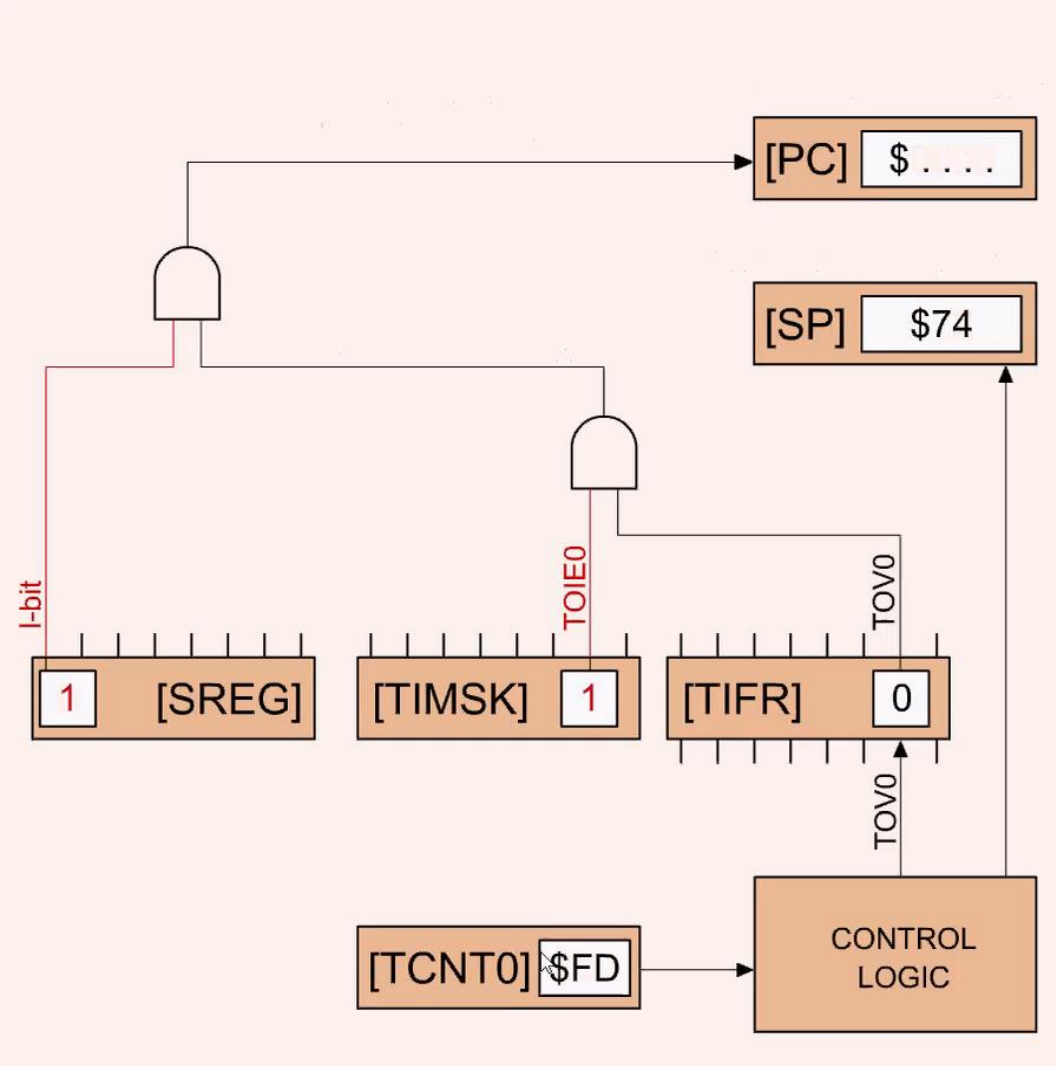
Bit	7	6	5	4	3	2	1	0	
0x25 (0x45)	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Delilnik ure - prescaler



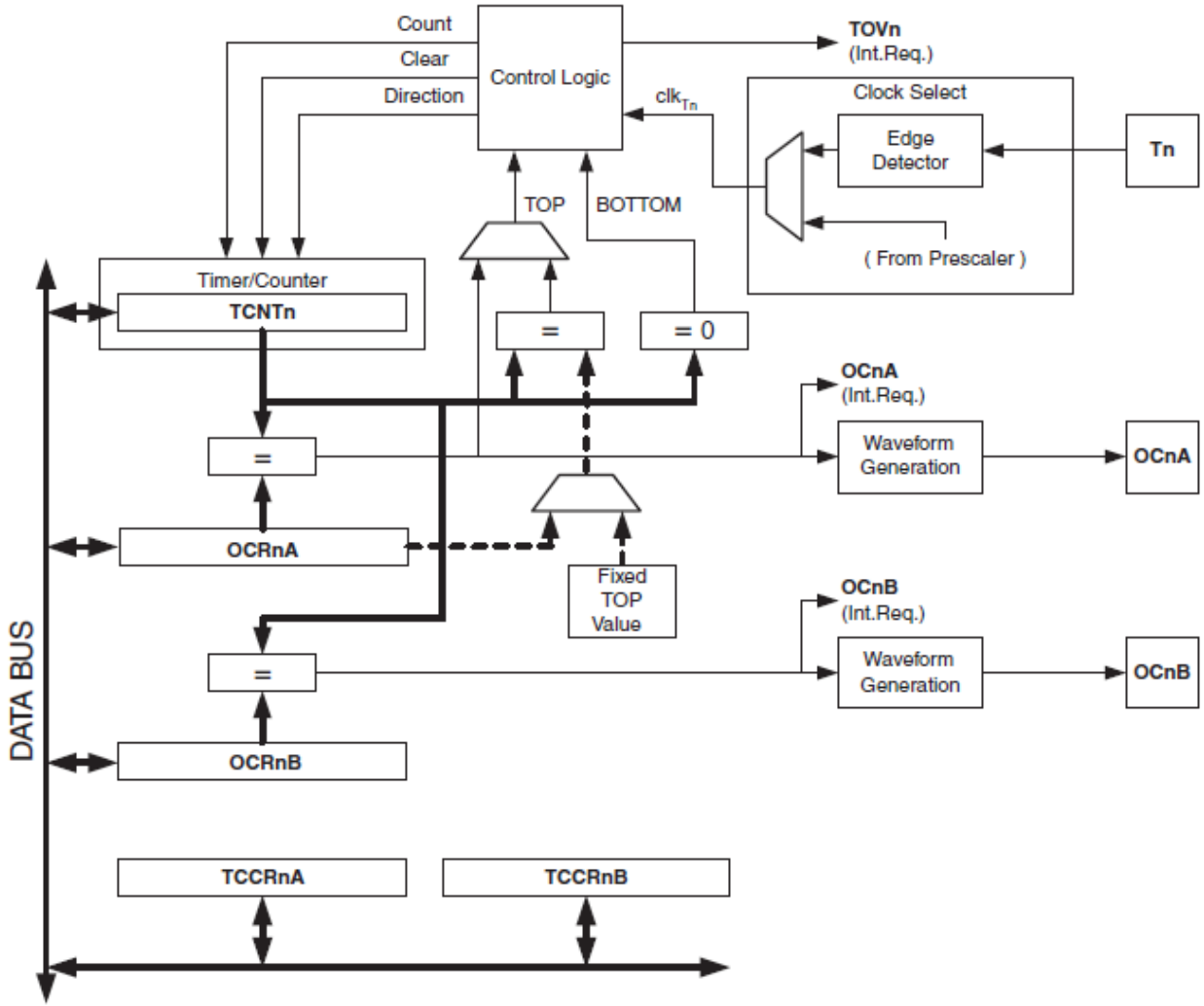
http://paris.fe.uni-lj.si/fileadmin/files/Izobrazevanje/OME/microschematics/ztcpresa.html

Prekinitev ob prelivu



http://paris.fe.uni-lj.si/fileadmin/files/Izobrazevanje/OME/microschematics/zytaovf.html

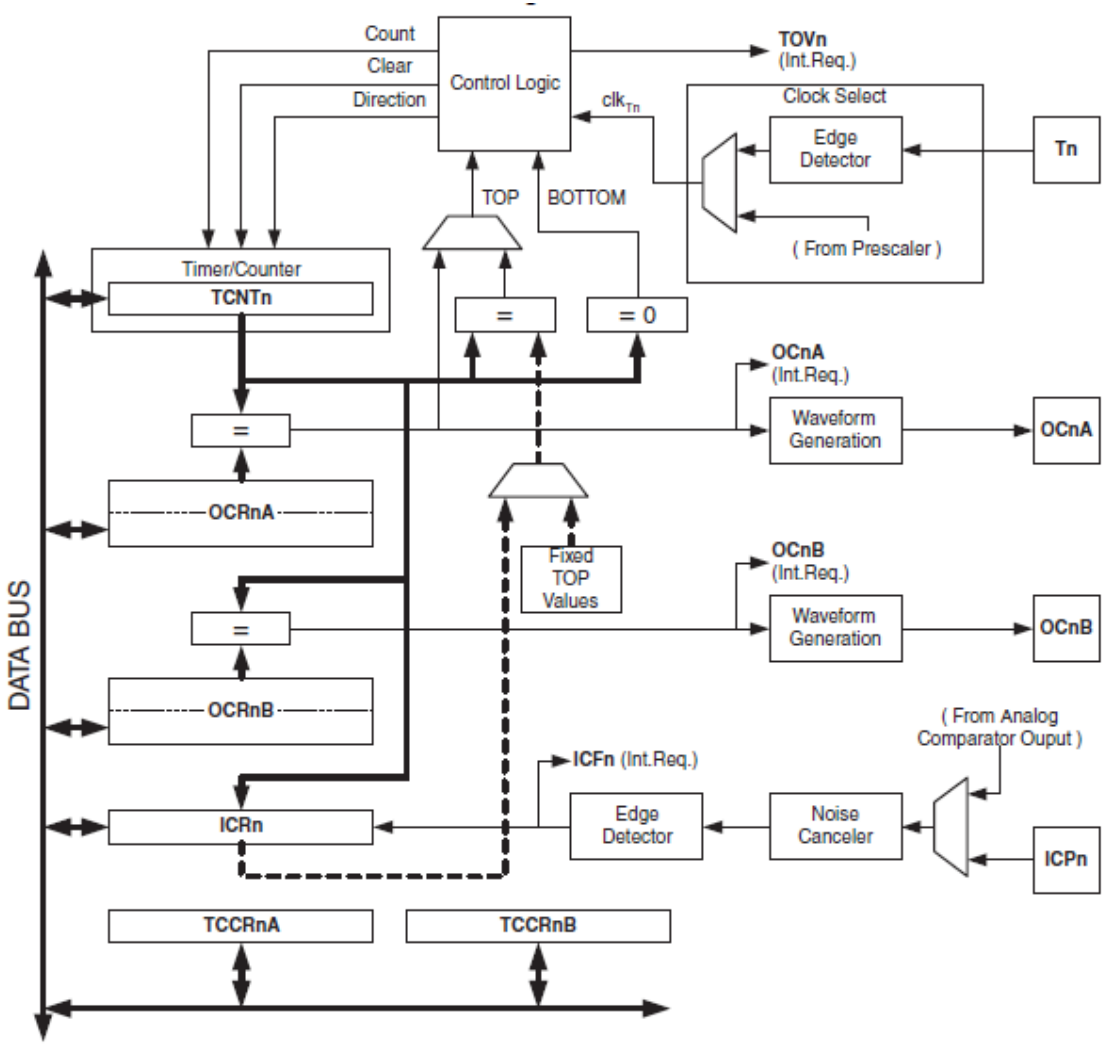
Dodatne funkcije TCNT0



Možnosti hitrega PWM pri 8-bitnem števcu

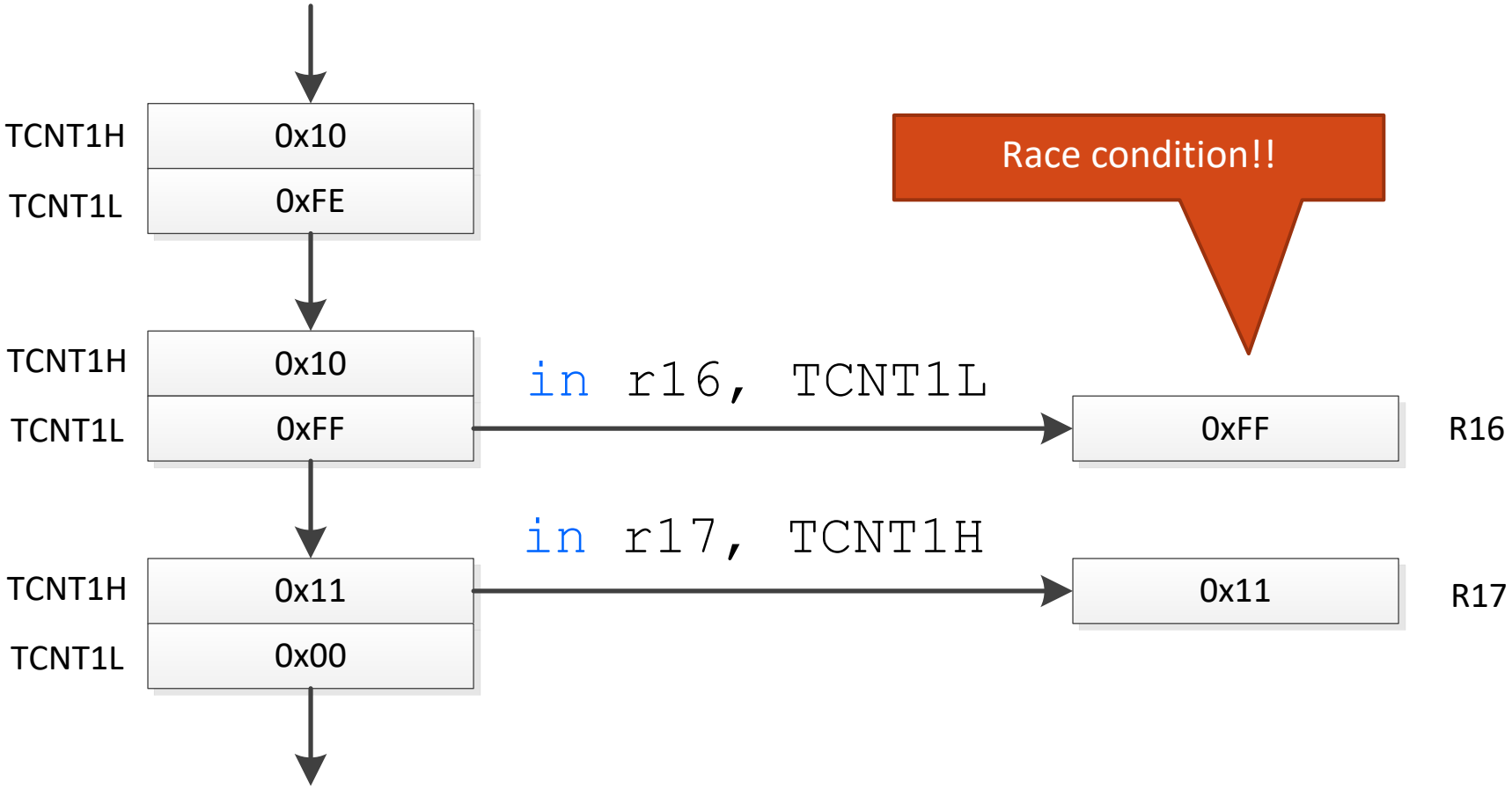
Mode	WGM2	WGM1	WGM0	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on (1)(2)
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

16-bitni števec v AVR – TCNT1, 3 in 4

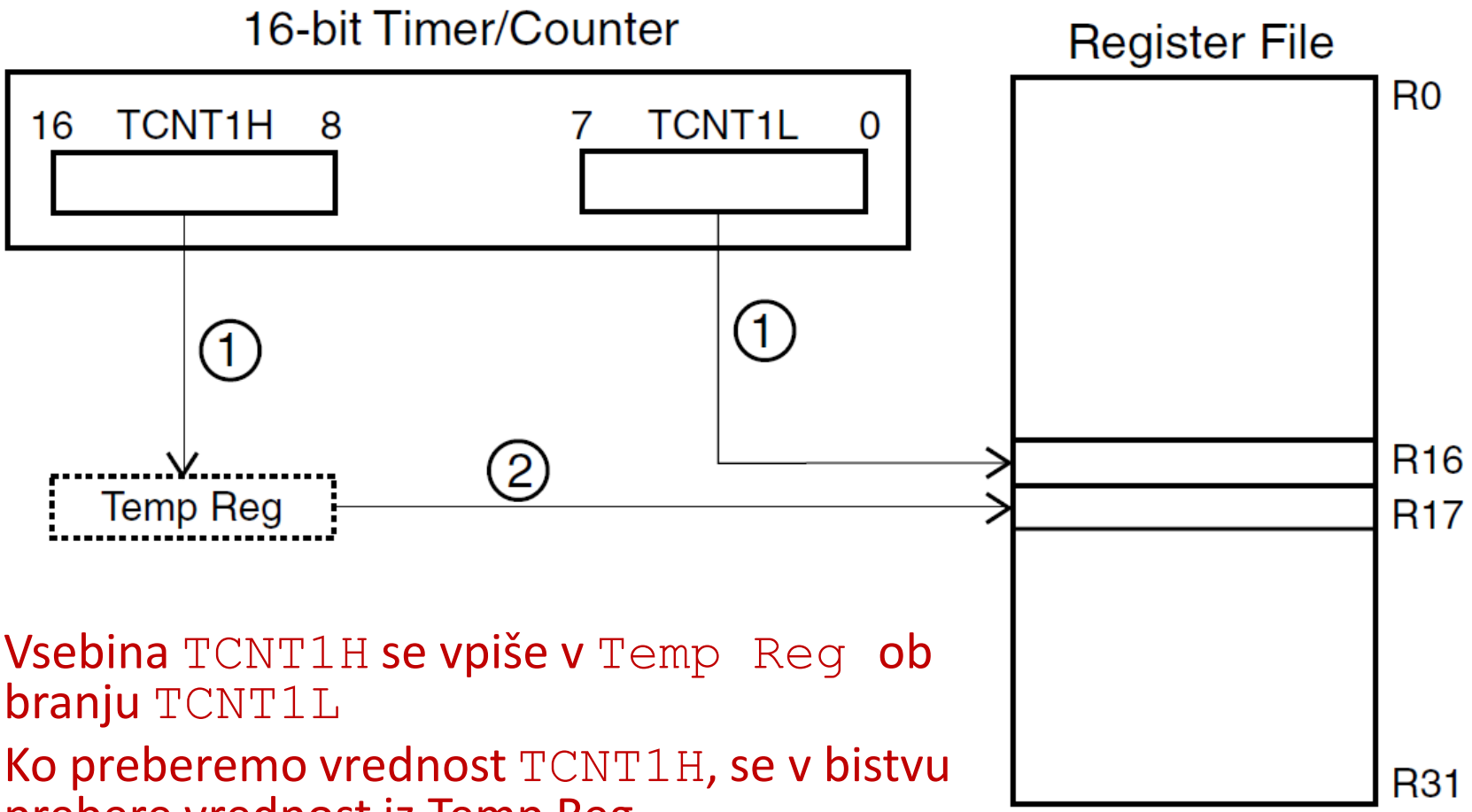


Mode	WGM3	WGM2 (CTC1)(1)	WGM1 (PWM11)(1)	WGM0 (PWM10)(1)	Timer/ Counter Mode of Operation	TOP	Update of OCRnx at	TOV1 Flag Set on
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR4A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR4A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR4A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved	-	-	-
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR4A	BOTTOM	TOP

Branje vrednosti 16-bitnega števca TCNT1

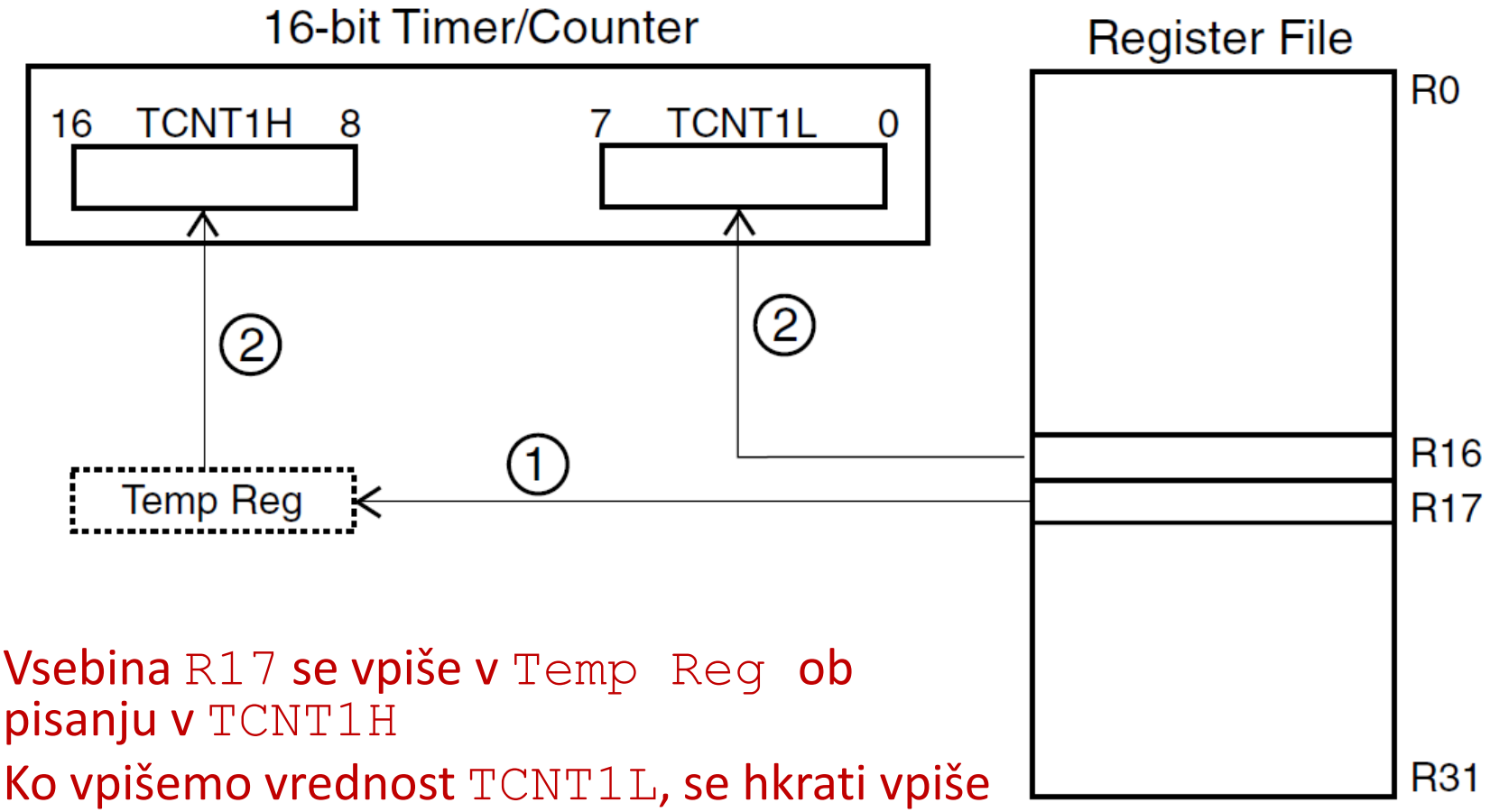


Branje 16-bitnega registra



1. Vsebina `TCNT1H` se vpiše v `Temp Reg` ob branju `TCNT1L`
2. Ko preberemo vrednost `TCNT1H`, se v bistvu prebere vrednost iz Temp Reg

Pisanje v 16-bitni register



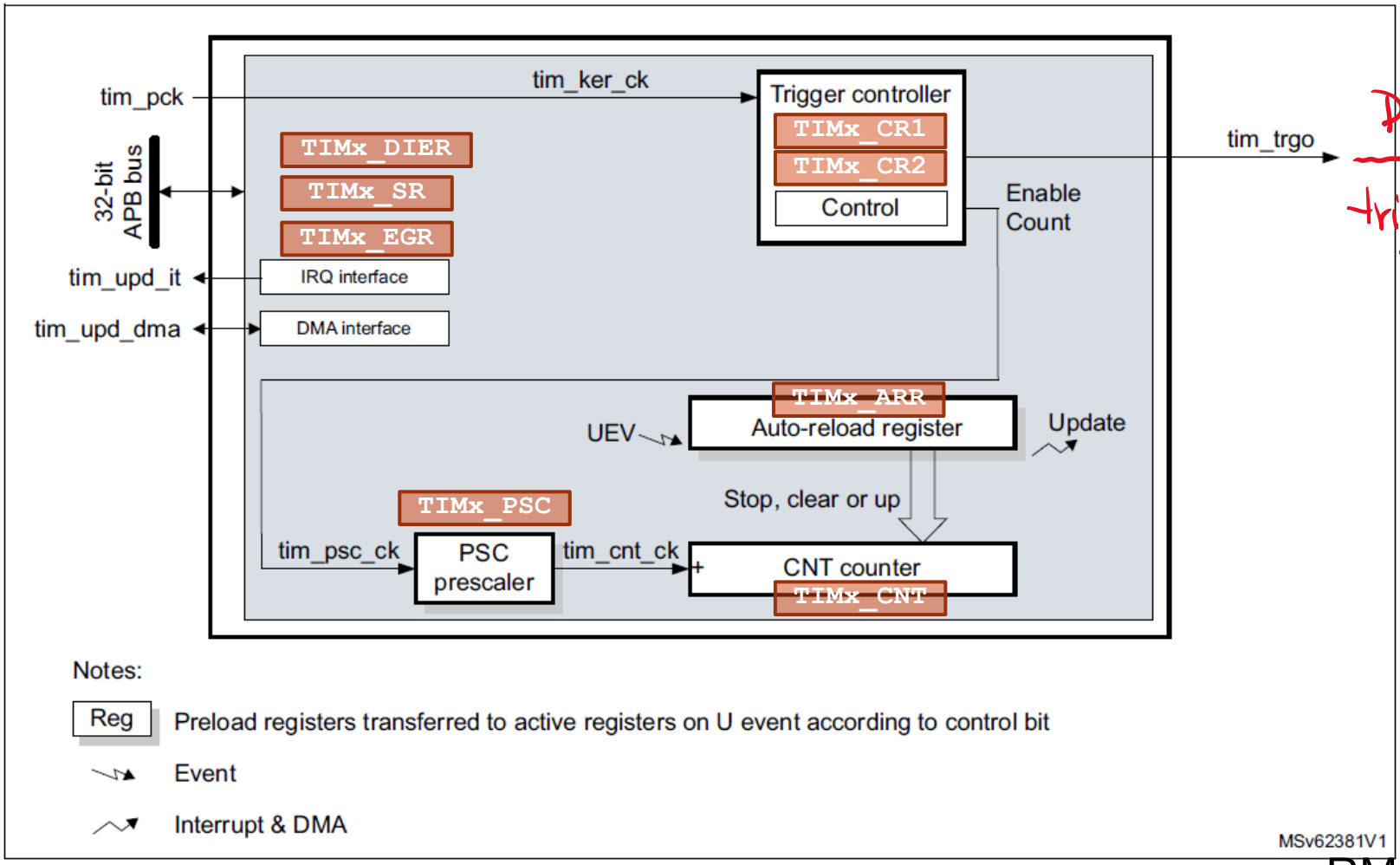
1. Vsebina `R17` se vpiše v `Temp Reg` ob pisanju v `TCNT1H`
2. Ko vpišemo vrednost `TCNT1L`, se hkrati vpiše tudi vrednost iz `Temp Reg` v `TCNT1H`

STM32G4 časovniki in števci

Tip	Timer	Resolucija	Štetje	Prescaler	CCR kanali	Komp. Izhodi
Basic	TIM6, TIM7	16-bit	Gor	1-65536	0	/
General purpose	TIM15, TIM16, TIM17	16-bit	Gor	1-65536	1, 2	1
General purpose	TIM3, TIM4	16-bit	Gor/Dol	1-65536	4	/
General purpose	TIM2, TIM5	32-bit	Gor/Dol	1-65536	4	/
Advanced control	TIM1, TIM8, TIM20	16-bit	Gor/Dol	1-65536	4	4
High resolution	HRTIM	16-bit	Gor	/1 /2 /4 x2 x4 x8 x16 x32, DLL	12	Da
Low power	LPTIM					

Basic timer (TIM6 in TIM7)

Figure 480. Basic timer block diagram



DAC trigger

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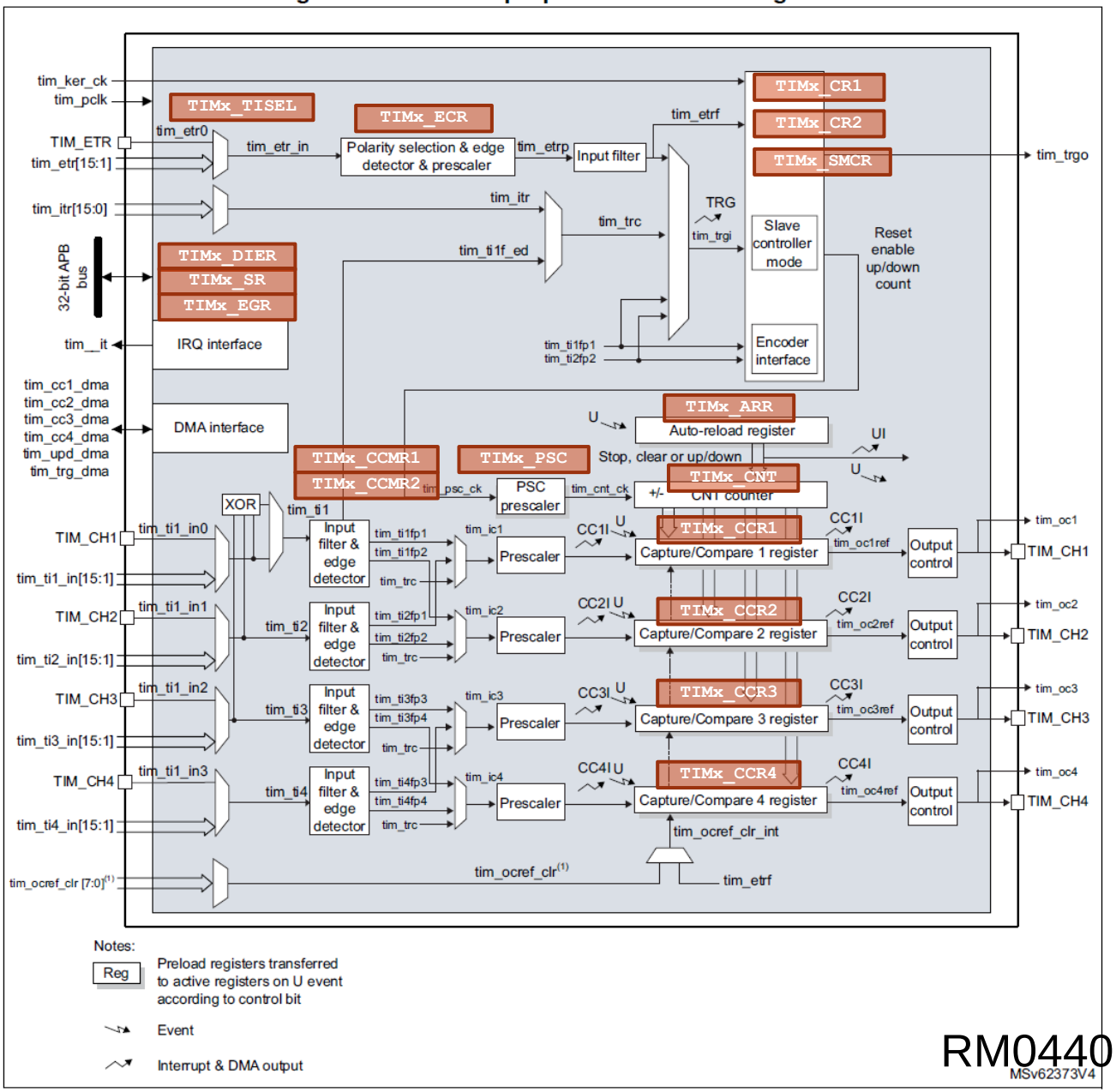
General purpose TIM2, TIM5 TIM3, TIM4

Figure 358. General-purpose timer block diagram



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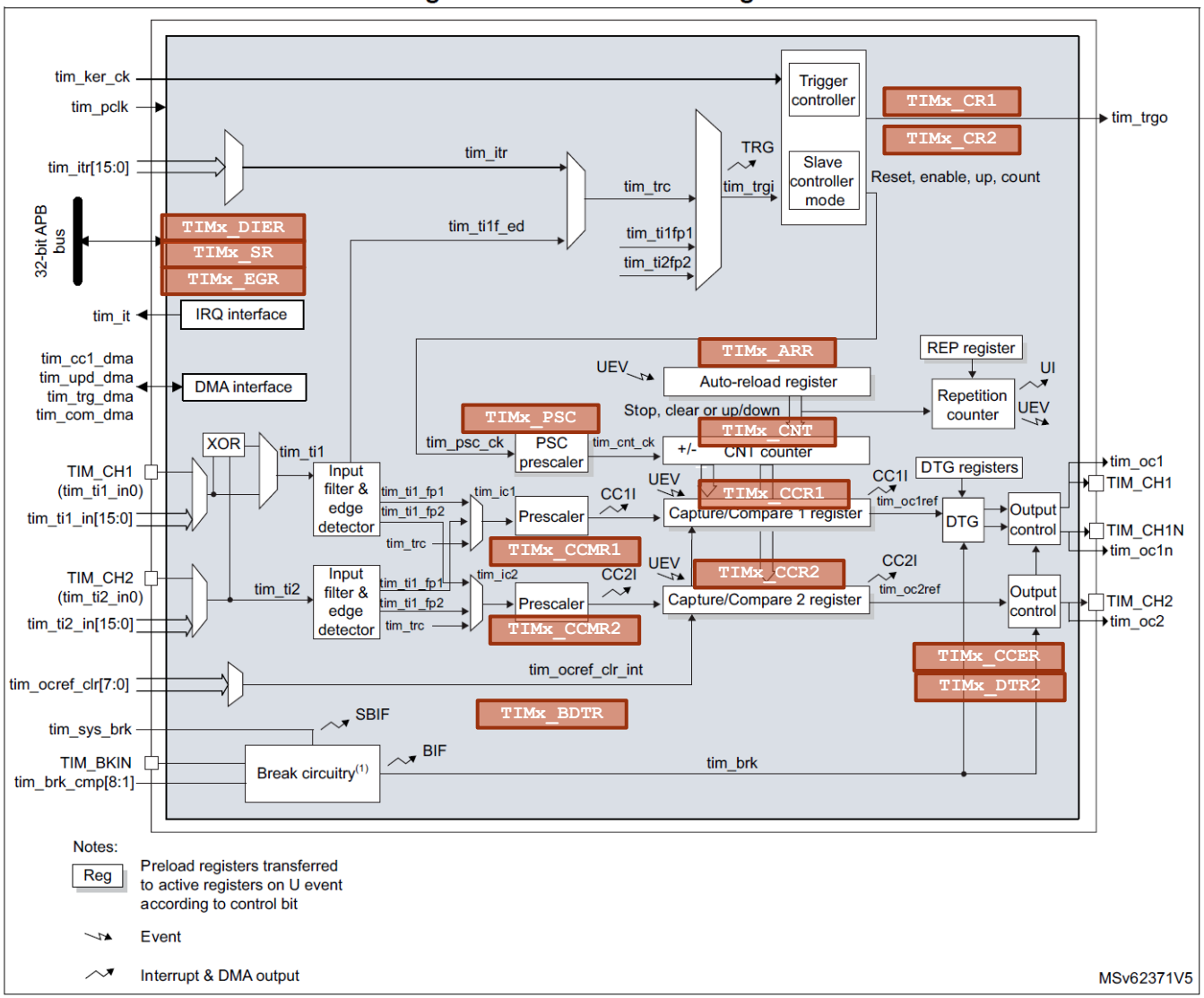
General purpose TIM15

Figure 439. TIM15 block diagram



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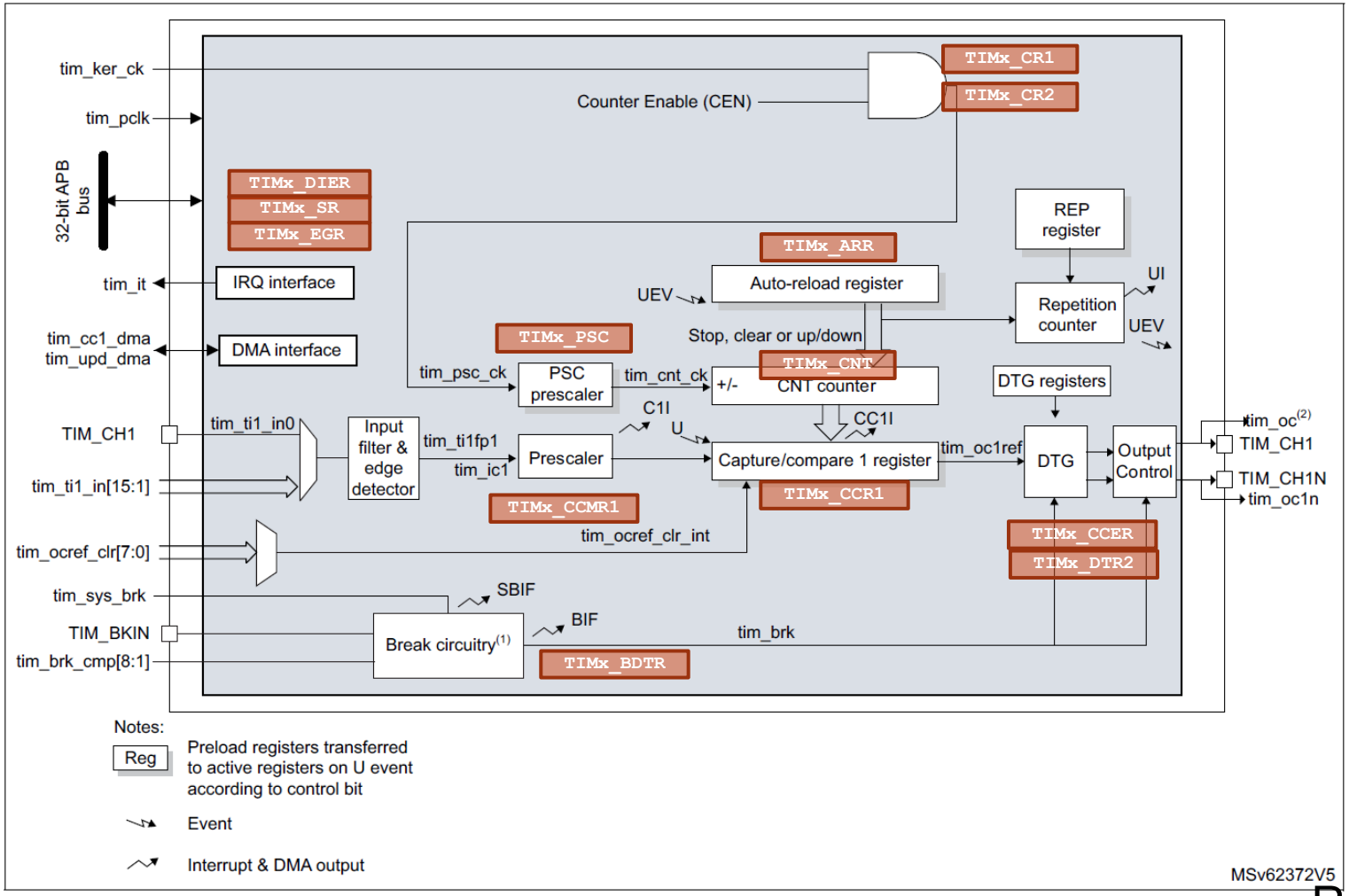
General purpose TIM16 - TIM17

Figure 440. TIM16/TIM17 block diagram



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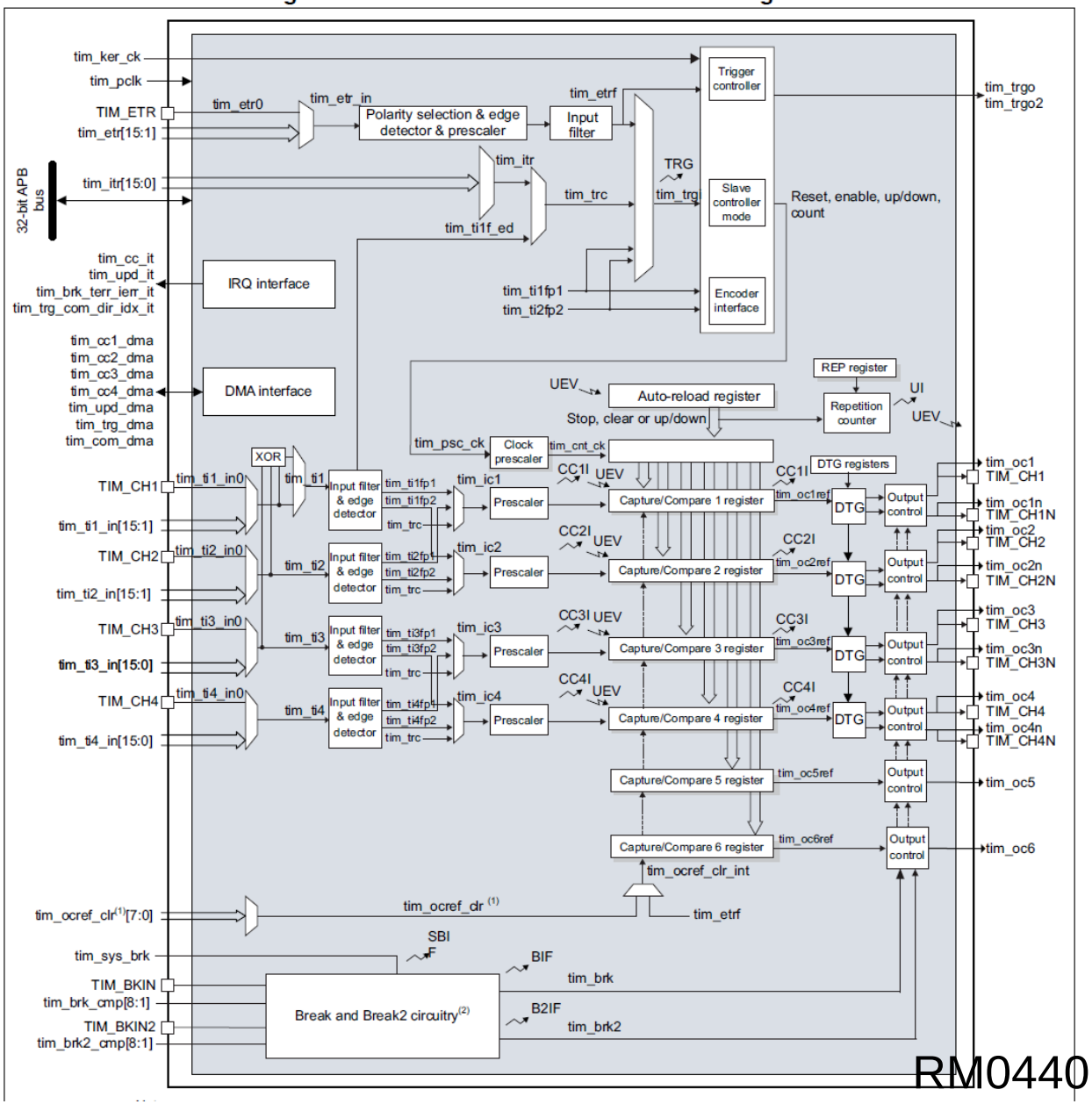
Advanced control timers (TIM1/8/20)

Figure 269. Advanced-control timer block diagram



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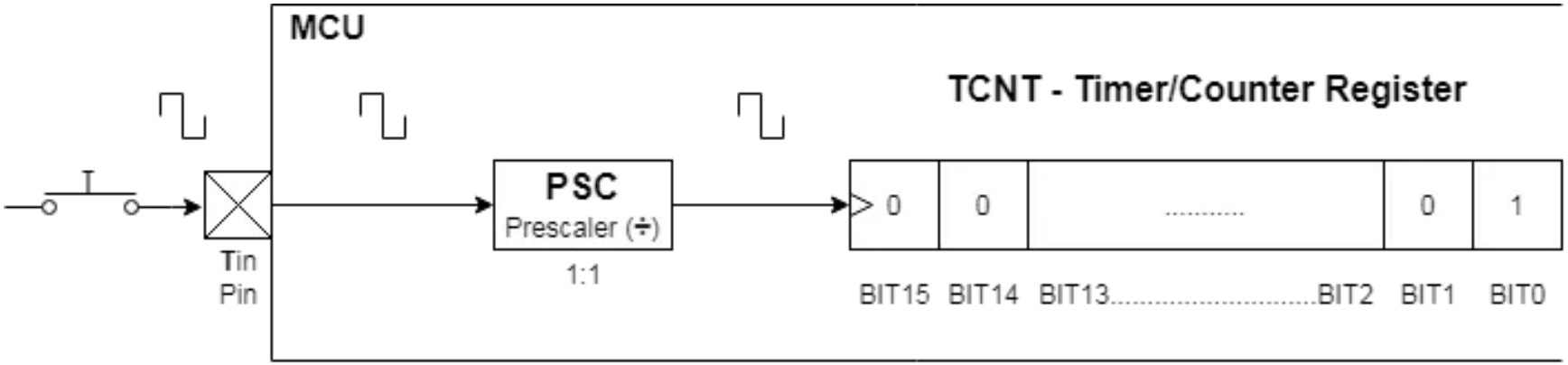
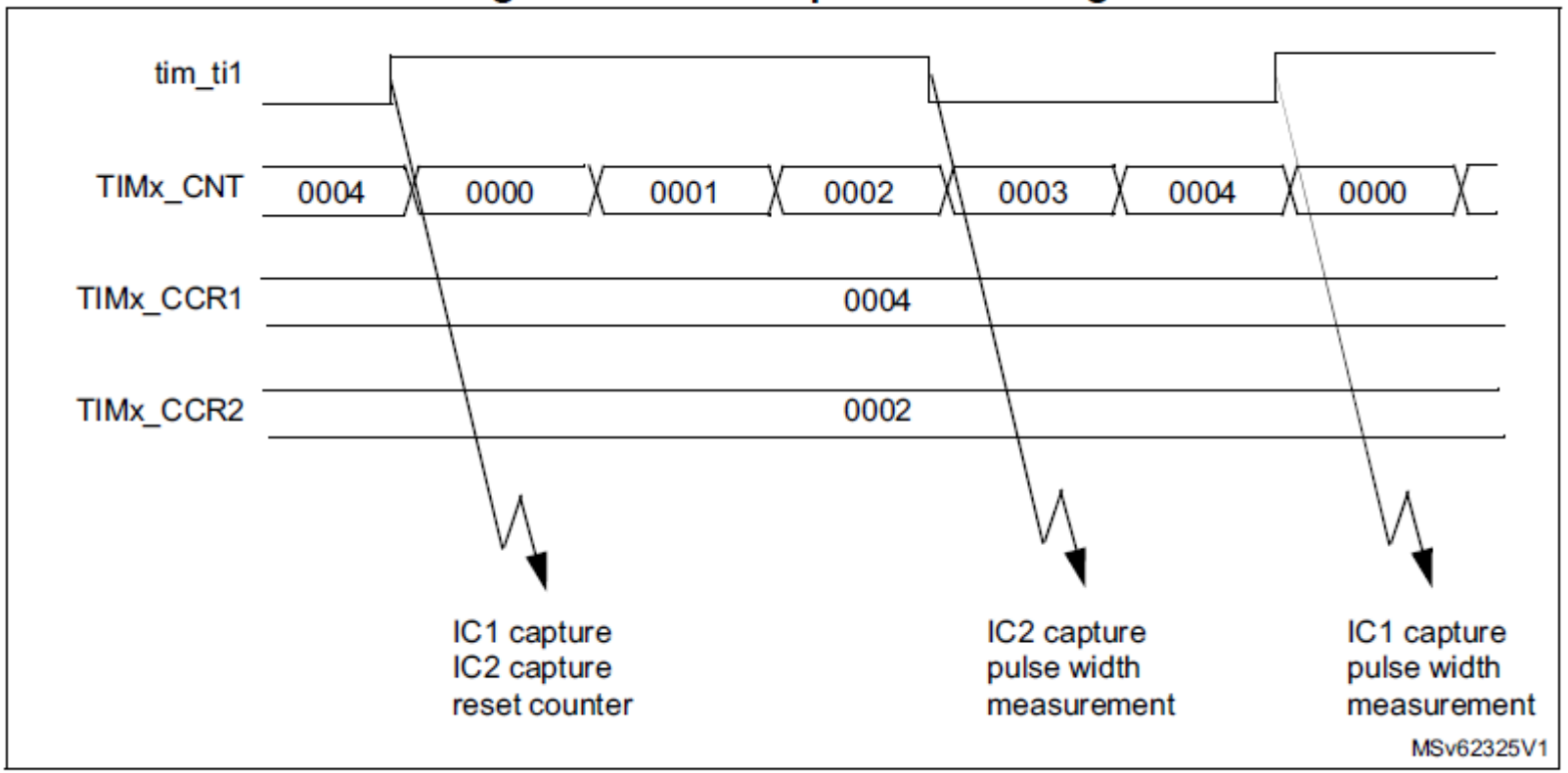
Način delovanja kot števec



- Input capture mode
- PWM input mode

Uporaba kot števec – PWM input mode

Figure 386. PWM input mode timing



1. The PWM input mode can be used only with the TIMx_CH1/TIMx_CH2 signals due to the fact that only tim_ti1fp1 and tim_ti2fp2 are connected to the slave mode controller.

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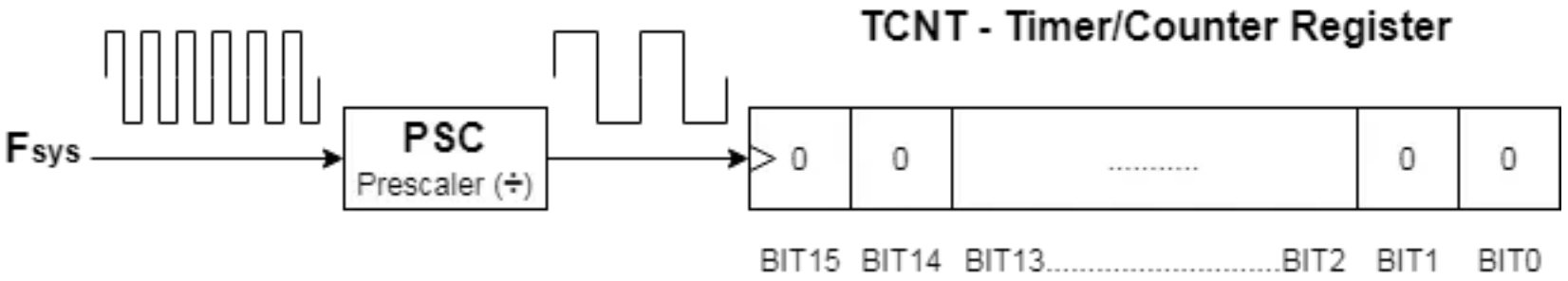
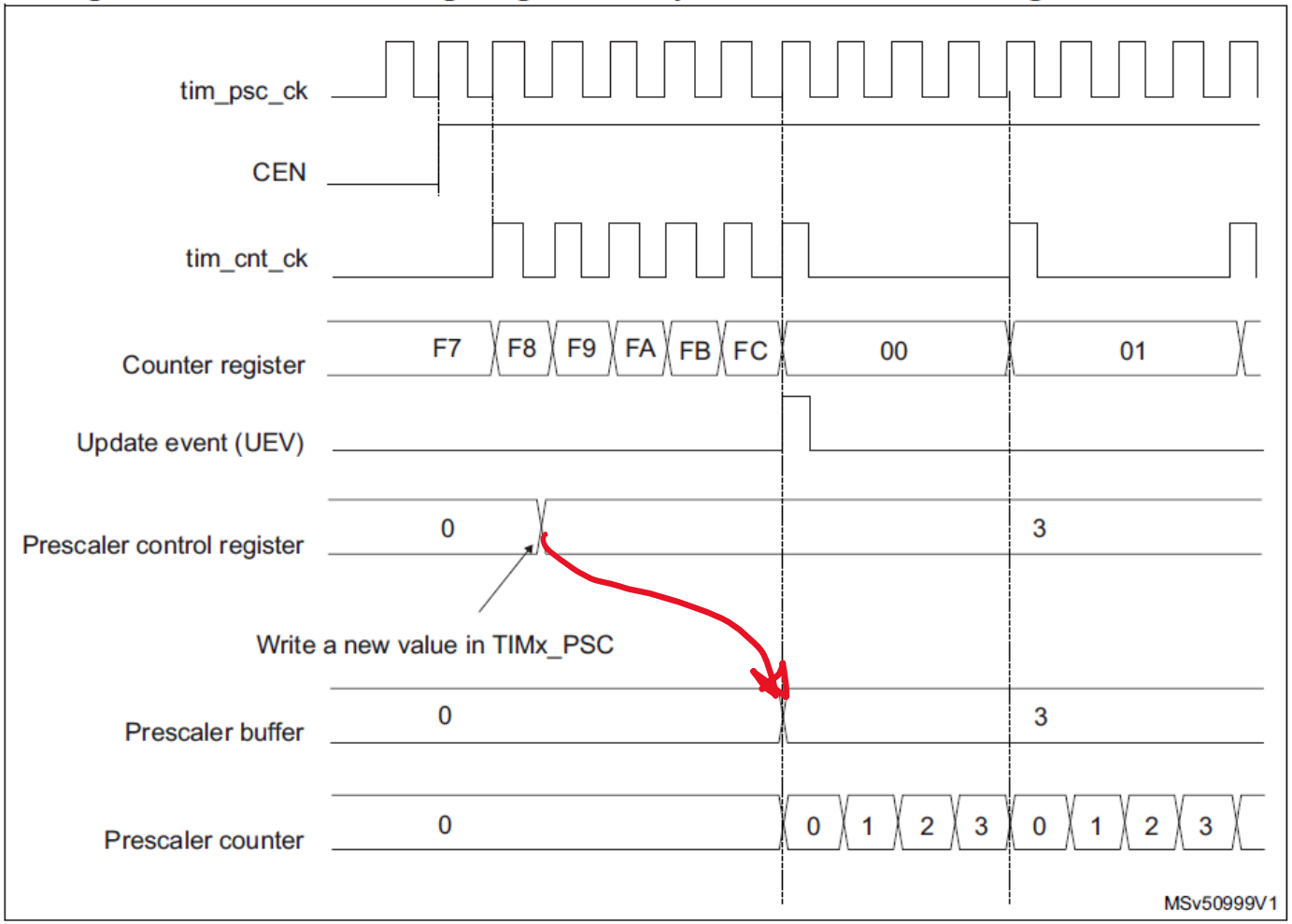
Način delovanja kot časovnik



- Output compare mode
- PWM mode
- One-pulse mode
- Encoder mode

Sprememba delilnika ure med delovanjem

Figure 483. Counter timing diagram with prescaler division change from 1 to 4



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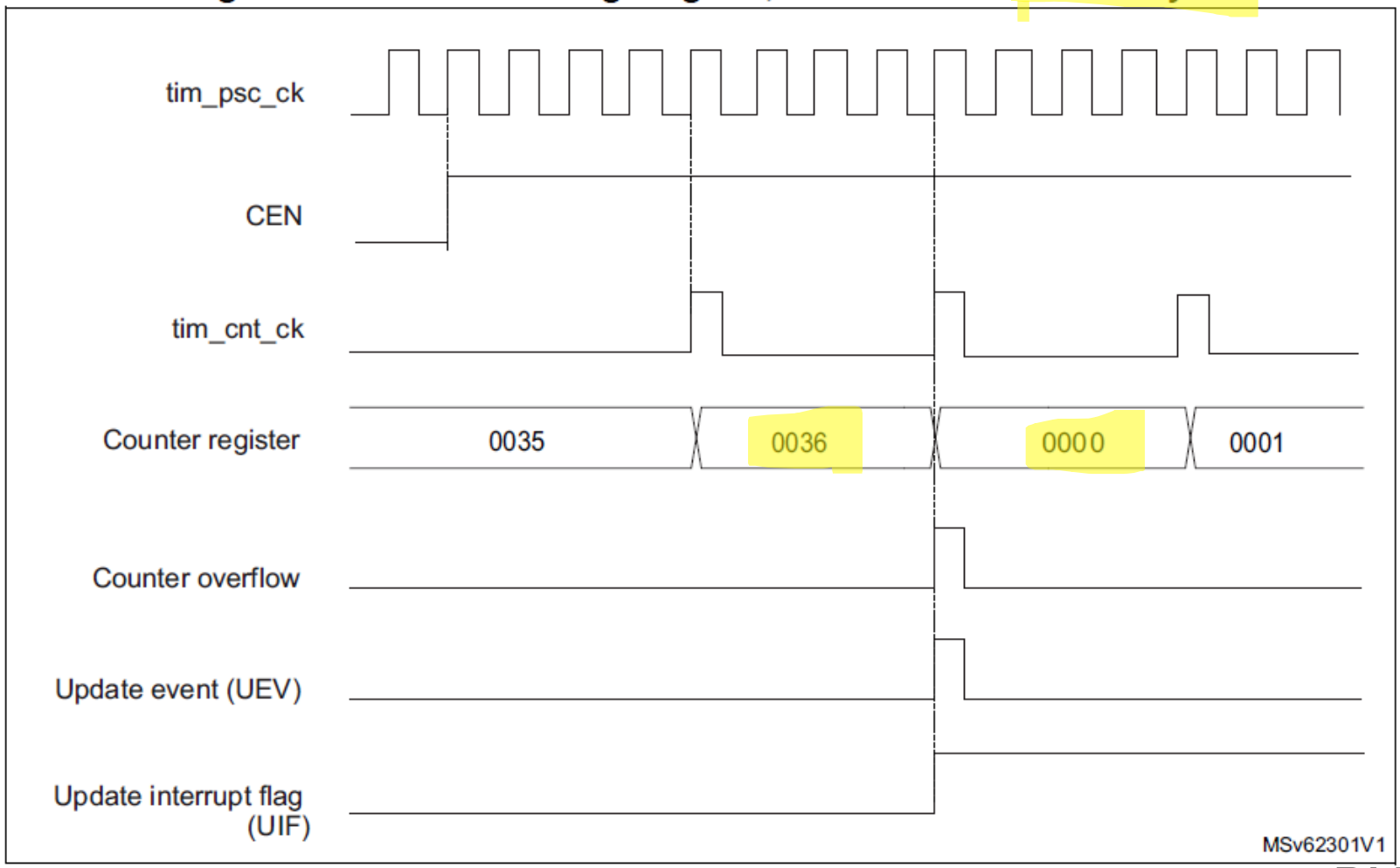
Primer preliva (update event)

TIMx_ARR = 0x36

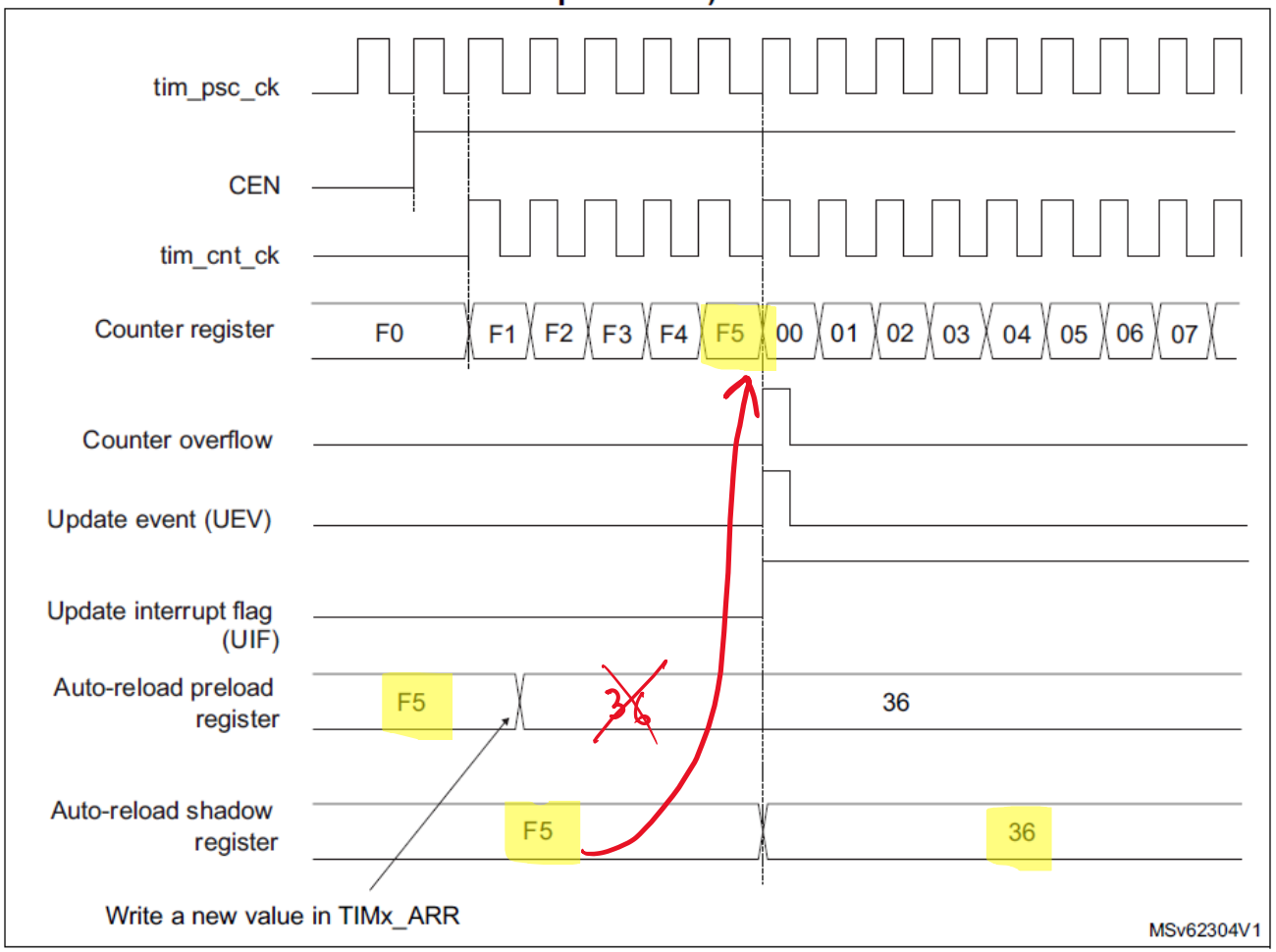
Figure 486. Counter timing diagram, internal clock divided by 4



RM0440

Vpliv ARPE=1: TIMx_ARR register is buffered

Figure 489. Counter timing diagram, update event when ARPE=1 (TIMx_ARR preloaded)



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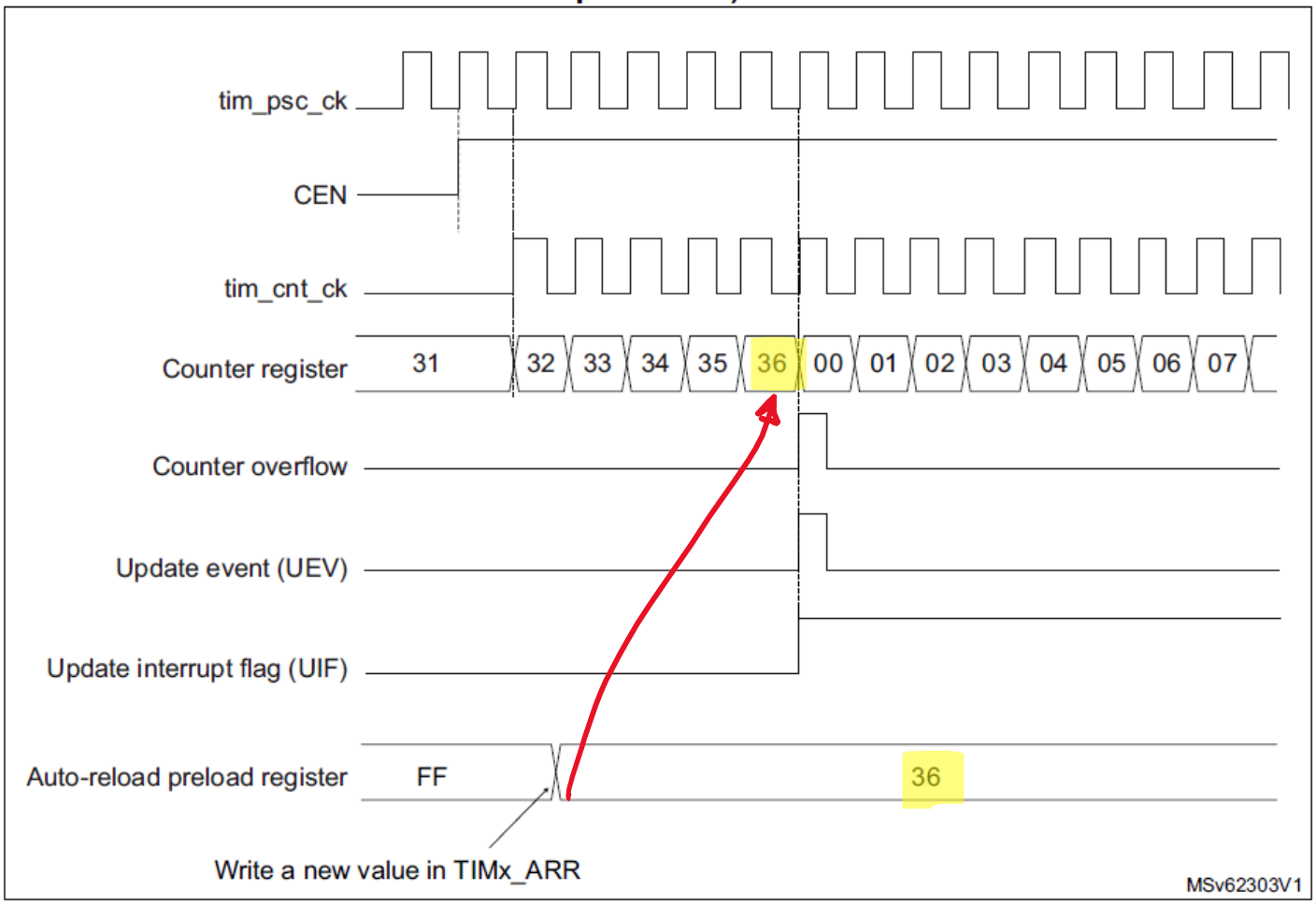
Vpliv ARPE=0: TIMx_ARR register is unbuffered

Figure 488. Counter timing diagram, update event when ARPE = 0 (TIMx_ARR not preloaded)



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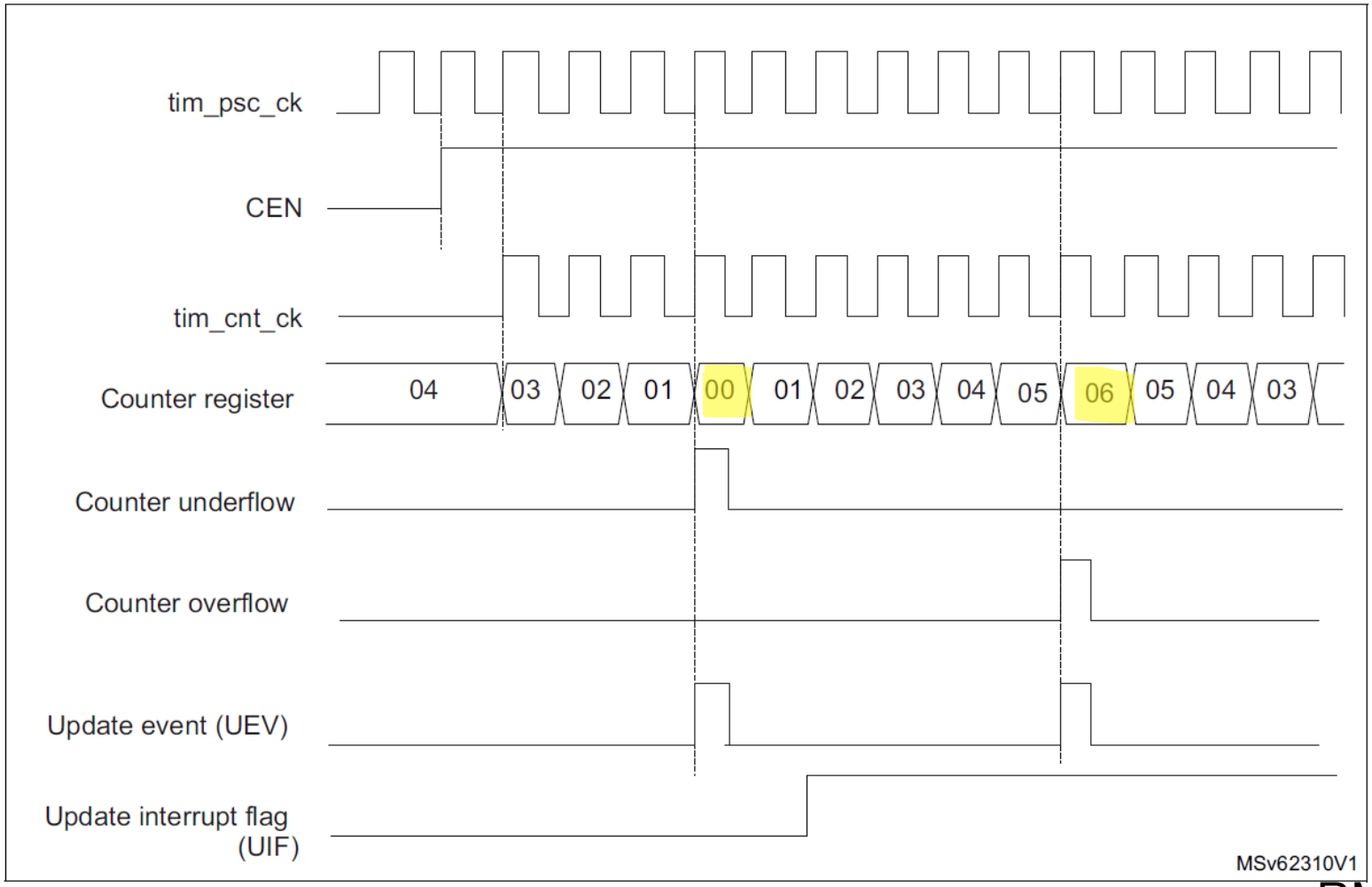
Štetje gor/dol, poravnano na sredino

Figure 372. Counter timing diagram, internal clock divided by 1, TIMx_ARR=0x6



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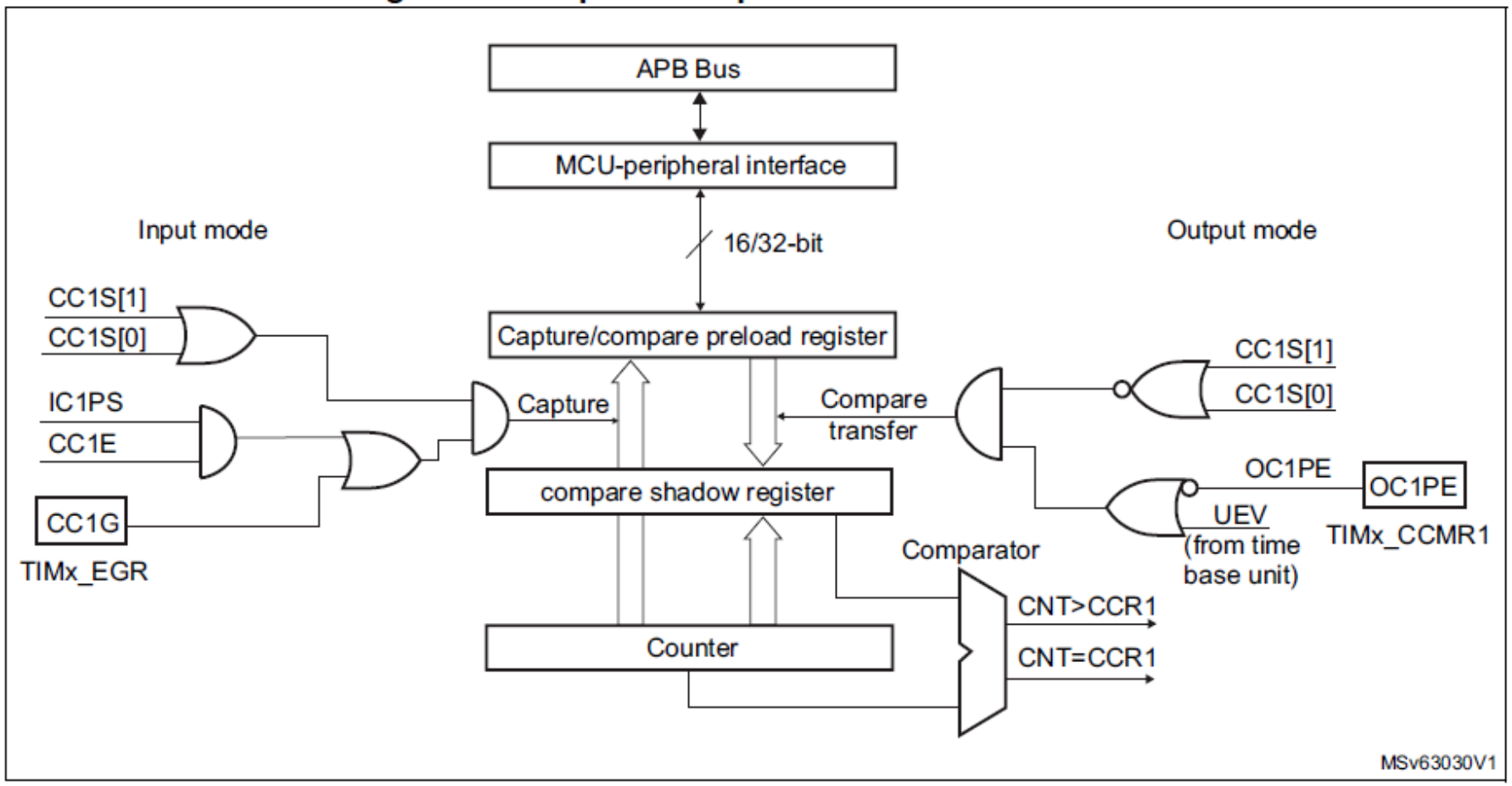
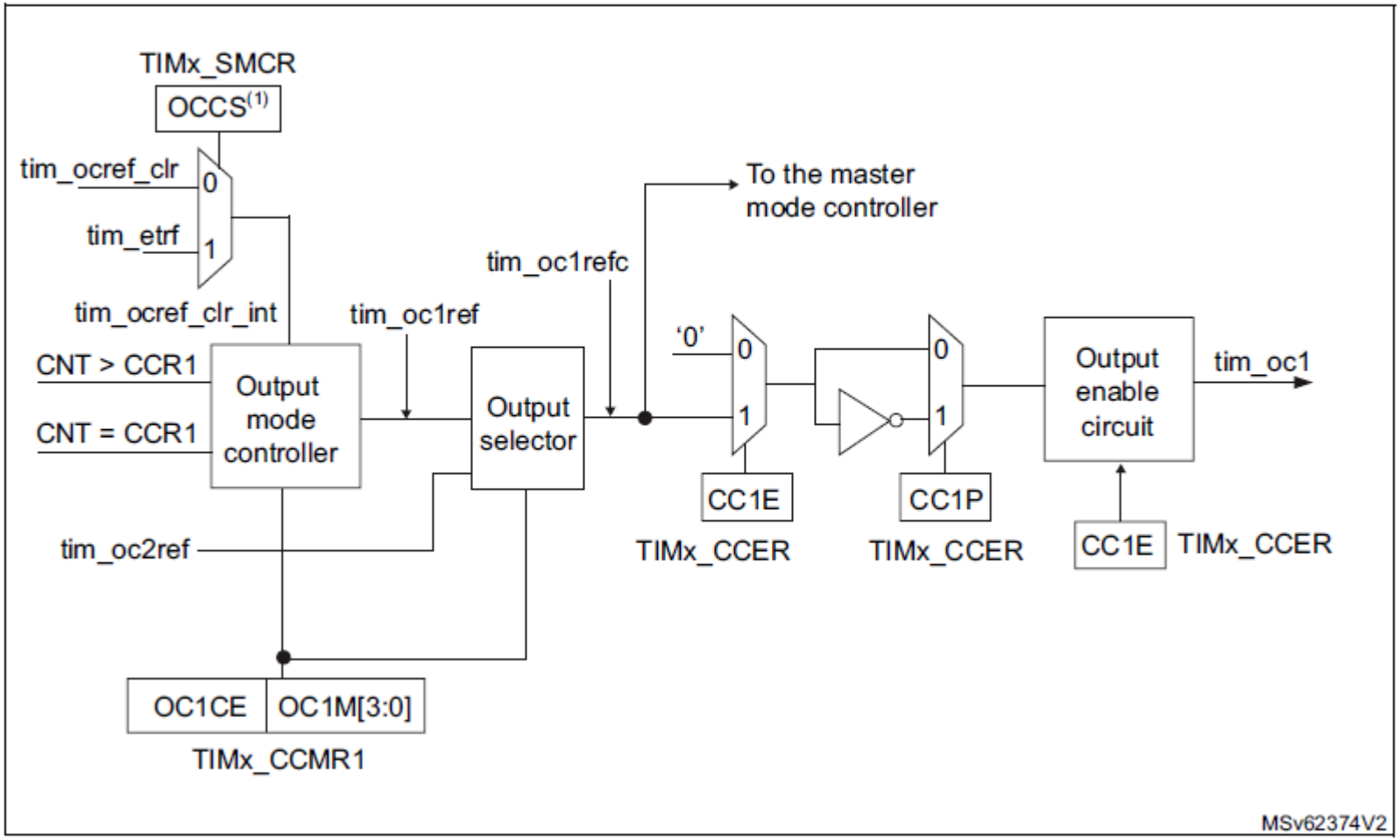
Capture/compare kanal

Figure 384. Capture/compare channel 1 main circuit



Izhodna stopnja časovnika

Figure 385. Output stage of capture/compare channel (channel 1, idem ch.2, 3 and 4)



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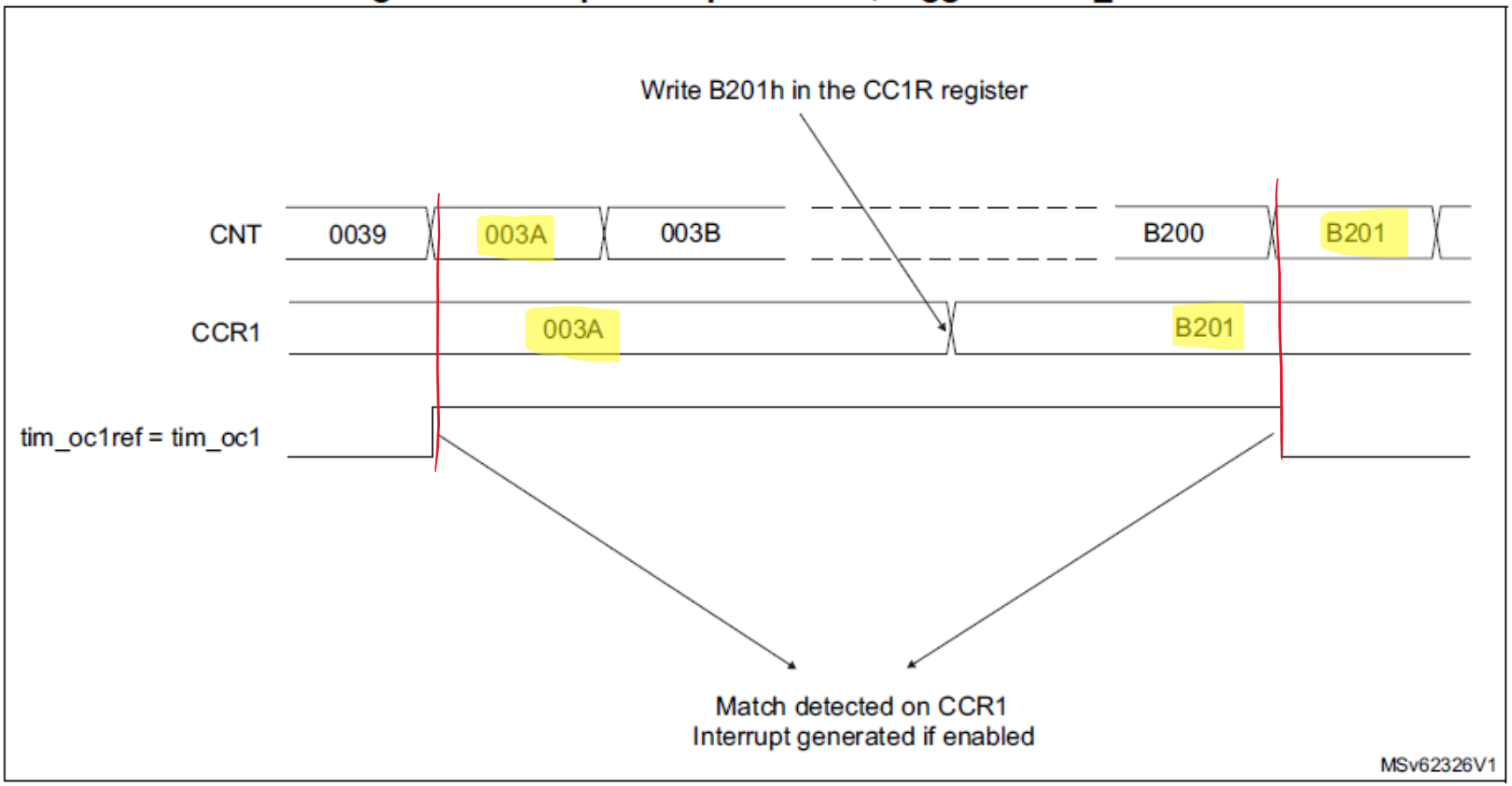
Output compare mode

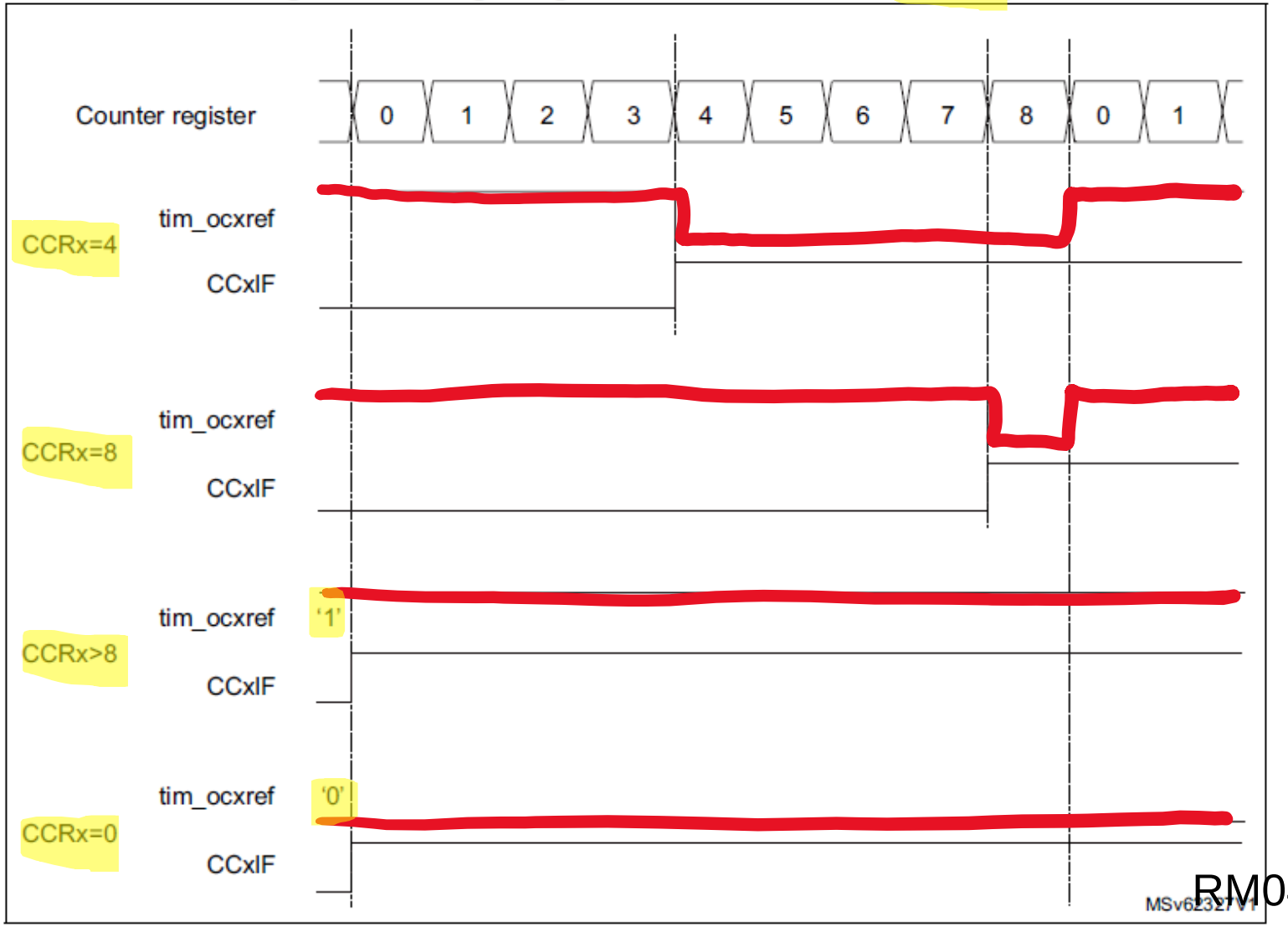
Figure 387. Output compare mode, toggle on tim_oc1



RM0440

Hitri PWM – Edge aligned

Figure 388. Edge-aligned PWM waveforms (ARR=8)



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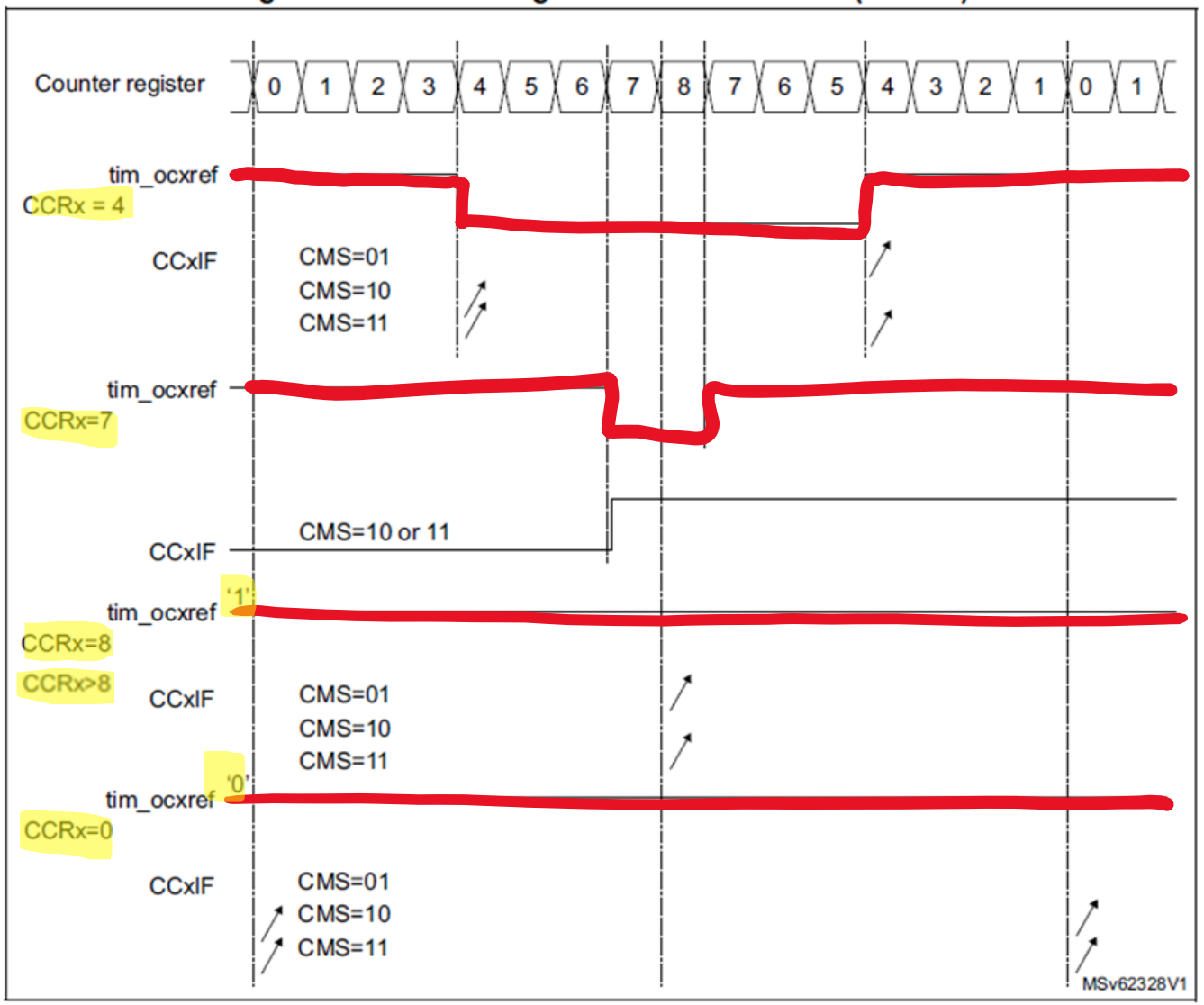
Fazno pravilni PWM – Center aligned

Figure 389. Center-aligned PWM waveforms (ARR=8)



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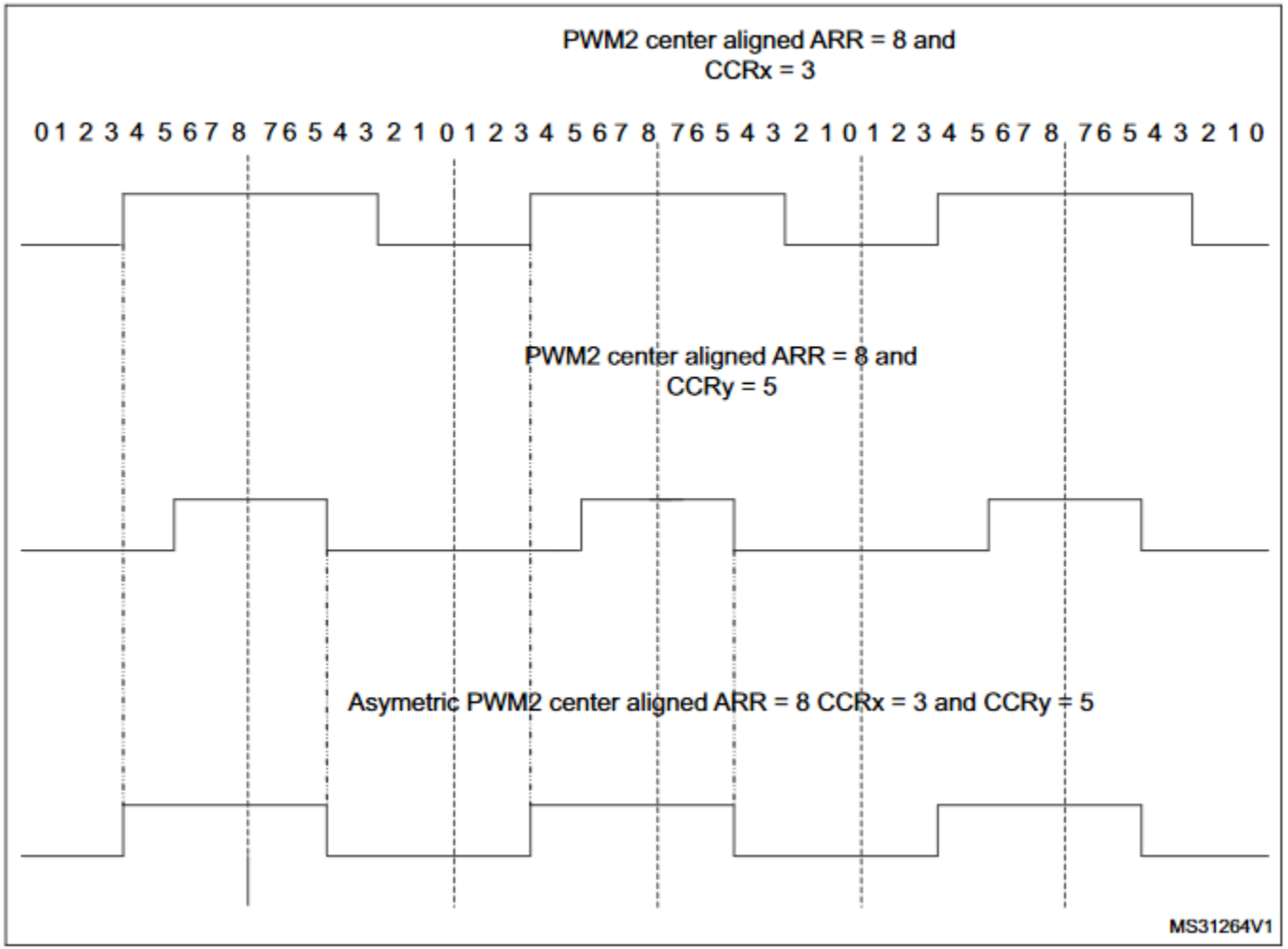
Asimetrični PWM

- Dva fazno pravilna PWM, zakasnjena za določen čas

Figure 1. Asymmetric PWM mode versus center Aligned PWM mode

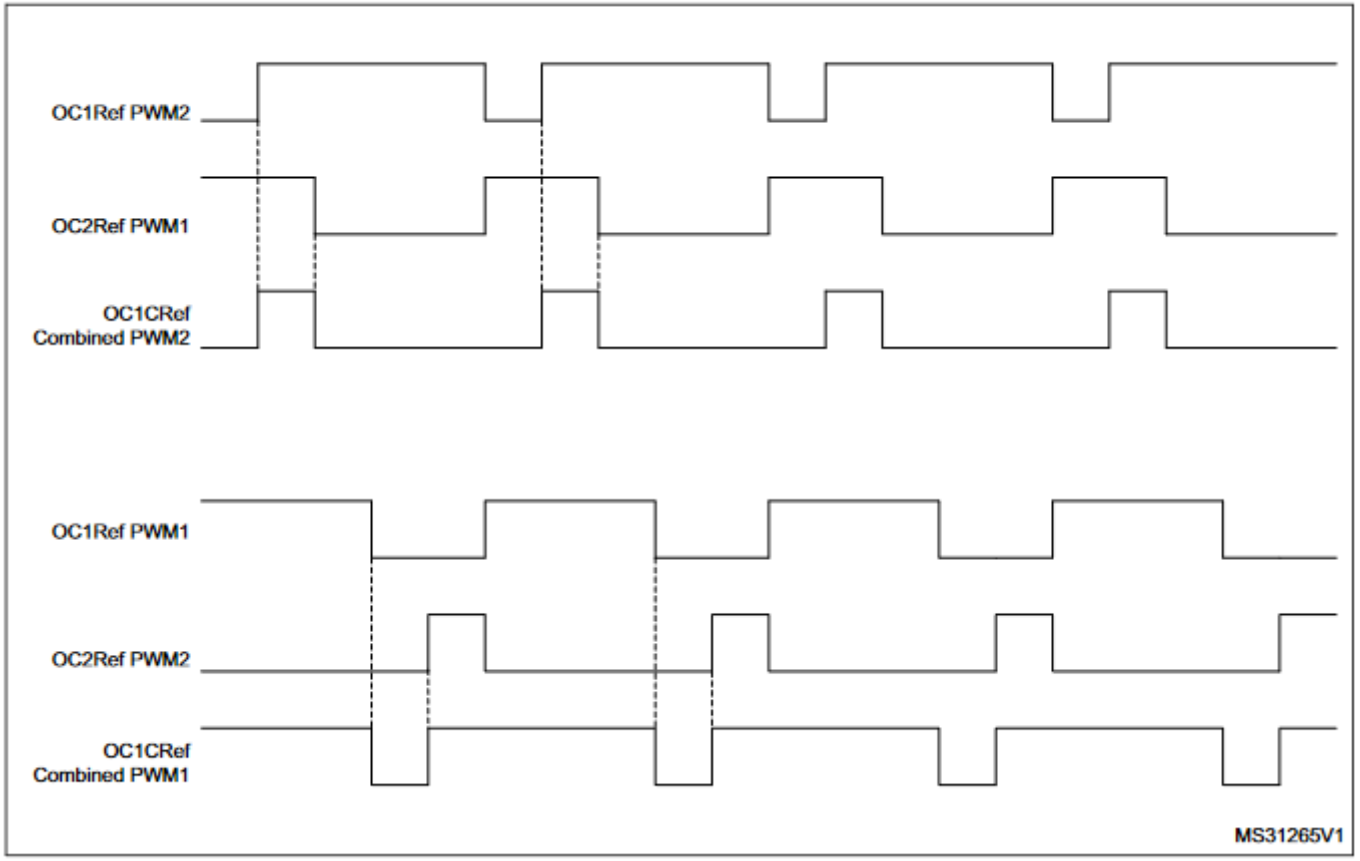


AN4013

Kombinirani PWM

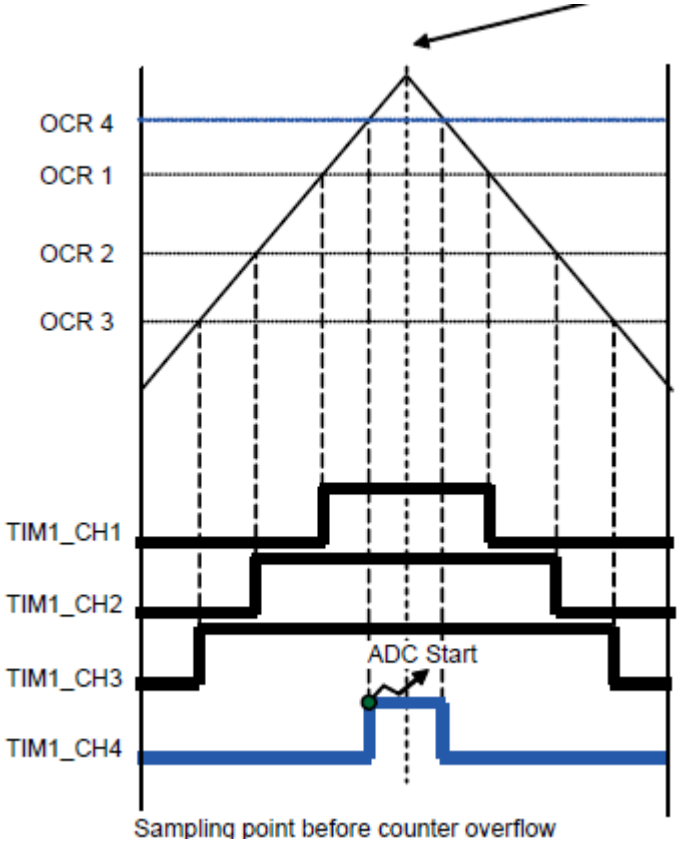
- Dva PWM, kombinirana z ALI ali IN logiko

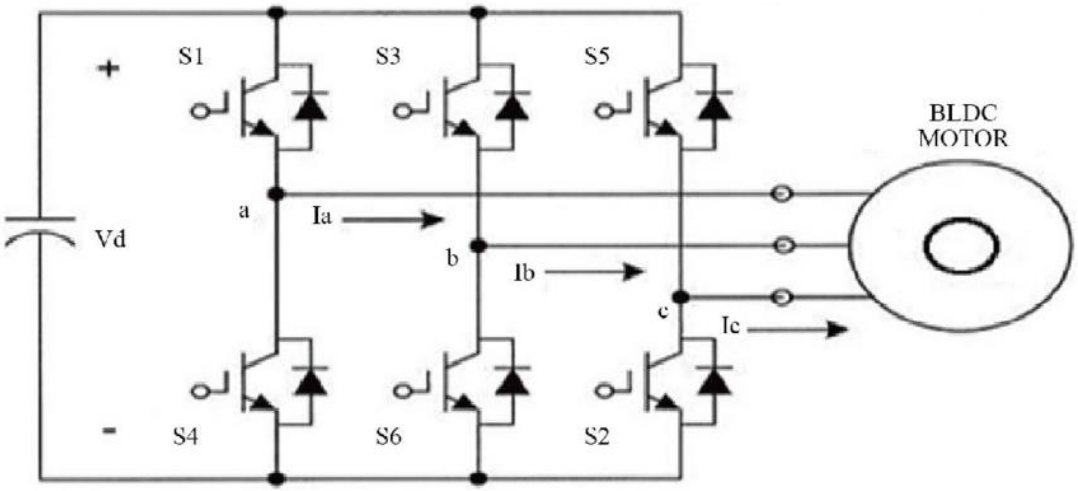
Figure 2. Combined PWM mode



AN4013

Kombinirani tri-fazni PWM





UM1052

Generacija mrtvih časov

- Protifazno krmiljenje polmostiča

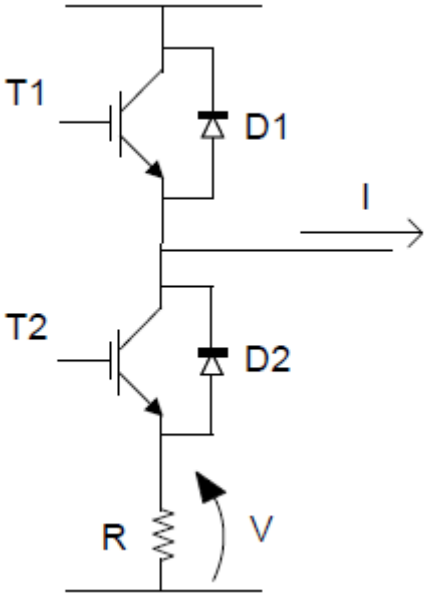
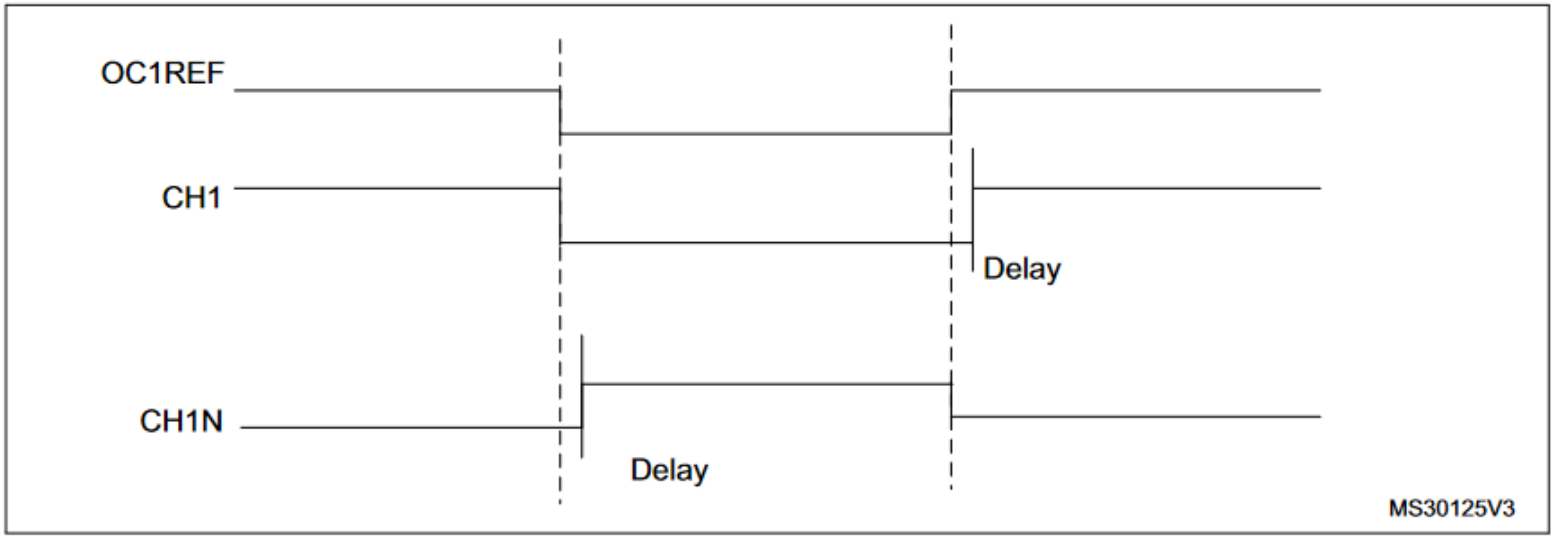
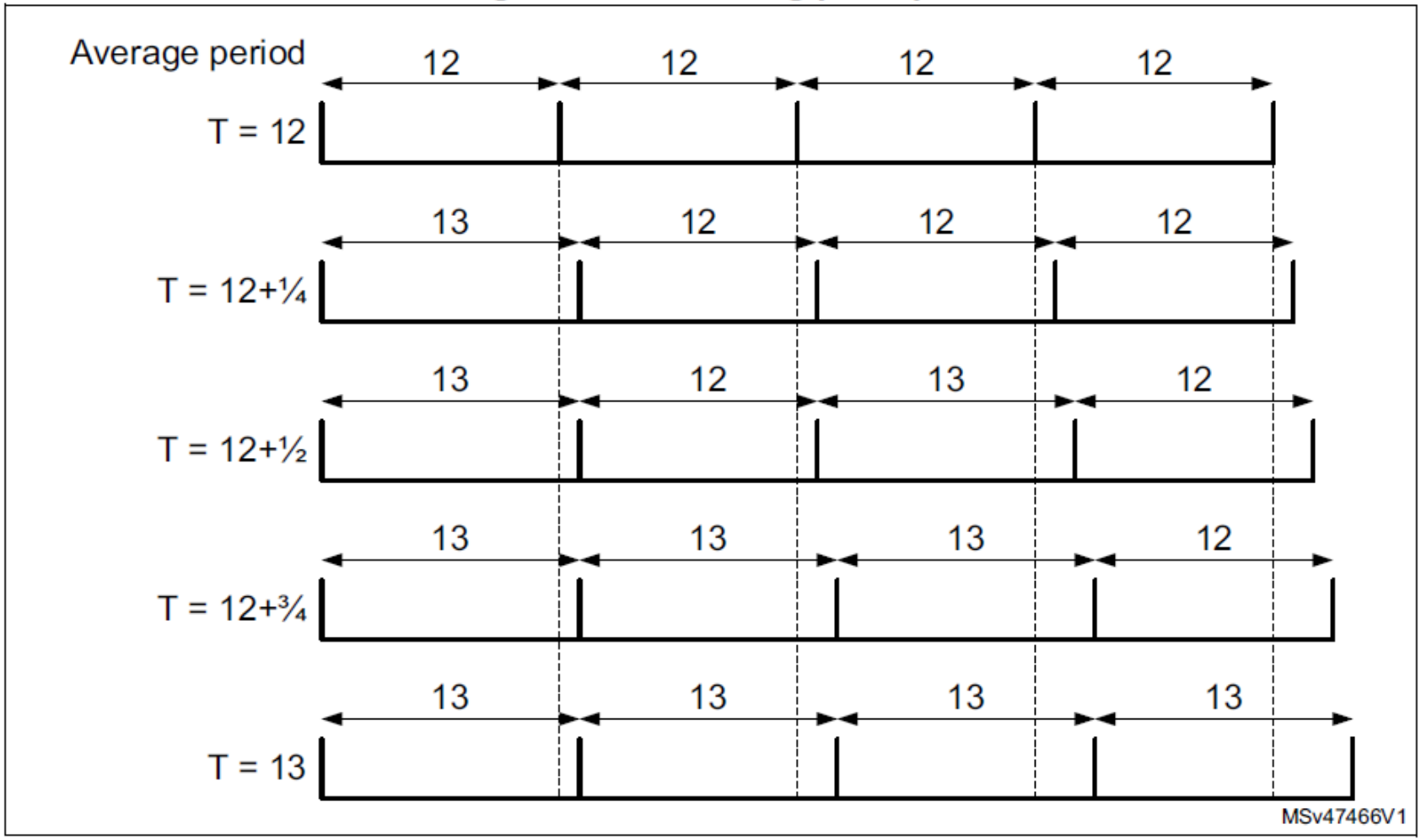


Figure 6. Two signals are generated with insertion of a deadtime



Povečanje ločljivosti - dithering

Figure 490. Dithering principle



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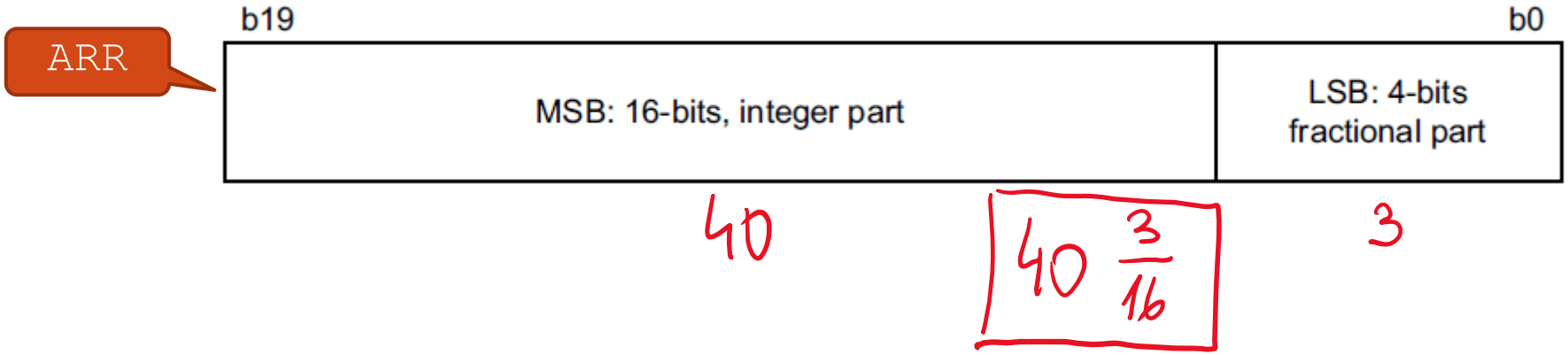
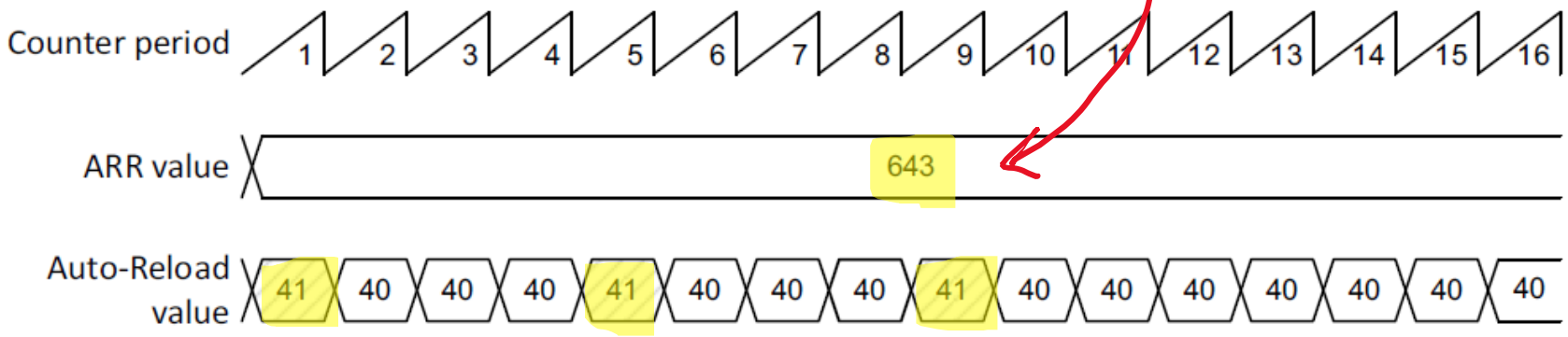
Povečanje ločljivosti s tresenjem - dithering



$40 \cdot 16 + 3 = 643$



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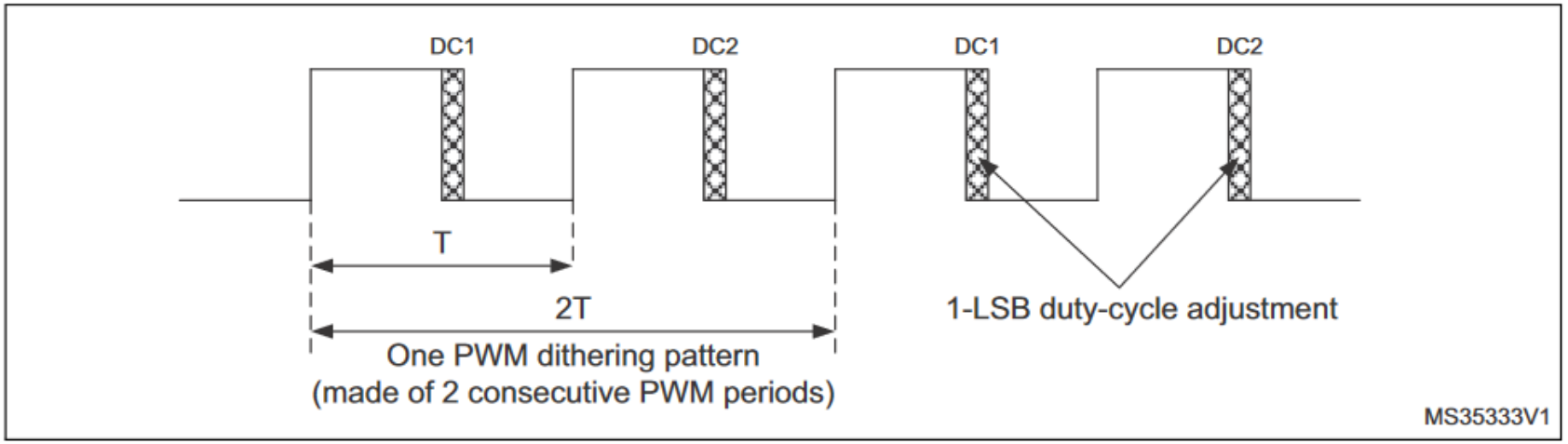
Povečanje ločljivosti PWM s tresenjem

Figure 1. Duty-cycle adjustment for PWM dithering technique

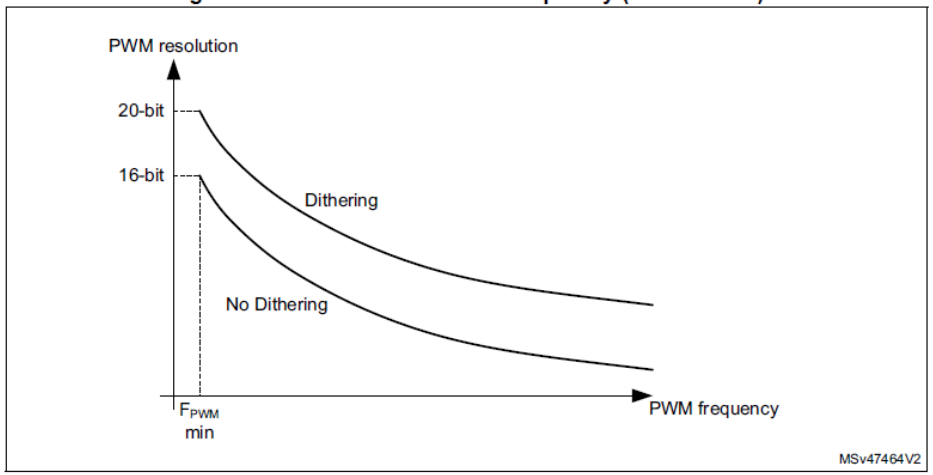


$$R_{PWM} = \frac{f_{clk}}{f_{PWM}}$$

$$R_{PWM+dith} = R_{PWM} + R_{dith}$$

$$N_{period\_dith} = 2^{R_{dith}}$$

Figure 392. PWM resolution vs frequency (16-bit mode)



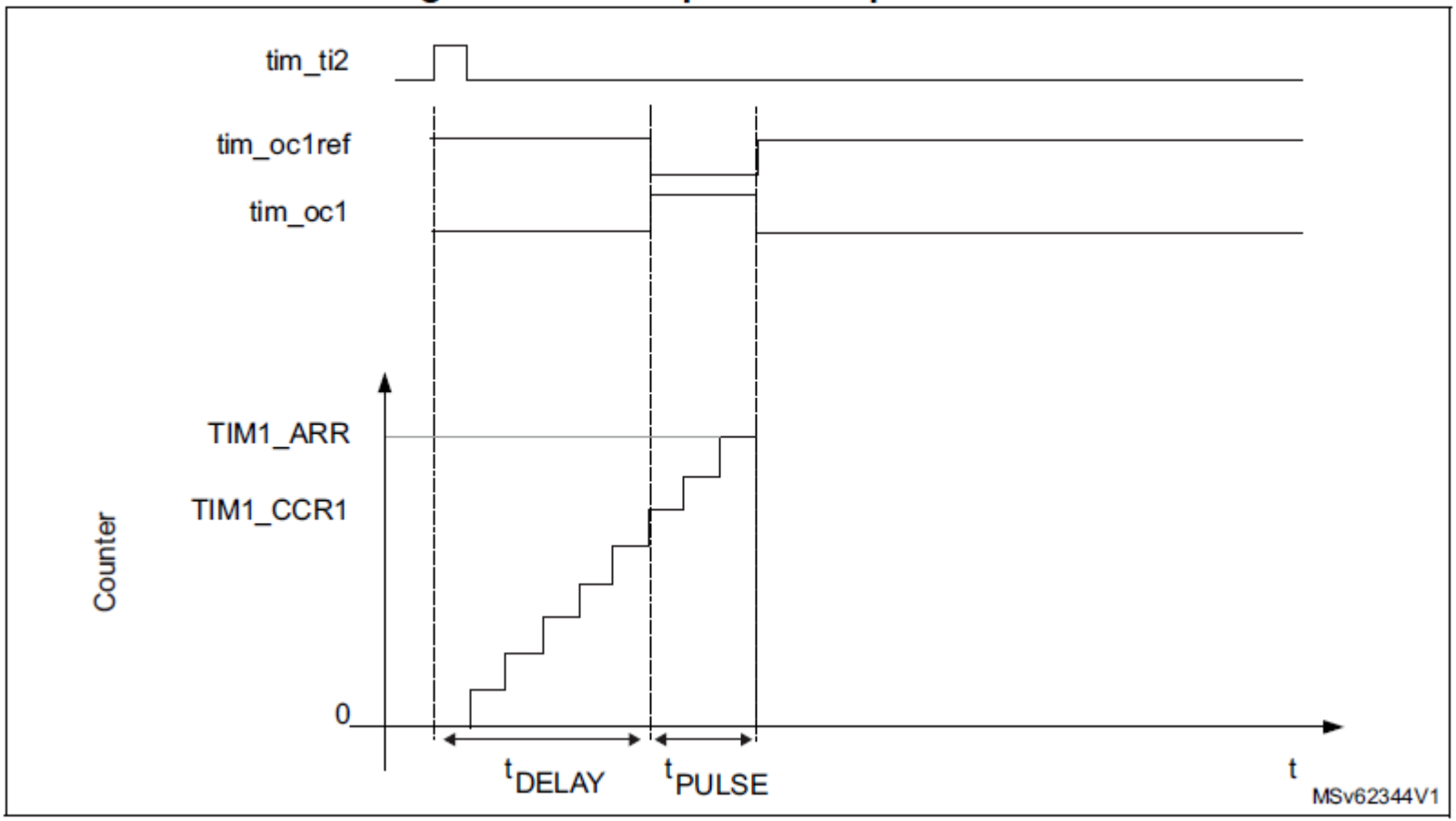
AN4507

Vpliv povečane ločljivosti s tresenjem

Figure 8. Dithering effect applied on the rising slope of the triangular waveform

Monostabilni način – One-pulse mode

Figure 400. Example of One-pulse mode

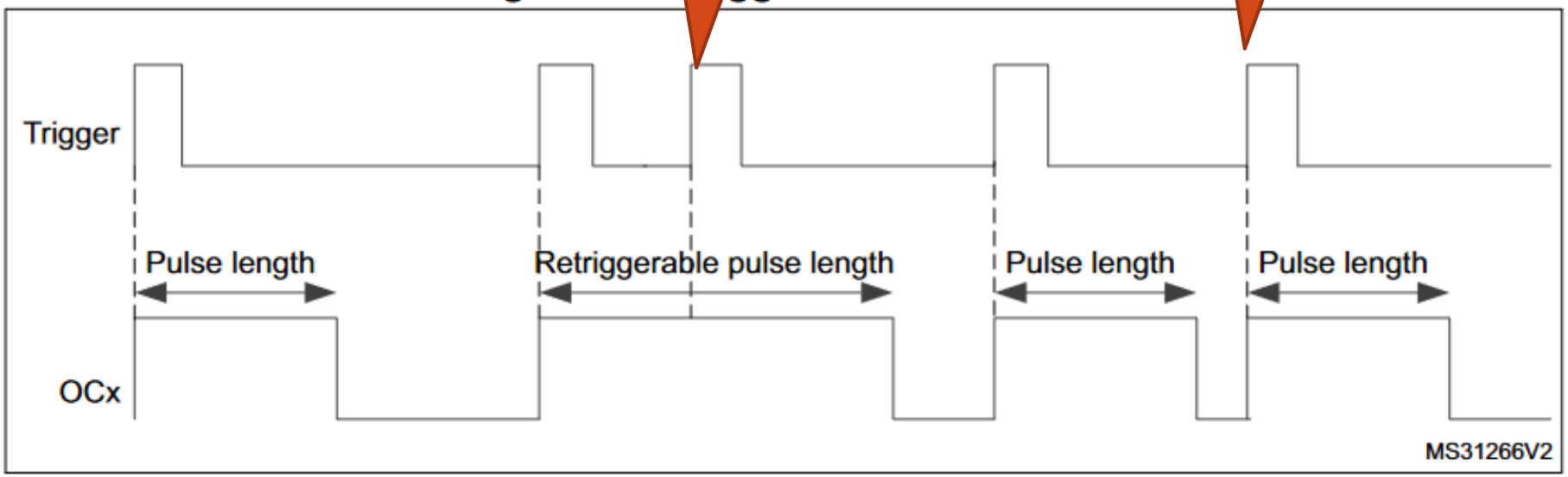


RM0440

Monostabilni način: Retriggerable one-pulse mode

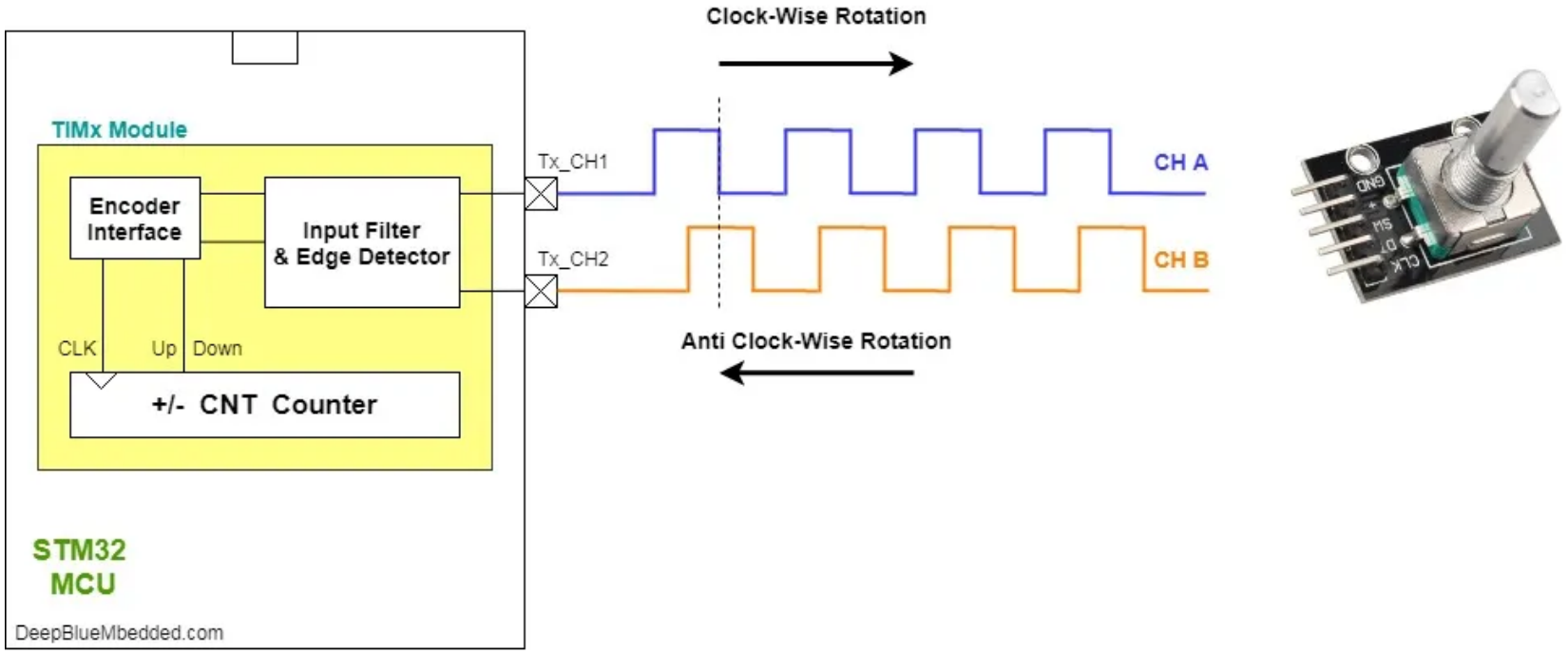
Trigger prišel v času pulza

Trigger prišel prepozno



AN4013

Enkoderski način – kvadraturni enkoder



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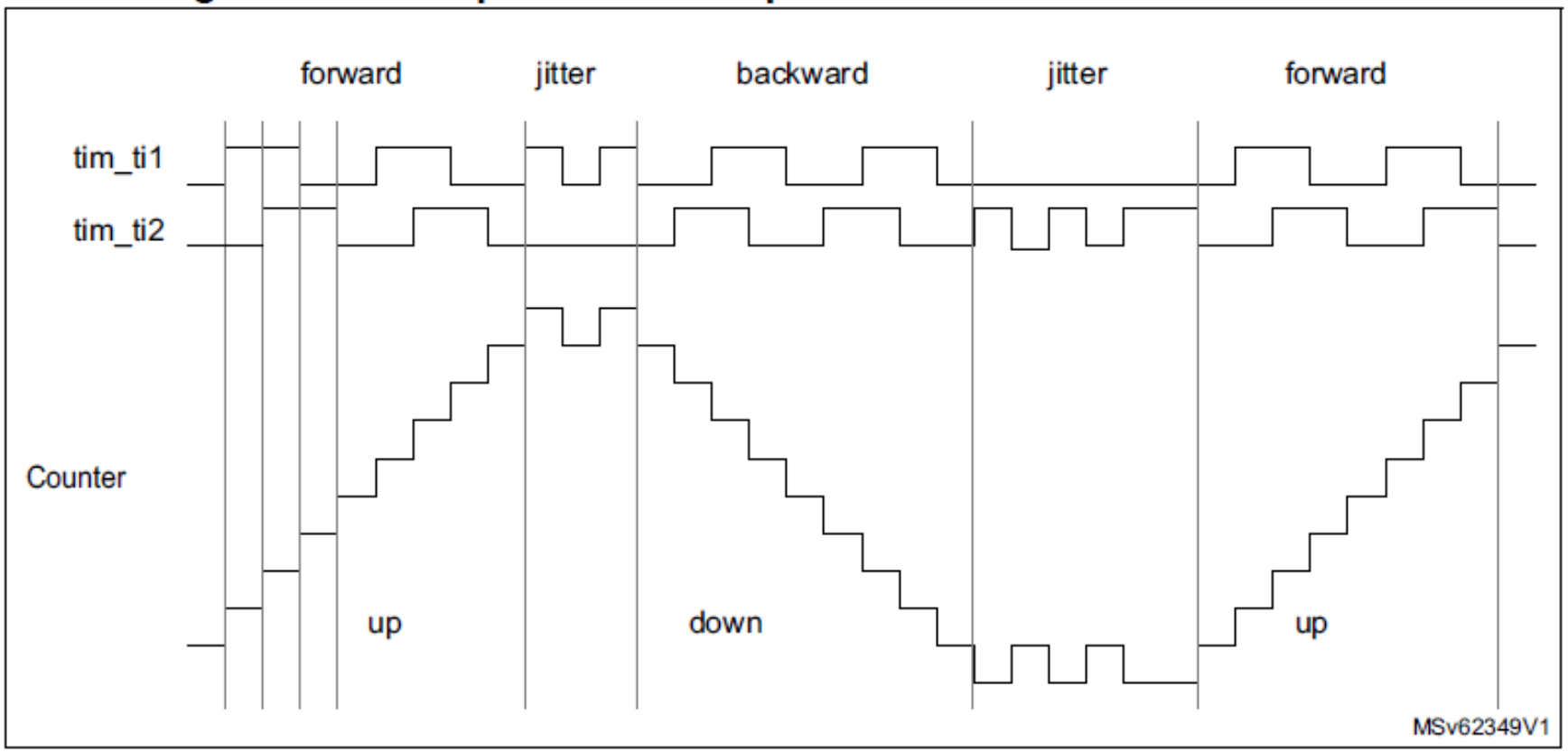
Enkoderski način – kvadraturni enkoder

Figure 405. Example of counter operation in encoder interface mode



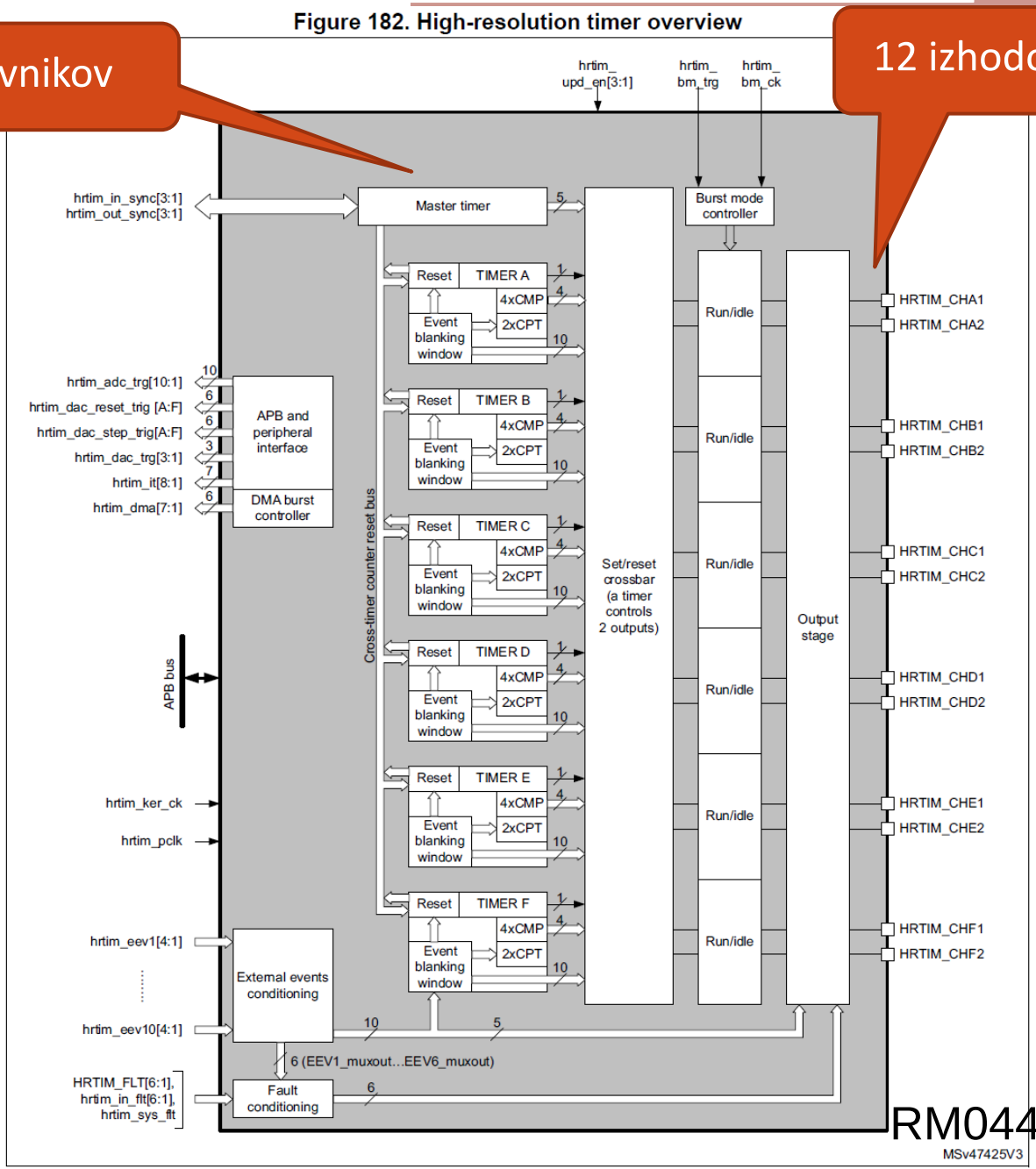
RM0440

High resolution timer HRTIM

7 časovnikov

12 izhodov

Figure 182. High-resolution timer overview



HRTIM osnovne frekvence

DLL –delay locked loop

Timer	TIMx	HRTIMER
Timer resolution	5.9ns	184ps
Equivalent Clock frequency	170MHz	5.44GHz
Resolution (F_{PWM} = 300kHz)	566 levels (9.1 bit)	18133 levels (14.1 bit)
Frequency adjustment step (F_{PWM} = 300kHz)	532Hz	16.5 Hz

Table 215. Timer resolution and min. PWM frequency for f_{HRTIM} = 170 MHz

CKPSC[2:0]	Prescaling ratio	f_{HRCK} equivalent frequency	Resolution	Min PWM frequency
000	1	170 x 32 MHz = 5.44 GHz	184 ps	83.0 kHz
001	2	170 x 16 MHz = 2.72 GHz	368 ps	41.5 kHz
010	4	170 x 8 MHz = 1.36 GHz	735 ps	20.8 kHz
011	8	170 x 4 MHz = 680 MHz	1.47 ns	10.4 kHz
100	16	170 x 2 MHz = 340 MHz	2.94 ns	5.19 kHz
101	32	170 MHz	5.88 ns	2.59 kHz
110	64	170/2 MHz = 85 MHz	11.76 ns	1.30 kHz
111	128	170/4 MHz = 42.5 MHz	23.53 ns	0.65 kHz

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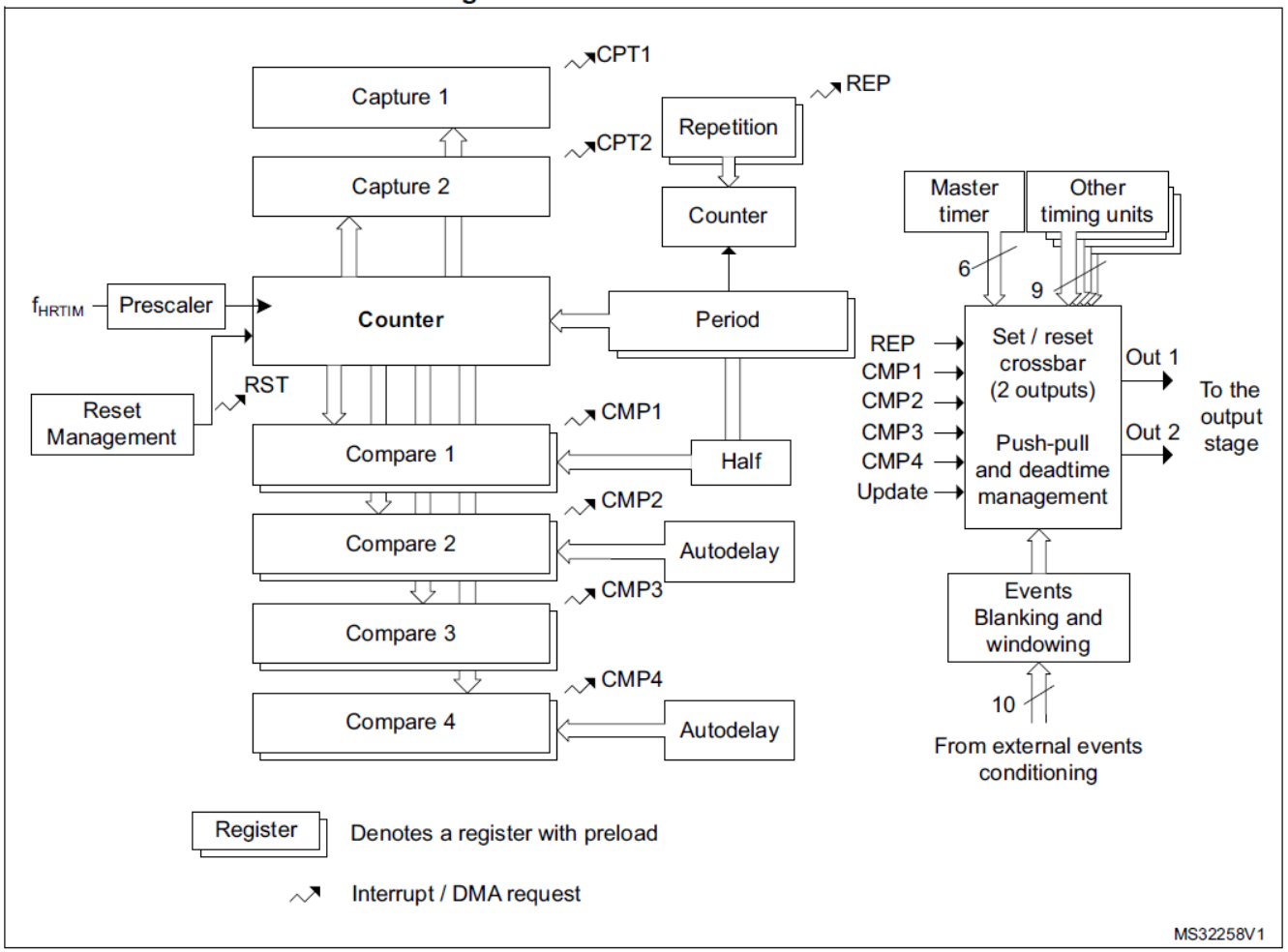
Posamezne enote časovnikov znotraj HRTIM

Figure 184. Timer A..F overview



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Aplikacija HRTIM – sinhroni pretvornik navzdol

Figure 263. Synchronous rectification depending on output current

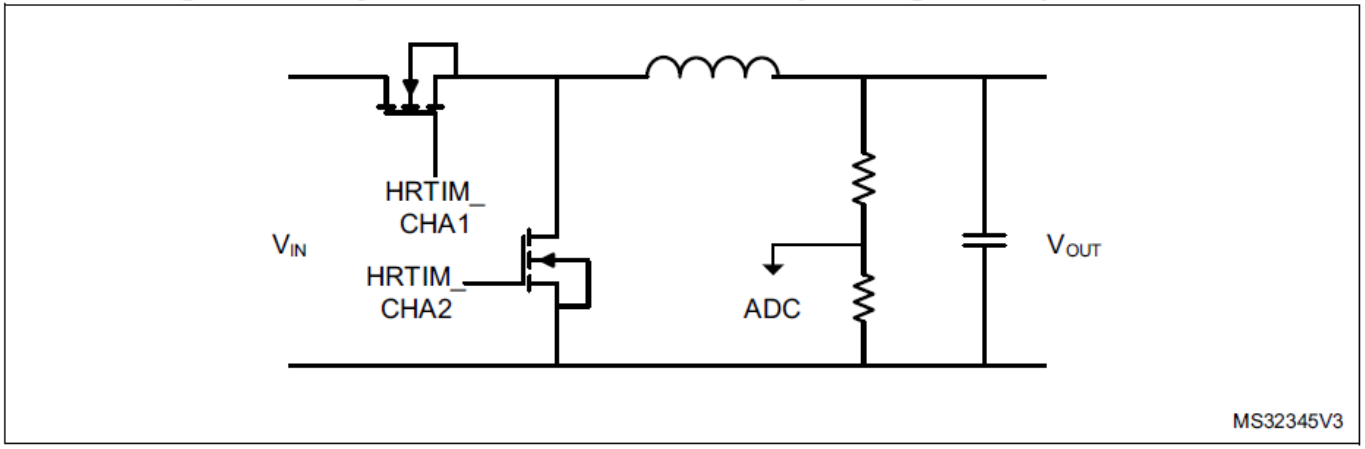
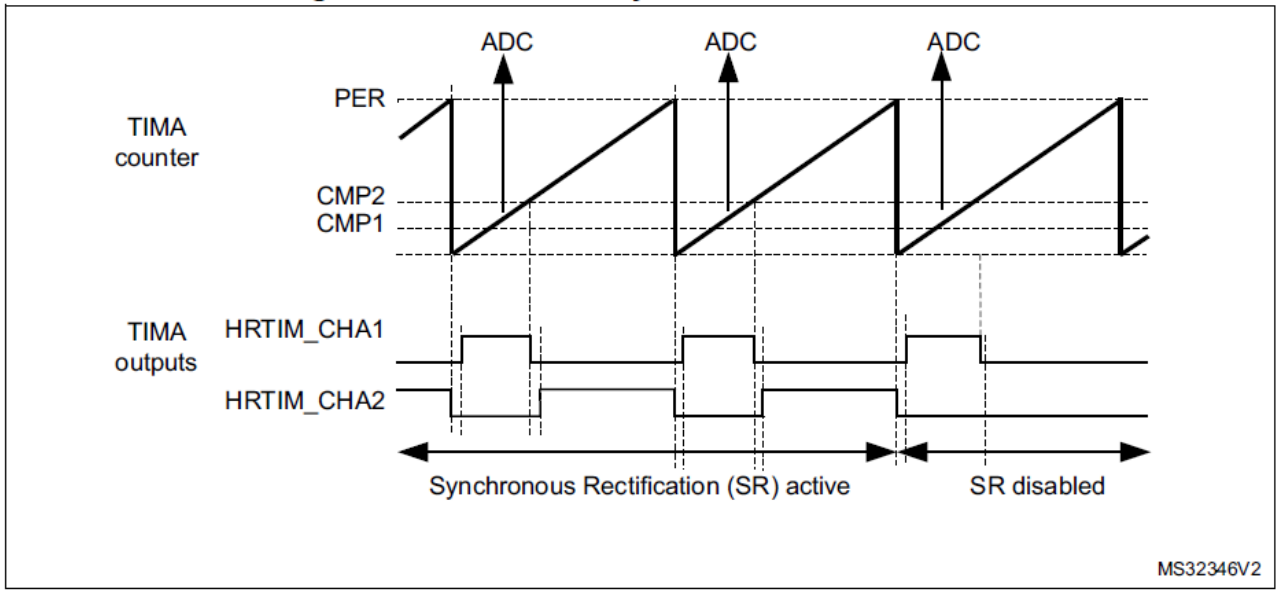


Figure 264. Buck with synchronous rectification



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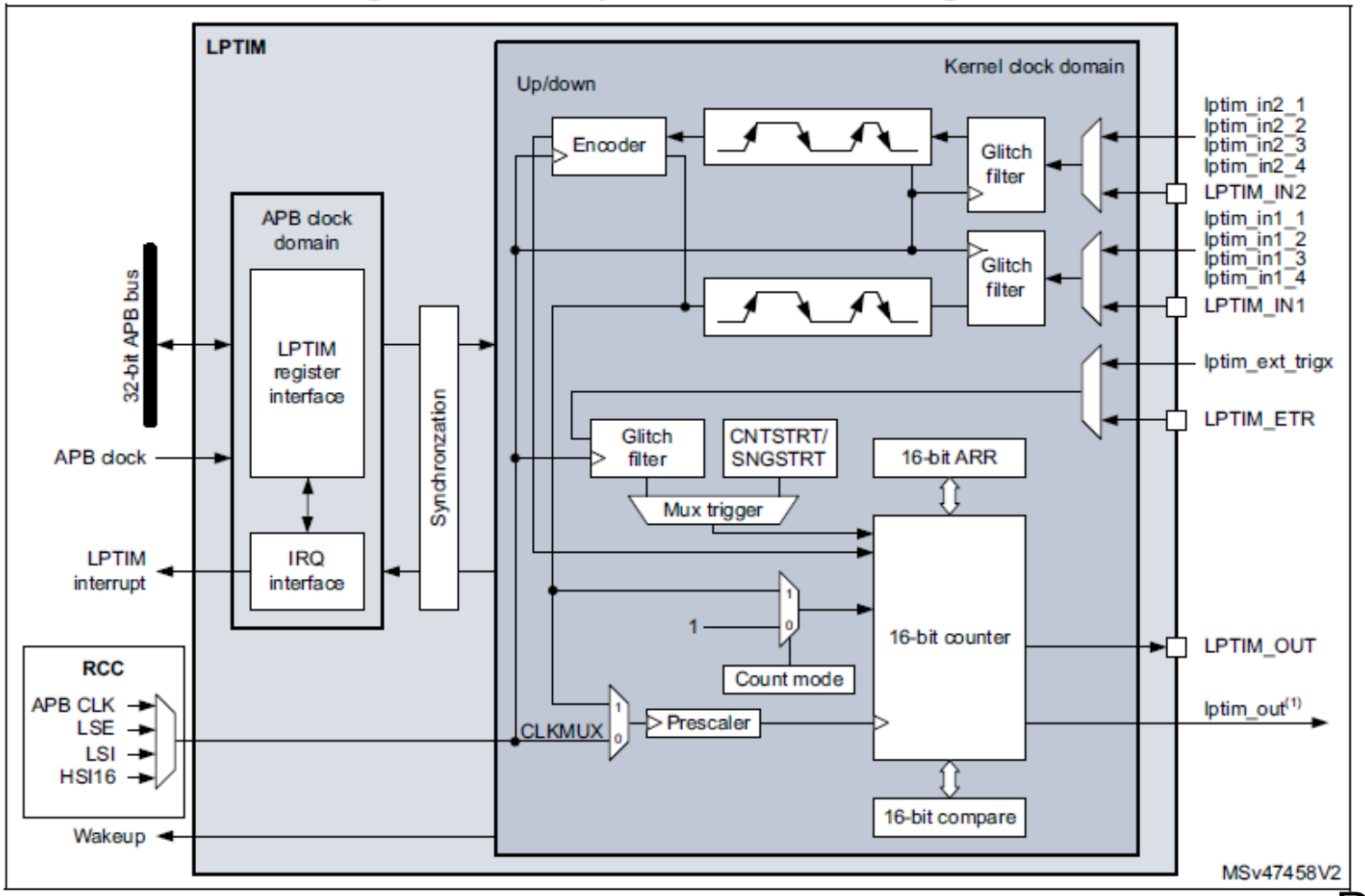
Časovnik z nizko porabo energije - LPTIM

Figure 494. Low-power timer block diagram



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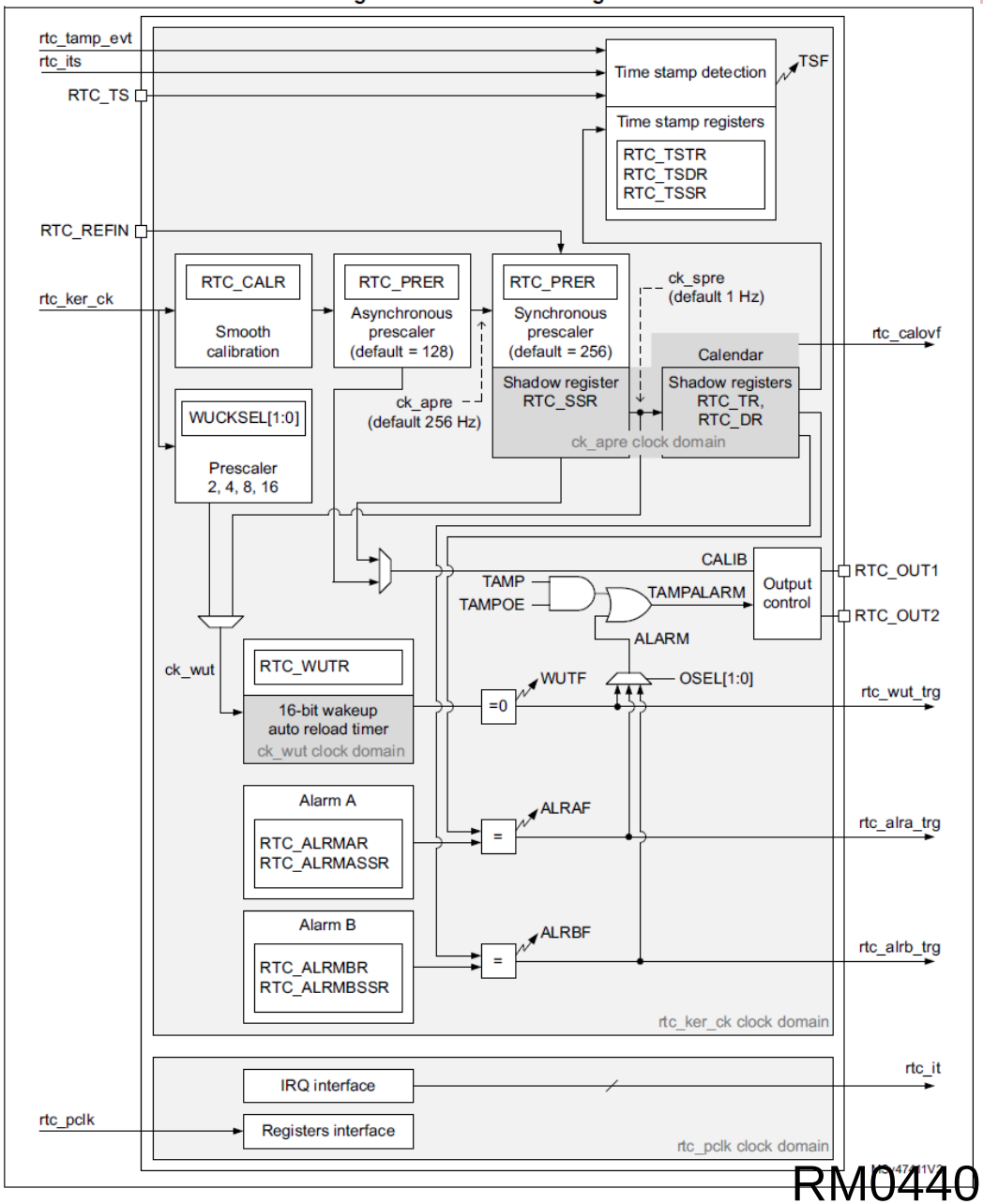
Ura realnega časa - RTC

Figure 529. RTC block diagram



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