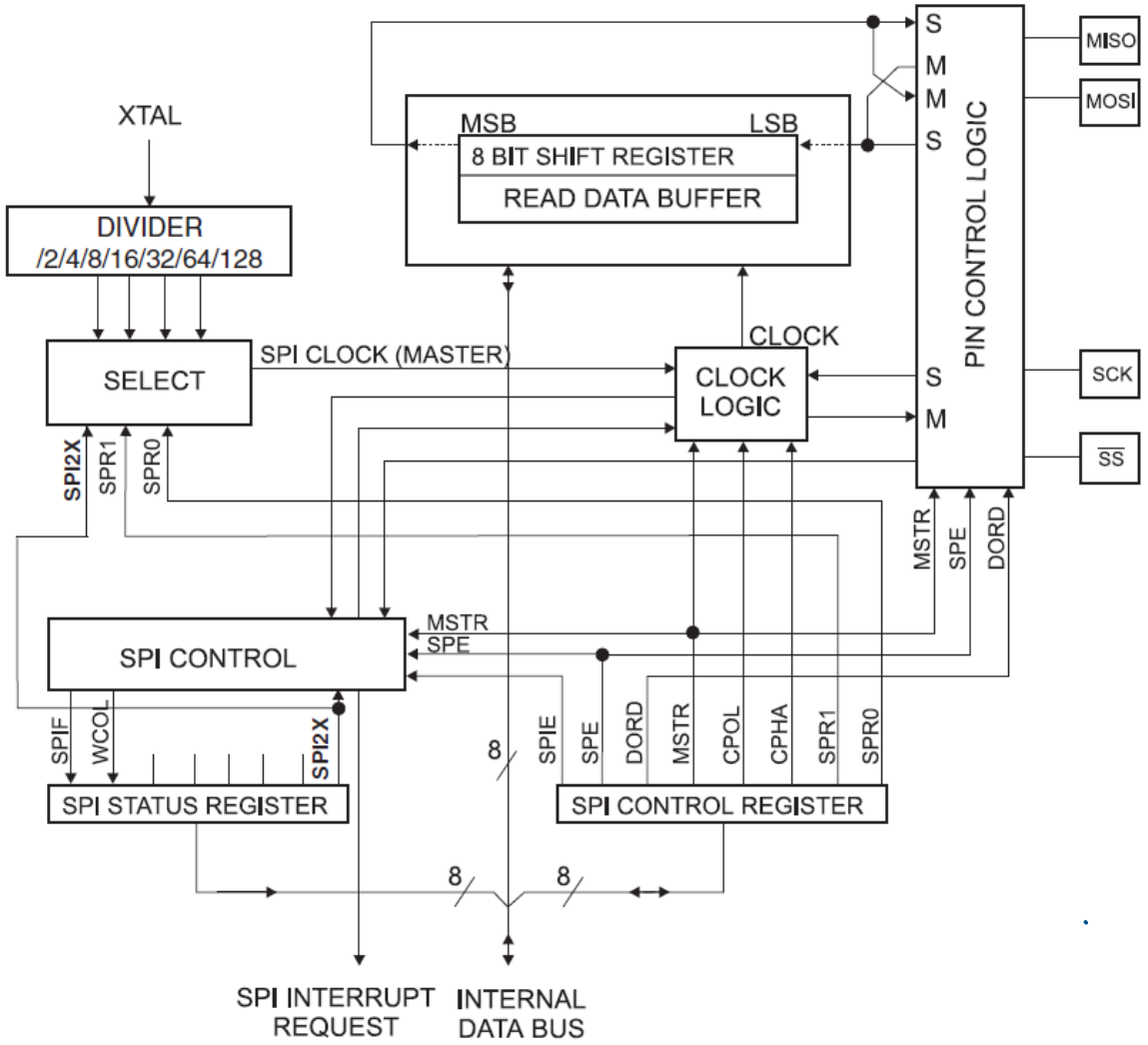
Osnove mikroprocesorske elektronike

Marko Jankovec

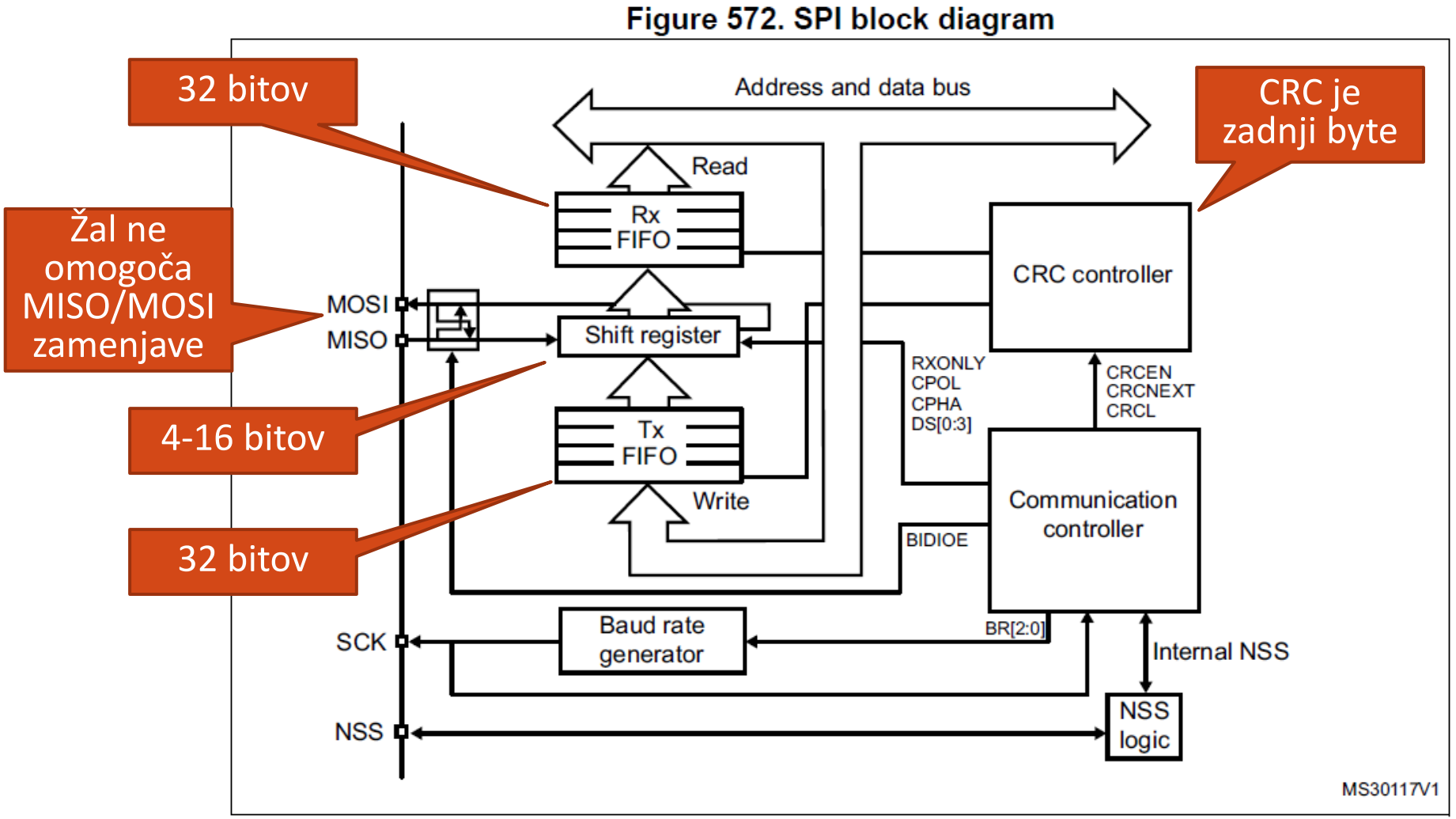
Sinhrona komunikacijska vodila

Primeri SPI

Vmesnik SPI pri AVR



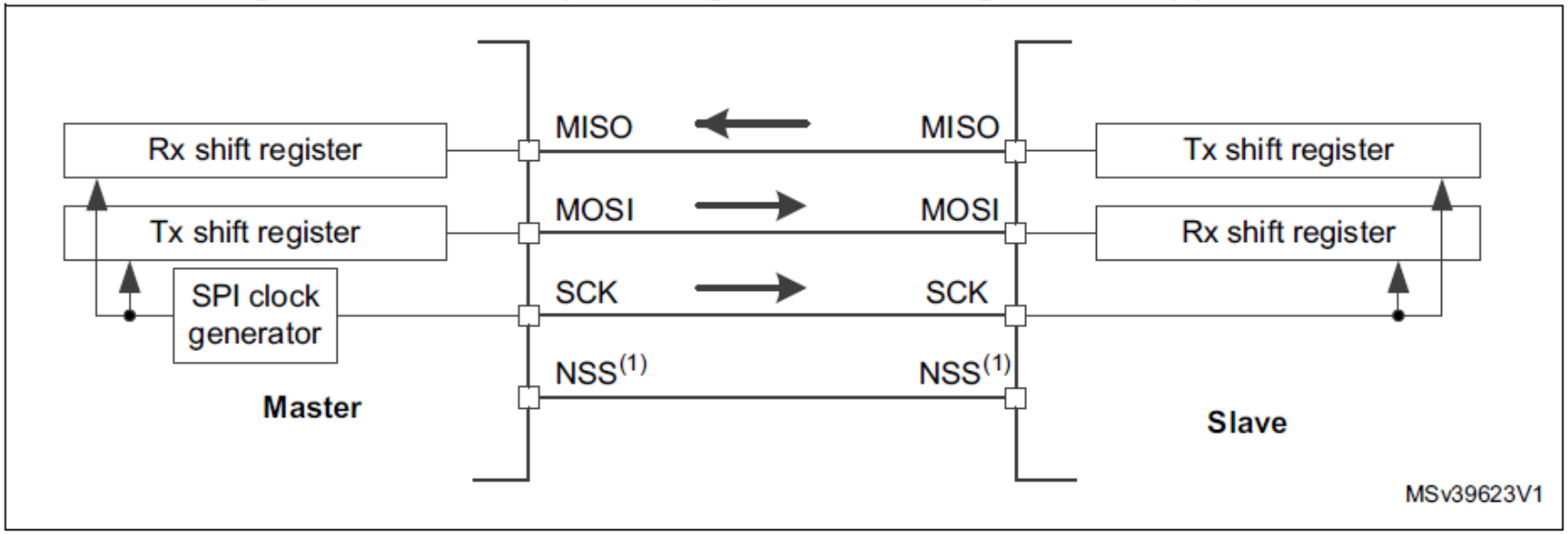
Vmesnik SPI pri STM32



RM0440

Full-duplex komunikacija

Figure 573. Full-duplex single master/ single slave application



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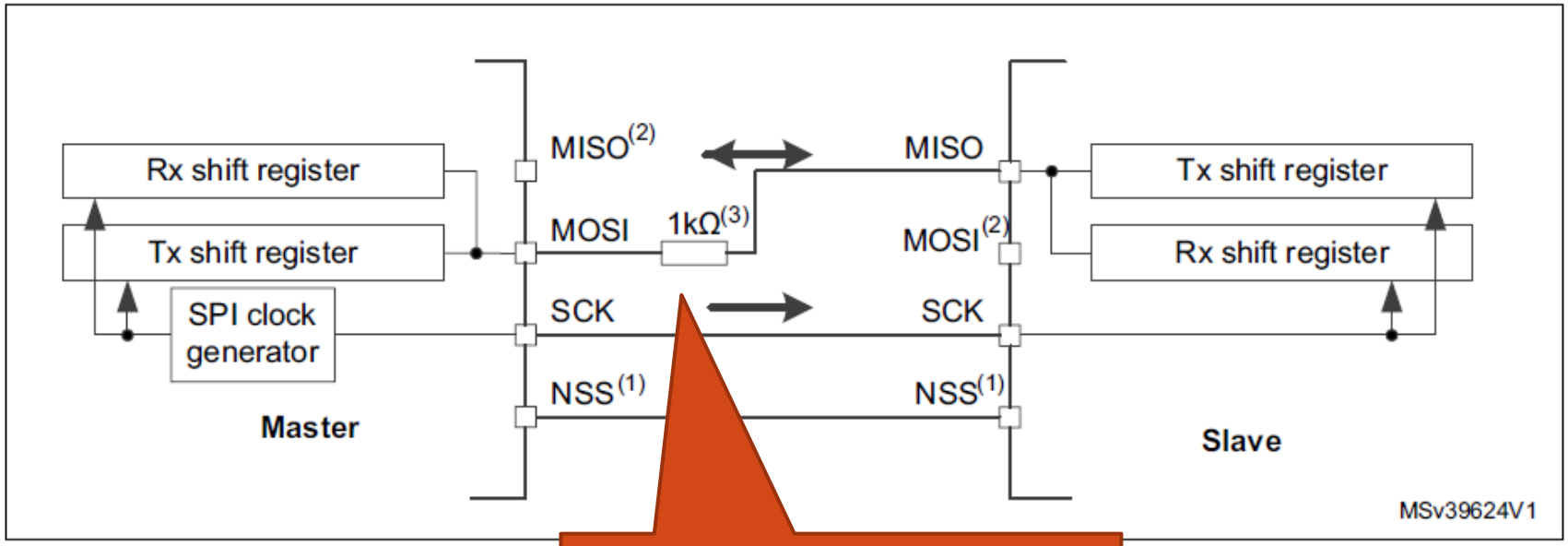
Half-duplex komunikacija

Figure 574. Half-duplex single master/ single slave application



Za primer, če bi kratek čas obe napravi dajali na vodilo

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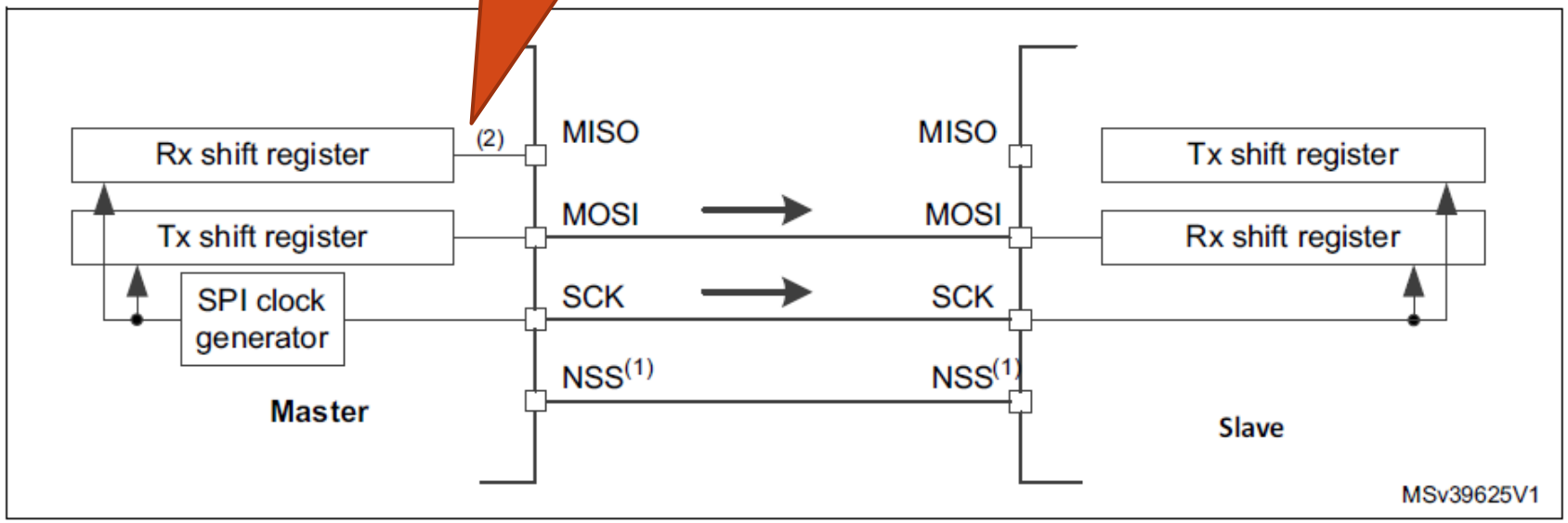
Simplex komunikacija

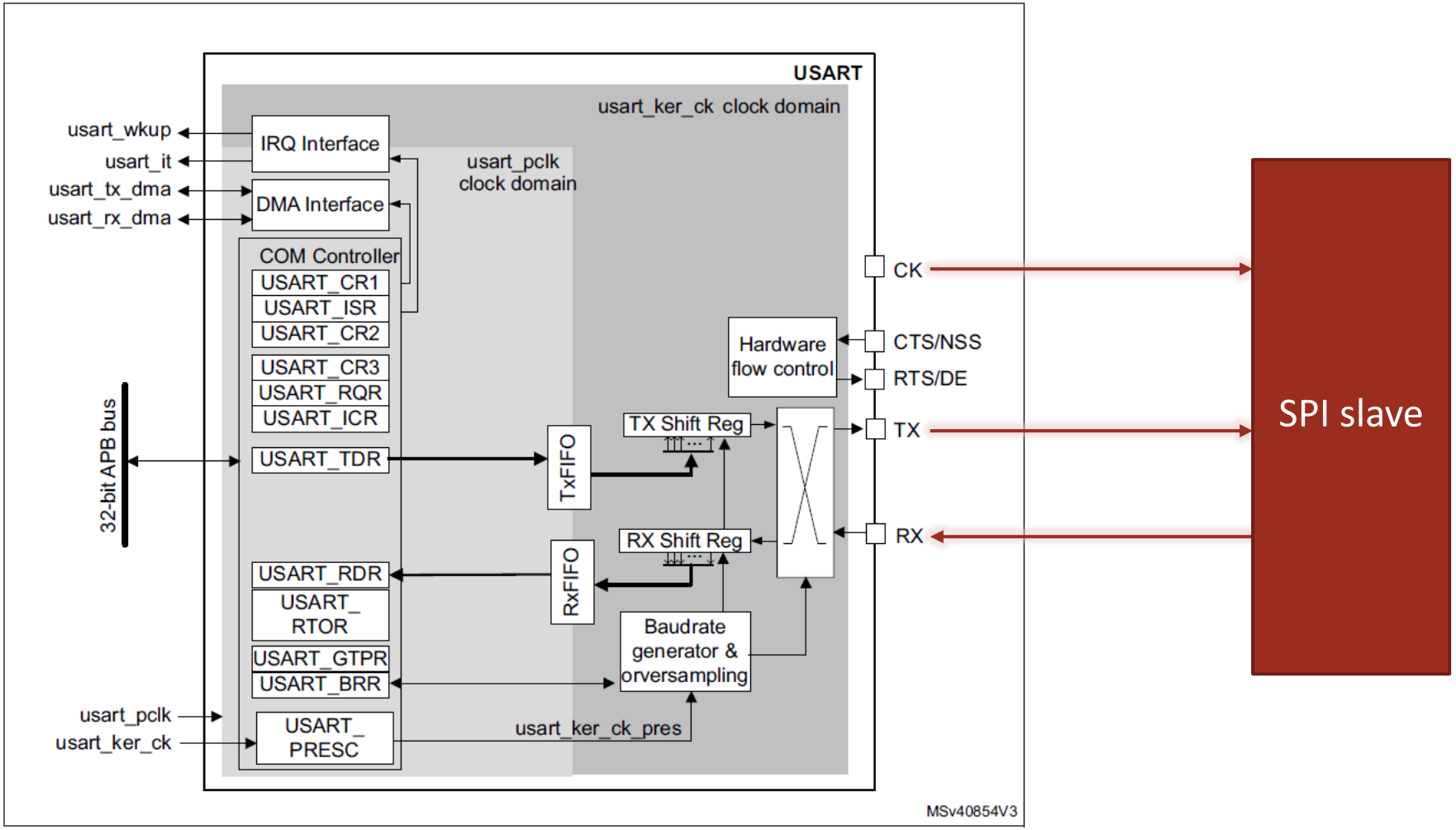
Sprejemnik sprejema nakljućen signal

Figure 575. Simplex singl ter/single slave application (master in transmit-only/ ave in receive-only mode)



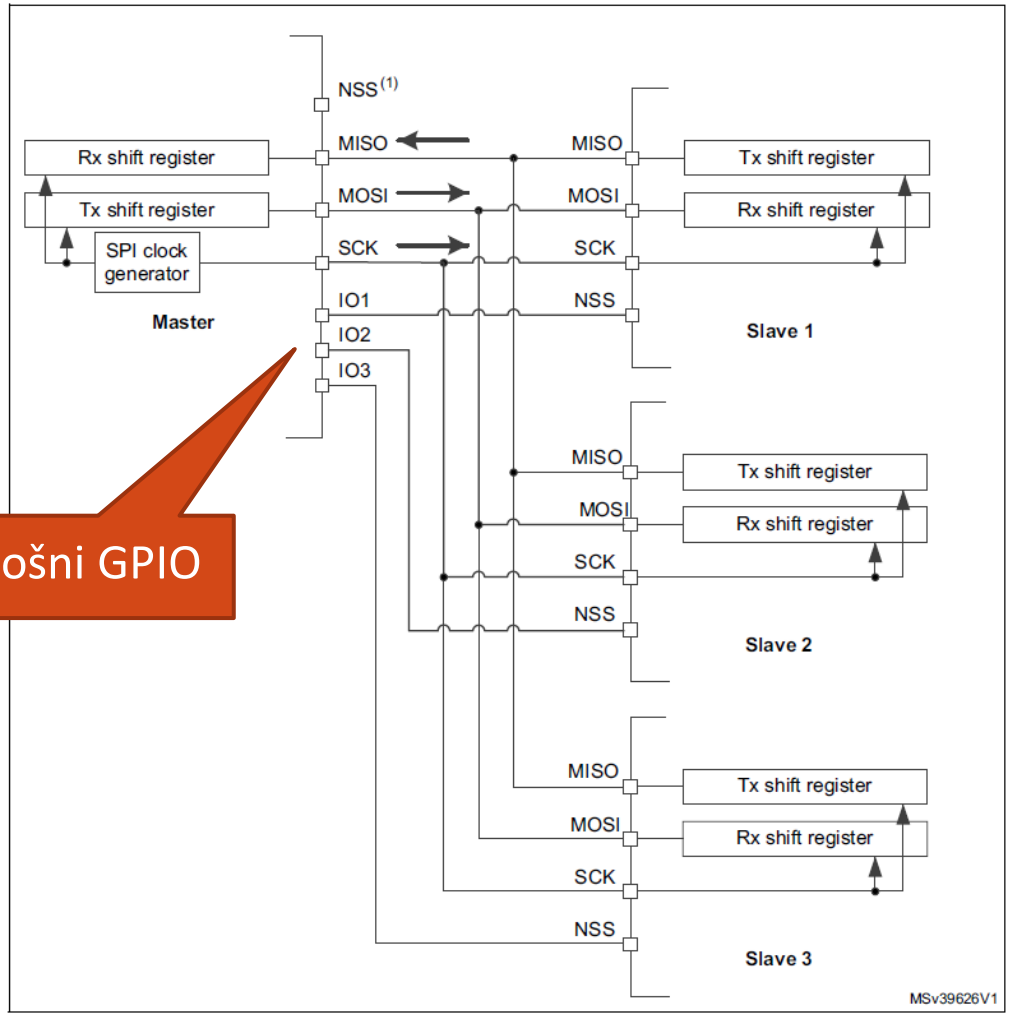
USART v sinhronem načinu

Figure 531. USART block diagram



Vzporedna vezava več naprav

Figure 576. Master and three independent slaves



Splošni GPIO

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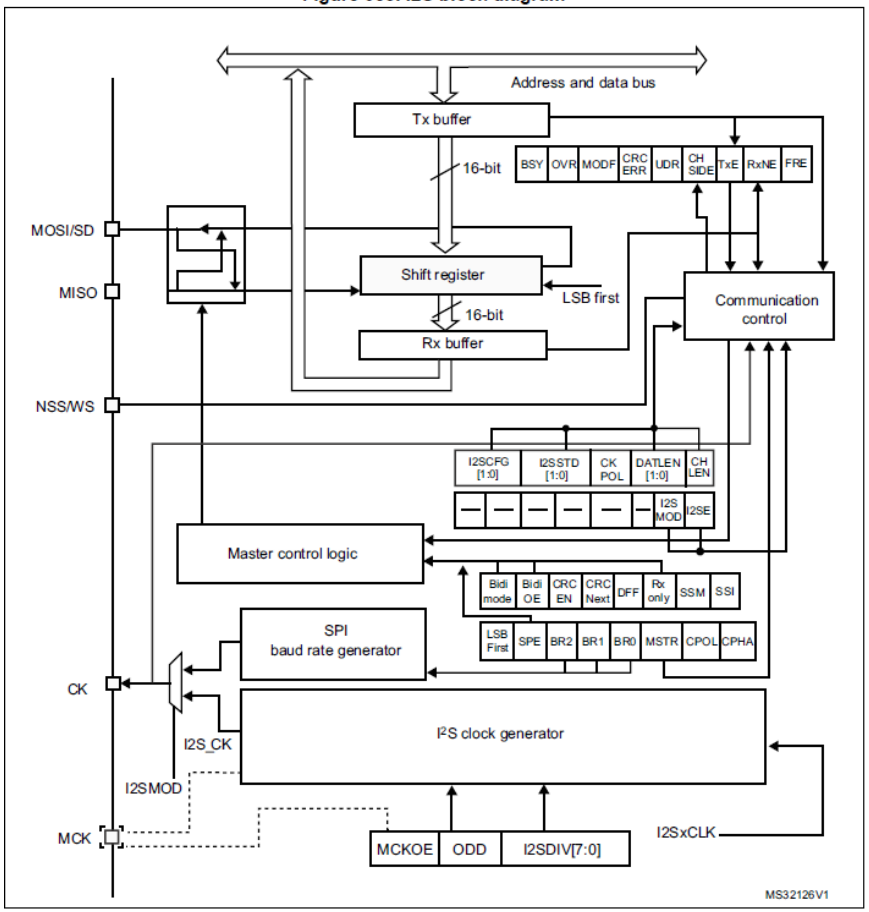
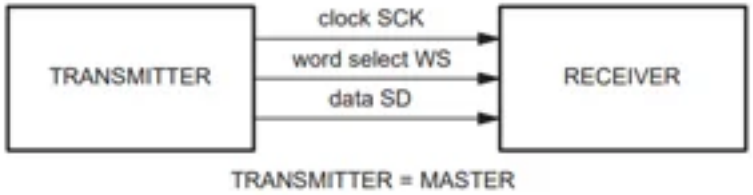
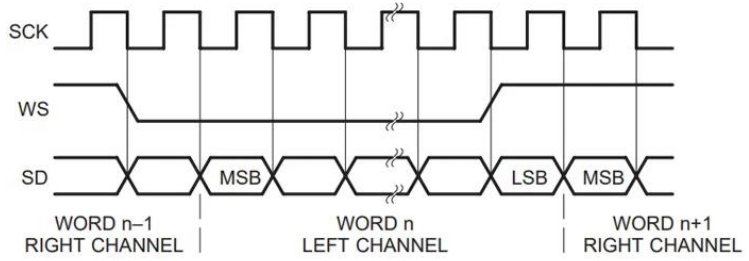
Vodilo I2S – Inter IC Sound protocol

Figure 588. I2S block diagram







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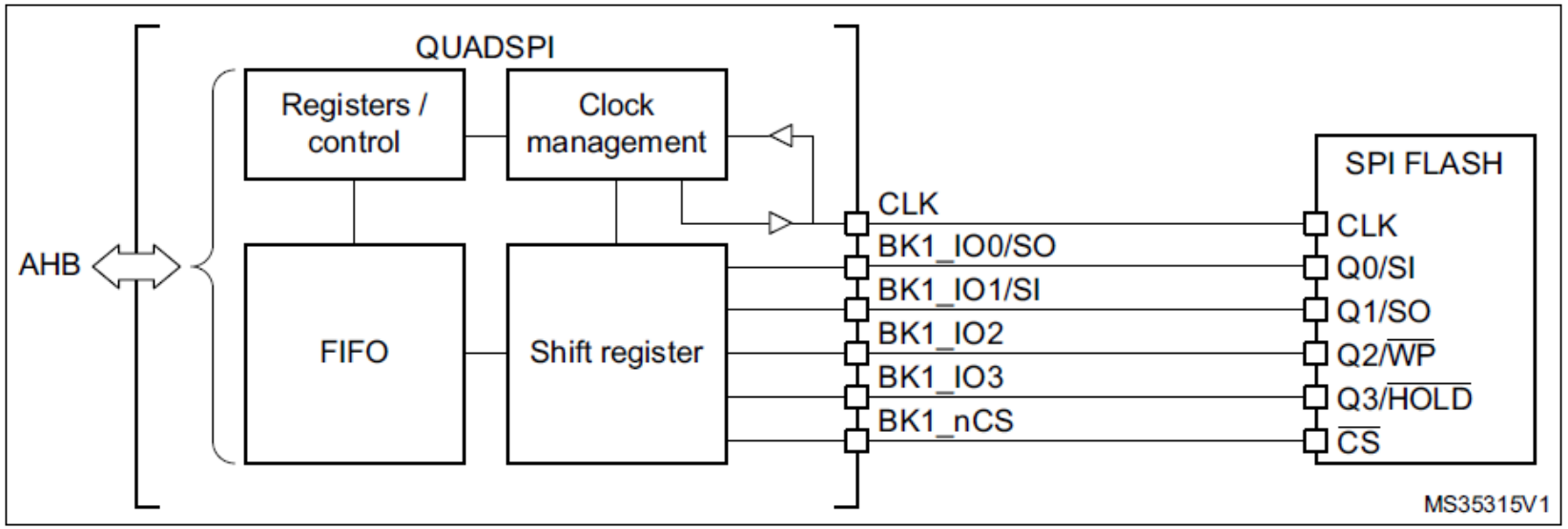
QUAD SPI

Figure 74. QUADSPI block diagram when dual-flash mode is disabled



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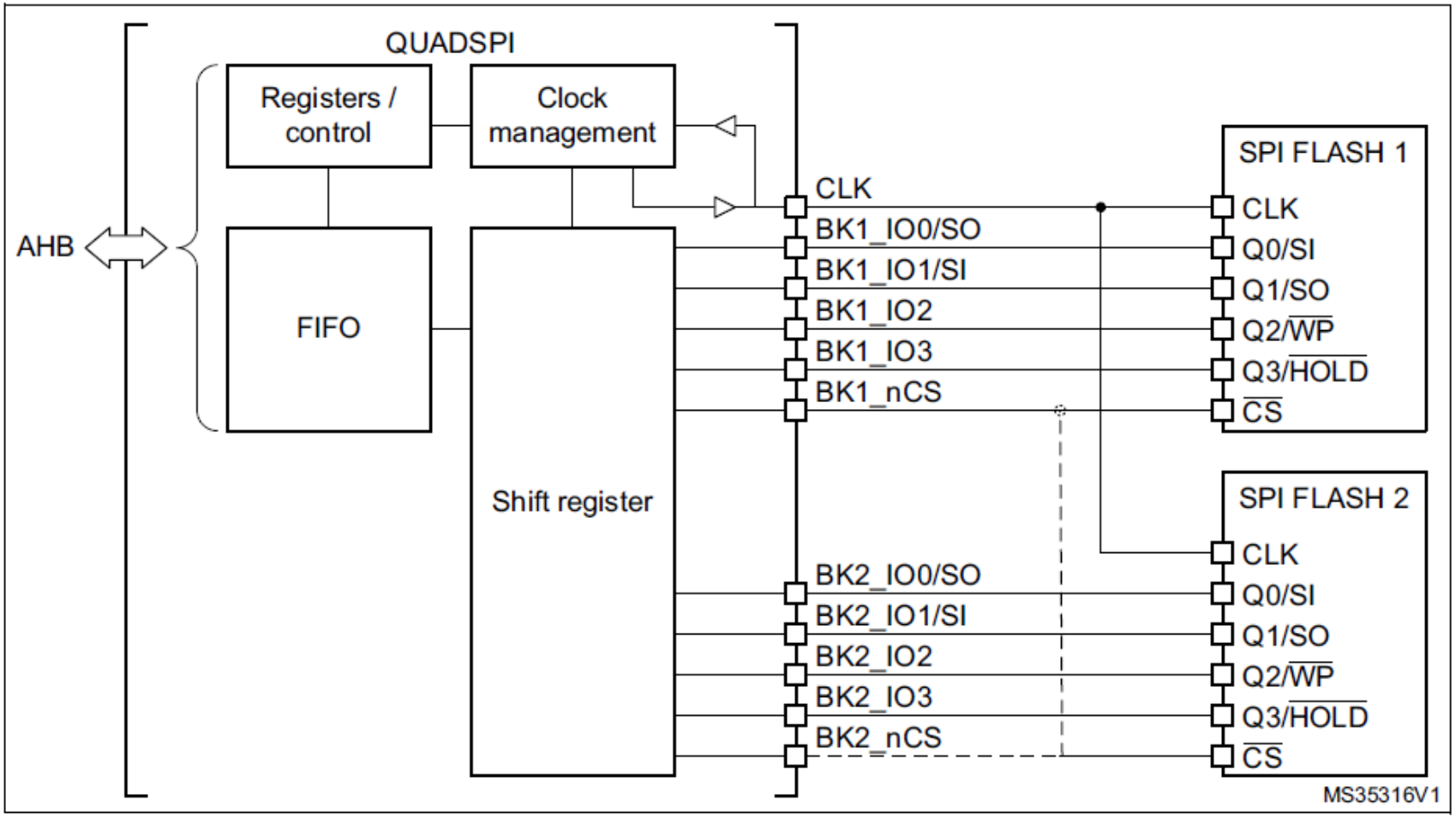
QUAD SPI

Figure 75. QUADSPI block diagram when dual-flash mode is enabled



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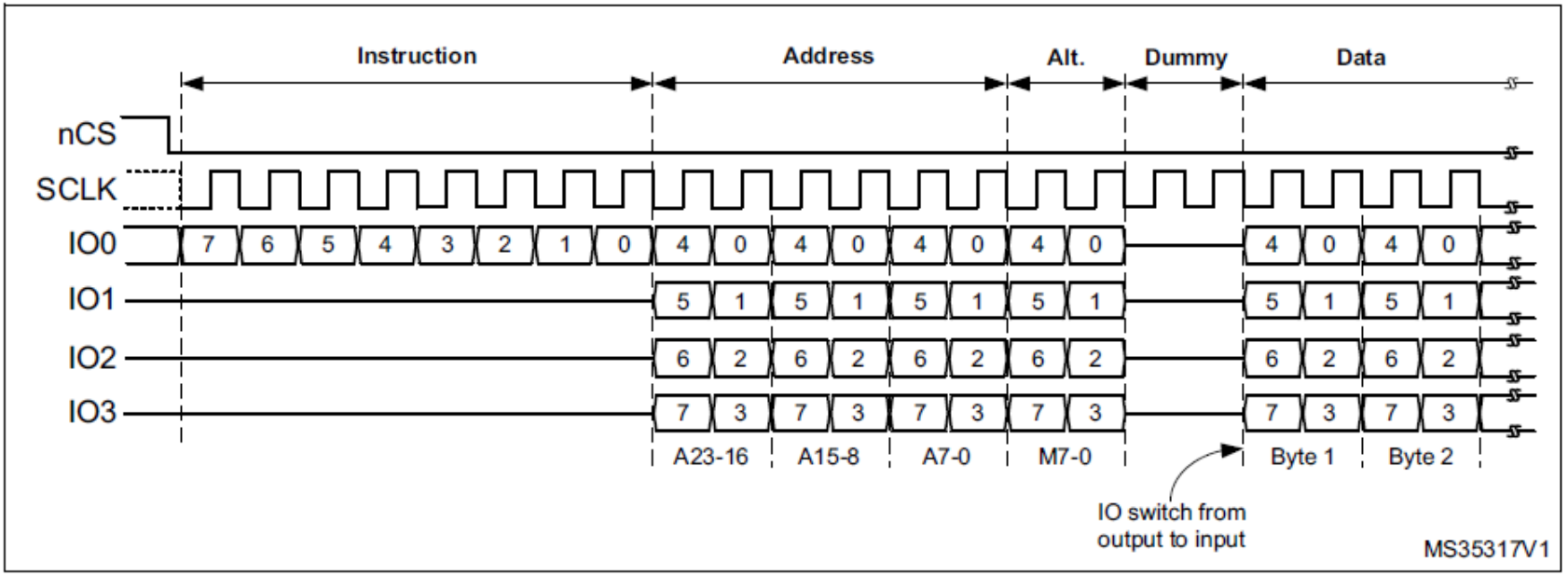
QUAD SPI

Figure 76. An example of a read command in quad mode



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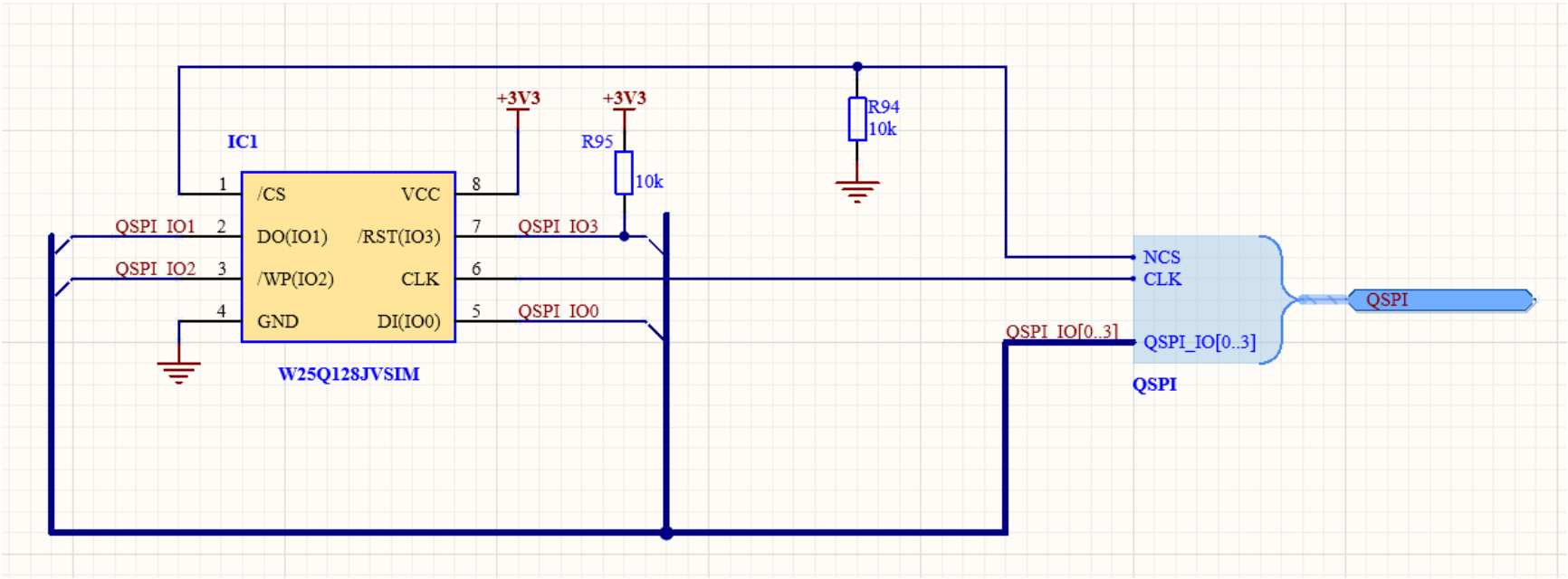
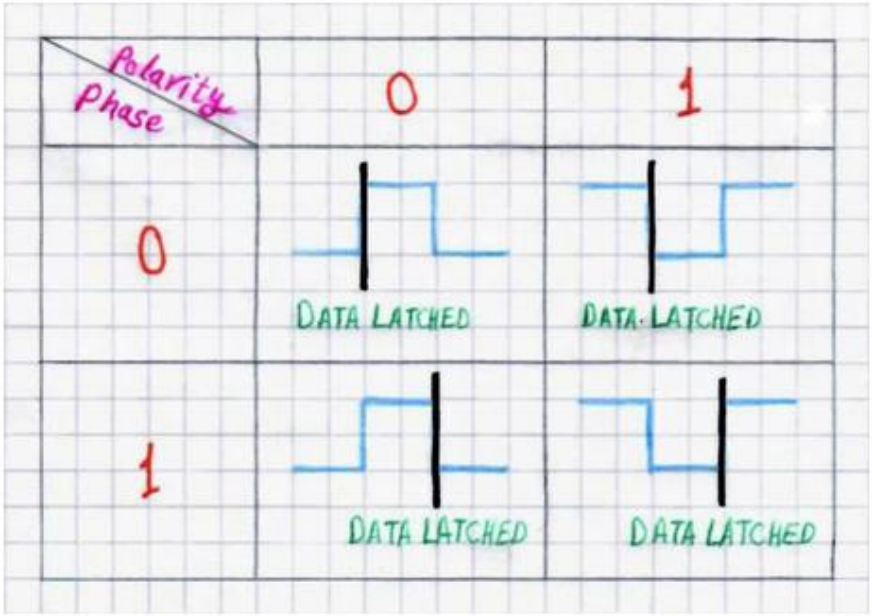
QUAD SPI pri MiŠKu 3



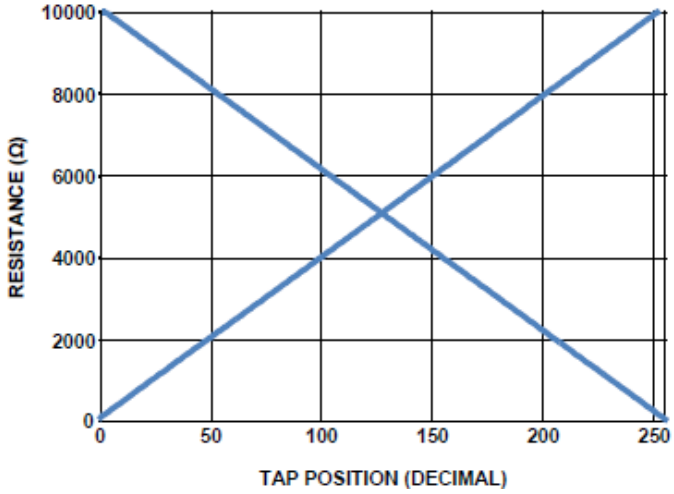
Možnost vodila SPI

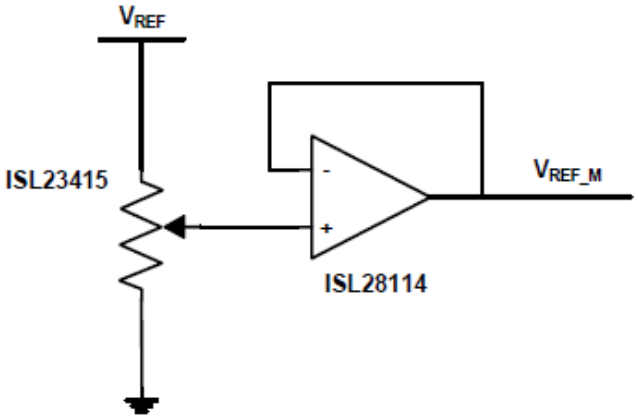


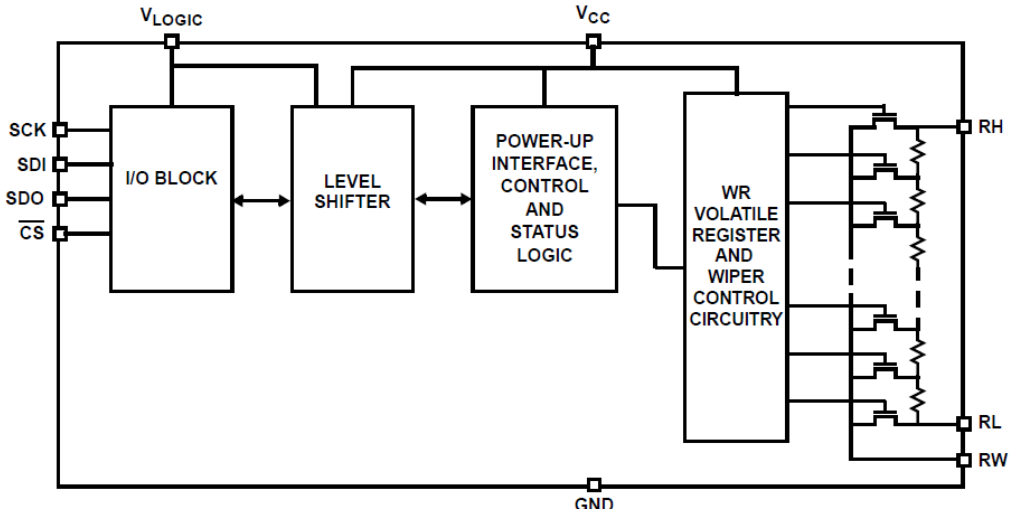
Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

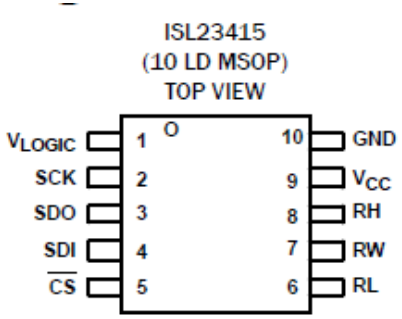
https://deepbluembedded.com/stm32-spi-tutorial/

Primer – digitalni potenciometer ISL23415

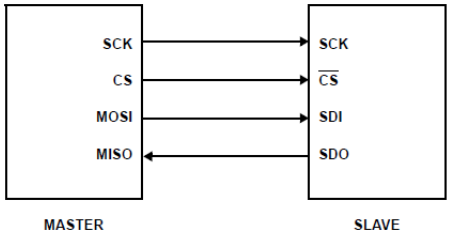




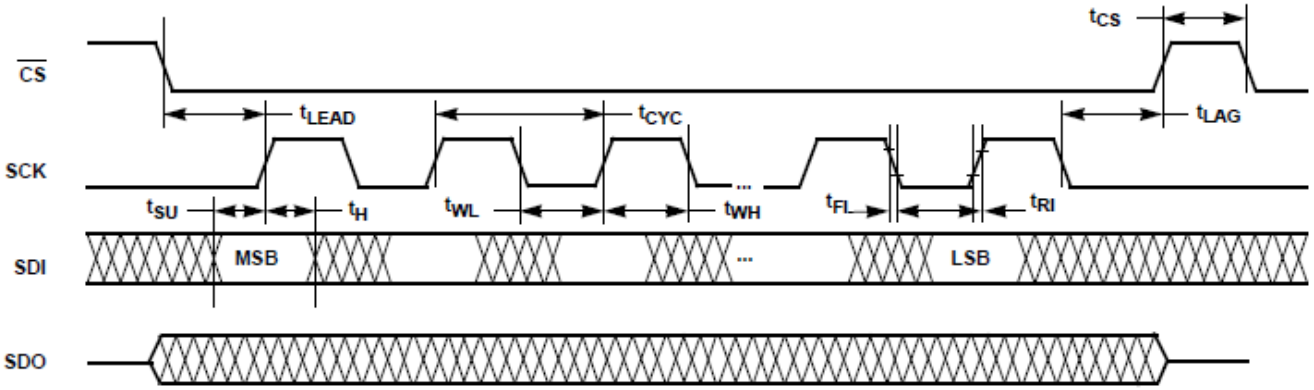




Vmesnik SPI pri ISL23415



Input Timing



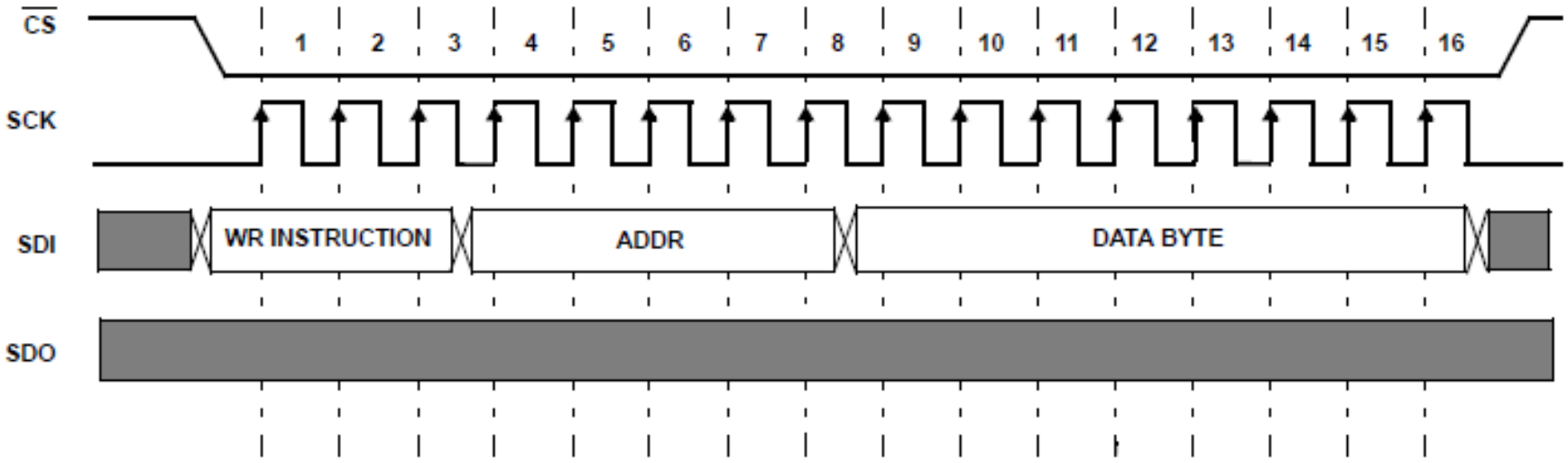
Param.	Vrednost
f_{sck}	5 MHz
t_{cyc}	200 ns
t_{wh}	100 ns
t_{wl}	100 ns
t_{LEAD}	250 ns
t_{LAG}	250 ns
t_{SU}	50 ns

SPI Serial Interface

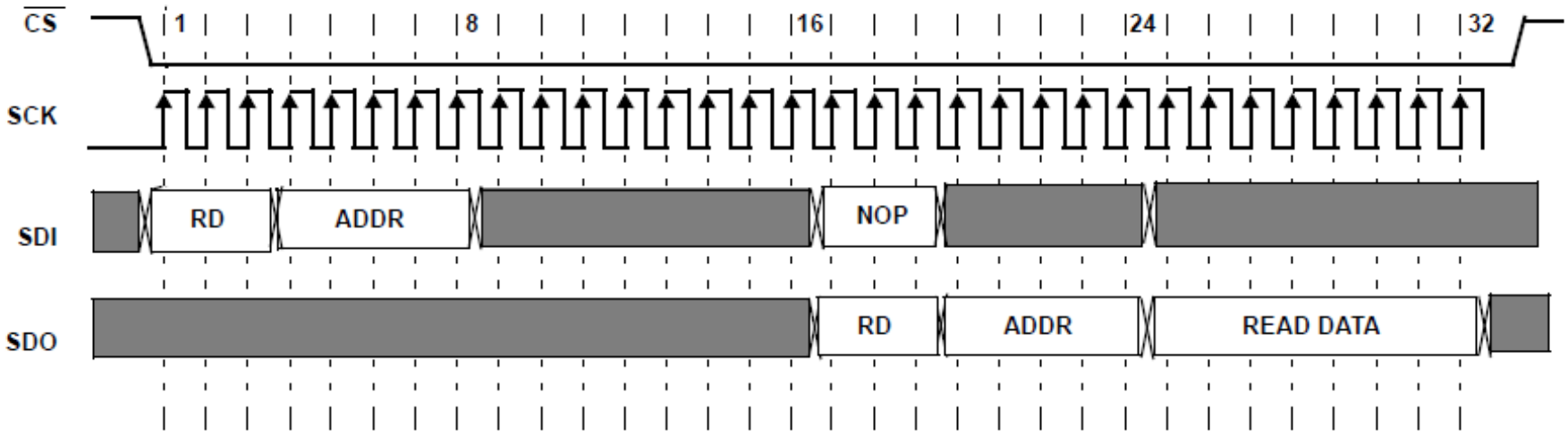
The ISL23415 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL23415. The SCK and $\overline{CS}$ lines are controlled by the host or master. The ISL23415 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Sekvenca pisanja podatka na ISL23415



Sekvenca branja podatka ISL23415



Ukazi in registri

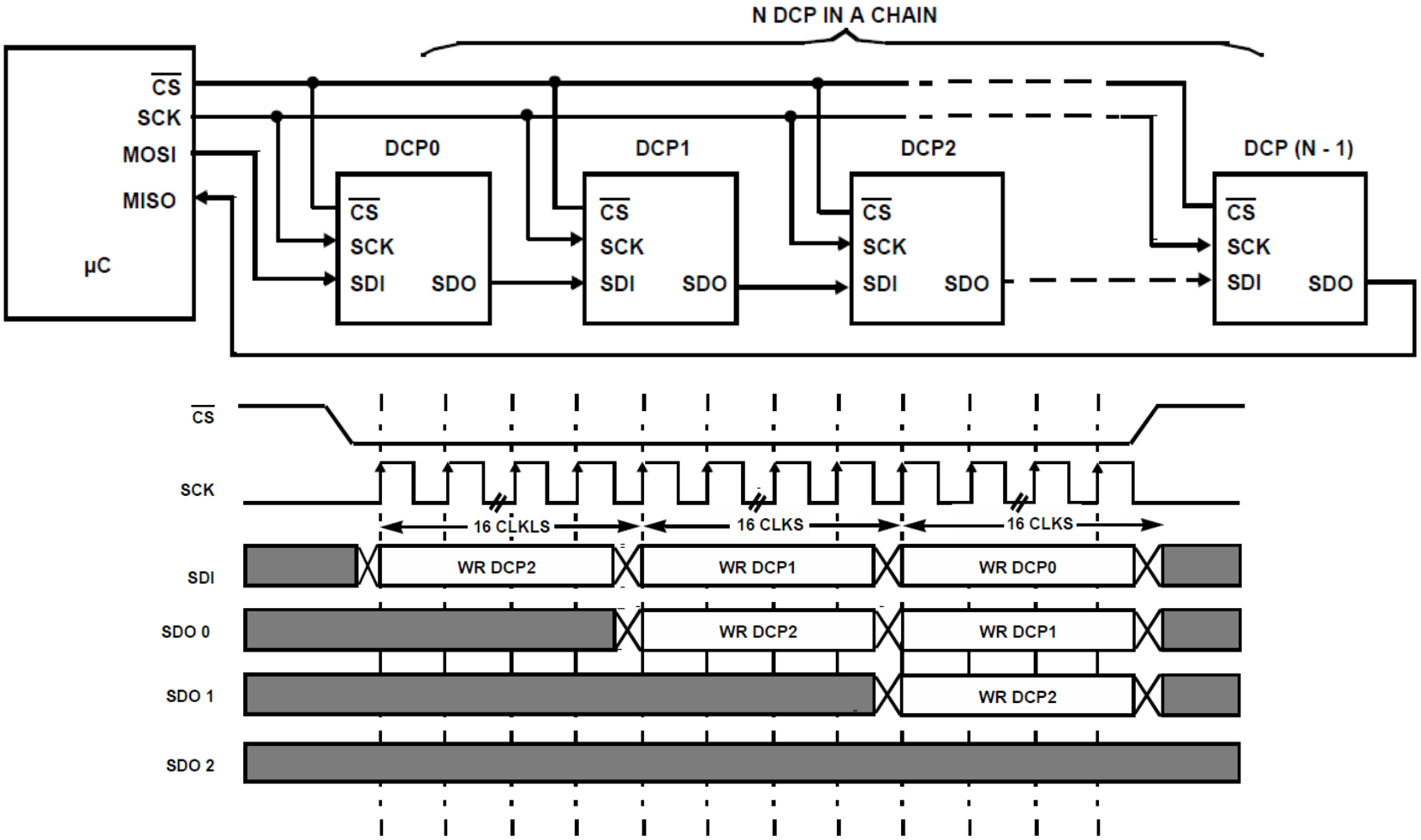
INSTRUCTION SET								
I2	I1	I0	R4	R3	R2	R1	R0	OPERATION
0	0	0	X	X	X	X	X	NOP
0	0	1	X	X	X	X	X	ACR READ
0	1	1	X	X	X	X	X	ACR WRTE
1	0	0	R4	R3	R2	R1	R0	WRi or ACR READ
1	1	0	R4	R3	R2	R1	R0	WRi or ACR WRTE

ADDRESS (hex)	VOLATILE	DEFAULT SETTING (hex)
10	ACR	40
0	WR	80

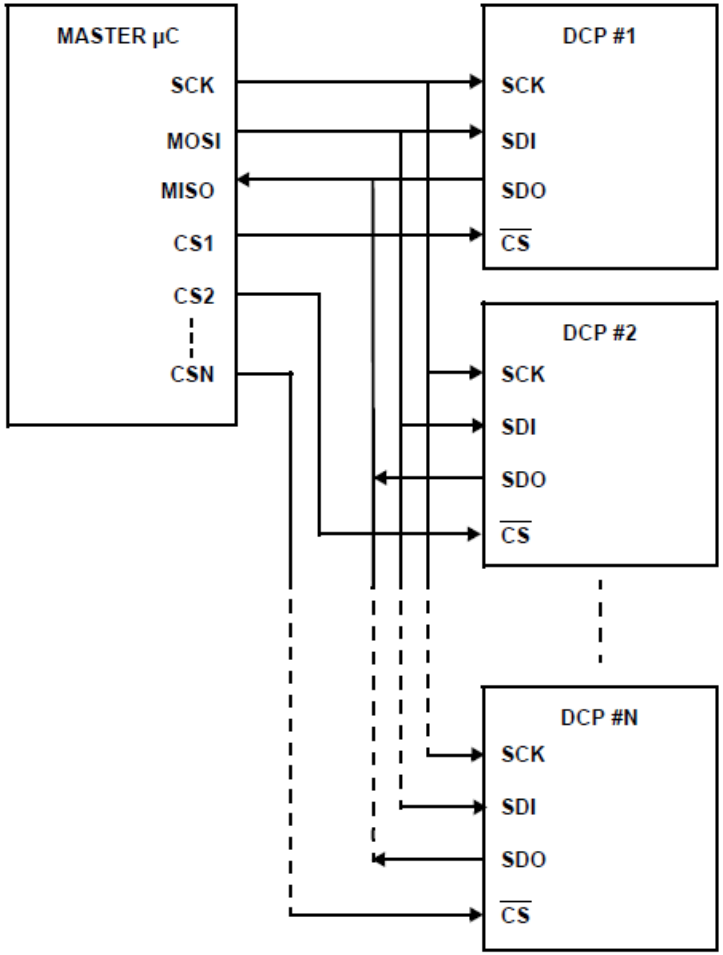
TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME	0	$\overline{\text{SHDN}}$	0	0	0	0	SDO	0

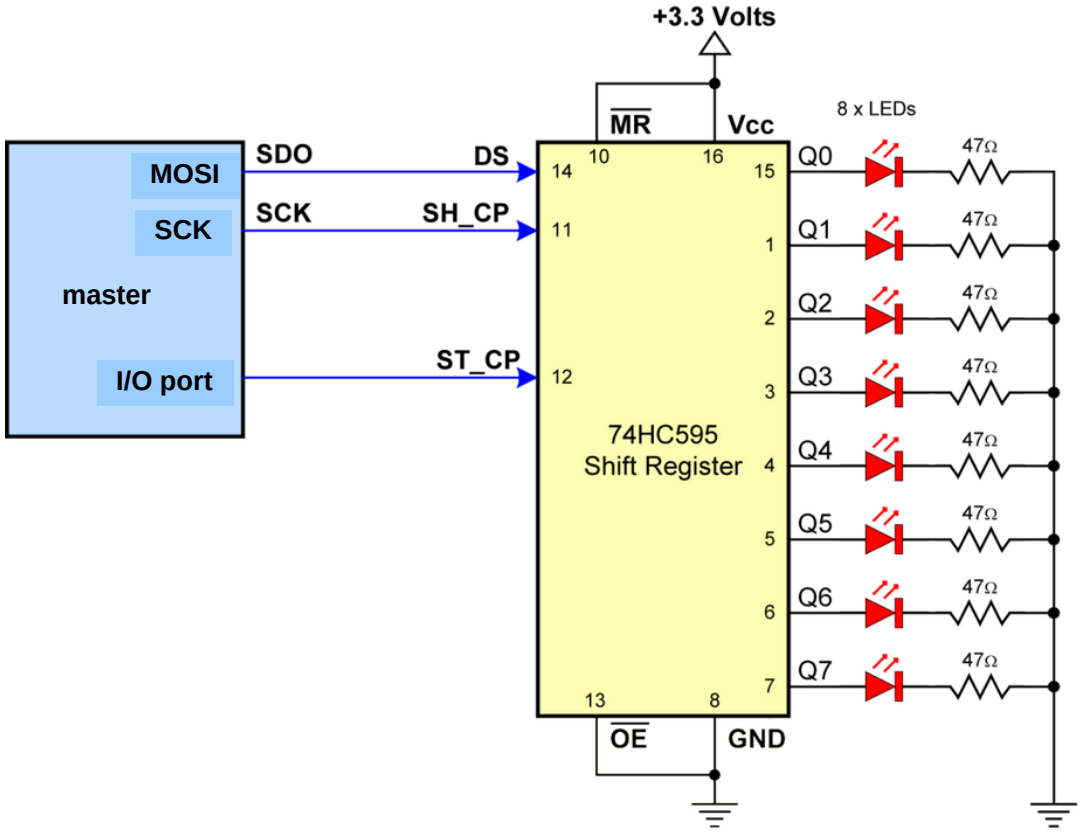
Zaporedna vezava več ISL23415



Vzporedna vezava več ISL23415



Primer razširitve I/O linij s pomikalnim registrom



Pin	Symbol	Description
1	Q1	Parallel data output (bit-1)
2	Q2	Parallel data output (bit-2)
3	Q3	Parallel data output (bit-3)
4	Q4	Parallel data output (bit-4)
5	Q5	Parallel data output (bit-5)
6	Q6	Parallel data output (bit-6)
7	Q7	Parallel data output (bit-7)
8	GND	Ground (0 V)
9	Q7`	Serial Data Output
10	$\overline{MR}$	Master Reset (Active Low)
11	SH_CP	Shift Register Clock Input
12	ST_CP	Storage Register Clock Input
13	$\overline{OE}$	Output Enable (Active Low)
14	DS	Serial Data Input
15	Q0	Parallel data output (bit-8)
16	Vcc	Positive Supply Voltage