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HW3

4.19.5

In the exercise, we examine in detail how an instruction is executed in single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word: `0x00c6ba23`.
For context: The encoded instruction is `sw x12, 20(x13)`

A. What are the values of the ALU control unit's inputs for this instruction?

    Op: 0100011
    Funct3: 010
    Imm: 0000000

B. What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

    PC + 4

C. For each mux, show the values of its inputs and outputs during the execution of this instruction. List values that are register outputs at `Reg [xn]`

    PC Source Mux:
        Input 0: PC + 4
        Input 1: N/A
        Output: PC + 4
    ALU Source Mux:
        Input 0: 20
        Input 1: x13
        Output: x13
    Memory Write Data Mux:
        Input 0: x12
        Input 1: N/A
        Output: x12
    Register Write Data Mux:
        Input 0: N/A
        Input 1: N/A
        Output: N/A

D. What are the input values for the ALU and the two add units?

ALU:
Input 1: x13
Input 2: 20

Add 1:
Input 1: x13
Input 2: 20

Add 2:
Input 1: PC + 4
Input 2: 4

E. What are the values of all inputs for the registers unit?

Register Read Data 1: x12
Register Read Data 2: x13
Write Register: N/A
Write Data: memory address for operation

4.19.6

COD Section 4.4 does not discuss I-type instructions like `addi` or `andi`

B. List the values of the signals generated by the control unit for `addi`. Explain the reasoning for any "don't care" control signals.

Reg2Loc = 0: Read register 2 gets value from instruction
Uncondbranch = 0: Not applicable
Branch = 0: Not a branch instruction
MemRead = 0: No memory read operation
MemtoReg = 0: The ALU result is selected
ALUOp = 00: Specifies the ALU operation
MemWrite = 0: No memory write operation
ALUSrc = 1: Second input comes from sign-extended immediate
RegWrite = 1: Register write operation