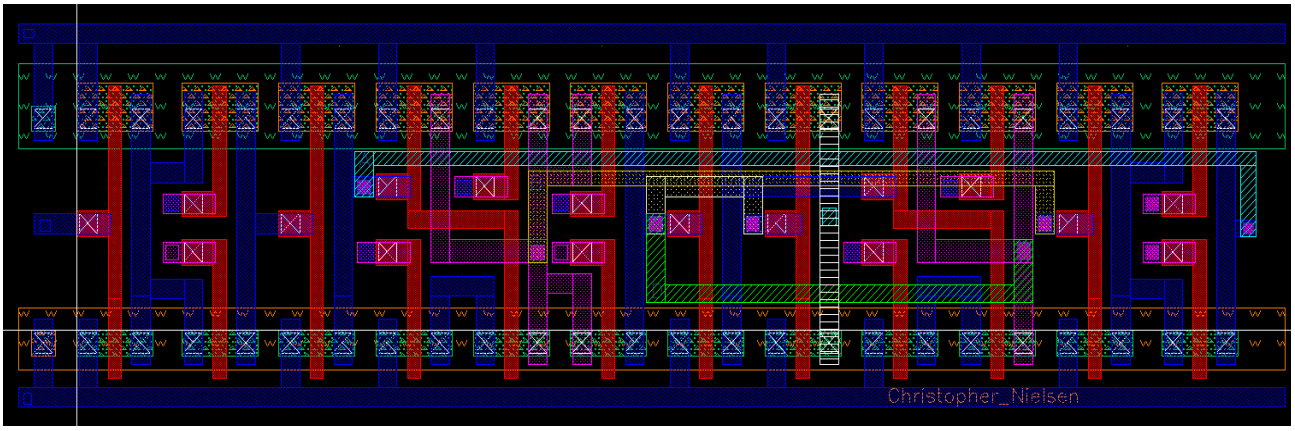
DFF CMOS Design Project - 2022

45nm CMOS D Flip Flop - Fall of 2022 at Stony Brook University



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11.10.2022

Sophomore Year - Audited Graduate Course ESE 555 - Advanced VLSI Design

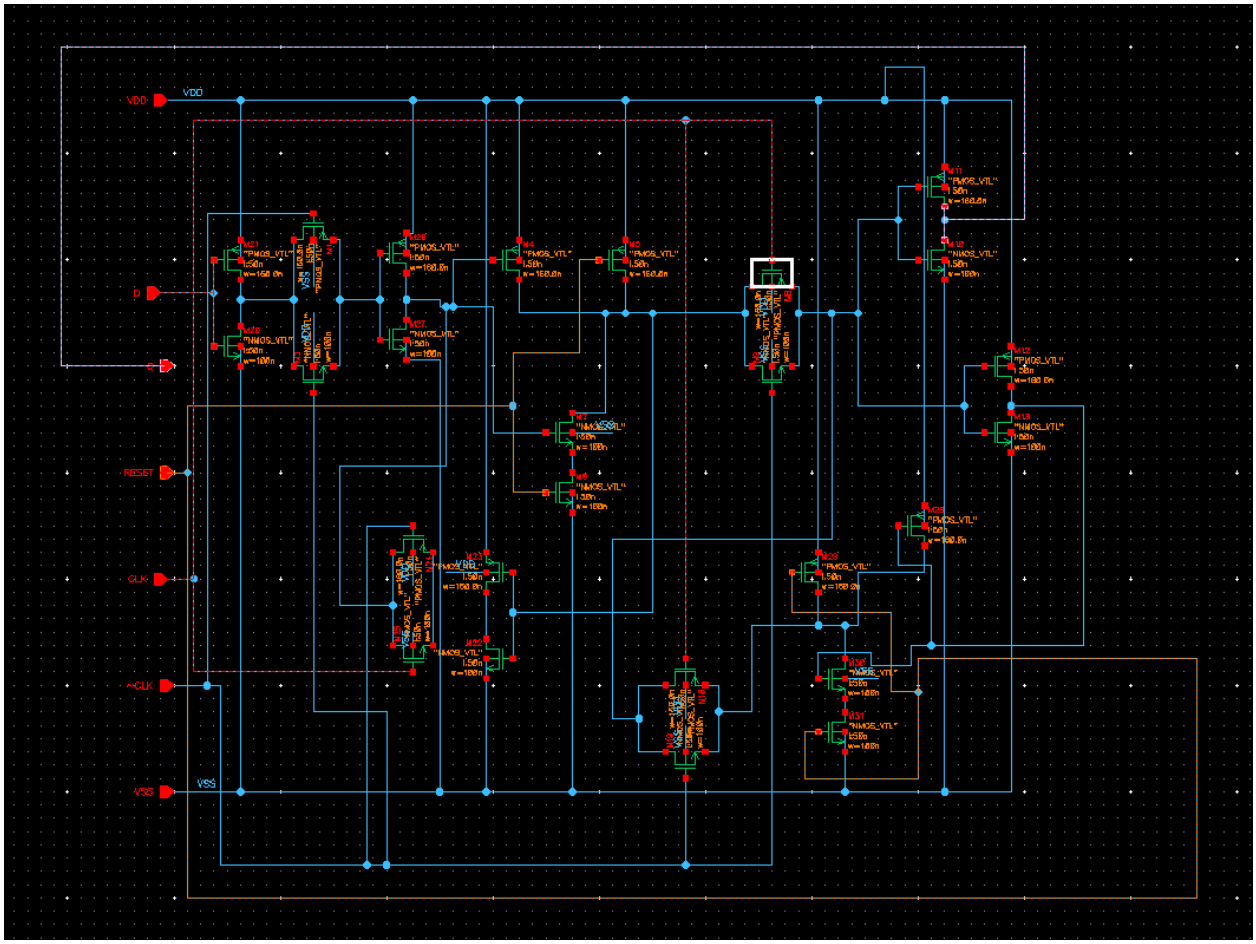
Restrictions/Assignment Details

Design and verify a CMOS positive (rising) edge triggered D-type flip-flop with an asynchronous reset (active at logic high) using 45 nm static CMOS technology. Flip-flop should have three inputs (data, clock, and reset) and one output (Q). The supply voltage is set to 1.1 Volts. The flip-flop should drive an external load of 5 fF in addition to the internal parasitic capacitances that exist at the output stage. Assume 20 ps of rise/fall times for the data and clock signals. Assume 50% duty cycle for both signals. Both signals should be periodic

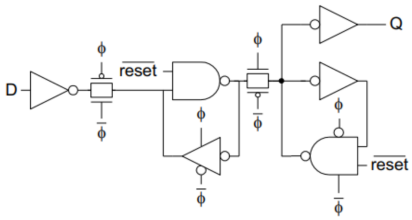
Libraries/Software

1. NCSU Cadence design kit (CDK)
2. Process design kit (PDK)
3. NCSU_TechLib_FreePDK45
4. ADE SPECTRE (Using HSPICE (From Synopsys) model libraries for 45nm CMOS Technology)
5. Calibre (Mentor Graphics)

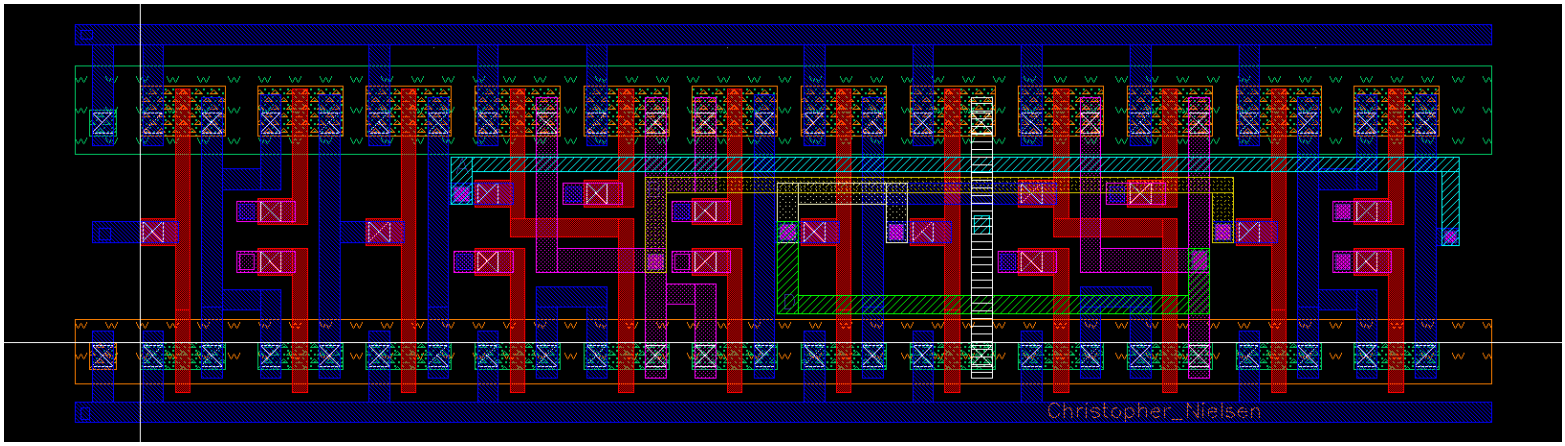
Schematic:



The schematic (above) is the gate level implementation of the shown DFF circuit model, except with the transmission gates separated from their components. For example any and all TRI-STATE components were modeled with an appropriately oriented transmission gate instead, for both workability, and clarity on my part while designing, and for the professor.

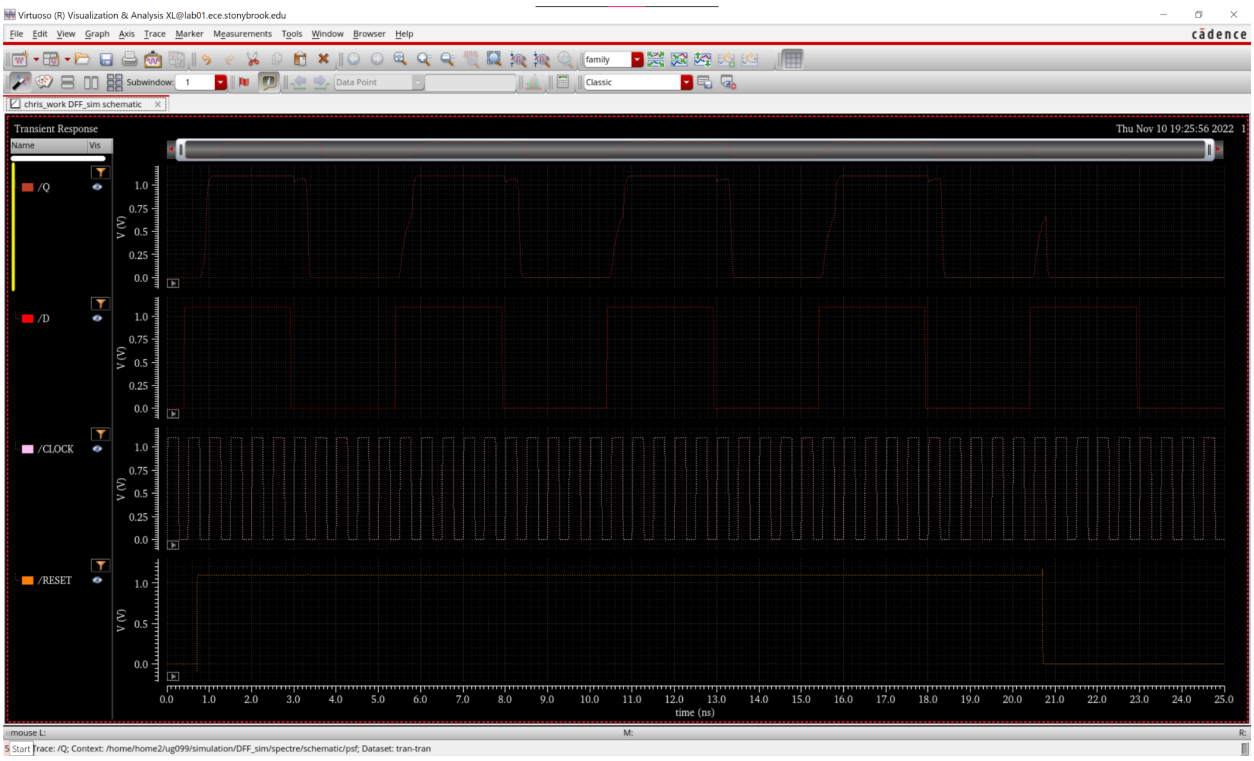


Layout

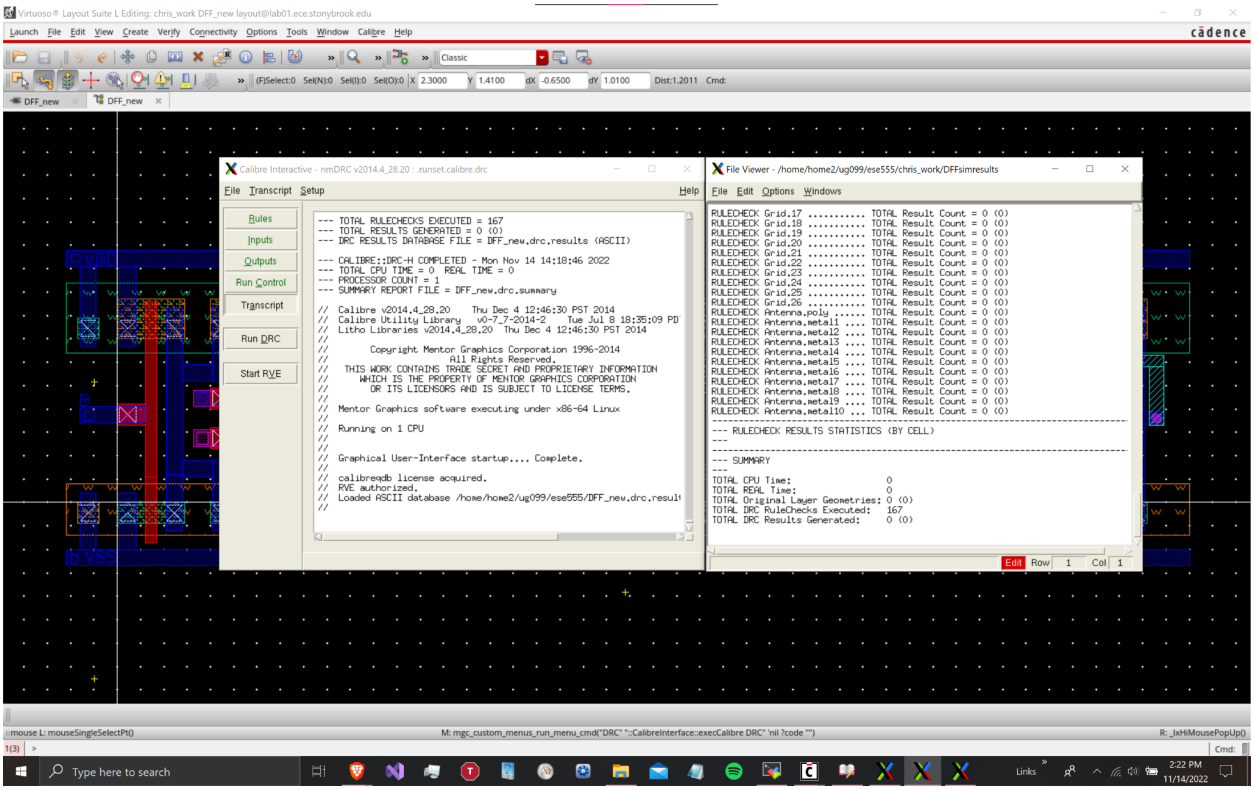


The layout (shown above) was completed in Cadence and passed all library based tests in the course (ESE555) during Fall of 2022 at Stony Brook University. It is the CMOS VLSI implementation of the above simulated DFF Schematic. Data is entered on the PIN all the way on the left hand side of the schematic. At various points CLK, CLKB, and RESET are fed into the design, and by following data path flow these pins can be recognized. (CADENCE export software excludes these pin labels). At the center of the layout Q can be read from the light colored metal layer (Light Blue PIN on Light Gray Metal). This finalized layout took nearly 10 hours of research/planning, 3 design iterations, and 5 hours of in lab work to build properly within Cadence.

Waveforms (ADE L)/ Passes (nmDRC)



The above waveform shows the proper operation of the negative asserted reset, and data update/propagation of D through to Q (Waveforms labeled on LEFT HAND SIDE). The test ran for 25 ns. At the 21ns mark a failure for D to make its way through to Q is viewable.



The below report outlines the results and parameters of the project. The tests were run on a LINUX machine via a remote login from my Macbook (Within Windows). This explains the UI/Operating System Inconsistencies.

For clarity: My work was based within < home/home2/ug099/ese555/chris_work/ > at the time of simulation/testing and the schematic was named “DFF_new” and simulated as a workable part within a “DFF_sim” cell view.

(The whole output file given by DRC-H)

==================== CALIBRE::DRC-H SUMMARY REPORT================

Execution Date/Time: Mon Nov 14 14:18:46 2022

Calibre Version: v2014.4_28.20 Thu Dec 4 12:46:29 PST 2014

Rule File Pathname: /home/home2/ug099/ese555/_calibreDRC.rul_

Rule File Title:

Layout System: GDS

Layout Path(s): DFF_new.calibre.db

Layout Primary Cell: DFF_new

Current Directory: /home/home2/ug099/ese555

User Name: ug099

Maximum Results/RuleCheck: 1000

Maximum Result Vertices: 4096

DRC Results Database: DFF_new.drc.results (ASCII)

Layout Depth: ALL

Text Depth: PRIMARY

Summary Report File: DFF_new.drc.summary (REPLACE)

Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO

NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO

Excluded Cells:

CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION

Layers: MEMORY-BASED

Keep Empty Checks: YES

---------- RUNTIME WARNINGS---------- ORIGINAL LAYER STATISTICS---

LAYER pwell ..... TOTAL Original Geometry Count = 0 (0)

LAYER nwell ..... TOTAL Original Geometry Count = 0 (0)

LAYER active ..... TOTAL Original Geometry Count = 0 (0)

LAYER poly ..... TOTAL Original Geometry Count = 0 (0)

LAYER pimplant ... TOTAL Original Geometry Count = 0 (0)

LAYER nimplant ... TOTAL Original Geometry Count = 0 (0)

LAYER vth ..... TOTAL Original Geometry Count = 0 (0)

LAYER vtg ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal1 ..... TOTAL Original Geometry Count = 0 (0)

LAYER contact .... TOTAL Original Geometry Count = 0 (0)

LAYER metal2 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal3 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal4 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal5 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal6 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal7 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal8 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal9 ..... TOTAL Original Geometry Count = 0 (0)

LAYER metal10 .... TOTAL Original Geometry Count = 0 (0)

LAYER via1 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via2 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via3 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via4 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via5 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via6 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via7 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via8 ..... TOTAL Original Geometry Count = 0 (0)

LAYER via9 ..... TOTAL Original Geometry Count = 0 (0)

---------- RULECHECK RESULTS STATISTICS

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RULECHECK Implant.6 ..... TOTAL Result Count = 0 (0)

RULECHECK Contact.1 ..... TOTAL Result Count = 0 (0)

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RULECHECK Via1.1 ..... TOTAL Result Count = 0 (0)

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RULECHECK Via3.4 ..... TOTAL Result Count = 0 (0)

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RULECHECK Antenna.metal9 .... TOTAL Result Count = 0 (0)

RULECHECK Antenna.metal10 ... TOTAL Result Count = 0 (0)

----------RULECHECK RESULTS STATISTICS (BY CELL)----------

--- SUMMARY---

TOTAL CPU Time: 0

TOTAL REAL Time: 0

TOTAL Original Layer Geometries: 0 (0)

TOTAL DRC RuleChecks Executed: 167

TOTAL DRC Results Generated: 0 (0)

Conclusion

The course had taught me a great deal about the past-established integrated circuit design process. The topics we covered included MOS transistor theory, CMOS processing technology, VLSI design methodologies. But never would i have thought something along the lines of me designing a project such as this would ever be possible given the high level of detail required, time involved, and knowledge of the software. However after months of learning the rules, becoming familiar with the software and its quirks, breaking down

schematics as practice, and constant work the “seemingly impossible” became a reality.

The academic/personal growth from this course was absolutely incredible and has left me eager to grow further in transistor technology, and more specifically the low level layout, floorplanning, and abstraction of future embedded systems.

The professor for the course, Emre Salman, was absolutely outstanding, and has introduced me to a world of engineering and design I never thought was within reach.

For all course requirements/standards/lecture content/questions he may reached at:

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Homepage: https://nanocas.ece.stonybrook.edu/salman/