RAM_CB_16k IP Core

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Dual port circular buffer with internal address generation and automatic output data alignment.

Features

16Kx18bit circular buffer
Internal write address counter
72-bit read data bus
Automatic output data alignment
Simultaneous write and read
Verilog synthesisable RTL code
Single clock read
Up to 147 MHz clock
Small area (354 LUTs, 16 BRAMs)
Optimized for FPGA Spartan6

Overall description

This block implements a circular buffer with 16K 18-bit data words, including an internal write address generator and automatic alignment of the read data. The memory features a write port for one data item (18-bit) controlled by an external write enable signal, and a 72-bit read port (four 18-bit words) for random reads, addressed by a 12 bit address bus (4096 memory locations). The origin of the read address space is the last memory address written, thus allowing to easily access data from the most recently written (reading address 0) to the oldest data in the buffer (reading address 4095). The design is provided as a fully synthesisable RTL code (Verilog) and operates synchronously with a single global clock signal. Synthesis with XILINX XST 14.6 reports a maximum clock frequency above 147 MHz and occupying only 354 LUTs (targeting the FPGA XILINX Spartan6).

Architecture

Figure 1 presents a functional block diagram of the RAM_CB_16k block and table 1 lists the function of the input/output ports. The core memory is implemented with four 4K x 18 bit dual-port RAM blocks, mapped to the Spartan6 BRAMs. The write address is generated by an internal 14-bit binary counter enabled by the write enable signal (**wen**). The read side includes an address calculator that combines the input read address with the current write address to compute the effective physical address to access the first data element. Then, the addresses for each memory are calculated and the 4 data words read from the memories are aligned to form the 72-bit output word in the correct order (more recent data first). The registers drawn in gray are only implemented in the 2-stage pipelined version.

Table 1 – Input/output ports of RAM_CB_16k IP core.

Name	Direction	Function
clock	Input	Master clock signal. The module operates synchronously with the rising edge of this clock signal.
reset	Input	Master reset, active high and synchronous with the master clock. The activation of reset will clear the write address counter.
din[17:0]	Input	Input bus with the data to be written into the memory.
wen	Input	Write enable. A one in this input will write into the memory the current data at din and increment the internal address counter.
addrin[11:0]	input	Address bus for read data. The address of data read is referred to the current write address (see text)
dout[71:0]	Output	Data out, formed by four 18-bit words; the least significant word is the oldest data read.

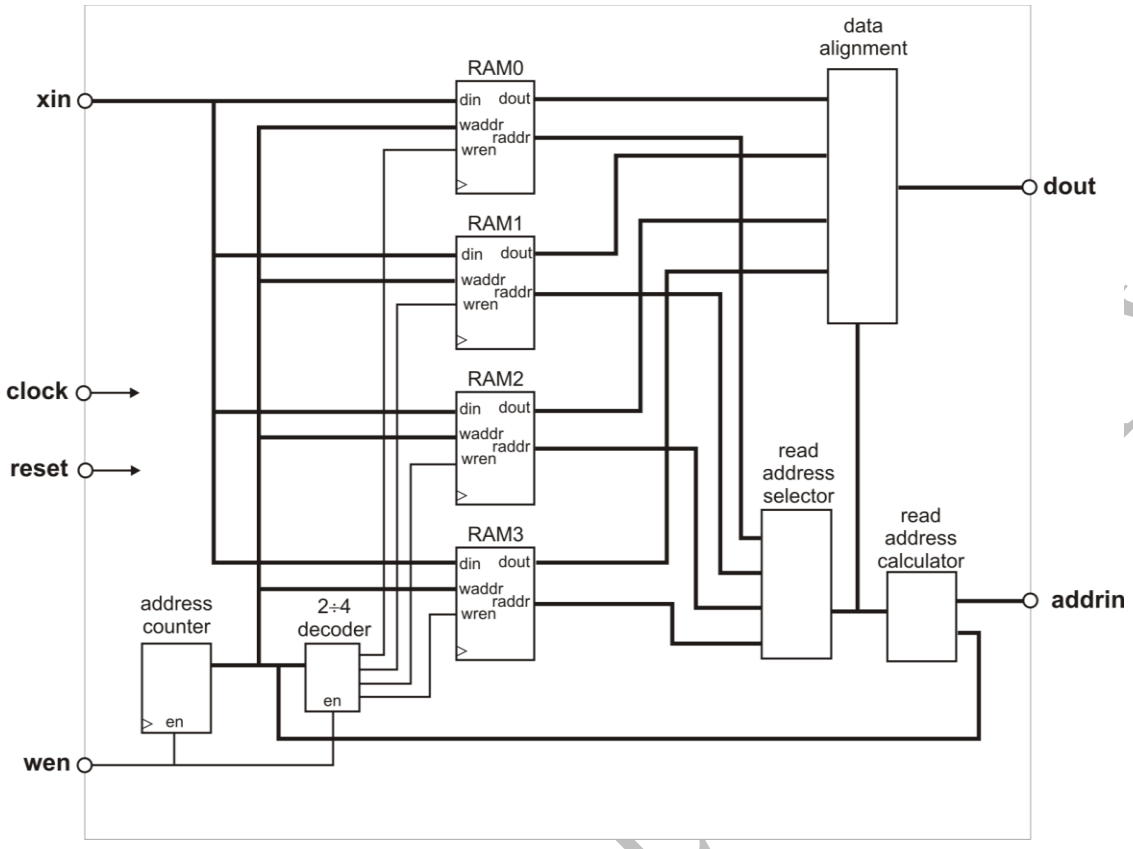

Figure 1 – Functional block diagram of the RAM_CB_16k IP core.

Memory write

From the write port side, the memory can be seen as a linear 16384 x 18bit RAM, addressed by the output of an internal 14-bit binary counter. The counter enable and the memory write enable signals are routed to the input **wen**. When **wen** is high and a positive clock transition occurs, the data present at the input port **din** is written into the memory location currently addressed by the address counter. At the same time the address counter is incremented, pointing to the next memory location to be written. The counter remains in that state until a new write is issued, or is set to zero when reset is applied. The address counter wraps naturally the 16384 address space, thus implementing the circular buffer behaviour.

Memory read

To increase the memory read bandwidth, the output data bus **dout** is 72-bit wide, providing four data words in a single memory read cycle. The read is synchronous with the clock and a read operation is performed by just applying the required read address at the address input **addrin**. The current implementation will respond the data read in the next clock cycle (see timing diagram).

The read address is combined with the internal write address to read blocks of 4 words, counting from the last data written. Reading from address 0 (zero) will return the 4 most recent data words written into the memory (x_{k-0}, x_{k-1}, x_{k-2}, x_{k-3}), considering that the subscript $_{k-0}$ refers to the last data written and $_{k-3}$ to the data written 3 cycles before; reading from address 1 will return x_{k-4}, x_{k-5}, x_{k-6}, x_{k-7}; reading from address A will return the data items x_{k-A*4}, $x_{k-A*4+1}$, $x_{k-A*4+2}$, $x_{k-A*4+3}$.

Write-read constraints

The operation of the block is fully synchronous with the global clock and the internal address counter changes state synchronously with the RAM output data register. Because of this, a read operation issued in the same clock cycle of a write operation will access a memory address based on the write address before that clock and will thus not reflect the data written in that same clock (see examples in the timing diagram). In the current architecture the block will output the data read in the same clock transition after the read address has been captured. If a write occurs at the same clock the read address is captured, the read data already reflects the recently written data but the write address used is still the address before the write.

To avoid errors due to misinterpretation of the operation when simultaneous reading and writing occur, it is recommended to issue a read only 2 clock cycles after a write.

Verilog interface and configuration

The Verilog interface is presented in figure 2.

```
module RAM_CB_16k(
                  clock,
                  reset,
                  din,
                  wen,
                  addrin,
                  dout
                 );
input          clock;
input          reset;
input  [17:0]  din;
input          wen;
input  [11:0]  addrin;
output [71:0]  dout;
```

Figure 2 – Verilog interface of the RAM_CB_16k IP core.

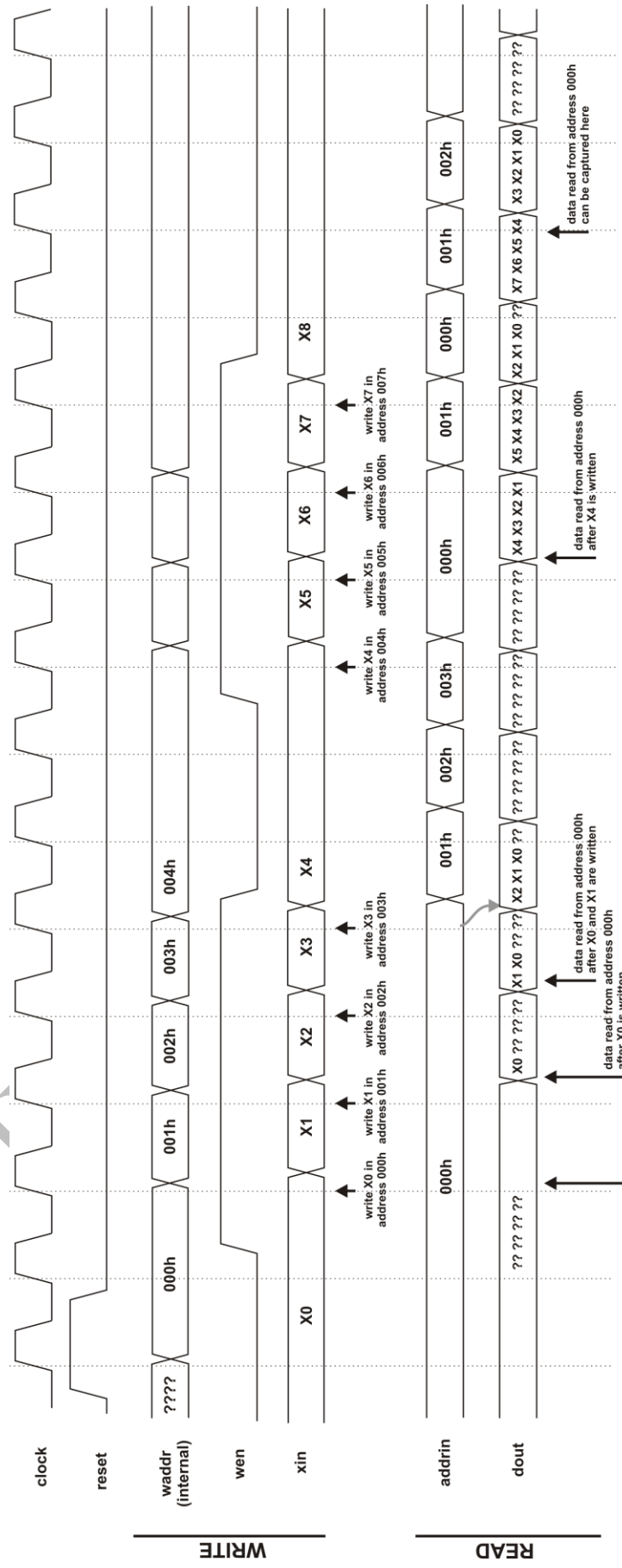

Figure 3 – Timing diagrams for the write and read processes.