Run **sinegen.m** to generate a test signal formed by a sum of unit amplitude sine waves into file **testsine.hex**. To generate a different test signal edit the Matlab script to define the frequencies of the sine wave components. File **coefs\_16k\_bandpass.mat** contains the coefficients of a bandpass filter with pass band from 2000Hz to 3000Hz, 10 Hz transition band and 60 dB attenuation in the stop band. Run the script **cfloat2hex36b.m** using that file as argument to generate the hex files with the filter coefficients required for initializing the RAM memories with **$readmemh()** Verilog task. All coefficients are stored in file **outcoefs\_RAM03.hex**, in hexadecimal, 36 bits and two's complement, in a format suitable to be read by **$readmemh()**. The same file will be uploaded to the FPGA board through the serial interface. This file is also split into the four hex files **outcoefs\_RAM0.hex** ~ **outcoefs\_RAM3.hex**, containing the contents for the coefficient memory bank defined in **RAM\_coefs\_16k.v** (this model uses these files to initialize the memory contents).

The script **hexconvol.m** executes the convolution between the input test signal and the FIR filter generating the file **goldenout.hex** to be used in the testbench to verify the output of the FIR module.

Figure 1 shown a segment of the input test signal, the bandpass filter impulse response and the output signal. Figures 2 and 3 show the FFTs of these signals. Note in figure 3 the rejection of the two components in 1980 Hz and 3020 Hz.





