MECH 421: Mechatronics System Instrumentation
2020/21 Winter Session – Term 2

Lab 2 – Power Transconductance Amplifier

Pre-lab due: Feb 22, 2021
Lab report due: Mar 12, 2021

1 Objectives

- Design a transconductance amplifier using a power operational amplifier.
- Measure the closed-loop step response.
- Measure the closed-loop frequency response.

2 Lab Description

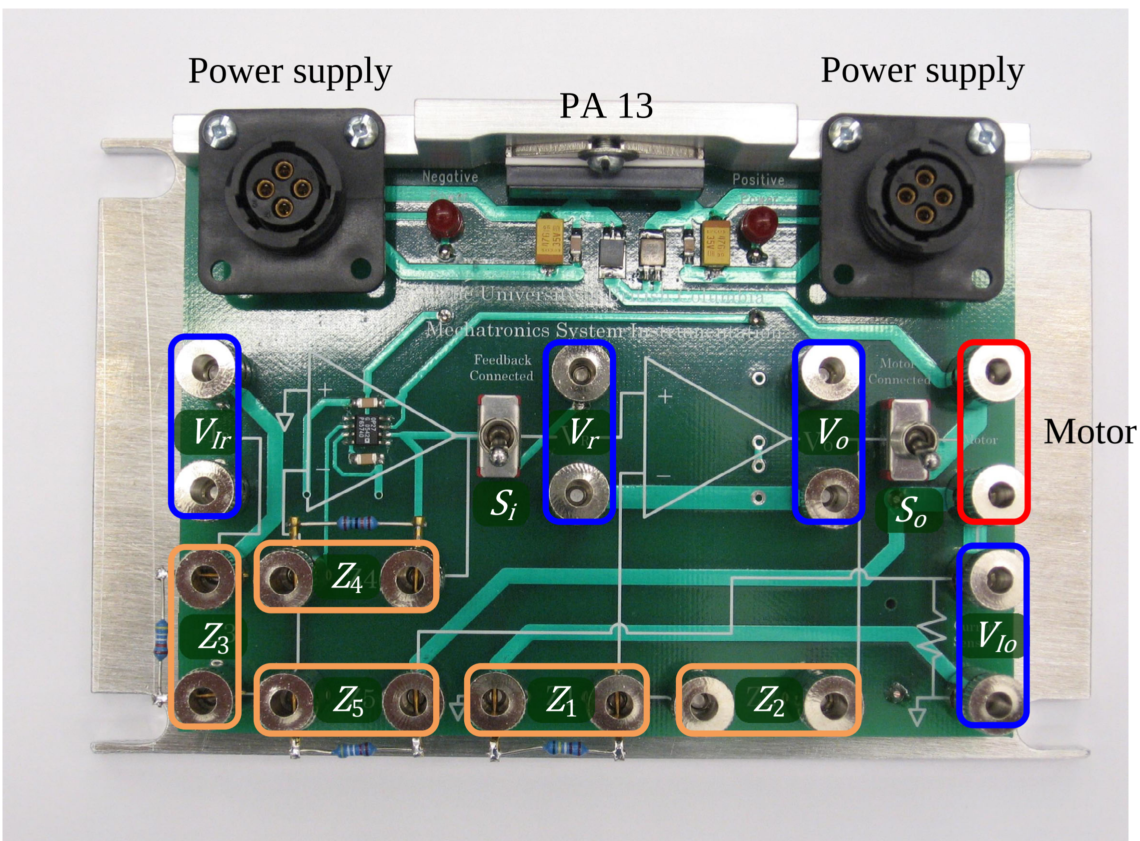

Figure 1: Picture of the power amplifier board.

Figure 1 shows a picture of the power amplifier board. Figure 2 shows a simplified circuit schematic. The board consists of two op-amp stages: a voltage stage based on a power op-amp (PA13 from Apex Microtechnology) and an analog current controller based on a precision op-amp

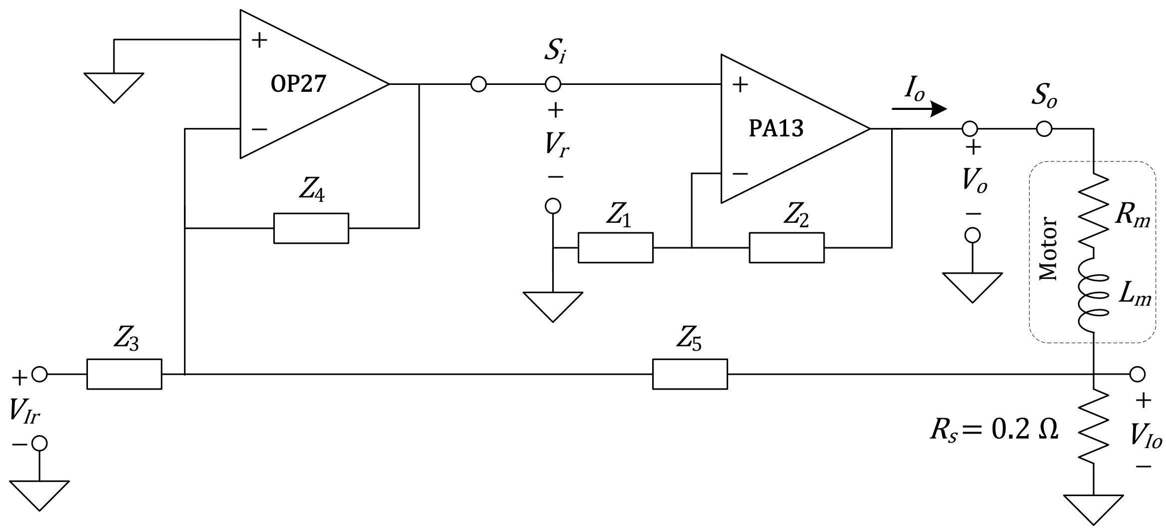

Figure 2: Power amplifier simplified schematic diagram.

(OP27 from Analog Devices). The power op-amp is attached to an aluminum heat sink and the precision op-amp is mounted on the printed circuit board. On the back side of the board, there is a shunt resistor $R_s = 0.2\,\Omega$ to measure the current through the motor winding.

The sockets labeled as Z_1-Z_5 are to configure impedances that program the amplifier board. The sockets labeled as Z_1 and Z_2 are for two resistors that set the gain and bandwidth of the voltage stage. Select $Z_1 = 2.2\,\text{k}\Omega$ and $Z_2 = 22\,\text{k}\Omega$ so that the DC gain of the voltage stage becomes $V_o/V_r = 11$. The sockets labeled as Z_3, Z_4, and Z_5 are for impedances that implement feedback current control. In this lab, we will select appropriate impedances Z_3, Z_4, and Z_5 to implement analog current control based on the design specifications.

The sockets labeled as `Motor` are for the DC motor. Do not measure the voltage across these sockets with an oscilloscope, as neither of them are grounded. This may irreversibly damage the power amplifier board or the oscilloscope.

The board provides dedicated sockets for voltage measurements: V_{Ir}, V_r, V_o, and V_{Io}. Here, V_{Ir} is the current-reference voltage, V_r is the voltage stage input voltage, V_o is the voltage stage output voltage, and V_{Io} is the current-sensing voltage. Please do not use any other sockets for measurement. Also, make sure that the banana connector's ground terminal is oriented toward the bottom side of the board.

There are two switches S_i and S_o at the input and output of the power op-amp. The input switch S_i connects/disconnects the current controller. The output switch S_o connects/disconnects the DC motor load. In this lab, we will switch S_i to `Feedback Connected` side to connect the current controller and switch S_o to `Motor Connected` side to connect the motor.

3 Pre-lab Assignment

1. For $Z_1 = 2.2\,\mathrm{k\Omega}$ and $Z_2 = 22\,\mathrm{k\Omega}$, draw a block diagram of the voltage stage that shows the relation between the input voltage V_r and output voltage V_o.

2. Draw a block diagram of the whole system that shows the relation between the current-reference voltage V_{Ir} and current-sensing voltage V_{Io}.

3. Current controller design: select appropriate values for Z_3, Z_4, and Z_5 to design a current controller that meets the following specifications.

   - Z_3, Z_4, and Z_5 consist of resistors and/or capacitors. The resistors in stock are from $10\,\Omega$ to $1\,\mathrm{M\Omega}$ in standard increments. The capacitors are from $100\,\mathrm{pF}$ to $4.7\,\mathrm{\mu F}$.
   - The DC gain of V_{Io}/V_{Ir} is $0.2\,\mathrm{V/V}$ (or, the DC transconductance of I_o/V_{Ir} is $1\,\mathrm{A/V}$).
   - The closed-loop bandwidth of V_{Io}/V_{Ir} should be greater than $5\,\mathrm{kHz}$.
   - The step response of V_{Io}/V_{Ir} should have zero steady state error.
   - The loop should have a phase margin of at least $60°$.

4. Based on your selected Z_3, Z_4, and Z_5, draw the Bode plot and step response of V_{Io}/V_{Ir}.

Note: The Bode plots must be appropriately labeled with DC gain, relevant break frequencies, and slopes. The Bode plots must include the phase plot as well as magnitude. The step responses should have the correct initial slope (based on the system order), labeled time constant, 10%-90% rise time, steady-state value, and percentage overshoot (if any).

4 Lab Assignment

In this lab, we will connect the voltage stage to the current controller and motor by turning on the switches S_i and S_o. Make sure that S_i is toward the `Feedback Connected` and S_o is toward the `Motor Conected`.

4.1 Set the impedances Z_1-Z_5

With the power supplies turned off, set $Z_1 = 2.2\,\mathrm{k\Omega}$ and $Z_2 = 22\,\mathrm{k\Omega}$, and populate Z_3, Z_4, and Z_5 based on the pre-lab design.

4.2 Step responses

Apply a current-reference voltage V_{Ir} using a signal generator and measure the current-sensing voltage V_{Io} as well as V_{Ir} using an oscilloscope. Make sure that nothing is connected for V_r.

Set V_{Ir} to be a 10-Hz square wave with different amplitudes ($0.1\,\mathrm{V_{pk\text{-}pk}}$, $0.2\,\mathrm{V_{pk\text{-}pk}}$, $0.5\,\mathrm{V_{pk\text{-}pk}}$, and $1.0\,\mathrm{V_{pk\text{-}pk}}$), and measure V_{Io} for each amplitude. Record the four step responses, and calculate the rise time (from 10% to 90%) and the percentage overshoot. Compare the results with the pre-lab predictions.

4.3 Frequency responses

Set V_{Ir} to be a sine wave with $0.1\,\mathrm{V_{pk\text{-}pk}}$ amplitude. Measure the frequency response of V_{Io}/V_{Ir} at more than 20 frequency points from $50\,\mathrm{Hz}$ to $5 \times \omega_h$, where ω_h is the designed closed-loop bandwidth. The frequency points should be nearly equally spaced in log scale. Take more data points around the break frequencies and interesting features. (Tip: initially sweep the frequencies quickly to identify the break frequencies and interesting features based on the phase difference between V_{Ir} and V_{Io}. Then, decide on the appropriate frequency points and proceed with the actual measurements.)

Record the amplitudes of V_{Ir} and V_{Io} and their phase difference. Calculate the -3 dB bandwidth of the closed loop response and compare with the pre-lab prediction. During the experiment, monitor both the current sensing voltage V_{Io} and the power stage output voltage V_o. If there is significant distortion on either of them, reduce the signal generator amplitude to ensure both V_{Io} and V_o remain sinusoidal.

4.4 Destabilize the current controller

This experiment is designed for you to understand sources of instability of the system. Keep Z_3 and Z_5 the same, but remove the resistor from Z_4 and leave the capacitor only. This will convert the current controller from a PI controller to a pure integrator. Set V_{Ir} to be a $10\,\mathrm{Hz}$ square wave with $0.2\,\mathrm{V_{pk\text{-}pk}}$ amplitude.

1. Measure the step response of V_{Io}/V_{Ir}. Record the step response using a camera and corresponding values of Z_3, Z_4, and Z_5. Does the system become unstable?

2. If the above system remains stable, then decrease the Z_4 capacitor value by a factor of two until the system becomes unstable. Be sure to record each step response and corresponding values of Z_3, Z_4, and Z_5.

3. Explain why the system becomes unstable.