

```
00 Label:          Step: Test_pgm      %M48.W      = 0
```

App_setupa] [_____ %V4034.0	V211_2.4 R T _____ %V211.4	Index_6 = 0 T _____ %M110a.W = 0x0	M1518 = X_index T _____ %M1518.W = %V5dc.W	Test_pgm = 1 (T) _____ %M48.W = 0x1
App_setupb] [_____ %V4034.1				
App_setupc] [_____ %V4034.2				
App_setupd] [_____ %V4034.3				
Jog_icla] [_____ %V4032.1				
				goto(END) (T) _____

```
01 Label: RESET      Step: Test_pgm      %M48.W      = 1
```

Reset byte piano/ventosa

Index_6 < 84]>[%M110a.W < 0x54	(1) (T)
	Index_6 += 1 (T)
	%M110a.W += 0x1 goto(RESET) (T)

```
(1) %V4500.B[%M110a.W] = 0x0      :   Piano10[Index_6] = 0
```

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02 Label: Step: Test_pgm %M48.W = 1

Setup non programmato(999) o allarme PGM

Tab_pm[M1518] == 999]>[%V5000.L[%M1518.W] == 0x3e7		No_setup () %V4030.2 Test_pgm = 99 (T) %M48.W = 0x63 goto(END) (T)
(1) (2) Tab_pm[M1518] != 164]>[]>[%V5000.L[%M1518.W] != 0xa4		Alarm_pgm () %V4031.5 Test_pgm = 99 (T) %M48.W = 0x63 goto(END) (T)

bit setup non programmato

tentativo di posizionare una ven

(1) %V5000.L[%M1518.W] != 0xa8 : Tab_pm[M1518] != 168
(2) %V5000.L[%M1518.W] != 0xa7 : Tab_pm[M1518] != 167

03 Label: Step: Test_pgm %M48.W = 1

Decodifica Area di Scambio

Tab_pm[M1518] == 167]>[T %V5000.L[%M1518.W] == 0xa7 %V4038.W = %V5dc.W		Remove_pdl (S) %V4031.6
Tab_pm[M1518] == 168]>[T %V5000.L[%M1518.W] == 0xa8 %V402a.W = %V5dc.W		Setup_pdl (S) %V4030.1
Tab_pm[M1518] == 164]>[T %V5000.L[%M1518.W] == 0xa4 %V4036.W = %V5dc.W		Verify_pdl (S) %V4030.5
		Test_pgm = 0 (T) %M48.W = 0x0
		goto(END) (T)

Start ciclo di parcheggio e rimo

start ciclo di setup

start ciclo di verifica

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