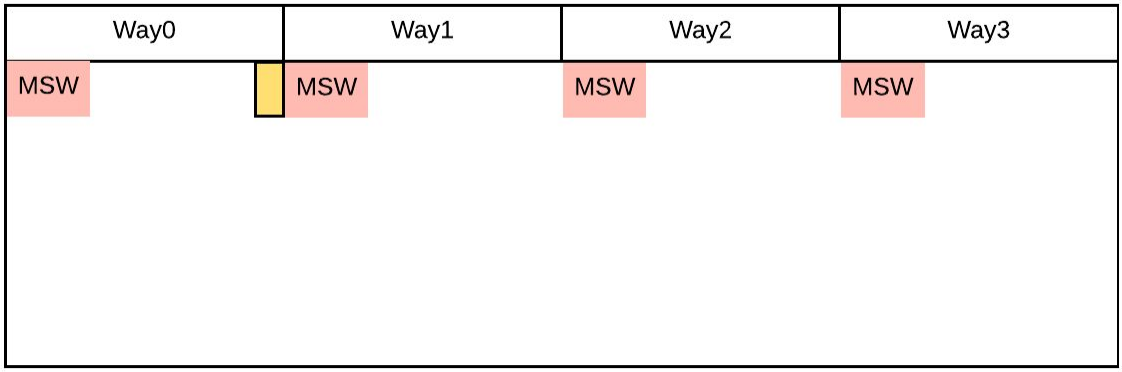
1. Write a cycle accurate SystemC OR SystemVerilog module for a 4-way set-associative cache [1MB (megabyte) , 256 bit cache lines]. The cache eviction policy is data dependent. Specifically, the “way” with the lowest value for the most significant 32-bit word is the one that gets evicted.
2. Please include:
    a. An architectural description of how you are implementing addressing (number of bits for tag, index, etc.) and the replacement policy
    b. A testbench for the above
3. Extra credit eviction policy: Evict the “way” which has the lowest “n”th 32-bit word where “n” is determined by the 3 LSBs of “way0”.



What are we looking for?

1. We value a complete solution both from correctness as well as handling of corner cases.
2. We want to evaluate your understanding of good software engineering practices. Please use your best judgement in that context when developing this code.