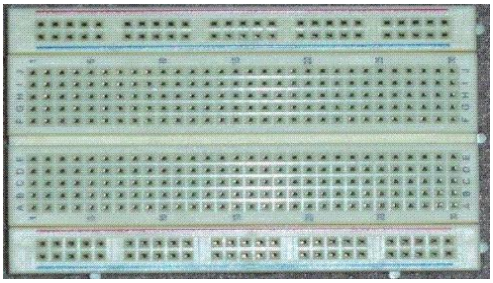
MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

(Affiliated to Osmania University)

Banjara Hills, Hyderabad, Telangana State

INFORMATION TECHNOLOGY DEPARTMENT

BASIC ELECTRONICS LAB MANUAL



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1. VISION OF THE INSTITUTION

To be part of universal human quest for development and progress by contributing high calibre, ethical and socially responsible engineers who meet the global challenge of building modern society in harmony with nature.

2. MISSION OF THE INSTITUTION

- To attain excellence in imparting technical education from the undergraduate through doctorate levels by adopting coherent and judiciously coordinated curricular and co-curricular programs
- To foster partnership with industry and government agencies through collaborative research and consultancy
- To nurture and strengthen auxiliary soft skills for overall development and improved employability in a multi-cultural work space
- To develop scientific temper and spirit of enquiry in order to harness the latent innovative talents
- To develop constructive attitude in students towards the task of nation building and empower them to become future leaders
- To nourish the entrepreneurial instincts of the students and hone their business acumen.
- To involve the students and the faculty in solving local community problems through economical and sustainable solutions.

3. VISION OF THE DEPARTMENT

Fostering a bright technological future by enabling the students to function as leaders in software industry and serve as means of transformation to empower society through ITeS.

4. MISSION OF THE DEPARTMENT

To create an ambience of academic excellence through state of art infrastructure and learner-centric pedagogy leading to employability in multi-disciplinary fields.

5. PROGRAM EDUCATIONAL OBJECTIVES

1. The Program Educational Objectives of Information Technology Program are as follows:
2. Graduates will demonstrate technical competence and leadership in their chosen fields of employment by identifying, formulating, analyzing and creating efficient IT solutions.
3. Graduates will communicate effectively as individuals or team members and be successful in varied working environment.
4. Graduates will demonstrate lifelong learning through continuing education and professional development.
5. Graduates will be successful in providing viable and sustainable solutions within societal, professional, environmental and ethical context.

6. PROGRAM OUTCOMES

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to

comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

7. PROGRAM SPECIFIC OUTCOMES

PSO1: Work as Software Engineers for providing solutions to real world problems using Structured, Object Oriented Programming languages and open source software.

PSO2: Function as Systems Engineer, Software Analyst and Tester for IT and ITeS.

GENERAL GUIDELINES AND SAFETY INSTRUCTIONS

1. Sign in the log register as soon as you enter the lab and strictly observe your lab timings.
2. Strictly follow the written and verbal instructions given by the teacher / Lab Instructor. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teacher.
3. **Never work alone!** You should be accompanied by your laboratory partner and / or the instructors / teaching assistants all the time.
4. It is mandatory to come to lab in a formal dress and wear your ID cards.
5. Do not wear loose-fitting clothing or jewellery in the lab. Rings and necklaces are usual excellent conductors of electricity.
6. Mobile phones should be switched off in the lab. Keep bags in the bag rack.
7. Keep the labs clean at all times, no food and drinks allowed inside the lab.
8. Intentional misconduct will lead to expulsion from the lab.

9. Do not handle any equipment without reading the safety instructions. Read the handout and procedures in the Lab Manual before starting the experiments.
10. Do your wiring, setup, and a careful circuit checkout before applying power. Do not make circuit changes or perform any wiring when power is on.
11. Avoid contact with energized electrical circuits.
12. Do not insert connectors forcefully into the sockets.
13. **NEVER** try to experiment with the power from the wall plug.
14. Immediately report dangerous or exceptional conditions to the Lab instructor / teacher: Equipment that is not working as expected, wires or connectors are broken, the equipment that smells or "smokes". If you are not sure what the problem is or what's going on, switch off the Emergency shutdown.
15. Never use damaged instruments, wires or connectors. Hand over these parts to the Lab instructor/Teacher.
16. Be sure of location of fire extinguishers and first aid kits in the laboratory.
17. After completion of Experiment, return the bread board, trainer kits, wires, CRO probes and other components to lab staff. Do not take any item from the lab without permission.
18. Observation book and lab record should be carried to each lab. Readings of current lab experiment are to be entered in Observation book and previous lab experiment should be written in Lab record book. Both the books should be corrected by the faculty in each lab.
19. Handling of Semiconductor Components: Sensitive electronic circuits and electronic components have to be handled with great care. The inappropriate handling of electronic component can damage or destroy the devices. The devices can be destroyed by driving to high currents through the device, by overheating the device, by mixing up the polarity, or by electrostatic discharge (ESD). Therefore, always handle the electronic devices as indicated by the handout, the specifications in the data sheet or other documentation.
20. Special Precautions during soldering practice
    a. Hold the soldering iron away from your body. Don't point the iron towards you.
    b. Don't use a spread solder on the board as it may cause short circuit.
    c. Do not overheat the components as excess heat may damage the components/board.
    d. In case of burn or injury seek first aid available in the lab or at the college dispensary.

Experiment No: 1

Study of CRO & Measurement of Voltage Amplitude & Frequency

Aim:

1. Study of CRO and to find the Amplitude and Frequency using CRO.
2. To measure the Unknown Frequency & Phase difference using CRO.

Components and Equipments Required: Cathode-ray oscilloscope, Function Generator (2), Decade Resistance Box (DRB), Capacitor, CRO Probes and Bread Board.

Theory:

An outline explanation of how an oscilloscope works can be given using the block diagram shown below.

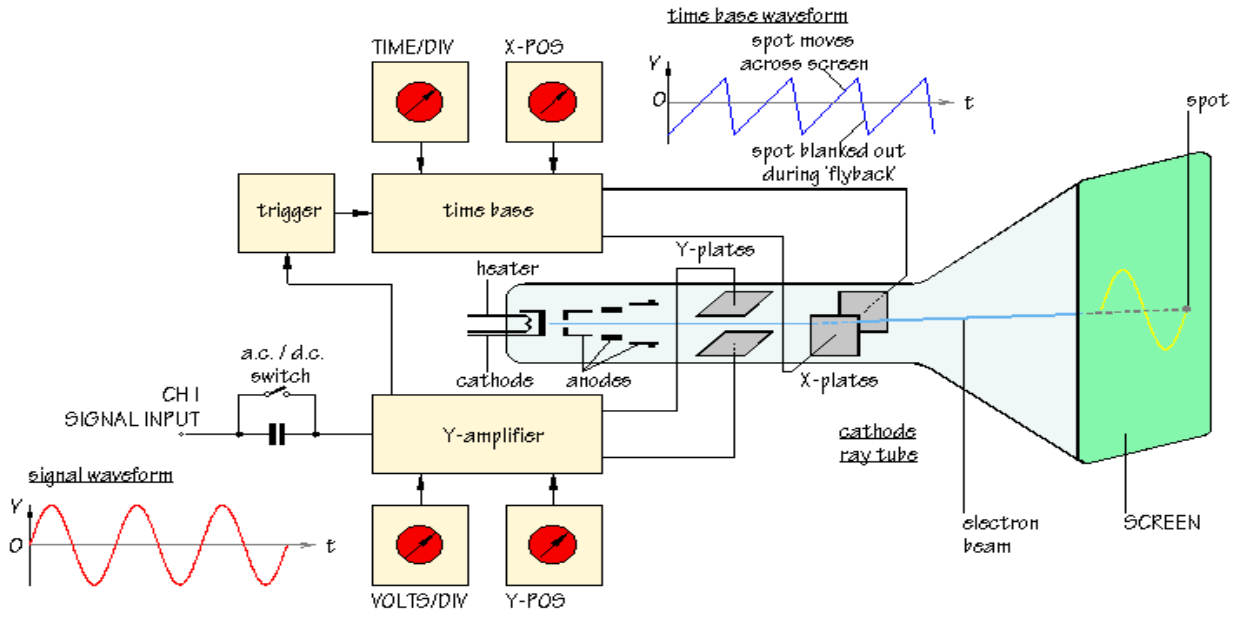


Fig. 1: Cathode Ray Oscilloscope

Like a television screen, the screen of an oscilloscope consists of a **Cathode Ray Tube**. Although the size and shape are different, the operating principle is the same. Inside the tube is a vacuum. The electron beam emitted by the heated cathode at the rear end of the tube is

accelerated and focused by one or more anodes, and strikes the front of the tube, producing a bright spot on the phosphorescent screen.

The electron beam is bent, or deflected, by voltages applied to two sets of plates fixed in the tube. The horizontal deflection plates or **X-plates** produce side to side movement. As you can see, they are linked to a system block called the **time base**. This produces a saw tooth waveform. During the rising phase of the saw tooth, the spot is driven at a uniform rate from left to right across the front of the screen. During the falling phase, the electron beam returns rapidly from right ot left, but the spot is 'blanked out' so that nothing appears on the screen. In this way, the time base generates the X-axis of the *V*/*t* graph.

The slope of the rising phase varies with the frequency of the saw tooth and can be adjusted, using the TIME/DIV control, to change the scale of the X-axis. Dividing the oscilloscope screen into squares allows the horizontal scale to be expressed in seconds, milliseconds or microseconds per division (s/DIV, ms/DIV, µs/DIV). Alternatively, if the squares are 1 cm apart, the scale may be given as s/cm, ms/cm or µs/cm.

The signal to be displayed is connected to the **input**. The AC/DC switch is usually kept in the DC position (switch closed) so that there is a direct connection to the **Y-amplifier**. In the AC position (switch open) a capacitor is placed in the signal path. The capacitor blocks DC signals but allows AC signals to pass.

The Y-amplifier is linked in turn to a pair of **Y-plates** so that it provides the Y-axis of the the *V*/*t* graph. The overall gain of the Y-amplifier can be adjusted, using the VOLTS/DIV control, so that the resulting display is neither too small nor too large, but fits the screen and can be seen clearly. The vertical scale is usually given in V/DIV or mV/DIV.

The **trigger** circuit is used to delay the time base waveform so that the same section of the input signal is displayed on the screen each time the spot moves across. The effect of this is to give a stable picture on the oscilloscope screen, making it easier to measure and interpret the signal.

Changing the scales of the X-axis and Y-axis allows many different signals to be displayed. Sometimes, it is also useful to be able to change the *positions* of the axes. This is possible using the **X-POS** and **Y-POS** controls. For example, with no signal applied, the normal trace is a straight line across the centre of the screen. Adjusting Y-POS allows the zero level on the Y-axis to be changed, moving the whole trace up or down on the screen to give an effective display of signals like pulse waveforms which do not alternate between positive and negative values.

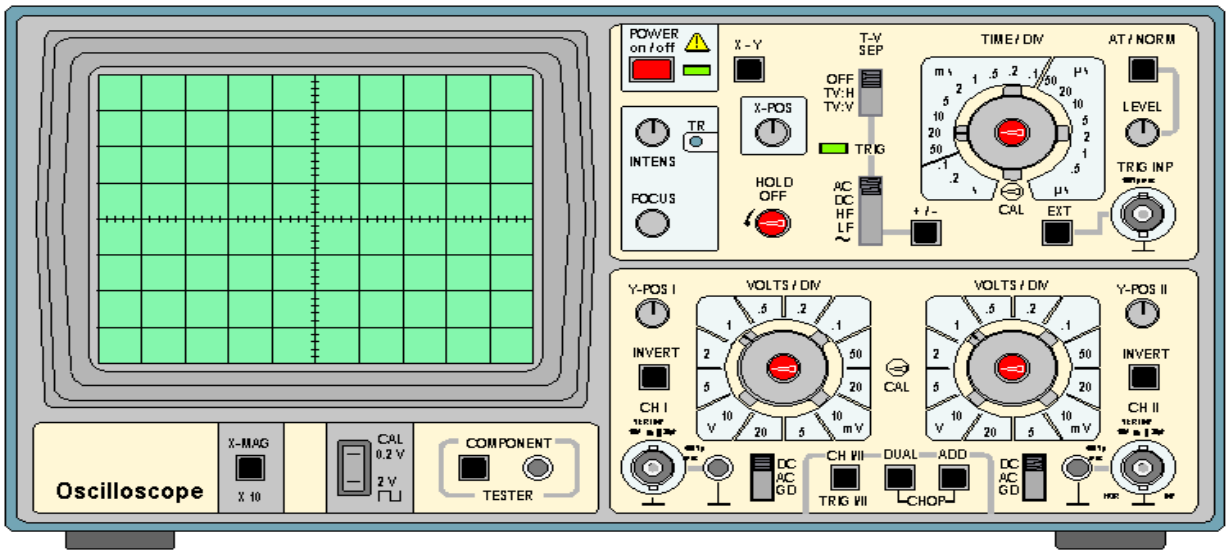


Fig. 2: Front View of Oscilloscope

Screen: Usually displays a *V*/*t* graph, with voltage *V* on the vertical axis and time *t* on the horizontal axis. The scales of both axes can be changed to display a huge variety of signals.

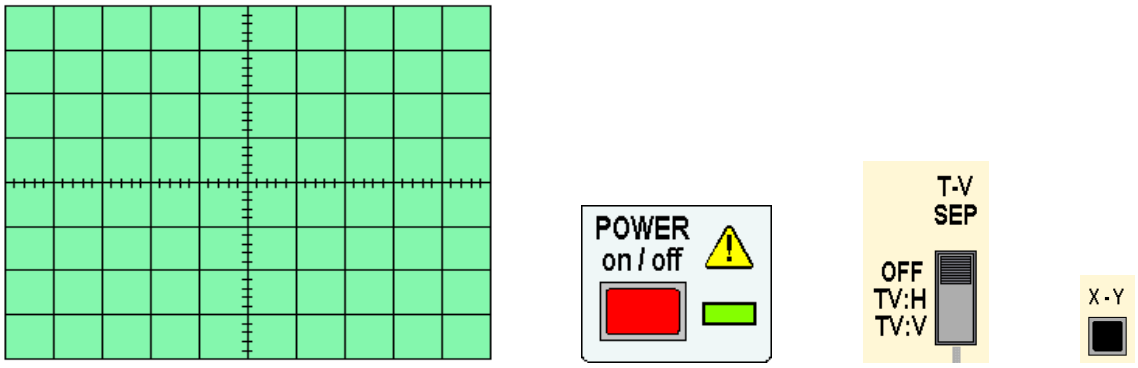


Fig. 3: Screen display of Oscilloscope

On/Off Switch: Pushed in to switch the oscilloscope on. The green LED illuminates.

X-Y Control: Normally in the OUT position.

When the X-Y button is pressed IN, the oscilloscope does not display a *V*/*t* graph. Instead, the vertical axis is controlled by the input signal to CH II. This allows the oscilloscope to be used to display a *V*/*V* voltage/voltage graph.

The X-Y control is used when you want to display component characteristic curves, or Lissajous figures. (Links to these topics will be added later.)

TV-Separation: Oscilloscopes are often used to investigate waveforms inside television systems. This control allows the display to be synchronized with the television system so that the signals from different points can be compared.

Time / Div: Allows the horizontal scale of the *V*/*t* graph to be changed.

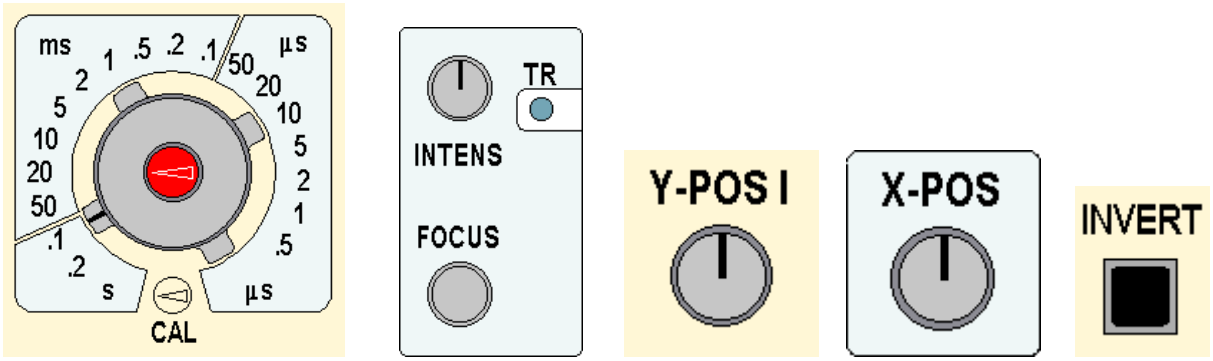


Fig. 4: Time division, Intensity, focus, X-Y mode knobs

With more experience of using the oscilloscope, you will develop a clear understanding of the functions of the important trigger controls and be able to use them effectively.

Intensity and Focus: Adjusting the INTENSITY control changes the brightness of the oscilloscope display. The FOCUS should be set to produce a bright clear trace.

If required, TR can be adjusted using a small screwdriver so that the oscilloscope trace is exactly horizontal when no signal is connected.

X-POS: Allows the whole *V*/*t* graph to be moved from side to side on the oscilloscope screen.

This is useful when you want to use the grid in front of the screen to make measurements, for example, to measure the period of a waveform.

Y-POS I and Y-POS II: These controls allow the corresponding trace to be moved up or down, changing the position representing 0 V on the oscilloscope screen.

To investigate an alternating signal, you adjust Y-POS so that the 0 V level is close to the centre of the screen. For a pulse waveform, it is more useful to have 0 V close to the bottom of the screen. Y-POS I and Y-POS II allow the 0 V levels of the two traces to be adjusted independently.

Invert: When the INVERT button is pressed IN, the corresponding signal is turned upside down, or inverted, on the oscilloscope screen. This feature is sometimes useful when comparing signals.

CH I And CH II Inputs: Signals are connected to the BNC input sockets using BNC plugs.

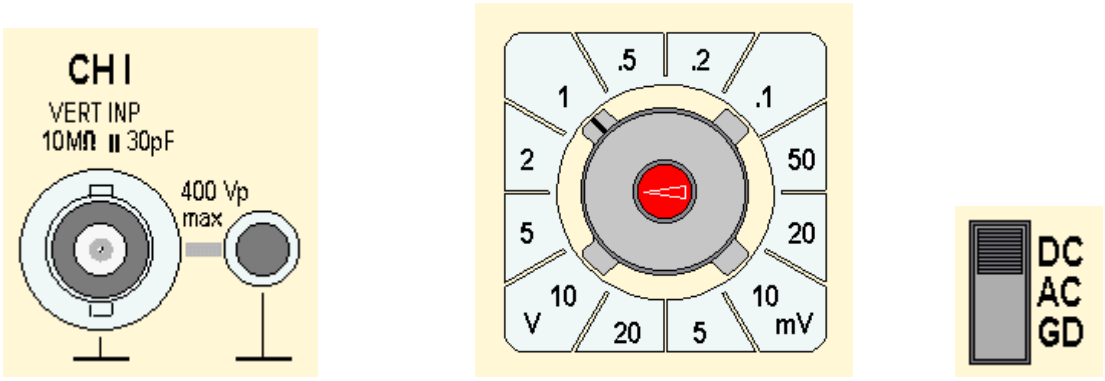


Fig. 5: Voltage division, Channels, AC, DC and GND knobs

The smaller socket next to the BNC input socket provides an additional 0 V, GROUND or EARTH connection.

Volts / Div: Adjust the vertical scale of the *V*/*t* graph. The vertical scales for CH I and CH II can be adjusted independently.

DC/AC/GND Slide Switches: In the DC position, the signal input is connected directly to the Y-amplifier of the corresponding channel, CH I or CH II. In the AC position, a capacitor is connected into the signal pathway so that DC voltages are blocked and only changing AC signals are displayed.

In the GND position, the input of the Y-amplifier is connected to 0 V. This allows you to check the position of 0 V on the oscilloscope screen. The DC position of these switches is correct for most signals.

Trace Selection Switches: The settings of these switches control which traces appear on the oscilloscope screen.

Measurement of Amplitude & Frequency:

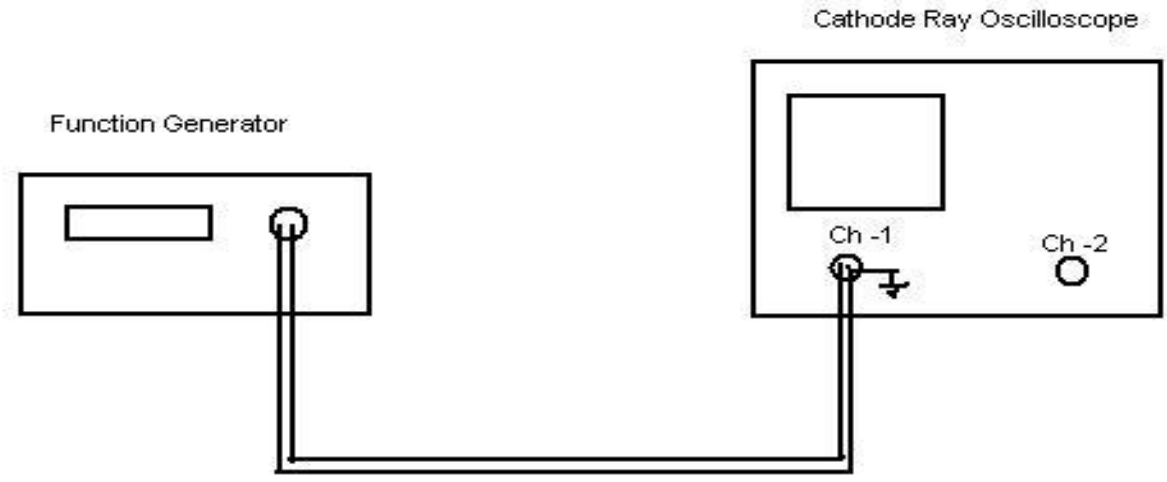


Fig. 6: Measurement of Amplitude & Frequency

Model waveforms:

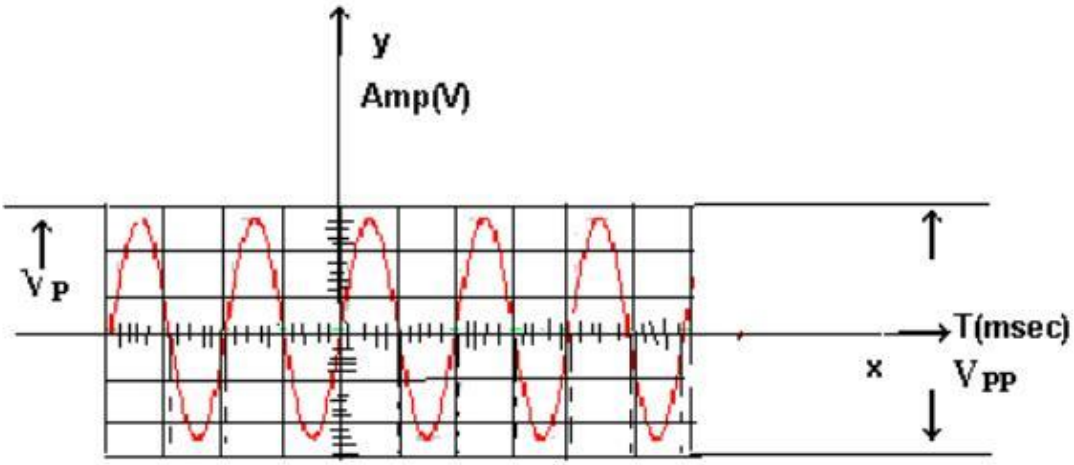


Fig. 7: Sinusoidal waveform

A) Measurement of Amplitude:

Procedure:

1. Make the connections as per the diagram shown above.
2. Put the CRO on a single channel mode and bring the CRO into operation by adjusting the trace of the beam to a normal brightness and into a thin line.
3. Now apply the sinusoidal wave of different amplitudes by using the LEVEL and COARSE buttons of the function generator.
4. Note on the vertical scale the peak to peak amplitude (Vpp).

Observations:

S. No.	No. of Vertical Divisions(X)	Voltage/ Division (Y)	Vp-p=X*Y	Vm=Vp-p/2

B) Measurement of Frequency:

Procedure:

1. Make the connections as per the diagram shown above.
2. Put the CRO on a single channel mode and bring the CRO into operation by adjusting the trace of the beam to a normal brightness and into a thin line.
3. Now apply the sinusoidal wave of different frequencies by using the LEVEL and COARSE buttons of the function generator.
4. Note down the horizontal scale period (T) in second by observing difference between the two successive peaks of the waveform.

Observations:

S. No.	No. of Horizontal Divisions(X)	Time/Division (Y)	T=X*Y	f=1/T

C) Measurement of Unknown Frequency:

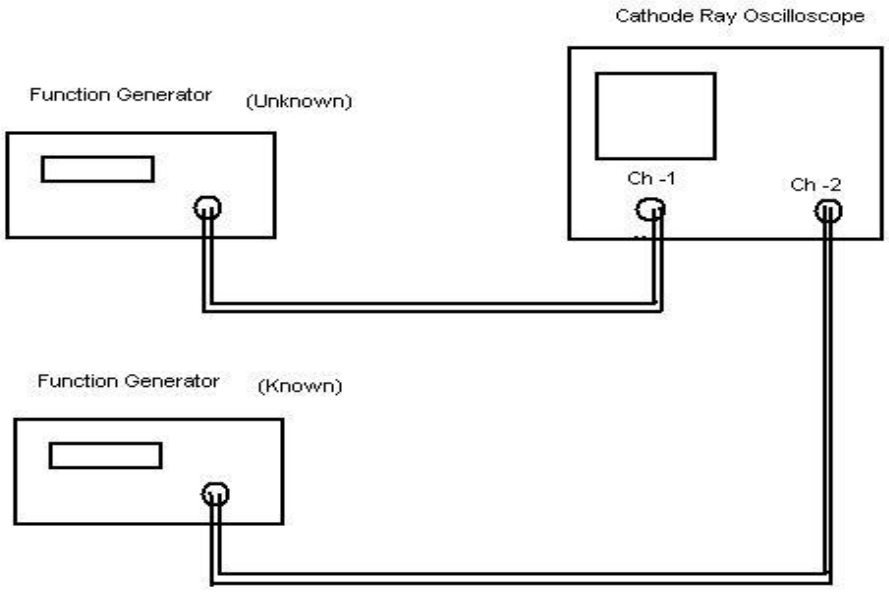


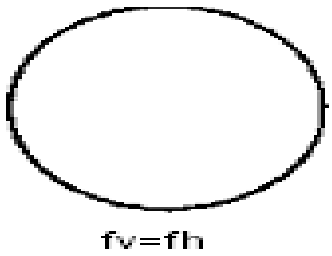
Fig. 8: Measurement of Unknown Frequency

Procedure:

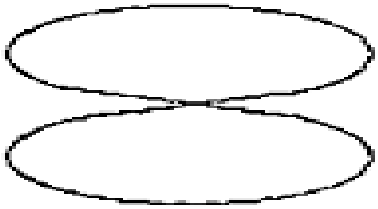
1. Connect the unknown frequency to the vertical (Y) deflection plates (CH -1) and the known frequency to the horizontal (X) deflection plates (Ch-2) from two function generators as shown in the figure.
2. Press X- Y mode button on the CRO and obtain the LISSAJOUS PATTERN. The lissajous pattern is obtained when two sinusoidal signals of different frequencies are applied to the X and Y deflection plates of the CRO. If the two frequencies are equal, we get a circle or ellipse.
3. Note down Nx (Number of touching points on X- axis), Ny (Number of touching points on Y – axis), Fx (Frequency of known signal).
4. If the LISSAJOUS pattern obtained is not clear to note the readings, Vary the known frequency such that a clear lissajous pattern is obtained.
5. The unknown frequency Fy is given by Fy = (Nx * Fx) / (Ny)

Observations:

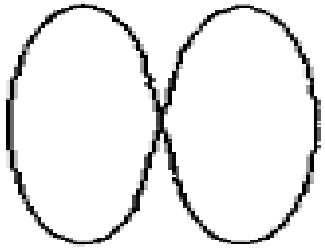
S. No.	Known frequency (f_x)	N_x	N_y	Unknown frequency $f_y=(N_x. f_x)/ N_y$



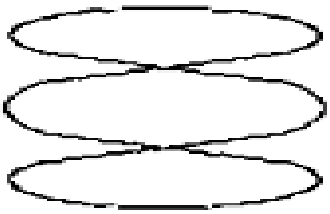
fv=fh



2fv=fh



fv=2fh



3fv=fh

$$\frac{fv}{fh} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

D) Measurement of Phase Difference:

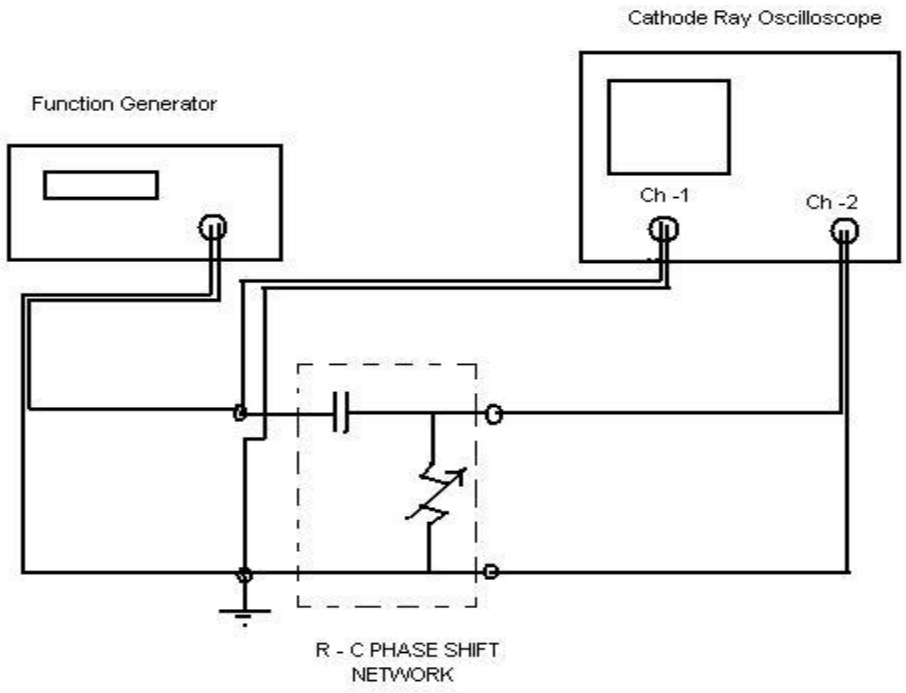


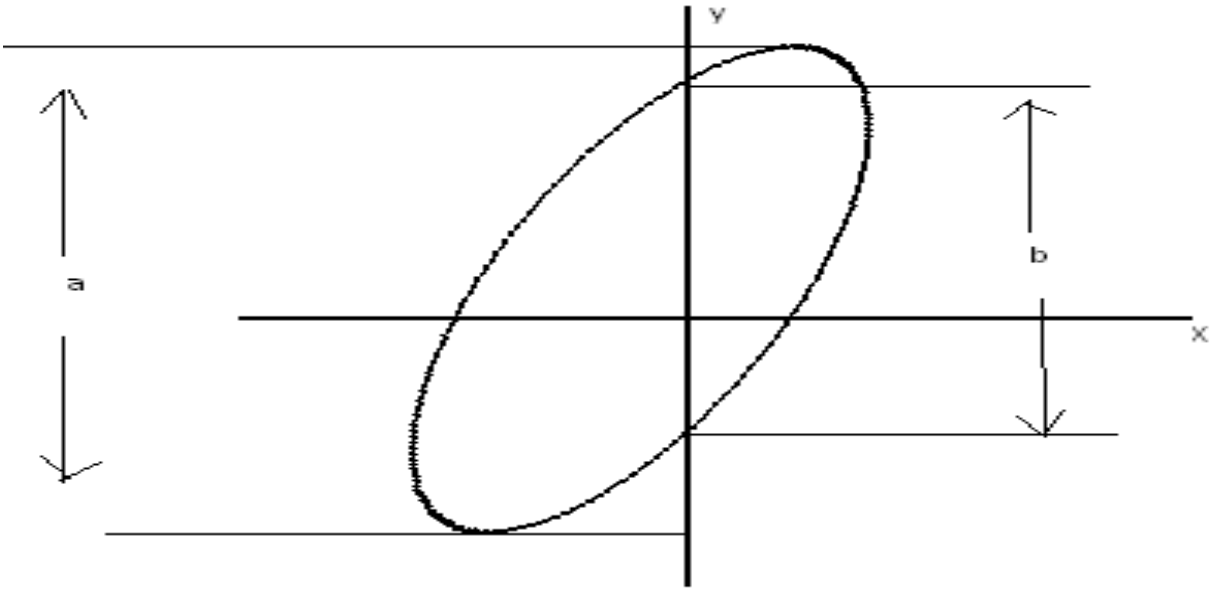
Fig. 9: Measurement of Phase Difference

Procedure:

1. Connect the RC phase shift network as shown above in the circuit diagram.
2. Obtain a sinusoidal signal of 5V (Pk- Pk) at 1 KHz from the function generator.
3. Connect the signal from the function generator to the input of the RC phase shift network and the same signal to the CH-1 of the CRO.
4. Connect the output of the Phase shift network to the CH-2 of the CRO.
5. Press X- Y mode button.
6. The pattern obtained on the screen will be an ellipse.
7. The phase difference between the two signals (θ) is given by $\theta = \sin^{-1}(B/A)$.
8. By varying the different values of the resistances from DRB, frequencies, note the values of B and A and hence find θ.

Observations:

S. No.	f	R	C	$\theta = \tan^{-1}(1/wRC)$	B	A	$\theta = \sin^{-1}(B/A)$



$$\theta = \sin^{-1}(b/a)$$

Where "θ" is the phase difference between the two signals

Results:

1. Working of CRO is studied. Amplitude and Frequency a signal is found using CRO.
2. Unknown Frequency & Phase difference are measured using CRO.

Experiment No: 2

V - I Characteristics of Si & Ge Diodes

Aim:

1. To plot V-I Characteristics of Silicon and Germanium P-N Junction Diodes.
2. To find cut-in voltage for Silicon and Germanium P-N Junction diodes.
3. To find static and dynamic resistances in both forward and reverse biased conditions.

Components:

Name	Quantity
Diodes 1N4007(Si)	1
Diodes DR-25(Ge)	1
Resistor 1KΩ	1

Equipment:

Name	Range	Quantity
Bread board		1
Regulated power supply	0-30V	1
Digital Ammeter	0-200μA/200mA	1
Digital Voltmeter	0-20V	1
Connecting Wires		

Specifications:

Silicon Diode 1N 4007:	**Germanium Diode DR 25:**
Max Forward Current = 1A	Max Forward Current = 250mA
Max Reverse Current = 5.0μA	Max Reverse Current = 200μA
Max Forward Voltage = 0.8V	Max Forward Voltage = 1V
Max Reverse Voltage = 1000V	Max Reverse Voltage = 25V
Max Power Dissipation = 30mW	Max Power Dissipation = 250mW
Temperature = -65 to 200° C	Temperature = -55 to 75° C

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a junction called depletion region (this region is depleted off the charge carriers). This region gives rise to a potential barrier called Cut-in Voltage. This is the voltage across the diode at which it starts conducting. The P-N junction can conduct beyond this potential.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected the cathode. Then diode is said to be **forward biased**. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current from n-side (injected minority current – due to holes crossing the junction and entering P- side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short- circuited switch.

If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be **reverse biased**. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on P-side and electrons on N-side tend to move away from the junction there by increasing the depleted region. However the process cannot continue indefinitely, thus a small current called reverse saturation current continues to flow in the diode. This current is negligible hence the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by the following equations

$$I = I_0 \left(e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

Where I = current flowing in the diode, I_0 = reverse saturation current V_D = Voltage applied to the diode

V_T = volt- equivalent of temperature = k T/q = T/ 11,600 = 26mV (@ room temp)

η = 1(for Ge) and 2 (for Si)

It is observed that **Ge** diodes has smaller cut-in-voltage when compared to **Si** diode. The reverse saturation current in **Ge** diode is larger in magnitude when compared to silicon diode.

Theoretically the dynamic resistance of a diode is determined using the following equation:

Dynamic Resistance:

$$R_D = \frac{\eta \ V_T}{\mathrm{I}}$$

Circuit Diagrams:

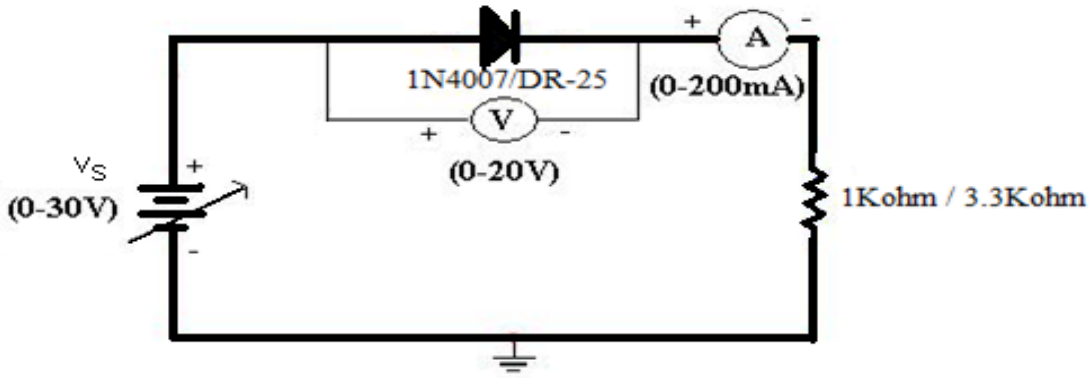


Fig. 1: Forward Bias Condition

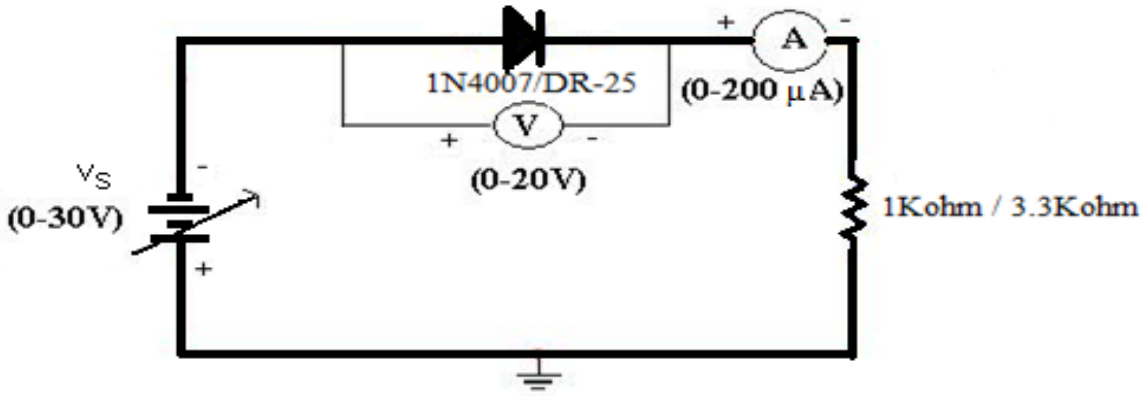


Fig. 2: Reverse Bias Condition

Procedure:

Forward Bias Condition:

1. Connect the components as shown in the Fig.1.
2. Vary the supply voltage such that the voltage across the Silicon diode varies from 0 to 0.6 V in steps of 0.1 V and in steps of 0.02 V from 0.6 to 0.76 V. In each step record the current flowing through the diode as I.
3. Repeat the above steps for Germanium diode too but with the exception that the voltage across the diode should be varied in steps of 0.01 V from 0.1 to 0.3 V in step-2.

Reverse Bias Condition:

1. Connect the diode in the reverse bias as shown in the Fig.2.
2. Vary the supply voltage such that the voltage across the diode varies from 0 to 10V in steps of 1 V. Record the current flowing through the diode in each step.
3. Repeat the above steps for Germanium diode too and record the current in each step.
4. Now plot a graph between the voltage across the diode and the current flowing through the diode in forward and reverse bias, for Silicon and Germanium diodes on separate graph sheets. This graph is called the V-I characteristics of the diodes.
5. Calculate the static and dynamic resistance of each diode in forward and reverse bias using the following formulae.

Static resistance, $R = V/I$

Dynamic resistance, $r = \Delta V/\Delta I$

Observations:

(a) Forward & Reverse bias characteristics of Silicon diode

Forward Bias Condition:

S. No.	Forward Voltage across the diode V_d (Volt)	Forward Current through the diode I_d (mA)

Reverse Bias Condition:

S. No.	Reverse Voltage across the diode V_R (Volt)	Reverse Current through the diode I_R (µA)

(b) Forward & Reverse bias characteristics of Germanium diode

Forward Bias Condition:

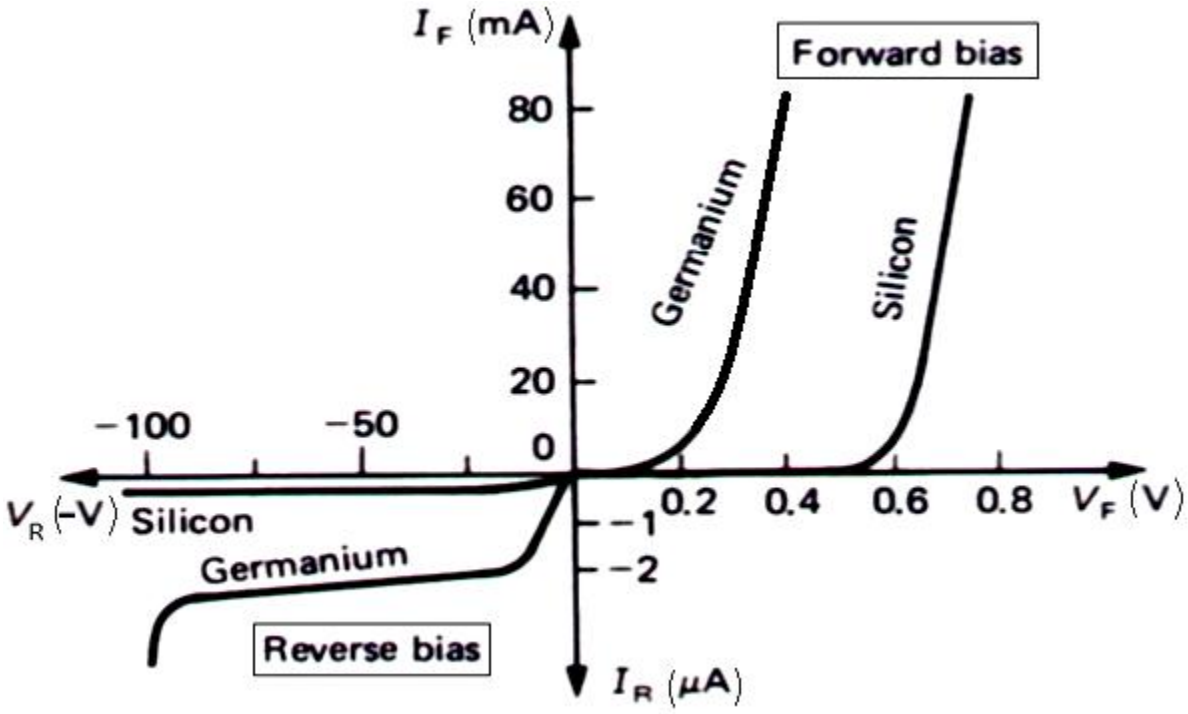
S. No.	Forward Voltage across the diode V_d (Volt)	Forward Current through the diode I_d (mA)

Reverse Bias Condition:

S. No.	Reverse Voltage across the diode V_r (Volt)	Reverse Current through the diode I_R (µA)

Graphs:

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark +ve X-axis as V_f, -ve X-axis as V_R, +ve Y-axis as I_f and –ve Y-axis as I_R.
3. Mark the readings tabulated for Si forward biased condition in first Quadrant and Si reverse biased condition in third Quadrant.
4. Repeat the same procedure for plotting the Germanium characteristics.



Calculations from Graph:

Static forward Resistance

$$R_{dc} = V_f / I_f \Omega$$

Static Reverse Resistance

$$R_{dc} = V_r / I_r \Omega$$

Dynamic Forward Resistance

$$r_{ac} = \Delta V_f / \Delta I_f \Omega$$

Dynamic Reverse Resistance

$$r_{ac} = \Delta V_r / \Delta I_r \Omega$$

Precautions:

1. While doing the experiment do not exceed the readings of the diode. This may lead to damaging of the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Results:

Cut in voltage = _____ V

Static Forward Resistance = _____ Ω

Dynamic Forward Resistance = _____ Ω

Static Reverse Resistance = _____ Ω

Dynamic Reverse Resistance = _____ Ω

V-I Characteristics of Silicon & Germanium P-N Junction Diodes are studied.

Viva Questions

1. What are trivalent and pentavalent impurities?

Ans: Doping is the process of adding impurity atoms to intrinsic silicon or germanium to improve the conductivity of the semiconductor.

Commonly Used Doping Elements

Trivalent Impurities to make p-Type: Aluminum (Al), Gallium (Ga), Boron(B) and Indium (In).

Pentavalent Impurities to make n-type: Phosphorus (P), Arsenic (As), Antimony (Sb) and Bismuth (Bi).

2. How PN junction diode does acts as a switch?

Ans: Apply voltage in one direction; it acts like an open circuit. Reverse the polarity of the voltage and it acts like a short circuit.

3. Diode current equation?

Ans: $I = I_S(e^{V_D/(\eta V_T)} - 1)$

4. What is the value of V_t at room temperature?

Ans: 25mV

5. What is cut-in-voltage?

Ans: The forward voltage at which the current through the junction starts increasing rapidly is called as the cut-in voltage. It is generally 0.7V for a Silicon diode and 0.3V for a germanium diode.

6. Dynamic resistance expression?

Ans: $r_d = \Delta V/\Delta I = \frac{\eta V_T}{I}$

Experiment No.:3

Zener Diode Characteristics

Aim: To plot V-I Characteristics of Zener Diode.

Components:

Name	Quantity
Zener Diodes 1N4735A/ FZ 5.1	1
Resistor 1KΩ	1

Equipments:

Name	Range	Quantity
Bread board		1
Regulated power supply	0-30V	1
Digital Ammeter	200mA	1
Digital Voltmeter	0-20V	1
Connecting Wires		

Specifications:

Breakdown Voltage = 5.1V

Power dissipation = 0.75W

Max Forward Current = 1A

Theory: Zener diode is a heavily doped Silicon diode. An ideal P-N junction diode does not conduct in reverse biased condition. A Zener diode conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage. A Zener diode when forward biased behaves like an ordinary P-N junction diode. A Zener diode when reverse biased can undergo avalanche break down or zener break down.

Avalanche Break down:

If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction increases the kinetic energy of the charge carriers which collides with the adjacent atoms and generates charge carriers by

breaking the bond, they in-turn collides with other atoms by creating new charge carriers, this process is cumulative which results in the generation of large current resulting in **Avalanche** Breakdown.

Zener Break down:

If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces, it leads to the development of strong electric field and application of even a small voltage at the junction may rupture covalent bond and generate large number of charge carriers. Such sudden increase in the number of charge carriers results in **Zener** break down.

Circuit Diagram:

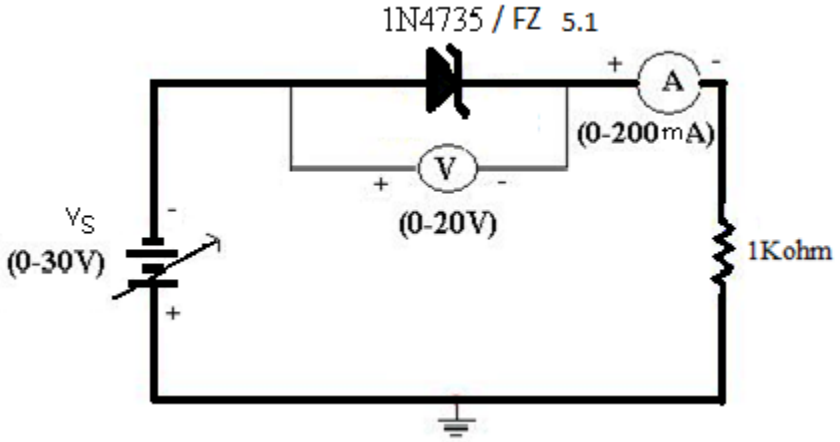


Fig. 1: Forward Bias Condition

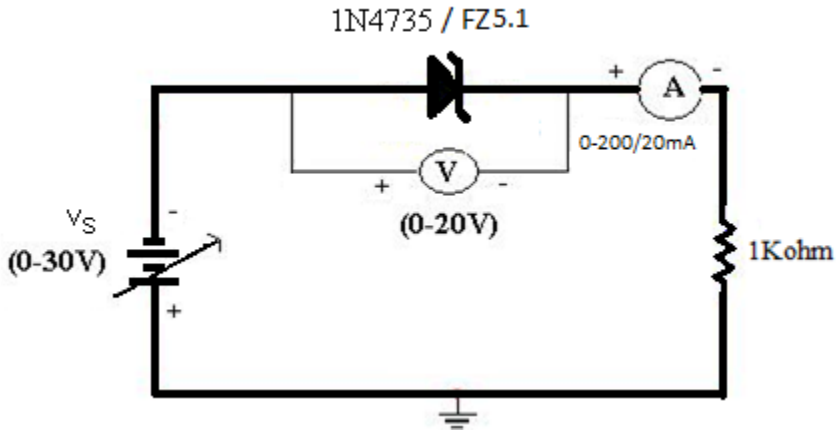


Fig. 2: Reverse Bias Condition

Procedure:

Forward Bias Condition:

1. Connect the circuit as shown in fig.1.
2. Vary V_F gradually from 0 to 0.6 V in steps of 0.1 V and in steps of 0.02 V from 0.6 to 0.76 V. In each step record the current flowing through the diode as I_F.
3. Tabulate different forward currents obtained for different forward voltages.

Reverse Bias Condition:

1. Connect the Zener diode in reverse bias as shown in the fig.2. Vary the voltage across the diode in steps of 1V from 0 V to 6 V and in steps 0.1 V till its breakdown voltage is reached. In each step note the current flowing through the diode
2. Plot a graph between V and I. This graph will be called the V-I characteristics of Zener diode. From the graph find out the breakdown voltage for the diode.

Observations:

Forward Bias Condition:

S. No.	Forward Voltage across the diode V_F (volts)	Forward Current through the diode I_F (mA)

Reverse Bias Condition:

S. No.	Reverse Voltage across the diode V_R (volts)	Reverse Current through the diode I_R (mA)

Graph:

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark +ve X-axis as V_F, -ve X-axis as V_R, +ve Y-axis as I_F and –ve Y-axis as I_R.
3. Mark the readings tabulated for forward biased condition in first Quadrant and reverse biased condition in third Quadrant.

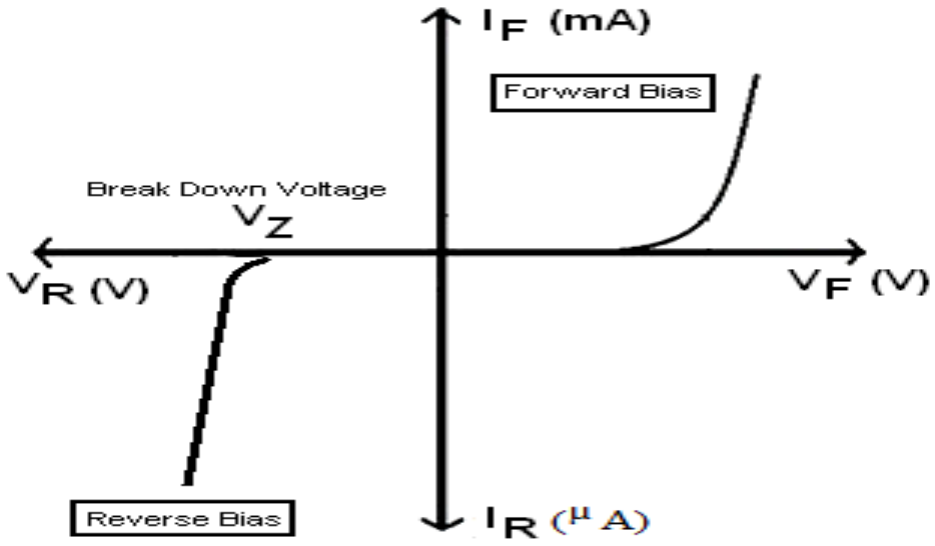


Fig. 3: V-I Characteristics of Zener Diode

Calculations from Graph:

Precautions:

1. While doing the experiment do not exceed the readings of the diode. This may lead to damaging of the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Results:

1. The Zener Diode Characteristics have been studied.
2. The breakdown voltage of Zener diode in reverse bias was found to be = _____

Viva Questions

1. What is the difference between p-n Junction diode and zener diode?

Ans: A zener is designed to operate stably in reverse breakdown, which is designed to be at a low voltage, between 3 volts and 200 volts. The breakdown voltage is specified as a voltage with a tolerance, such as 10 volts ±5%, which means the breakdown voltage (or operating voltage) will be between 9.5 volts and 10.5 volts. A signal diode or rectifier will have a high reverse breakdown, from 50 to 2000 volts, and is NOT designed to operate in the breakdown region. So exceeding the reverse voltage may result in the device being damaged. In addition, the breakdown voltage is specified as a minimum only. Forward characteristics are similar to both, although the zener's forward characteristics is usually not specified, as the zener will never be used in that region. A signal diode or rectifier has the forward voltage specified as a max voltage at one or more current levels.

2. What is break down voltage?

Ans: The breakdown voltage of a diode is the minimum reverse voltage to make the diode conduct in reverse.

3. What are the applications of Zener diode?

Ans: Zener diodes are widely used as voltage references and as shunt regulators to regulate the voltage across small circuits.

4. What is cut-in-voltage ?

Ans: The forward voltage at which the current through the junction starts increasing rapidly, is called the knee voltage or cut-in voltage. It is generally 0.6v for a Silicon diode.

5. What is voltage regulator?

Ans: A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations.

Experiment No: 4

Characteristics of BJT in Common Emitter Configuration

Aim: To plot the Characteristics of a BJT in Common Emitter Configuration.

Components:

Name	Quantity
Transistor BC 107	1
Resistor 1KΩ	1

Equipment:

Name	Range	Quantity
Bread Board		1
Regulated power supply	0-30V	2
Digital Ammeter	0-200mA/0-200μA	1
Digital Voltmeter	0-20V	2
Connecting Wires		

Specifications:

For Transistor BC 107:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

A BJT is called as Bipolar Junction Transistor and it is a three terminal active device which has emitter, base and collector as its terminals. It is called as a bipolar device because the flow of current through it is due to two types of carriers i.e., majority and minority carriers.

A transistor can be in any of the three configurations viz, Common base, Common emitter and Common Collector.

The relation between $\boldsymbol{\alpha}$ **,** $\boldsymbol{\beta}$ **,** $\boldsymbol{\gamma}$ **of CB, CE, CC are**

$$\boldsymbol{\alpha} = \frac{\boldsymbol{\beta}}{\mathbf{1}+\boldsymbol{\beta}} \qquad \boldsymbol{\beta} = \frac{\boldsymbol{\alpha}}{\mathbf{1}-\boldsymbol{\alpha}} \qquad \boldsymbol{\gamma} = \mathbf{1} + \boldsymbol{\beta} = \frac{\mathbf{1}}{\mathbf{1}-\boldsymbol{\alpha}}$$

In CE configuration base will be input node and collector will be the output node .Here emitter of the transistor is common to both input and output and hence the name common emitter configuration.

The collector current is given as

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Where I_{CO} is called as reverse saturation current

A transistor in CE configuration is used widely as an amplifier. While plotting the characteristics of a transistor the input voltage and output current are expressed as a function of input current and output voltage.

i.e, $V_{BE} = f (I_B, V_{CE})$ and

$I_C = f (I_B, V_{CE})$

Transistor characteristics are of two types.

Input characteristics:- Input characteristics are obtained between the input current and input voltage at constant output voltage. It is plotted between V_{BE} and I_B at constant V_{CE} in CE configuration

Output characteristics:- Output characteristics are obtained between the output voltage and output current at constant input current. It is plotted between V_{CE} and I_C at constant I_B in CE configuration

The different regions of operation of the BJT are

Emitter Junction	Collector Junction	Region	Application
RB	RB	CUTT OFF	OFF SWITCH
FB	FB	SATURATION	ON SWITCH
FB	RB	ACTIVE	AMPLIFIER
RB	FB	REVERSE ACTIVE	ATTENUATOR

Circuit Diagram:

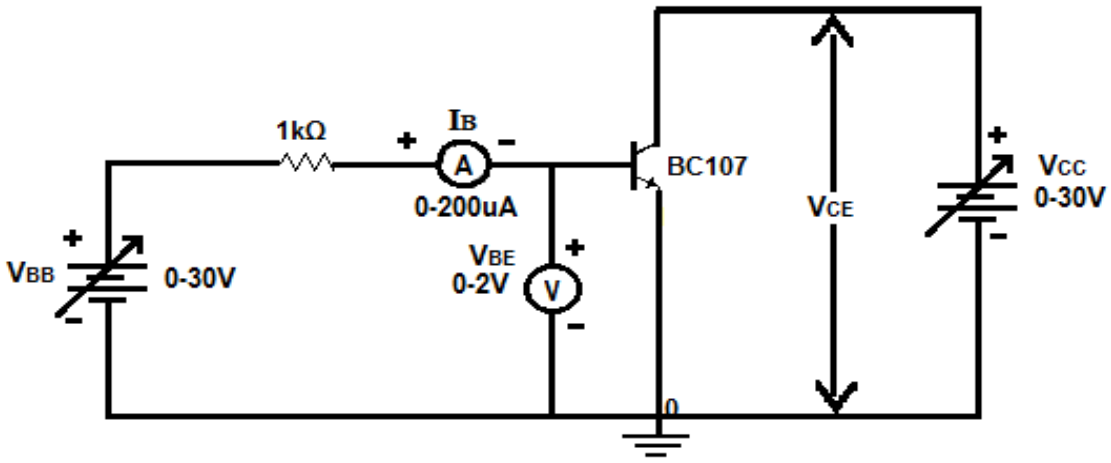


Fig. 1: Input Characteristics

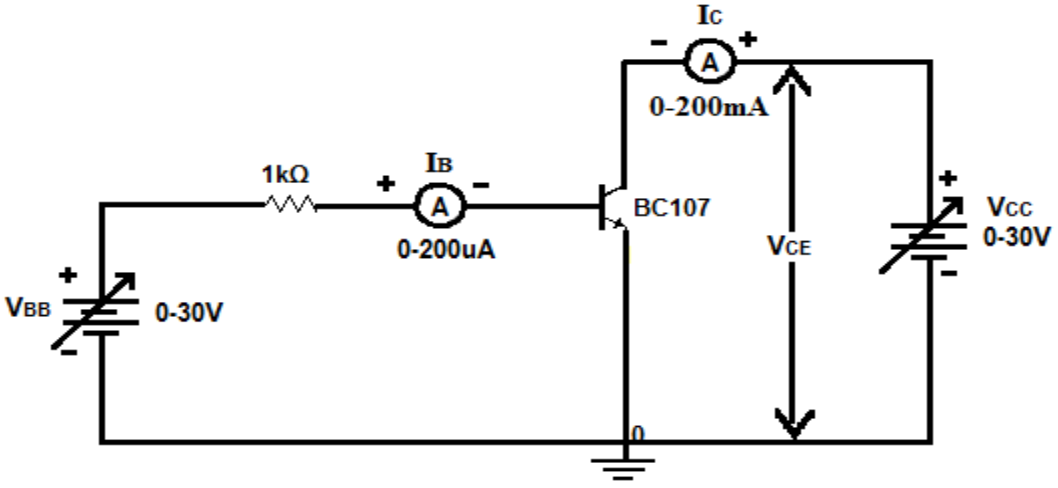
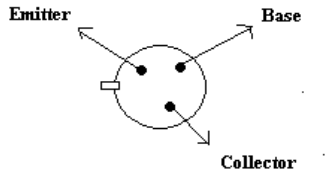


Fig. 2: Output Characteristics

Pin assignment of Transistor:



Procedure:

Input Characteristics:

1) Connect the circuit as shown in fig.(1). Adjust all the knobs of the power supply to their minimum positions before switching the supply on.
2) Adjust the V_{CE} to 0 V by adjusting the supply $V_{CC.}$
3) Vary the supply voltage V_{BB} so that V_{BE} varies in steps of 0.1 V from 0 to 0.5 V and then in steps of 0.02 V from 0.5 to 0.7 V. In each step note the value of base current I_B.
4) Adjust V_{CE} to 1, 2V and repeat step-3 for each value of $V_{CE.}$
5) Plot a graph between V_{BE} and I_B for different values of V_{CE}. These curves are called input characteristic

Output Characteristics:

1) Connect the circuit as shown in fig. (2). All the knobs of the power supply must be at the minimum position before the supply is switched on.
2) Adjust the base current I_B to 20 μA by adjusting the supply V_{BB}.
3) Vary the supply voltage V_{CC} so that the voltage V_{CE} varies in steps of 0.2 V from 0 to 2 V and then in steps of 1 V from 2 to 10 V. In each step the base current should be adjusted to the present value and the collector current I_C should be recorded.
4) Adjust the base current at 40, 60 μA and repeat step-3 for each value of I_B.
5) Plot a graph between the output voltage V_{CE} and output current I_C for different values of the input current I_B. These curves are called the output characteristics.

Observations:

Input Characteristics

V_{CE} = 0V		V_{CE} = 2V	
V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)

Output Characteristics

I_B = 20µA		I_B = 40µA		I_B = 60µA	
V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

Graph:

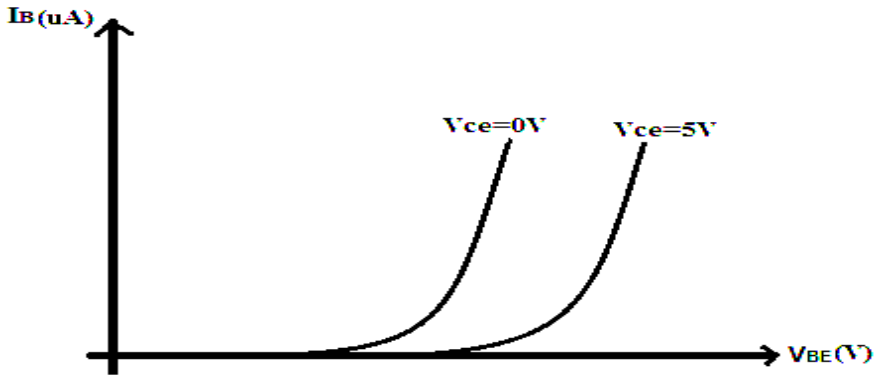


Fig. 3: Input Characteristics

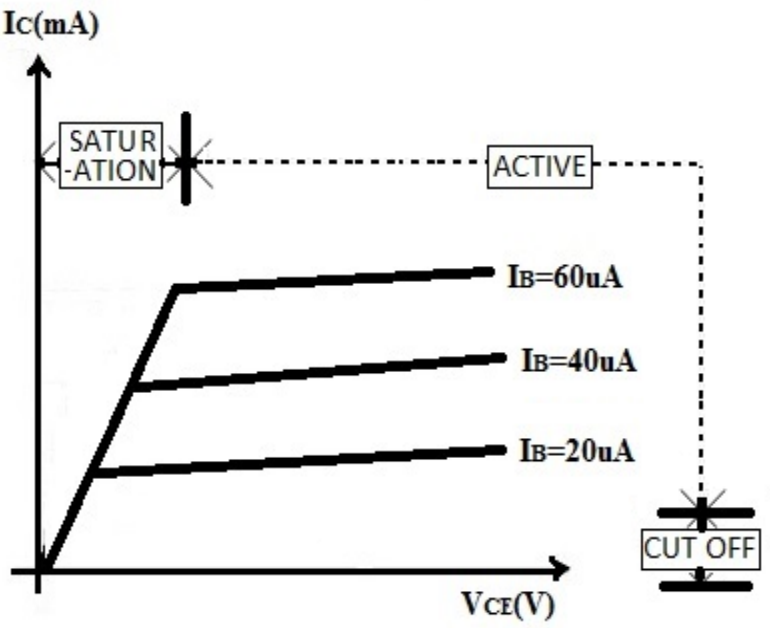


Fig. 4: Output Characteristics

Precautions:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Results:

Input and output Characteristics of a BJT in Common Emitter Configuration are studied.

Viva Questions

1. What is transistor?

Ans: A transistor is a semiconductor device used to amplify and switch electronic signals and electrical power. It is composed of semiconductor material with at least three terminals for connection to an external circuit. The term transistor was coined by John R. Pierce as a portmanteau of the term "transfer resistor".

2. Write the relation between α, β and γ?

Ans: $\alpha = \frac{\beta}{1+\beta}$ $\beta = \frac{\alpha}{1-\alpha}$ $\gamma = 1 + \beta = \frac{1}{1-\alpha}$

3. What is the range of α ?

Ans: The important parameter is the common-base current gain, α. The common-base current gain is approximately the gain of current from emitter to collector in the forward-active region. This ratio usually has a value close to unity; between 0.98 and 0.998.

4. Why is α is less than unity?

Ans: It is less than unity due to recombination of charge carriers as they cross the base region.

5. Input and output impedance equations for CB configuration?

Ans: $h_{ib}=V_{EB}/I_E, 1/h_{ob}=V_{CB}/I_C$

6. Can we replace transistor by two back to back connected diodes?

Ans: No, because the doping levels of emitter (heavily doped), base(lightly doped) and collector(doping level greater than base and less than emitter) terminals are different from p and n terminals in diode.

7. For amplification CE is preferred, why?

Ans: Because amplification factor beta is usually ranges from 20-500 hence this configuration gives appreciable current gain as well as voltage gain at its output on the other hand in the Common Collector configuration has very high input resistance(~750KΩ) & very low output resistance(~25Ω) so the voltage gain is always less than one & its most important application is for impedance matching for driving from low impedance load to high impedance source

8. To operate a transistor as amplifier, emitter junction is forward biased and collector junction is reverse biased, why?

Ans: Voltage is directly proportional to Resistance. Forward bias resistance is very less compared to reverse bias. In amplifier input forward biased and output reverse biased so voltage at output increases with reverse bias resistance.

9. Which transistor configuration provides a phase reversal between the input and output signals?

Ans: Common emitter configuration (180 DEG)

10. What is the range if β?

Ans: β usually ranges from 20-500.

Experiment No: 5

Characteristics of JFET in Common source Configuration

Aim:

1. To study Drain Characteristics and Transfer Characteristics of a Junction Field Effect Transistor (JFET).
2. To measure drain resistance, trans-conductance and amplification factor.

Components:

Name	Quantity
JFET BFW 11	1
Resistor 1MΩ	1

Equipment:

Name	Range	Quantity
Bread Board		1
Regulated power supply	0-30V	1
Digital Ammeter	0-200mA	1
Digital Voltmeter	0-20V	2
Connecting Wires		

Specifications:

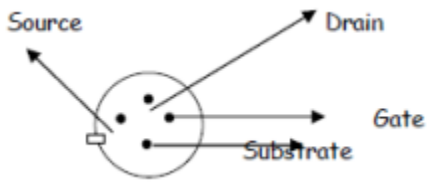
For FET BFW11:

Gate Source Voltage V_{GS} = -30V

Forward Gain Current I_{GF} = 10mA

Maximum Power Dissipation P_D = 300mW

Pin assignment of FET:



Circuit Diagram:

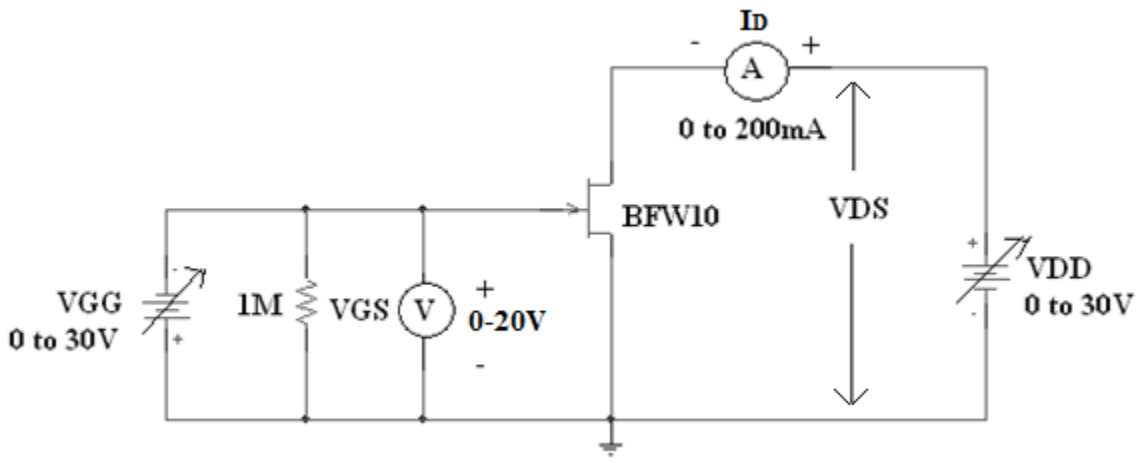


Fig. 1: Characteristics of FET

Theory:

A JFET is called as Junction Field effect transistor. It is a unipolar device because the flow of current through it is due to one type of carriers i.e., majority carriers where as a BJT is a Bi - Polar device, It has 3 terminals Gate, Source and Drain. A JFET can be used in any of the three configurations viz, Common Source, Common Gate and Common Drain. The input gate to source junction should always be operated in reverse bias, hence input resistance $R_i = \infty$, $I_G \approx 0$.

Pinch off voltage V_P is defined as the gate to source reverse bias voltage at which the output drain current becomes zero.

In CS configuration Gate is used as input node and Drain as the output node. A JFET in CS configuration is used widely as an amplifier. A JFET amplifier is preferred over a BJT amplifier when the demand is for smaller gain, high input resistance and low output resistance. Any FET operation is governed by the following equation.

The drain current equation and trans-conductance is given as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 , \qquad g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2}{|v_p|}\sqrt{I_D\, I_{DSS}}$$

Where I_{DSS} is called as Drain to Source Saturation current & V_p is called as the Pinch off voltage

Procedure:

Transfer Characteristics:

1) Connect the circuit as shown. All the knobs of the power supply must be at the minimum position before the supply is switched on.
2) Adjust the output voltage V_{DS} to 4V by adjusting the supply V_{DD}.
3) Vary the supply voltage V_{GG} so that the voltage V_{GS} varies in steps of -0.25 V from 0 V onwards. In each step note the drain current I_D. This should be continued till I_D becomes zero.
4) Repeat above step for V_{DS} = 8 V.
5) Plot a graph between the input voltage V_{GS} and output current I_D for output voltage V_{DS} in the second quadrant. This curve is called the transfer characteristics.

Drain Characteristics:

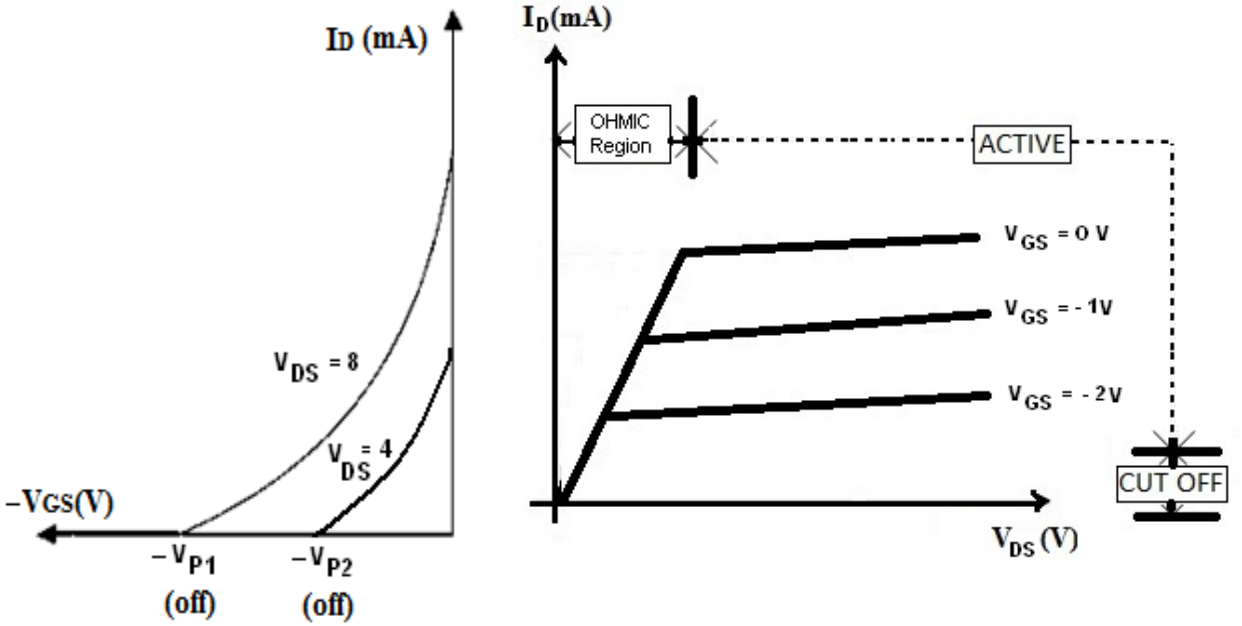
1) Connect the circuit as shown in figure. Adjust all the knobs of the power supply to their minimum positions before switching the supply on.
2) Adjust the input voltage V_{GS} to 0 V by adjusting the supply $V_{GG.}$
3) Vary the supply voltage V_{DD} so that V_{DS} varies in steps of 0.5 V from 0 to 4 V and then in steps of 1 V from 4 to 10 V. In each step note the value of drain current I_D.
4) Adjust V_{GS} to -1 and -2 V and repeat step-3 for each value of $V_{GS.}$
5) Plot a graph between V_{DS} and I_D for different values of V_{GS}. These curves are called drain characteristics.
6) Mark the various regions in the drain characteristics graph and calculate the drain resistance.

Observations:

Transfer Characteristics			
V_{DS} = 4V		V_{DS} = 6V	
V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)

Drain Characteristics					
V_{GS} = 0V		V_{GS} = -1V		V_{GS} = -2V	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

Graph:



Transfer Characteristics

Drain Characteristics

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at a constant V_{GS}.
2. Plot the transfer characteristics by taking V_{GS} on X-axis and taking I_D on Y-axis at constant V_{DS}.

Calculations from Graph:

1. **Drain Resistance (r_d):** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region.
2. **Trans Conductance (gm):** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.

gm $= \dfrac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS} (from transfer characteristics).

The value of **gm** is expressed in mho's ($\mho$) or Siemens (**s**).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

Precautions:

1. While performing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the transistor.

Results:

1. Drain Characteristics and Transfer Characteristics of a Field Effect (FET) Transistor are studied.
2. Drain resistance, trans-conductance and amplification factor are measured.

Viva Questions

1. Why FET is called a Unipolar device?

Ans: FETs are unipolar transistors as they involve single-carrier-type operation.

2. What are the advantages of FET?

Ans: The main advantage of the FET is its high input resistance, on the order of 100 MΩ or more. Thus, it is a voltage-controlled device, and shows a high degree of isolation between input and output. It is a unipolar device, depending only upon majority current flow. It is less noisy. and is thus found in FM tuners and in low-noise amplifiers for VHF and satellite receivers. It is relatively immune to radiation. It exhibits no offset voltage at zero drain current and hence makes an excellent signal chopper. It typically has better thermal stability than a bipolar junction transistor (BJT)

3. What is trans-conductance?

Ans: Trans-conductance is an expression of the performance of a bipolar transistor or field-effect transistor (FET). In general, the larger the trans-conductance figure for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. The symbol for trans-conductance is gm. The unit is Siemens, the same unit that is used for direct-current (DC) conductance.

4. What are the disadvantages of FET?

Ans: It has a relatively low gain-bandwidth product compared to a BJT. The MOSFET has a drawback of being very susceptible to overload voltages, thus requiring special handling during installation.The fragile insulating layer of the MOSFET between the gate and channel makes it vulnerable to electrostatic damage during handling. This is not usually a problem after the device has been installed in a properly designed circuit.

5. Relation between μ, g_m and r_d?

Ans: $\mu = g_m * r_d$

Experiment No: 6

Half Wave and Full Wave Rectifier without Filter

Aim: (i) To study the operation of Half wave and Full wave rectifier without filter

(ii) To find its:

1. Ripple Factor
2. Efficiency
3. Percentage Regulation

Components:

Name	Quantity
Diodes 1N4007(Si)	2
Resistor 1KΩ	1

Equipments:

Name	Range	Quantity
CRO	(0-20)MHz	1
CRO probes		2
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
Transformer	220V/9V, 50Hz	1
Connecting Wires		

Specifications:

Silicon Diode 1N4007:

Max. Forward Current = 1A

Max. Reverse Current = 5.0µA

Max. Forward Voltage = 0.8V

Max. Reverse Voltage = 1000V

Max. Power Dissipation = 30mW

Temperature = -65 to 200° C

Theory:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components.

A half wave rectifier makes use of single diode to carry out this conversion. It is named so as the conversion occurs for half input signal cycle. During the positive half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor. During the negative half cycle, the diode is reverse biased and it is equivalent to an open circuit, hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half wave rectified output.

A full wave rectifier makes use of a two diodes to carry out this conversion. It is named so as the conversion occurs for complete input signal cycle. The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased it results in a current Id1 through the load R. During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased. Resulting in a current Id2 through the load at the same instant a negative voltage appears at the anode of D1 thus reverse biasing it and hence it doesn't conduct.

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol 'γ'.

$$\gamma_{HWR} = \frac{V_{AC}}{V_{DC}} = 1.21 \qquad \gamma_{FWR} = \frac{V_{AC}}{V_{DC}} = 0.48$$

Rectification Factor:

The ratio of output DC power to input AC power is defined as efficiency.

$$\eta = \frac{(V_{DC})^2}{(V_{AC})^2} \qquad \eta_{HWR} = 40.6\% \qquad \eta_{FWR} = 81\%$$

Percentage of Regulation:

It is a measure of the variation of AC output voltage as a function of DC output voltage.

Percentage of regulation = $(\frac{V_{NL} - V_{FL}}{V_{FL}}) * 100$ %

V_{NL} = Voltage across load resistance, when minimum current flows through it.

V_{FL} = Voltage across load resistance, when maximum current flows through.

For an ideal rectifier, the percentage regulation is 0 percent. The percentage of regulation is very small for a practical half wave and full wave rectifier.

Peak- Inverse – Voltage (PIV):

It is the maximum voltage that has to be with stood by a diode when it is reverse biased

$PIV_{HWR} = Vm$ $PIV_{FWR} = 2Vm$

Comparison of Half-wave and Full-wave rectifier

S. No.	Particulars	Type of Rectifier	
		Half-Wave	Full-Wave
1.	No. of diodes	1	2
2.	Maximum Rectification Efficiency	40.6%	81.2%
3.	$V_{d.c}$ (no load)	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$
4.	Ripple Factor	1.21	0.48
5.	Peak Inverse Voltage	V_m	$2V_m$
6.	Output Frequency	f	2f
7.	Transformer Utilization Factor	0.287	0.693

Circuit Diagram:

Half wave Rectifier (without filter):

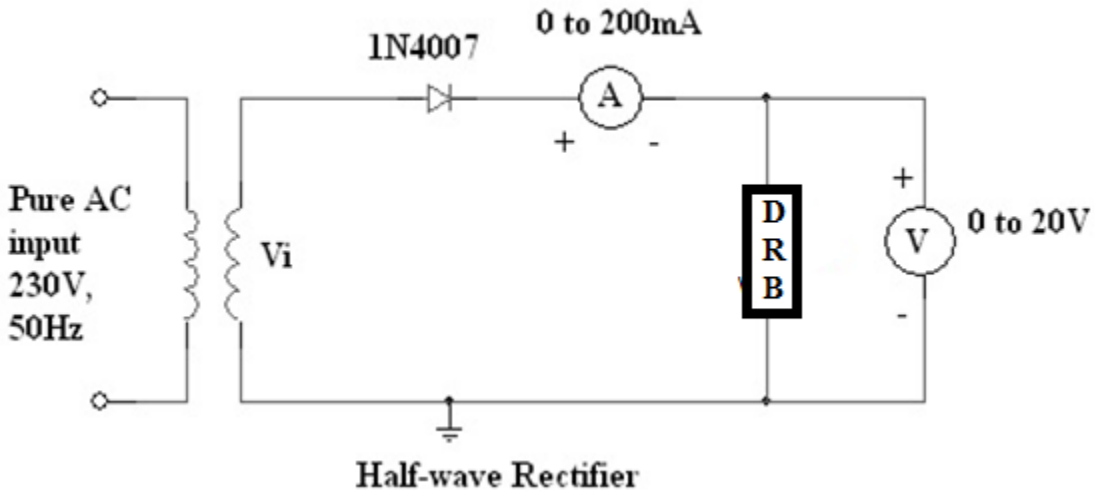


Fig. 1: Circuit diagram of Half-wave rectifier

Full Wave Rectifier (without filter):

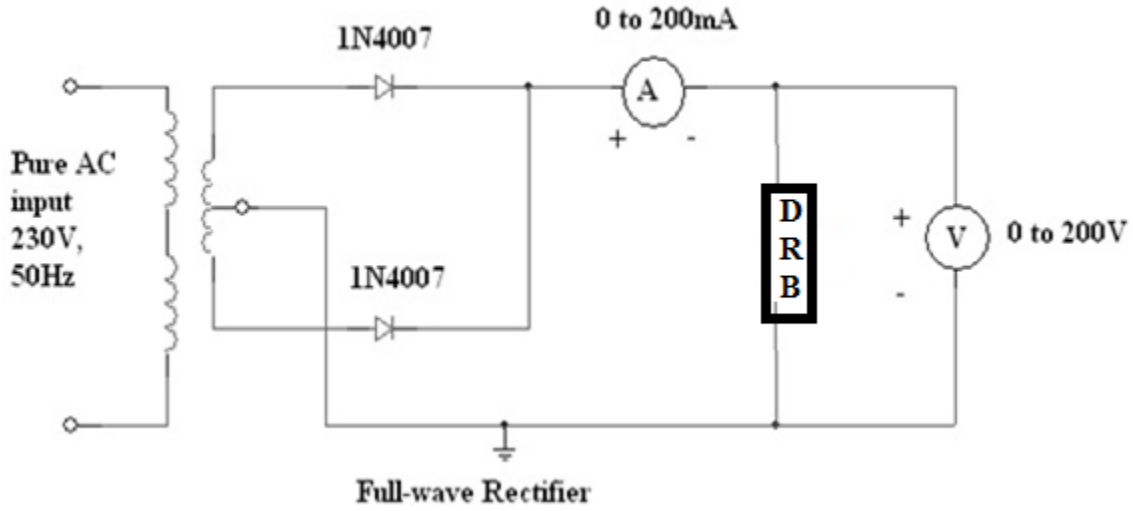


Fig. 2: Circuit diagram of Full wave rectifier

Procedure:

PART-I: Half wave rectifier without filter

1. Connect the circuit as shown in the fig.1.
2. Connect the multimeter across the 1kΩ load.
3. Measure the AC and DC voltages by setting multimeter to ac and dc mode respectively.
4. Now calculate the ripple factor using the following formula.

$$\text{Ripple factor } (\gamma) = \frac{V_{AC}}{V_{DC}}$$

5. Connect the CRO channel-1 across input and channel-2 across output i.e load and Observe the input and output Waveforms.
6. Now calculate the peak voltage of input and output waveforms and also the frequency.

PART-II: Full wave rectifier without filter

1. Connect the circuit as shown in the fig.2.
2. Repeat the above steps 2-6
3. Plot different graphs for wave forms and calculate ripple factor

Observations:

Half wave rectifier without Filter

Load Resistance (R_L)	V_{AC}(V)	V_{DC}(V)	Ripple Factor $\gamma=\frac{Vac}{Vdc}$	Input Signal		Output Signal	
				Vm p-p(v)	Frequency (Hz)	Vm p-p(v)	Frequency (Hz)

Full wave rectifier without Filter

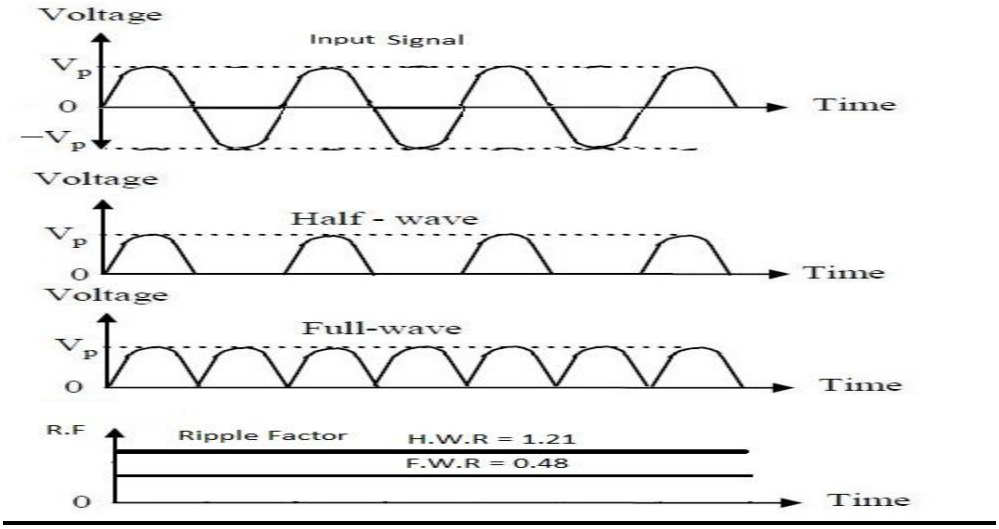
Load Resistance (R_L)	V_{AC}(V)	V_{DC}(V)	Ripple Factor $\gamma=\frac{Vac}{Vdc}$	Input Signal		Output Signal	
				Vm p-p(v)	Frequency (Hz)	Vm p-p(v)	Frequency (Hz)

Calculations:

1. Ripple Factor = $\gamma_{HWR} = \frac{V_{AC}}{V_{DC}}$

2. Percentage Regulation = $\frac{V_{NL}-V_{FL}}{V_{FL}} \times 100$

Expected Waveforms:



Results:

1. Half Wave and Full Wave rectifier characteristics are studied.
2. Ripple factor of Half wave rectifier = ----------
3. Ripple factor of Full wave rectifier = ----------
4. Regulation of Half wave rectifier = ----------
5. Regulation of Full wave rectifier = ----------

Viva Questions

1. What is a rectifier?

Ans: A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification.

2. What is a ripple factor?

Ans: Ripple factor can be defined as the variation of the amplitude of DC (Direct current) due to improper filtering of AC power supply. it can be measured by RF = v_{rms} / v_{dc}

3. What is efficiency?

Ans: Rectifier efficiency is the ratio of the DC output power to the AC input power.

4. What is PIV?

Ans: The peak inverse voltage is either the specified maximum voltage that a diode rectifier can block, or, alternatively, the maximum that a rectifier needs to block in a given application.

5. What are the applications of rectifier?

Ans: The primary application of rectifiers is to derive DC power from an AC supply. Virtually all electronic devices require DC, so rectifiers are used inside the power supplies of virtually all electronic equipment. Rectifiers are also used for detection of amplitude modulated radio signals. rectifiers are used to supply polarized voltage for welding.

6. Give some rectifications technologies?
Ans: Synchronous rectifier, Vibrator, Motor-generator set, Electrolytic ,Mercury arc, and Argon gas electron tube.

7. What is the efficiency of bridge rectifier?
Ans: 81 %

Experiment No: 7

Half Wave and Full Wave Rectifier with Filter

Aim: (i) To study the operation of a Half wave and Full wave rectifier with filters

(ii) To find its:

1. Ripple Factor
2. Percentage Regulation

Components:

Name	Quantity
Diodes 1N4007(Si)	2
Resistor 1KΩ	1
Capacitor 100μF	2
Inductor (35 mH),	1

Equipment:

Name	Range	Quantity
CRO	(0-20)MHz	1
CRO probes		2
Digital Ammeter, Voltmeter	[0-200μA/200mA], [0-20V]	1
Transformer	220V/9V, 50Hz	1
Connecting Wires		

Specifications:

Silicon Diode 1N4007:

Max Forward Current = 1A

Max Reverse Current = 5.0μA

Max Forward Voltage = 0.8V

Max Reverse Voltage = 1000V

Max Power Dissipation = 30mW

Temperature = -65 to 200° C

Theory:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components. In DC supplies, a rectifier is often followed by a filter circuit which converts the pulsating DC signal into pure DC signal by removing the AC component. An L-section filter consists of an inductor and a capacitor connected in the form of an inverted L. A π- section filter consists of two capacitors and one induction in the form symbol pi.

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol 'γ'.

$$\gamma_{HWR\ L-section} = \frac{V_{AC}}{V_{DC}} = \frac{\pi}{2\sqrt{2}} \frac{X_C}{X_L} \qquad \text{where} \quad X_L = \omega L,\ X_C = \frac{1}{\omega C}$$

$$\gamma_{FWR\ \pi-section} = \frac{V_{AC}}{V_{DC}} = \sqrt{2} \frac{X_{C1}\ X_{C2}}{R\ X_L} \qquad \text{where} \quad X_L = 2\omega L,\ X_C = \frac{1}{2\omega C}$$

Circuit Diagram:

Half Wave Rectifier (with L-section filter):

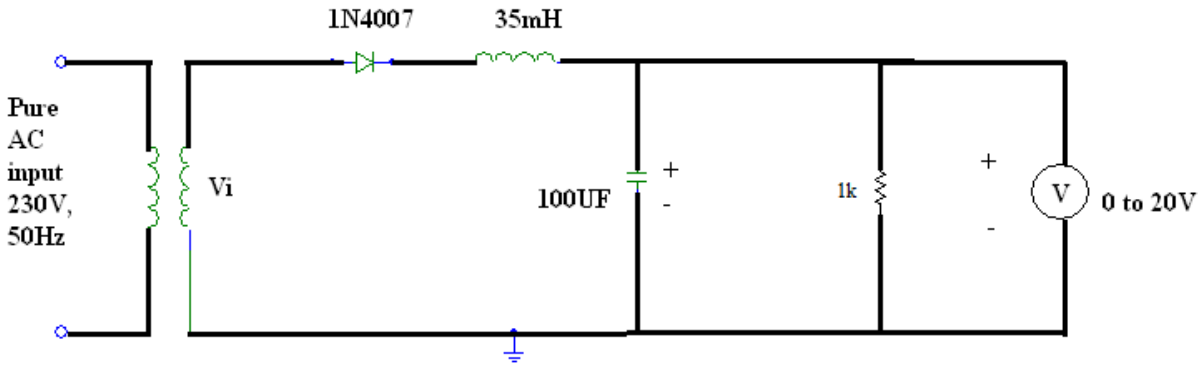


Fig. 1: Half wave rectifier with L-section Filter

Full Wave Rectifier (with π-section filter):

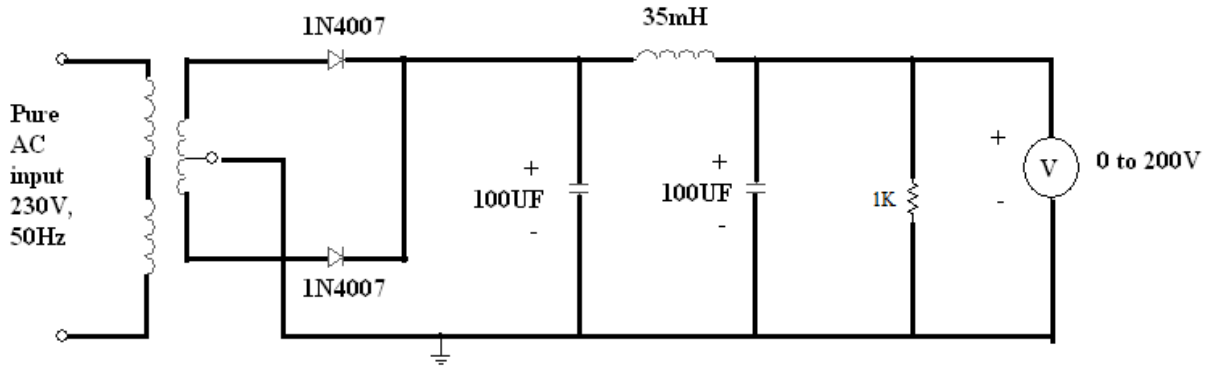


Fig. 2: Full wave rectifier with π-section filter

Procedure:

PART-I: Half wave rectifier with L-section filter

1. Connect the circuit as shown in the fig.1.
2. Connect the multimeter across the 1kΩ load.
3. Measure the AC and DC voltages by setting multimeter to ac and dc mode respectively.
4. Now calculate the ripple factor using the following formula.

$$\text{Ripple factor } (\gamma) = \frac{V_{AC}}{V_{DC}}$$

5. Connect the CRO channel-1 across input and channel-2 across output i.e load and Observe the input and output Waveforms.
6. Now calculate the peak voltage of input and output waveforms and also the frequency.

PART-II: Full wave rectifier with π-section filter

1. Connect the circuit as shown in the fig.2.
2. Repeat the above steps 2-6
3. Plot different graphs for wave forms and calculate ripple factor

Observations:

Half wave rectifier with L-section filter

Load Resistance (R_L)	V_{AC}(V)	V_{DC}(V)	Ripple Factor $\gamma=\frac{Vac}{Vdc}$	Input Signal		Output Signal	
				Vm p-p(v)	Frequency (Hz)	Vm p-p(v)	Frequency (Hz)

Full wave rectifier with pi-Section filter

Load Resistance (R_L)	V_{AC}(V)	V_{DC}(V)	Ripple Factor $\gamma=\frac{Vac}{Vdc}$	Input Signal		Output Signal	
				Vm p-p(v)	Frequency (Hz)	Vm p-p(v)	Frequency (Hz)

Calculations:

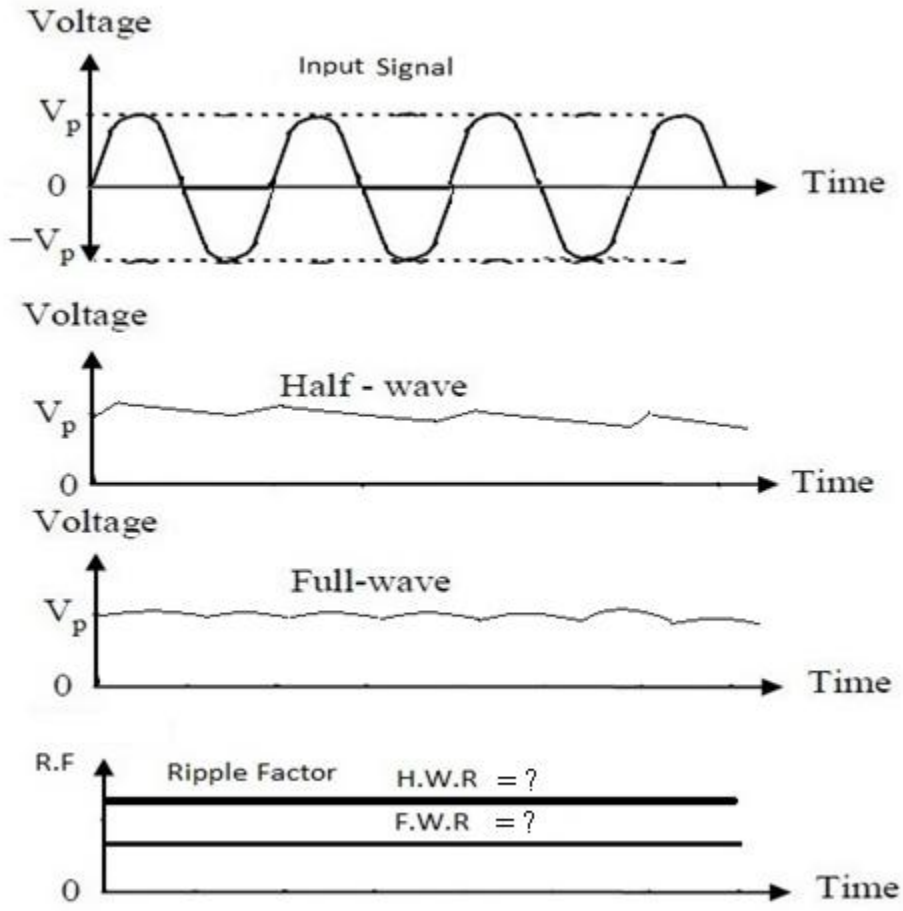
1. Ripple factor :

$$HWR_{L-SECTION} = \frac{Vac}{Vdc}$$

$$FWR_{\pi-Section} = \frac{Vac}{Vdc}$$

2. Percentage Regulation = $\frac{V_{DCNL} - VDC_{FL}}{V_{DCFL}} \times 100\ \%$

Expected Waveforms:



Results:

Full Wave rectifier characteristics are studied.

1. Ripple factor of Half wave with L-section filter = ----------
2. Ripple factor of Full wave with π-section filter = ----------
3. Regulation of Half wave with L-section filter = ----------
4. Regulation of Half wave with π -section filter = ----------

Viva Questions

1. What is filter?

Ans: Electronic filters are electronic circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal.

2. PIV center tapped FWR?

Ans: $2V_{m.}$

3. In filters capacitor is always connected in parallel, why?

Ans: Capacitor allows AC and blocks DC signal, in rectifier for converting AC to DC, capacitor placed in parallel with output, where output is capacitor blocked voltage. If capacitance value increases its capacity also increases which increases efficiency of rectifier.

Experiment No: 8

Common Emitter BJT Amplifier

Aim:

1. To plot the frequency response of a Common Emitter BJT amplifier.
2. To find the cut off frequencies, Bandwidth and calculate its gain.

Components:

Name	Quantity
Transistor BC547	1
Resistor 74KΩ, 15KΩ, 4.7KΩ, 1KΩ, 2.2KΩ, 8.2KΩ	1,1,1,1,1,1
Capacitor 10µF,100µF, 1 KPF	2, 1,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

An amplifier is an electronic circuit that can increase the strength of a weak input signal without distorting its shape. The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification with 180^0 phase shift.

The factor by which the input signal gets multiplied after passing through the amplifier circuit is called the gain of the amplifier. It is given by the ratio of the output and input signals.

Gain = output signal / input signal

A self bias circuit is used in the amplifier circuit because it provides highest Q-point stability among all the biasing circuits. Resistors R1 and R2 forms a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.

In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design it is always set to Vcc/2. This will confirm that the Q-point always swings within the active region. Output is produced without any clipping or distortion for the maximum input signal. If not reduce the input signal magnitude.

The Bypass Capacitor:

The emitter resistor is required to obtain the DC quiescent stability. However the inclusion of it in the circuit causes a decrease in amplification. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance which increases the A.C gain.

The Coupling capacitor:

An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the

amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

Frequency response :

The plot of gain versus frequency is called as frequency response. The coupling and bypass capacitors causes the gain to fall at low frequency region and internal parasitic capacitance and shunt capacitor causes the gain to fall at high frequency region. In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appear in the mid frequency range. Hence the mid band frequency gain is maximum. Hence we get a Band Pass frequency response

Characteristics of CE Amplifier:

- Large current gain.
- Large voltage gain.
- Large power gain.
- Current and voltage phase shift of 180°.
- Moderate output resistance.

Circuit Diagram:

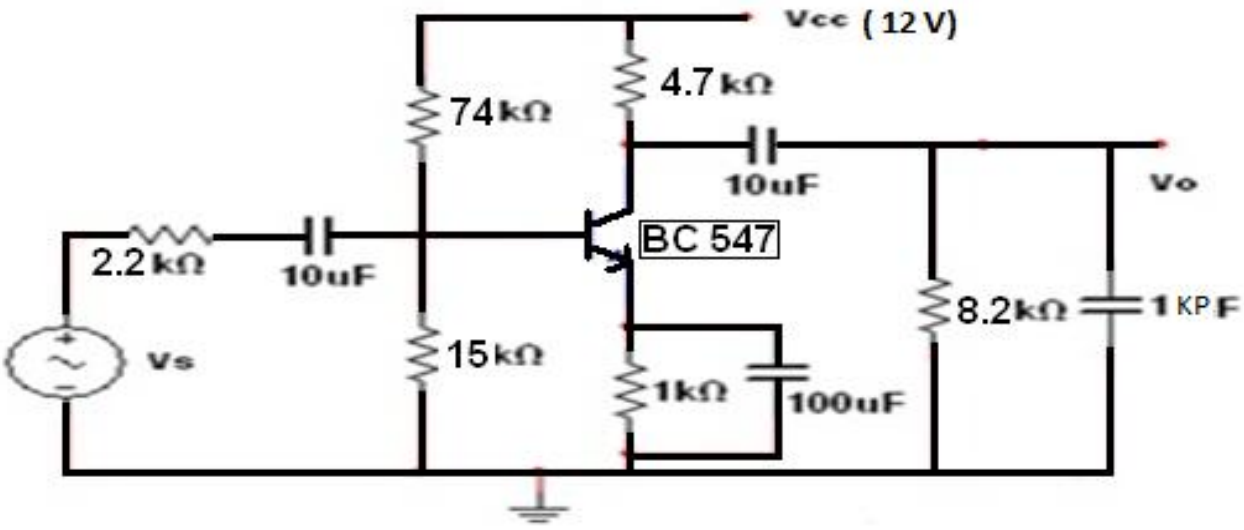


Fig. 1: CE BJT Amplifier

Procedure:

1. Connect the circuit as shown in fig.1, Set source voltage as 50mV P-P at 1 KHz frequency using the function generator.
2. Keeping the input voltage as constant, vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage.
3. Plot the graph for gain in (dB) verses Frequency on a semi log graph sheet.
4. Calculate the bandwidth from the graph.

Observations:

Frequency	Vs (Volts)	Vo(Volts)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Graph:

In the usual application, mid band frequency range is defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L, f_H and are called as the 3dB frequencies or simply the lower and higher cut off frequencies respectively. The difference between the higher cut off and lower cut off frequency is referred to as the bandwidth (f_H - f_L).

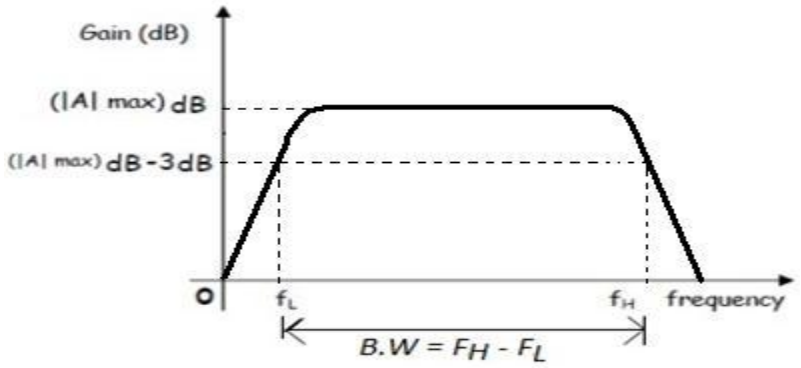


Fig. 2: Frequency Response Curve of RC coupled BJT CE Amplifier

Calculations from Graph:

Precautions:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Results:

1. The BJT CE amplifier is studied
2. The frequency response curve of the BJT CE amplifier is plotted.
3. Lower cutoff frequency, f_L = …….
   Higher cutoff frequency, f_H = ……

   Bandwidth = $f_H - f_L$ = ……

Viva Questions

1. What is the equation for voltage gain?

Ans:

$$A_V = -h_{fe} \frac{R_l'}{h_{ie}}$$

2. What is cut off frequency?

Ans: In electronics, cutoff frequency or corner frequency is the frequency either above or below which the power output of a circuit, such as a line, amplifier, or electronic filter has fallen to a given proportion of the power in the pass band. Most frequently this proportion is one half the pass band power, also referred to as the 3 dB point since a fall of 3 dB corresponds approximately to half power. As a voltage ratio this is a fall to of the pass band voltage

3. What are the applications of CE amplifier?

Ans: Low frequency voltage amplifier, radio frequency circuits and low-noise amplifiers

4. What is active region?

Ans: The active region of a transistor is when the transistor has sufficient base current to turn the transistor on and for a larger current to flow from emitter to collector. This is the region where the transistor is on and fully operating. In this region JE in forward bias and JC in reverse bias and transistor works as an amplifier

5. What is Bandwidth?

Ans: Bandwidth is the difference between the upper and lower frequencies in a continuous set of frequencies. It is typically measured in hertz, and may sometimes refer to pass band bandwidth, sometimes to baseband bandwidth, depending on context. Pass band bandwidth is the difference between the upper and lower cutoff frequencies of, for example, a band pass filter, a communication channel, or a signal spectrum. In case of a low-pass filter or baseband signal, the bandwidth is equal to its upper cutoff frequency.

Experiment No: 9

Hartley & Colpitts Oscillators

Aim: To study the operation of Hartley & Colpitts oscillator circuits and to determine their frequency of oscillations.

Components and Equipments required: HI-Q electronics Hartley oscillator trainer, HI-Q electronics Colpitts oscillator trainer, CRO, CRO probe & connecting patch cords.

Theory: An Oscillator is an electronic circuit that provides an AC output without using an AC input. All sinusoidal oscillator circuits use the concept of positive feedback to produce oscillations.

An oscillator circuit must satisfy the Barkhausen's criteria of unity loop gain to produce oscillations. Oscillators are extensively used in radio & TV receivers to generate a high frequency carrier signal in the tuning stages.

Frequency of oscillations is the frequency at which the phase of loop gain equals zero or integral multiple of 2π. Oscillations are sustained when the magnitude of loop gain equals unity.

Circuit Diagram:

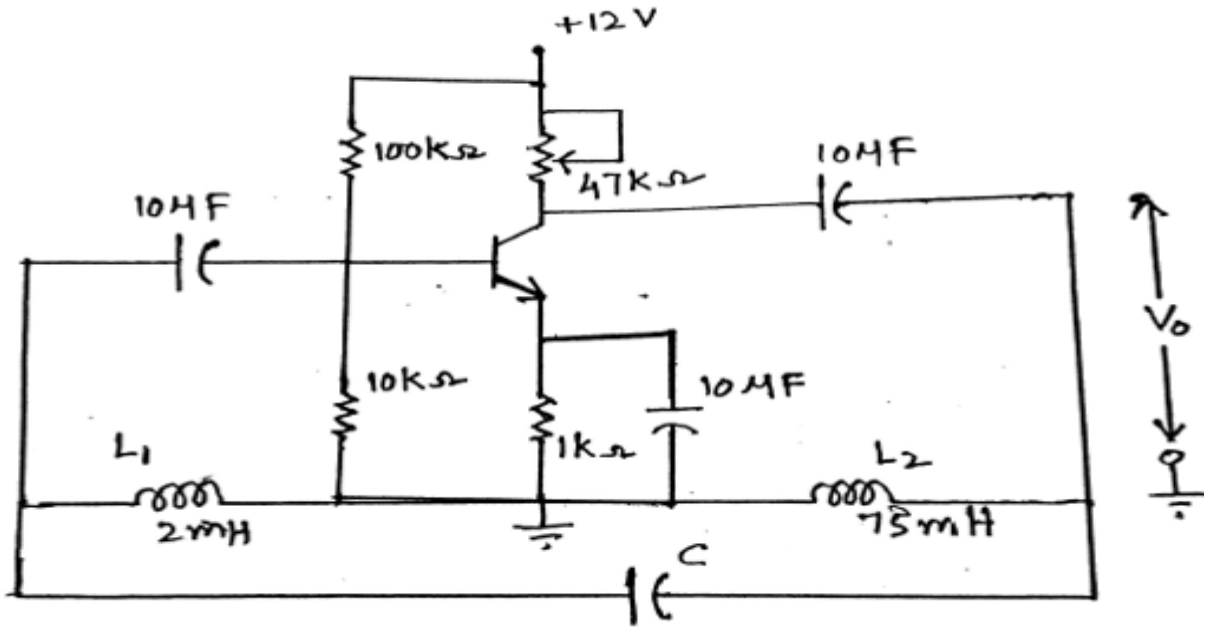


Fig. 1: Hartley oscillator

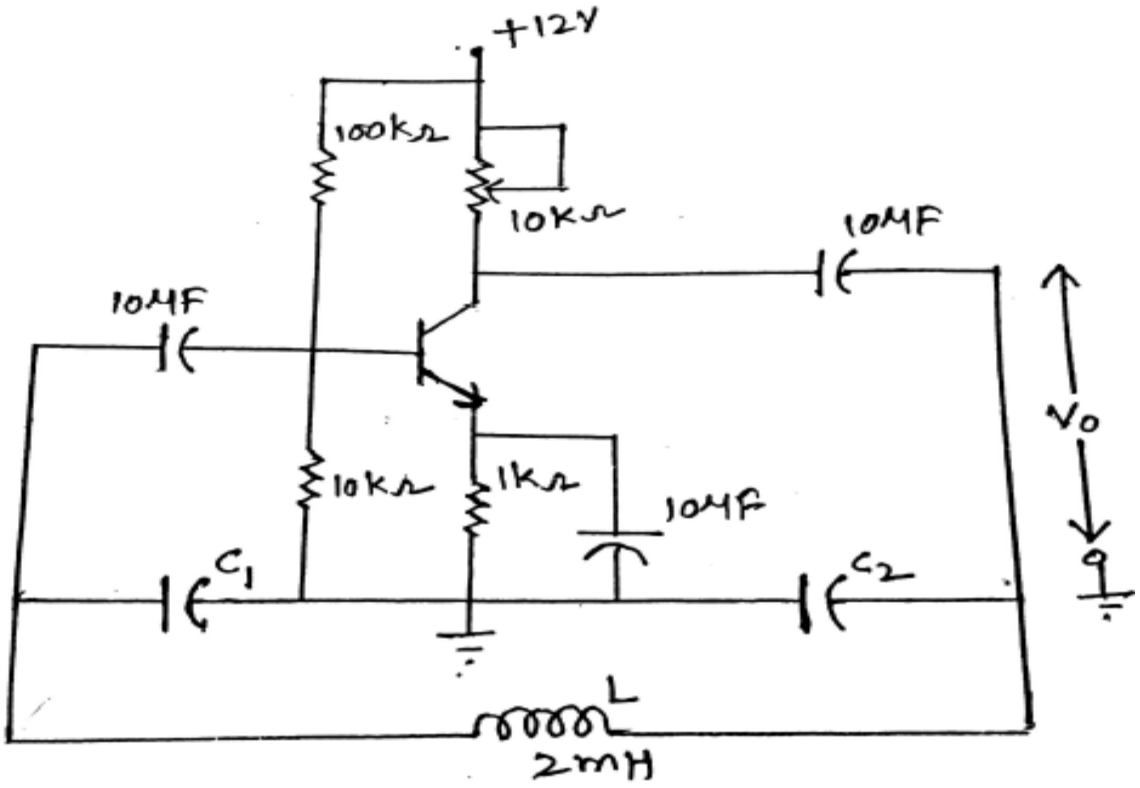


Fig. 2: Colpitts oscillator

Procedure:

Part-1: Hartley Oscillator

1) Complete the circuit as shown in Fig. 1, by connecting the capacitor C1 provided on panel of the trainer.
2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & vary the Rc till the stable oscillations are obtained on the CRO.
4) Now measure the frequency of oscillations practically.
5) Repeat the above steps for different values of capacitors C2, C3 & C4.
6) Draw the oscillations obtained on a graph sheet.

Part-2: Colpitts Oscillator

1) Complete the circuit as shown in Fig. 2, by connecting the capacitors C1 & C2 provided on panel of the trainer.

2) Switch ON the power supply for trainer.
3) Connect the CRO to the output terminals & measure the frequency of oscillations practically.
4) Repeat the above steps by selecting another pair of capacitors C1 & C2.
5) Draw the oscillations obtained on a graph sheet.

Observations:

Hartley Oscillator

S. No.	C	L1	L2	$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$	T	f = 1/T

Colpitts Oscillator

S. No.	C1	C2	L	$f_0 = \frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{LC_1C_2}}$	T	f = 1/T

Results: The operation of Hartley & Colpitts oscillator circuits is studied, & their frequency of oscillations is verified with the theoretical values.

Experiment No: 10

Applications of Operational Amplifier

Aim: To study the Operational amplifier as Adder, Subtractor, Comparator, Integrator & Differentiator.

Components and Equipments required: IC741, Regulated DC power supply (2), Resistors (10 kΩ (4), 1kΩ (2)), Capacitors (0.01 µF (2)), Multimeter, Signal generator, CRO, CRO probes, Bread board and connecting wires.

Theory: The Operational amplifier (Op-amp) is a high gain, direct coupled, differential amplifier with high input resistance & low output resistance. It is named so as it can be used to perform a number of mathematical operations, like addition, subtraction, comparison, integration & differentiation etc.

A circuit in which the output voltage is sum of the inputs is called an adder.
A circuit in which the output voltage is difference between the inputs is called a subtractor.
A circuit which compares an input with a reference voltage is called a comparator.
A circuit in which the output voltage is the integral of the input is called an integrator.
A circuit in which the output voltage is the derivative of the input is called a differentiator.

Part-1: Adder, Subtractor & Comparator

Circuit Diagrams:

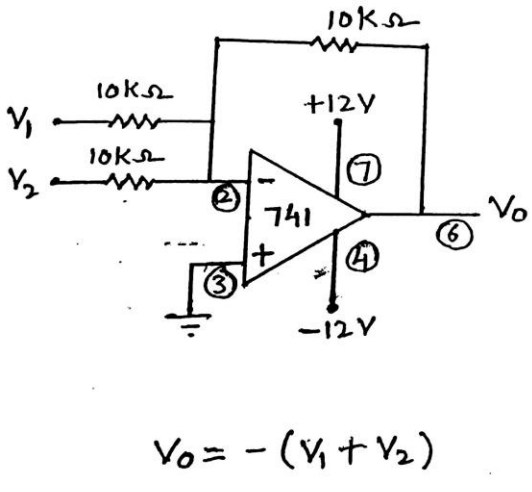


Figure 1: Inverting Adder

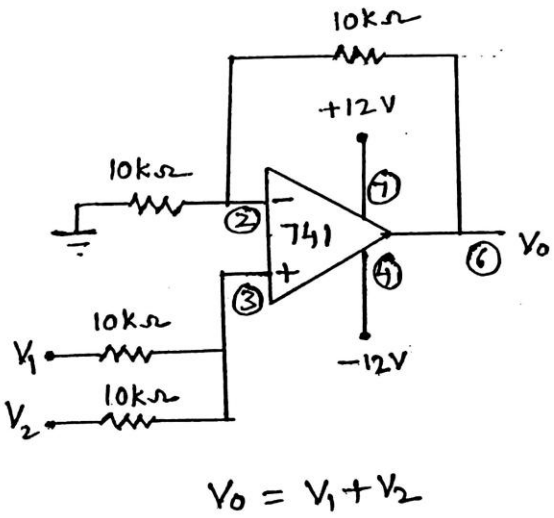


Figure 2: Non-inverting Adder

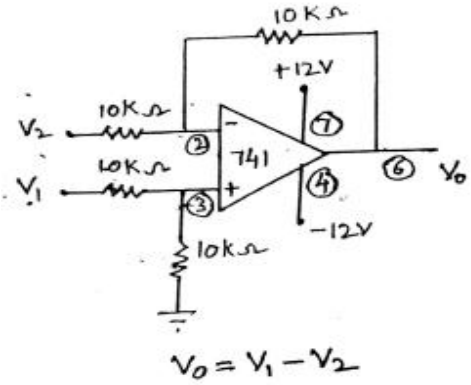


Figure 3: Subtractor

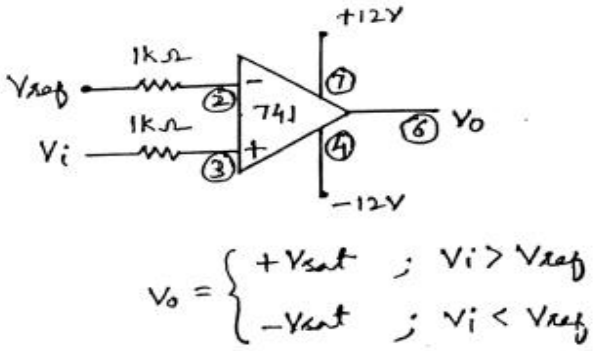


Figure 4: Comparator

Procedure:

1. Connect the circuits as shown in Fig. 1, Fig. 2, Fig. 3 & Fig. 4.
2. Apply the inputs from a regulated power supply.
3. Measure the output voltage using a multimeter.
4. Repeat the above steps for different values of inputs.

Observations:

Inverting Adder

S. No.	V_1	V_2	V_o

Non-inverting Adder

S. No.	V_1	V_2	V_o

Subtractor

S. No.	V_1	V_2	V_o

Comparator

S. No.	V_1	V_2	V_o

Part-2: Integrator & Differentiator

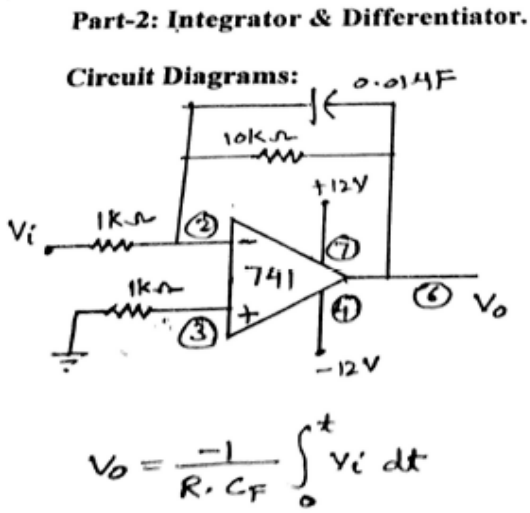


Figure 5: Integrator

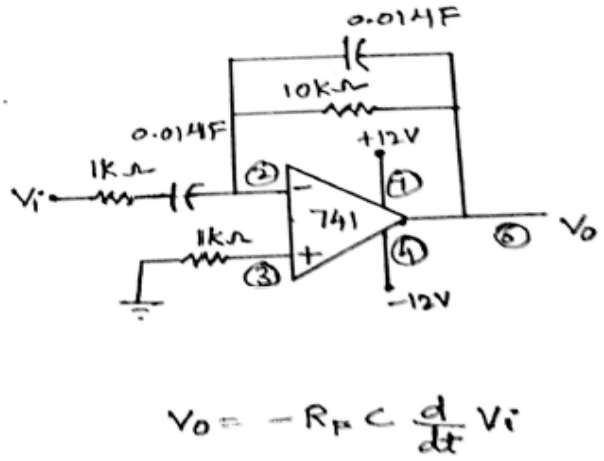


Figure 6: Differentiator

Procedure:

1. Connect the circuits as shown in Fig. 5 & Fig. 6.
2. Apply a square wave of 3 kHz frequency from Function generator, as input to the Integrator. Observe the output waveform.
3. Apply a triangular wave of 3 kHz frequency from Function generator, as input to the Differentiator. Observe the output waveform.
4. Draw the input & output waveforms for above circuits on a graph sheet.

Expected Waveforms:

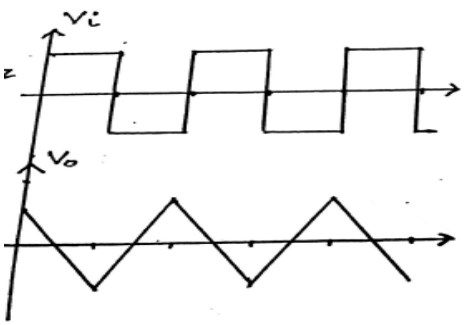


Figure 7: Integrator

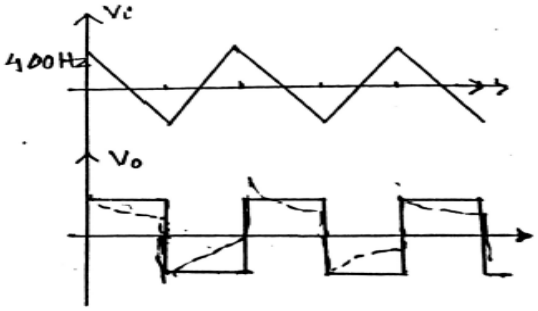


Figure 8: Differentiator

Results: The Operational amplifier is studied as Adder, Subtractor, Comparator, Integrator & Differentiator, and their outputs are verified.

Experiment No: 11

Truth Table verification of Logic Gates

Aim: To verify the truth tables of various logic Gates.

Components and Equipments required: Digital IC trainer kit, IC's (7400, 7402, 7404, 7408, 7432 & 7486) & connecting wires.

Theory:

Digital circuits are implemented using logic gates. The basic logical operations are performed by NOT, AND, OR gates.

NAND, NOR (the complements of AND, OR gates respectively) are the universal gates as any logic can be implemented using only NAND or only NOR.

NOT .gate complements the input.

AND gate gives logic 1 as output only if all of its inputs are at logic 1.

OR gate gives logic 0 as output only if all of its inputs are at logic 0.

NAND gate gives logic 0 as output only if all of its inputs are at logic 1.

NOR gate gives logic 1 as output only if all of its inputs are at logic 0.

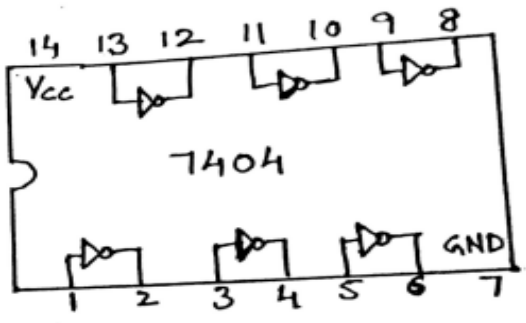
Ex-OR gate gives logic 1 output if the two inputs are dissimilar.

Truth Tables & IC Diagrams:

NOT Gate:

X	Y
0	1
1	0

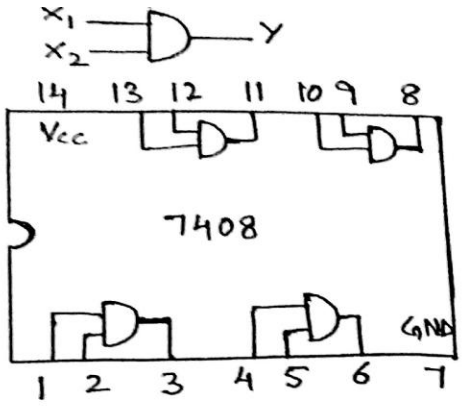
$Y = \overline{X}$



AND Gate:

x_1	x_2	Y
0	0	0
0	1	0
1	0	0
1	1	1

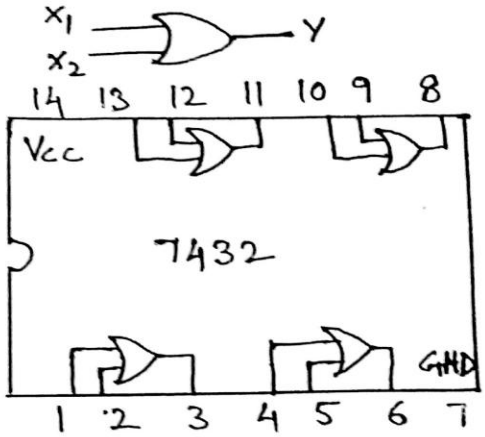
$Y = x_1 \cdot x_2$



OR Gate:

x_1	x_2	Y
0	0	0
0	1	1
1	0	1
1	1	1

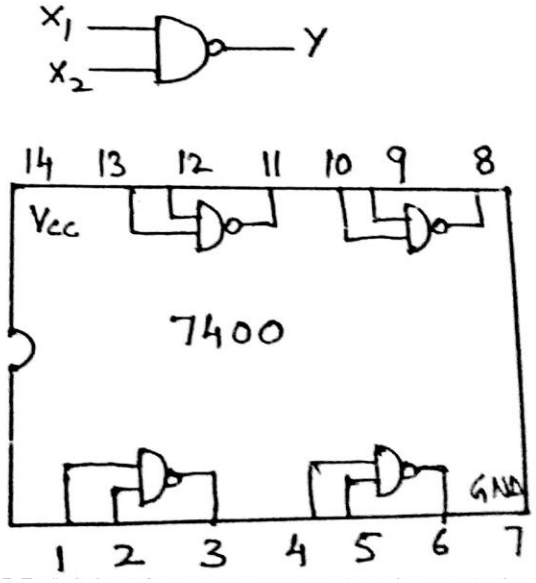
$Y = x_1 + x_2$



NAND Gate:

X_1	X_2	Y
0	0	1
0	1	1
1	0	1
1	1	0

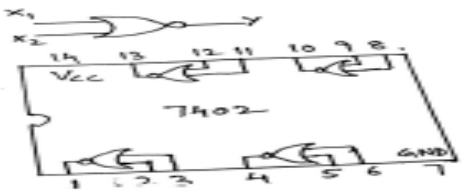
$Y = \overline{X_1 \cdot X_2}$



NOR Gate:

X_1	X_2	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{X_1 + X_2}$

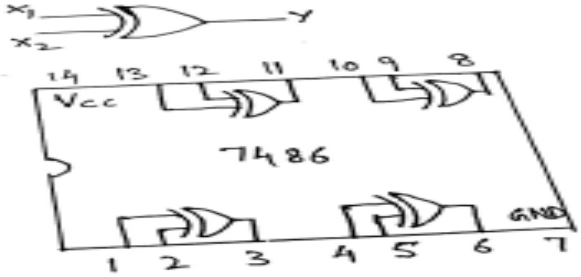


Ex-OR Gate:

X_1	X_2	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A \cdot \overline{B} + \overline{A} \cdot B$

$= A \oplus B$



Procedure:

1. Connect the IC's on the trainer kit.
2. Connect Vcc = 5V & GND to pin 14 & 7 respectively.
3. Apply inputs to the logic gates from switches block of the trainer kit.
4. Verify output of the logic gates at LED indicators of the trainer kit.
5. Repeat the steps 3 & 4 for all the gates present in the IC.

Results: The truth tables of various logic Gates are verified.

Experiment No: 12

Combinational circuits

Aim: To verify the truth tables of Half Adder, Full Adder & 8X1 MUX.

Components and Equipments required: Digital IC trainer kit, IC's (7400 (3), & 74151) & connecting wires.

Theory:

Half Adder is a combinational circuit which adds the two binary inputs (A & B) to produce sum (S = A Ex-or B) & carry (cy = A.B).

Full Adder is a combinational circuit which adds the three binary inputs (A, B & C) to produce sum (sum = A Ex-or B Ex-or C) & carry (cy = A.B+B.C+C.A).

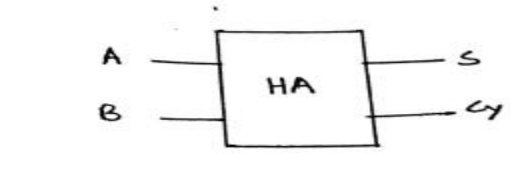
Multiplexer is a combinational circuit in which an input data line is connected to the output through select lines.

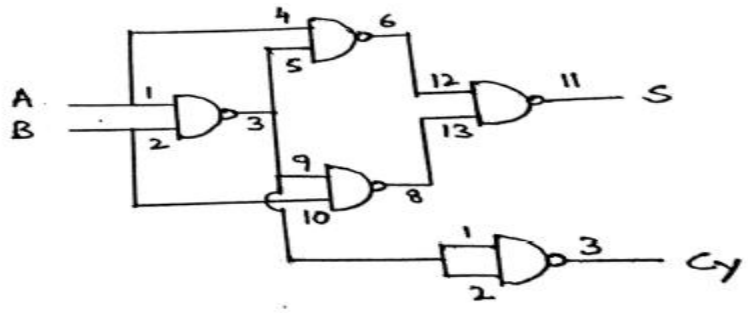
Truth Tables & Circuit Diagrams:

A	B	S	Cy
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A \oplus B$

$Cy = A \cdot B$



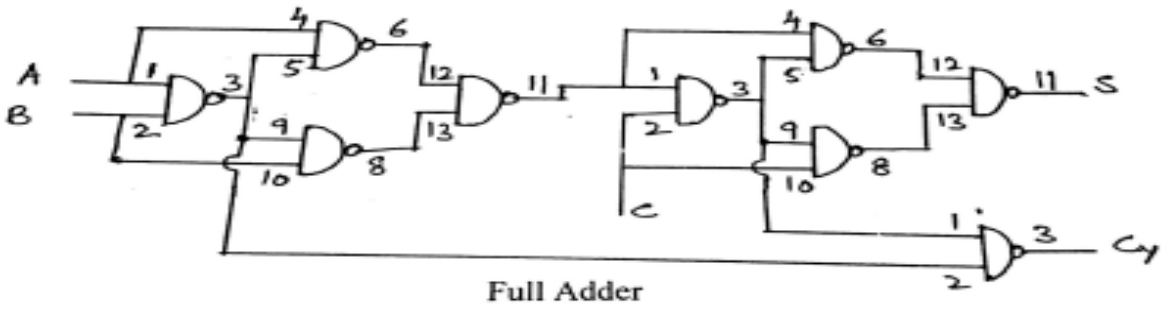


Half Adder

$S = A \oplus B \oplus C$

$Cy = A.B + B.C + C.A$

A	B	C	S	Cy
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Full Adder

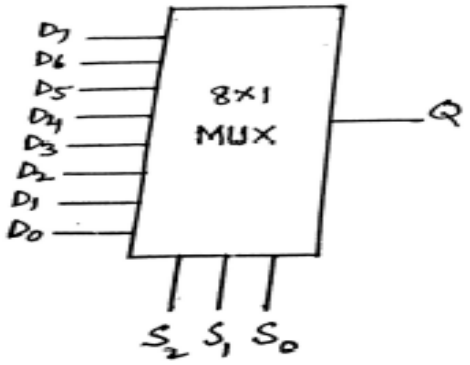
Part-1: Half Adder, Full Adder.

Procedure:

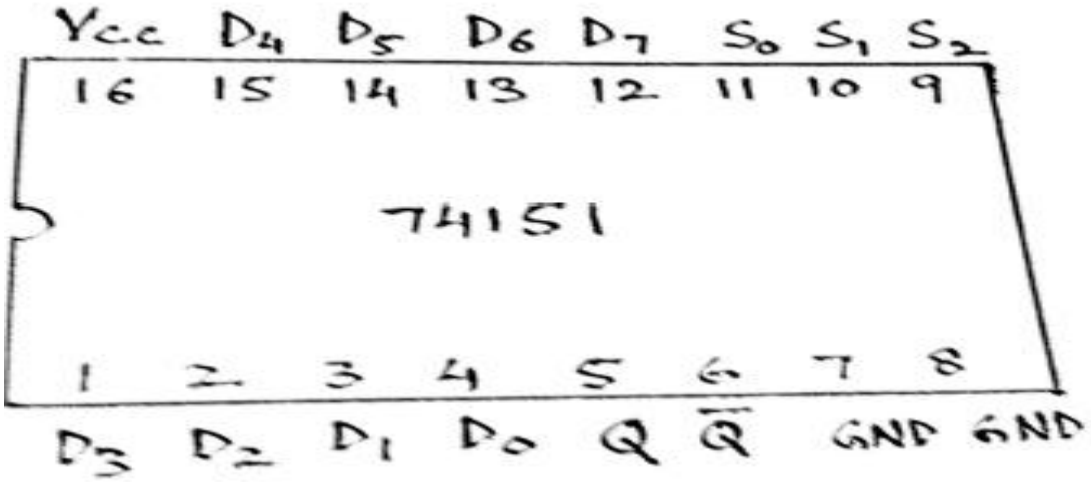
1) Connect the 7400 IC's on the trainer kit.
2) Make the connections as per the circuit diagrams.
3) Connect Vcc = 5V & GND to pin 14 & 7 respectively.
4) Apply inputs from switches block of the trainer kit.
5) Verify output at LED indicators of the trainer kit.

Part-2: 8X1 Multiplexer.

Truth Table & IC Diagram:



S_2	S_1	S_0	Q
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7



Procedure:

1) Connect the 74151 IC on the trainer kit.
2) Connect Vcc = 5V & GND to the respective pins.
3) Apply the select line inputs & the data lines from switches block of the trainer kit.
4) Verify output at LED indicators of the trainer kit.

Results: The truth tables of Half Adder, Full Adder & 8X1 MUX are verified.

Experiment No: 13

Sequential Circuits

Aim:

i) To verify the truth tables of D Flip-flop & Decade Counter.

ii) To study the working of Shift registers.

Components and Equipments required:

i) Digital IC trainer kit, D flip flop (IC 7474), Decade Counter (IC 7490) & connecting wires.

ii) Shift register trainer kit & connecting wires.

Theory:

Sequential circuits are those in which the output depends on the present inputs & the past outputs. Sequential circuits usually consist of Logic gates & memory devices like flip flops.

Delay Flip-flop is a special case of S-R Flip-flop or J-K Flip-flop, in which the output is the present input. It is used to store 1 bit data.

A Decade counter is a sequential circuit which counts the decimal digits i.e; 0 to 9.

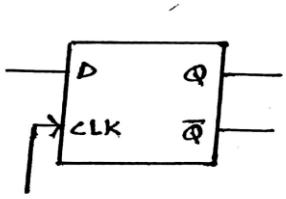
A Shift register is a sequential circuit which is generally used to convert data bits from parallel to serial form (PISO) & vice versa (SIPO). It is also used to shift data either in right or left directions.

Truth Tables & Circuit Diagrams:

D Flip-flop.

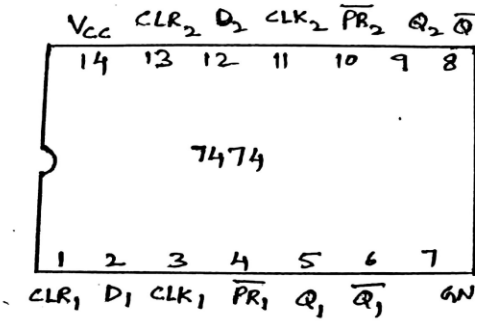
D Flip-flop:

Truth Table & IC Diagram:



D	Q
0	0
1	1

$Q = D$



Procedure:

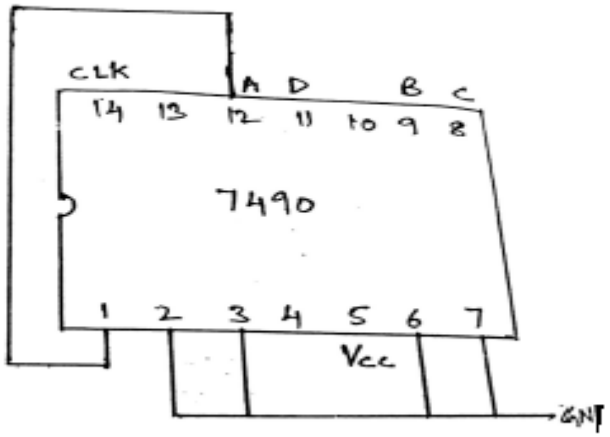
1) Connect the 7474 IC on the trainer kit.
2) Connect Vcc = 5V & GND to the respective pins.
3) Apply logic 1 for preset & clear inputs of Flip-flop.
4) Apply the D input & the clk from respective blocks at the trainer kit.
5) Verify output at LED indicators of the trainer kit.
6) Repeat steps 3 to 5 for the second flip flop of the IC.

Decade Counter.

Decade Counter:

Truth Table & IC Diagram:

A	B	C	D	Output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

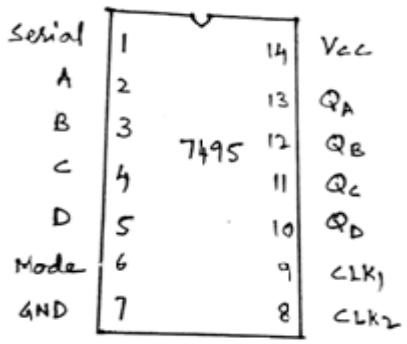


Decade Counter

Procedure:

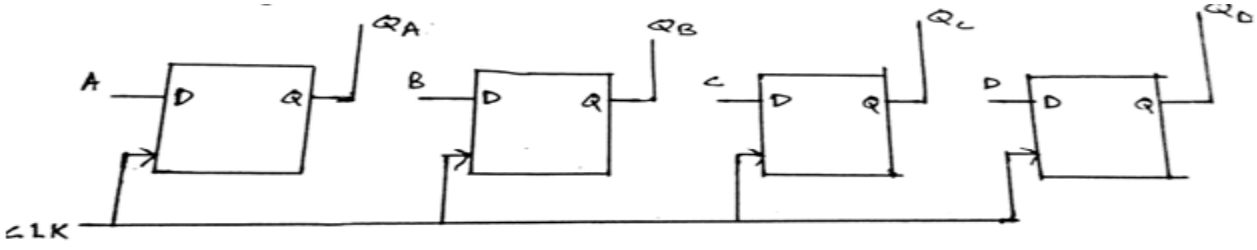
1) Connect the 7490 IC on the trainer kit.
2) Connect Vcc = 5V & GND to respective pins.
3) Apply the clk input and short the pins 1 & 12..
4) Connect the pins 8, 9, 11 & 12 of 7490 to the respective slots of 7 segment display at the trainer kit.
5) Observe the output at LED indicators & the 7 segment display.

Shift Registers using IC 7495



PIPO:

Circuit Diagram:



PIPO

Procedure:

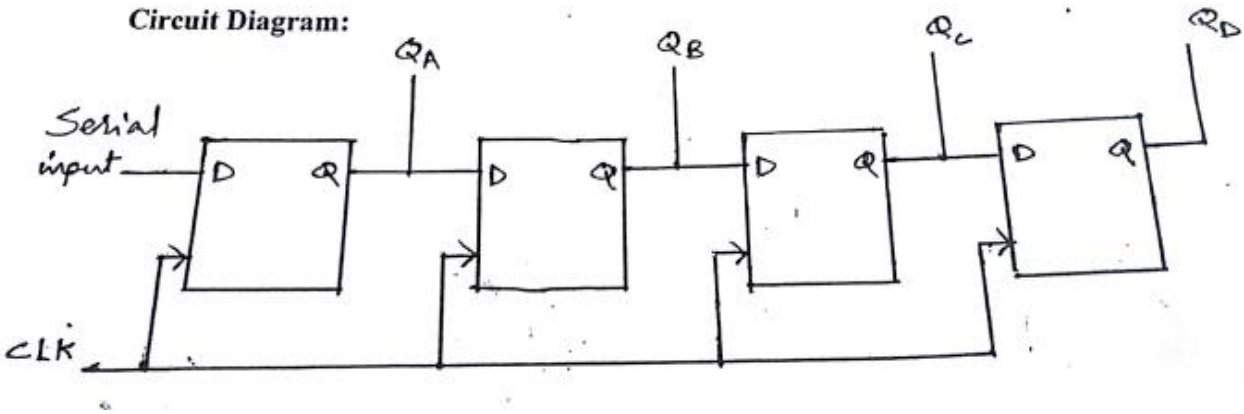
1) Connect the inputs A, B, C & D from switches block of the trainer kit.
2) Connect outputs Q_A, Q_B, Q_C & Q_D to LED indicators on the trainer kit.
3) Apply Logic 1 at MODE input of the IC.
4) Connect the clock from respective block on the trainer kit at clk2 input of the IC.
5) Now switch ON the trainer kit.
6) Apply different input values at A, B, C & D to verify the output at LED indicators.

Observations:

Mode	CLK_2	A	B	C	D	Q_A	Q_B	Q_C	Q_D
1	⊓	a_1	b_1	c_1	d_1	a_1	b_1	c_1	d_1
		a_2	b_2	c_2	d_2	a_2	b_2	c_2	d_2
		a_3	b_3	c_3	d_3	a_3	b_3	c_3	d_3

SIPO (Shift Right):

Circuit Diagram:

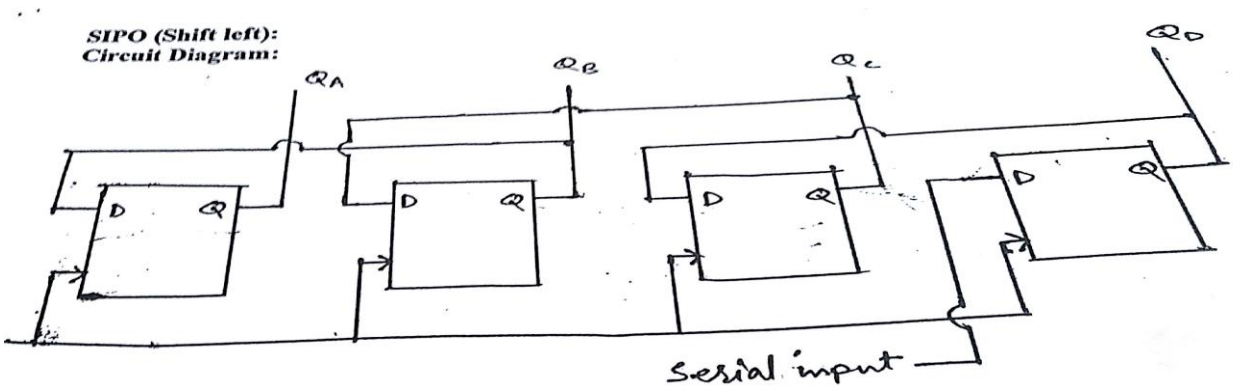


Procedure:

1) Connect the serial input from switches block of the trainer kit at pin 1 of the IC.
2) Connect outputs Q_A, Q_B, Q_C & Q_D to LED indicators on the trainer kit.
3) Apply Logic 0 at MODE input of the IC.
4) Connect the clock from respective block on the trainer kit at clk1 input of the IC.
5) Now switch ON the trainer kit.
6) Apply a sequence of input 1000 at pin 1 & verify the output at LED indicators.

Observations:

Mode	CLK_1	Serial input	Q_A	Q_B	Q_C	Q_D
			0	0	0	0
		1 (D_0)	D_0	0	0	0
		0 (D_1)	D_1	D_0	0	0
		0 (D_2)	D_2	D_1	D_0	0
0	↓	0 (D_3)	D_3	D_2	D_1	D_0
			0	D_3	D_2	D_1
			0	0	D_3	D_2
			0	0	0	D_3
			0	0	0	0



Procedure:

1) Connect the serial input at D from switches block of the trainer kit.
2) Also connect Q_D to C, Q_C to B & Q_B to A.
3) Connect outputs Q_A, Q_B, Q_C & Q_D to LED indicators on the trainer kit.
4) Apply Logic 1 at MODE input of the IC.
5) Connect the clock from respective block on the trainer kit at clk2 input of the IC.
6) Now switch ON the trainer kit.
7) Apply a sequence of input 1000 at D input & verify the output at LED indicators.

Observations:

Mode	CLK_2	serial input	Q_A	Q_B	Q_C	Q_D
1	↓	1 (D_0)	0	0	0	0
		0 (D_1)	0	0	0	D_0
		0 (D_2)	0	0	D_0	D_1
		0 (D_3)	0	D_0	D_1	D_2
			D_0	D_1	D_2	D_3
			D_1	D_2	D_3	0
			D_2	D_3	0	0

Results:

i) The truth tables of D-Flip flop & Decade Counter are verified.
ii) Working of Shift Registers is verified.

ANNEXURE-I
NON-PROGRAMMING LABORATORY COURSES

i. The number of experiments in each laboratory course shall be as per the curriculum in the scheme of instructions provided by OU. Mostly the number of experiments is 10 in each laboratory course under semester scheme and 18 under year wise scheme.

ii. The students will maintain a separate note book for observations in each laboratory course.

iii. In each session the students will conduct the allotted experiment and enter the data in the observation table.

iv. The students will then complete the calculations and obtain the results. The course coordinator will certify the result in the same session.

v. The students will submit the record in the next class. The evaluation will be continuous and not cycle-wise or at semester end.

vi. The internal marks of 25 are awarded in the following manner:

a. Laboratory record - Maximum Marks 15
b. Test and Viva Voce - Maximum Marks 10

vii. Laboratory Record: Each experimental record is evaluated for a score of 50. **The rubric parameters are as follows:**

a. Write up format - Maximum Score 15
b. Experimentation Observations & Calculations - Maximum Score 20
c. Results and Graphs - Maximum Score 10
d. Discussion of results - Maximum Score 5

While (a), (c) and (d) are assessed at the time of record submission, (b) is assessed during the session based on the observations and calculations. Hence if a student is absent for an experiment but completes it in another session and subsequently submits the record, it shall be evaluated for a score of 30 and not 50.

viii. The experiment evaluation rubric is therefore as follows:

Parameter	Max Score	Outstanding	Accomplished	Developing	Beginner	Points
Observations & Calculations	20					
Write up format	15					
Results & graphs	10					
Discussion of Results	5					

LABORATORY EXPERIMENT EVALUATION RUBRIC

CATEGORY	OUTSTANDING (Up to 100%)	ACCOMPLISHED (Up to 75%)	DEVELOPING (Up to 50%)	BEGINNER (Up to 25%)
Write up format	Aim, Apparatus, material requirement, theoretical basis, procedure of experiment, sketch of the experimental setup etc. is demarcated and presented in clearly labeled and neatly organized sections.	The write up follows the specified format but a couple of the specified parameters are missing.	The report follows the specified format but a few of the formats are missing and the experimental sketch is not included in the report	The write up does not follow the specified format and the presentation is shabby.
Observations and Calculations	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures. One sample calculation is explained by substitution of values	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures but sample calculation is not shown	The experimental observations and calculations are recorded neatly but correct units and significant figures are not used. Sample calculation is also not shown	The experimental observations and results are recorded carelessly. Correct units significant figures are not followed and sample calculations not shown
Results and Graphs	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations are performed from the graphs. Equations are obtained by regression analysis or curve fitting if relevant	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations from the graphs are incomplete and equations are not obtained by regression analysis or curve fitting	Results obtained are correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting	Results obtained are not correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting
Discussion of results	All relevant points of the result are discussed and justified in light of theoretical expectations. Reasons for divergent results are identified and corrective measures discussed.	Results are discussed but no theoretical reference is mentioned. Divergent results are identified but no satisfactory reasoning is given for the same.	Discussion of results is incomplete and divergent results are not identified.	Neither relevant points of the results are discussed nor divergent results identified

ix. The first page of the record will contain the following title sheet:

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGHY
LABORATORY EXPERIMENT ASSESSMENT SHEET
INFORMATION TECHNOLOGY DEPARTMENT
B.E. 2/4 I SEMESTER 2015-2016
BASIC ELECTRONICS -I LABORATORY

NAME: **ROLL NO.**

Exp. No.	Title of the Experiment	Date conducted	Date Submitted	Observations & Calculations (Max 20)	Write up (Max 15)	Results and Graphs (Max 10)	Discussion of Results (Max 5)	Total Score (Max 50)
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
	TOTAL							

Date: **Signature of Course Coordinator**

x. The 15 marks of laboratory record will be scaled down from the TOTAL of the assessment sheet.

xi. The test and viva voce will be scored for 10 marks as follows:

Internal Test	-	6 marks
Viva Voce / Quiz	-	4 marks

xii. Each laboratory course shall have 5 course outcomes.

The proposed course outcomes are as follows:

On successful completion of the course, the student will acquire the ability to:

1. Conduct experiments, take measurements and analyze the data through hands-on experience in order to demonstrate understanding of the theoretical concepts of _____, while working in small groups.

2. Demonstrate writing skills through clear laboratory reports.

3. Employ graphics packages for drawing of graphs and use computational software for statistical analysis of data.

4. Compare the experimental results with those introduced in lecture, draw relevant conclusions and substantiate them satisfactorily.

5. Transfer group experience to individual performance of experiments and demonstrate effective oral communication skills.

xiii. The Course coordinators would prepare the assessment matrix in accordance with the guidelines provided above for the five course outcomes. The scores to be entered against each of the course outcome would be the sum of the following as obtained from the assessment sheet in the record:

a. Course Outcome 1: Sum of the scores under ‘Observations and Calculations’.
b. Course Outcome 2: Sum of the scores under ‘Write up’.
c. Course Outcome 3: Sum of the scores under ‘Results and Graphs’.
d. Course Outcome 4: Sum of the scores under ‘Discussion of Results’.
e. Course Outcome 5: Marks for ‘Internal Test and Viva voce’.

xiv. Soft copy of the assessment matrix would be provided to the course coordinators.

ANNEXURE-II
UNIVERSITY SYLLABUS

BIT 231

BASIC ELECTROINICS LABORATORY

Instruction	3 Periods Per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessionals	25 Marks

Course Objectives:

1. To study the electronics components.
2. To study characteristics of semi-conductor devices and design rectifiers, filters and amplifiers.
3. To study simple electronic circuits.

List of Experiments

ANALOG:

1. CRO and its applications: Measurement of amplitude, frequency. Obtaining transfer characteristics and lissajous figures. Determination of unknown frequency using CRO.
2. Characteristics of pn junction diode , zener diode, BJT and FET. Applications: Half-wave and full-wave rectifiers, clipping and clamping circuits, BJT and FET as switches
3. Frequency response of Common Emitter amplifier
4. Hartley, colpitts and RC phase shift oscillators
5. Operational Amplifier as an adder, sub tractor, differentiator, integrator and comparator

DIGITAL:

6. Truth table verification of logic gates using TTL 74 series ICs. Transfer characteristics of a TTL gate using CRO.
7. Half Adder, Full Adder, Decoder, MUX, implementation of Boolean logic using decoders and MUXes.
8. Truth table verification of D flip flop, T flip-flop and JK flip-flop.
9. Counters.
10. Shift Registers.

SOFTWARE:

Any 3 experiments using PSPICE.

Note: All the experiments are compulsory