

24-bit Audio CODEC

數位電路實驗

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Outline

- Introduction to Audio Signal
- Architecture Overview
- Device Initialization
- Device Operation

Introduction to Audio Signal

Introduction

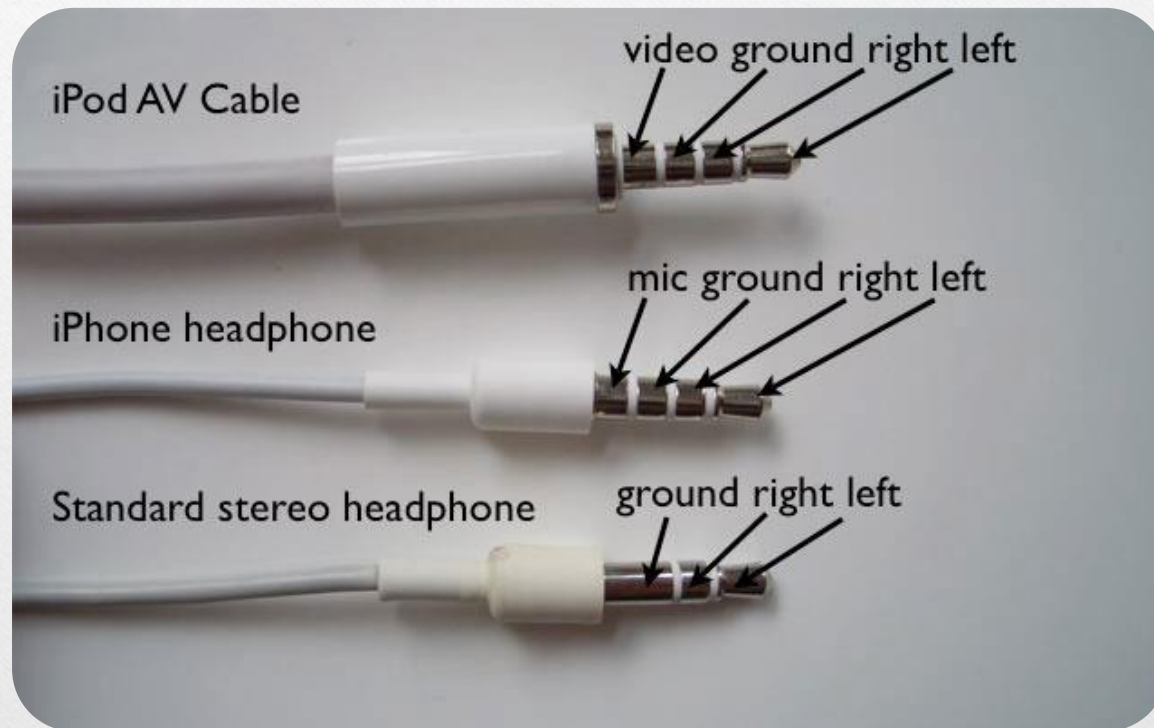
- An audio signal = electrical voltage.
- **Headphones** convert electrical signals into sound.
- **Microphones** convert sound into electrical signals.
- Audio signals have frequencies in the audio frequency range of roughly **20 to 20,000 Hz**.

Line In V.S. Mic In

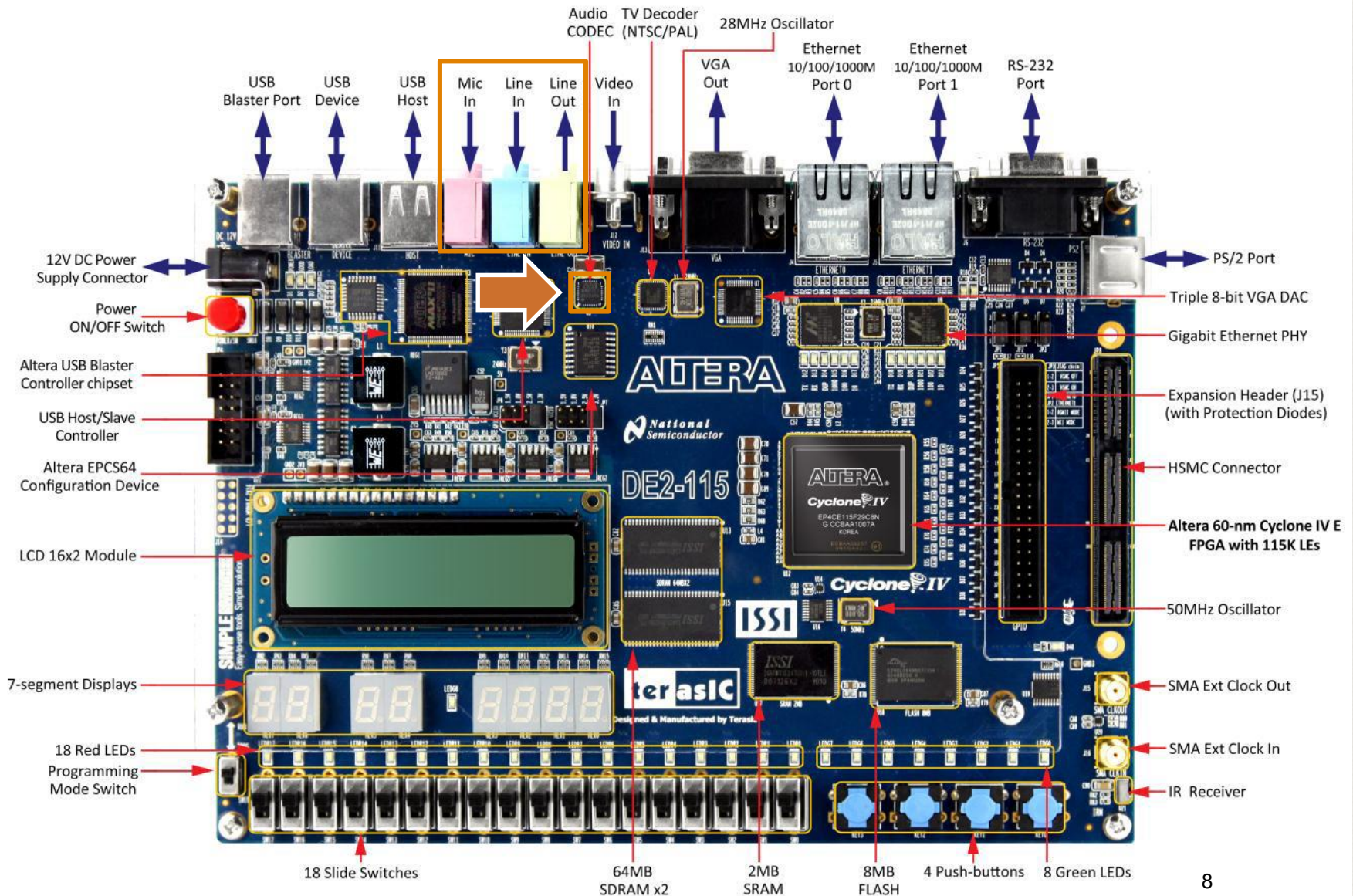
- Line input/output: 0.3 to 2 Volts.
- Microphone input: 5 to 50 mV.
- ADC is required to convert Voltage to 00101010



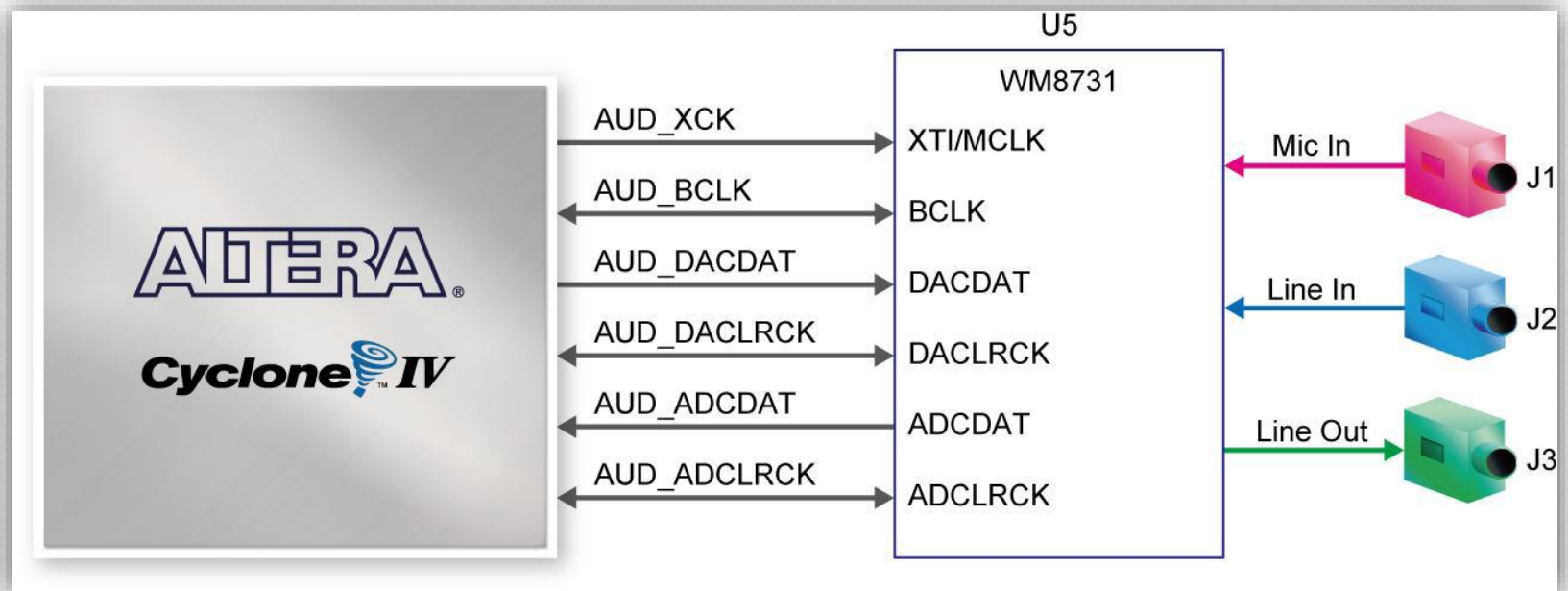
Dual Channel



Architecture Overview



Schematic Diagram



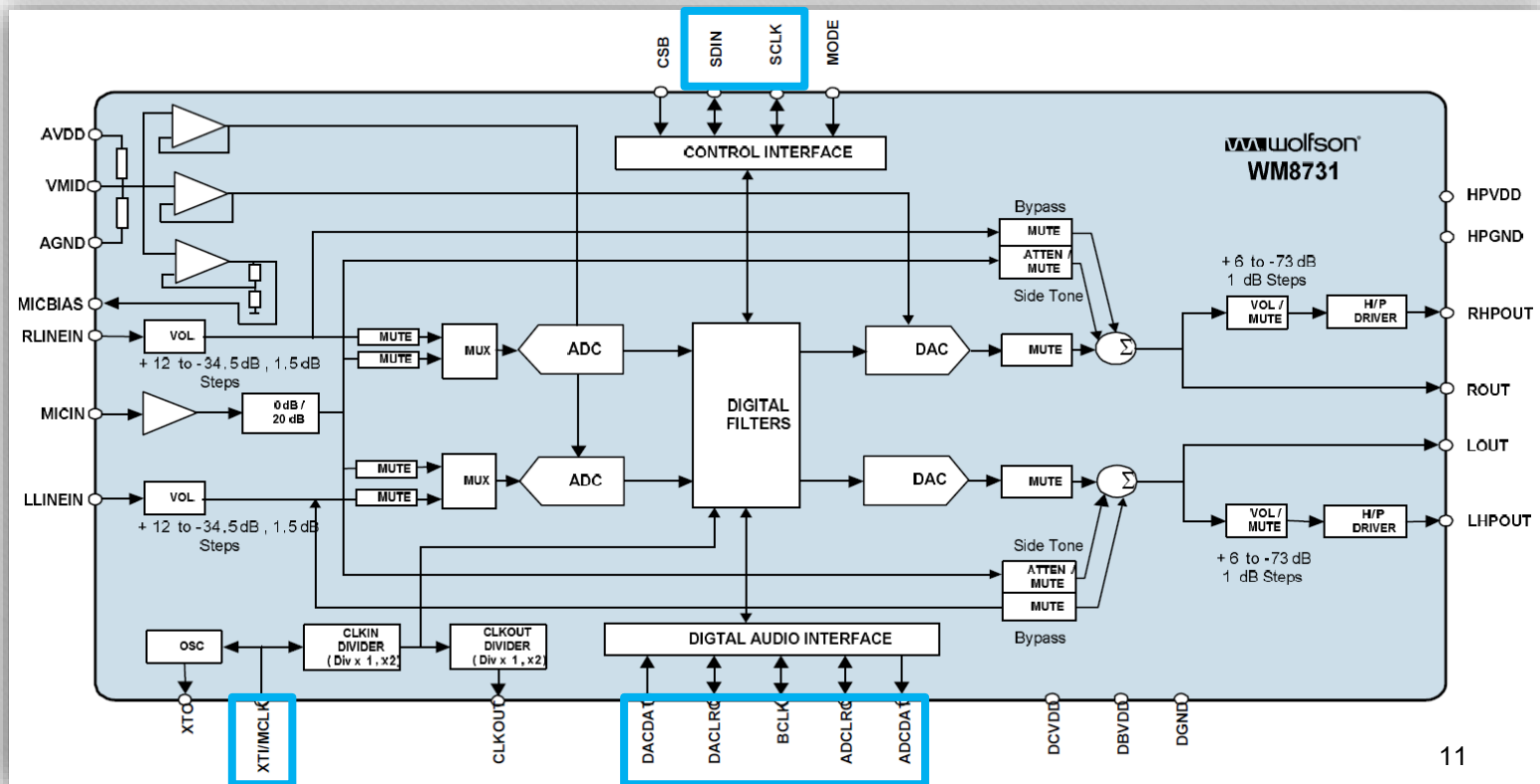
Audio CODEC Pin Assignments

Signal Name	FPGA Pin No.	Description
I2C_SCLK	PIN_B7	I2C Clock
I2C_SDAT	PIN_A8	I2C Data
AUD_XCK	PIN_E1	Audio CODEC Chip Clock
AUD_BCLK	PIN_F2	Audio CODEC Bit-Stream Clock
AUD_ADCLRCK	PIN_C2	Audio CODEC ADC LR Clock
AUD_ADCDAT	PIN_D2	Audio CODEC ADC Data
AUD_DACLK	PIN_E3	Audio CODEC DAC LR Clock
AUD_DACDAT	PIN_D1	Audio CODEC DAC Data

Control

Data

WM8731 Block Diagram

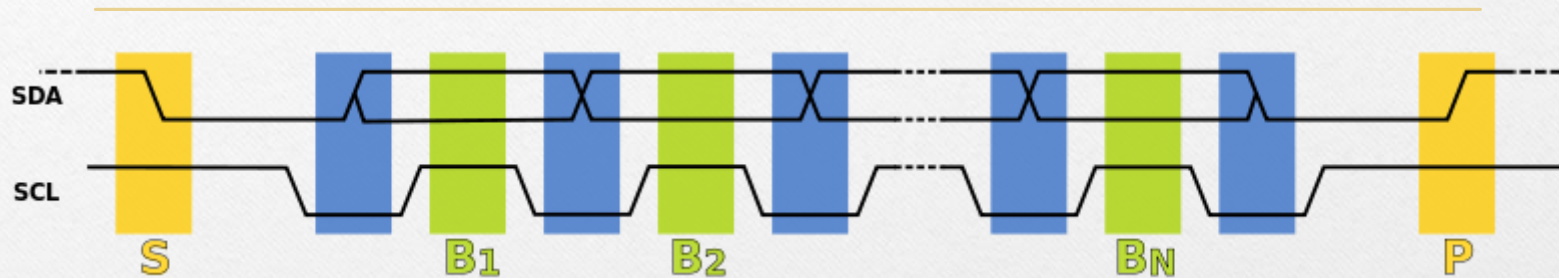


How to Use WM8731?

1. Initialize the device by setting the registers via I2C bus interface.
2. After correct initialization, we can receive or transmit audio data via digital audio interface.

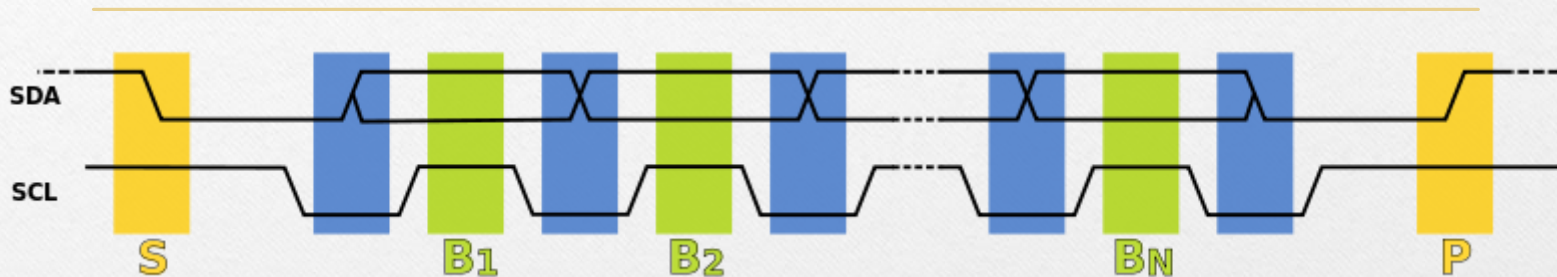
Device Initialization

I²C Protocol (1/4)



- Data transfer is initiated with the START bit (**S**) when SDA is **pulled low** while SCL stays high.
SDA=1'b0
- Then, SDA sets the transferred bit while SCL is low (**blue**) and the data is sampled (received) when SCL rises (**green**).

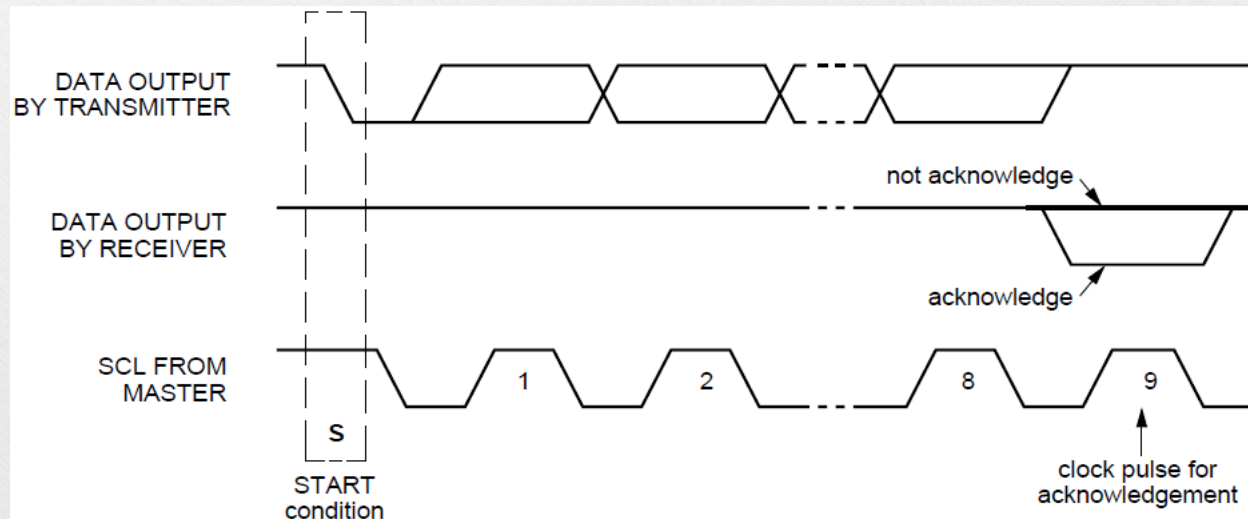
I²C Protocol (2/4)



- When the transfer is complete, a STOP bit (P) is sent by **releasing** the data line to allow it to be pulled up while SCL is constantly high. *SDA=1'b1 or SDA=1'bz*
- In order to avoid false marker detection, the level on SDA is changed on the **falling edge** and is captured on the **rising edge** of SCL.

I²C Protocol (3/4)

- After every 8 data bits in one direction, an "acknowledge" bit (0) is transmitted in the other direction.



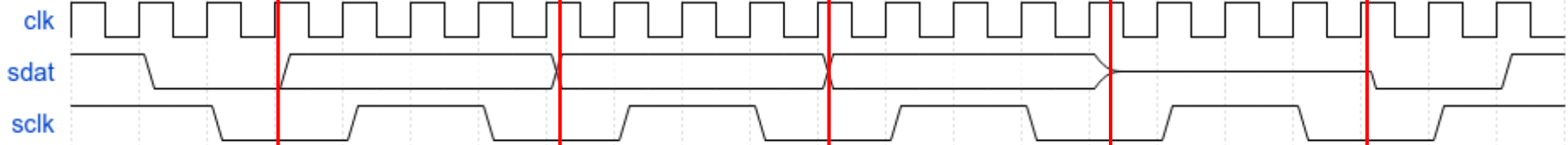
I²C Protocol (4/4)

- Inout port example:

```
input in_dat;  
input clk;  
input out_enable;  
output logic out_r;  
logic out_w;  
  
assign out_dat = out_enable ? out_r : 1'bz;  
  
always_ff @(posedge clk) begin  
    out_r <= in_dat;  
end
```

Workable I²C Protocol

- 4/cycle bit, 1 ack bit/byte
- 3+3 cycles header
- #Cycles is required for N-Bytes?
- (This is not the full specification.)



Software Control Interface (1/2)

- Different modes can be configured under software control.
 - Input to ADC: Microphone
 - Sampling rate: 32kHz
 - Input audio data bit length: 16 bits
 - etc.

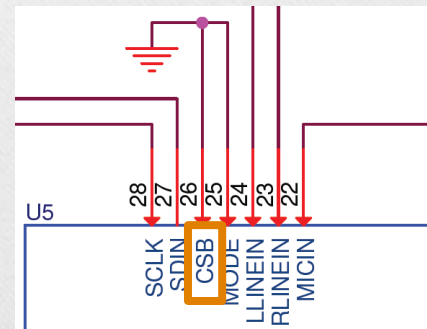
2-Wire Serial Control Mode

- The WM8731/L supports a 2-wire MPU (Microprocessor unit) interface, which is compatible with I²C protocol.
 - I²C (Inter-Integrated Circuit, referred to as I-squared-C) uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL).

2-Wire Interface (1/2)

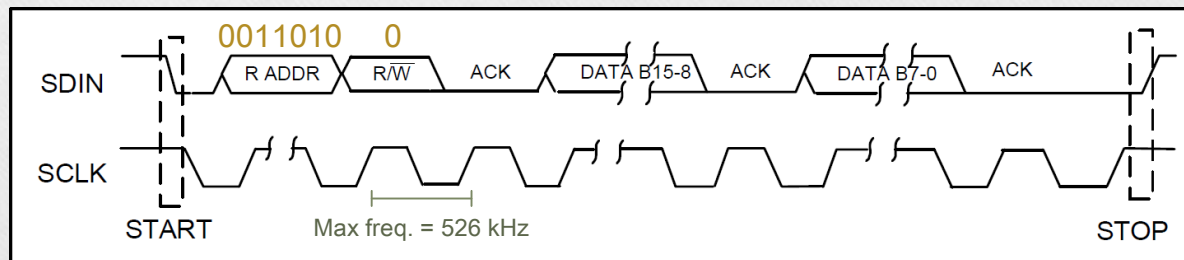
- The device operates as a **slave device** only.
- The WM8731/L has one of two slave address that are selected by setting the state of the **CSB** pin.

CSB STATE	ADDRESS
0	0011010
1	0011011



2-Wire Interface (2/2)

- 2-wire serial interface
 - ADDR[6:0] (7 bits) are Slave Address Bits
 - R/W is '0', indicating a write
 - B[15:9] (7 bits) are Register Address Bits
 - B[8:0] (9 bits) are Register Data Bits



Register Map

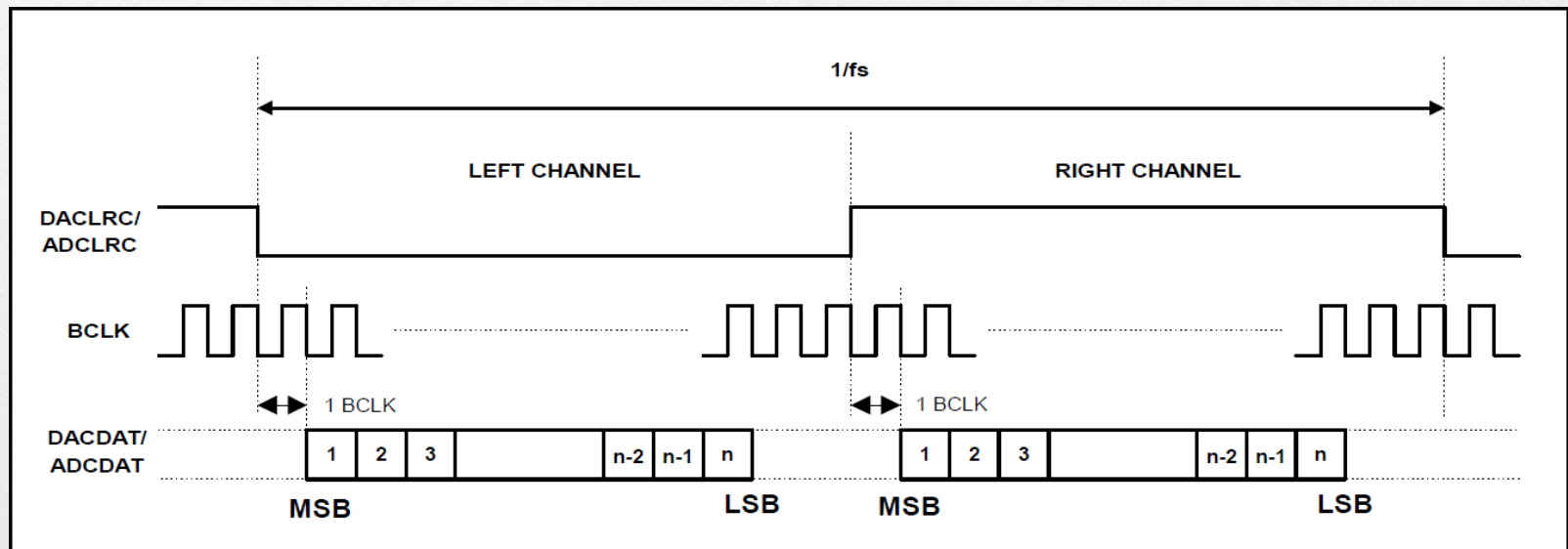
REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R0 (00h) Left Line In	LRINBOTH	LINMUTE	0	0	LINVOL[4:0]					0_1001_0111
R1 (01h) Right Line In	RLINBOTH	RINMUTE	0	0	RINVOL[4:0]					0_1001_0111
R2 (02h) Left Headphone Out	LRHPBOTH	LZCEN	LHPVOL[6:0]						0_0111_1001	
R1 (01h) Right Headphone Out	RLHPBOTH	RZCEN	RHPVOL[6:0]						0_0111_1001	
R4 (04h) Analogue Audio Path Control	0	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST	0_0000_1010
R5 (05h) Digital Audio Path Control	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADCHPD	0_0000_1000
R6 (06h) Power Down Control	0	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	0_1001_1111
R7 (07h) Digital Audio Interface Format	0	BCLKINV	MS	LRSWAP	LRP	IWL[1:0]		FORMAT[1:0]		0_1001_1111
R8 (08h) Sampling Control	0	CLKODIV2	CLKIDIV2	SR[3:0]				BOSR	USB/ NORMAL	0_0000_0000
R9 (09h) Active Control	0	0	0	0	0	0	0	0	Active	0_0000_0000
R15 (0Fh) Reset	RESET[8:0]									not reset

Digital Audio Interfaces

- WM8731/L may be operated in either one of the 4 offered audio interface modes. These are:
 - Right justified
 - Left justified
 - I²S
 - DSP mode

Digital Audio Interface Format

- I²S format

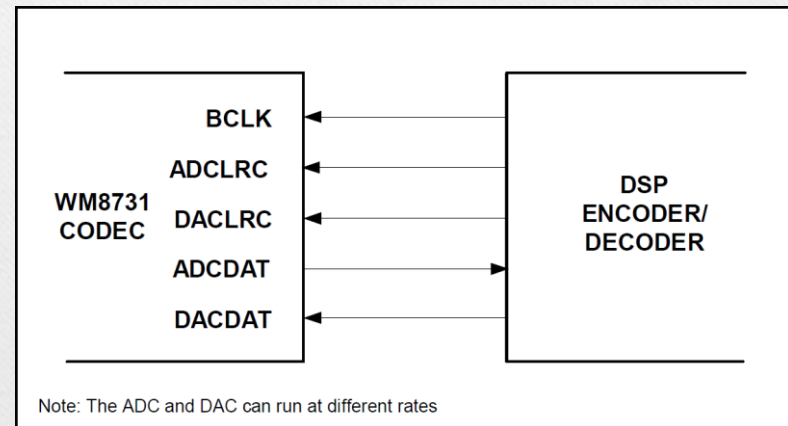
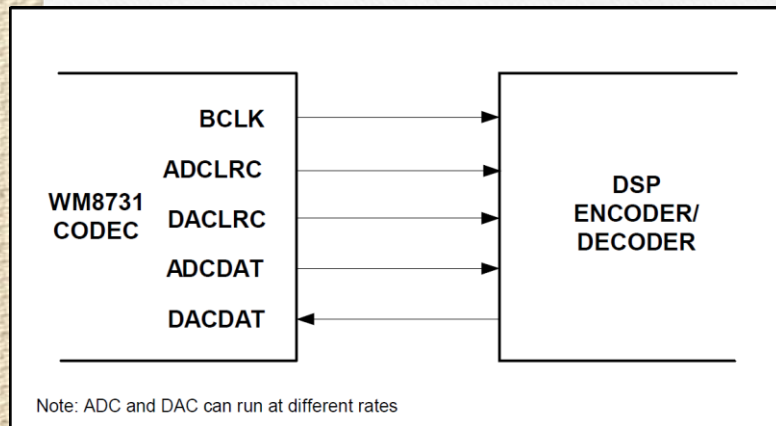


Digital Audio Interfaces

- The length of the digital audio data is programmable at 16/20/24 or 32 bits.
- The data is signed 2's complement.
 - -32768~32767
 - `logic signed [15:0] dat;`

Digital Audio Interface Format

- Master mode v.s. Slave mode



Digital Audio Interface Format (1/2)

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R7 (07h) Digital Audio Interface Format	0	BCLKIVE	MS	LRSWAP	LRP	IWL[[1:0]		FORMAT[1:0]		0_0000_1010

- Choose I²S format, 16-bit length, and master mode.
 - 000_0111_0_0100_0010

Recommended I²C Settings

Left Line In	000_0000_0_1001_0111
Right Line In	000_0001_0_1001_0111
Left Headphone Out	000_0010_0_0111_1001
Right Headphone Out	000_0011_0_0111_1001
Analogue Audio Path Control	000_0100_0_0001_0101
Digital Audio Path Control	000_0101_0_0000_0000
Power Down Control	000_0110_0_0000_0000
Digital Audio Interface Format	000_0111_0_0100_0010
Sampling Control	000_1000_0_0001_1001
Active Control	000_1001_0_0000_0001

The End.

Any question?

Reference

1. http://en.wikipedia.org/wiki/Audio_signal
2. <http://en.wikipedia.org/wiki/I%C2%B2C>
3. "THE I 2C-BUS SPECIFICATION VERSION 2.1" by Philips.
4. "DE2-115 User Manual" by Terasic.
5. "DE2-115_MB.pdf" by Terasic.
6. "WM8731.pdf" by Wolfson Microelectronics.

Appendix

Left Line In

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R0 (00h) Left Line In	LRINBOTH	LINMUTE	0	0	LINVOL[4:0]					0_1001_0111

- Just use the default setting if we do not use the line input.
 - 000_0000_0_1001_0111

Right Line In

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R1 (01h) Right Line In	RLINBOTH	RINMUTE	0	0	RINVOL[4:0]					0_1001_0111

- Just use the default setting if we do not use the line input.
 - 000_0001_0_1001_0111

Left Headphone Out

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R2 (02h) Left Headphone Out	LRHPBOTH	LZCEN	LHPVOL[6:0]							0_0111_1001

- Here we can just use the default setting.
 - 000_0010_0_0111_1001

Right Headphone Out

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R3 (03h) Right Headphone Out	RLHPBOTH	RZCEN	RHPVOL[6:0]							0_0111_1001

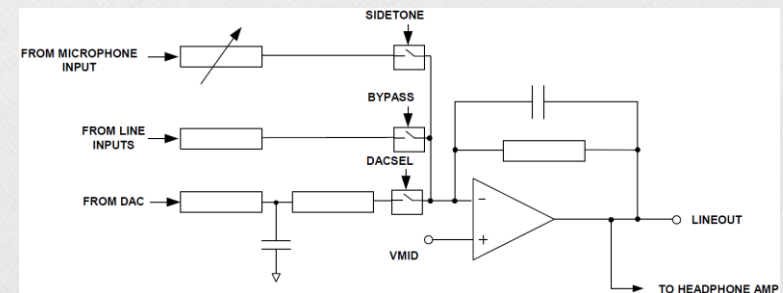
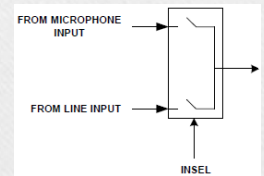
- Here we can just use the default setting.
 - 000_0011_0_0111_1001

Analogue Audio Path Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R4 (04h) Analogue Audio Path Control	0	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST	0_0000_1010

- Enable boost, disable mute, choose microphone input, disable bypass, and select DAC.

- 000_0100_0_0001_0101



Digital Audio Path Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R5 (05h) Digital Audio Path Control	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADCHPD	0_0000_1000

- Disable soft mute
 - 000_0101_0_0000_0000

Power Down Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R6 (06h) Power Down Control	0	POWER OFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	0_1001_1111

- Choose power on and disable all the power down options.
 - 000_0110_0_0000_0000

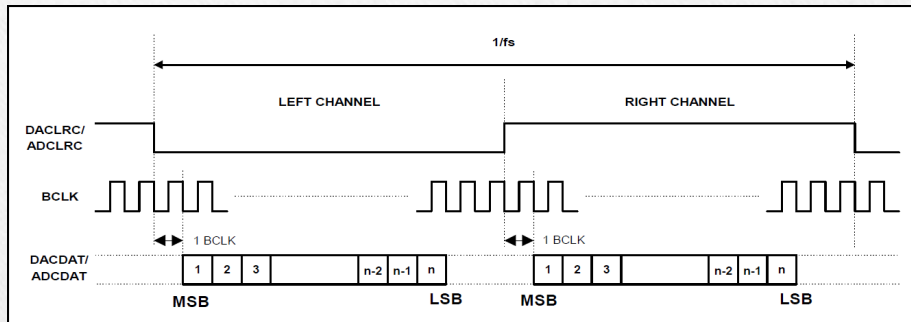
Digital Audio Interface Format (1/2)

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R7 (07h) Digital Audio Interface Format	0	BCLKIVE	MS	LRSWAP	LRP	IWL[[1:0]		FORMAT[1:0]		0_0000_1010

- Choose I²S format, 16-bit length, and master mode.
 - 000_0111_0_0100_0010

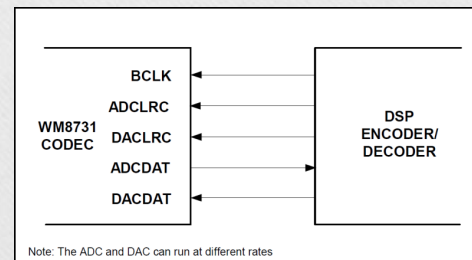
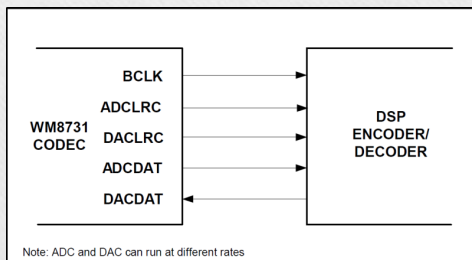
Digital Audio Interface Format (2/2)

- I²S format



➤ 16-bit length

- Master mode v.s. Slave mode



Sampling Control (1/2)

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R8 (08h) Sampling Control	0	CLKODIV2	CLKIDIV2	SR[3:0]				BOSR	USB/ Normal	0_0000_0000

- Choose USB mode (fixed MCLK 12MHz) and sampling rate = 32 kHz.
 - 000_1000_0_0001_1001

Sampling Control (2/2)

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC		REGISTER SETTINGS					
kHz	kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	48	12.000	0	0	0	0	0	0
44.1 (Note 2)	44.1 (Note 2)	12.000	1	1	0	0	0	1
48	8	12.000	0	0	0	0	1	0
44.1 (Note 2)	8 (Note 1)	12.000	1	1	0	0	1	1
8	48	12.000	0	0	0	1	0	0
8 (Note 1)	44.1 (Note 2)	12.000	1	1	0	1	0	1
8	8	12.000	0	0	0	1	1	0
8 (Note 1)	8 (Note 1)	12.000	1	1	0	1	1	1
32	32	12.000	0	0	1	1	0	0
96	96	12.000	0	0	1	1	1	3
88.2 (Note 3)	88.2 (Note 3)	12.000	1	1	1	1	1	2

Active Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R9 (09h) Active Control	0	0	0	0	0	0	0	0	Active	0_0000_0000

- Activate interface
 - 000_1001_0_0000_0001

Reset Register

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R15 (15h) Active Control	RESET[8:0]									not reset

- You can try to reset the device to a known (?) state.
 - 000_1111_0_0000_0000 (?)